MAPS-010164

Digital Phase Shifter
6-Bit, 2.3 - 3.8 GHz

Rev. V3

Features

- 6 Bit Digital Phase Shifter
- 360° Coverage with LSB = 5.6°
- Integrated CMOS Driver
- Serial or Parallel Control
- Low DC Power Consumption
- Minimal Attenuation Variation over Phase Shift Range
- 50 Ω Impedance
- EAR99
- Lead-Free 4 mm 24-Lead PQFN Package
- RoHS* Compliant

Description

The MAPS-010164 is a GaAs pHEMT 6-bit digital phase shifter with an integrated CMOS driver in a 4 mm PQFN plastic surface mount package. Step size is 5.6° providing phase shift from 0° to 360° in 5.6° steps. This design has been optimized to minimize variation in attenuation over the phase shift range.

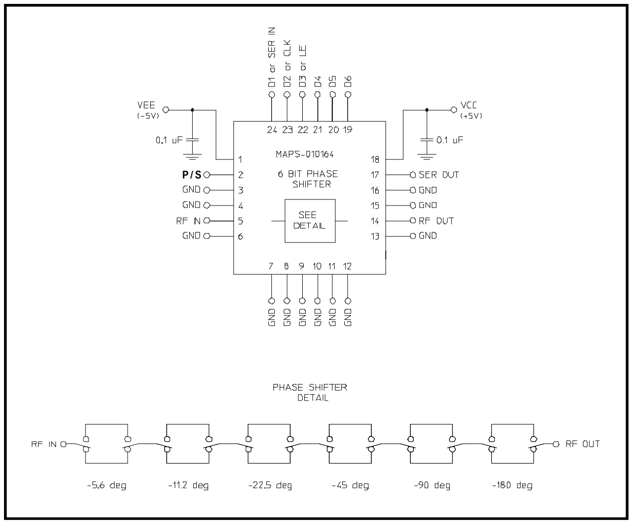
The MAPS-010164 is ideally suited for use where high phase accuracy with minimum loss variation over the phase shift range are required. The 4 mm PQFN package provides a smaller footprint than is typically available for a digital phase shifter with an internal driver. Typical applications include communications antennas and phased array radars.

Ordering Information [1]

Part Number	Package
MAPS-010164-TR0500	500 piece reel
MAPS-010164-001SMB	Sample Test Board

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration [2]

Pin No.	Function	Pin No.	Function
1	VEE	13	GND
2	P/S	14	RF OUT
3	GND	15	GND
4	GND	16	GND
5	RF IN	17	SER OUT
6	GND	18	VCC
7	GND	19	D6
8	GND	20	D5
9	GND	21	D4
10	GND	22	D3 or LE
11	GND	23	D2 or CLK
12	GND	24	D1 or SER IN

2. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Electrical Specifications:
Freq. = 2.3 - 3.8 GHz, T_A = 25°C, Z_0 = 50 Ω, V_{CC} = +5.0 V, V_{EE} = -5.0 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Operating Power [3]	2.3 - 3.8 GHz	dBm	—	—	+25
Insertion Loss (Any Phase State)	Any Phase State	dB	—	3.2	4.5
Attenuation Variation	Across All Phase States	dB	—	± 0.6	—
RMS Attenuation Error [4]	All Values Relative to Insertion Loss at Reference Phase	dB	—	0.3	—
RMS Phase Error [4]	All Values Relative to Reference Phase	deg	—	3	—
Phase Accuracy Relative to Reference Loss State	5.6 Degree Bit 11.2 Degree Bit 22.5 Degree Bit 45 Degree Bit 90 Degree Bit 180 Degree Bit Sum of All Bits	deg	— — — — — — —	± 1.5 ± 1.5 ± 2 ± 2 ± 3 ± 4 ± 5	— — — — — — —
VSWR	RF IN RF OUT	Ratio	— —	1.3:1 1.3:1	— —
1 dB Compression	Reference State	dBm	—	25	—
Input IP3	Two-tone inputs up to +5 dBm	dBm	—	45	—
T_{RISE}, T_{FALL}	10% to 90% RF, 90% to 10% RF	ns	—	50	—
V_{CC} V_{EE}	— —	V	3.0 -5.5	— -5.0	5.5 -3.0
V_{IL} V_{IH}	LOW-level input voltage HIGH-level input voltage	V	0.0 0.7 x V_{CC}	— —	0.3 x V_{CC} V_{CC}
I_{IN} (Input Control Current)	V_{IN} = V_{CC} or GND	µA	—	1	—
V_{OH} V_{OL}	For serial out; I_{OH} = -100 µA For serial out; I_{OL} = 100 µA	V	V_{CC} - 0.2 —	— —	— 0.2
Icc (Quiescent Supply Current)	Vcntrl = V_{CC} or GND	µA	—	—	2.5
I_{EE}	V_{EE} min to max Vin = V_{IL} or V_{IH}	mA	-1.0	-0.1	—

3. Maximum operating power is the maximum power where the specifications are guaranteed.
4. RMS is calculated across all 63 amplitude or phase states relative to the amplitude or phase in the 0° phase state at a given frequency.

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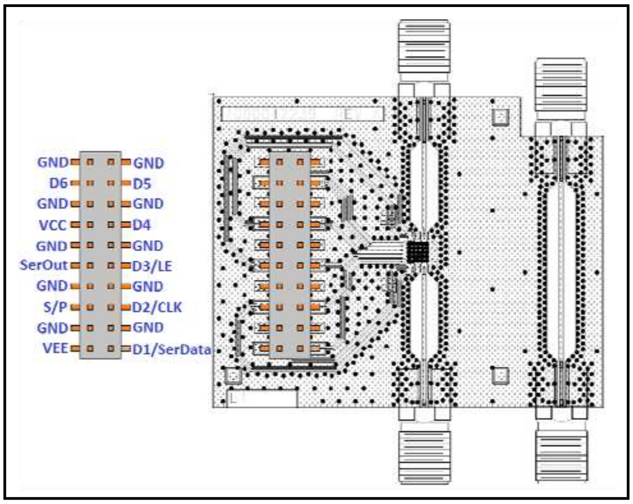
Absolute Maximum Ratings [5,6]

Parameter	Absolute Maximum
Input Power 2.3 - 3.8 GHz	+27 dBm
V_{CC}	$-0.5V \le V_{CC} \le +7.0V$
V_{EE}	$-7.0V \le V_{EE} \le +0.5V$
D1-D6, P/S, LE, CLK or SER IN	$-0.5V \le V_{IN} \le VCC + 0.5V$
SER OUT	$-0.5V \le V_{OUT} \le V_{CC} + 0.5V$
Operating Temperature	-40ºC to +85ºC
Storage Temperature	-65ºC to +150ºC

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. M/A-COM Technology Solutions does not recommend sustained operation near these survivability limits.

Sample Board Header Pin Labels



Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide and Silicon Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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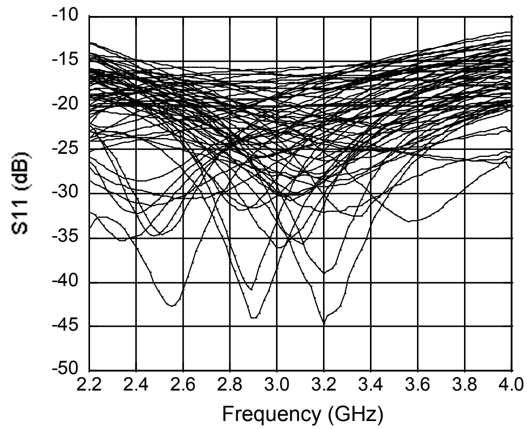
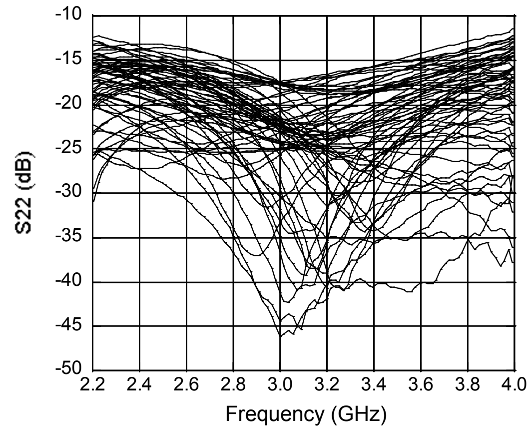
Typical Performance Curves

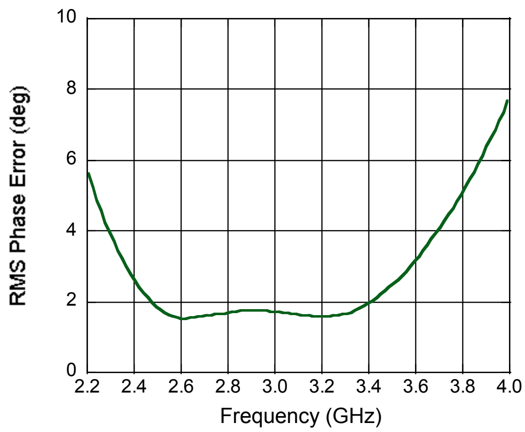
RF_{IN} Return Loss vs. Frequency (All States)



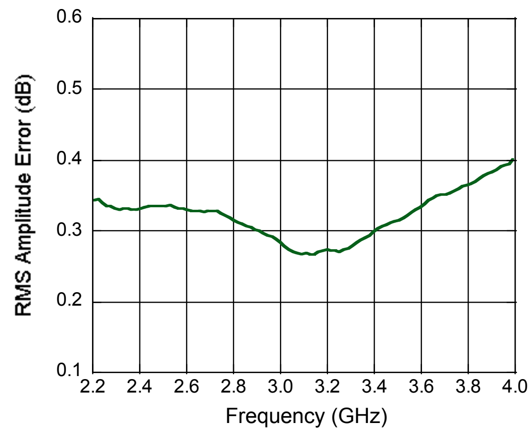
RF_{OUT} Return Loss vs. Frequency (All States)



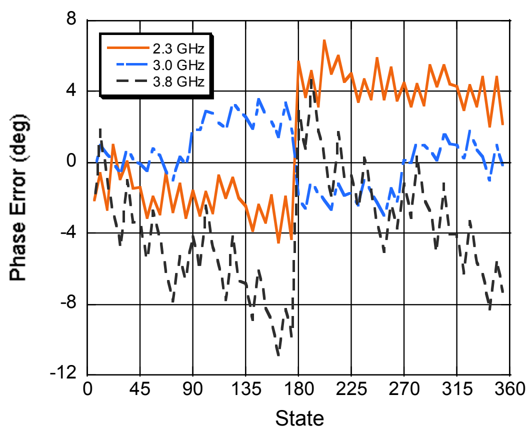
Mean RMS Phase Error vs. Frequency



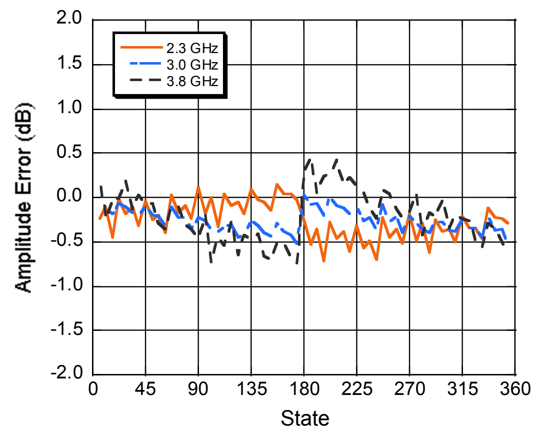
Mean RMS Amplitude Error vs. Frequency



Phase Error (degrees) vs. State

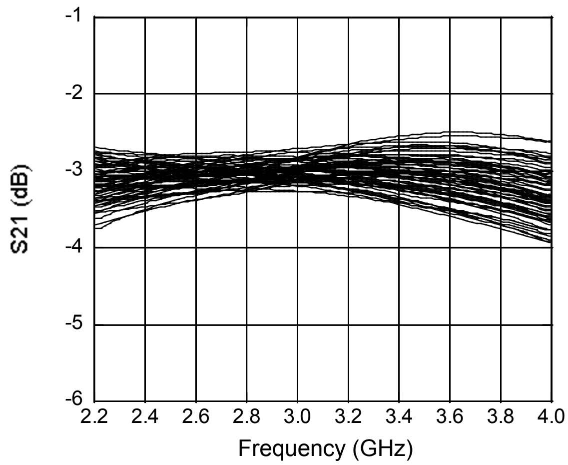


Amplitude Error (dB) vs. State

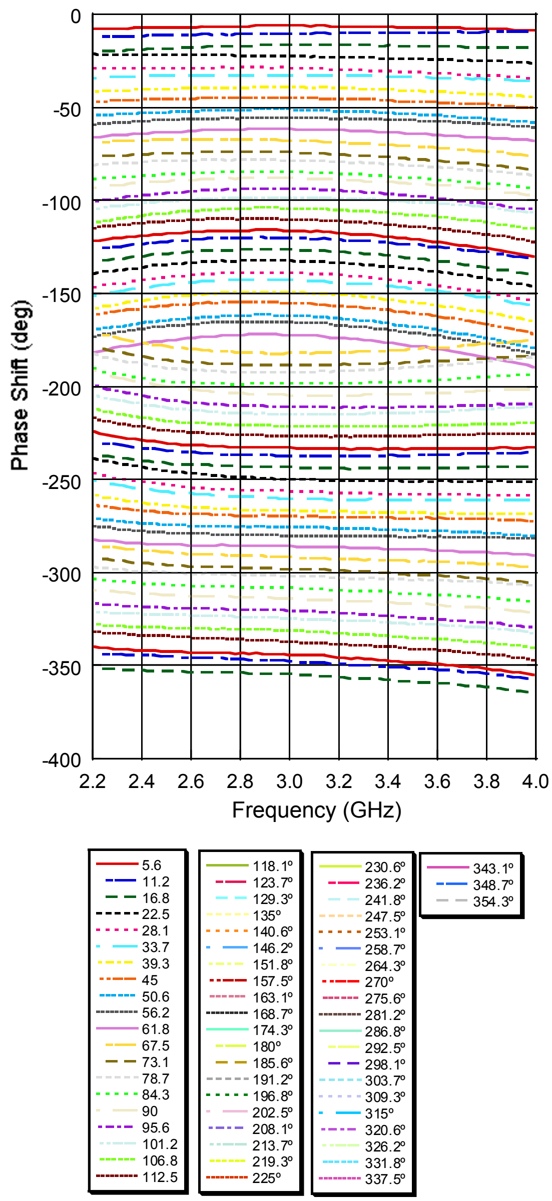


Typical Performance Curves

Amplitude Variation vs. Phase State



Phase Shift vs. Frequency (All States)



Modes of Operation:
Serial and Direct Parallel

Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with the MSB first. After shifting in the 6 bit word, a rising edge on LE will set the phase shifter to the desired state. While LE is high the CLK is masked to protect the data while implementing the change. SEROUT is SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled. When P/S is set high, Pins 22, 23, and 24 have the LE, CLK, and SER IN function.

In serial mode operation, the outputs will stay constant while LE is kept low.

Direct Parallel Mode

The parallel mode is enabled when P/S is set low. In the direct parallel mode, the phase shifter is controlled by the parallel control inputs directly. When P/S is set low, Pins 22, 23, and 24 have the D3, D2, and D1 function.

Mode Truth Table

P/S	LE	Mode
1	X	Serial
0	N/A	Direct Parallel

Truth Table (Digital Phase Shifter) [7]

D6	D5	D4	D3	D2	D1	Phase Shift
0	0	0	0	0	0	Reference Phase
0	0	0	0	0	1	5.6 deg
0	0	0	0	1	0	11.2 deg
0	0	0	1	0	0	22.5 deg
0	0	1	0	0	0	45 deg
0	1	0	0	0	0	90 deg
1	0	0	0	0	0	180 deg
1	1	1	1	1	1	354.4 deg

7. 0 = CMOS Low; 1 = CMOS High, X is CMOS Low or High

Serial Interface Timing Characteristics

Symbol	Parameter	Typical Performance			Units
		-40°C	25°C	+85°C	
t_{SCK}	Min. Serial Clock Period	100	100	100	ns
t_{CS}	Min. Control Set-up Time	20	20	20	ns
t_{CH}	Min. Control Hold Time	20	20	20	ns
t_{LS}	Min. LE Set-up Time	10	10	10	ns
t_{LEW}	Min. LE Pulse Width	10	10	10	ns
t_{LH}	Min. Serial Clock Hold Time from LE	10	10	10	ns
t_{LES}	Min. LE Pulse Spacing	630	630	630	ns

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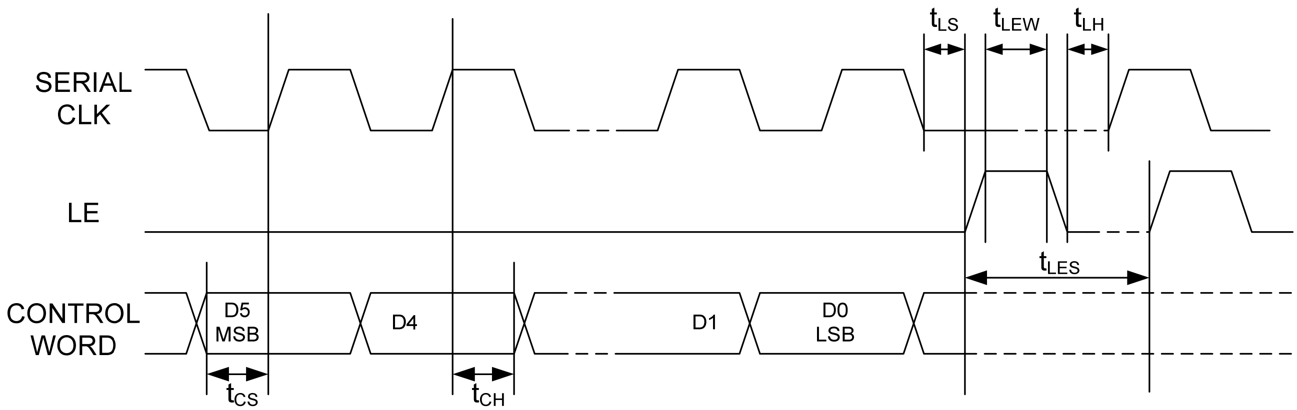
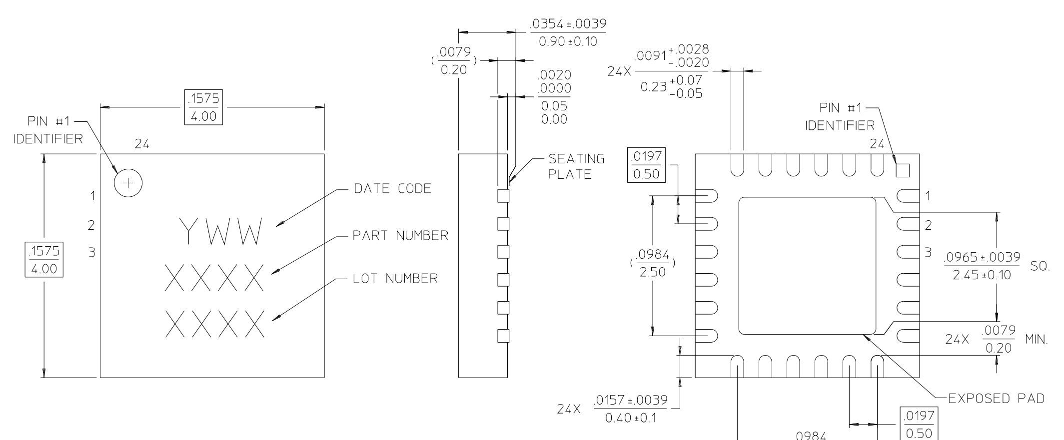
Functionality
Modes of Operation: Serial and Direct Parallel

Serial Input Interface Timing Diagram



Lead Free 4 mm 24-Lead PQFN †



NOTES:
1. REFERENCE JEDEC MO-220, VAR VGGD-2 FOR ADDITIONAL DIMENSIONS AND TOLERANCE INFORMATION.
2. REFERENCE S2083 APPLICATION NOTE FOR PCB FOOTPRINT INFORMATION.
3. ALL DIMENSIONS SHOWN AS INCHES/MM.

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.