MAUC-010515

Up Converter
40.5 - 43.5 GHz

Rev. V3

Features

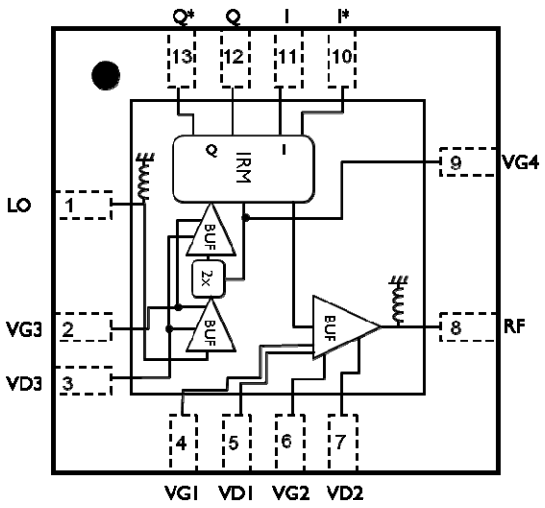
- Integrates Image Reject (Balanced) Mixer, LO Buffer, LO Doubler, and RF Buffer
- 11 dB Conversion Gain
- 30 dBm Output Third Order Intercept (OIP3)
- -15 dBm (2×) LO Leakage (at RF Port)
- Variable Gain with Adjustable Bias
- Lead-Free 6 mm Laminate Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The MAUC-010515 is an integrated USB up-converter that has a typical conversion gain of 10 dB, and an image rejection of greater than 15 dBc. The device includes a LO doubler and buffer, and can be tuned to give 2×LO leakage of less than -15 dBm. Variable gain can be achieved by adjusting the bias, with turn-down trajectories optimized to maintain linearity and 2×LO leakage over the gain control range. At full gain, an OIP3 of 30 dBm is typical. It is ideally suited for 42 GHz band point-to-point radios.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using an efficient pHEMT process.

Functional Schematic



Pin Configuration [1]

Pin No.	Function
1	LO
2	VG3
3	VD3
4	VG1
5	VD1
6	VG2
7	VD2
8	RF
9	VG4
10	I* Input
11	I Input
12	Q Input
13	Q* Input

1. The exposed pad centered on the package bottom must be connected to RF and DC ground.

Ordering Information

Part Number	Package
MAUC-010515-000000	Bulk Quantity
MAUC-010515-TR0500	500 Piece Reel
MAUC-010515-001SMB	Sample Evaluation Board

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

• **North America** Tel: 800.366.2266 • **Europe** Tel: +353.21.244.6400
• **India** Tel: +91.80.43537383 • **China** Tel: +86.21.2407.1588
Visit www.macomtech.com for additional data sheets and product information.

Up Converter
40.5 - 43.5 GHz

Electrical Specifications: RF Freq: 40.5-43.5 GHz, LO = 0 dBm, IF = -10 dBm, VD = 4 V, ID1 = ID2 = 90 mA, ID3 = 60 mA, T_A = 25°C

Parameter	Units	Min.	Typ.	Max.
Frequency Range (LO)[2]	GHz	18.5	-	21.75
Frequency Range (IF)	GHz	DC	-	3.5
LO Input Power (Plo)	dBm	0	-	8.0
Conversion Gain	dB	8.0	11.0	16.0
Image Rejection	dBc	-	22	-
Output IP3	dBm	25.0	30.0	-
Spurious (2xLO) [tuned]	dBm	-	-40	-
Spurious (1xLO)	dBm	-	-57	-
Noise Figure	dB	-	19	-
Input Return Loss (IF port)	dB	-	12	-
Output Return Loss (RF Port)	dB	-	8	-
LO Return Loss	dB	-	15	-
Current[3] (ID1 + ID2 + ID3)	mA	-	240	400
Gate Voltage (VG4)	V	-	-3	-
Gate Current (IG4)	mA	-	4.0	-

2. LO frequency range limits the performance characteristics to USB only.
3. Adjust VG1, VG2, VG3 between –1.0 and –0.1 V to achieve specified current. Typical 240 mA = 90 (ID1) + 90 (ID2) + 60 (ID3)

Absolute Maximum Ratings [4,5,6]

Parameter	Absolute Max.
Drain Voltage	+4.3 V
Gate Bias Voltage (VG1,2,3)	-1.5V < VG < 0V
Gate Bias Voltage (VG4)	-4.0V < VG < 0V
Input Power	+10 dBm
LO Input Power	+13 dBm
Storage Temperature	-55°C to +150°C
Operating Temperature	-40°C to +85°C
Junction Temperature[7]	150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. M/A-COM Technology Solutions does not recommend sustained operation near these survivability limits.
6. Operating at nominal conditions with $T_J \leq 150°C$ will ensure MTTF > 1 x 10^6 hours.
7. Junction Temperature (T_J) = $T_C + \Theta_{jc} * (V * I)$
   Typical thermal resistance (Θ_{jc}) = 40° C/W.
   a) For T_C = 25°C, T_J = 64°C @ 4 V, 240 mA
   b) For T_C = 85°C, T_J = 124°C @ 4 V, 240 mA

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Human Body Model Class 1B and Machine Model Class B devices.

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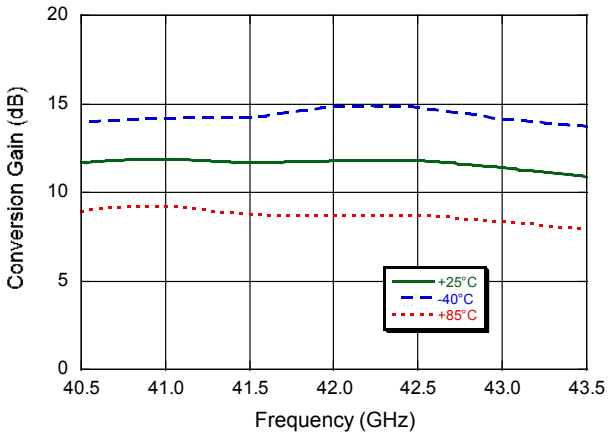
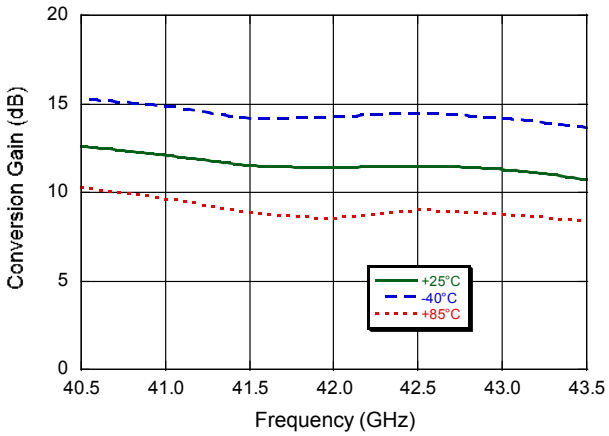
Typical Performance Curves: VD = 4 V, ID1 = ID2 = 90 mA, ID3 = 60 mA, LO = 0 dBm, IF = -10 dBm, T_A = 25°C

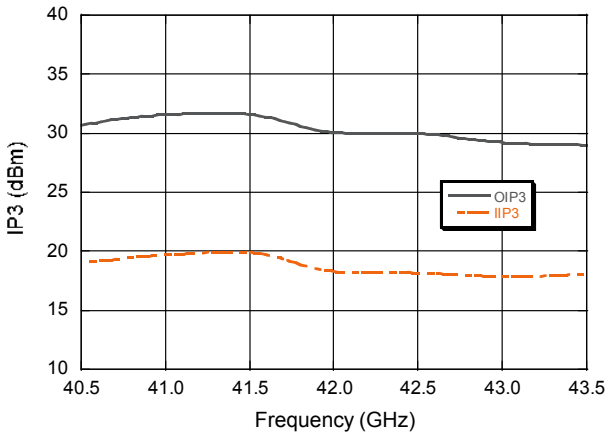
Conversion Gain @ 3.5 GHz IF



Conversion Gain @ 2 GHz IF



IP3 @ 3.5 GHz IF



Output IP3 @ 2 GHz IF

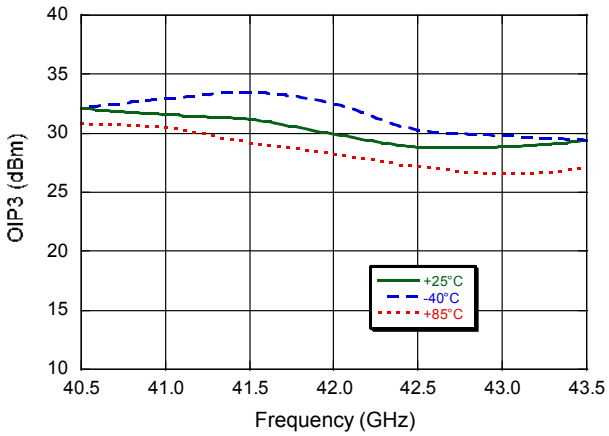
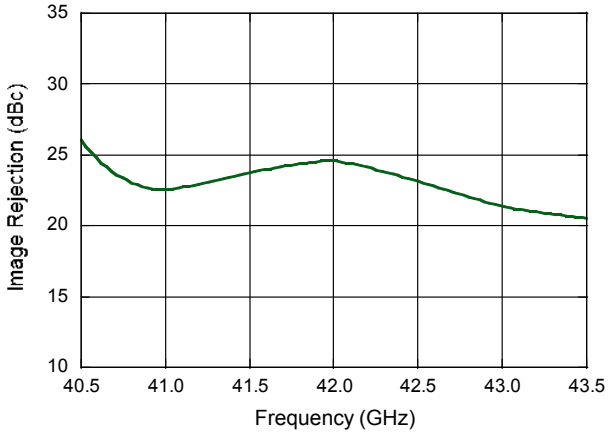


Image Rejection @ 3.5 GHz IF



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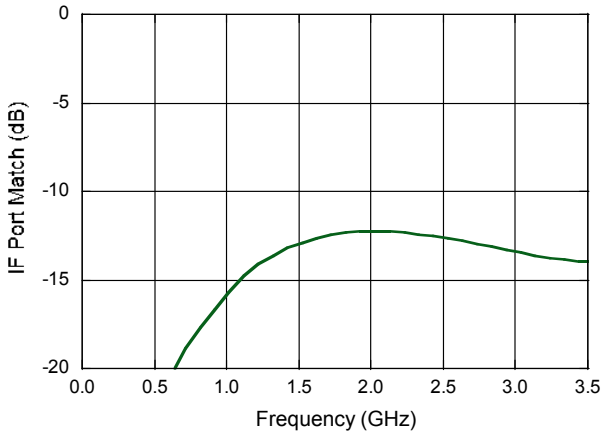
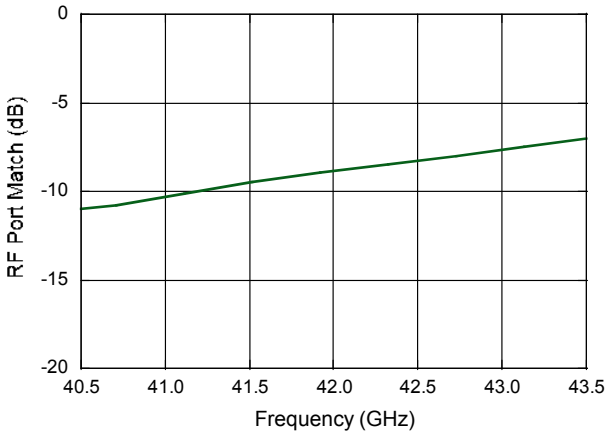
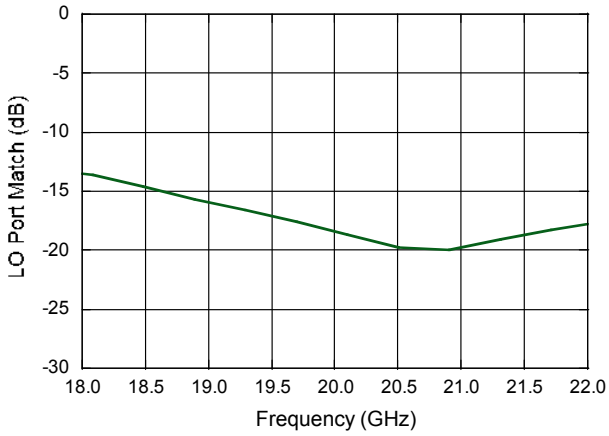
IF Return Loss



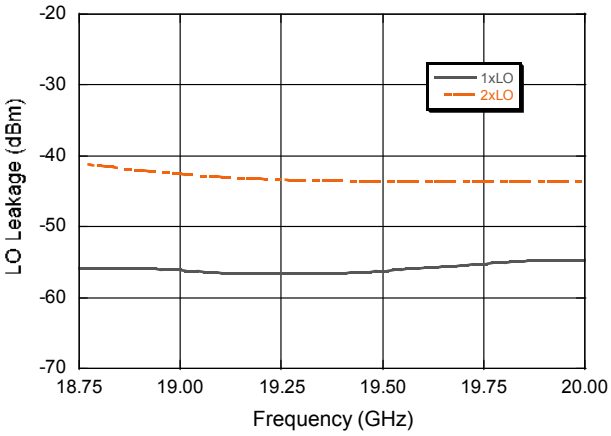
RF Return Loss



LO Return Loss

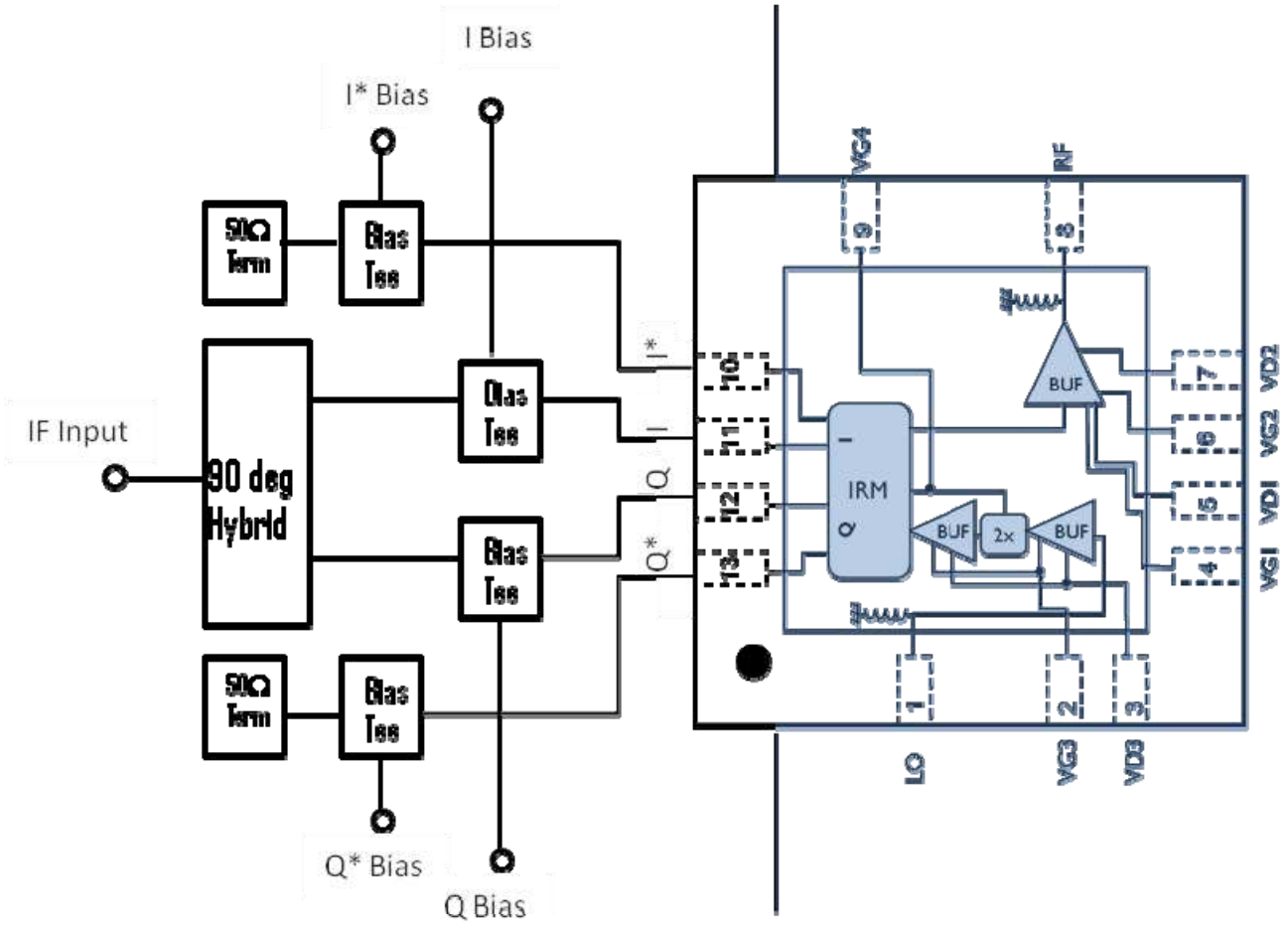


LO Leakage



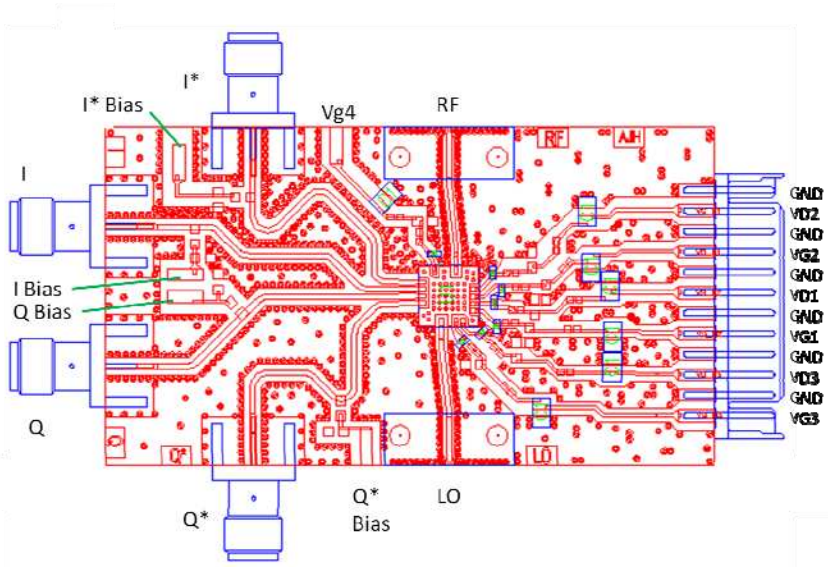
App Note [1] Biasing - As shown in the Pin Designations table, the device is operated by biasing Vd1, Vd2, and Vd3 at 4.0 V. The corresponding drain currents are set to 90 mA, 90 mA, and 60 mA respectively. Vg4 requires a fixed voltage bias of nominally -3 V. It is recommended to use active bias on Vg1, Vg2, Vg3 to keep the currents in Vd1, Vd2, and Vd3 constant, in order to maintain the best performance over temperature. Depending on the supply voltages available and the power dissipation constraints, the bias circuits may include a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply to sense the current. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] I/Q versus I*/Q* - The IF input to the typical configuration is through a 90deg hybrid coupler. The hybrid splits the IF input into inphase and quadrature phase components. These two signals enter the MAUC-010515 on either the I/Q pair, or the I*/Q* complimentary pair. Whichever pair are not used must be terminated into 50 Ω. There are subtle differences between the performance when using the main IF ports (I, Q) versus the complimentary ports (I*, Q*). For highest gain, best image rejection and lowest noise figure, the main IF ports (I, Q) should be used.



App Note [3] Board Layout - As shown in the recommended board layout, it is recommended to provide 100 pF decoupling capacitors as close to the bias pins as possible. Additional 10 nF and 1 µF on each of the bias lines are recommended placed a distance further away.

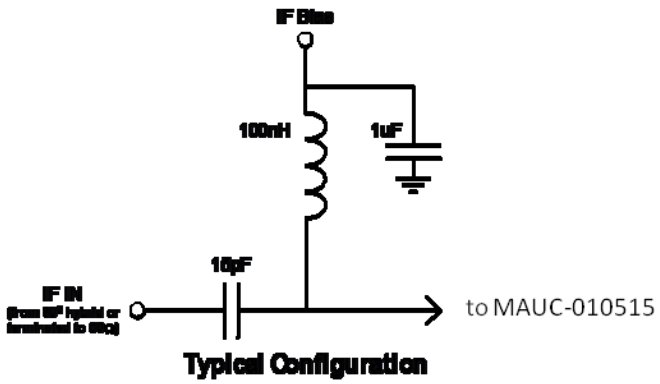
Recommended Board Layout



App Note [4] IF Bias - To obtain optimum 2xLO leakage performance, tuning is achieved by adjusting the DC bias on each of the IF inputs (I, Q, I*, Q*). DC bias is implemented by adding simple bias tees to each of the four IF ports. The diagram below shows a typical bias tee design used.

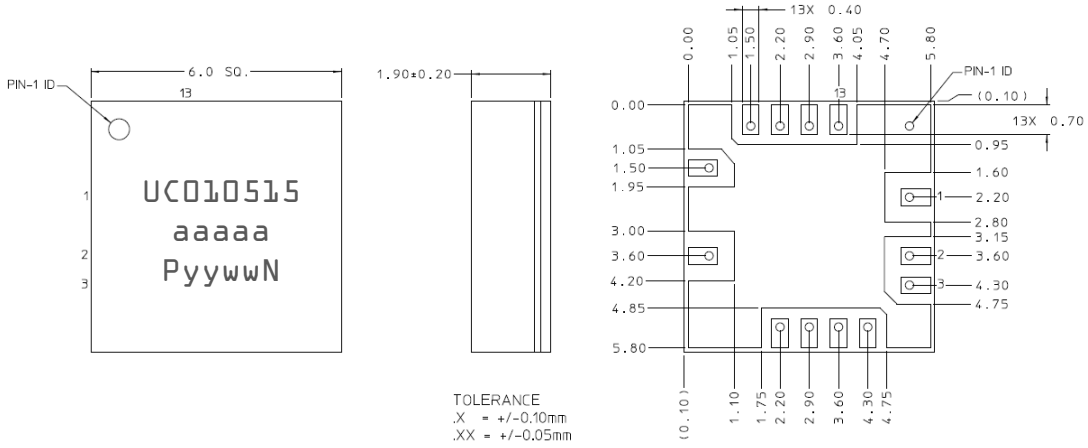
If the I and Q ports are used for the IF input, the I* and Q* ports are DC biased and terminated into 50 Ω. A typical tuning arrangement is to apply a fixed 0.3 V DC bias to both the used IF input ports: I, Q. The remaining two IF ports which have been terminated to 50 Ω tuning independently for minimum 2xLO leakage.

For minimum 2xLO leakage in a system, it may be necessary to correct the IF DC bias for different frequency and temperature conditions. This can be implemented by calibration and offset tables stored in memory, and used to control IF bias over all practical conditions.



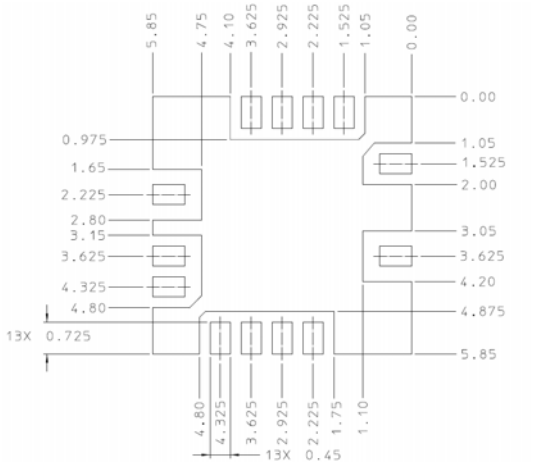
Typical Configuration

Lead-Free 6 mm Laminate Package†



Top View Side View Bottom View

Recommended Substrate Footprint



All dimensions are in mm.

Markings:
Line 1: MACOM Part Number
Line 2: Lot Wafer Number
Line 3:
P = Philippines (Country of Origin)
yyww: Date Stamp (year-year-week-week)
N = Nickel/Gold plating

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.