MAAD-000523

Digital Attenuator, 6-Bit, Serial / Parallel Control
31.5 dB, 0.7 - 6.0 GHz

Rev. V2

Features

- Integrated CMOS/TTL Compatible Driver
- Parallel & Serial (P/S) Control with power-up state selection
- Insertion Loss: 1.6 dB typical @ 2.1 GHz
- IP3: 50 dBm typical @ 2 GHz
- Attenuation Accuracy:
  +/-(0.4 + 4% of attenuation setting) dB
- 0.5-dB Attenuation Steps to 31.5 dB
- Useable from 0.4 to 8.0 GHz
- Lead-Free 4 mm 24-Lead PQFN Package
- Halogen-Free "Green" Mold Compound
- RoHS* Compliant and 260°C Re-flow Compatible
- Small Relative Phase Variation per Bit

Description

The MAAD-000523 is a 6-bit, 0.5-dB step GaAs MMIC digital attenuator in a lead-free 4 mm 24 lead PQFN surface mount plastic package. This device is ideally suited for use where high accuracy, very low power consumption and low intermodulation products are required. Typical applications include Cellular Basestation R_X/T_X Line-up, Femtocells, and other gain / level control circuits.

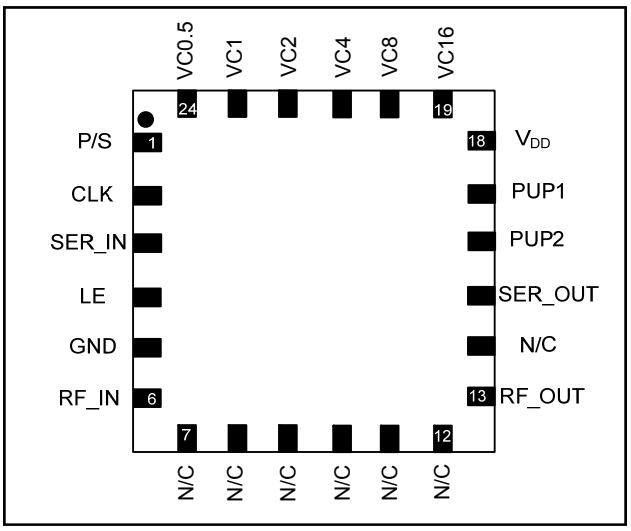
This attenuator is controlled with either a SPI compatible serial interface or a 6 bit parallel word.

Ordering Information [1]

Part Number	Package
MAAD-000523-TR1000	1000 piece reel
MAAD-000523-TR3000	3000 piece reel
MAAD-000523-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

Functional Schematic [3,4]



3. Blocking capacitors are required on all RF ports.
4. For optimum RF performance all N/C's should be terminated to GND.

Pin Configuration

Pin No.	Function	Pin No.	Function
1	P/S	13	RF_OUT
2	CLK	14	No Connection
3	Serial IN	15	Serial OUT
4	LE	16	PUP2
5	Ground	17	PUP1
6	RF_IN	18	V_{DD}
7	No Connection	19	VC16
8	No Connection	20	VC8
9	No Connection	21	VC4
10	No Connection	22	VC2
11	No Connection	23	VC1
12	No Connection	24	VC0.5

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Electrical Specifications [5]: T_A = 25°C, Z_0 = 50 Ω, V_{DD} = 5 V, V_C = 0/+5 V [6]

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Reference Insertion Loss	0.7 GHz 2.1 GHz 4.0 GHz 6.0 GHz	dB	— — — —	1.3 1.6 2.0 2.5	— 2.3 — —
Attenuation Accuracy	0.7 - 6.0 GHz	± (0.4 + 4% of attenuation setting) dB typ.			
VSWR	0.7 - 6.0 GHz	Ratio	—	1.2:1	—
Trise, Tfall	10% to 90% RF, 90% to 10% RF	ns	—	70	—
Ton, Toff	50% Control to 90% RF, 50% Control to 10% RF	ns	—	100	—
Settling Time Loss Delta (Gate Lag)	RF Loss Difference within 30 µs to 500 µs @ 2 GHz and 500 µs Pulse	dB	—	0.2	—
Transients	In Band	mV	—	50	—
Input P1dB	2.0 GHz	dBm	—	25	—
IP_2	2-Tone, +10 dBm/tone, 1 MHz Spacing 2.0 - 6.0 GHz	dBm	—	75	—
IP_3	2-Tone, +10 dBm/tone, 1 MHz Spacing 2.0 - 6.0 GHz	dBm	—	50	—
I_{DD}	V_{DD} = 5V	µA	0	—	600

5. External DC blocking capacitors are required on all RF ports. Loss varies at 0.003 dB/°C.

Truth Table [6]

VC16	VC8	VC4	VC2	VC1	VC0.5	Attenuation (dB)
1	1	1	1	1	1	Reference IL
1	1	1	1	1	0	0.5
1	1	1	1	0	1	1
1	1	1	0	1	1	2
1	1	0	1	1	1	4
1	0	1	1	1	1	8
0	1	1	1	1	1	16
0	0	0	0	0	0	31.5

6. 0 = 0 to 0.8V, 1 = 2 to 5V.

Absolute Maximum Ratings [7,8]

Parameter	Absolute Maximum
Input Power 700 - 6000 MHz	+27 dBm
Operating Voltage	6 V
Control Voltage	-0.5 V ≤ V_C ≤ 5.5 V
Operating Temperature	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. M/A-COM Technology Solutions does not recommend sustained operation near these survivability limits.

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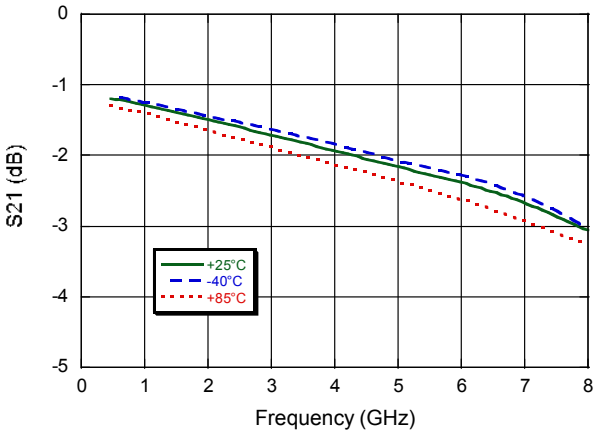
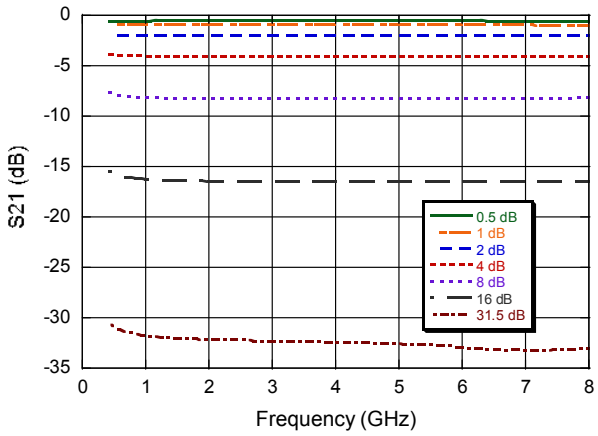
Typical Performance Curves

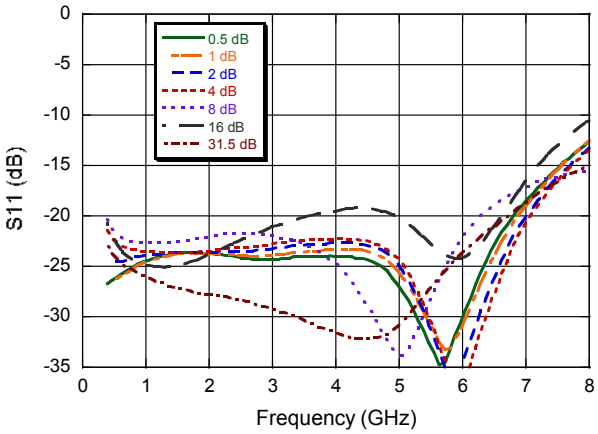
Insertion Loss



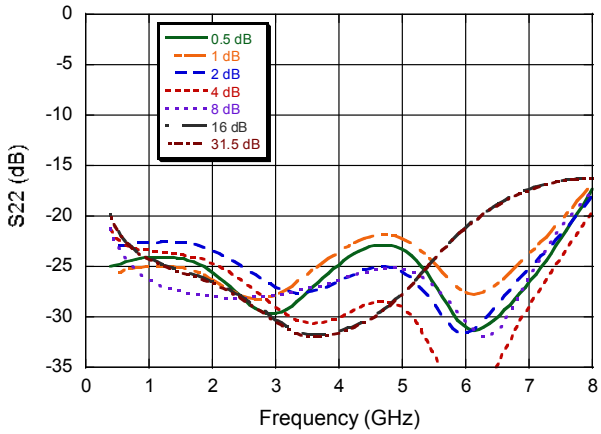
Relative Attenuation across all major states



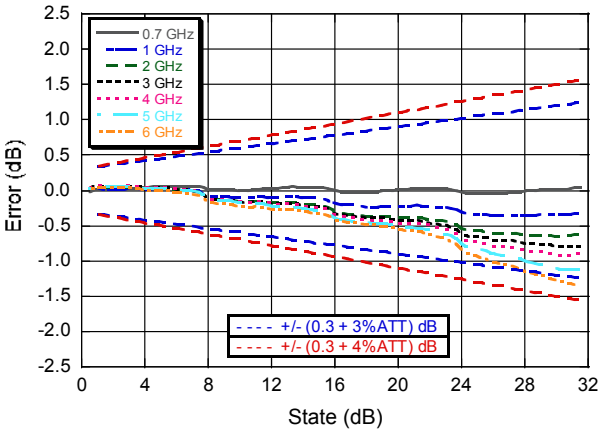
Input Return Loss, across all attenuation states



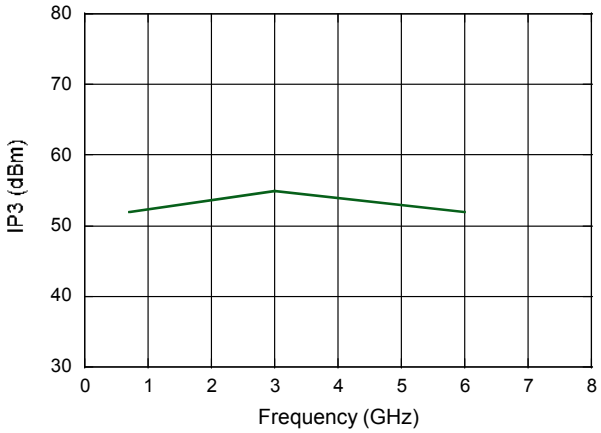
Output Return Loss, across all attenuation states



Step Error vs. State over Frequency



IP3



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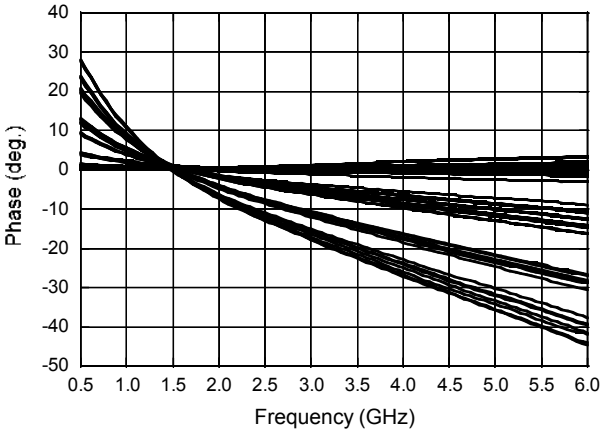
Typical Performance Curve:

Relative Phase Variation vs. Frequency and all states



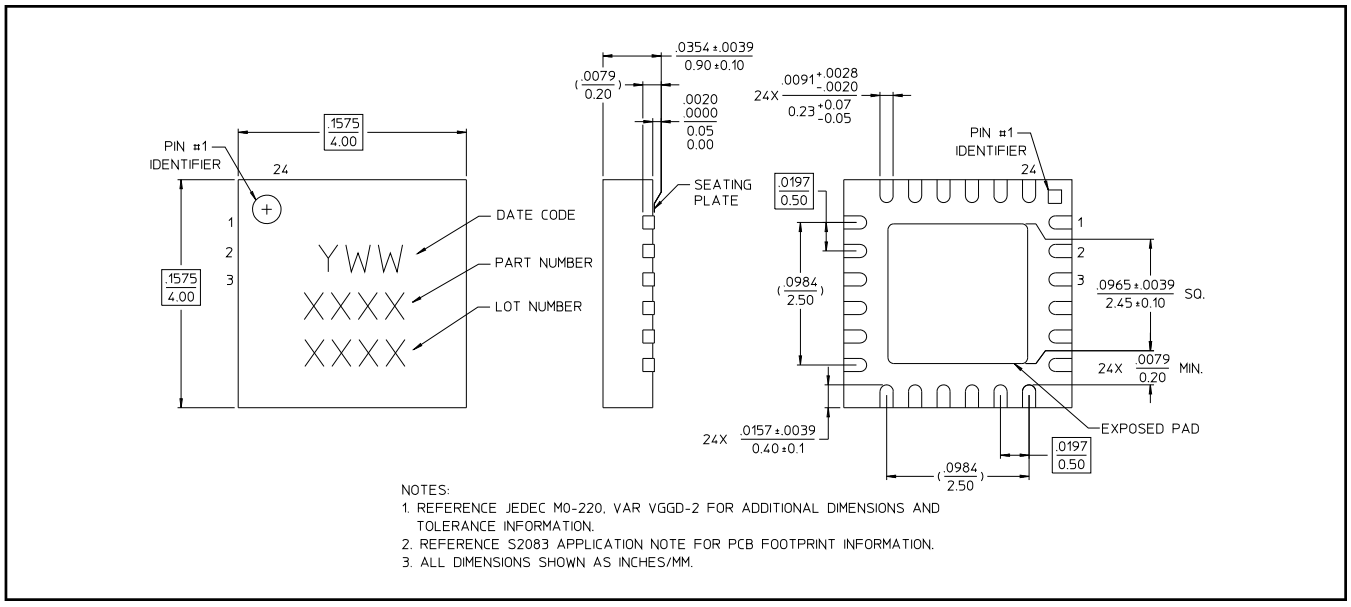
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Lead Free 4 mm 24-Lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.

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Functionality
Modes of Operation: Serial, Direct Parallel, and Latched Parallel

Mode Truth Table

P/S	LE	Mode
1	X	Serial
0	Constant High	Direct Parallel
0	Pulsed	Latched Parallel

Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with the MSB first. After shifting in the 6 bit word, bringing LE high will set the attenuator to the desired state. While LE is high the CLK is masked to protect the data while implementing the change. SEROUT is the SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled and the serial input register is loaded asynchronously with parallel digital inputs.

For all modes of operations, the outputs will stay constant while LE is kept low.

Direct Parallel Mode

The parallel mode is enabled when P/S is set to low. In the direct parallel mode, the attenuator is controlled by the parallel control inputs directly. The LE must be at logic high to control the attenuator in this mode.

Latched Parallel Mode

In the latched parallel mode, the parallel control inputs will be buffered by registers, and loaded to the outputs when LE is high. The outputs shall not change states when LE is low.

Power-up States

The power-up (PUP) states will work in both serial and parallel modes, and initiate the attenuator according to the PUP truth table. During power up, the digital inputs shall be held constant for at least 1 µs after V_{CC} reaches 90% of final value. For serial mode, the PUP states will only work when LE is held low. The PUP state shall be locked out after the first LE pulse.

Functionality
Modes of Operation: Serial, Direct Parallel, and Latched Parallel

PUP Truth Table

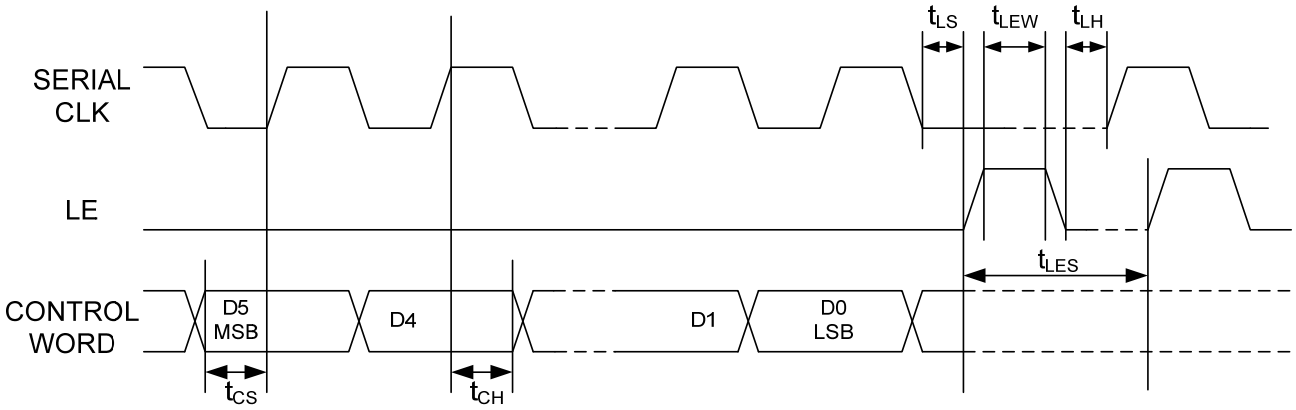
Inputs				Gain Relative to Max. Gain	Notes
PS	LE	PUP2	PUP1		
0	0	0	0	-31.5 dB	Parallel Mode
0	0	0	1	-24 dB	
0	0	1	0	-16 dB	
0	0	1	1	Insertion Loss	
0	1	X	X	0 to –31.5 dB (Set VC0.5 - VC16)	
1	0	X	X	0 to –31.5 dB (Set VC0.5 - VC16)	Serial Mode
1	1	X	X	No Definition	

Serial Interface Timing Characteristics

Symbol	Parameter	Typical Performance			Units
		-40°C	25°C	+85°C	
t_{SCK}	Min. Serial Clock Period	100	100	100	ns
t_{CS}	Min. Control Set-up Time	20	20	20	ns
t_{CH}	Min. Control Hold Time	20	20	20	ns
t_{LS}	Min. LE Set-up Time	10	10	10	ns
t_{LEW}	Min. LE Pulse Width	10	10	10	ns
t_{LH}	Min. Serial Clock Hold Time from LE	10	10	10	ns
t_{LES}	Min. LE Pulse Spacing	630	630	630	ns

Functionality
Modes of Operation: Serial, Direct Parallel, and Latched Parallel

Serial Input Interface Timing Diagram



Parallel Control Word