Features

- 28 VDC, 32 VDC and 36VDC output voltage preset via VID pins
- Margining via I^2C
- Active current/load sharing
- Wide input voltage range 85-264 VAC
- Highly-efficient topology yields 89% at 230 VAC
- 1U high: 5.6” x 1.6” x 12” cassette
- Input fuse protected
- I^2C interface status and control
- High density design:13.4 W/in^3
- Up to 4500 W in a 1U-high, 19-inch wide rack
- Standby voltage 5 VDC/1A
- Adjustable output voltage
- Overtemperature, output overvoltage, and output overcurrent protection
- ORing circuit for true redundant operation
- Status LEDs: AC OK, DC OK, Fan Fail/ Overtemperature Fail
- Auto select power limits [1]

Applications

- Test & measurement, RF amplifiers & transmitters, factory automation, semiconductor & LD-MOS based equipment, and other distributed power applications

The FXR-3-32G shelf provides capability to parallel up to three FXP1500-32G PSUs in a 19" rack, see rack section (below) for power shelf details.

RoHS Compliant

Description

The FXP1500-32G is a 1500 watt, power factor corrected (PFC) front-end, which provides a user-adjustable 32 VDC (26-38 VDC range) main output for test & measurement, RF amplifiers and transmitters, factory automation, semiconductor equipment, and other distributed power applications. The FXP1500-32G provides for true hot-swap with AC and DC connections at the rear of the model and can be used for redundant system applications. Its very small dimensions allow configuration of up to three units in a 1U rack (up to 4500 W).[2] The highly-efficient thermal design with internal fan cooling permits its use in wide operating voltage and temperature ranges to provide very high reliability.

Status information is provided with front panel LEDs, logic signals, and via the I^2C management interface. In addition, the I^2C bus can enable the power supply, control the fan speed, adjust the output voltage, and set the output current limit.

The FXP1500-32G meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Model Selection

Model	Input voltage VAC auto selected [1]	Output 1		Output 2		Rated power W
		$V_{o\ nom}$ VDC	$I_{o\ max}$ ADC	$V_{o\ nom}$ VDC	$I_{o\ max}$ ADC	
FXP1500-32G	85 – 264	32	46.9	5	1	1505 [3]

[1] The available output power is automatically adjusted depending on the input voltage.
[2] 1U standard rack FXR-3-32G for FXP1500-32G is available from Power-One.
[3] Automatic derating of main output below 108 VAC to: $I_{o\ max}$ = 37.5 A (1200 W).

Absolute Maximum Ratings

Stress in excess of the absolute maximum ratings may cause performance degradation, adversely effect long-term reliability, or cause permanent damage to the converter.

Parameter	Conditions/description	Min	Max	Unit
Input voltage	Continuous Transient, 60 ms max.		264 300	VAC VAC
Operating ambient temperature	$V_{i\ min}$- $V_{i\ max}$, $I_{o\ nom}$, cooling by internal fan 100 % load from 0 to 50°C linear derating to 50% load from 50°C to 70°C	0	70	 °C °C
Storage temperature	Non-Operating	-40	85	°C

Environmental, Mechanical, & Reliability Specifications

Parameter	Conditions/description	Min	Nom	Max	Unit
Altitude	Operating Non-Operating			10 k 40 k	ASL Ft. ASL Ft.
Relative humidity, non-condensing	Operating	10		90	% RH
	Storage	5		95	% RH
Temperature coefficient	0 °C to 70 °C (after 15 min warm-up)			0.02	%/K
Shock	IEC/EN 60068-2-27, 11 ms			40	g_{pk}
Sinusoidal vibration	IEC/EN 60068-2-6 2-8 Hz 8-200 Hz 200-500 Hz		 7.5 2 4		 mil g_{pk} g_{pk}
Random vibration	10-2000 Hz		6.15		g_{rms}
MTBF	Calculated per Bellcore (SR-332, Issue 1): GB 25°C Demonstrated	 230 250			 kh kh

Safety Specifications

Maximum electric strength testing is performed in the factory according to EN 550116, IEC/EN60950-1 2nd ed., and UL/CSA60950-1 2nd ed. Input-to-output electric strength tests should not be repeated in the field. Power-One will not honor any warranty claims resulting from electric strength field tests.

Parameter	Conditions/description	Min	Nom	Max	Unit
Agency approvals	UL/CSA60950-1 2nd ed., EN60950-1 2nd ed., IEC60950-1 2nd ed., CE Mark for LVD				
Insulation safety rating	Input to case Input to output Output to case	Basic Reinforced Functional			
Electric strength test voltage	Input to case Input to output Output to case Output 1 to output 2	2.12 Note [1] 0.1 0.1			kVDC kVDC kVDC kVDC

[1] Subassemblies are pre-tested with 4.2 kVDC in accordance with EN50116 and IEC/EN60950-1 2nd ed.

EMC Specification

Parameter	Description	Criterion
Electrostatic discharge	IEC/EN 61000-4-2, level 4 (contact/air)	8/15 kV, Performance criterion B
Electromagnetic field	IEC/EN 61000-4-3, level 3	10 V/m, Performance criterion A
Electrical fast transients/burst	IEC/EN 61000-4-4, level 3 (L/L, L/E)	2 / 1 kV, Performance criterion B
Surge	IEC/EN 61000-4-5, level 3 (L/L, L/E)	1 / 2 kV, Performance criterion B
Voltage dips and interruptions	IEC/EN 61000-4-11 Dip 30 %, 100 ms Dip 30 %, 200 ms Dip 60 %, 20 ms Dip 60 %, 100 ms Dip > 95 %, 20 ms Dip > 95 %, 100 ms	 Performance criterion A Performance criterion B Performance criterion A Performance criterion B Performance criterion A Performance criterion B
RF conducted immunity	IEC/EN 61000-4-6	10 VAC, AM 80 %, 1 kHz Performance criterion A
Emissions conducted	CISPR 22/EN 55022/EN 61204	Class B
Emissions radiated	CISPR 22/EN 55022/EN 61204	Class A
Harmonics	IEC/EN 61000-3-2	Class B
Voltage fluctuation and flicker	IEC/EN 61000-3-3	Pass
Voltage sag	SEMI F47-0200 (High Line 230V)	Pass

Input Specification

Specification is valid for input voltage, load, and temperature ranges, unless otherwise stated.

Parameter	Conditions/description	Min	Nom	Max	Unit
Input voltage		85	230	264	VAC
Input frequency		47	50/60	63	Hz
Turn-on input voltage	Ramping up	79	-	85	VAC
Turn-off input voltage	Ramping down	70	-	78	VAC
Inrush current limitation	115/230 VAC acc. ETS 300 132-1 < 100 ms			50	A_{pk}
Hold-up time	After last AC line peak , V_i = 230 VAC, $P_{o\ nom}$	20			ms
Power factor	$V_{i\ nom}$, $I_{o\ nom}$	0.95			W/VA
Efficiency	V_i = 230 VAC, $V_{o\ nom}$, $I_{o\ nom}$, T_c=25°C	89	89.5		%
Max input current				20	A_{rms}

Output Specification

Specification is valid for input voltage, load, and temperature ranges, unless otherwise stated.

Parameter	Conditions/Description	Min	Nom	Max	Units
Total output voltage range	Adjustable via T4, T5 pins & I^2C	26		38	VDC
Output voltage set point	Adjustable via T4, T5 pins (LL=28V, LH=HL=32V, HH=36V)		28 32 36		VDC VDC VDC
Output voltage trimming	Adjustable via I^2C from any set point. **Note**: all changes to V_{o1} made via I^2C are volatile and are lost upon power cycling the PSU	-2		+2	VDC
Overvoltage protection latching	28V set point 32V set point 36V set point		35 40 45		VDC VDC VDC
Nominal current output 1	$I_{o1\ nom}$ @ V_i =105 VAC – 264 VAC, P_o 1.5 kW 28V set point 32V set point 36V set point $I_{o1\ nom}$ @ V_i = 85 VAC – 105 VAC, P_o 1.2 kW 28V set point 32V set point 36V set point		 46.9 46.9 41.7 42.9 37.5 33.4		 ADC ADC ADC ADC ADC ADC
Nominal current output 2	$I_{o2\ nom}$ @ Vi = 85 VAC – 265 VAC, P_o 5 W		1.0		ADC
Current limit output 1	$I_{o1\ max}$ @ V_i = 105 VAC – 264 VAC high droop hic-cup $I_{o1\ max}$ @ V_i = 85 VAC – 105 VAC high droop hic-cup		48.8 50.8 39.0 41.0		ADC ADC ADC ADC
Current limit output 2	$I_{o2\ max}$ @ V_i = 85 VAC – 265 VAC		1.3		ADC
Static line regulation output 1	$V_{i\ min}$ - $V_{i\ max}$, 50 % $I_{o\ nom}$	-0.5		0.5	% $V_{o\ nom}$
Static load regulation output 1 (droop characteristic)	V_i = 230 V, 0-100 % $I_{o\ nom}$ V_o : full load (46.9 ADC) to no load	 31.68 -1.0	 32	13.6 32.32 +1.0	mV/A VDC % $V_{o\ nom}$
Dynamic load regulation	Load change 1% ⟷100% Io nom, dI_o/dt =1 A/µs Voltage deviation (droop + over- or undershoot) Max. recovery time to within 1 % of $V_{o1\ nom}$	-4		+4 2000	% $V_{o\ nom}$ µs
Start-up time	Time required for output within regulation after initial application of AC-input ($V_{i\ nom}$, $I_{o\ nom}$) after removal of inhibit ($V_{i\ nom}$, $I_{o\ nom}$)		 100	1.5	s ms
Output voltage ripple and noise	$V_{i\ nom}$, $I_{o\ nom}$, 20 MHz bandwidth V_{o1} V_{o2}			 320 50	 mV_{pp} mV_{pp}
Remote sense	Total compensation for cable losses			500	mV
Active current share	Difference in current between two units for V_{o1} above 10 % load. Active current share pin with its 1kΩ internal impedance enables control of output voltage. Voltage on this pin is proportional to output current, 2V at $I_{o1\ nom}$			5	ADC

Controls and Indicators

Specification is valid for input voltage, load, and temperature ranges, unless otherwise stated.

Parameter	Type[1]	Conditions/Description
Visual Status Indication	FP	LED indicators[2]: • DC OK (green) • AC OK (green) • Fan fail & Over-temperature (amber)
I^2C communication bus	OC[S1, S2]	• Monitors alarm functions and allows control of specific parameters. • Uses standard Philips two wire bus (SCL and SDA signal lines)
I^2C communication bus addressing	OC[T1-T3]	Three lines provide up to 8 separate PSU I^2C addresses
PS present pin	OC[U3]	• Used by system to indicate a PSU is installed in a system shelf • Contact closure to logic ground (internal pull-down resistor of 1 kΩ)
PS main output remote shutdown	OC[R1]	• TTL compatible signal, inhibited when open contact, high or at TTL logic "1" • Signal referenced to logic return (LRTN)
	FP	Two position switch in series with OC signal (logical AND) allows local enable/disable; "0" Position => PS disabled; "1" Position => PS Enabled
Power supply OK	I^2C	AC OK & DC OK & no overcurrent & no over-temperature & fans working
DC current fail	I^2C	Reports over-current condition on main output, I_{O1}
AC fail / Power down warning	OC[U2] & I^2C	Provides a warning that the input power has failed at least 5 ms before the output falls out of regulation (<90% V_{O1} set). • Open collector signal with 20 mA pull-down capability, referenced to logic return (LRTN). • AC fail will go high or open during power fail condition and will go low when input is within the operating range. • A Power Fail warning will turn off the front panel green AC OK LED.
DC fail / Output voltage fault	OC[U4] & I^2C	Internal under-voltage and overvoltage supervision of V_{O1}. • Open collector signal with 20 mA pull-down capability, referenced to logic return (LRTN). • DC fail will go high or open if *Vo*1 < 90% or V_{O1}> 110% of V_{O1} set, measured in front of the ORing FETs. • Green LED on the front panel indicates normal operation; LED will flash if in parallel operation V_{O1} is OK, but the unit is disabled.
Critical temperature Warning/Fan Fail	OC[U1] & I^2C	Indicates the PSU operating temperature has reached [$T_{shut\text{-}down}$ – 10K] Indicates if the unit is in over-temperature shutdown. • Open collector signal with 20 mA pull-down capability, referenced to logic return (LRTN). • The OC-output will go low 100 ms before an over-temperature condition shuts down the unit. • An amber LED on the front panel indicates over-temperature or fan fail.
DC voltage monitoring	I^2C	Monitors the main output voltage, V_{O1}, seen at the output connector Accuracy is ±1% over setting range and temperature.
DC current monitoring	I^2C	Monitors the output current I_{O1} : Accuracy ± 1% over the load range.
Active current share interconnect	OC[R4]	Line must be connected to all paralleled PSUs to allow active current share functionality between units
V_{O1} presets	OC[T4,T5]	Output voltage is preset per programming of T4, T5 • T4/T5 = LOW / LOW => V_{O1}=28VDC • T4/T5 = LOW / HIGH = HIGH / LOW => V_{O1}=32VDC • T4/T5 = HIGH / HIGH => V_{O1}=36VDC
V_{O1} voltage trimming (margining)	I^2C	Output voltage trimming Vo1: ±2 VDC Setting accuracy over I^2C: ± 50mV at V_{O1}nom, ± 150 mV over setting range
Fan speed control	I^2C	Two fan speed levels automatically set depending on the internal temperature. The fan speed can be set to full speed or automatic control via I^2C command.
Fan OK/FAIL	OC[U1] & I^2C	Indicates if the cooling fans are operating or have failed.
Synchronized startup pin	OC[R5]	Overcurrent signal which can be used for synchronous startup of units in parallel or to recover from an overload condition.

[1] Abbreviations used:

- ***OC[#]*** => Hardwired signal accessible at PSU output connector, with pin number reference
- ***FP*** => Provided by devices located on PSU Front panel
- ***I^2C*** => Signal provided over I^2C communication system; detailed I^2C information is available from the specific model's I^2C Manual found on the Power-One web site.

[2] See LED Function table for further details

Output Connector Pinning and Signal Specification

Output Connector Description	OC Pin #	Type	Signal Reference	Low level High level	V max I max
Over-temperature / Fan Fail	U1	OC-output, protected by 16 V Zener diode and a 10Ω resistor in series	LGND	<0.4 V @ 20 mA Pull up	15 V 20 mA
AC Fail / Power down warning	U2			<0.4 V @ 20 mA Pull up	15 V 20 mA
Power Supply Present	U3	1KΩ Resistor connected to logic GND	LGND	Open Pull up	10 V 10 mA
DC Fail / Output voltage fault	U4	OC-output, protected by 16 V Zener diode and a 10Ω resistor in series	LGND	<0.4V @ 20 mA Pull up	15 V 20 mA
Internal ground (INT GND)	U5	Used only for ADDRx and V_{O1} set. Do not connect the internal grounds in systems with several units.	Connected to V_{O1} - line before the output filter	-	-
ADDR0 I^2C address bus	T1	High = internal 10 KΩ PU to 5V=> Logic 1 Low = connect to INT GND => Logic 0	INT GND	Logic 1 Logic 0	5V 0V
ADDR1 I^2C address bus	T2				
ADDR2 I^2C address bus	T3				
V_{O1} set	T4				
V_{O1} set	T5				
SDA, I^2C serial data line	S1	I^2C compatible signal referenced to logic GND 5 V or 3.3 V logic	LGND	Logic 1 Logic 0	5V 0V
SCL, I^2C serial clock line	S2				
Auxiliary power +5 V	S3	V_{O2}+ output, isolated from main output	Aux output is floating	-	-
Auxiliary power +5 VRTN	S4	Aux output return; ground isolated from main output			
Logic ground (LGND)	S5	Internally connected to Aux GND through 10Ω resistor. Wire LGND separately from Aux RTN and main output GND to minimize noise on signals and I^2C bus. Leave open if not used.	-	-	-
Output inhibit R1	R1	PS active when pulled low (DC-DC stage off when left open)	LGND	<0.8 V >2.0 V	10 V 3.5 mA
V sense +	R2	Open or connected to V_{O1}+ at the load Internally connected to V_{O1}+ via 100 Ω.	-	-	dV<3 V_{pp} 30 mA
V sense -	R3	Open or connected to V_{O1}- at the load Internally connected to V_{O1}- via 100 Ω.	-	-	
Active Current Share	R4	This pin must be interconnected to pin R4 of all other paralleled PSUs for proper operation of active current share function	-	-	2V
Synchronized Startup (for paralleled units)	R5	Open or connected to synch startup circuit	V_{o1} - at the OC		12V 2mA
V_{O1}-	P1, P3, P5	Main output - pins	-	-	-
V_{O1}+	P2, P4, P6	Main output + pins	-	-	-

Input Connector Description	OC Pin #	Type
Protection Earth	P1	PE
Phase	P2	L
Neutral	P3	N

Protection

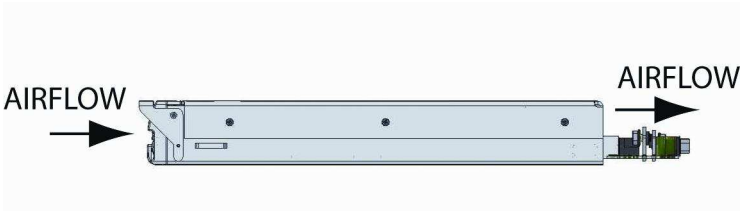
Parameter	Conditions/description	Min	Nom	Max	Unit
Input fuse	Not user accessible		25AF		
Inrush current limitation			with NTCs		
Output			No-load, short circuit, and overload proof		
Overvoltage protection latching [1]	Absolute		40		V
Over-temperature protection	Automatic power shutdown at T_C		95		℃

LED Indicator Functionality

Condition	Power Fail (AC OK)	Output Good (DC OK)	Fan Fail and Over - Temperature
Normal Operation	Green	Green	OFF
Power Supply is inhibited	Green	OFF	Amber
Input AC is low	OFF	OFF	Amber
Input AC is low or missing	OFF	OFF	Amber/OFF
Over-temperature	Green	OFF	Amber
Output overload (In regulation)	Green	Green	OFF
Output Overloaded (Out of Regulation)	Green	OFF	OFF
Fan Not running	Green	OFF	Amber
Power Supply Failed	OFF	OFF	OFF/ Amber

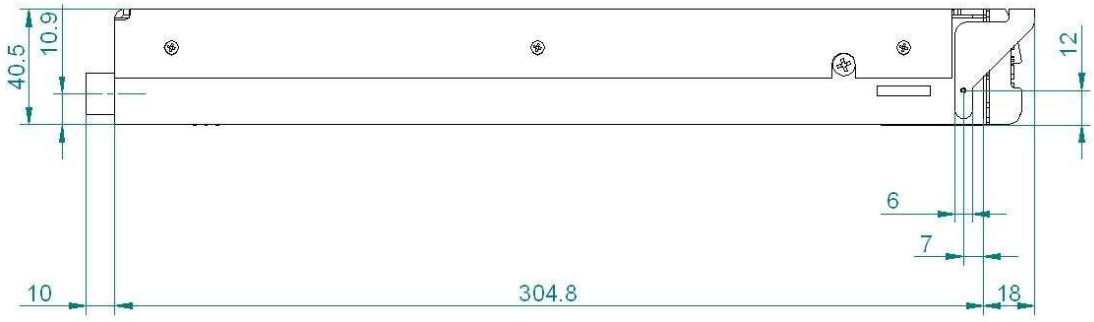
Cooling:

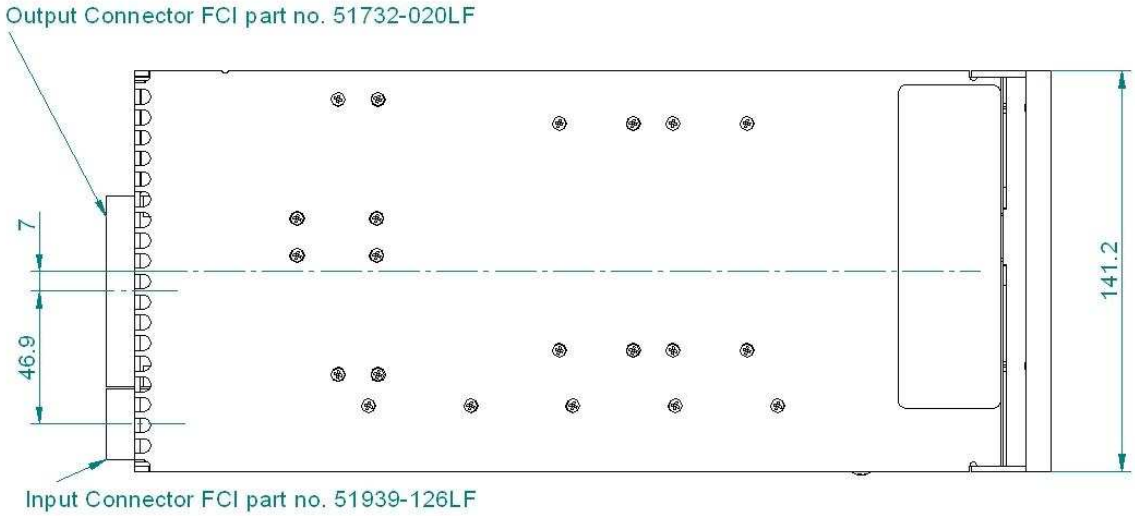
To achieve best cooling results sufficient airflow through the unit must be ensured. Do not block or obstruct the airflow at the rear of the unit by placing large components directly at the output connector.



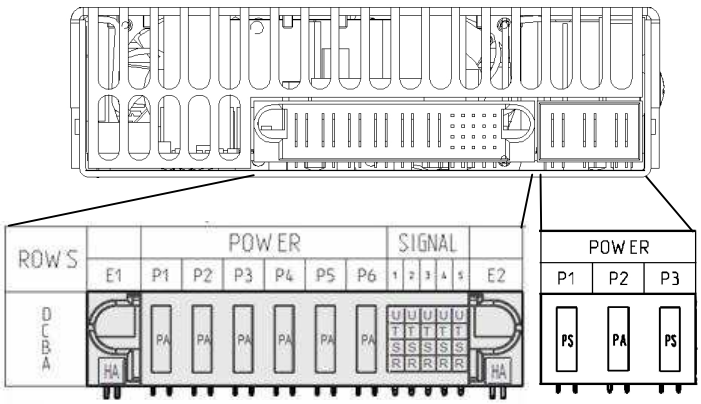
Mechanical Data

Mechanical Data (W, H, D)	5.6” (141.2mm) x 1.6” (40.5mm) x 12” (304.8mm)



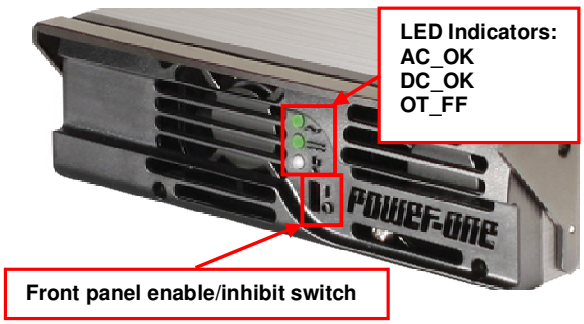


Input and Output Connector Descriptions



Output Connector: FCI (51732-020 LF)

Input Connector: FCI (51939-126 LF)



FXP series front bezel showing LED indicators and recessed enable switch

Female ledge connector: Manufacturer: FCI
Output connector Part No.: 51762-106020000AA LF (Horizontal)
Output connector Part No.: 51742-106020000AA LF (Vertical)
Input connector Part No.: 51915-056LF (Horizontal)
Input connector Part No.: 51940-099LF (Vertical)
Information on availability under http://www.stkcheck.com/evs/fcielectronics/fcisearch.asp

Paralleling Front-Ends:

For parallel use in minimal configuration systems, only the inhibit pins must be shorted to logic GND. All other pins can be left open. The power supplies will share the output current automatically (droop current share).

For parallel applications without I^2C bus, but the use of all other features, it is recommended to connect all logic GND's on a backplane together, to connect all V_{o2} -, all V_{o2} + and to leave the internal GND's open.
The sense wires can be left open or connected to a common load point, the synch-start pin can be left open or connected to a synch-start circuit, the inhibit pins can be connected together or used individually. All I^2C signals (T1-T5, S1, and S2) can be left open.

Use of a small foil capacitor > 3µF directly at the power outputs of each unit is recommended in order to prevent voltage drops at the hot plug. For additional information on paralleling see the following Rack (Power Shelf) section.

Racks

(FXR-3-32G Power Shelves)

Each rack (power shelf) is 1U high with backplane and designed for up to three front-end models in parallel or in n+1 operation. Each power shelf has:

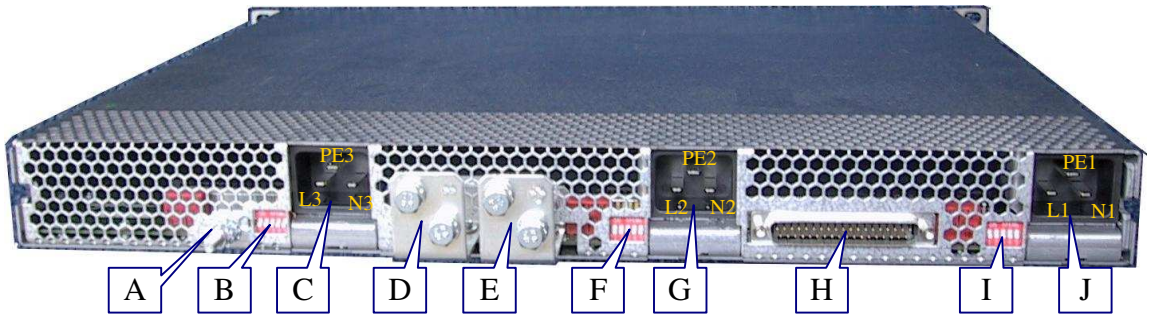
- Generous copper bus bars for low-loss current distribution.
- Output terminals with two M4-screws on each power tab.
- Two fast-on contacts for system earthing.
- Address coding over five pole DIP switch on each unit, 37-pin D-Sub connector with I^2C-lines, monitoring signals and support functions.
- Provides a start-up synchronization circuit and EMV filters.

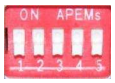
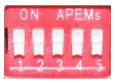
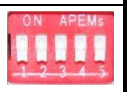
FXR-3-32G Power Shelf Front View

Overall Mechanical Dimensions (FXR-3-32G Power Shelves)

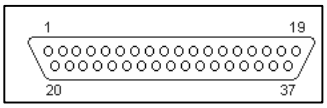
FXR-3 Mechanical Data (W, H, D)	17.7" (449.6 mm) x 1.7" (43.1 mm) x 14" (355.6 mm)

Output Connector Descriptions (FXR-3-32G)



Location	Description
A	Earth connection
B	5-bit DIP switch, pins 1,2,3 for I^2C addressing and pins 4,5 for Vo setting of PSU #3 
C	Mains connector of PSU #3
D	Output 1 Minus
E	Output 1 Plus
F	5-bit DIP switch, pins 1,2,3 for I^2C addressing and pins 4,5 for Vo setting of PSU #2 
G	Mains connector of PSU #2
H	37-pin SUB-D connector, control, sense, check and Auxiliary power (Output 2)
I	5-bit DIP switch, pins 1,2,3 for I^2C addressing and pins 4,5 for Vo setting of PSU #1 
J	Mains connector of PSU #1

SUB-D Output Connector Pinout and Signal Specification



Output Connector Description	OC Pin	Type	Signal Reference	Low level High level	V max I max
Over-temperature / Fan Fail PSU1	1	OC-output, protected by 16 V Zener diode and a 10 Ω resistor in series	LGND	<0.4 V @ 20 mA Pull up	15 V 20 mA
Power Supply Present PSU 1	2	Resistor (1 kΩ) connected to LGND	LGND	Open Pull up	10 V 10 mA
Power Supply Present PSU 2	3				
Spare	4				
Over-temperature / Fan Fail PSU 3	5	OC-output, protected by 16 V Zener diode and a 10 Ω resistor in series	LGND	<0.4 V @ 20 mA Pull up	15 V 20 mA
AC Fail / Power down warning PSU 3	6				
Power Supply Present PSU 3	7	Resistor (1 kΩ) connected to logic GND	LGND	Open Pull up	10 V 10 mA
DC Fail / Output voltage fault PSU 3	8	OC-output, protected by 16 V Zener diode and a 10 Ω resistor in series	LGND	<0.4 V @ 20 mA Pull up	15 V 20 mA
Overtemperature / Fan Fail PSU 2	9				
Synch._Start_A	10	Sync_start_A , Active high The signals of several racks can be connected together in such a way that all supplies will be inhibited until the last supply has recovered from its overcurrent condition	LGND	<7V off < 9V	15V 10mA
Open	11				
Output inhibit PSU 1-3	12	DC-DC stage ON when pin is open or connected to LGND DC-DC stage OFF when pin is connected on high potential	LGND	<0.8 V >2.0 V	10 V 3.5 mA
V sense +	13	Open or connected to V_{O1}+ at the load Internally (PSU) connected to V_{O1}+ over 100 Ω	V_{O1+}		dV < 3 Vpp 30 mA
V sense -	14	Open or connected to V_{O1}- at the load Internally (PSU) connected to V_{O1}- over 100 Ω	V_{O1-}		dV < 3 Vpp 30 mA
Open	15				
NC	16				
NC	17				
NC	18				
NC	19				
AC Fail/ Power-down warning PSU 1	20	OC-output, protected by 16 V Zener diode and a 10 Ω resistor in series	LGND	<0.4 V @ 20 mA Pull up	15 V 20 mA
DC Fail/ Output voltage fault PSU 1	21				
AC Fail/ Power-down warning PSU 2	22				
DC Fail/ Output voltage fault PSU 2	23				
SDA, I^2C data line	24	I^2C compatible signal	LGND	5 V or 3.3 V logic	

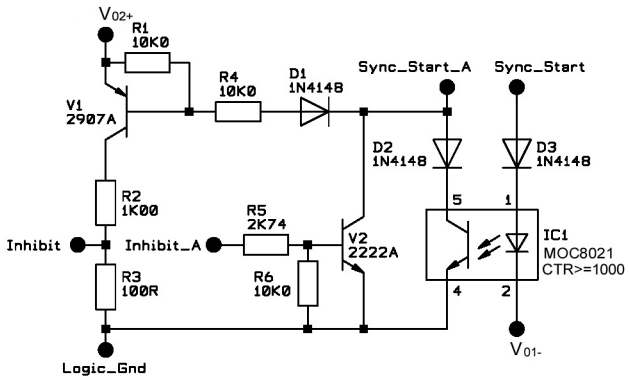
SUB-D Output Connector Pinout and Signal Specification (Cont.)

Output Connector Description	OC Pin	Type	Signal Reference	Low level High level	V max I max
SCL, I^2C clock line	25	I^2C compatible signal	LGND	5 V or 3.3 V logic	
V_{O2}+ = +5 V (Auxiliary power)	26	V_{O2}+ Aux output, insulated from main output	Aux output is isolated supply		
V_{O2}- = +5 VRTN (Auxiliary power)	27	V_{O2}- Aux output, insulated from main output			
Logic Gnd (LGND)	28	Wire separately from auxiliary and main output GND to minimize noise and avoid voltage drops on signal- and I^2C return. Leave open if not used.	Internally connected to V_{O2}- Auxiliary GND via 10 Ω		
Active curretnt share	29	This pin must be interconnected to all other parallel shelfs for proper operation of active current share function.			2V
NC	30				
NC	31				
NC	32				
NC	33				
NC	34				
Internal Ground PSU1	35	Used only for ADDRx and V_{O1} set. Do not connect the internal grounds in the system with several units.	Connected to V_{O1}- line before the output filter		
Internal Ground PSU2	36				
Internal Ground PSU3	37				

Synchronized start-up circuit for paralleling operation

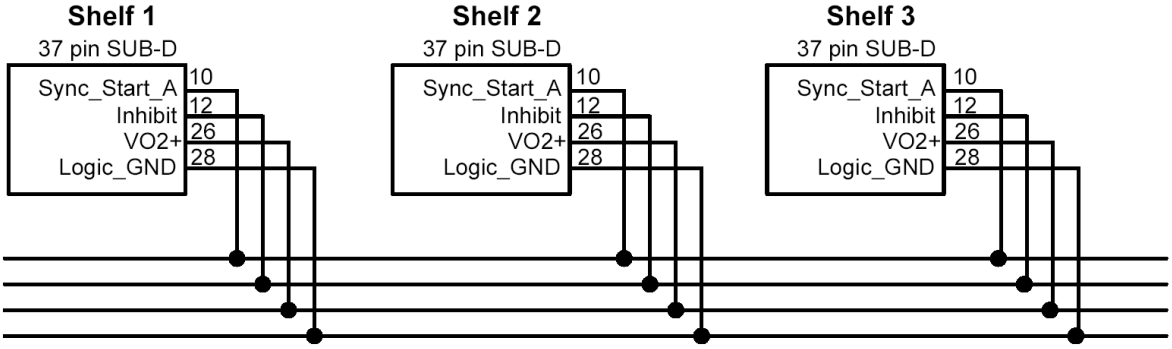
The FXP1500-32G power supply exhibit an overcurrent hiccup behavior. This means if either of these supplies reaches an overcurrent limit, the output voltage will immediately turn OFF and after a delay turn ON again. In parallel use, all power supplies have to start synchronized because of the internal hiccup behavior. Otherwise, the supply which has reached overcurrent first will go to hiccup; this will overload the other supplies, which then will also go to hiccup. When the first supply has recovered from hiccup (hiccup dead time), the others remain in hiccup. This will immediately drive the first one into hiccup once again. This means that without a start-up circuit, a system with several power supplies can never recover from an overload condition or start-up into full load.

The following additional circuit, required to reach synchronized startup, is already implemented inside the FXR-3-32G shelf.



Synch Start-up Connection Between Shelves

The following connection between the shelves is required to achieve a parallel operation. The synch-start circuits inside the shelves inhibit all power supplies until the last one has recovered from its overcurrent condition and then synchronize the restart of the outputs.

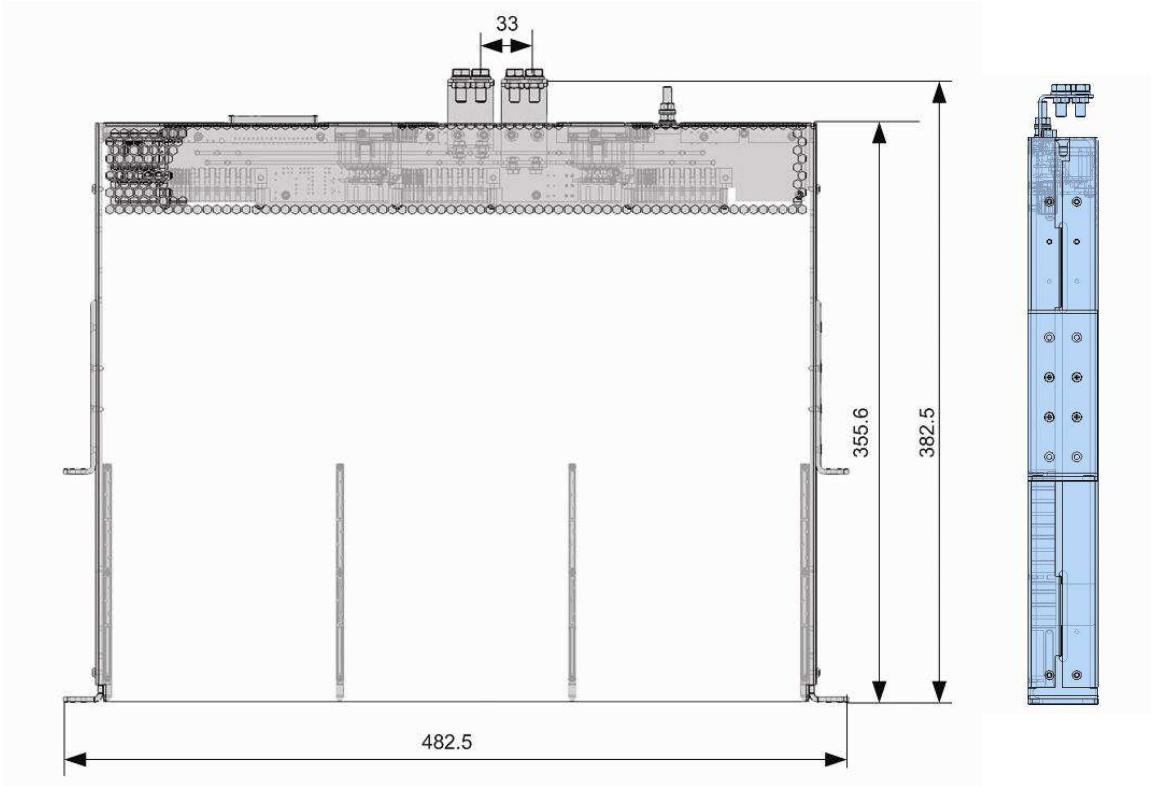


Synch Start-up Circuit Description

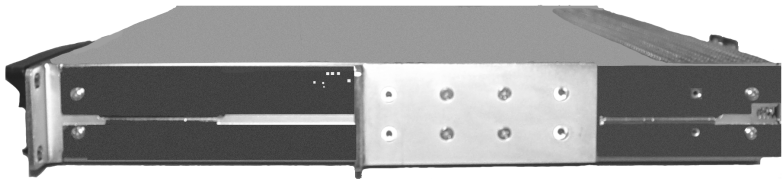
Description	Pin Location, Definition	Type	Signal Reference	Low level High level	V max I max
Auxiliary power +5 V (Output 2)	26	V_{O2}+, Aux output, insulated from main output			
Logic ground	28	Logic_GND , Internally connected over 10 Ω to V_{O2}-, (Auxiliary power ground (Output 2))	Internally connected over 10 Ω to V_{O2}-,		
Output inhibit_A PSU 1-3	12	Inhibit_A, DC-DC stage ON when pin is open or connected to LGND DC-DC stage OFF when pin is connected on high potential	LGND	<0.8 V >2.0 V	10 V 3.5 mA
Synch. Startup 1 PSU 1-3	R5 (at PSU OC)	The synch_start pin is connected to the over-current signal of the PSU1-3. In the case of an overcurrent shutdown, this signal goes high.	Vo1-	<7V off > 9V	15V 10mA
Synch. Startup_A Rack FXR-3-32G 1-N Pin on the D-Sub connector on the backplane	10	Sync_start_A , Active high The signals of several racks can be connected together in such a way that all supplies will be inhibited until the last supply has recovered from its overcurrent condition.	LGND		

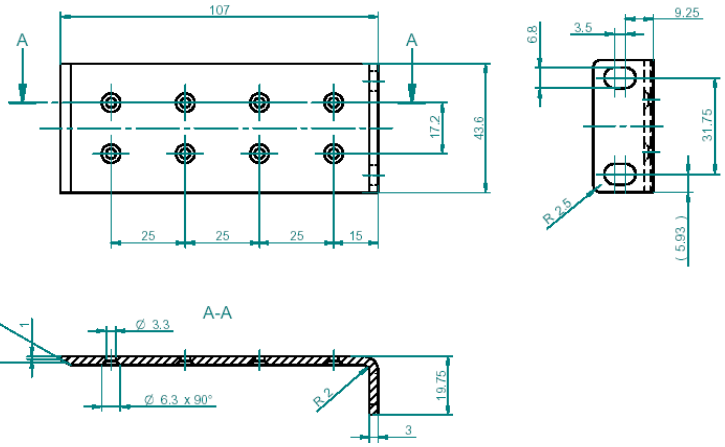
NOTE: The Sync-Start pins can be wired together only if the power supplies are connected with a minimal voltage drop on power ground as achieved on a backplane with massive copper bus bars. If there is a less ideal connection, it is recommended to use an opto-coupler for each unit (IC1, D3, D2).

Mechanical Data (FXR-3-32G Power Shelf)



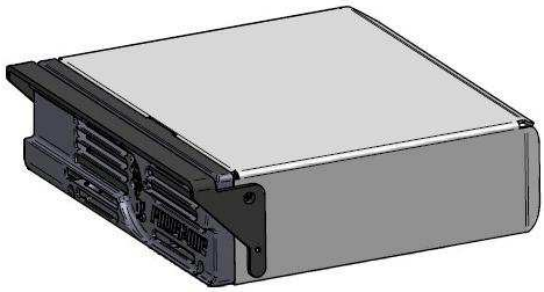
Accessories:
Center Angular Brackets are set in the middle for shelf mounting:

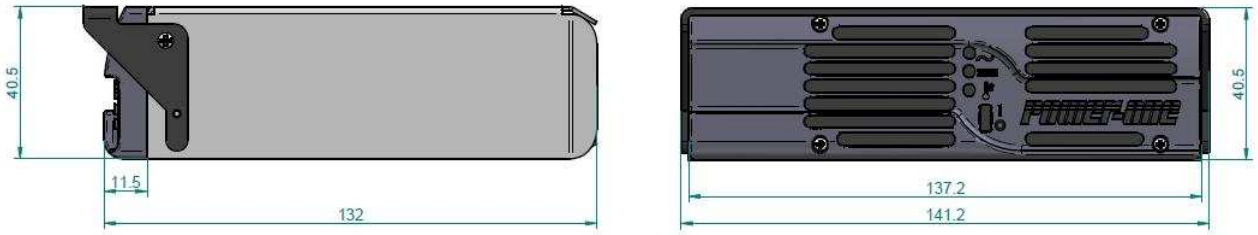




Center Angular Bracket sets can be ordered: Power-One part no.: HZZ01222
Note: Each Center Angular Bracket set contains 2 brackets and 8 screws.

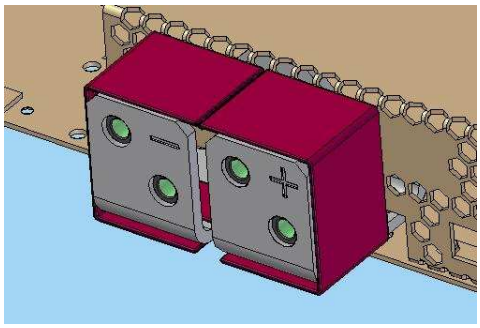
Filler for covering of the empty shelf slots

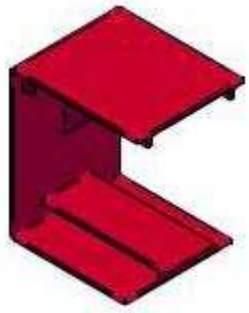


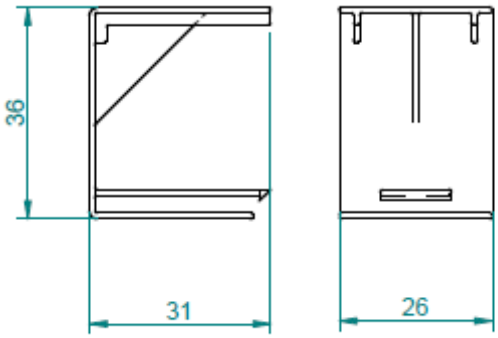


Filler can be ordered: Power-One part no.: XAK.00043.0

Plastic cover set for the bus bars:



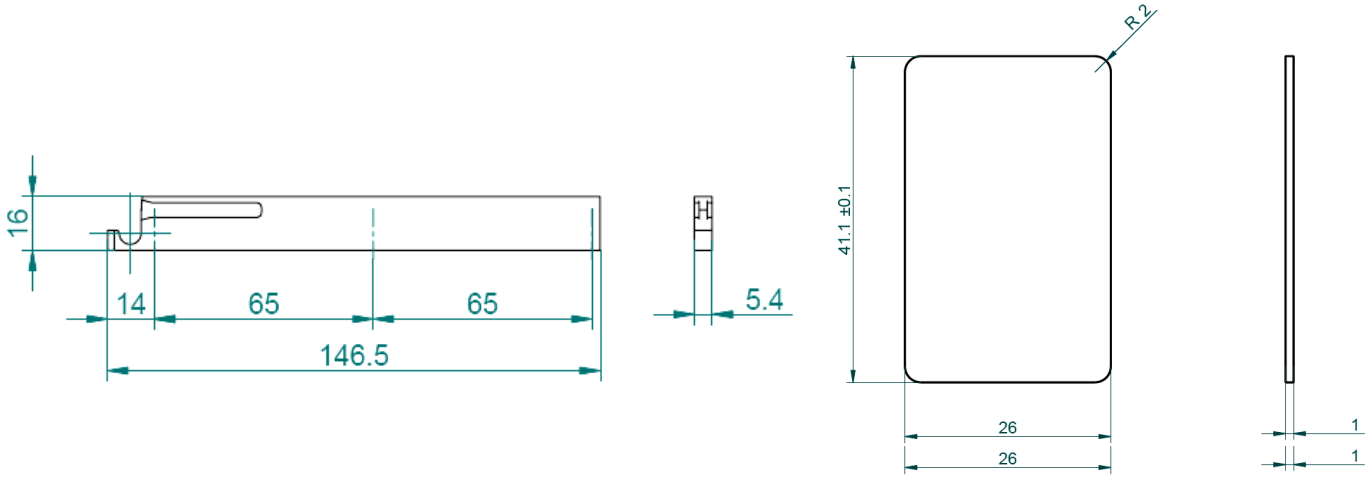




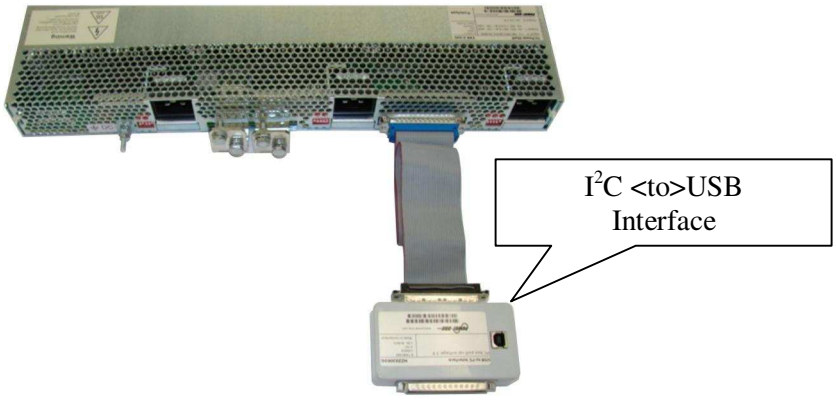
Plastic cover set can be ordered: Power-One part no.: XEB.00031.0
Note1: Available upon special request.
Note2: Each plastic cover set contains 2pcs.

Fulcrum:
The handle has been designed to allow easy plug-in and -out in a rack system. The handle (lever) fits into a counter piece (fulcrum) which is fixed to the bottom of the rack. During the plug, the fulcrum holds the unit down and guides it towards the output connector. The Power-One part number of the fulcrum and its associated mounting accessories is: HZZ01223.

Individual fulcrum sets can be also ordered: Power-One part no.: HZZ01223.
Note: Each HZZ01223 set contain 2 fulcrums, 2 supports, and mounting accessories.



I²C to USB Interface HZZ02002G:



I²C Management Software: All FNP and FXP front-ends can be controlled via Power-One's GUI-driven I²C Management software and an I²C-to-USB interface (P/N HZZ02002G). An I²C Programming Manual describes the complete range of parameters that can be programmed to the FXP1500/1800 front-ends. This manual is available by searching on "FXP1500" at www.power-one.com.