DATA SHEET

AS211-334: 0.1–4.0 GHz pHEMT SPDT Switch

Applications

- General purpose switch for telecommunications

Features

- P1dB: +30 dBm typical @ 3 V
- IP3: +43 dBm typical @ 3 V
- Low insertion loss: 0.3 dB @ 0.9 GHz
- Low DC power consumption
- Small footprint, LGA (6-pin, 1.5 x 1.2 x 0.8 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

NEW

Skyworks offers lead (Pb)-free RoHS (Restriction of Hazardous Substances) compliant packaging.

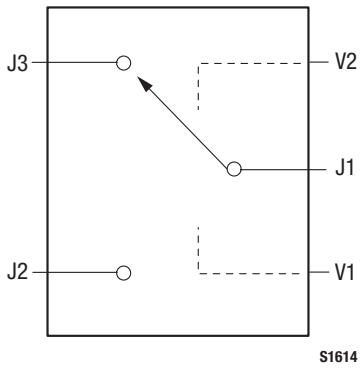


Figure 1. AS211-334 Block Diagram

Description

The AS211-334 is an FET Single-Pole, Double-Throw (SPDT) switch for general telecommunications applications. The device features low insertion loss and positive voltage operation with very low DC power consumption.

The switch is manufactured in a compact, 1.5 x 1.2 x 0.8 mm, 6-pin Land Grid Array (LGA) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

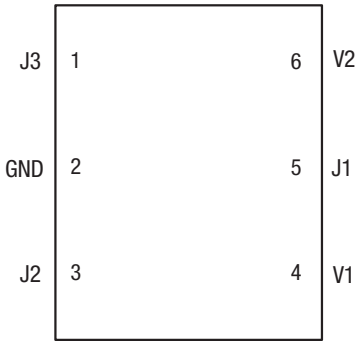


Figure 2. AS211-334 Pinout – 6-Pin LGA (Top View)

Table 1. AS211-334 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	J3	RF output	4	V1	Positive control voltage
2	GND	Ground	5	J1	RF common/antenna port
3	J2	RF output	6	V2	Positive control voltage

Table 2. AS211-334 Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Input power	P_{IN}	Any frequency >500 MHz, V_{CTL} = 0/7 V			6	W
Control voltage	V_{CTL}		–0.2		+8.0	V
Operating temperature	T_{OP}		–40		+85	°C
Storage temperature	T_{STG}		–65		+150	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Electrical and Mechanical Specifications

The absolute maximum ratings of the AS211-334 are provided in Table 2. Electrical specifications are provided in Table 3.

Typical performance characteristics of the AS211-334 are illustrated in Figures 3 through 5.

The state of the AS211-334 is determined by the logic provided in Table 4.

Table 3. AS211-334 Electrical Specifications (Note 1)
(Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Insertion loss	IL	0.1 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 3.0 GHz 3.0 to 4.0 GHz		0.3 0.4 0.5 0.6	0.5 0.6 0.7 0.8	dB dB dB dB
Isolation	ISO	0.1 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 3.0 GHz 3.0 to 4.0 GHz	22 20 20 23	25 22 23 26		dB dB dB dB
Voltage Standing Wave Ratio	VSWR	Low frequency to 4 GHz		1.2:1	1.3:1	–
Switching characteristics: Rise, fall On, off Video feedthrough		 10/90% or 90/10% RF 50% control to 90/10% RF T_{RISE} = 1 ns, bandwidth = 500 MHz		 10 20 25		 ns ns mV
1 dB input compression point	IP1dB	V_{CTL} = 0 and 3 V, 0.5 to 3.0 GHz V_{CTL} = 0 and 5 V 0.5 to 3.0 GHz		+30 +34		dBm dBm
3rd Order Input Intercept Point	IIP3	Two-tone P_{IN} = +5 dBm V_{CTL} = 0 and 3 V V_{CTL} = 0 and 5 V		 +43 +50		 dBm dBm
Thermal resistance	Θ_{JC}			25		°C/W
Control voltage: Low High	 V_{CTL_L} V_{CTL_H}	 V_{CTL_L} = 0 to 0.2 V @ 20 µA max. V_{CTL_H} = 3 V @ 100 µA max. to 5 V @ 200 µA max.				

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

(V_{CTL} = 3 V, C_{BL} = 47 pF, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

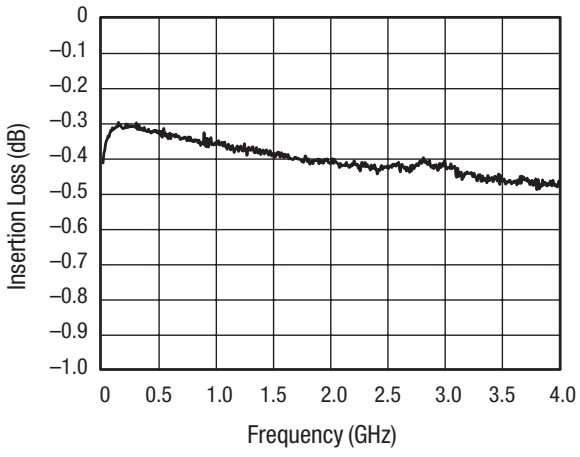


Figure 3. Insertion Loss vs Frequency

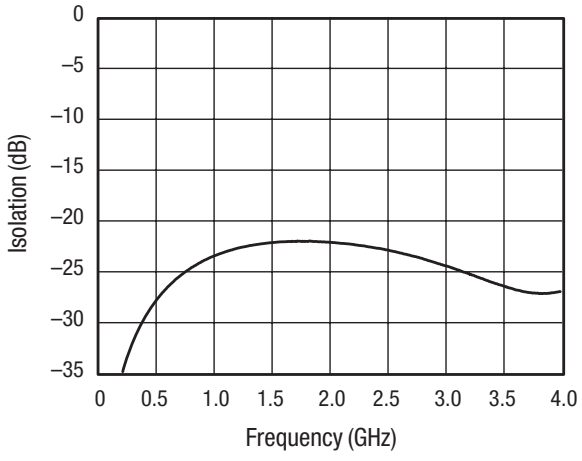


Figure 4. Isolation vs Frequency

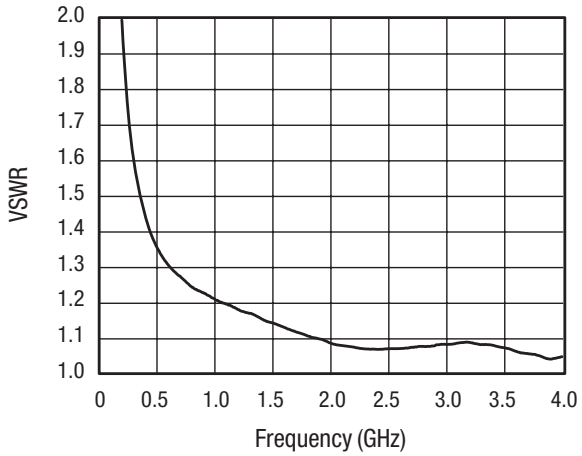


Figure 5. VSWR vs Frequency

Table 4. AS211-334 Truth Table

V1 (Pin 4)	V2 (Pin 6)	J1 to J2 Path	J1 to J3 Path
0	V_{HIGH}	Insertion loss	Isolation
V_{HIGH}	0	Isolation	Insertion loss

Note: V_{HIGH} = +3 V to +5 V. "0" = 0 V to +0.2 V. Any state other than described in this Table places the switch into an undefined state. An undefined state will not damage the device.

Evaluation Board Description

The AS211-334 Evaluation Board is used to test the performance of the AS211-334 SPDT Switch. An assembly drawing for the Evaluation Board is shown in Figure 6. The Evaluation Board schematic diagram is provided in Figure 7.

Package Dimensions

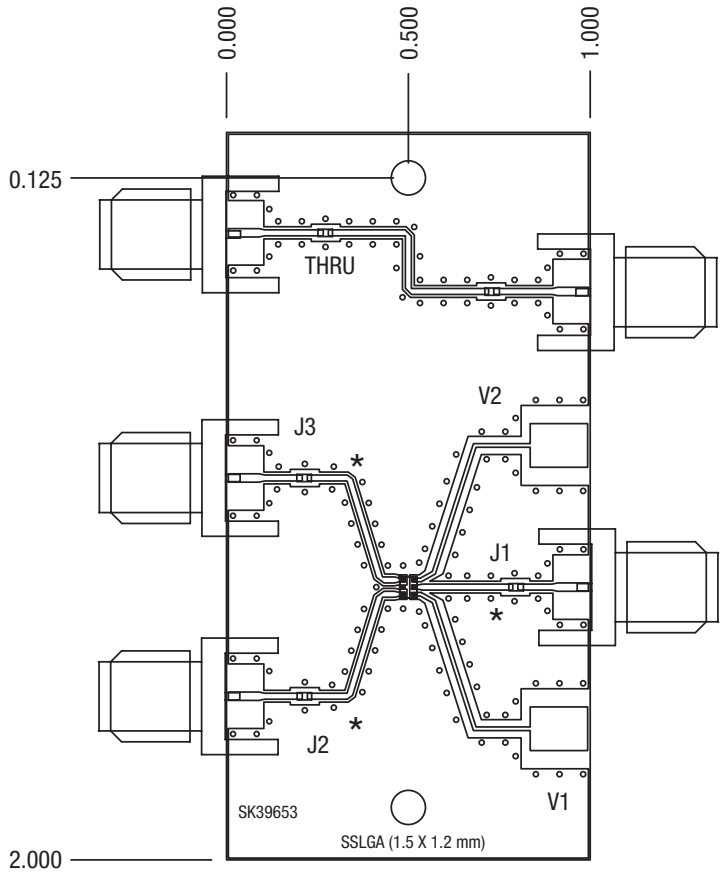
The PCB layout footprint for the AS211-334 is provided in Figure 8. Typical case markings are shown in Figure 9. Package dimensions for the 6-pin LGA are shown in Figure 10, and tape and reel dimensions are provided in Figure 11.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE AS211-334 is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format. For packaging details, refer to the Skyworks Application Note, *Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation*, document number 200083.



Dimensions are in millimeters **S1837**

Figure 6. AS211-334 Evaluation Board Assembly Diagram

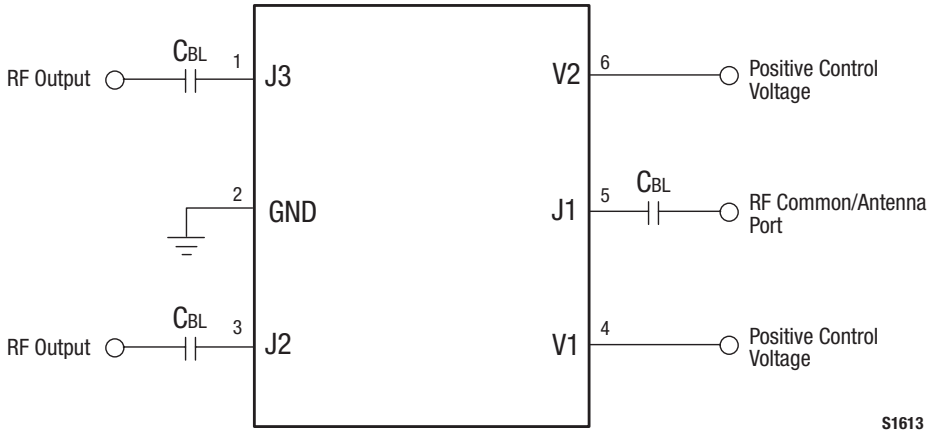


Figure 7. AS211-334 Evaluation Board Schematic

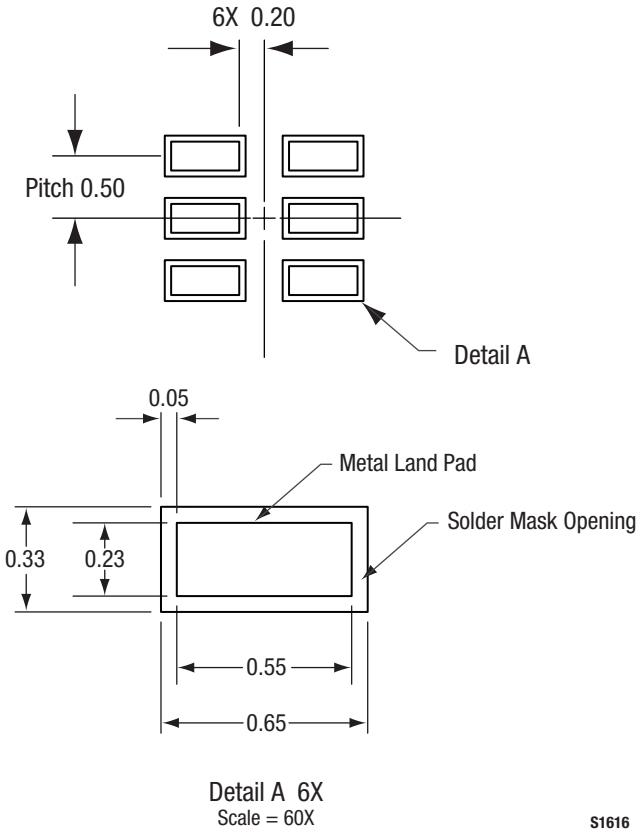


Figure 8. AS211-334 PCB Layout Footprint (Top View)

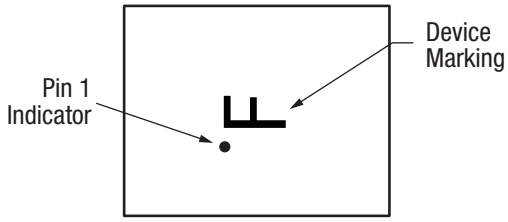
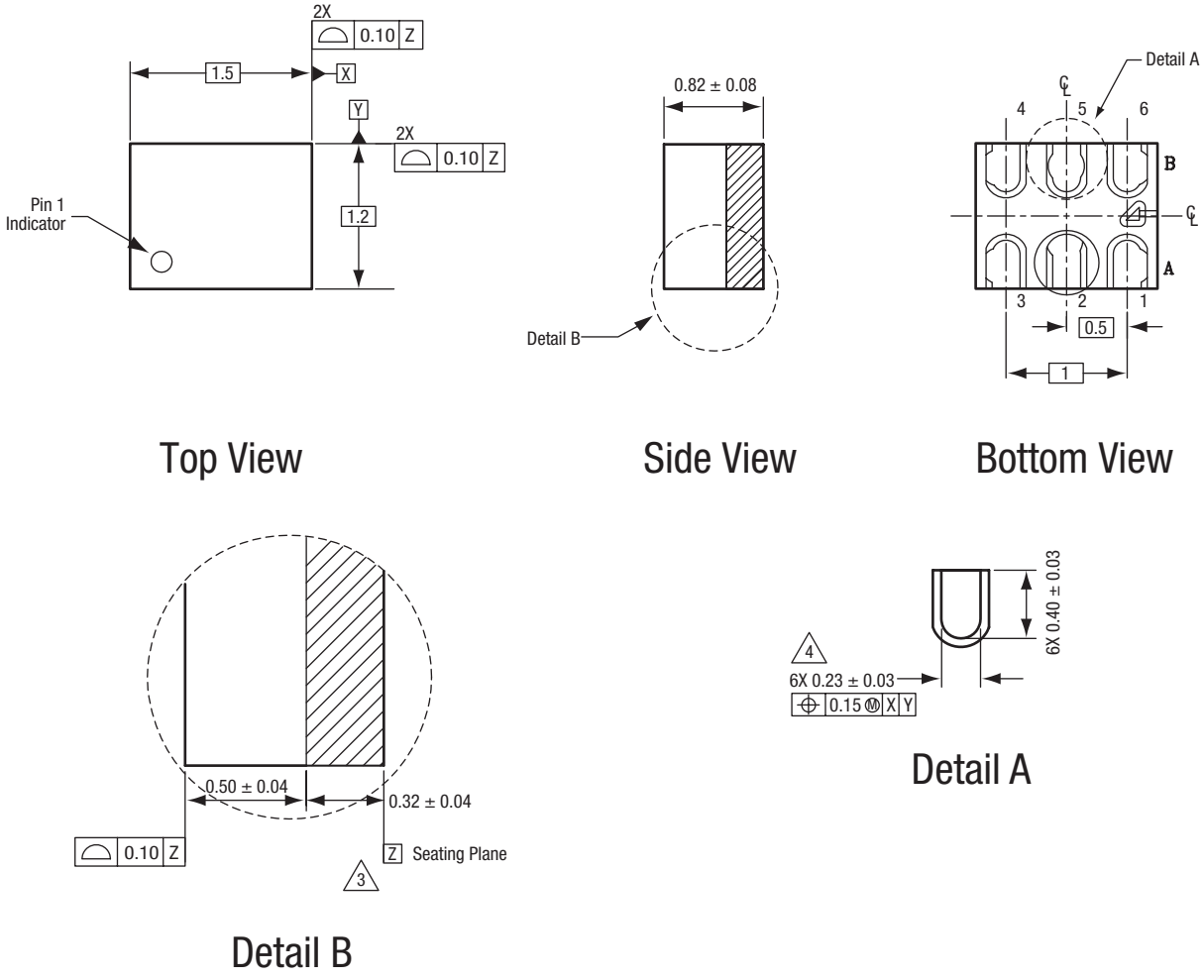


Figure 9. Typical Part Markings (Top View)



All measurements are in millimeters.
Dimensioning and tolerancing according to ASME Y14.5M-1994.
Primary datum –Z– is seating plane.
Lead width is measured at the maximum land diameter, parallel to primary datum –Z–.
Termination metalization is gold.

S1615

Figure 10. AS211-334 6-Pin LGA Package Dimensions

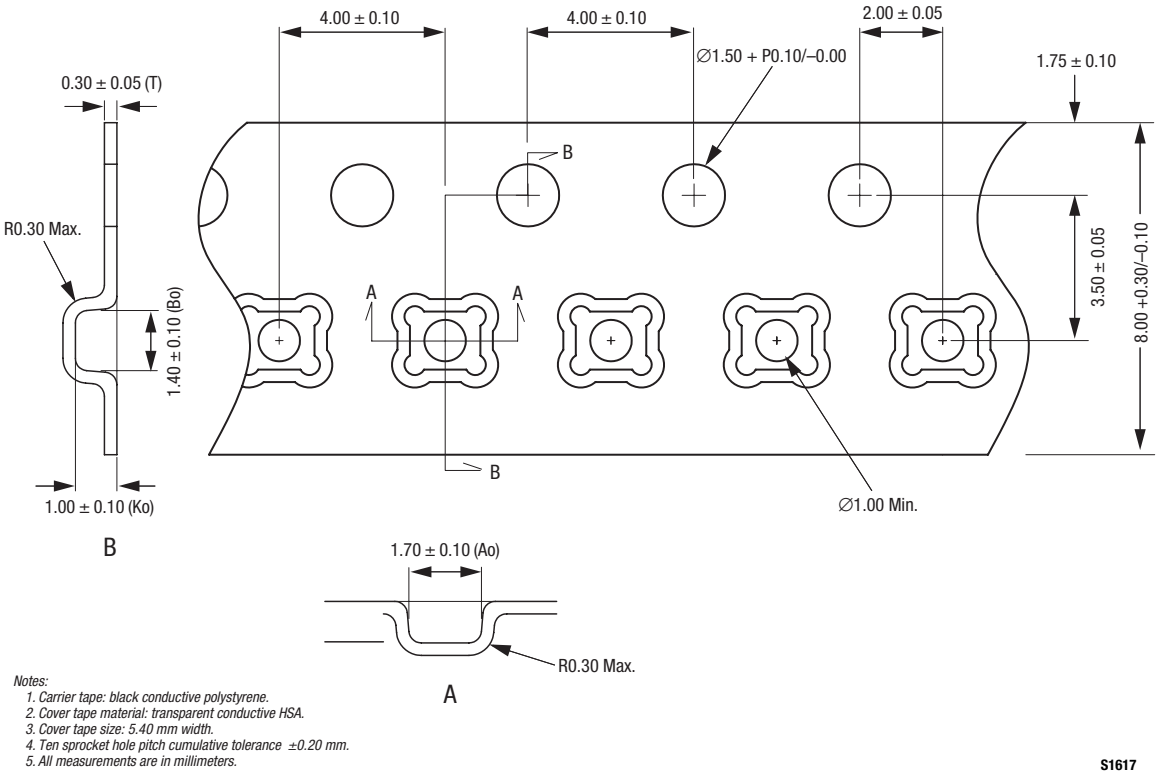


Figure 11. AS211-334 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
AS211-334 SPDT Switch	AS211-334 (Pb-free package)	SK39653, rev. 2