

PM50CL1A120

FLAT-BASE TYPE
INSULATED PACKAGE

PM50CL1A120



FEATURE

Inverter + Drive & Protection IC

- a) Adopting new 5th generation Full-Gate CSTBT™ chip
- b) The over-temperature protection which detects the chip surface temperature of CSTBT™ is adopted.
- c) Error output signal is possible from all each protection upper and lower arm of IPM.
- d) Compatible L-series package.

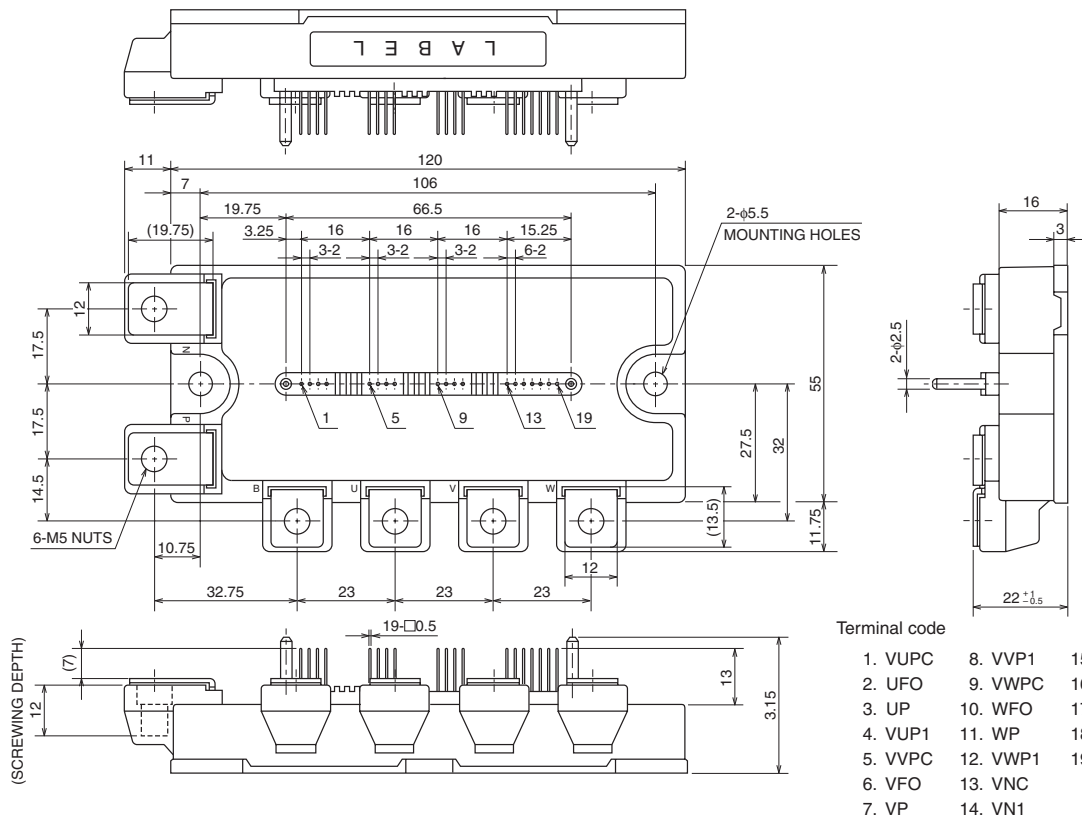
- 3φ 50A, 1200V Current-sense and temperature sense IGBT type inverter
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-FO available from upper arm devices)
- UL Recognized

APPLICATION

General purpose inverter, servo drives and other motor controls

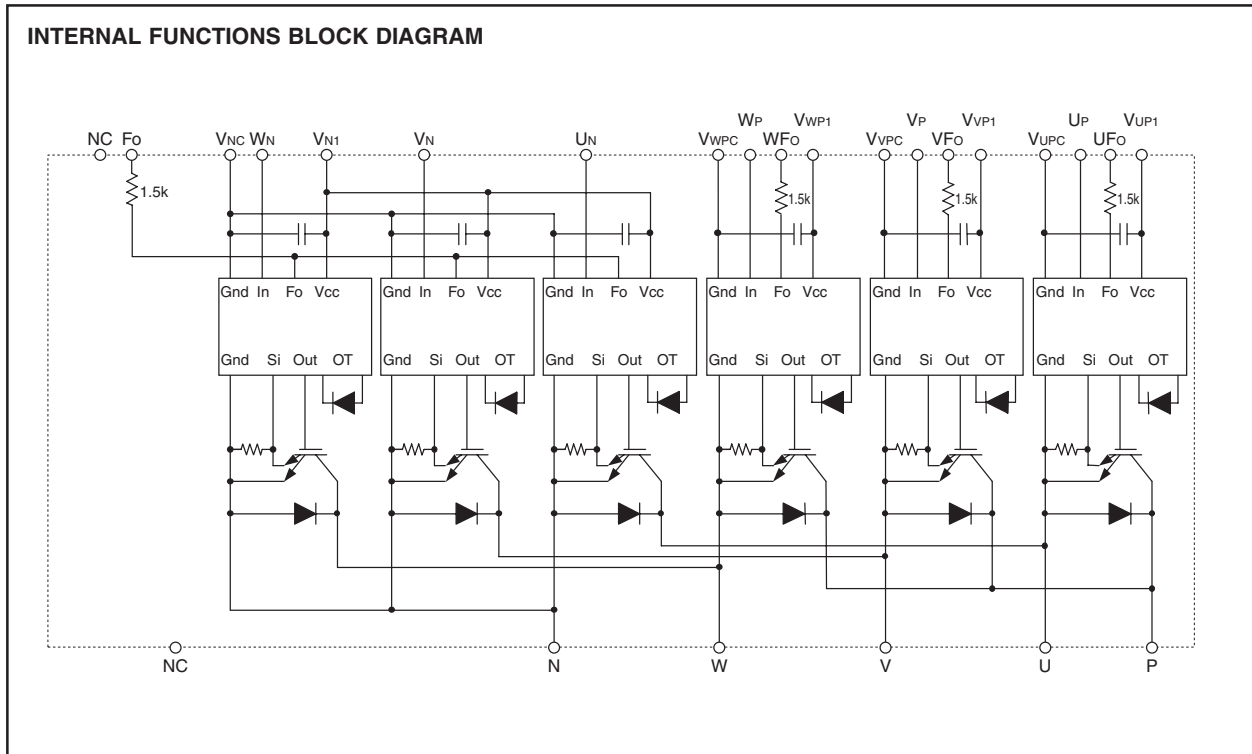
PACKAGE OUTLINES

Dimensions in mm



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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	$V_D = 15\text{V}$, $V_{CIN} = 15\text{V}$	1200	V
$\pm I_C$	Collector Current	$T_C = 25^\circ\text{C}$ (Note-1)	50	A
$\pm I_{CP}$	Collector Current (Peak)	$T_C = 25^\circ\text{C}$	100	A
P_C	Collector Dissipation	$T_C = 25^\circ\text{C}$ (Note-1)	462	W
T_j	Junction Temperature		$-20 \sim +150$	$^\circ\text{C}$

*: T_C measurement point is just under the chip.

CONTROL PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Supply Voltage	Applied between : $V_{UP1}-V_{UPC}$, $V_{VP1}-V_{VPC}$ $V_{WP1}-V_{WPC}$, $V_{N1}-V_{NC}$	20	V
V_{CIN}	Input Voltage	Applied between : U_P-V_{UPC} , V_P-V_{VPC} , W_P-V_{WPC} $U_N \cdot V_N \cdot W_N - V_{NC}$	20	V
V_{FO}	Fault Output Supply Voltage	Applied between : $U_{FO}-V_{UPC}$, $V_{FO}-V_{VPC}$, $W_{FO}-V_{WPC}$ $F_O - V_{NC}$	20	V
I_{FO}	Fault Output Current	Sink current at U_{FO} , V_{FO} , W_{FO} , F_O terminals	20	mA

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TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Supply Voltage Protected by SC	V _D = 13.5 ~ 16.5V Inverter Part, T _j = +125°C Start	800	V
VCC(surge)	Supply Voltage (Surge)	Applied between : P-N, Surge value	1000	V
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V _{rms}

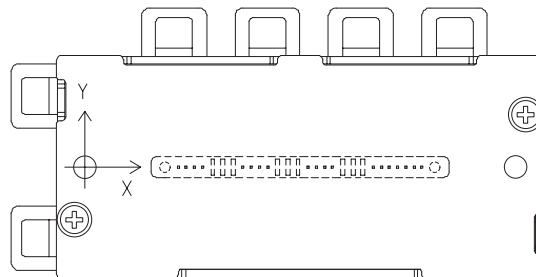
THERMAL RESISTANCES

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	Inverter IGBT part (per 1 element) (Note-1)	—	—	0.27	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1 element) (Note-1)	—	—	0.47	
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied (Note-1)	—	—	0.038	

* If you use this value, R_{th(f-a)} should be measured just under the chips.

(Note-1) T_C (under the chip) measurement point is below. (unit : mm)

axis \ arm	UP		VP		WP		UN		VN		WN	
	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X	28.6	28.6	65.4	65.4	87.4	87.4	38.6	38.6	54.6	54.6	76.6	76.6
Y	-8.4	0.2	-8.4	0.2	-8.4	0.2	6.8	-1.8	6.8	-1.8	6.8	-1.8



Bottom view

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

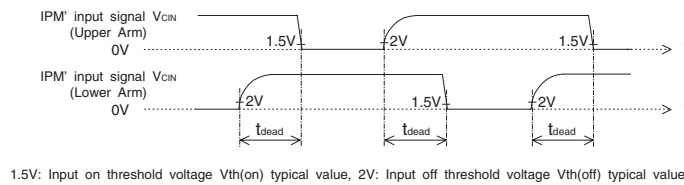
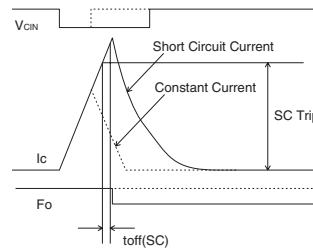
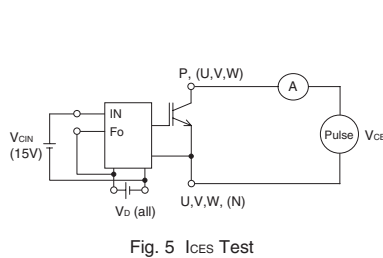
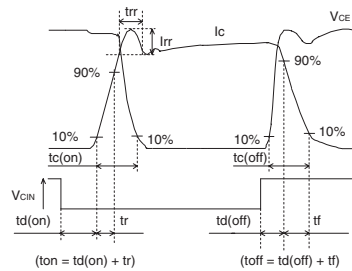
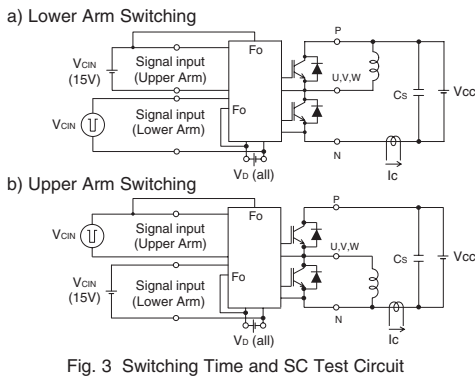
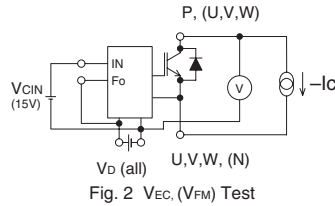
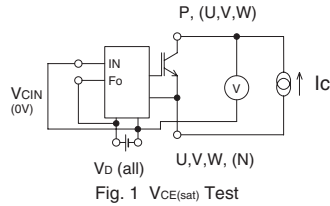
Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 50A V _{CE} = 0V, Pulsed (Fig. 1)	—	1.65	2.15	V
		T _j = 25°C	—	1.85	2.35	
V _{EC}	FWDi Forward Voltage	-I _C = 50A, V _D = 15V, V _{CE} = 15V (Fig. 2)	—	2.3	3.3	V
t _{on}	Switching Time	V _D = 15V, V _{CE} = 0V ↔ 15V V _{CE} = 600V, I _C = 50A T _j = 125°C Inductive Load (Fig. 3,4)	0.3	0.8	2.0	μs
t _{tr}			—	0.3	0.8	
t _{c(on)}			—	0.4	1.0	
t _{off}			—	1.2	2.8	
t _{c(off)}			—	0.4	1.2	
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CE(sat)} , V _D = 15V (Fig. 5)	—	—	1	mA
		T _j = 125°C	—	—	10	

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PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)



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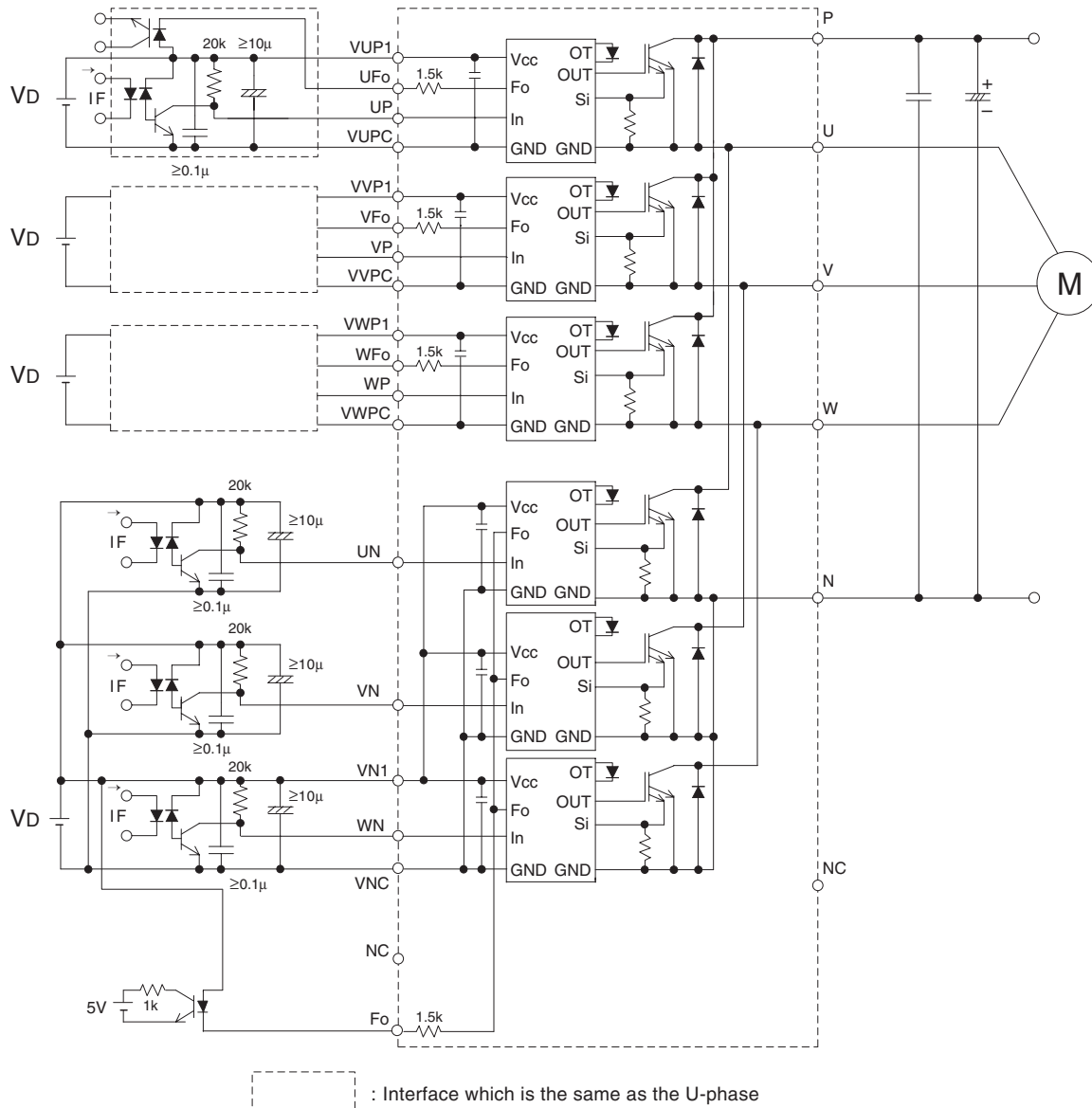


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

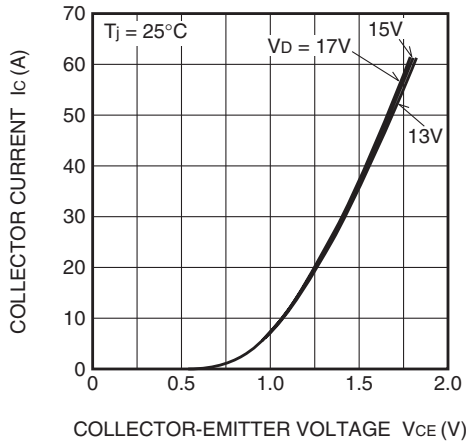
- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.

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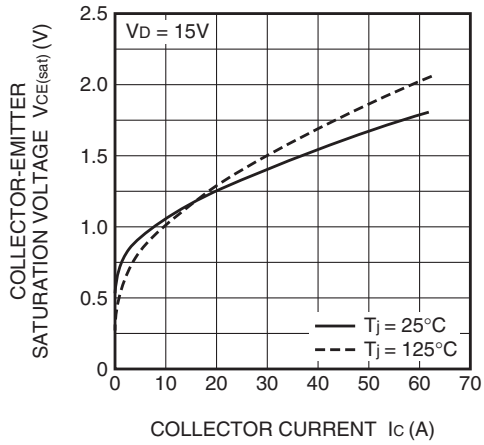
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PERFORMANCE CURVES

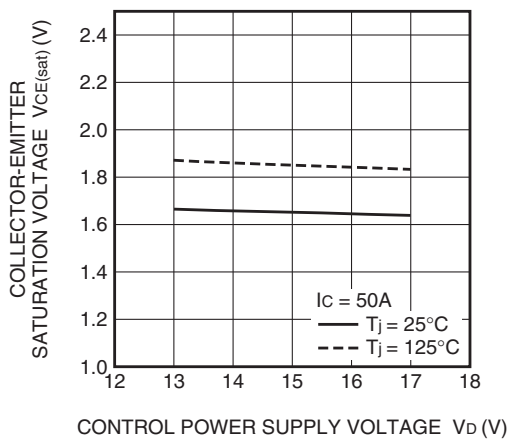
OUTPUT CHARACTERISTICS (TYPICAL)



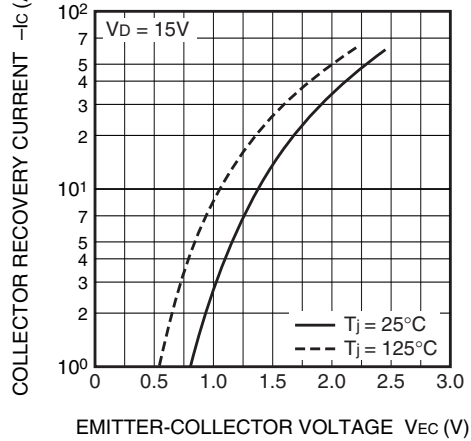
COLLECTOR-EMITTER SATURATION VOLTAGE (VS. I_c) CHARACTERISTICS (TYPICAL)



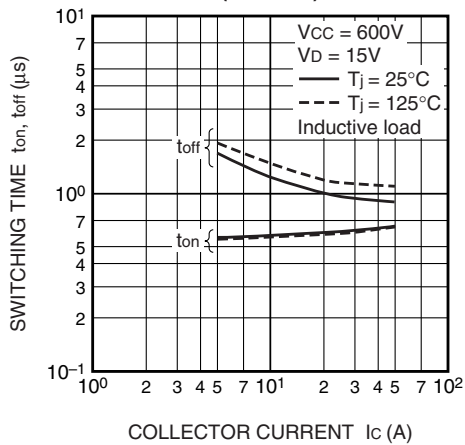
COLLECTOR-EMITTER SATURATION VOLTAGE (VS. V_D) CHARACTERISTICS (TYPICAL)



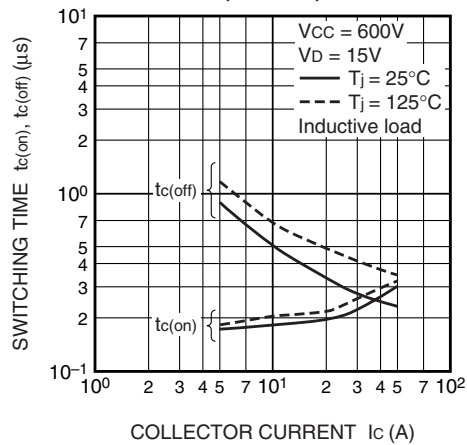
DIODE FORWARD CHARACTERISTICS (TYPICAL)



SWITCHING TIME (t_{on} , t_{off}) CHARACTERISTICS (TYPICAL)



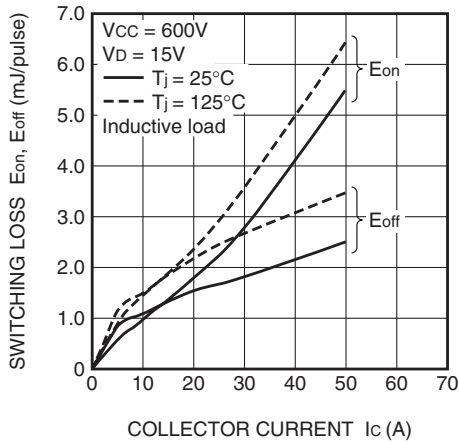
SWITCHING TIME ($t_{c(on)}$, $t_{c(off)}$) CHARACTERISTICS (TYPICAL)



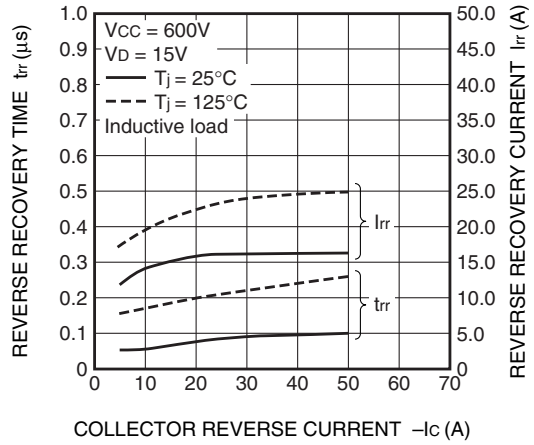
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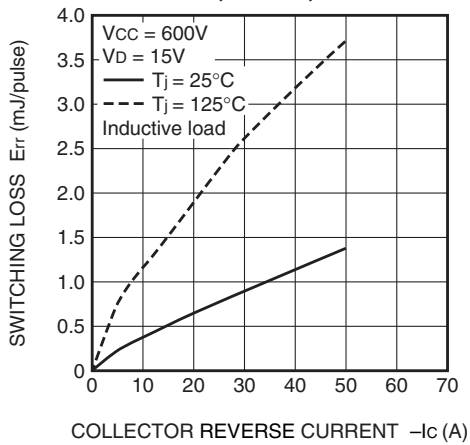
SWITCHING LOSS CHARACTERISTICS (TYPICAL)



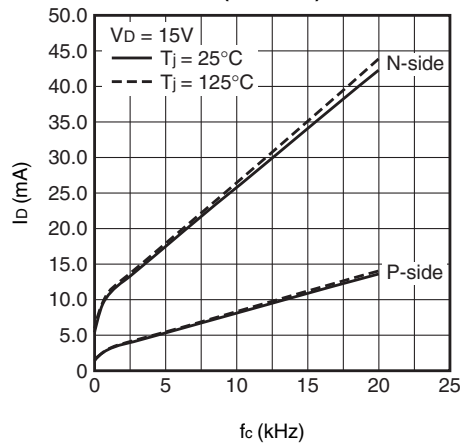
DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)



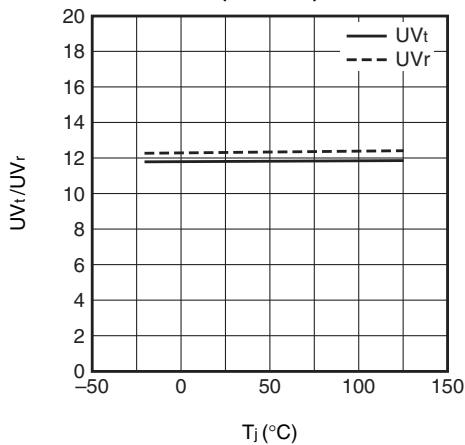
SWITCHING RECOVERY LOSS CHARACTERISTICS (TYPICAL)



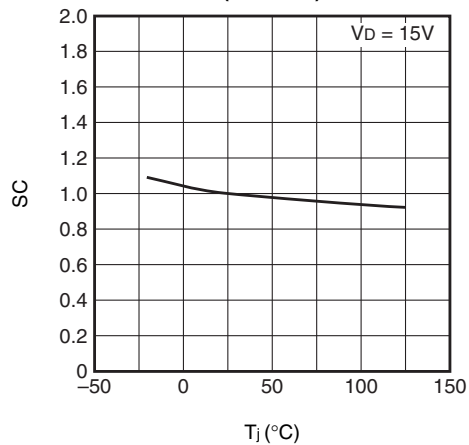
I_D VS. f_c CHARACTERISTICS (TYPICAL)



UV TRIP LEVEL VS. T_j CHARACTERISTICS (TYPICAL)



SC TRIP LEVEL VS. T_j CHARACTERISTICS (TYPICAL)



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