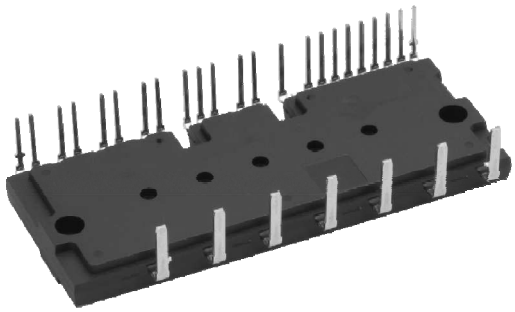
PS21A7A

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21A7A



MAIN FUNCTION AND RATINGS

- 3 phase inverter with N-side open emitter structure
- 600V / 75A (CSTBT)

APPLICATION

- AC100 ~ 200Vrms class, motor control

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC),
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply)
- Temperature monitoring : Analog output of LVIC temperature
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Approved : File No. E80276

MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V
V_{CES}	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	T_C= 25°C	75	A
$\pm I_{CP}$	Each IGBT collector current (peak)	T_C= 25°C, less than 1ms	150	A
P_C	Collector dissipation	T_C= 25°C, per 1 chip	162	W
T_j	Junction temperature		-20~+150	°C

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_j = 125°C, non-repetitive, less than 2μs	400	V
T_C	Module case operation temperature	(Note 1)	-20~+100	°C
T_{stg}	Storage temperature		-40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1minute, between connected all pins and heat-sink plate	2500	V_{rms}

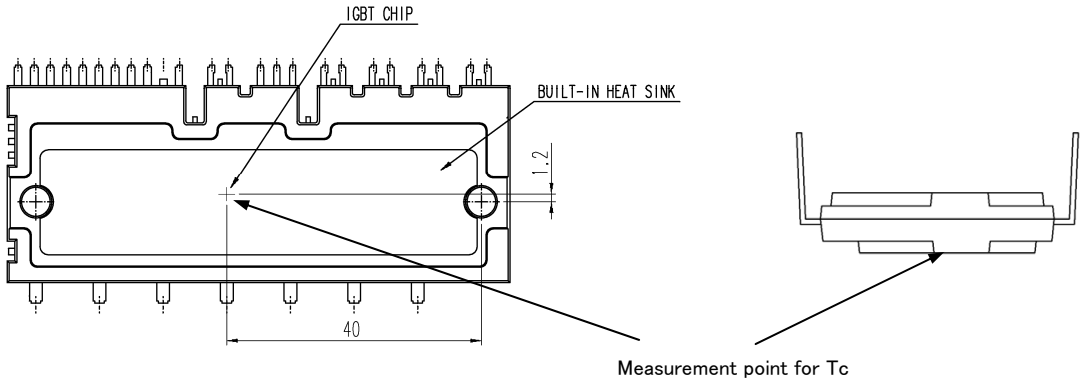
Note 1: Tc measurement point is described in Fig.1.

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 2)	Inverter IGBT part (per 1/6 module)	-	-	0.77	°C/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	1.25	°C/W

Note 2: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat-sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.2°C/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m•k).

Fig. 1: T_C MEASUREMENT POINT



ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D=V_{DB} = 15V, V_{IN}= 5V, I_C= 75A	T_j= 25°C	-	1.55	2.05	V
			T_j= 125°C	-	1.65	2.10	
V_{EC}	FWDi forward voltage	-I_C= 75A, V_{IN}= 0V		-	1.70	2.20	V
t_{on}	Switching times	V_{CC}= 300V, V_D= V_{DB}= 15V, I_C= 75A, T_j= 125°C, V_{IN}= 0↔5 V, Inductive Load (upper-lower arm)		1.80	2.40	3.60	μs
$t_{C(on)}$				-	0.40	0.60	μs
t_{off}				-	3.40	4.80	μs
$t_{C(off)}$				-	0.60	1.20	μs
t_{rr}				-	0.30	-	μs
I_{CES}	Collector-emitter cut-off current	V_{CE}=V_{CES}	T_j= 25°C	-	-	1	mA
			T_j= 125°C	-	-	10	

CONTROL (PROTECTION) PART

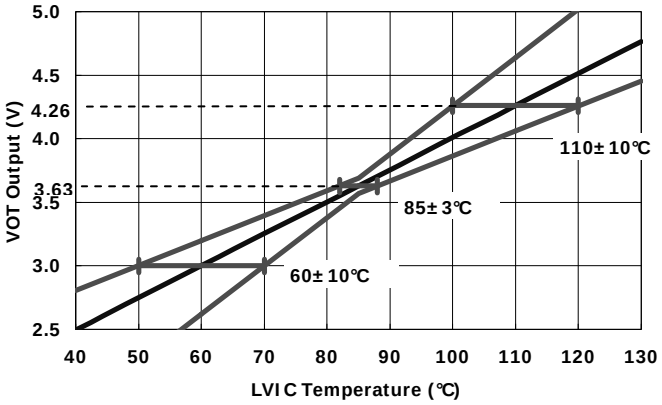
Symbol	Parameter	Condition			Limits			Unit
					Min.	Typ.	Max.	
I_D	Circuit current	Total of V_{P1}-V_{PC}, V_{N1}-V_{NC}	V_D = 15V, V_{IN} = 0V		-	-	5.50	mA
			V_D = 15V, V_{IN} = 5V		-	-	5.50	
I_{DB}	Circuit current	V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	V_D = V_{DB} = 15V, V_{IN} = 0V		-	-	0.55	
			V_D = V_{DB} = 15V, V_{IN} = 5V		-	-	0.55	
I_{SC}	Short circuit trip level	-20°C≤Tj≤125°C, Rs= 23.2Ω (±1%), Not connecting outer shunt resistors to NU,NV,NW terminals (Note 3)			127	-	-	A
UV_{DBt}	Control supply under-voltage protection	T_j ≤125°C	P-side	Trip level	10.0	-	12.0	V
UV_{DBr}				Reset level	10.5	-	12.5	V
UV_{Dt}			N-side	Trip level	10.3	-	12.5	V
UV_{Dr}				Reset level	10.8	-	13.0	V
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pull-up to 5V by 10kΩ			4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA			-	-	0.95	V
t_{FO}	Fault output pulse width	C_{FO}=22nF (Note 4)			1.6	2.4	-	ms
I_{IN}	Input current	V_{IN} = 5V			0.7	1.0	1.5	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}			2.1	2.3	2.6	V
$V_{th(off)}$	OFF threshold voltage				0.8	1.4	2.1	V
V_{OT}	Temperature output	LVIC temperature = 85°C (Note 5)			3.57	3.63	3.69	V

Note 3 : Short circuit protection can work for N-side IGBTs only. Isc level can change by sense resistance. For details, please refer the application note for this DIPIPM or contact us. And in that case, it should be for sense resistor to be larger resistance than the value mentioned above.

4 : Fault signal is output when short circuit or N-side control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO}. (C_{FO} (typ.) = t_{FO} x (9.1 x 10^{-6}) [F])

5 : DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM. And this output might exceed 5V when temperature rises excessively, so it is recommended for protection of control part like MCU to insert a clamp Di between supply (e.g. 5V) for control part and this output. Temperature of LVIC vs. V_{OT} output characteristics is described in Fig.2

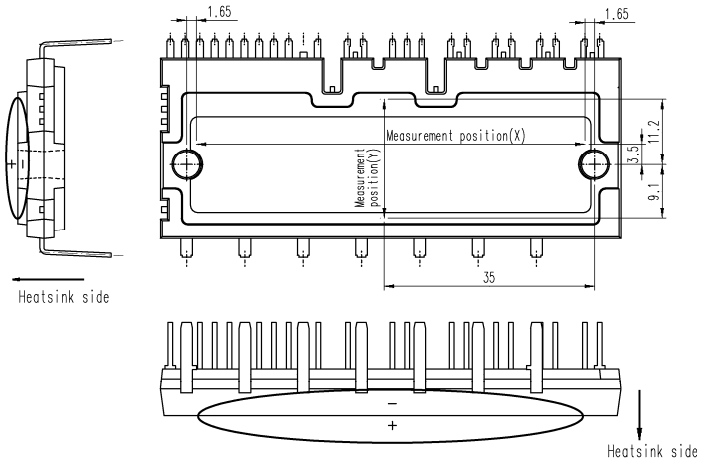
Fig.2 Temperature of LVIC - V_{OT} output characteristics



MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4	Recommended 1.18N・m	0.98	1.18	1.47	N・m
Terminal pulling strength	Load 19.6N	EIAJ-ED-4701	10	-	-	s
Terminal bending strength	Load 9.8N, 90deg. bend	EIAJ-ED-4701	2	-	-	times
Weight			-	46	-	g
Heat-sink flatness		(Note 6)	-50	-	100	μm

Note 6: Measurement point of heat-sink flatness

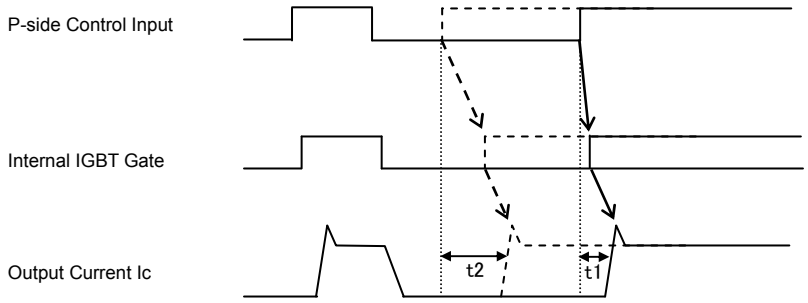


RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-NU, NV, NW		0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}		13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation			-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal, $T_C \leq 100°C$		2.7	-	-	μs
f_{PWM}	PWM input frequency	$T_C \leq 100°C$, $T_j \leq 125°C$		-	-	20	kHz
I_O	Allowable r.m.s. current	V_{CC} = 300V, V_D = 15V, P.F = 0.8, Sinusoidal PWM $T_C \leq 100°C$, $T_j \leq 125°C$ (Note 7)	f_{PWM}= 5kHz	-	-	35.0	Arms
			f_{PWM}= 15kHz	-	-	17.0	
PWIN(on)	Minimum input pulse width	200≤ V_{CC} ≤ 350V, 13.5≤ V_D ≤ 16.5V, 13.0≤ V_{DB} ≤ 18.5V, -20°C ≤ T_C ≤ 100°C, N line wiring inductance less than 10nH (Note 9)	(Note 8)	1.3	-	-	μs
PWIN(off)			I_C≤75A	3.0	-	-	
			75<I_C≤127.5A	5.0	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)		-5.0	-	+5.0	V
T_j	Junction temperature			-20	-	+125	°C

Note 7: The allowable r.m.s. current value depends on the actual application conditions.
8: DIPIPM might not make response to the input on signal with pulse width less than PWIN (on).
9: IPM might make no response or delayed response (at P-side IGBT only) for the input signal with off pulse width less than PWIN(off). Please refer Fig. 3 about delayed response.

Fig. 3 About Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only)



Solid line ···Off pulse width ≥ PWIN(off);
Turn on time t1 (Normal delay)
Broken line ···Off pulse width < PWIN(off);
Turn on time t2 (Longer delay in some cases)

Fig. 4 INTERNAL CIRCUIT

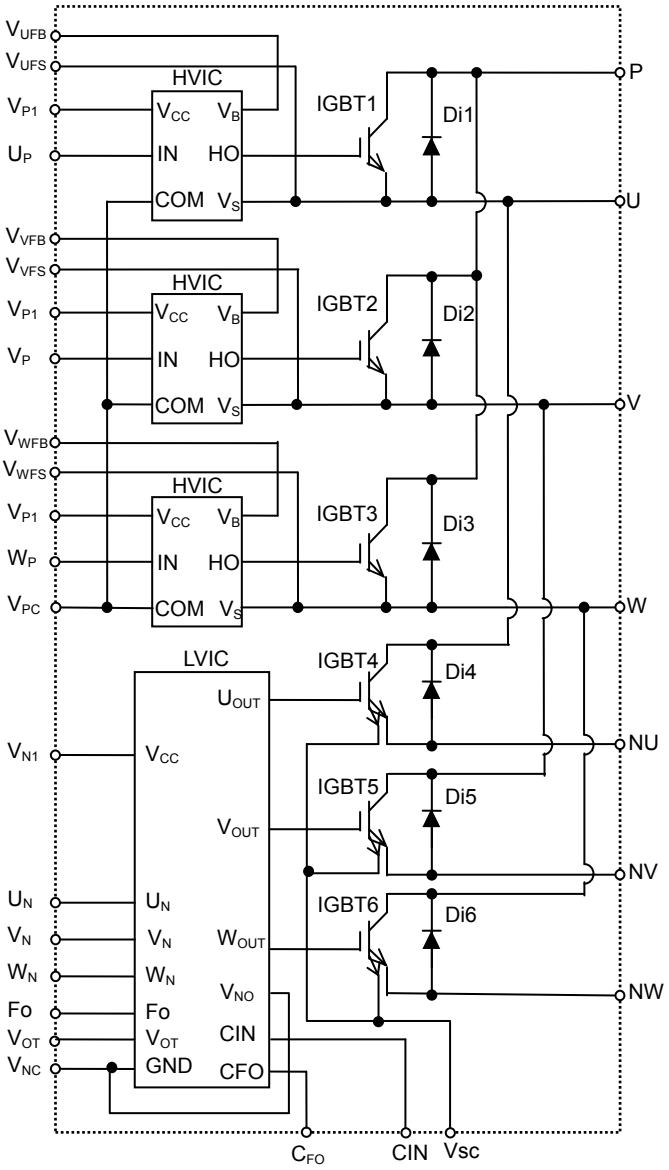
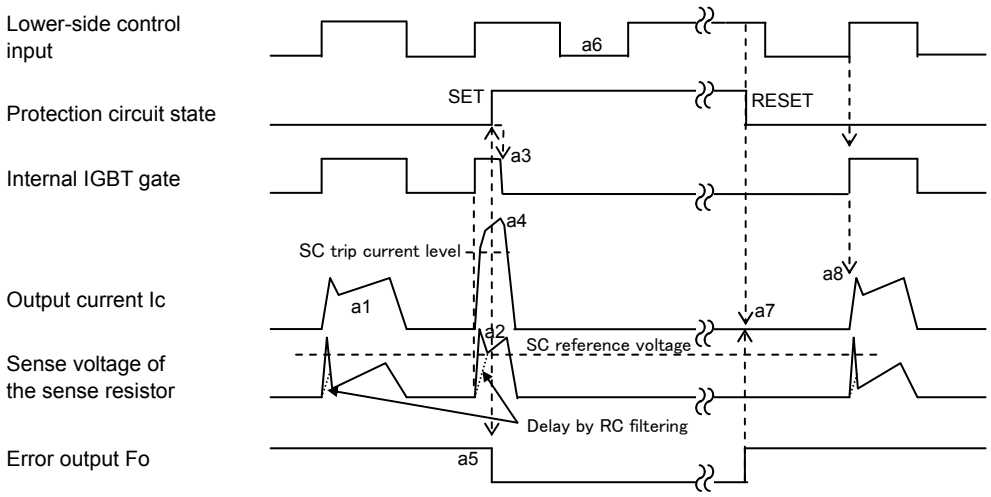


Fig. 5 TIMING CHARTS OF THE DIPIPM PROTECTIVE FUNCTIONS

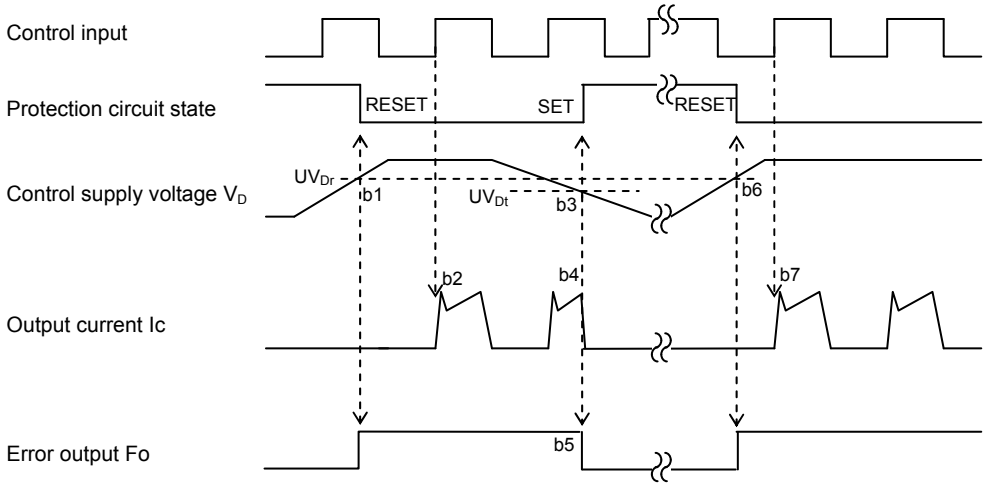
[A] Short-Circuit Protection (N-side only with the external sense resistor and RC filter)

a1. Normal operation: IGBT ON and outputs current.
a2. Short circuit current detection (SC trigger) (It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC.)
a3. All N-side IGBT's gates are hard interrupted.
a4. All N-side IGBTs turn OFF.
a5. F_O outputs with a fixed pulse width determined by the external capacitor C_{FO}.
a6. Input = "L": IGBT OFF
a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: IGBT ON and outputs current.



[B] Under-Voltage Protection (N-side, UV_D)

b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON when inputting next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
b2. Normal operation: IGBT ON and outputs current.
b3. V_D level drops to under voltage trip level. (UV_{Dt}).
b4. All N-side IGBTs turn OFF in spite of control input condition.
b5. Fo outputs for the period determined by the capacitance $C_{FO,}$ but output is extended during V_D keeps below UV_{Dr}.
b6. V_D level reaches UV_{Dr}.
b7. Normal operation: IGBT ON and outputs current.



[C] Under-Voltage Protection (P-side, UV_{DB})

c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, IGBT can turn on when inputting next ON signal (L→H).
c2. Normal operation: IGBT ON and outputs current.
c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
c4. IGBT of corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
c5. V_{DB} level reaches UV_{DBr}.
c6. Normal operation: IGBT ON and outputs current.

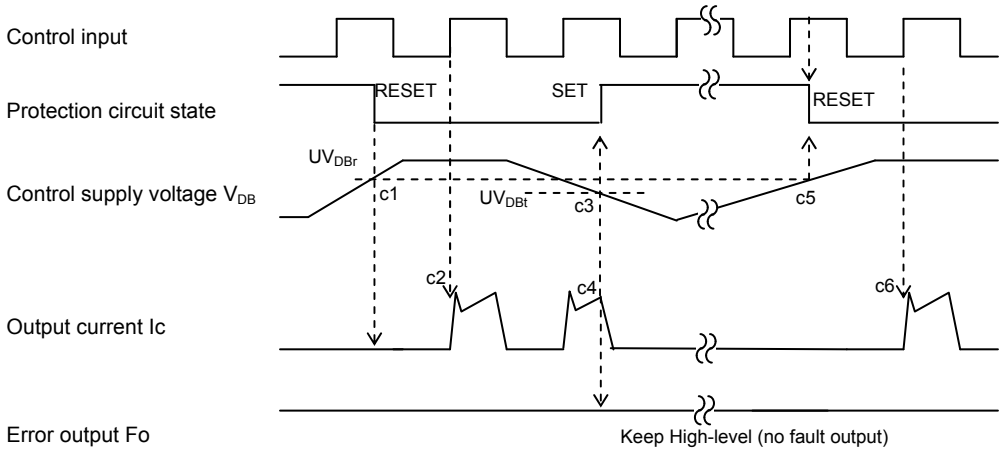
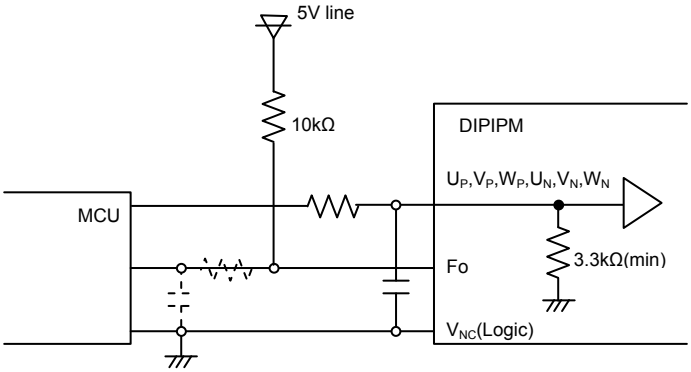


Fig. 6 MCU I/O INTERFACE CIRCUIT

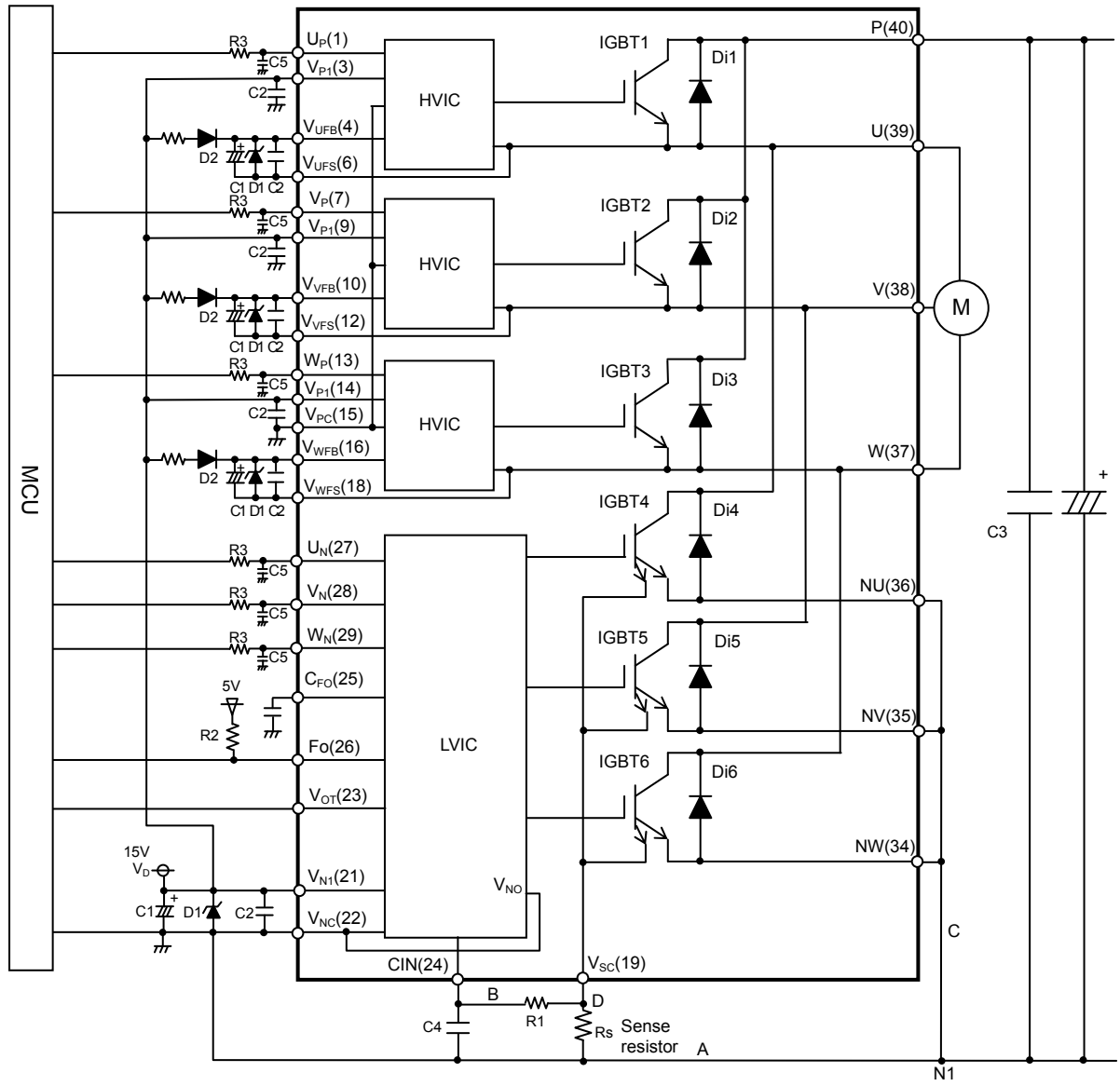


Note)

Design for input RC filter depends on the PWM control scheme used in the application and the wiring impedance of the printed circuit board. The DIPIPM input signal interface integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using RC filter, be careful to satisfy the turn-on threshold voltage requirement.

Fo output is open drain type. It should be pulled up to the positive side of 5V or 15V power supply with the resistor that limits Fo sink current I_{Fo} under 1mA. In the case of pulling up to 5V supply, over 5.1kΩ is needed. (10kΩ is recommended.)

Fig. 7 AN EXAMPLE OF APPLICATION CIRCUIT



Note

1 :If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point at which NU, NV, NW are connected to power GND line.

2 :To prevent surge destruction, the wiring between the smoothing capacitor and the P,N1 terminals should be as short as possible. Generally inserting a 0.1µ~0.22µF snubber capacitor C3 between the P-N1 terminals is recommended.

3 :The time constant R1C4 of RC filter for preventing protection circuit malfunction should be selected in the range of 1.5µs~2µs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1,C4. When R1 is too small, it will leads to delay of protection. So R1 should be min. 10 times larger resistance than Rs. (Over 100 times is recommended.)

4 :All capacitors should be mounted as close to the terminals of the DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2: 0.22µ~2.0µF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)

5 :It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.

6 :To prevent erroneous SC protection, the wiring from V_{SC} terminal to CIN filter should be divided at the point D that is close to the terminal of sense resistor. And the wiring should be patterned as short as possible.

7 :For sense resistor, the variation within 1%(including temperature characteristics), low inductance type is recommended. And the over 1/8W is recommended, but it is necessary to evaluate in your real system finally.

8 :To prevent erroneous operation, the wiring of A, B, C should be as short as possible.

9 :Fo output is open drain type. It should be pulled up to the positive side of 5V or 15V power supply with the resistor that limits Fo sink current I_{Fo} under 1mA. In the case pull up to 5V supply, over R2=5.1kΩ is needed. (10kΩ is recommended.)

10 :Error signal output width (t_{Fo}) can be set by the capacitor connected to C_{FO} terminal. C_{FO}(typ.) = t_{Fo} x (9.1 x 10^{-6}) (F)

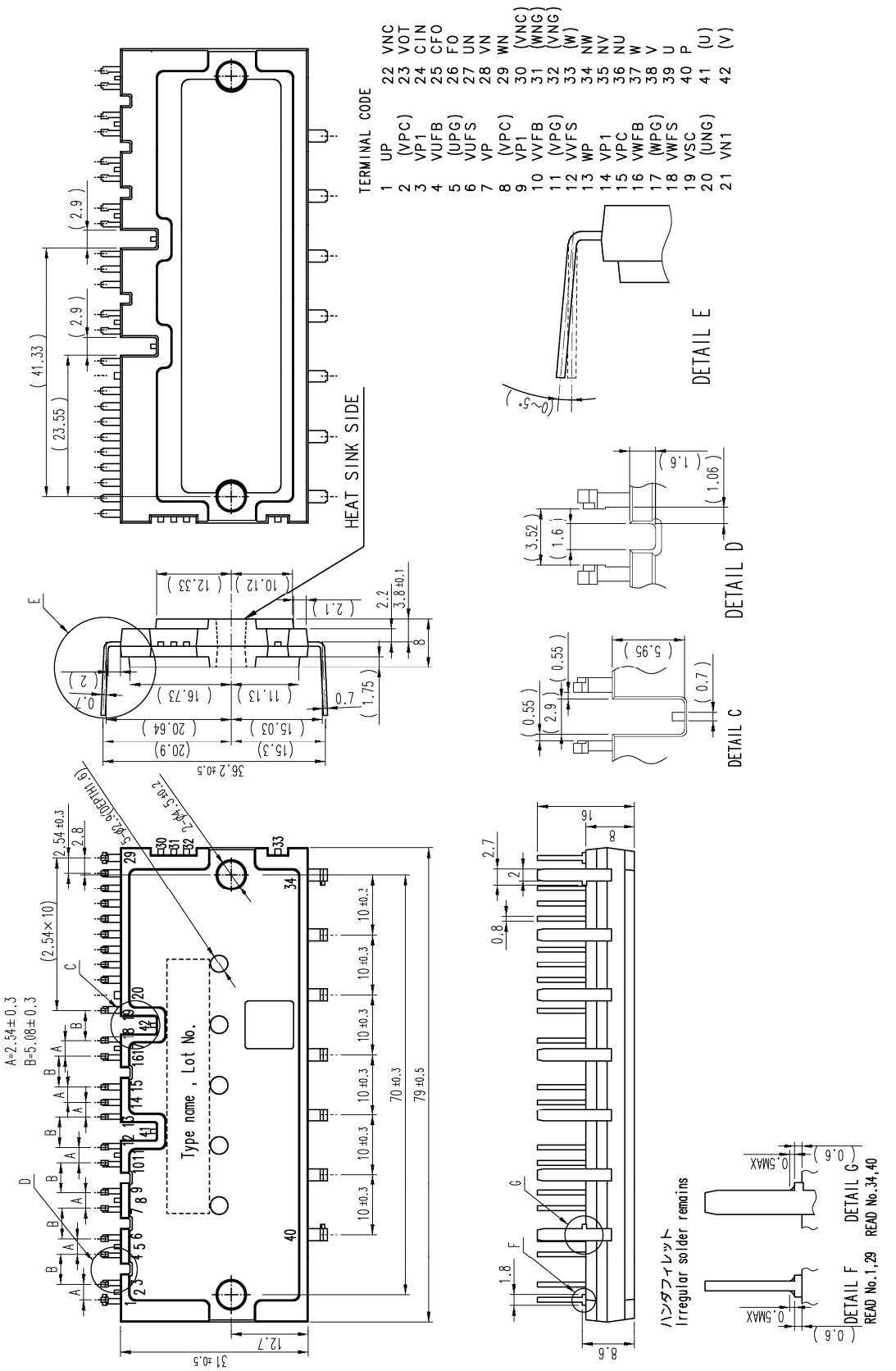
11 :High voltage (V_{RRM} =600V or more) and fast recovery type (trr=less than 100ns or less) diode D2 should be used in the bootstrap circuit.

12 :If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause erroneous operation. To avoid such problem, voltage ripple of control supply line should meet dV/dt ≤+/-1V/µs, Vripple≤2Vp-p.

13 :Input drive is High-Active type. There is a 3.3kΩ(min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be patterned as short as possible. When using RC filter R3C5, it is necessary to confirm the input signal level to meet the turn-on and turn-off threshold voltage. Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

Fig. 8 PACKAGE OUTLINES

Dimensions in mm



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