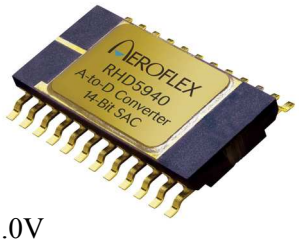
Advanced

Standard Products

RadHard-by-Design
RHD5940
14-Bit Analog to Digital Converter

www.aeroflex.com/RHDseries

January 10, 2012



FEATURES

- Single power supply operation 3.3V to 5.0V
- Radiation performance
  - Total dose: >1Mrad(Si); Dose rate = 50 - 300 rads(Si)/s
  - ELDRS Immune
  - SEL Immune >100 MeV-cm^2/mg
  - Neutron Displacement Damage >10^{12} neutrons/cm^2
- 14-Bit Digital Output
- Successive Approximation A-to-D
- Tri-State digital outputs
- Power Down (Sleep) mode
- Single or continuous conversion
- 20 clock conversion period
- Digital output available until the completion of the next conversion
- Busy (Prime) and End-of-Conversion status outputs
- 2000V Input/Output ESD protection
- Full military temperature range
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic ceramic
  - 24-pin, 0.614"L x 0.299"W x 0.120"Ht SOIC
  - Typical Weight 2 grams

- **Aeroflex Plainview's Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.**

GENERAL DESCRIPTION

Aeroflex's RHD5940 is a radiation hardened, single supply, 14-Bit Analog-to-Digital converter in a 24-pin SOIC package. The RHD5940 design uses specific circuit topology and layout methods to mitigate total ionizing dose effects and single event latchup. These characteristics make the RHD5940 especially suited for the harsh environment encountered in Deep Space missions. It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534 Class K, the RHD5940 is ideal for demanding military and space applications.

ORGANIZATION AND APPLICATION

The RHD5940 takes an analog signal and performs a 14-bit successive approximation analog-to-digital conversion in a nominal period of 20uS. The 14-Bit digital output has a tri-state control allowing the connection of multiple RHD5940s. This provides the ability to interface many voltage readings to the digital processor data bus. The full-scale range is determined by reference input voltages which will typically include any ~ 4 volt span anywhere in the power supply range (nominal 5V supply). The input impedance of the reference/span terminals is a constant 4K ohms.

Gain compression will occur near either power supply extremes but can be avoided if the references are more than 200mV away from the respective supply terminals. The input span can be less than 4 volts at the expense of ultimate resolution

The analog input impedance is primary capacitance (20pF). The input voltage charges a track-and-hold hold capacitor through transmission gates. The input bandwidth is determined by the slew rate of the hold amplifier and is adequate to allow input sampling in three clock periods (3uS nominal). The ultimate bandwidth is determined by the aperture uncertainty associated with the closing of the sample gate (approximately 5nS). The converter bandwidth is then determined by the sampling Nyquist frequency rather than the input signal; change rate (dv/dt) and the LSB weight in volts as would be the case if there were no sample and hold.

Start-Convert (STCNV_H), Busy (BUSY_L) and End-Of-Convert (EOC_H) status and control line are provided. The converter will operate in either continuous or single conversion modes. The digital output register changes at the end of a conversion and is available until the next End-Of-Convert. Digital input and output circuits operate from a voltage independent of the remainder of the chip such that I/O is compatible with digital systems from less than 3.3 to 5 volts.

The converter divides the reference voltage into 16 segments with a linear weighted resistor network. The voltage on any segment is passed to a linear 10-bit DAC for interpolation. The architecture is inherently capable of monotonic operation. INL is ±10 LSBs. DNL is ±1/2 LSB. The sampled input voltage is compared to the output of the two stage DAC for a 14-bit successive approximation conversion.

All inputs are protected to both power supply rails by semiconductor diodes. Inputs should be constrained to Vcc +0.4 and Vee-0.4 to avoid forward biasing protection paths.

The devices will not latch with SEU events to above 100 MeV-cm^2/mg. Total dose degradation is minimal to above 1Mrad(Si). Displacement damage environments to neutron fluence equivalents in the mid 10^{12} neutrons per cm^2 range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependant.

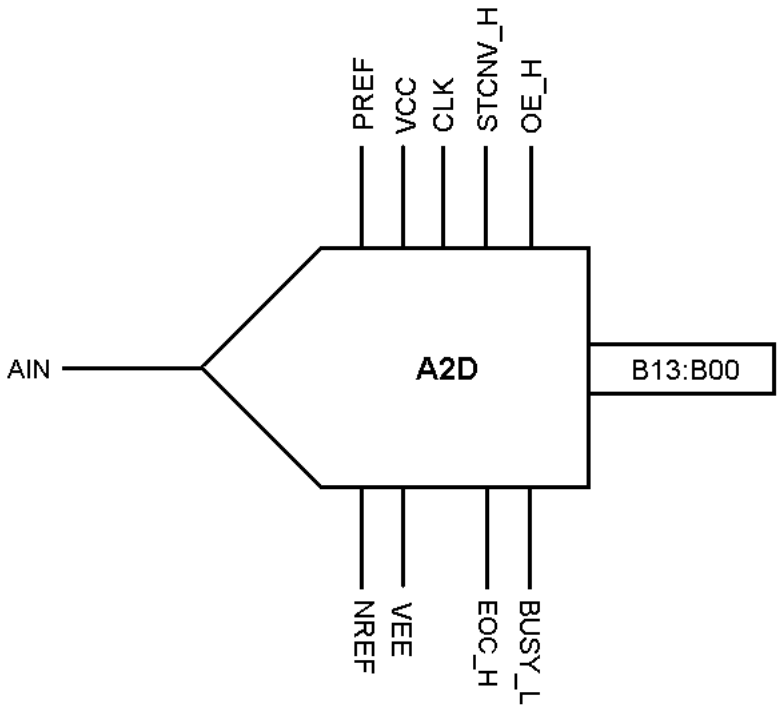


FIGURE 1: BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	+150	°C
Supply Voltage VCC - VEE	+6.0	V
Input Voltage	VCC +0.4 VEE -0.4	V
Lead Temperature (soldering, 10 seconds)	300	°C
Thermal Resistance, Junction to Case, Θjc	3.5	°C/W
ESD Rating	2.0	KV
Power @25°C	TBD	mW

NOTICE: Stresses above those listed under “Absolute Maximums Rating” may cause permanent damage to the device. These are stress rating only; functional operation beyond the “Operation Conditions” is not recommended and extended exposure beyond the “Operation Conditions” may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Typical	Units
+VCC	Power Supply Voltage	5.0	V

ELECTRICAL PERFORMANCE CHARACTERISTICS

(TC = -55°C TO +125°C, +VCC = +5.0V -- UNLESS OTHERWISE SPECIFIED)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current Sleep	ICC_S				TBD	mA
Supply Current Static	ICC_Q				TBD	mA
Supply Current Dynamic	ICC_D				TBD	mA
High Analog Reference Voltage	PREF		1	4	VCC	V
Low Analog Reference Voltage	NREF			VEE		V
Full-scale Input Range			0		PREF - NREF	V
Operating Range			-0.1		PREF - NREF +0.1	V
Input Capacitance				40		pF
Effective Number of Bits	EOB			14		BITS
Integral Non Linearity	INL			0.5		LSB
Differential Non Linearity	DNL			0.5		LSB
DC Offset					TBD	V
DC Gain			TBD			V
Input Range			1	4	5	V
Reference Input Current					TBD	mA

ELECTRICAL PERFORMANCE CHARACTERISTICS (continued)

(TC = -55°C TO +125°C, +VCC = +5.0V -- UNLESS OTHERWISE SPECIFIED)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Maximum Sampling Rate	fSAMPLE(MAX)			25		KSPS
Conversion Time	tCONV			16		Clk Cycles
Acquisition Time	tACQ			4		Clk Cycles
Signal to Noise Ratio	SNR			TBD		dB

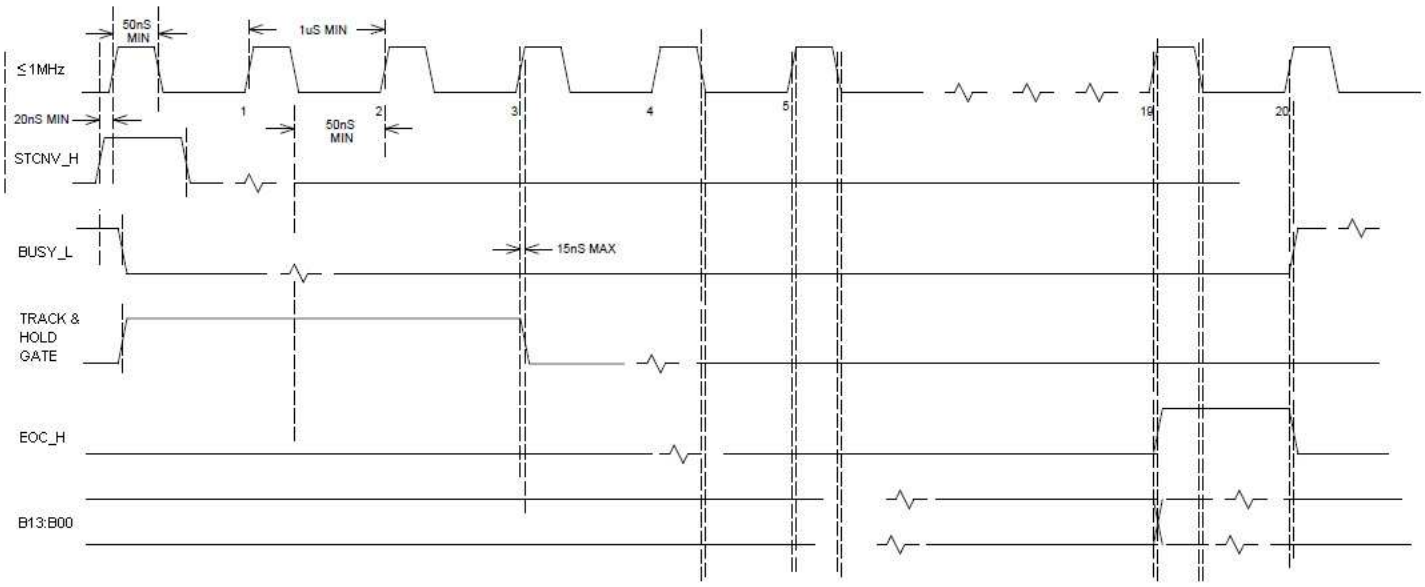


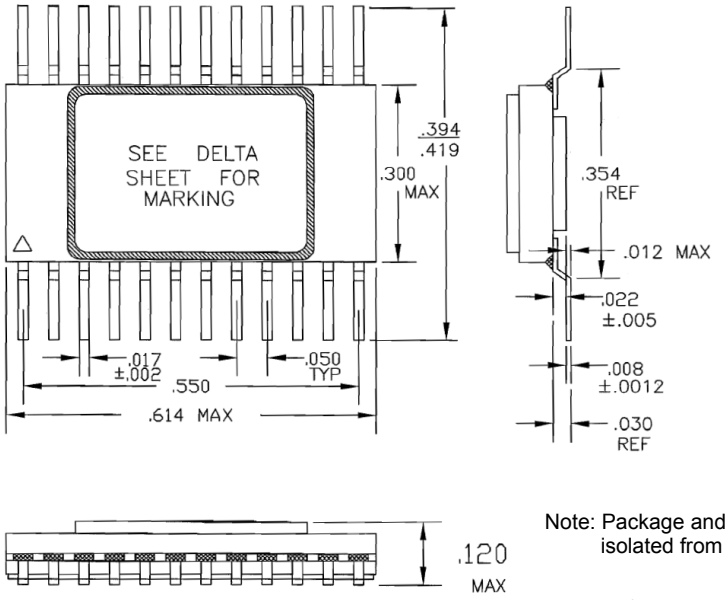
FIGURE 2: BASIC TIMING DIAGRAM

Pin #	Signal	Definition
1	AIN	Analog Input
2	NREF	Low Analog Reference Voltage
3	VCC	Supply Voltage
4	STCNV_H	Start Conversion
5	OE_H	Output Enable
6	CLK	Clock Input
7	B00	Digital Output 00
8	B01	Digital Output 01
9	B02	Digital Output 02
10	B03	Digital Output 03
11	B04	Digital Output 04
12	B05	Digital Output 05
13	B06	Digital Output 06
14	B07	Digital Output 07
15	B08	Digital Output 08
16	B09	Digital Output 09
17	B10	Digital Output 10
18	B11	Digital Output 11
19	B12	Digital Output 12
20	B13	Digital Output 13
21	EOC_H	End of Convert
22	BUSY_L	Busy
23	VEE	Supply Return
24	PREF	High Analog Reference Voltage

FIGURE 3: PACKAGE PIN-OUT AND SIGNAL DEFINITION

ORDERING INFORMATION

Model	DLA SMD #	Screening	Package
RHD5940-7	-	Commercial Flow, +25°C testing only	24-pin SOIC Package
RHD5940-S	-	Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
RHD5940-201-1S	Pending	DLA SMD Pending	
RHD5940-201-2S	Pending		
RHD5940-901-1S	Pending	DLA SMD and Radiation Certification Pending	
RHD5940-901-2S	Pending		



Note: Package and lid are electrically isolated from signal pads.

FIGURE 4: PACKAGE OUTLINE

EXPORT CONTROL:

This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Department of State is required prior to the export of this product from the United States.

EXPORT WARNING:

Aeroflex's military and space products are controlled for export under the International Traffic in Arms Regulations (ITAR) and may not be sold or proposed or offered for sale to certain countries. (See ITAR 126.1 for complete information.)

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