

RadHard-by-Design

RHD5958 8-Channel Multiplexed 14-Bit Analog-to-Digital Converter

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January 22, 2013



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FEATURES

- Single power supply operation 5.0V or Dual supply 5.0V with 3.3V for output drivers.
- Radiation performance
 - Total dose: > 1 Mrad(Si); Dose rate = 50 - 300 rads(Si)/s
 - ELDRS Immune
 - SEL Immune > 100 MeV-cm²/mg
 - Neutron Displacement Damage > 10¹⁴ neutrons/cm²
- 8-Channel Input Multiplexer
- Successive Approximation A-to-D
- Level Shifting Digital I/O Receiver/Drivers allow interfaces to 5.0 or 3.3 volt logic
- Tri-State digital outputs
- Power Down (Sleep) mode
- Single or continuous conversion
- 20 clock conversion period
- Digital output available until the completion of the next conversion
- Multiplexer address is latched on first clock rising edge of a cycle
- Busy (Prime) and End-of-Conversion status outputs
- 2000V Input/Output ESD protection
- Full military temperature range
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic Ceramic
 - 40 leads, 0.600" Sq x 0.120"Ht quad flat pack
 - Weight - 4.5 grams max
- **Aeroflex Plainview's Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.**

GENERAL DESCRIPTION

Aeroflex's RHD5958 is a radiation hardened, single supply, 8-Channel Multiplexed Analog-to-Digital converter in a 40-pin Ceramic Quad Flat Package. The RHD5958 design uses specific circuit topology and layout methods to mitigate total ionizing dose effects and single event latchup. These characteristics make the RHD5958 especially suited for the harsh environment encountered in Deep Space missions. It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534 Class K, the RHD5958 is ideal for demanding military and space applications.

ORGANIZATION AND APPLICATION

The RHD5958 takes 8 analog sensor signals and using 3 address inputs and an enable input, selects one of the 8 analog inputs and performs a 14-bit successive approximation analog-to-digital conversion in a nominal period of 40uS. The 14-bit digital output has a tri-state control allowing the connection of multiple RHD5958s. This provides the ability to interface many sensor voltage readings to the digital processor data bus. The full-scale range is determined by reference input voltages which will typically include any ~ 4 volt span anywhere in the power supply range (nominal 5V supply). The input impedance of the reference/span terminals is a constant 4K ohms.

Gain compression will occur near either power supply extremes but can be avoided if the references are more than 200mV away from the respective supply terminals. The input span can be less than 4 volts at the expense of ultimate resolution

The analog channels input impedance is primary capacitance (20pF). The input voltage charges a track-and-hold hold capacitor through transmission gates. The input bandwidth is determined by the slew rate of the hold amplifier and is adequate to allow input sampling in three clock periods (6uS nominal). The ultimate bandwidth is determined by the aperture uncertainty associated with the closing of the sample gate (approximately 5nS). The converter bandwidth is then determined by the sampling Nyquist frequency rather than the input signal; change rate (dv/dt) and the LSB weight in volts as would be the case if there were no sample and hold.

Start-Convert (STCNV_H), Busy (BUSY_L) and End-Of-Convert (EOC_H) status and control line are provided. The converter will operate in either continuous or single conversion modes. To operate in continuous mode, STCNV_H should be tied to BUSY_L. The digital output register changes at the end of a conversion and is available while BUSY_L is High. Digital input and output circuits operate from a voltage independent of the remainder of the chip such that I/O is compatible with digital systems from, less than 3.3 volts, to 5 volts.

The converter divides the reference voltage into 16 segments with a linear weighted resistor network. The voltage on any segment is passed to a linear 10-bit DAC for interpolation. The architecture is inherently capable of monotonic operation. INL is ± 10 LSBs. DNL is $\pm 1/2$ LSB. The sampled input voltage is compared to the output of the two stage DAC for a 14-bit successive approximation conversion.

All inputs are protected to both power supply rails by semiconductor diodes. Inputs should be constrained to $V_{cc} + 0.4$ and $V_{ee} - 0.4$ to avoid forward biasing protection paths.

The devices will not latch with SEU events to above 100 MeV-cm²/mg. Total dose degradation is minimal to above 1 Mrad(Si). Displacement damage environments to neutron fluence equivalents in the mid 10¹⁴ neutrons per cm² range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependant.

- Notes:
- The STCNV_H is a dynamic input and should not be tied to a static voltage.
 - The input signals should be low pass filtered to reduce high frequency noise

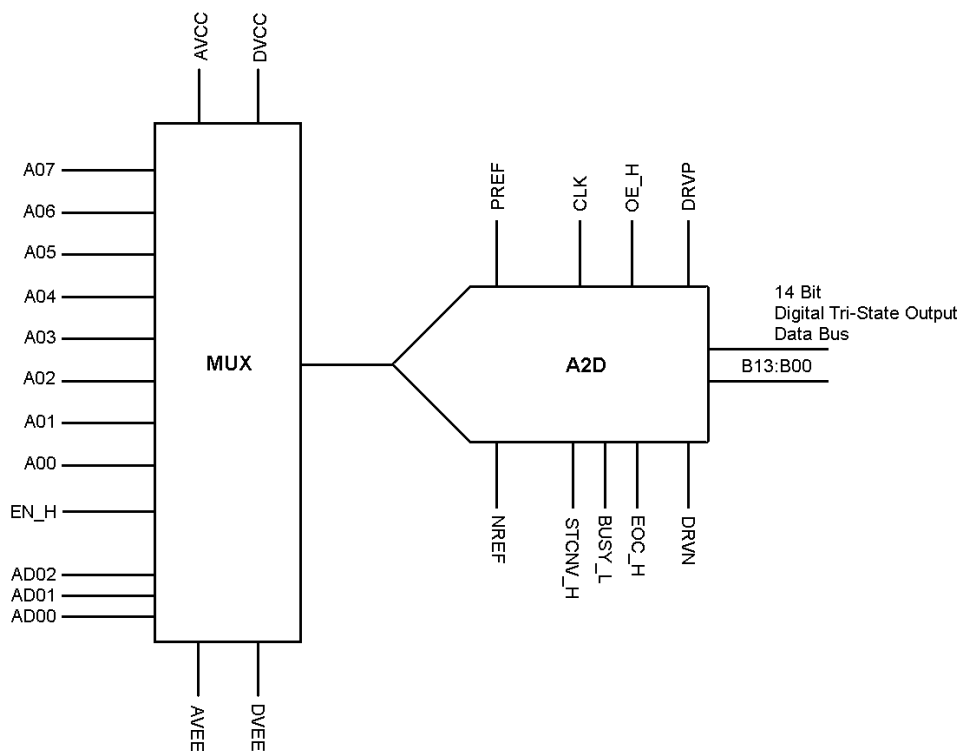


FIGURE 1: BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	+150	°C
Supply Voltage V _{CC} - V _{EE}	+6.0	V
Input Voltage	V _{CC} +0.4 V _{EE} -0.4	V
Lead Temperature (soldering, 10 seconds)	300	°C
Thermal Resistance, Junction to Case, θ_{jc}	3.5	°C/W
ESD Rating (MIL-STD-883, Method 3015, class 2)	2,000 - 3.999	V

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Typical	Units
+AVCC	Analog Power Supply Voltage	5.0	V
+DVCC	Digital Power Supply Voltage	5.0	V
DRV _P	Digital Output High Reference Level	3.3 to 5.0	V
DRV _N	Digital Output Low Reference Level	0	V

ELECTRICAL PERFORMANCE CHARACTERISTICS 1/

(T_C = -55°C TO +125°C, +V_{CC} = +5.0V)

Parameter	Symbol	Conditions	Min	Max	Units
Digital Supply Current Sleep	D _{ICCS}			1	mA
Digital Supply Current Active	D _{ICCA}			1	mA
Analog Supply Current Sleep	A _{ICCS}			2	mA
Analog Supply Current Active	A _{ICCA}			10	mA
Digital IO Supply Current Sleep	DIO _{ICCS}			1	mA
Digital IO Supply Current Active	DIO _{ICCA}			10	mA
Input Leakage Current	ILK			500	pA
Input Range	V _{IN}		1	5	V
Full-scale Input Range			0	PREF - NREF	V
Operating Range			-0.1	PREF - NREF+0.1	V
Input Capacitance 2/	C _{IN}			50	pF
High Analog Reference Current	IPREF			2	mA
High Analog Reference Voltage	VPREF			5	V
Low Analog Reference Voltage	VNREF		1		V
Integral Non Linearity	INL	10 Typical			LSB
Differential Non Linearity	DNL	1.5 Typical			LSB
DC Offset	V _{OS}	PREF-NREF ≥ 4.0V		2	mV
DC Gain	AE	PREF-NREF ≥ 4.0V	0.1		% FSR
Channel Isolation 2/			80		dB
Maximum Sampling Rate	f _{SAMPLE} (MAX)			25	kSPS
Conversion Time 2/	t _{CONV}	16 Typical			Clk Cycles
Clock Frequency	f _C			500	KHz

ELECTRICAL PERFORMANCE CHARACTERISTICS 1/ (continued)

(T_C = -55°C TO +125°C, +V_{CC} = +5.0V)

Parameter	Symbol	Conditions	Min	Max	Units
Address Input Voltage V _(A0-A3)	V _{AHI}		70%V _{CC}		V
	V _{ALO}			30%V _{CC}	V
Address Input Current (A0-A3)	I _{AL}	V _A = GND		50	nA
	I _{AH}	V _A = V _{CC}		50	nA
Enable Input Voltage V _{EN}	V _{ENHI}		70%V _{CC}		V
	V _{ENLO}			30%V _{CC}	V
Enable Input Current (EN)	I _{ENL}	V _{EN} = GND		50	nA
	I _{ENH}	V _{EN} = V _{CC}		50	nA
High Input Leakage Current (CH0-CH15)	I _{INLK₅}	V _{IN} = +5V, V _{EN} = V _{CC} , Output and all unused MUX inputs under test = 0V		50	nA
Low Input Leakage Current (CH0-CH15)	I _{INLK₀}	V _{IN} = 0V, V _{EN} = V _{CC} Output and all unused MUX inputs under test = +5V		50	nA
Multiplexer Settling Time 2/	t _s	A0-3-to-Out & EN-to-Out		200	nS

Notes:

1/ Specification derated to reflect Total Dose exposure to 1 Mrad(Si) @ +25°C.

2/ Not tested. Shall be guaranteed by design, characterization, or correlation to other test parameters.

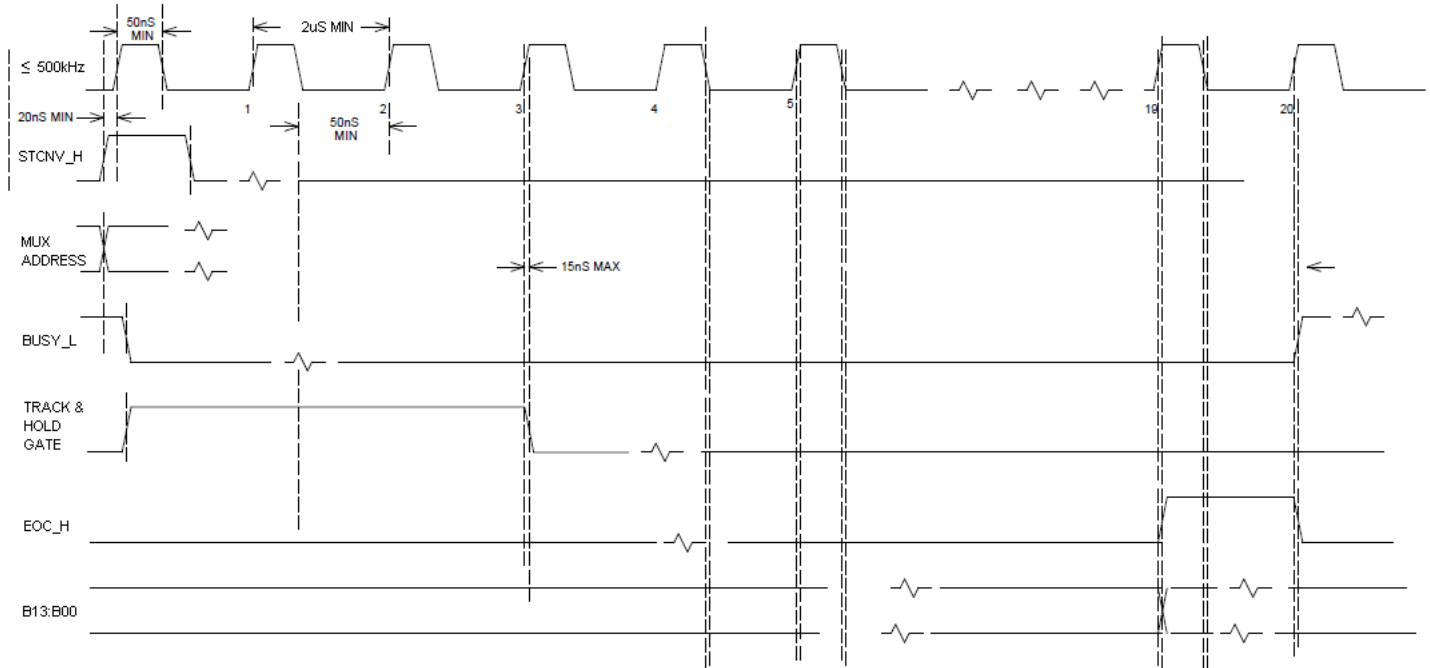


FIGURE 2: BASIC TIMING DIAGRAM

Pin #	Signal	Definition	Pin #	Signal	Definition
1	AVCC	Analog Supply Voltage	21	B10	Digital Output 10
2	DVCC	Digital Supply Voltage	22	B11	Digital Output 11
3	AD02	Multiplexer Address 02	23	B12	Digital Output 12
4	AD01	Multiplexer Address 01	24	B13	Digital Output 13
5	AD00	Multiplexer Address 00	25	EOC_H	End of Convert
6	CASE	Case Ground	26	BUSY_L	Busy
7	STCNV_H	Start Conversion	27	DRVN	Digital Output Low Reference Level
8	EN	Multiplexer Enable	28	DRVP	Digital Output High Reference Level
9	OE	Output Enable	29	DVEE	Digital Supply Return
10	CLK	Clock Input	30	AVEE	Analog Supply Return
11	B00	Digital Output 00	31	PREF	High Analog Reference Voltage
12	B01	Digital Output 01	32	AIN07	Analog Multiplexer Input 07
13	B02	Digital Output 02	33	AIN06	Analog Multiplexer Input 06
14	B03	Digital Output 03	34	AIN05	Analog Multiplexer Input 05
15	B04	Digital Output 04	35	AIN04	Analog Multiplexer Input 04
16	B05	Digital Output 05	36	AIN03	Analog Multiplexer Input 03
17	B06	Digital Output 06	37	AIN02	Analog Multiplexer Input 02
18	B07	Digital Output 07	38	AIN01	Analog Multiplexer Input 01
19	B08	Digital Output 08	39	AIN00	Analog Multiplexer Input 00
20	B09	Digital Output 09	40	NREF	Low Analog Reference Voltage

FIGURE 3: PACKAGE PIN-OUT AND SIGNAL DEFINITION

ORDERING INFORMATION

Model	DLA SMD #	Screening	Package
RHD5958-7	-	Commercial Flow, +25°C testing only	40-lead CQFP
RHD5958-S	-	Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
RHD5958-201-1S	5962-1220302KYC	DLA SMD Pending	
RHD5958-201-2S	5962-1220302KYA		
RHD5958-901-1S	5962H1220302KYC	DLA SMD and Radiation Certification Pending	
RHD5958-901-2S	5962H1220302KYA		

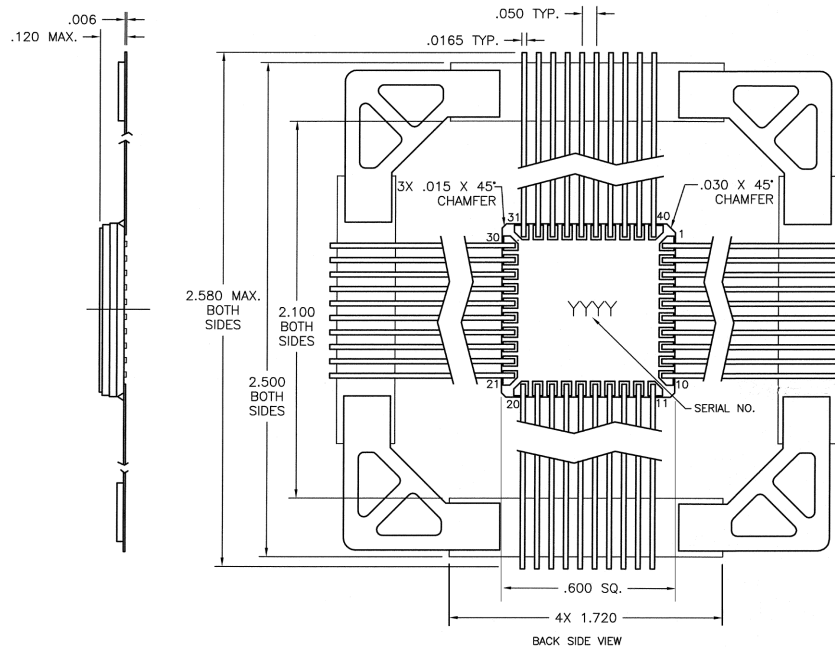


FIGURE 4: PACKAGE OUTLINE

EXPORT CONTROL:

This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Department of State is required prior to the export of this product from the United States.

EXPORT WARNING:

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