

RadHard-by-Design RHD8541 64-Channel Analog Multiplexer

www.aeroflex.com/RHDseries

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FEATURES

- 64 channels provided by four 16-channel multiplexers
- Single power supply operation at +3.3V to +5V
- Radiation performance
 - Total dose: $>1\text{Mrad}(\text{Si})$, Dose rate = 50 - 300 rads(Si)/s
 - ELDRS Immune
 - SEL Immune: $>100\text{ MeV}\cdot\text{cm}^2/\text{mg}$
 - Neutron Displacement Damage: $>10^{14}\text{ neutrons}/\text{cm}^2$
- Full military temperature range
- Low power consumption $< 4.0\text{mW}$
- CMOS analog switching allows rail to rail operation and low switch impedance
- Two address busses A(0-3) & B(0-3) and four enable lines afford flexible organization
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic ceramic
 - 96 leads, 1.320" Sq x 0.200"Ht quad flat pack
 - Weight - 15 grams max
- Aeroflex Plainview's Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.

GENERAL DESCRIPTION

Aeroflex's RHD8541 is a radiation hardened, single supply, 64-Channel Multiplexer MCM (multi-chip module). The RHD8541 design uses specific circuit topology and layout methods to mitigate total ionization dose effects and single event latchup. These characteristics make the RHD8541 especially suited for the harsh environment encountered in Deep Space missions. It is available in a 96 lead High Temperature Co-Fired Ceramic (HTCC) Quad Flatpack (CQFP). It is guaranteed operational from -55°C to $+125^{\circ}\text{C}$. Available screened in accordance with MIL-PRF-38534 Class K, the RHD8541 is ideal for demanding military and space applications.

ORGANIZATION AND APPLICATION

The RHD8541 consists of four, single supply, 16-Channel Multiplexers arranged as shown in the Block Diagram. The RHD8541 design is inherently radiation tolerant.

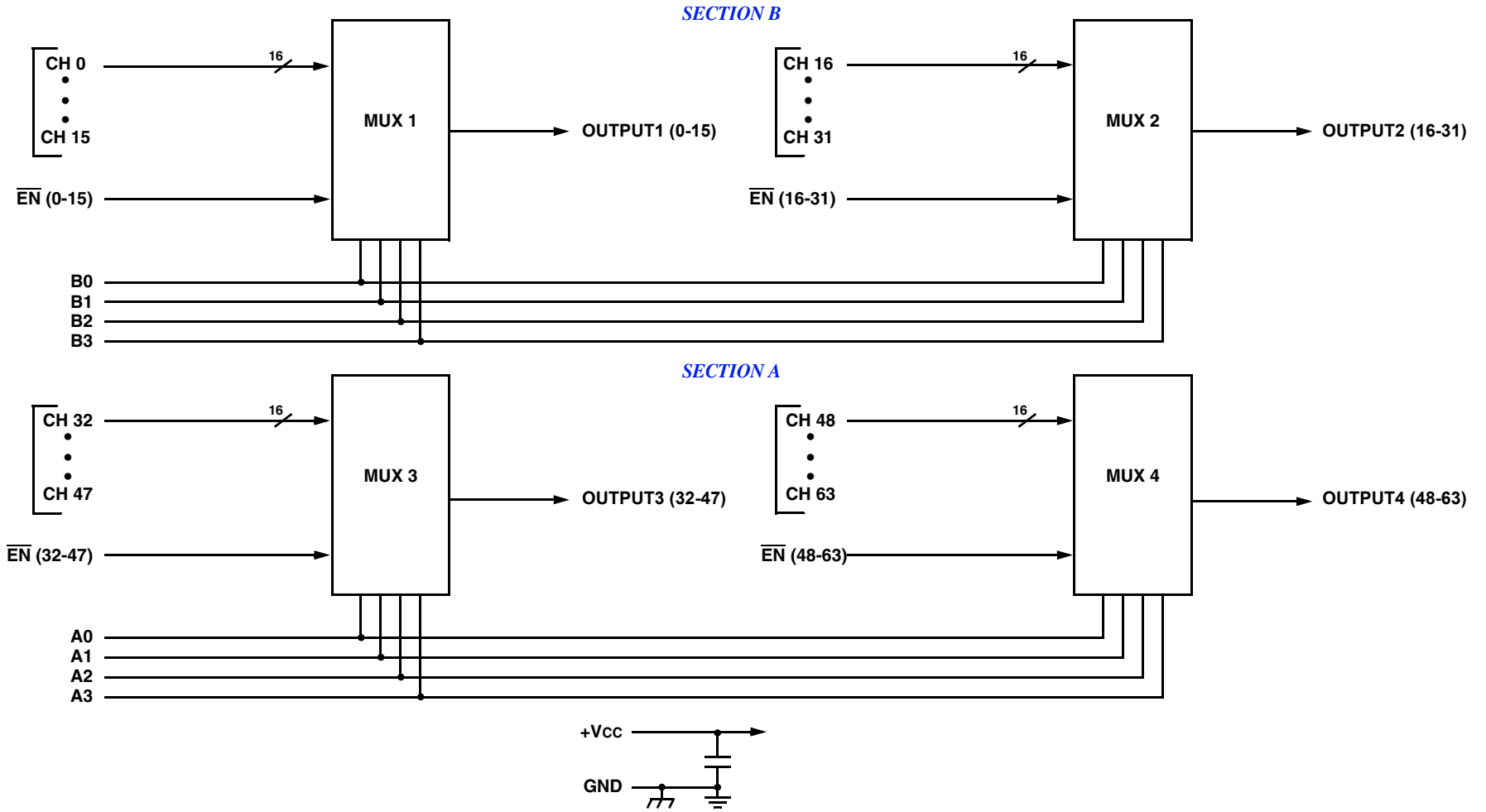
The device will not latch with SEU events to above $100\text{MeV}\cdot\text{cm}^2/\text{mg}$. Total dose degradation is minimal to above $1\text{Mrad}(\text{Si})$. Displacement damage environments to neutron fluence equivalents in the mid 10^{14} neutrons per cm^2 range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependant.

A SECTION

Thirty-two (32) channels addressable by bus A(0-3), in two 16-channel blocks, each block enabled separately.

B SECTION

Thirty-two (32) channels addressable by bus B(0-3), in two 16-channel blocks, each block enabled separately.



RHD8541 64-CHANNEL ANALOG MUX BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS ^{1/}

| Parameter | Range | Units |
|--|--------------------------------------|--------|
| Case Operating Temperature Range | -55 to +125 | °C |
| Storage Temperature Range | -65 to +150 | °C |
| Supply Voltage +V _{CC} (Pin 44) | +3.0 to +6.0 | V |
| Digital Input Overvoltage V _{EN} (Pins 5, 6, 91, 92), V _A (Pins 1, 3, 93, 95), V _B (Pins 2, 4, 94, 96) | < V _{CC} +0.4 > GND -0.4 | V V |
| Analog Input Over Voltage V _{IN} (CH0-CH63) | < V _{CC} +0.4 > GND -0.4 | V |

Notes:

^{1/} All measurements are made with respect to ground.

NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress rating only; functional operation beyond the 'Operation Conditions' is not recommended and extended exposure beyond the 'Operation Conditions' may affect device reliability.

RECOMMENDED OPERATING CONDITIONS ^{1/}

| Symbol | Parameter | Typical | Units |
|-------------------------------------|----------------------|---------------------|-------|
| +V _{CC} | Power Supply Voltage | 3.3 to 5.0 | V |
| V _{ENL} , V _{VAL} | Logic Low Level | 30% V _{CC} | V |
| V _{ENH} , V _{VAH} | Logic High Level | 70% V _{CC} | V |

DC ELECTRICAL PERFORMANCE CHARACTERISTICS ^{1/}

(T_c = -55°C to +125°C, +V_{CC} = +5V - Unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Max | Units |
|---|--------------------------|---|------|-----|-------|
| Supply Current +V _{CC} | +I _{CC} | $\overline{EN} = 30\% V_{CC}$ | 0 | 40 | μA |
| | +I _{SBY} | $\overline{EN} = 70\% V_{CC}$ | 0 | 40 | μA |
| Address Input Current A(0-3) | I _{AL} (0-3)A | V _A = 30% V _{CC} | -100 | 100 | nA |
| | I _{AH} (0-3)A | V _A = 70% V _{CC} | -100 | 100 | nA |
| | I _{AL} (0-3)B | V _B = 30% V _{CC} | -100 | 100 | nA |
| | I _{AH} (0-3)B | V _B = 70% V _{CC} | -100 | 100 | nA |
| Enable Input Current \overline{EN} | I _{ENL} (0-15) | V _{EN} (0-15) = 30% V _{CC} | -50 | 50 | nA |
| | I _{ENH} (0-15) | V _{EN} (0-15) = 70% V _{CC} | -50 | 50 | nA |
| | I _{ENL} (16-31) | V _{EN} (16-31) = 30% V _{CC} | -50 | 50 | nA |
| | I _{ENH} (16-31) | V _{EN} (16-31) = 70% V _{CC} | -50 | 50 | nA |
| | I _{ENL} (32-47) | V _{EN} (32-47) = 30% V _{CC} | -50 | 50 | nA |
| | I _{ENH} (32-47) | V _{EN} (32-47) = 70% V _{CC} | -50 | 50 | nA |
| | I _{ENL} (48-63) | V _{EN} (48-63) = 30% V _{CC} | -50 | 50 | nA |
| | I _{ENH} (48-63) | V _{EN} (48-63) = 70% V _{CC} | -50 | 50 | nA |

DC ELECTRICAL PERFORMANCE CHARACTERISTICS 1/ (continued)

(Tc = -55°C to +125°C, +Vcc = +5V - Unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Max | Units | |
|---|--------------------|--|--------|-----|-------|---|
| High Input Leakage Current (CH0-CH63) | IINLK ₅ | V _{IN} = +5V, V _{EN} = 70% V _{CC} , Output and all unused MUX inputs under test = 0V | -50 | 50 | nA | |
| Low Input Leakage Current (CH0-CH63) | IINLK ₀ | V _{IN} = 0V, V _{EN} = 70% V _{CC} , Output and all unused MUX inputs under test = +5V | -50 | 50 | nA | |
| Output Leakage Current V _{OUT} (pins 25,26, 68 & 70) | IOUTLK | V _{OUT} = +5V, V _{EN} = 70% V _{CC} , All inputs grounded except channel being tested. 3/, 4/ | -50 | 50 | nA | |
| Switch ON Resistance OUTPUTS (pins 25,26, 68 & 70) 6/ | RDS(ON) | V _{IN} = 0V, V _{IN} = +2.5V, V _{IN} = +5V V _{EN} = 30% V _{CC} I _{OUT} = -1mA 2/, 3/, 5/ | -55°C | - | 500 | Ω |
| | | | +25°C | - | 750 | Ω |
| | | | +125°C | - | 1000 | Ω |

Notes:

- 1/ Measure inputs sequentially. Ground all unused inputs of the device under test. V_A is the applied input voltage to the address lines A(0-3). V_B is the applied input voltage to the address lines B(0-3).
- 2/ V_{IN} is the applied input voltage to the input channels (CH0-CH63).
- 3/ V_{EN} is the applied input voltage to the enable lines \overline{EN} (0-15), \overline{EN} (16-31), \overline{EN} (32-47) and \overline{EN} (48-63).
- 4/ V_{OUT} is the applied input voltage to the output lines OUTPUT1(0-15), OUTPUT2(16-31), OUTPUT3(32-47) and OUTPUT4(48-63).
- 5/ Negative current is the current flowing out of each of the MUX pins. Positive current is the current flowing into each MUX pin.
- 6/ The RHD8541 cannot be operated with analog inputs below 0 volts.
- 7/ Not tested, guaranteed to the specified limits.

SWITCHING CHARACTERISTICS

(Tc = -55°C to +125°C, +Vcc = +5V - Unless otherwise specified)

| Parameter | Symbol | Conditions | Temp | Min | Max | Units |
|-------------------------|--------------------|--|--------|-----|-----|-------|
| Address to Output Delay | t _{AHL} | V _{OUT} High to Low Transition | -55°C | 10 | 150 | ns |
| | | | +25°C | 10 | 150 | ns |
| | | | +125°C | 10 | 200 | ns |
| | t _{ALH} | V _{OUT} Low to High Transition | -55°C | 10 | 150 | ns |
| | | | +25°C | 10 | 150 | ns |
| | | | +125°C | 10 | 200 | ns |
| Enable to Output Delay | t _{ONEN} | V _{EN} = 30% V _{CC} (Enabled) | -55°C | 10 | 150 | ns |
| | | | +25°C | 10 | 150 | ns |
| | | | +125°C | 10 | 200 | ns |
| | t _{OFFEN} | V _{EN} = 70% V _{CC} (Disabled) | ALL | 10 | 200 | ns |

TRUTH TABLE (CH0 – CH15)

| B3 | B2 | B1 | B0 | $\overline{\text{EN}}(0-15)$ | "ON" CHANNEL <u>1/</u> |
|----|----|----|----|------------------------------|------------------------|
| X | X | X | X | H | NONE |
| L | L | L | L | L | CH0 |
| L | L | L | H | L | CH1 |
| L | L | H | L | L | CH2 |
| L | L | H | H | L | CH3 |
| L | H | L | L | L | CH4 |
| L | H | L | H | L | CH5 |
| L | H | H | L | L | CH6 |
| L | H | H | H | L | CH7 |
| H | L | L | L | L | CH8 |
| H | L | L | H | L | CH9 |
| H | L | H | L | L | CH10 |
| H | L | H | H | L | CH11 |
| H | H | L | L | L | CH12 |
| H | H | L | H | L | CH13 |
| H | H | H | L | L | CH14 |
| H | H | H | H | L | CH15 |

1/ Between (CH0-CH15) and OUTPUT1(0-15)

TRUTH TABLE (CH16 – CH31)

| B3 | B2 | B1 | B0 | $\overline{\text{EN}}(16-31)$ | "ON" CHANNEL <u>2/</u> |
|----|----|----|----|-------------------------------|------------------------|
| X | X | X | X | H | NONE |
| L | L | L | L | L | CH16 |
| L | L | L | H | L | CH17 |
| L | L | H | L | L | CH18 |
| L | L | H | H | L | CH19 |
| L | H | L | L | L | CH20 |
| L | H | L | H | L | CH21 |
| L | H | H | L | L | CH22 |
| L | H | H | H | L | CH23 |
| H | L | L | L | L | CH24 |
| H | L | L | H | L | CH25 |
| H | L | H | L | L | CH26 |
| H | L | H | H | L | CH27 |
| H | H | L | L | L | CH28 |
| H | H | L | H | L | CH29 |
| H | H | H | L | L | CH30 |
| H | H | H | H | L | CH31 |

2/ Between (CH16-CH31) and OUTPUT2 (16-31)

TRUTH TABLE (CH32 – CH47)

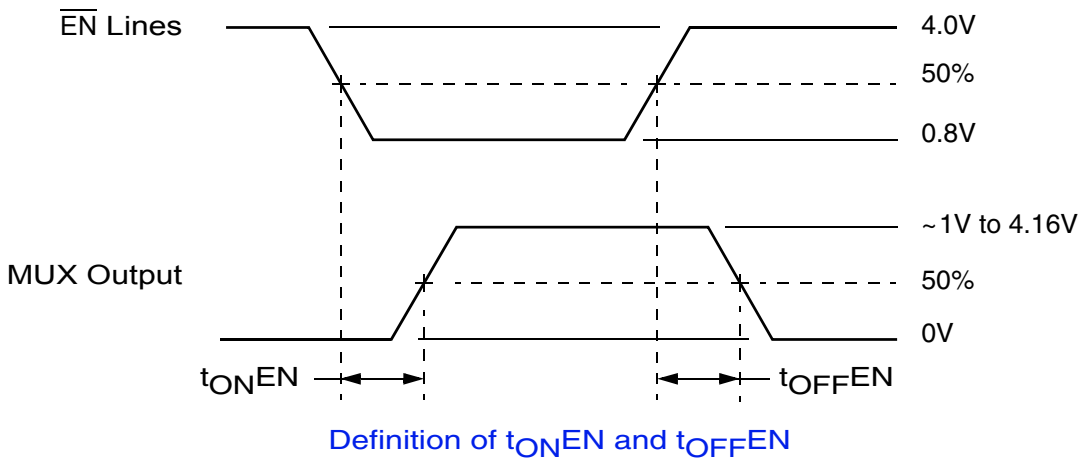
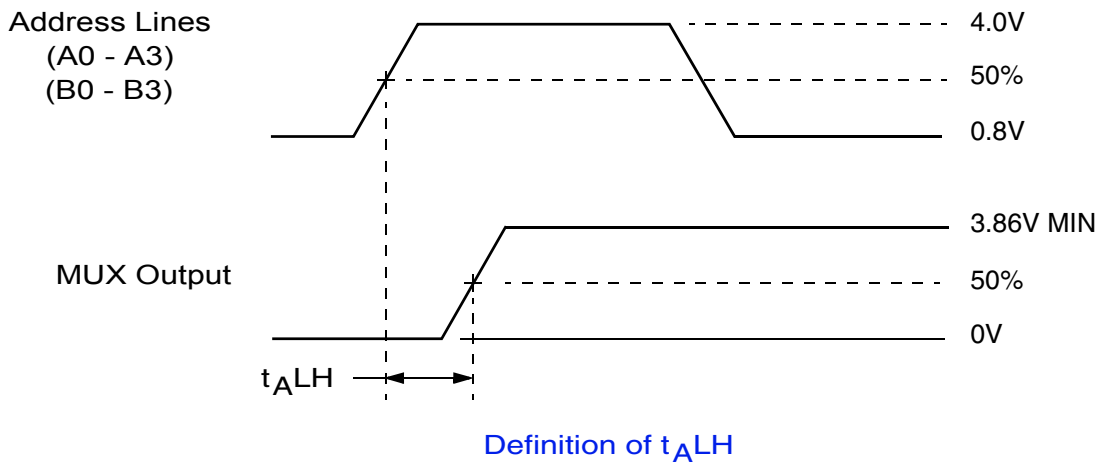
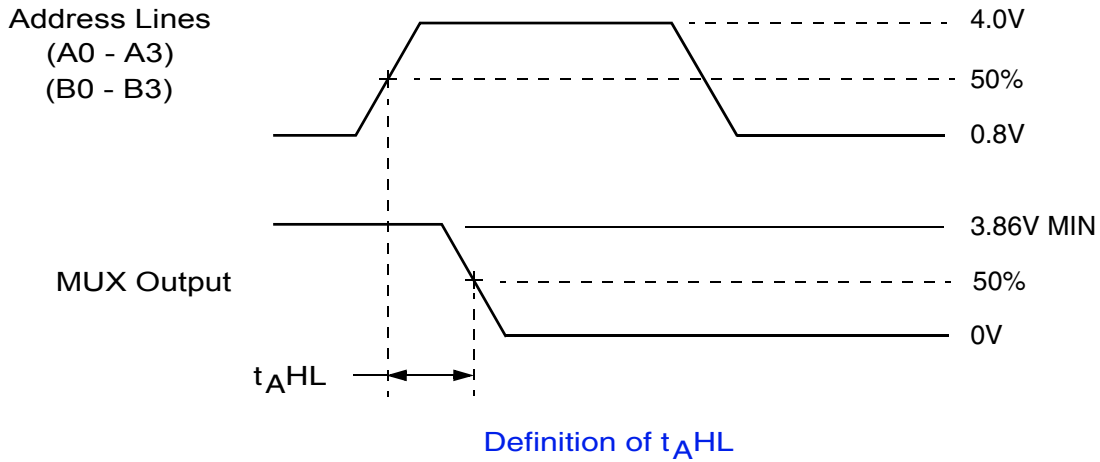
| A3 | A2 | A1 | A0 | $\overline{\text{EN}}(32-47)$ | "ON" CHANNEL <u>3/</u> |
|----|----|----|----|-------------------------------|------------------------|
| X | X | X | X | H | NONE |
| L | L | L | L | L | CH32 |
| L | L | L | H | L | CH33 |
| L | L | H | L | L | CH34 |
| L | L | H | H | L | CH35 |
| L | H | L | L | L | CH36 |
| L | H | L | H | L | CH37 |
| L | H | H | L | L | CH38 |
| L | H | H | H | L | CH39 |
| H | L | L | L | L | CH40 |
| H | L | L | H | L | CH41 |
| H | L | H | L | L | CH42 |
| H | L | H | H | L | CH43 |
| H | H | L | L | L | CH44 |
| H | H | L | H | L | CH45 |
| H | H | H | L | L | CH46 |
| H | H | H | H | L | CH47 |

3/ Between (CH32-CH47) and OUTPUT3 (32-47)

TRUTH TABLE (CH48 – CH63)

| A3 | A2 | A1 | A0 | $\overline{\text{EN}}(48-63)$ | "ON" CHANNEL <u>4/</u> |
|----|----|----|----|-------------------------------|------------------------|
| X | X | X | X | H | NONE |
| L | L | L | L | L | CH48 |
| L | L | L | H | L | CH49 |
| L | L | H | L | L | CH50 |
| L | L | H | H | L | CH51 |
| L | H | L | L | L | CH52 |
| L | H | L | H | L | CH53 |
| L | H | H | L | L | CH54 |
| L | H | H | H | L | CH55 |
| H | L | L | L | L | CH56 |
| H | L | L | H | L | CH57 |
| H | L | H | L | L | CH58 |
| H | L | H | H | L | CH59 |
| H | H | L | L | L | CH60 |
| H | H | L | H | L | CH61 |
| H | H | H | L | L | CH62 |
| H | H | H | H | L | CH63 |

4/ Between (CH48-CH63) and OUTPUT4 (48-63)



NOTE: $f = 10\text{KHz}$, Duty cycle = 50%.

RHD8541 SWITCHING DIAGRAMS

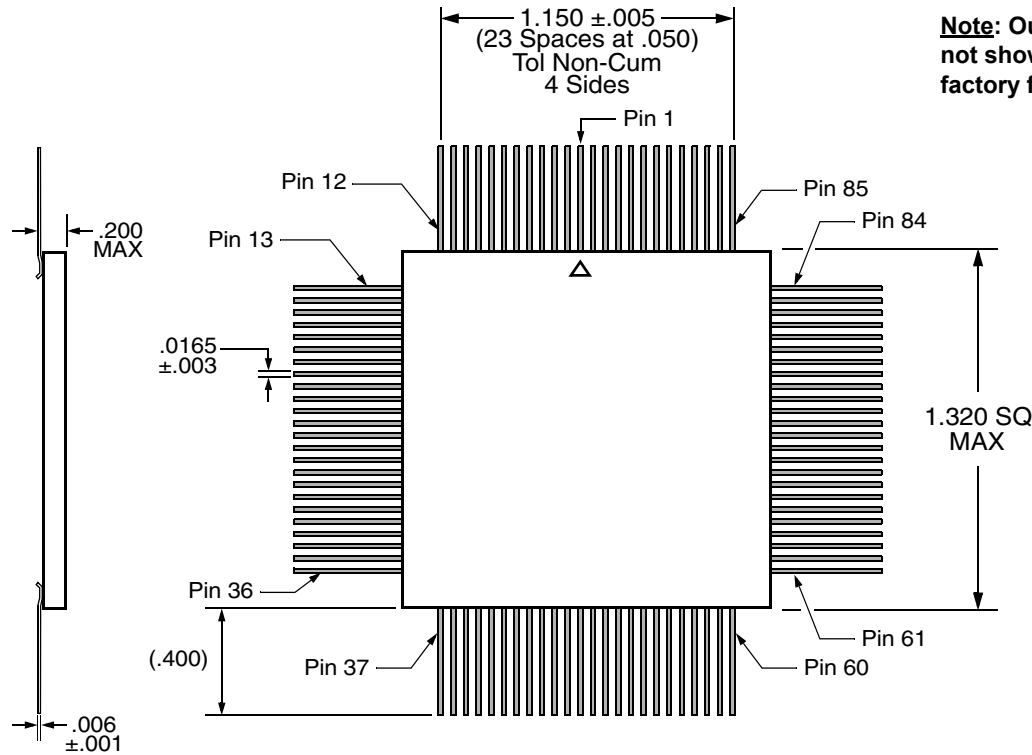
PIN NUMBERS & FUNCTIONS

| RHD8541 – 96 Leads Ceramic QUAD Flat Pack | | | | | |
|---|--------------------------------|-------|----------|-------|--------------------------------|
| Pin # | Function | Pin # | Function | Pin # | Function |
| 1 | A2 | 33 | CH11 | 65 | CH49 |
| 2 | B2 | 34 | CH27 | 66 | CH48 |
| 3 | A3 | 35 | CH12 | 67 | NC |
| 4 | B3 | 36 | CH28 | 68 | Output4 (48-63) |
| 5 | $\overline{\text{EN}}$ (0-15) | 37 | CH13 | 69 | NC |
| 6 | $\overline{\text{EN}}$ (16-31) | 38 | CH29 | 70 | Output3 (32-47) |
| 7 | CH0 | 39 | CH14 | 71 | GND |
| 8 | CH16 | 40 | CH30 | 72 | GND |
| 9 | CH1 | 41 | CH15 | 73 | CH47 |
| 10 | CH17 | 42 | CH31 | 74 | CH46 |
| 11 | CH2 | 43 | NC | 75 | CH45 |
| 12 | CH18 | 44 | +Vcc | 76 | CH44 |
| 13 | CH3 | 45 | NC | 77 | CH43 |
| 14 | CH19 | 46 | NC | 78 | CH42 |
| 15 | CH4 | 47 | NC | 79 | CH41 |
| 16 | CH20 | 48 | NC | 80 | CH40 |
| 17 | CH5 | 49 | NC | 81 | CH39 |
| 18 | CH21 | 50 | CASE GND | 82 | CH38 |
| 19 | CH6 | 51 | CH63 | 83 | CH37 |
| 20 | CH22 | 52 | CH62 | 84 | CH36 |
| 21 | CH7 | 53 | CH61 | 85 | CH35 |
| 22 | CH23 | 54 | CH60 | 86 | CH34 |
| 23 | GND | 55 | CH59 | 87 | CH33 |
| 24 | GND | 56 | CH58 | 88 | CH32 |
| 25 | Output1 (0-15) | 57 | CH57 | 89 | GND |
| 26 | Output2 (16-31) | 58 | CH56 | 90 | GND |
| 27 | CH8 | 59 | CH55 | 91 | $\overline{\text{EN}}$ (48-63) |
| 28 | CH24 | 60 | CH54 | 92 | $\overline{\text{EN}}$ (32-47) |
| 29 | CH9 | 61 | CH53 | 93 | A0 |
| 30 | CH25 | 62 | CH52 | 94 | B0 |
| 31 | CH10 | 63 | CH51 | 95 | A1 |
| 32 | CH26 | 64 | CH50 | 96 | B1 |

NOTE: It is recommended that all "NC" or "no connect" pins be grounded. This eliminates or minimizes any ESD or static buildup.

ORDERING INFORMATION

| Model Number | DLA SMD # | Screening | Package |
|----------------|-----------------|---|-------------------|
| RHD8541-7 | - | Commercial Flow, +25°C testing only | QUAD Flat Pack |
| RHD8541-S | - | Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications | |
| RHD8541-201-1S | 5962-1221101KXC | DLA SMD Pending | |
| RHD8541-901-1S | 5962H1221101KXC | DLA SMD and Radiation Certification Pending | |



Note: Outside ceramic tie bars not shown for clarity. Contact factory for details.

FLAT PACKAGE OUTLINE

EXPORT CONTROL:

This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Department of State is required prior to the export of this product from the United States.

EXPORT WARNING:

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