Standard Products

UT16MX110/111/112 Analog Multiplexer

Data Sheet
September 7, 2012
www.aeroflex.com/MUX

FEATURES

- ❑ 16-to-1 Analog Mux
- ❑ 100Ω Signal paths (typical)
- ❑ 5V single supply
- ❑ Rail-to-Rail signal handling
- ❑ Asynchronous $\overline{\text{RESET}}$ input
- ❑ SPI™/QSPI™ and MICROWIRE™ compatible serial interface (UT16MX112)
- ❑ Asynchronous parallel input Interface (UT16MX110)
- ❑ Synchronous parallel input Interface (UT16MX111)
- ❑ LVCMOS/LVTTL compatible inputs (provided by internal voltage regulator)
- ❑ 2kV ESD Protection (per MIL-STD-883, Method 3015.7)
- ❑ Operational environment:
  - Total ionizing dose: 300 krad(Si)
  - SEL immune to a LET of 110 MeV-cm^2/mg
  - SEU immune to a LET of 62.3 MeV-cm^2/mg
- ❑ Packaging: 28-Lead Ceramic Flatpack
- ❑ Standard Microcircuit Number 5962-10233
  - QML Q, QML V

INTRODUCTION

The UT16MX110/111/112 are low voltage analog multiplexers with a convenient LVCMOS (3.3V) digital interface. The analog muxes have Break-Before-Make architecture with a low channel resistance. The muxes support rail-to-rail input signal levels. The multiplexer supports serial (SPI™), or parallel (asynchronous or synchronous) interface.

The UT16MX110/111/112 operates with a single 5V($\pm$10%) power supply. The voltage used for the digital circuitry and the digital I/O is generated internally from the positive analog supply voltage. Therefore, no external digital voltage supply is required.

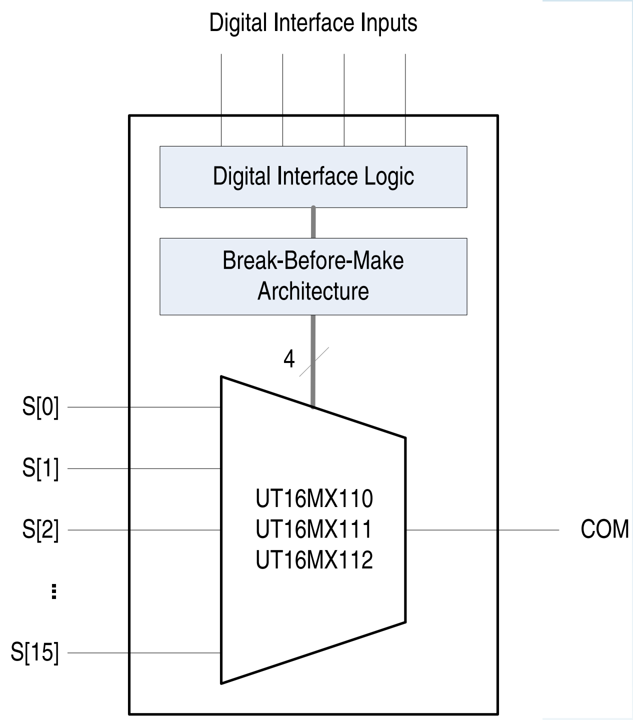


Figure 1. UT16MX110/111/112 Block Diagram

FUNCTIONAL DESCRIPTION

All mux decoding (whether for the UT16MX110, UT16MX111, or UT16MX112 device) operation utilizes a Break-Before-Make process to prevent shorting between analog inputs during address transitions.

The 3V_OUT pin provides a regulated voltage of 3.3V. This voltage is derived from the AVDD supply and is used internally as the positive supply voltage for the digital logic and digital I/O circuitry. The 3V_OUT pin requires a load capacitor of 0.1uF for proper operation.

UT16MX110:
The UT16MX110 utilizes a parallel interface which operates in asynchronous mode much like discrete logic switches. During operation, the connection between COM and the S[15:0] pins are steered, asynchronously, based on the binary decoding of the A[3:0] static logic levels. The address pins A[3:0] are required to hold static levels for proper mux operation. Any change in A[3:0] pins directs the COM connection to the appropriate S[x] input after approximately 100ns propagation delay (including the Break-Before-Make delay). All bits (A[3:0]) of any address change should be received by the UT16MX110 within 18 ns of the first bit change for proper operation. The asynchronous parallel interface mode requires $\overline{\text{CS}}$ to be low for accepting a change on the address pins A[3:0]. When $\overline{\text{CS}}$ is high, the UT16MX110 disables the address pins A[3:0], as well as holding the last valid address state, thereby mitigating against any single-event upsets or transients on the address bus.

UT16MX111:
The UT16MX111 utilizes a parallel interface which operates in a synchronous mode which utilizes the PLATCH input as the latching clock. Upon rising edge of PLATCH, logic level at the A[3:0] pins will be registered and retained internally to decode the mux. Based on the values of the A[3:0] pins, COM is connected to the appropriate S[x] input after approximately 100ns propagation delay (including the Break-Before-Make delay).

UT16MX112:
The UT16MX112 utilizes a serial interface that supports the standard that is compatible with MICROWIRE™, SPI™, and QSPI™. The UT16MX112 SPI™ interface can be depicted as an 8-bit serial shift register controlled by $\overline{\text{SS}}$, clocked by the rising edge of SCLK. The 8-bit shift register is for compatibility purposes, even though this UT16MX112 serial address setting requires only 4 bits. The four LSB of the 8-bit shift register are the four bits decoding the mux address. When shifting data into the part, the MSB enters the part first. The four MSB may be set to zeroes, e.g., the 8-bit command "00001001" would set the mux to connect COM to S[9].

The UT16MX112 is considered a slave SPI™ device with MOSI (Master Out Slave In) as the data input pin to the device. The data is shifted with D7 as the first bit into the shift register, and also the first bit out to the MISO (Master In Slave Out) output pin after eight clock cycles of SCLK. The signal on the $\overline{\text{SS}}$ pin defines the window when the address bits are shifted into the device. This occurs when signal on $\overline{\text{SS}}$ is low. Only when $\overline{\text{SS}}$ is high at the close of the shifting window, does the mux decoding get updated and COM is directed to the decoded S[x] input (after Break-Before-Make delay).

SPI™ Operations:
The SPI™ (Serial Peripheral Interface) is implemented as a synchronous 8-bit serial shift register controlled by four pins: MOSI, MISO, SCLK, and $\overline{\text{SS}}$. This is compatible with the SPI™/QSPI™ standard as defined by Motorola on the MC68HCxx line of microcontrollers. This SPI™ also conforms to the MICROWIRE™ interface, an SPI™ subset interface, as defined by National Semiconductor.

The UT16MX112 SPI™ is always a slave device, where MOSI, SCLK, and $\overline{\text{SS}}$ are controlled by a master device. MISO output is used as receiving slave data or to daisy chain several SPI™ devices in appropriate applications.

The MUX select functionality is controlled by the four LSB of the 8-bit SPI™ shift registers. When shifting, the first SCLK rising edge clocks in the MSB first. The first falling edge of the SCLK clocks out the 6th bit of the current values in the SPI™ registers, since the 7th bit already appears at the MISO at the start of a serial transmission before the first SCLK (Figures 7 and 8).

Reset Function (UT16MX111/112 Only):
The $\overline{\text{RESET}}$ pin is used to reset all internal logic circuits. $\overline{\text{RESET}}$ held low also keeps all COM and S[15:0] analog I/Os in a high impedance state. This is the recommended condition at system power-up.

Asserting $\overline{\text{RESET}}$ (active low) resets all of the internal address decoding registers to 0, thus steering the COM to connect to S[0] while in the high impedance state. When $\overline{\text{RESET}}$ is de-asserted (high), both COM and S[0] will come out of the high impedance state and COM will be driven by S[0].

Table 1: UT16MX110 Pin Description

Pin No.	Name	I/O	Type	Description
1	AV_{DD}	--	Power	Analog Positive Supply
2	NC	--	--	No Connection
3	NC	--	--	No Connection
4-11	S[15:8]	Input	Analog	Muxed Inputs
12	GND	--	Power	Digital Ground
13	3V_OUT	Output	Power	Digital Power Bypass Connection[1]
14	A3	Input	Digital	Parallel A3
15	A2	Input	Digital	Parallel A2
16	A1	Input	Digital	Parallel A1
17	A0	Input	Digital	Parallel A0
18	$\overline{CS}$	Input	Digital	Active Low Parallel Chip Select with Internal Pull-up
19-26	S[0:7]	Input	Analog	Muxed Inputs
27	AV_{SS}	--	Power	Analog Negative Supply
28	COM	Output	Analog	Muxed Output[2]

Notes:
1. Bypass capacitor of 0.1 µF required for proper operation (See Figure 11)
2. Continuous operation with low load resistance is not recommended. (See Figure 12)

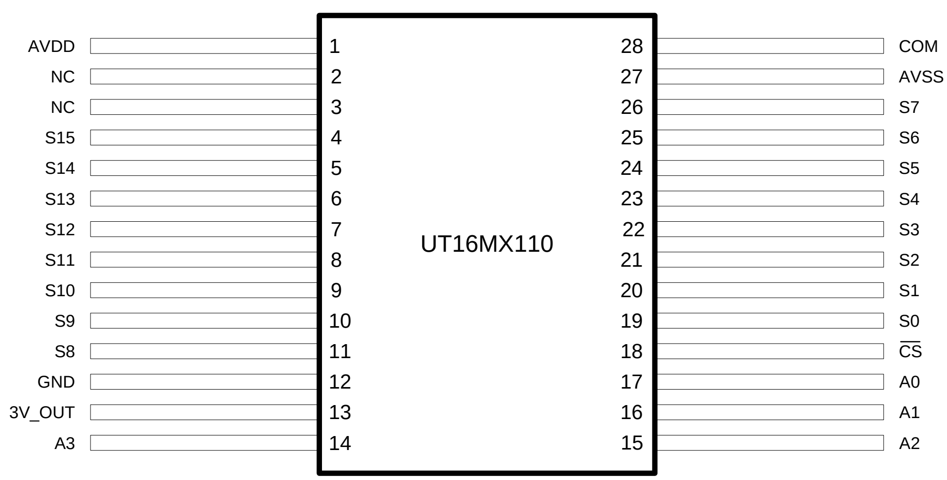


Figure 2. UT16MX110 Pinout

Table 2: UT16MX111 Pin Description

Pin No.	Name	I/O	Type	Description
1	AV_{DD}	--	Power	Analog Positive Supply
2	$\overline{RESET}$	Input	Digital	Active Low Reset with Internal Pull-up
3	PLATCH	Input	Digital	Parallel Latch with Internal Pull-down
4-11	S[15:8]	Input	Analog	Muxed Inputs
12	GND	--	Power	Digital Ground
13	3V_OUT	Output	Power	Digital Power Bypass Connection[1]
14	A3	Input	Digital	Parallel A3
15	A2	Input	Digital	Parallel A2
16	A1	Input	Digital	Parallel A1
17	A0	Input	Digital	Parallel A0
18	NC	--	--	No Connection
19-26	S[0:7]	Input	Analog	Muxed Inputs
27	AV_{SS}	--	Power	Analog Negative Supply
28	COM	Output	Analog	Muxed Output[2]

Notes:
1. Bypass capacitor of 0.1 μF required for proper operation. (See Figure 11)
2. Continuous operation with low load resistance is not recommended. (See Figure 12)

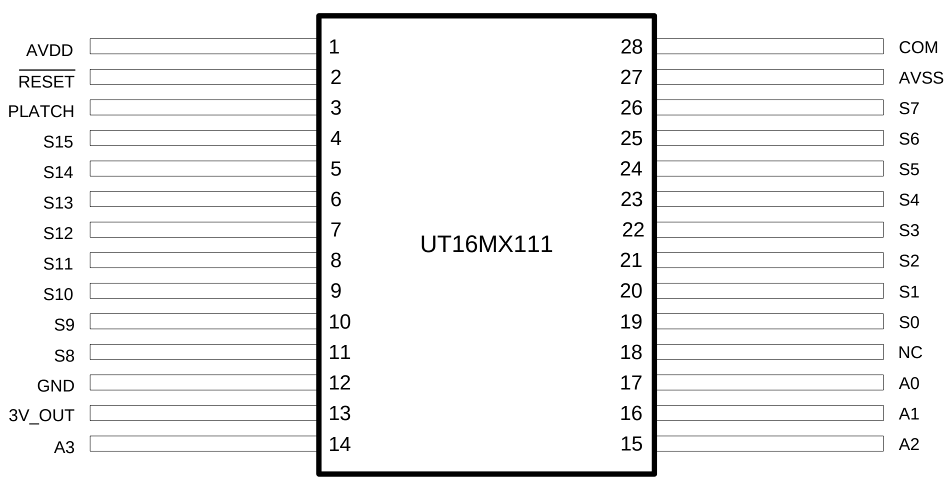


Figure 3. UT16MX111 Pinout

Table 3: UT16MX112 Pin Description

Pin No.	Name	I/O	Type	Description
1	AV_{DD}	--	Power	Analog Positive Supply
2	$\overline{RESET}$	Input	Digital	Active Low Reset with Internal Pull-up
3	NC	--	--	No Connection
4-11	S[15:8]	Input	Analog	Muxed Inputs
12	GND	--	Power	Digital Ground
13	3V_OUT	Output	Power	Digital Power Bypass Connection[1]
14	NC	--	--	No Connection
15	SCLK	Input	Digital	SPI™ Clock
16	MOSI	Input	Digital	Master-out-Slave-in (Din)
17	MISO	Output	Digital	Master-in-Slave-out (Dout)
18	$\overline{SS}$	Input	Digital	SPI™ Shift Control with Internal Pull-up
19-26	S[0:7]	Input	Analog	Muxed Inputs
27	A_{VSS}	--	Power	Analog Negative Supply
28	COM	Output	Analog	Muxed Output[2]

Notes:
1. Bypass capacitor of 0.1 μF required for proper operation. (See Figure 11)
2. Continuous operation with low load resistance is not recommended. (See Figure 12)

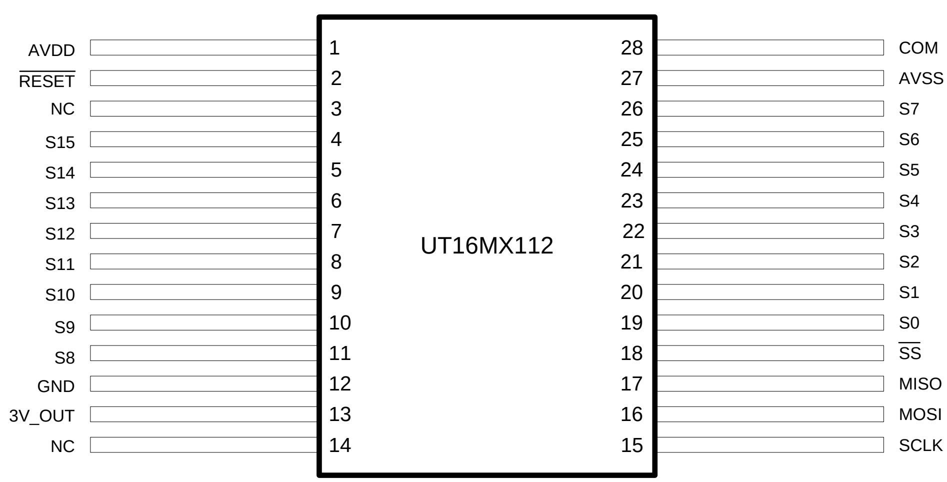


Figure 4. UT16MX112 Pinout

Table 4: UT16MX110 Truth Table

$\overline{CS}$	A3	A2	A1	A0	COM
1	X	X	X	X	Previous Decide State
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15

Table 5: UT16MX111 Truth Table

$\overline{\text{RESET}}$	PLATCH	A3	A2	A1	A0	COM
0	X	X	X	X	X	Tri-State (S[15:0] and COM)
1	Rising Edge	0	0	0	0	S0
1	Rising Edge	0	0	0	1	S1
1	Rising Edge	0	0	1	0	S2
1	Rising Edge	0	0	1	1	S3
1	Rising Edge	0	1	0	0	S4
1	Rising Edge	0	1	0	1	S5
1	Rising Edge	0	1	1	0	S6
1	Rising Edge	0	1	1	1	S7
1	Rising Edge	1	0	0	0	S8
1	Rising Edge	1	0	0	1	S9
1	Rising Edge	1	0	1	0	S10
1	Rising Edge	1	0	1	1	S11
1	Rising Edge	1	1	0	0	S12
1	Rising Edge	1	1	0	1	S13
1	Rising Edge	1	1	1	0	S14
1	Rising Edge	1	1	1	1	S15

OPERATIONAL ENVIRONMENT

PARAMETER	LIMIT	UNITS
Total Ionizing Dose (TID)	300	krad(Si)
Single Event Latchup (SEL)	>110	MeV-cm^2/mg
Single Event Upset Threshold (SEU)	>62.3	MeV-cm^2/mg

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMITS
AV_{DD}	Analog Positive Supply Voltage	7.5V
AV_{SS}	Analog Negative Supply Voltage	-0.3V
P_D	Static Power Dissipation	150 mW
T_J	Junction Temperature	-55^{o}C to +130^{o}C
T_{STG}	Storage Temperature	-65^{o}C to +150^{o}C
ESD_{HBM}	Electrostatic Discharge using Human Body Model	2kV

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
AV_{DD}	Analog Positive Supply Voltage	4.5V to 5.5V
AV_{SS}	Analog Negative Supply Voltage	0.0V
V_I	Analog Switch Input Voltage	AV_{SS} to AV_{DD}
T_C	Case Operating Temperature Range	-55^{o}C to +125^{o}C
T_J	Junction Operating Temperature[1]	-55^{o}C to +130^{o}C

Notes:

1. Thermal resistance, Θ_{JC}, of junction-to-case is 4.8^o C/W.

DC ELECTRICAL CHARACTERISTICS [1]

(AV_{DD}=5.0V ± 0.5V, GND=0V; -55°C ≤ T_C ≤ +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Digital input low		-0.3		0.8	V
V_{IH}	Digital input high		2.0		3.6	V
V_{OL}	Digital output low (UT16MX112)	I_{OL} = 100µA			0.2	V
		I_{OL} = 2mA			0.4	V
V_{OH}	Digital output high (UT16MX112)	I_{OH} = -100µA	2.8			V
		I_{OH} = -2mA	2.4			V
R_{ON}	On resistance	V_{IN}= AV_{SS} to AV_{DD} V_{COM} = V_{IN} - 0.3V	40	145	300	Ω
I_{OFF}	Analog I/O leakage current (switch off)[2]	AV_{DD} = 5.5V V_{IN} = AV_{SS} or AV_{DD}	-1.6		1.6	µA
I_{IL}	Digital input current low LVCMOS / CMOS inputs Inputs with a pull-up Inputs with a pull-down	AV_{DD} = 5.5V V_{IL} = GND	 -1.0 -380 -5.0			 µA µA µA
I_{IH}	Digital input current high LVCMOS / CMOS inputs Inputs with a pull-up[3] Inputs with a pull-down	AV_{DD} = 4.5V V_{IH} = 3.6V			 300 300 200	 µA µA µA
	Digital input current high LVCMOS / CMOS inputs Inputs with a pull-up[3] Inputs with a pull-down	AV_{DD} = 5.5V V_{IH} = 3.0V	 -50 		 1.0 100	 µA µA µA
Q_{IDD}	Quiescent analog supply current	A_{VDD} = 5.5V V_{IH} = 3.3V V_{IL} = GND			3.0	mA

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. This parameter cannot be tested on COM for the UT16MX110 device because the pin is continuously on.
3. This parameter tested with PLATCH held low on the UT16MX111 device.

AC ELECTRICAL CHARACTERISTICS [1,2]

(AV_{DD}=5.0V ± 0.5V, GND=0V; -55°C ≤ T_C ≤ +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance (switch off)[3]	F_{IN} = 1MHz @ 0V		40	50	pF
$C_{IN\_DIGITAL}$	Input digital capacitance[3]	F_{IN} = 1MHz @ 0V		46	55	pF
C_{OUT}	Output capacitance at COM[3]	F_{IN} = 1MHz @ 0V		68	80	pF
O_{ISO}	Off isolation[4]	R_L = 600Ω C_L = 50pF F_{IN} = 1kHz sine wave			-80	dB
BW	Bandwidth[4]	R_{SOURCE} = 50Ω R_L = 2.2MΩ C_L = 12pF V_{IN} = 1Vp-p	51			MHz
X_{TALK2}	Cross talk (Between any 2 Channels)[4]	R_L = 1kΩ C_L = 50pF F_{IN} = 1kHz sine wave			-80	dB
t_S	Settling time of output at COM within 1% of final output voltage[4]	R_L = 100kΩ C_L = 50pF			120	ns
THD	Total Harmonic Distortion[4]	R_L = 1kΩ C_L = 50pF F_{IN} = 1MHz sine wave V_{IN} = 5Vp-p			5.0	%

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Continuous operation with low load resistance is not recommended. (See Figure 12)
3. Parameters guaranteed by characterization.
4. Parameters guaranteed by design.

TIMING CHARACTERISTICS (UT16MX110)[1,2]

(AV_{DD}=5.0V $\pm$ 0.5V, GND = 0V; -55°C $\leq T_C \leq$ +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
t_{PROP_S}	Propagation delay of analog input (S[x]) to analog output (COM) measured at 50%	$R_T = 50\Omega$ C_L = 50pF See Figures 10 & 13			25	ns
t_{PROP_D}	Propagation delay of any changes in the digital inputs (A[3:0], $\overline{CS}$, PLATCH, $\overline{SS}$) affecting the analog output (COM)	$R_T = 50\Omega$ C_L = 50pF See Figures 5 & 13	25		140	ns
t_{MUX}	Mux decoding time	$R_T = 50\Omega$ C_L = 50pF See Figures 5 & 13			50	ns
t_{BBM}	Break-Before-Make-Delay	$R_T = 50\Omega$ C_L = 50pF See Figures 5 & 13	15		90	ns
t_{AS1}	The minimum amount of time required for the address signals (A[3:0]) to be stable before the falling edge of $\overline{CS}$[3]	See Figure 5	3.0			ns
t_{AS2}	The minimum amount of time required for the address signals (A[3:0]) to be stable after the rising edge of $\overline{CS}$[3]	See Figure 5	5.0			ns

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Continuous operation with low load resistance is not recommended. (See Figure 12)
3. Parameters guaranteed by design.

TIMING CHARACTERISTICS (UT16MX111)[1,2]

(AV_{DD}=5.0V $\pm$ 0.5V, GND=0V; -55°C $\leq T_C \leq$ +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
t_{PROP_S}	Propagation delay of analog input (S[x]) to analog output (COM) measured at 50%	R_T = 50Ω C_L = 50pF See Figures 10& 13			25	ns
t_{PROP_D}	Propagation delay of any changes in the digital inputs (A[3:0], $\overline{CS}$, PLATCH, $\overline{SS}$) affecting the analog output (COM)	R_T = 50Ω C_L = 50pF See Figures 6 & 13	25		140	ns
t_{MUX}	Mux decoding time	R_T = 50Ω C_L = 50pF See Figures 6 & 13			50	ns
t_{BBM}	Break-Before-Make-Delay	R_T = 50Ω C_L = 50pF See Figures 6 & 13	15		90	ns
t_{PZLH}	Output enable time from HiZ to low or high once $\overline{RESET}$ is pulled high	R_T = 50Ω C_L = 50pF See Figures 9 & 13			90	ns
t_{PLHZ}	Output disable time from low or high to HiZ once $\overline{RESET}$ is pulled low	R_T = 50Ω C_L = 50pF See Figures 9 & 13			55	ns
t_{LSU}	Address setup time wrt rising edge PLATCH	R_T = 50Ω C_L = 50pF See Figures 6 & 13	5.0			ns
t_{LHD}	Address hold time wrt rising edge PLATCH	R_T = 50Ω C_L = 50pF See Figures 6 & 13	10			ns

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information)
2. Continuous operation with low load resistance is not recommended. (See Figure 12)

TIMING CHARACTERISTICS (UT16MX112)[1,2]

(AV_{DD}=5.0V ± 0.5V, GND = 0V; -55°C ≤ T_C ≤ +125°C)

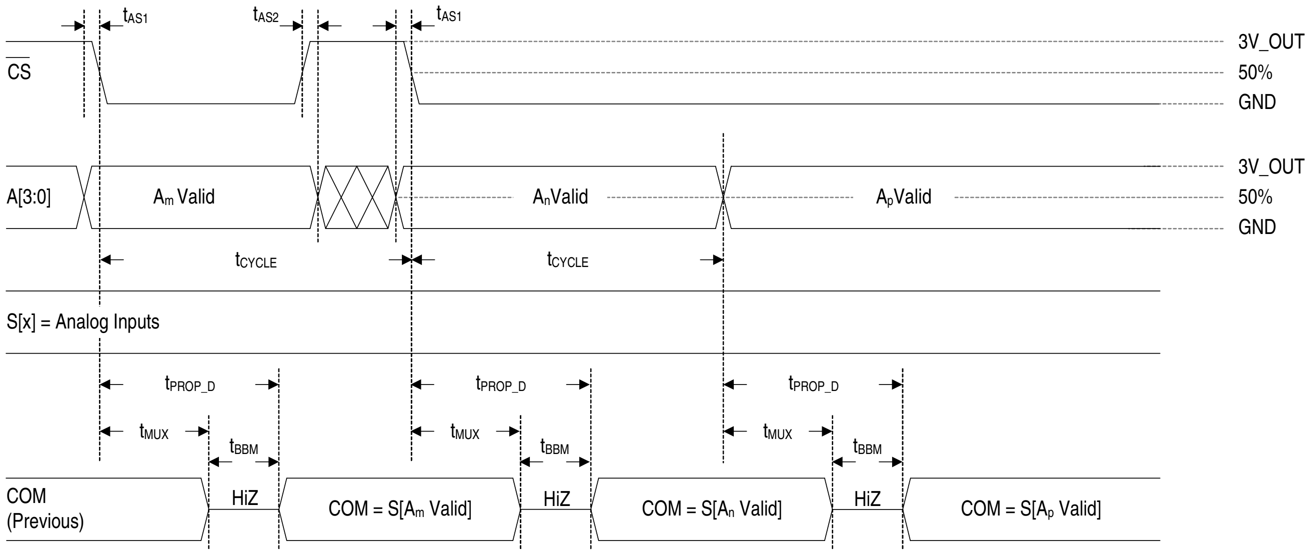
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
t_{PROP_S}	Propagation delay of analog input (S[x]) to analog output (COM) measured at 50%	R_T = 50Ω C_L = 50pF See Figures 10 & 13			25	ns
t_{PROP_D}	Propagation delay of any changes in the digital inputs (A[3:0], $\overline{CS}$, PLATCH, $\overline{SS}$) affecting the analog output (COM)	R_T = 50Ω C_L = 50pF See Figures 7 & 13	25		140	ns
t_{MUX}	Mux decoding time	R_T = 50Ω C_L = 50pF See Figures 7 & 13			50	ns
t_{BBM}	Break-Before-Make-Delay	R_T = 50Ω C_L = 50pF See Figures 7 & 13	15		90	ns
t_{PZLH}	Output enable time from HiZ to low or high once $\overline{RESET}$ is pulled high	R_T = 50Ω C_L = 50pF See Figures 9 & 13			90	ns
t_{PLHZ}	Output disable time from low or high to HiZ once $\overline{RESET}$ is pulled low	R_T = 50Ω C_L = 50pF See Figures 9 & 13			55	ns
f_{SCLK}	SCLK frequency	See Figure 7			2.0	MHz
t_H	SCLK high time	See Figure 7	190			ns
t_L	SCLK low time	See Figure 7	190			ns
t_{SSU}	First SCLK setup time (for shifting window)	See Figure 7	6.0			ns
t_{SSH}	Last SCLK hold time (for shifting window)	See Figure 7	10			ns
t_{SU}	Data in (MOSI) setup time wrt rising edge SCLK	See Figure 7	3.0			ns
t_{HD}	Data in (MOSI) hold time wrt rising edge SCLK	See Figure 7	5.0			ns
t_{DO}	Data out (MISO) valid (after falling edge of SCLK)	C_L = 50pF See Figure 7			43	ns
t_{DR}	Data out (MISO) rise time	10-90% of 3V_OUT C_L = 50pF			30	ns
t_{DF}	Data out (MISO) fall time	10-90% of 3V_OUT C_L = 50pF			20	ns

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Continuous operation with low load resistance is not recommended. (See Figure 12).

Timing Diagrams

Multiplexer Asynchronous Parallel Timing (UT16MX110)

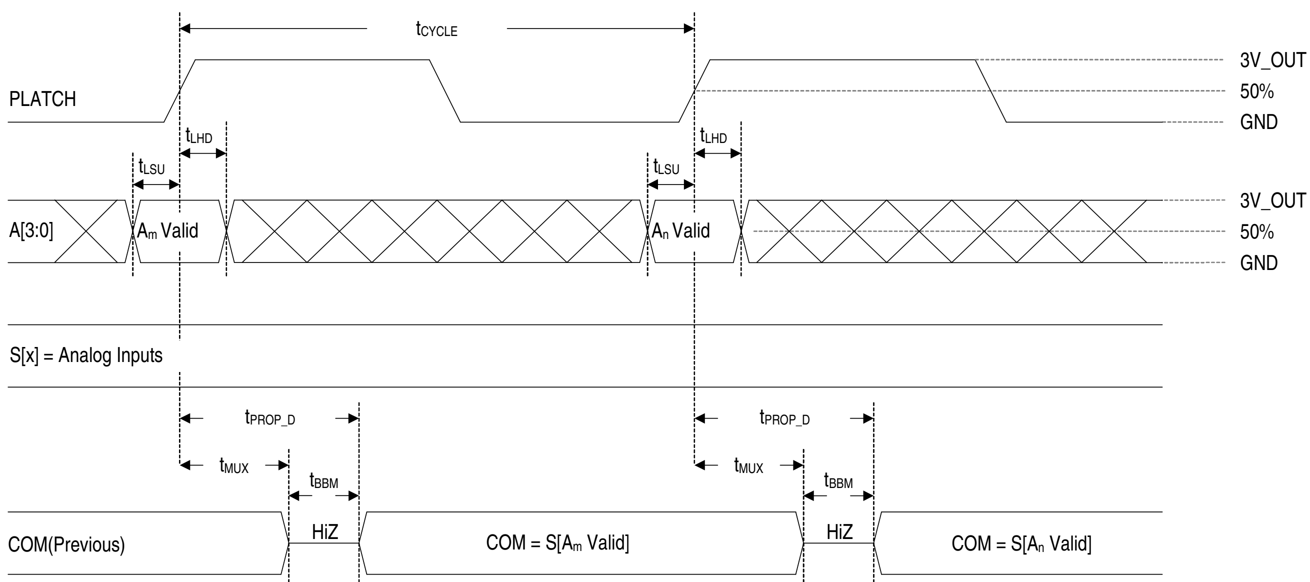


Note:

1. $\overline{CS}$ may be held in a continuous low state, holding $\overline{CS}$ high provides protection for false address change.
2. t_{CYCLE} is the minimum cycle time between the falling edges of $\overline{CS}$ and/or any address changes. If t_{CYCLE} is shorter than t_{PROP_D}, an addressing error may occur.
3. All bits (A[3:0]) of any address change should be received by the MUX within 18ns of the first bit change for proper operation.

Figure 5. UT16MX110 Timing Diagram

Multiplexer Synchronous Parallel Timing (UT16MX111)



Note:

1. When PLATCH is in a high or low state, it provides protection for false address change.
2. t_{CYCLE} must not be less than the maximum value of t_{PROP_D}.

Figure 6. UT16MX111 Timing Diagram

Multiplexer Serial Timing (UT16MX112)

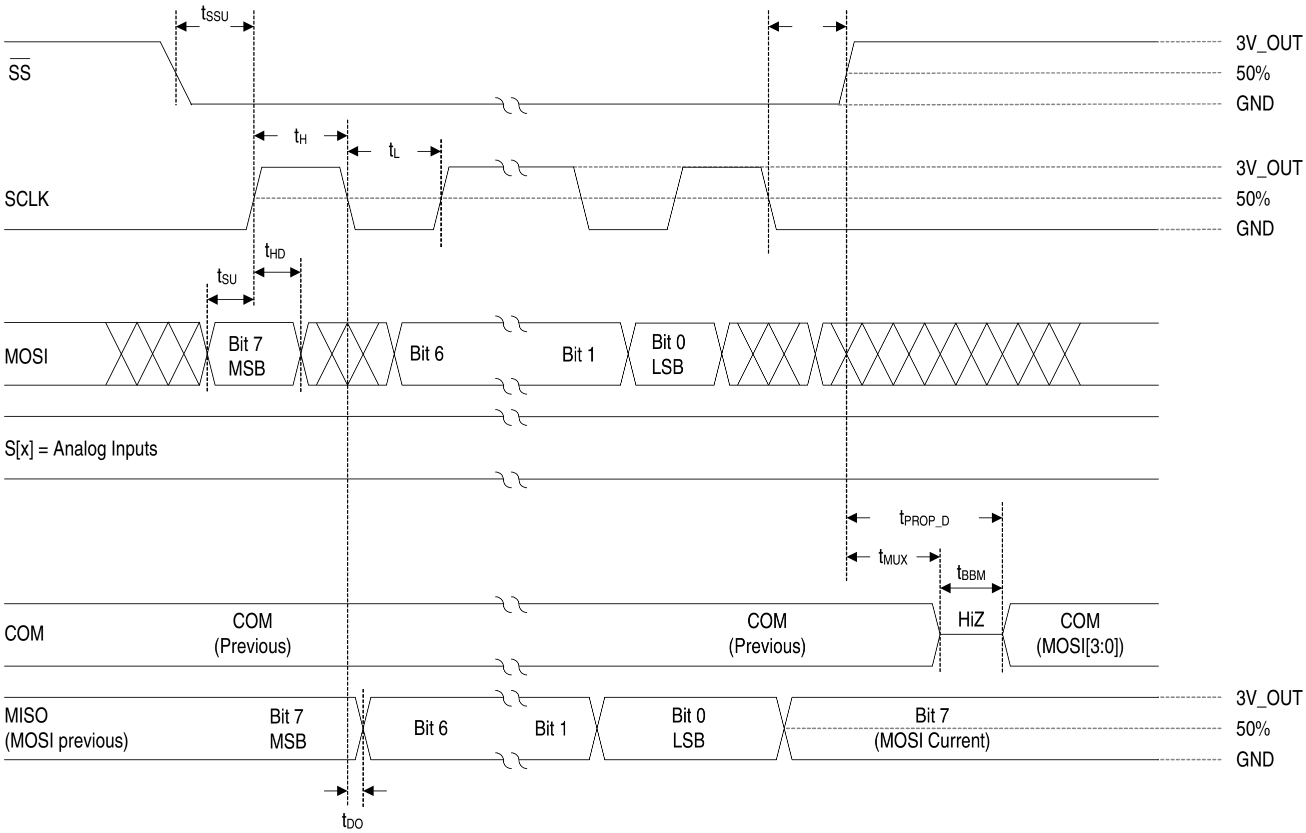
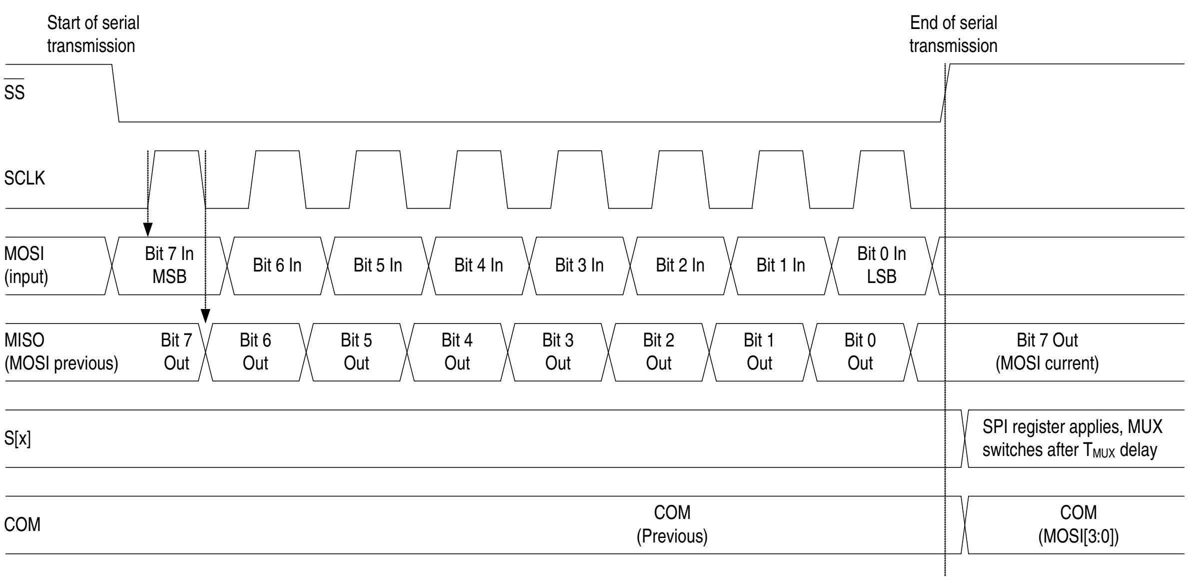


Figure 7. UT16MX112 Timing Diagram

SPI™ Protocol (UT16MX112)

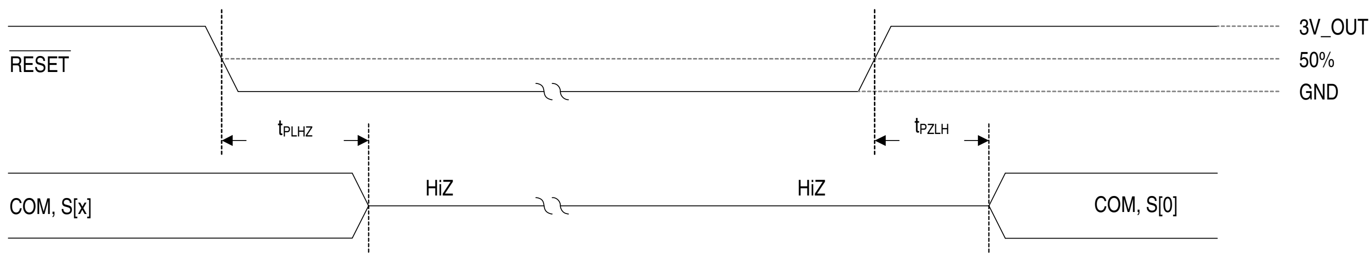


Note:

1. See FIGURE 7, Multiplexer Serial Timing (UT16MX112), for detailed timing.

Figure 8. SPI™ Protocol Timing

Multiplexer RESET Enable/Disable (UT16MX111/112)

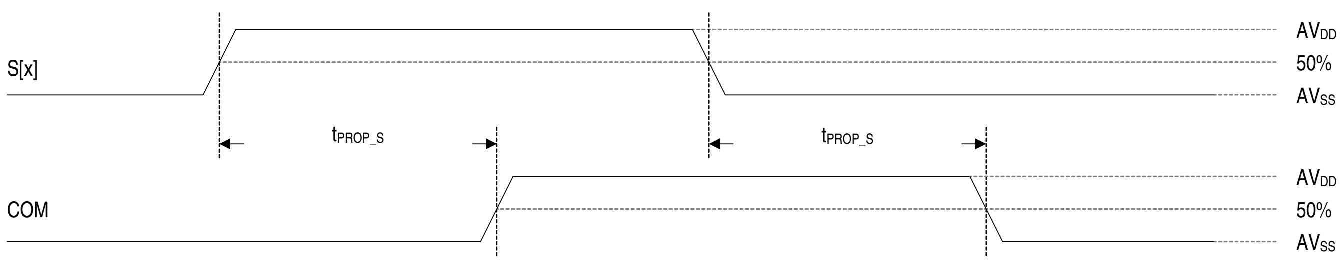


Note:

1. S[x] represents the analog signal channel connected to COM prior to the falling edge of RESET.

Figure 9. RESET Timing Diagram (Used for UT16MX111/112 only)

Multiplexer Analog Timing (UT16MX110/111/112)

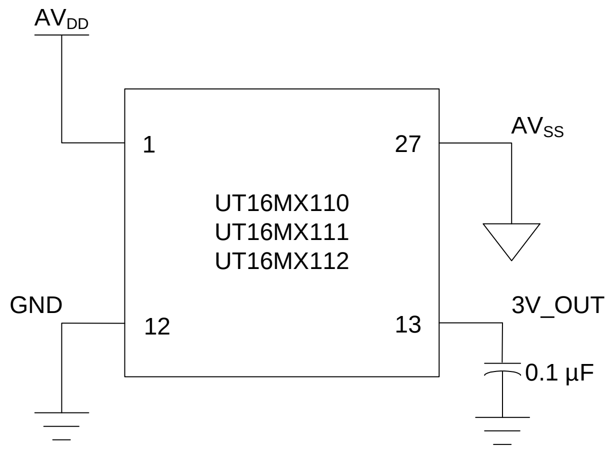


Note:

1. S[x] represents the analog signal channel connected to COM while in active mode of all device types with the address already set and all digital inputs held constant.

Figure 10. Analog Timing Diagram (Used for UT16MX110/111/112

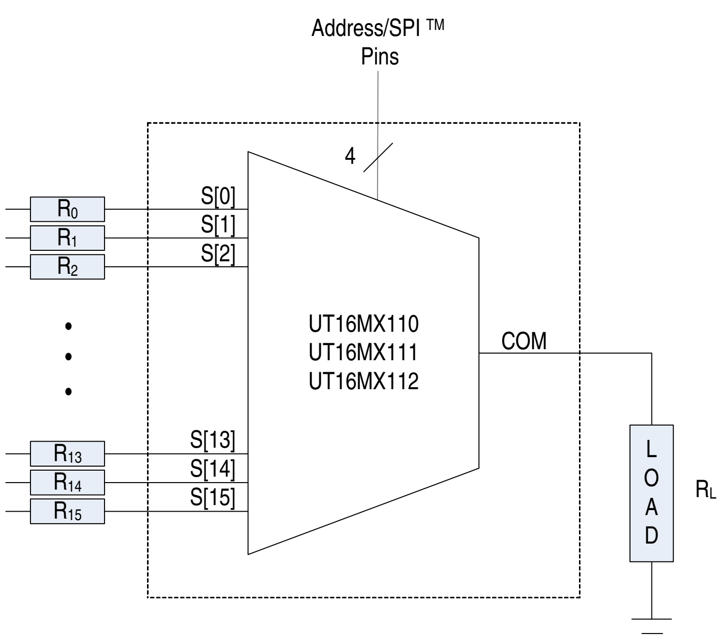
Power Supply Requirements Schematic (UT16MX110/111/112)



Note:
1. Bypass capacitor of 0.1µF required on 3V_OUT for proper operation.

Figure 11. Power Supply Requirements

Minimum Multiplexer Total Path Resistance (UT16MX110/111/112)



$R_i + R_L \geq 500\Omega$
$(0 \leq i \leq 15)$

Note:

1. Continuous DC operation on any single channel where $R_i + R_L < 500\Omega$ will degrade device reliability and performance.

Figure 12. Minimum Total Path Resistance for Continuous DC Operation on Any Single Channel

Multiplexer Load Conditions for Test (UT16MX110/111/112)

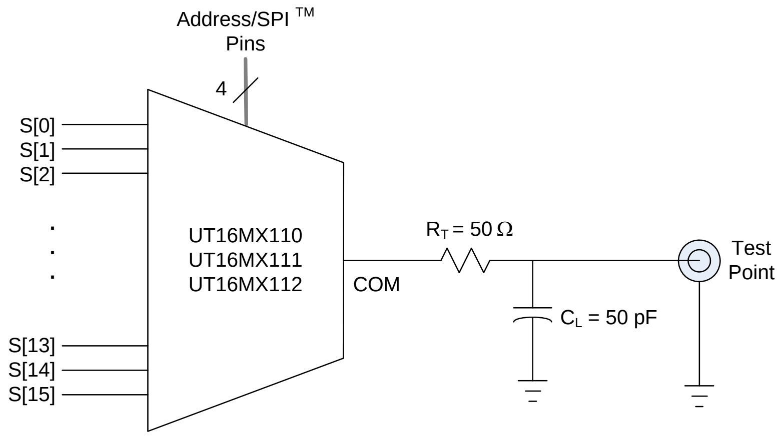


Figure 13. UT16MX110/111/112 Test Circuit

PACKAGING

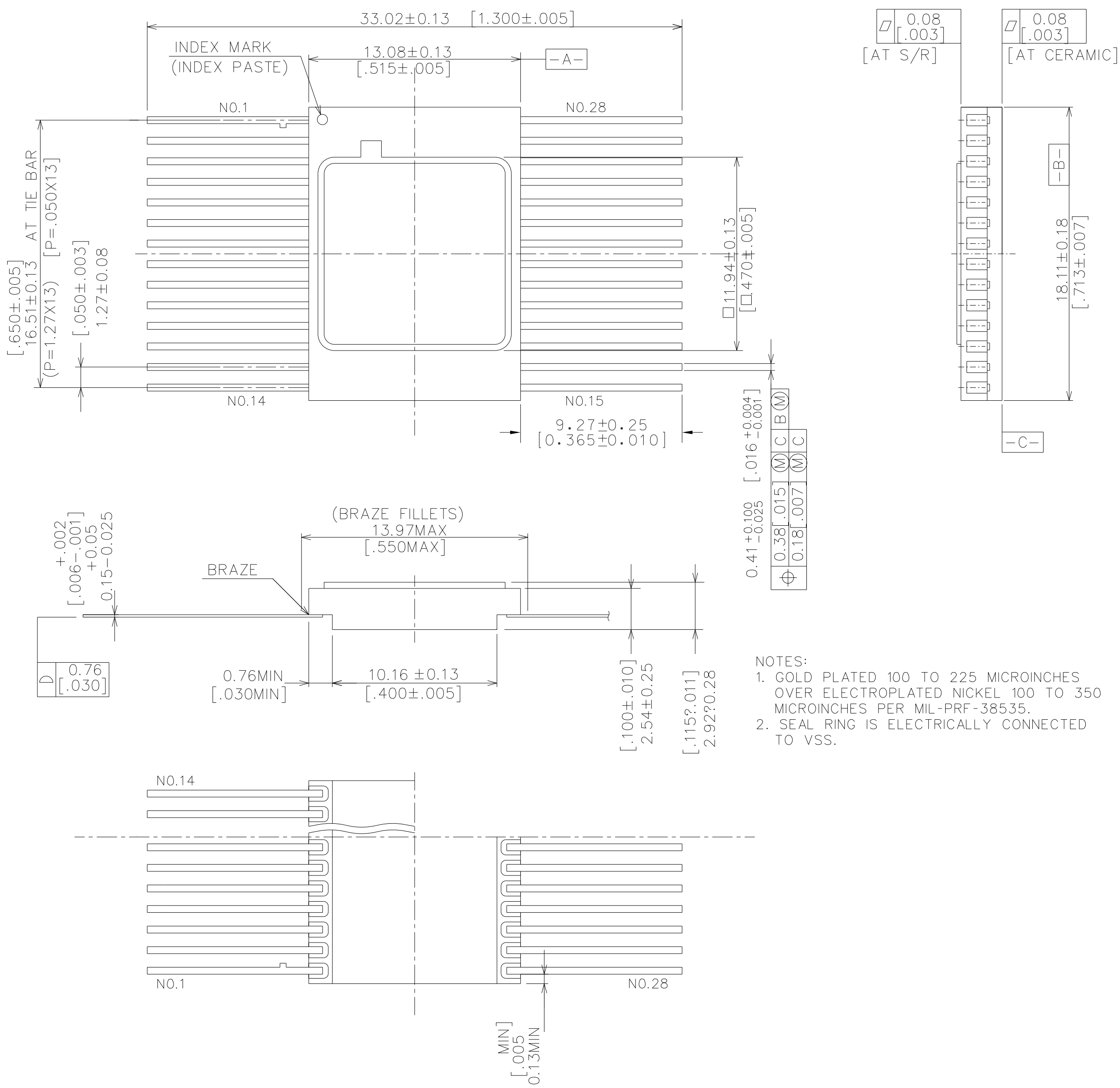


Figure 14. 28-Lead Ceramic Flat Package

TRADEMARKS:

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ORDERING INFORMATION

UT16MX110/111/112 ANALOG MULTIPLEXER

UT ***** ** * * * *

Lead Finish: **(Note 1)**
(C) = Gold

Screening Level: **(Note 2 and 3)**
(P) = Prototype Flow
(C) = HiRel Flow

Case Outline:
(X) = 28-pin CFP ceramic flatpack

TID Tolerance:
(-) = None

Device Type:
(10) = Asynchronous Parallel
(11) = Synchronous Parallel
(12) = Serial (SPI™)

Generic Part Number:
(16MX1) = 16:1 MUX

Notes:
1. Lead finish is "C" (Gold) only.
2. Prototype flow per Aeroflex Manufacturing Flows Document. Devices are tested at 25°C only. Lead finish is Gold "C" only. Radiation neither tested nor guaranteed.
3. HiRel flow per Aeroflex Manufacturing Flows Document.

UT16MX110/111/112 ANALOG MULTIPLEXER: SMD

5962 * 10233 ** * * *

Lead Finish **(Note 1)**:
(C) = Gold

Case Outline:
(X) = 28-pin CFP ceramic flatpack

Class Designator:
(Q) = QML Class Q
(V) = QML Class V

Device Type:
(01) = Asynchronous Parallel
(03) = Synchronous Parallel
(04) = Serial (SPI™)

Drawing Number:10233

Total Dose:
(R) = 100 krad(Si)
(F) = 300 krad(Si)

Federal Stock Class Designator: No options

Notes:
1. Lead finish is "C" (Gold) only.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

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