

# UT54ALVC2525 Clock Driver

## 1 to 8 Minimum Skew

Data Sheet  
October 2012



### FEATURES

- ❑ 2.0V to 3.6V Power supply operation
- ❑ Guaranteed pin-to-pin and part-to-part skew
- ❑ Eight LVTTTL outputs with high drive strength
- ❑ Operational environment:
  - Total-dose tolerance: 100 to 300 krad(Si), or 1 Mrad(Si)
  - SEL Immune to a LET of 111 MeV-cm<sup>2</sup>/mg
- ❑ HiRel temperature range: -55°C to +125°C
- ❑ Packaging options:
  - 14-Lead Ceramic Flatpack
- ❑ Standard Microcircuit Drawing: 5962-06233
  - QML Q and V

### INTRODUCTION

The UT54ALVC2525 is a low-voltage, minimum skew, one-to-eight clock driver. The UT54ALVC2525 distributes a single clock to eight, high-drive, outputs with low skew across all outputs during both the  $t_{PLH}$  and  $t_{PHL}$  transitions making it ideal for signal generation and clock distribution. The output pins act as a single entity and will follow the state of the CLK pin.

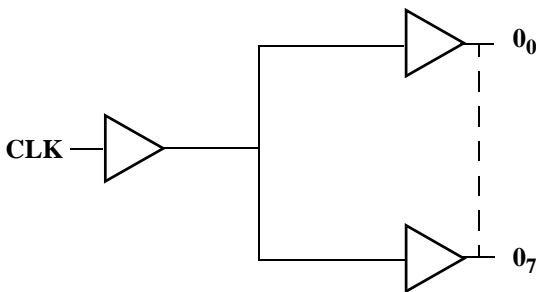


Figure 1: UT54ALVC2525 Block Diagram

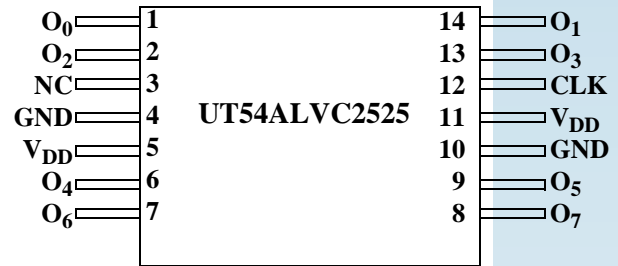


Figure 2. 14-Lead Ceramic Flatpack Pinouts

## PIN DESCRIPTION

Flatpack Pin No.	Name	I/O	Type	Description
12	CLK	I	LVTTL	Primary reference clock input. This pin must be driven by an LVTTL or LVCMOS clock source.
3	N/C	--	--	No connect.
1, 2, 6, 7, 8, 9, 13, 14	O <sub>n</sub>	O	LVTTL	Eight output clocks.
5, 11	V <sub>DD</sub>	PWR	Power	Power supply for internal circuitry and output buffers.
4, 10	V <sub>SS</sub>	PWR	Power	Ground

## OPERATIONAL ENVIRONMENT

The UT54ALVC2525 incorporates special design, layout, and process features which allows operation in a limited HiRel environment.

Parameter	Limit	Units
Total Ionizing Dose (TID)	>1E6	rads(Si)
Single Event Latchup (SEL) <sup>1, 2</sup>	>111	MeV-cm <sup>2</sup> /mg
Onset Single Event Upset (SEU) LET (@2.0V) <sup>3, 5</sup>	52	MeV-cm <sup>2</sup> /mg
Onset Single Event Upset (SEU) LET (@3.0V) <sup>4, 5</sup>	66	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1.0E14	n/cm <sup>2</sup>
Dose Rate Upset	TBD	rads(Si)/sec
Dose Rate Survivability	TBD	rads(Si)/sec

### Notes:

1. The UT54ALVC2525 is latchup immune to particle LETs >111 MeV-cm<sup>2</sup>/mg.
2. SEL temperature and voltage conditions of T<sub>C</sub> = +125°C, V<sub>DD</sub> = 3.6V.
3. SEU temperature and voltage conditions of T<sub>C</sub> = +25°C, V<sub>DD</sub> = 2.0V. Tested at 200MHz.
4. SEU temperature and voltage conditions of T<sub>C</sub> = +25°C, V<sub>DD</sub> = 3.0V. Tested at 200MHz.
5. For the UT54ALVC2525 SET performance at select operating frequency data ranges, please contact the factory.

## ABSOLUTE MAXIMUM RATINGS:<sup>1</sup>

(Referenced to  $V_{SS}$ )

Symbol	Description	Limits	Units
$V_{DD}$	Core Power Supply Voltage	-0.3 to 4.0	V
$V_{IN}$	Voltage Any Clock Input	-0.3 to $V_{DD} + 0.3$	V
$V_{OUT}$	Voltage Any Clock Output	-0.3 to $V_{DD} + 0.3$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Maximum Power Dissipation	1	W
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_J$	Maximum Junction Temperature <sup>2</sup>	+150	°C
$\Theta_{JC}$	Thermal Resistance, Junction to Case	20	°C/W
$ESD_{HBM}$	ESD Protection (Human Body Model) - Class II	>3000	V

### Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.

## RECOMMENDED OPERATING CONDITIONS:

Symbol	Description	Limits	Units
$V_{DD}$	Core Operating Voltage	2.0 to 3.6	V
$V_{IN}$	Voltage Clock Input	0 to $V_{DD}$	V
$V_{OUT}$	Voltage Any Clock Output	0 to $V_{DD}$	V
$T_C$	Case Operating Temperature	-55 to +125	°C

## DC ELECTRICAL CHARACTERISTICS (Pre- and Post-Radiation)\*

( $V_{DD} = 2.0V$  to  $3.6V$ ;  $T_C = -55^{\circ}C$  to  $+125^{\circ}C$ )

Symbol	Description	Conditions	$V_{DD}$	Min.	Max.	Units
$V_{IH}^1$	High level input voltage		2.0V 2.75V 3.0V 3.6V	1.25 1.5 1.75 2.0		V
$V_{IL}^1$	Low level input voltage		2.0V 2.75V 3.0V 3.6V		0.7 0.8 0.8 0.8	V
$V_{OL}$	Low level output voltage	$I_{OL} = 12mA$ $I_{OL} = 12mA$ $I_{OL} = 12mA$ $I_{OL} = 12mA$	2.0V 2.75V 3.0V 3.6V		0.45 0.4 0.4 0.4	V
$V_{OH}$	High level output voltage	$I_{OH} = -12mA$ $I_{OH} = -12mA$ $I_{OH} = -12mA$ $I_{OH} = -12mA$	2.0V 2.75V 3.0V 3.6V	1.5 2.2 2.4 3.0		V
$I_{OS}^2$	Short-circuit output current	$V_{OUT} = V_{DD}$ and $V_{SS}$	2.0V 3.6V	-200 -300	200 300	mA
$I_{IL}$	Input leakage current	$V_{IN} = V_{DD}$ or $V_{SS}$	3.6V	-1	1	$\mu A$
$I_{DDQ}$	Quiescent Supply Current	$V_{IN} = V_{DD}$ or $V_{SS}$	2.0V 3.6V		1.0 1.0	mA
$P_{TOTAL}^3$	Total power dissipation	$C_L = 20pF$	2.0V 2.75V 3.0V 3.6V		1.2 2.7 3.5 5.2	mW/MHz
$C_{IN}^4$	Input capacitance	$f = 1MHz$	0V		15	pF
$C_{OUT}^4$	Output capacitance	$f = 1MHz$	0V		15	pF

### Notes:

\* Post-radiation performance guaranteed at  $25^{\circ}C$  per MIL-STD-883 Method 1019, Condition A up to a TID level of  $1.0E6$  rad(Si).

- Functional tests are conducted in accordance with MIL-STD-883 with the following test conditions:  $V_{IH} = V_{IH}(\min) + 20\%$ ,  $-0\%$   $V_{IL} = V_{IL}(\max) + 0\%$ ,  $-50\%$ , as specified herein for the LVTTTL and LVCMOS inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH}(\min)$ ,  $V_{IL}(\max)$ .
- Supplied as a design limit. Neither guaranteed nor tested.
- When measuring the dynamic supply current, all outputs are loaded in accordance with the equivalent test load defined in figure 3.
- Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and the VSS at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.

**AC ELECTRICAL CHARACTERISTICS (Pre- and Post-Radiation)\***

( $V_{DD} = 2.0V$  to  $3.6V$ ;  $T_C = -55^{\circ}C$  to  $+125^{\circ}C$ )

Symbol	Description	Condition	$V_{DD}$	Min.	Max.	Unit
$t_R, t_F^3$	Input rise/fall time	$V_{IH}(\text{min}) - V_{IL}(\text{max})$	3.6V		20	ns/V
$t_{PHL}^{1,2}$	Propagation delay: CLK to On, high-to-low transition	Measured as transition time between $V_{IN} = V_{DD} \div 2$ to $V_{OUT} = V_{DD} \div 2$	2.0V 2.75V 3.0V 3.6V	3.5 3.0 2.75 2.25	7.5 5.5 5.25 4.75	ns
$t_{PLH}^{1,2}$	Propagation delay: CLK to On, low-to-high transition	Measured as transition time between $V_{IN} = V_{DD} \div 2$ to $V_{OUT} = V_{DD} \div 2$	2.0V 2.75V 3.0V 3.6V	3.25 2.75 2.5 2.0	7.25 5.25 5.0 4.5	ns
$t_{OSHL}^{2,4,5}$	Maximum skew: common edge, output-to-output, high-to-low transition	Measured as $V_{On} = V_{DD} \div 2$ to $V_{Om} = V_{DD} \div 2$ where $n, m = 0$ to $7$ ; $n$ not equal to $m$ @ $f_{CLK} = 200\text{MHz}$	2.0V 3.6V		0.15 0.25	ns
$t_{OSLH}^{2,4,5}$	Maximum skew: common edge, output-to-output, low-to-high transition	Measured as $V_{On} = V_{DD} \div 2$ to $V_{Om} = V_{DD} \div 2$ where $n, m = 0$ to $7$ ; $n$ not equal to $m$ @ $f_{CLK} = 200\text{MHz}$	2.0V 3.6V		0.15 0.25	ns
$t_{ORISE}^3$ & $t_{OFALL}$	Output rise/fall time	Measured as transition time between $20\% * V_{OL}$ and $80\% * V_{OH}$ @ $f_{CLK} = 100\text{MHz}$	2.0V 3.6V		2.4 2.0	ns
$t_{PART}^{4,5}$	Part-part skew	Skew between the same output of any two devices under identical settings and conditions ( $V_{DD}$ , temp, air flow, frequency, etc).	2.0V 3.6V		0.1 0.15	ns
$t_{PBAL}^{1,4}$	Propagation delay balance: difference between same output, low-to-high and high-to-low transitions	Measured as transition time between $V_{IN} = V_{DD} \div 2$ to $V_{OUT} = V_{DD} \div 2$	2.0V 2.75V 3.0V 3.6V		0.43 0.3 0.26 0.21	ns

**Notes:**

\* Post-radiation performance guaranteed at  $25^{\circ}C$  per MIL-STD-883 Method 1019, Condition A up to a TID level of  $1.0E6$  rad(Si).

1. Test load =  $40\text{pF}$ , terminated to  $V_{DD} \div 2$ . All outputs are equally loaded. Reference Figure 3 for clock output loading.
2. Reference Figure 4 for AC timing diagram.
3. Supplied only as a design guideline, neither tested nor guaranteed.
4. Guaranteed by characterization, but not tested.
5. Test load =  $40\text{pF}$ , terminated to  $V_{DD} \div 2$ . All outputs are equally loaded. Reference Figure 5 for clock output loading.

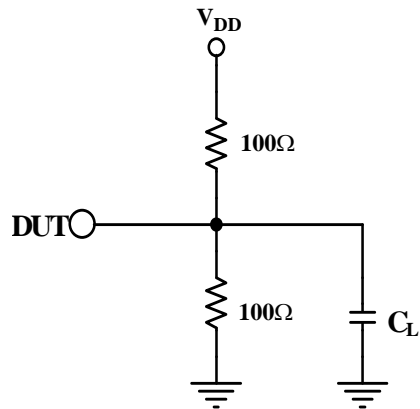


Figure 3.

**Test Load Circuit for Dynamic Power Supply Current and AC Measurements**

Note: This is not the recommended termination for normal user operation.

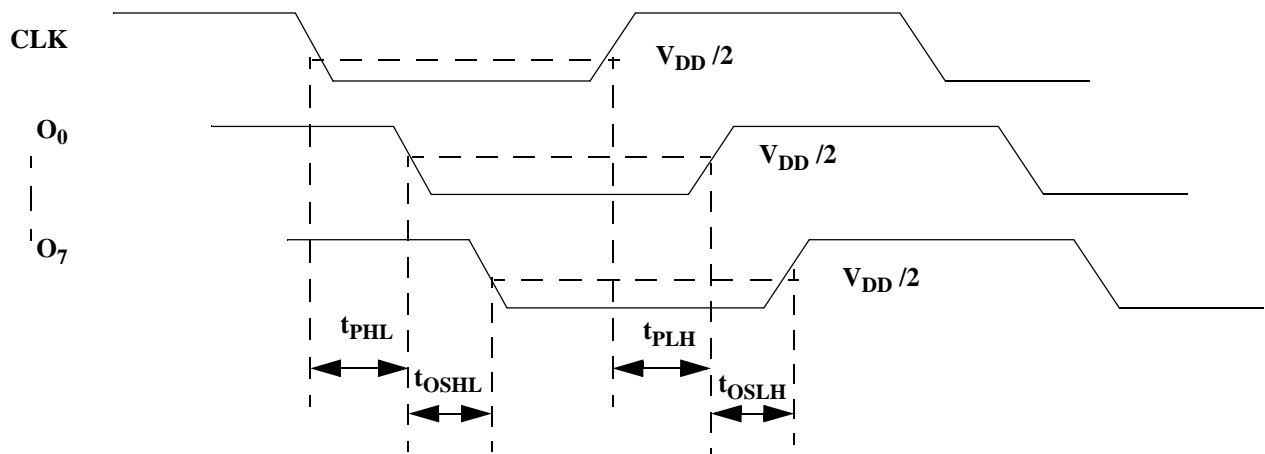


Figure 4. AC Timing Diagram

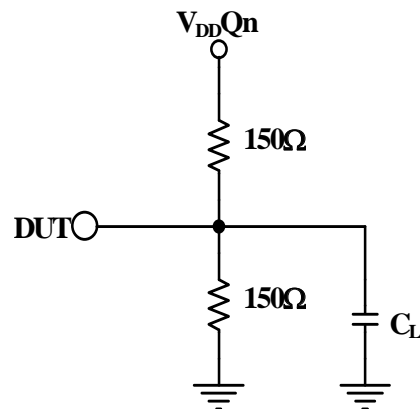
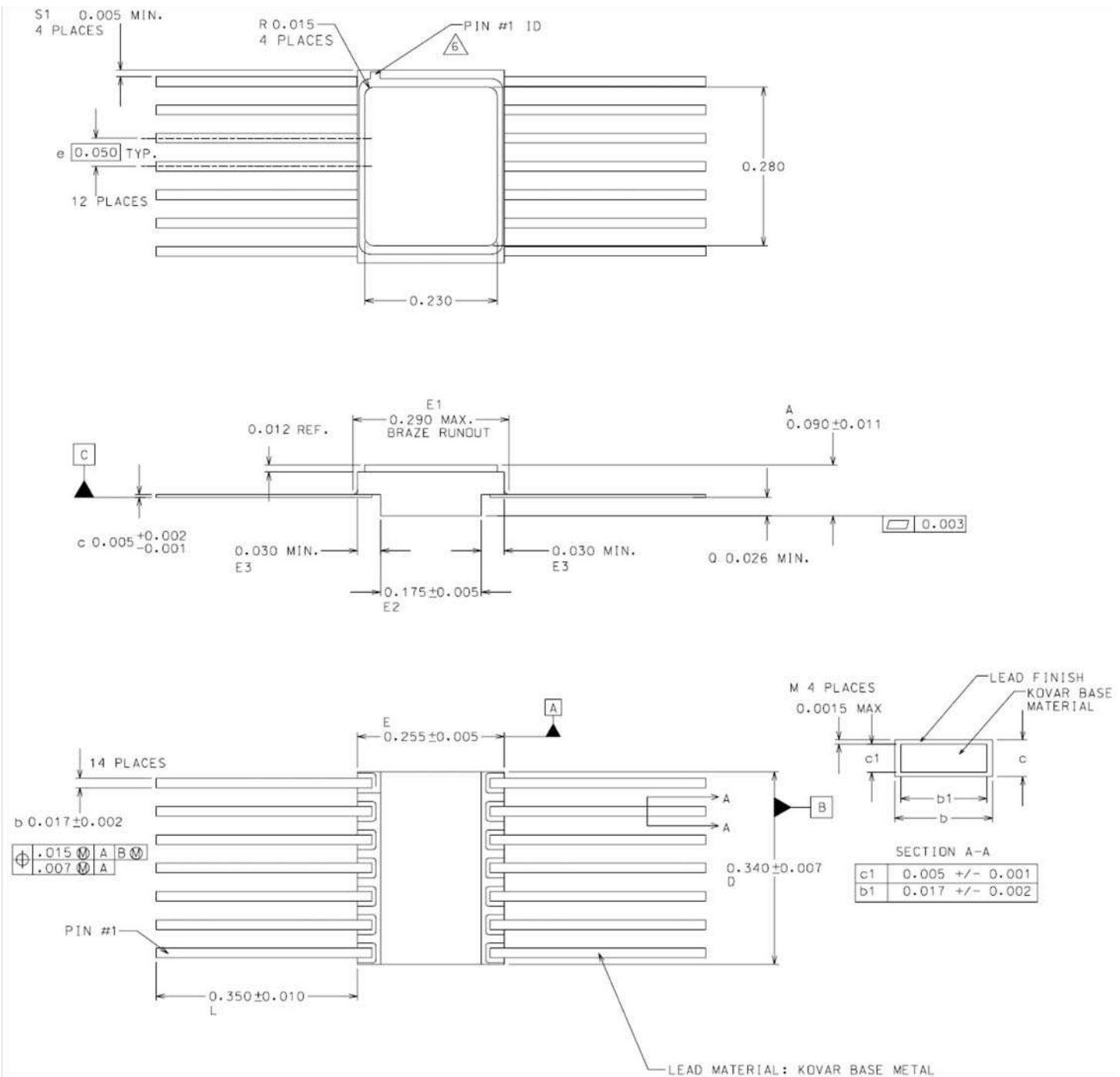


Figure 5. Test Load Circuit for  $t_{OSHL}$  and  $t_{OSLH}$  Measurements

# PACKAGING

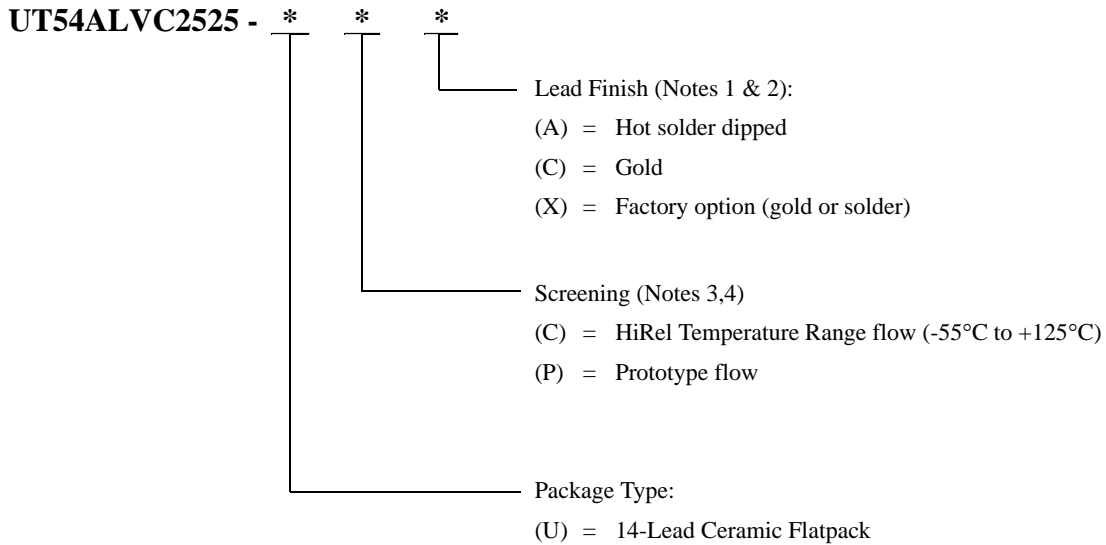


1. All exposed metallized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to  $V_{SS}$ .
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbol is in accordance with MIL-PRF-38533.
5. Lead position and colanarity are not measured.
6. ID mark symbol is vendor option.

Figure 6. 14-Pin Flatpack Package

## ORDERING INFORMATION

### UT54ALVC2525:

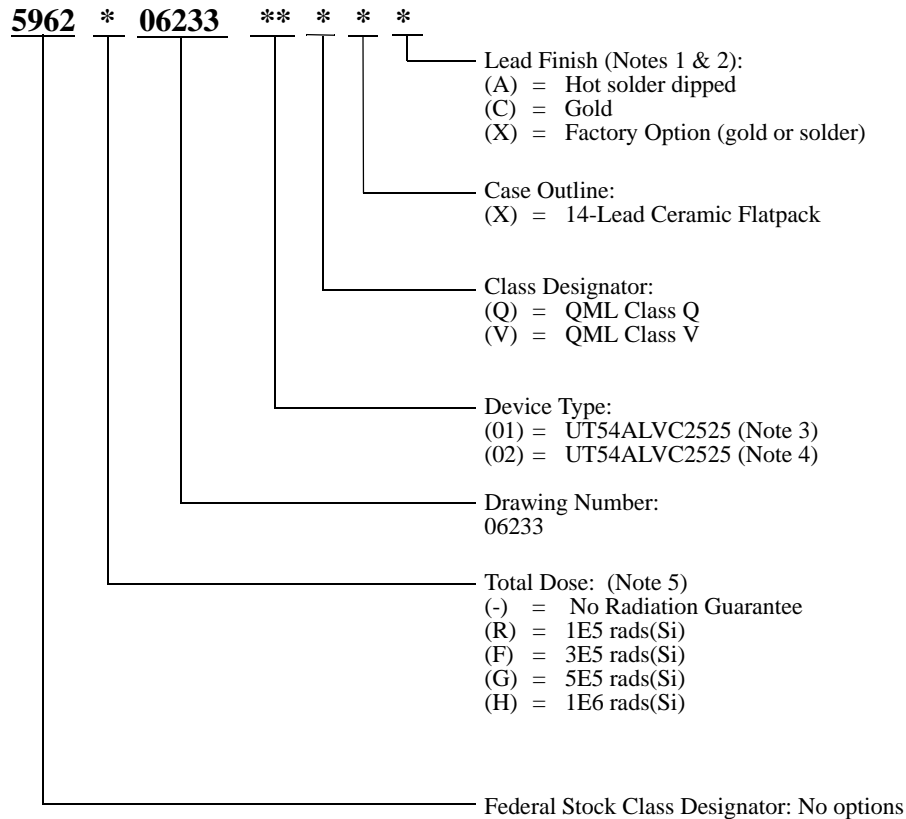


#### Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. HiRel Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.



## UT54ALVC2525: SMD



### Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold)
3. Available to a maximum RHA level of H.
4. Available to a maximum RHA level of R. Device is irradiated at a dose rate = 50-300 rads(Si)/s in accordance with MIL-STD-883, Method 1019, Condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rads(Si)/s per MIL-STD-883, Method 1019, Condition A, section 3.11.2. The total dose specification for these devices only applies to a low dose rate environment.
5. Total dose radiation must be specified when ordering. QML Q and QML V are not available without radiation hardening.

# ***Aeroflex Colorado Springs - Datasheet Definition***

**Advanced Datasheet - Product In Development**

**Preliminary Datasheet - Shipping Prototype**

**Datasheet - Shipping QML & Reduced HiRel**

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Fax: 805-778-1980

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Fax: 603-888-4585

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Fax: 321-951-4254

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