

Surface Mount PIN Diode Limiters

LM202402-Q-E-301 & LM202402-Q-F-301

Series Datasheet

Features

- Surface Mount Limiters in Compact Package:
8 mm L x 5 mm W x 2.5 mm H
- Incorporates PIN Limiter Diodes, DC Blocks, Schottky Diode & DC Return
- Wide Frequency Range (2 to 4 GHz)
- Higher Peak Power Handling than Plastic-Packaged Limiters (1000 W Peak)
- Higher Average Power Handling than Plastic-Packaged Limiters (100 W CW)
- Very Low Insertion Loss (0.35 dB)
- Low Flat Leakage Power (17 dBm)
- RoHS Compliant



Applications

- Receiver protection

Description

The LM202402-Q-E-301 and LM202402-Q-F-301 are surface mount, two-stage silicon PIN diode limiters which can operate over the frequency range of 2 GHz to 4 GHz. They are manufactured using Aeroflex/Metelics proven hybrid manufacturing process incorporating PIN diodes, Schottky diodes and passive devices integrated onto a ceramic substrate. This low profile, compact (8 mm L x 5 mm W x 2.5 mm H), surface mount component, offers outstanding small and large signal performance. The LM202402-Q-E-301 comprises a DC block at its input, shunt PIN limiter diodes driven by a Schottky diode detector stage, and an antiparallel pair of a limiter PIN diode and a Schottky detector diode at its output. The LM202402-Q-F-301 comprises all these components as well as a DC block at its output.

The very low thermal resistance (< 70 °C/W, from the input limiter PIN diode junctions to the package mounting surface) of the PIN diodes in this device enables it to reliably handle RF incident power levels up to 50 dBm CW and RF peak incident power levels up to 60 dBm (25 μ s pulse width, 1% duty cycle) at $T_{CASE} = 85$ °C. The I layer thickness of the output stage and the barrier height of its Schottky detector diode are selected to produce flat leakage of 13 dBm typical and spike leakage energy of 0.5 ergs, typical. No external control signals are required.

Environmental Capabilities

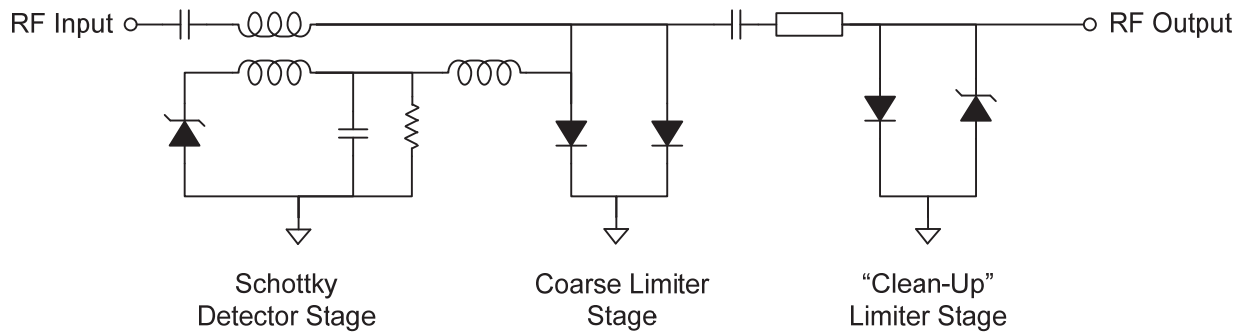
The LM202402-Q-E-301 and LM202402-Q-F-301 limiters are ideal for 2 to 4 GHz radar, IED jammers and LTE-TDD base station applications. They are compatible with high volume, surface mount, solder re-flow manufacturing methods. These products are durable, reliable, and capable of operating reliably in military, commercial, and industrial environments. These devices are RoHS compliant and are available in tube and tape-reel. The LM102202-Q-C-301 limiter is capable of meeting the environmental requirements of MIL-STD-750 and MIL-STD-202.

ESD and Moisture Sensitivity Level Rating

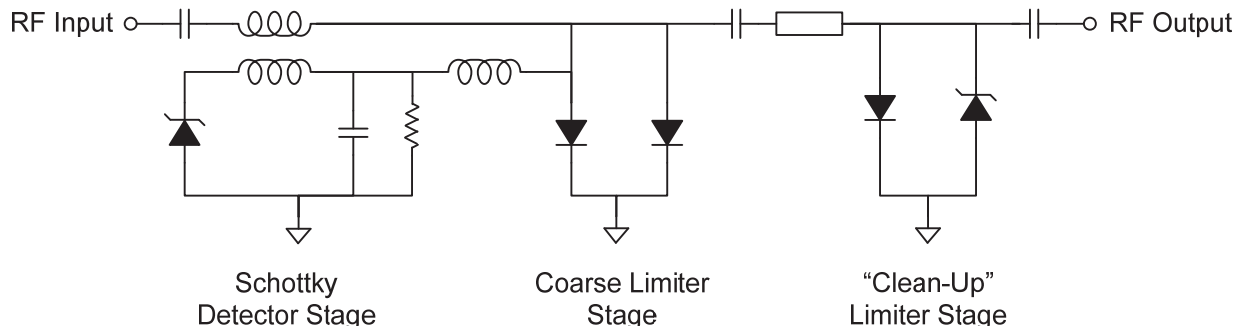
As are all semiconductor devices, PIN and Schottky diodes are susceptible to damage from ESD events. The ESD rating for LM202402-Q-E-301 and LM202402-Q-F-301 is Class 0 (HBM). The moisture sensitivity level rating for these devices is MSL 1.



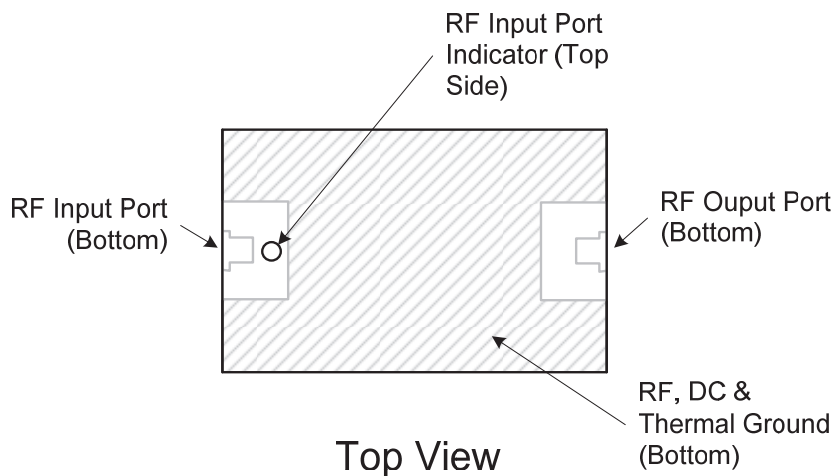
Limiter Schematic – LM202402-Q-E-301



Limiter Schematic – LM202402-Q-F-301



Pinout



Absolute Maximum Ratings

@ $Z_0 = 50 \Omega$, $T_A = +25^\circ\text{C}$, as measured in Aeroflex evaluation board (Unless Otherwise Defined)

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		- 65 °C to 150 °C
Storage Temperature		- 65 °C to 150 °C
Junction Temperature		175 °C
RF CW Incident Power	$T_{\text{case}} = 85^\circ\text{C}$, source and load VSWR < 1.2:1, derate linearly to 0 W at $T_{\text{case}} = 150^\circ\text{C}$ (note 1)	50 dBm
RF Peak Incident Power	$T_{\text{case}} = 85^\circ\text{C}$, source and load VSWR < 1.2:1, RF pulse width = 25 μs , duty cycle = 5%, derate linearly to 0 W at $T_{\text{case}} = 150^\circ\text{C}$ (note 1)	60 dBm
Θ_{jc} Thermal Resistance	Junction to bottom surface of package	40 °C/W
Assembly Temperature	t = 10 seconds	260 °C

Notes:

1. T_{case} is defined as the temperature of the bottom surface of the package.

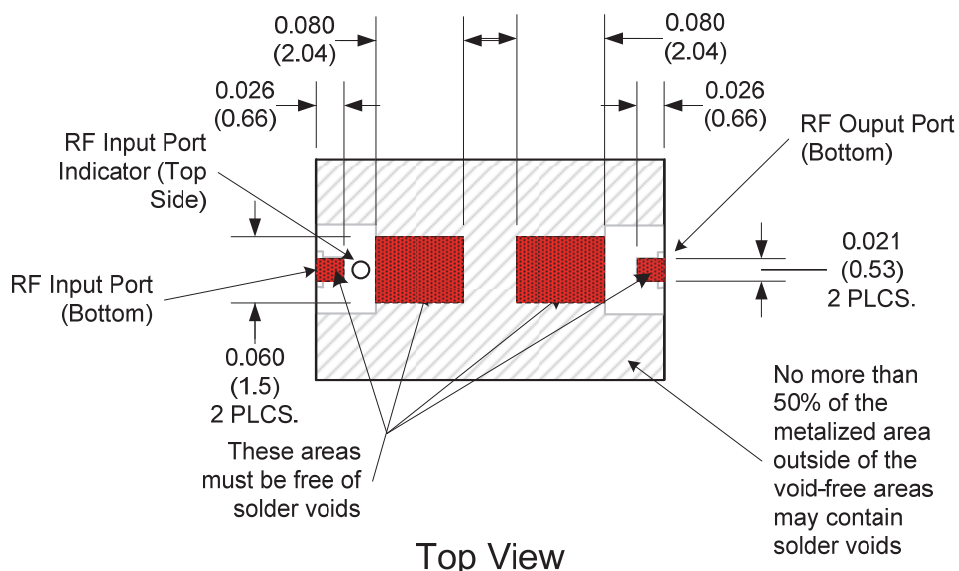
LM202402-Q-E-301 & LM202402-Q-F-301 Electrical Specification

@ $Z_0 = 50 \Omega$, $T_A = +25^\circ\text{C}$, as measured in Aeroflex evaluation board (Unless Otherwise Defined)

Parameter	Symbol	Test Conditions	Minimum Value	Typical Value	Maximum Value	Units
Frequency	F		2	- - -	4	GHz
Insertion Loss	IL	2 GHz \leq F \leq 4 GHz, Pin = -10 dBm		0.5	0.7	dB
Return Loss	RL	2 GHz \leq F \leq 4 GHz, Pin = -10 dBm	12	14		dB
Input 1 dB Compression Point	IP _{1dB}	2 GHz \leq F \leq 4 GHz	0	5	8	dBm
2nd Harmonic	2F ₀	Pin = -10 dBm, F ₀ = 3.0 GHz		-40	-30	dBc
Peak Incident Power	Pinc(Pk)	RF Pulse Width = 25 μs , duty cycle = 1%, $t_{\text{rise}} \leq 3 \mu\text{s}$, $t_{\text{fall}} \leq 3 \mu\text{s}$			60	dBm
CW Incident Power	Pinc(CW)	2 GHz \leq F \leq 4 GHz			50	dBm
Flat Leakage Power	FL	60 dBm, RF pulse width = 25 μs , duty cycle = 0.01, $t_{\text{rise}} \leq 3 \mu\text{s}$, $t_{\text{fall}} \leq 3 \mu\text{s}$		13	14	dBm
Spike Leakage Energy	SL	Pin = 60 dBm peak, RF pulse width = 25 μs , duty cycle = 0.01		0.5	0.7	erg
Recovery Time	T _R	50% falling edge of RF pulse to 1 dB IL, Pin = 60 dBm peak, RF pulse width = 25 μs , duty cycle = 1%, $t_{\text{rise}} \leq 3 \mu\text{s}$, $t_{\text{fall}} \leq 3 \mu\text{s}$		3	5	μs

Criteria for Proper Mounting on PCB

When a large signal is incident upon the input of the LM202402-Q-E-301 or the LM202402-Q-F-301, the impedance of the coarse limiter diodes is forced to a low value by the charge which is injected into these diodes by the combination of the current from the internal detector stage and the large RF voltage initially present across these diodes. As the impedance of these diodes decreases, an increasingly large impedance mismatch with the impedance of the transmission line to which the limiter is connected is created. Ultimately, the impedance of the coarse limiter diodes is reduced to a few ohms. This mismatch creates a standing wave, with a current maximum and voltage minimum located at the position of the coarse limiter diodes. While the large majority of the input signal power is reflected back to its source due to the impedance mismatch, the significant RF current that flows at the current maximum causes Joule heating to occur in the coarse limiter diodes, so in order to maintain the junction temperature of these diodes below their maximum rated value, there must be a path with minimal thermal resistance from the coarse diodes to the external system heat sink. Also, there must be a minimal electrical resistance and inductance between the underside of the limiter module package and the system ground in order to achieve maximum RF isolation between the input and the output of the limiter module.



Dimensions in inches mm

For these reasons, it is imperative that there are no voids in the electrical and thermal paths directly under the coarse limiter diodes. Care must be taken when mounting the LM202402-Q-E-301 and LM202402-Q-F-301 to avoid voids in the solder joint in the area along the lengthwise axis of the package, under and between the filled vias in the AlN substrate of the module, which are shown in the diagram (above). It is also important to ensure no solder voids exist between the limiter module RF ports and the PCB to which the limiter module is attached.

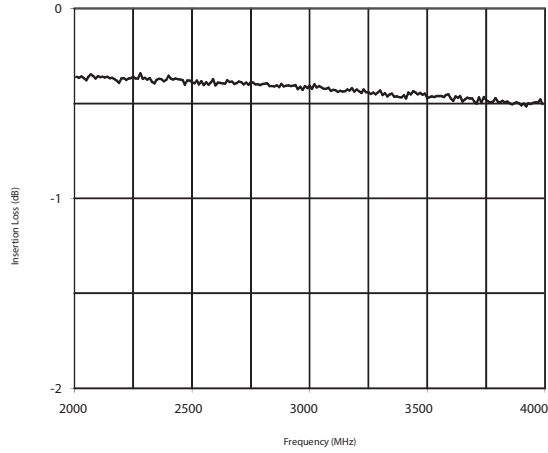
No greater than 50% of the remaining metalized area on the bottom of the package may contain solder voids.

PIN Diode Limiter

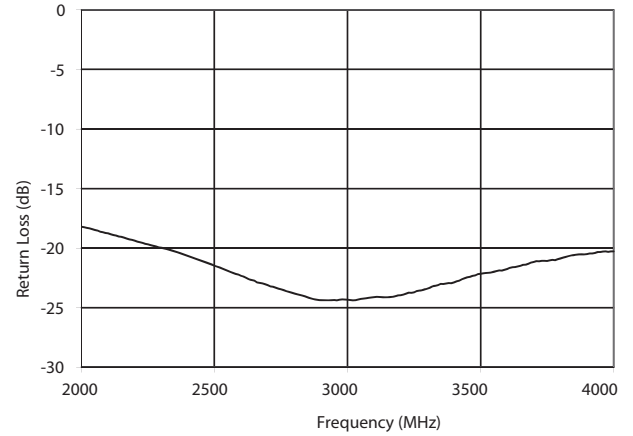


LM202402-Q-E-301 & LM202402-Q-F-301 Electrical Specification

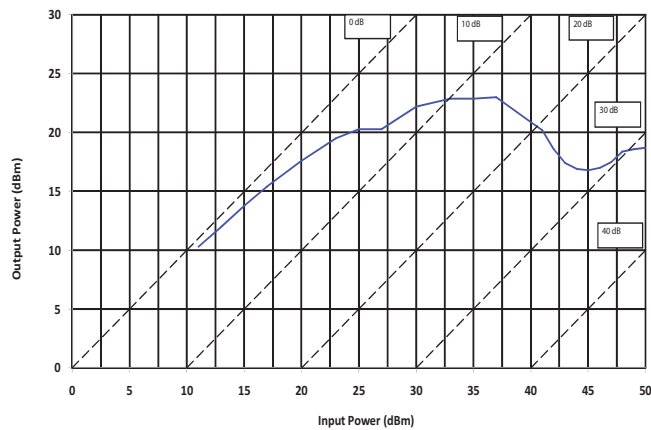
@ $Z_0 = 50 \Omega$, $T_A = +25^\circ\text{C}$, $P_{in} = 10 \text{ dBm}$, as measured in Aeroflex evaluation board (Unless Otherwise Defined)



Insertion Loss vs. Frequency

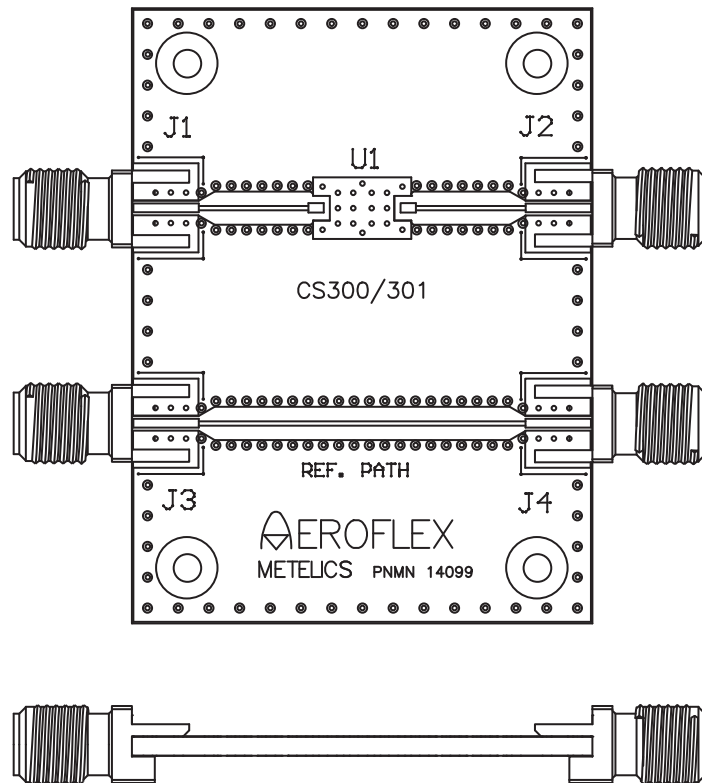


Return Loss vs. Frequency



CW Output Power vs. CW Input Power

Evaluation Board



The evaluation board for the LM202402-Q-E-301 and LM202402-Q-F-301 limiters is shown above. This evaluation board comprises two sections: the evaluation circuit for the limiter module; and, a reference transmission line.

The limiter module is mounted in position U1. Its RF input is connected to J1 and its output port is connected to J2, via two 50 Ω microstrip transmission lines.

The reference path 50 Ω microstrip transmission line structure can be utilized to determine the insertion loss of the transmission line structures connected between J1 and the limiter module input, as well as between the limiter module output and J2, so that their respective insertion losses may be subtracted from the total insertion loss measured between J1 and J2. This enables the resolution of the insertion loss of the limiter module only.

The evaluation board is supplied mounted on a heat sink. The maximum RF input power specified in the Absolute Maximum Ratings table must not be exceeded.

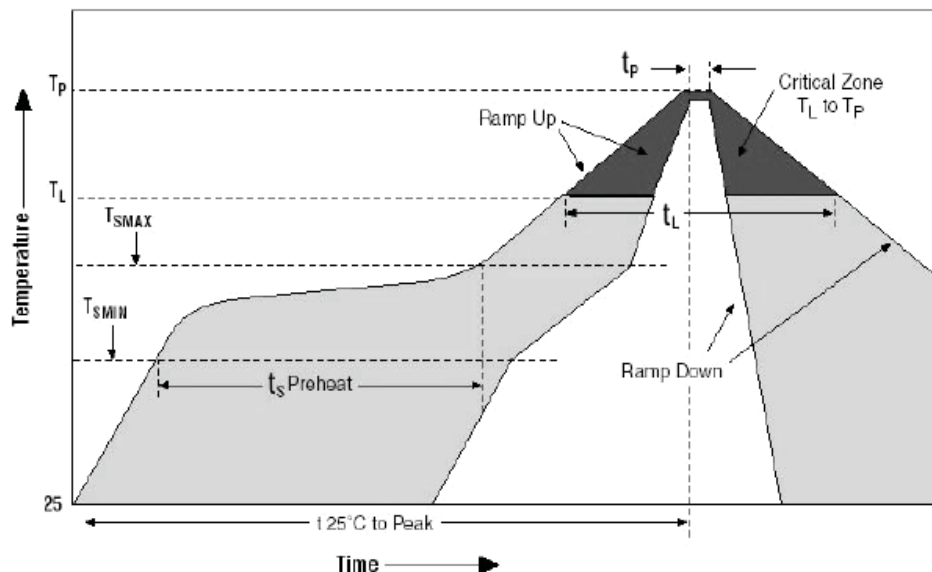
Assembly Instructions

The LM102202-Q-C-301 limiter is capable of being placed onto a circuit board by pick-and-place manufacturing equipment from tube or tape-reel dispensing. The device is attached to the circuit board using conventional solder re-flow or wave soldering procedures with RoHS type or Sn60/Pb40 type solders per the recommended time-temperature profile shown below.

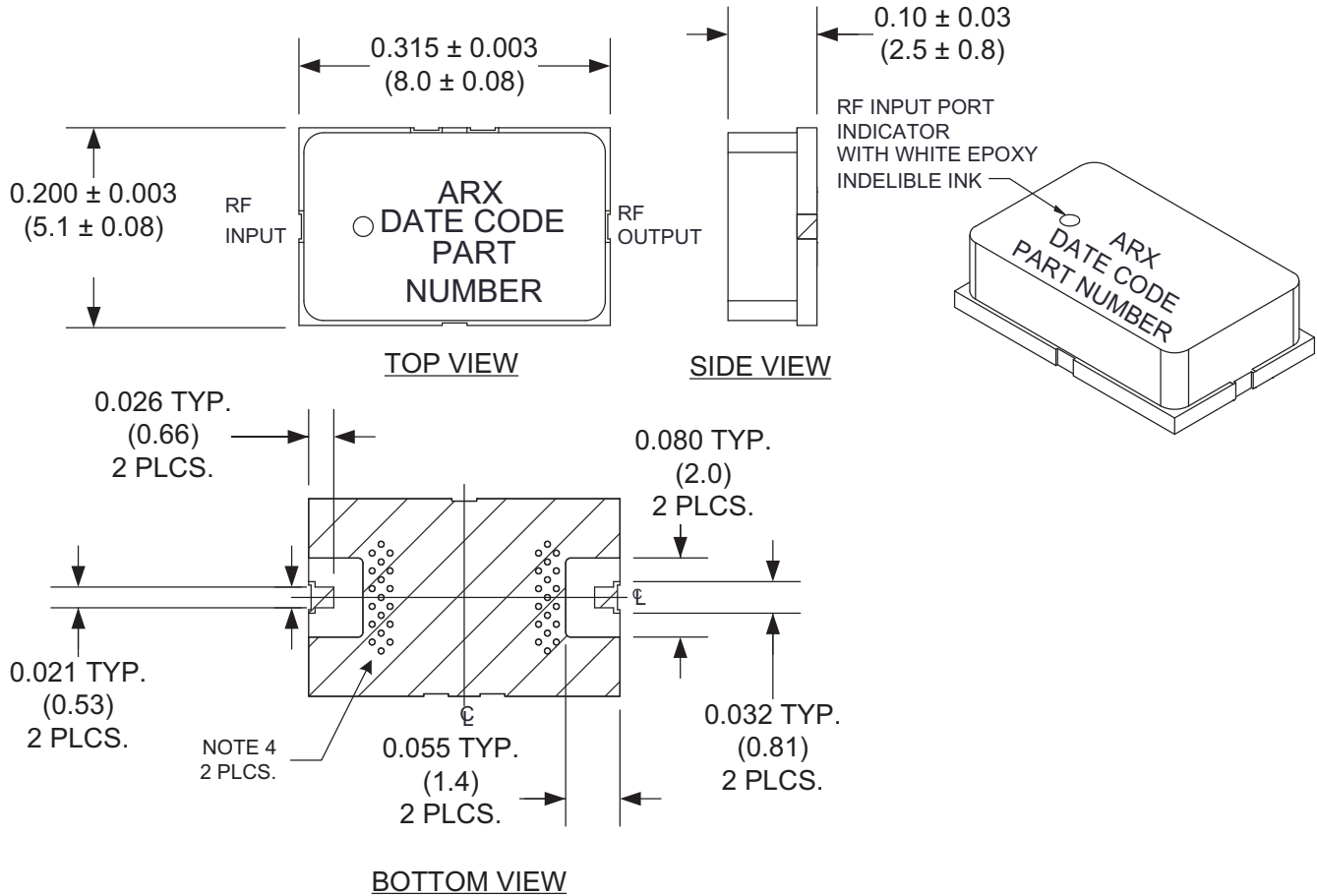
Time-Temperature Profile for Sn 60 / Pb 40 or RoHS Type Solders

Profile Feature	Sn-Pb Solder Assembly	Pb-Free Solder Assembly
Average ramp-up rate (T_L to T_P)	3°C/second maximum	3°C/second maximum
Preheat <ul style="list-style-type: none"> - Temperature Minimum (T_{SMIN}) - Temperature Maximum (T_{SMAX}) - Time (Minimum to maximum) (t_s) 	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
T_{SMAX} to T_L <ul style="list-style-type: none"> - Ramp-up Rate 		3°C/second maximum
Time Maintained above: <ul style="list-style-type: none"> - Temperature (T_L) - Time (t_L) 	183°C 60-150 seconds	217°C 60-150 seconds
Peak Temperature (T_P)	225 +0 / -5°C	260 +0/-5°C
Time within 5°C of actual Peak Temperature (T_P)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second maximum	6°C/second maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Solder Re-Flow Time-Temperature Profile



Outline Drawing, Case Style 301, (CS301)

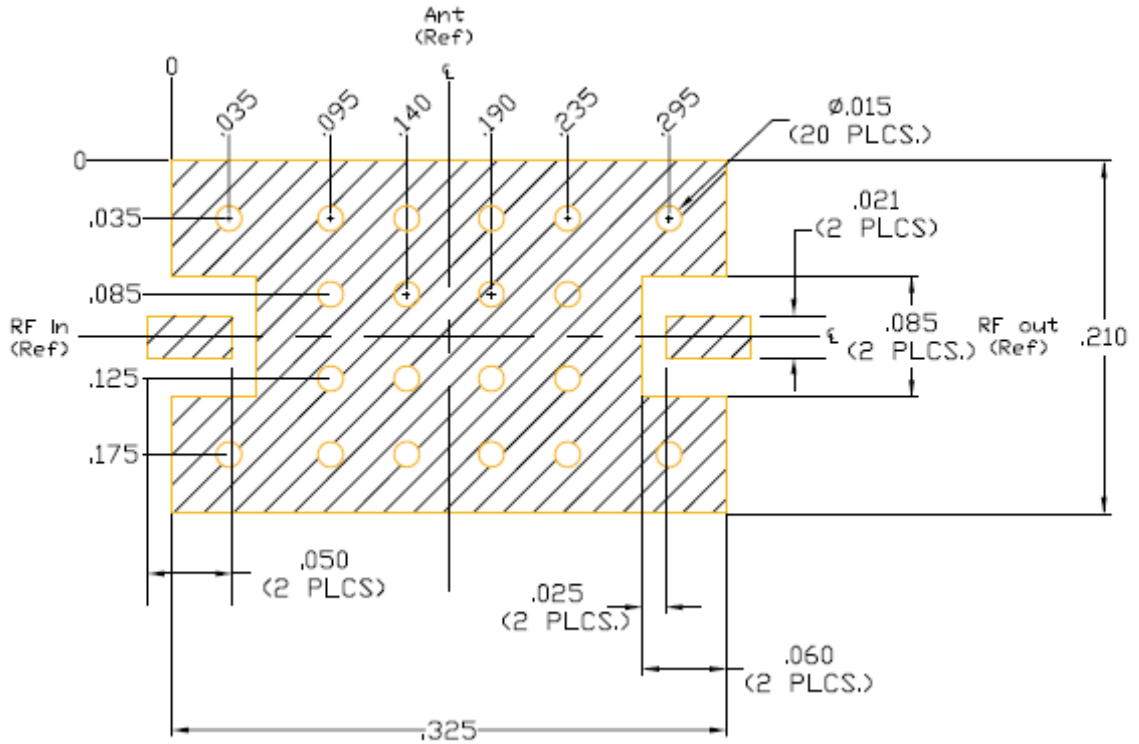


Notes:

1. Substrate material: 20 mil thick aluminum nitride (AlN).
2. RF cover: black ceramic
3. Top side and back side metalization: 0.5 μ m typical plated Au over Ti-Pd.
4. Locations and numbers of plated through vias are for reference only.
5. Dimensions in parentheses are in (mm).

PIN Diode Limiter

Recommended PCB Footprint for Case Style 301 (CS 301)



Notes:

1. Recommended PCB material is Rogers 4350, 10 mils THK.
2. Hatched area is RF, DC, and thermal ground. Vias should be solid copper filled and gold plated for optimum heat transfer from backside of limiter module through circuit vias to thermal ground.

Part Number Ordering Information:

Part Number	Packaging
LM202402-Q-E-301-T	Tube Packaging
LM202402-Q-E-301-R	Tape-Reel Packaging (Quantities of 250 or 500)
LM202402-Q-E-301-W	Waffle Packaging
LM202402-Q-E-301-E	RF Evaluation Board with Heat Sink
LM202402-Q-F-301-T	Tube Packaging
LM202402-Q-F-301-R	Tape-Reel Packaging (Quantities of 250 or 500)
LM202402-Q-F-301-W	Waffle Packaging
LM202402-Q-F-301-E	RF Evaluation Board with Heat Sink

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