

UT54ACTQ16245

RadHard CMOS 16-bit Bidirectional Transceiver, TTL Inputs, and Three-State Outputs
Datashheet

May 16, 2012

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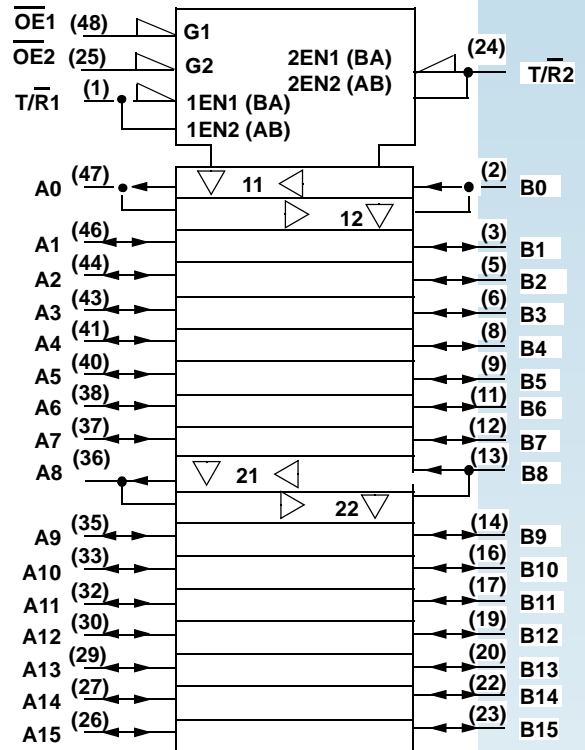
FEATURES

- ❑ 16 non-inverting bidirectional buffers with three-state outputs
- ❑ Guaranteed simultaneously switching noise level and dynamic threshold performance
- ❑ Separate control logic for each byte
- ❑ 0.6µm Commercial RadHard™ CMOS
 - Total dose: 100K rad(Si)
 - Single Event Latchup immune
- ❑ High speed, low power consumption
- ❑ Output source/sink 24mA
- ❑ Standard Microcircuit Drawing 5962-06244
 - QML compliant part
- ❑ Package:
 - 48-lead flatpack, 25 mil pitch (.390 x .640)

DESCRIPTION

The 16-bit wide UT54ACTQ16245 transceiver is built using Aeroflex's Commercial RadHard™ epitaxial CMOS technology and is ideal for space applications. This high speed, low power UT54ACTQ16245 transceiver is designed to perform asynchronous two-way communication and signal buffering. Balanced outputs and low "on" output impedance make the UT54ACTQ16245 well suited for driving high capacitance loads and low impedance backplanes. The Transmit/Receive input (T/\bar{R}) controls the direction of data flow through the device. The output enable input (\overline{OEn} , active low) overrides the direction control (T/\bar{R}) and disables both the A and B ports by placing them in a high impedance state. These signals can be driven from either port A or B. The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver

LOGIC SYMBOL



PIN DESCRIPTION

Pin Names	Description
\overline{OEn}	Output Enable Input (Active Low)
$T/\bar{R}n$	Direction Control Inputs
A0-A15	Side A Inputs or 3-State Outputs
B0-B15	Side B Inputs or 3-State Outputs

FUNCTION TABLE

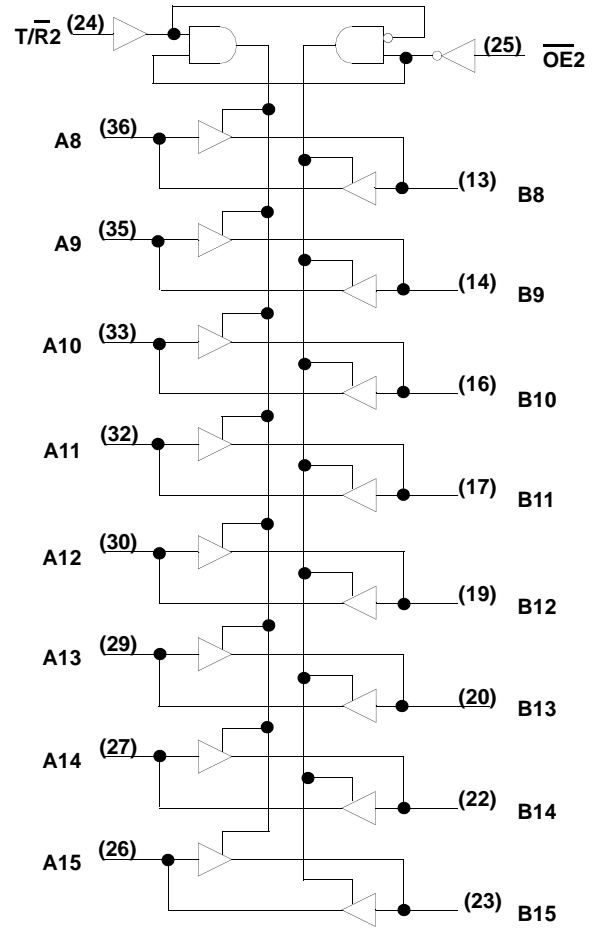
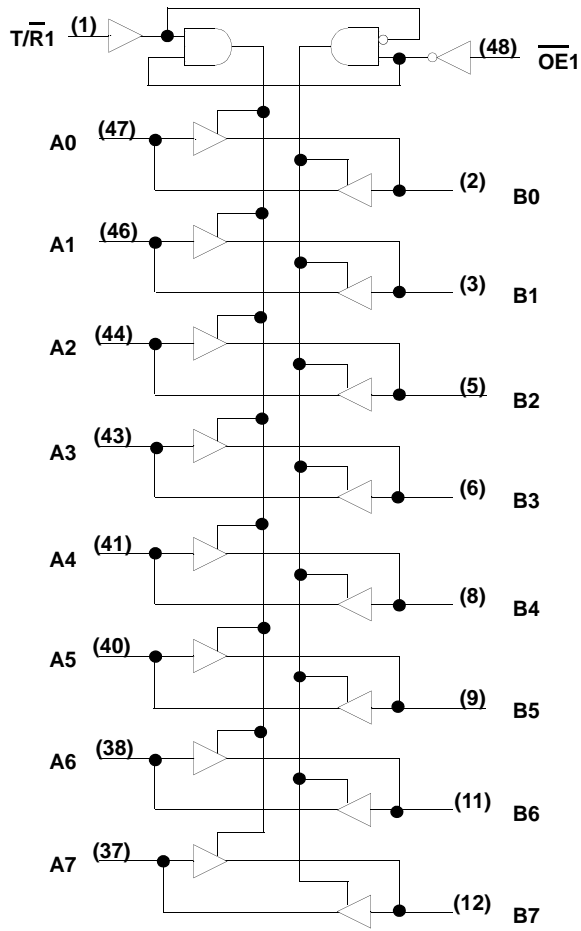
ENABLE \overline{OEn}	DIRECTION $T/\bar{R}n$	OPERATION
L	L	B Data To A Bus
L	H	A Data To B Bus
H	X	Isolation, High-Z State on Bus A and Bus B

PINOUTS

48-Lead Flatpack Top View

$\overline{T/R1}$	1	48	$\overline{OE1}$
B0	2	47	A0
B1	3	46	A1
V _{SS}	4	45	V _{SS}
B2	5	44	A2
B3	6	43	A3
V _{DD}	7	42	V _{DD}
B4	8	41	A4
B5	9	40	A5
V _{SS}	10	39	V _{SS}
B6	11	38	A6
B7	12	37	A7
B8	13	36	A8
B9	14	35	A9
V _{SS}	15	34	V _{SS}
B10	16	33	A10
B11	17	32	A11
V _{DD}	18	31	V _{DD}
B12	19	30	A12
B13	20	29	A13
V _{SS}	21	28	V _{SS}
B14	22	27	A14
B15	23	26	A15
$\overline{T/R2}$	24	25	$\overline{OE2}$

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS ¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E5	rad(Si)
SEL Latchup	>108	MeV-cm ² /mg
SEU Onset Let	N/A ³	MeV-cm ² /mg
Neutron Fluence ²	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits $V_{DD} = 5.5V$, $T = 125^{\circ}C$.
2. Not tested, inherent of CMOS technology.
3. This device contains no memory storage elements which can be upset.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	LIMIT (Mil only)	UNITS
$V_{I/O}$	Voltage any pin during operation	-3 to $V_{DD} + 3$	V
V_{DD}	Supply voltage	-0.3 to 6.0	V
T_{STG}	Storage Temperature range	-65 to +150	$^{\circ}C$
T_J	Maximum junction temperature	+175	$^{\circ}C$
Θ_{JC}	Thermal resistance junction to case	20	$^{\circ}C/W$
I_I	DC input current	± 10	mA
P_D	Maximum power dissipation	310	mW

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to +125	$^{\circ}C$
t_{INRISE} t_{INFALL}	Maximum input rise or fall time (V_{IN} transitioning between V_{IL} (max) and V_{IH} (min))	20	ns

DC ELECTRICAL CHARACTERISTICS ¹

(-55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V _{IL}	Low level input voltage ²	V _{DD} from 4.5V to 5.5V			0.8	V
V _{IH}	High level input voltage ²	V _{DD} from 4.5 V to 5.5V		2.0		V
I _{IN}	Input leakage current	V _{DD} from 4.5V to 5.5V V _{IN} = V _{DD} or V _{SS}		-1	1	μA
I _{OZ}	Three-state output leakage current	V _{DD} from 4.5V to 5.5V V _{IN} = V _{DD} or V _{SS}		-10	10	μA
I _{OS}	Short-circuit output current ^{3,4}	V _O = V _{DD} or V _{SS} V _{DD} from 4.5V to 5.5V		-600	600	mA
V _{OL1}	Low-level output voltage ⁵	I _{OL} = 24mA I _{OL} = 24mA I _{OL} = 100μA V _{IN} = 2.0V or 0.8V V _{DD} = 4.5V to 5.5V	-55°C, 25°C		0.35	V
			+125°C		0.5	
					0.2	
V _{OL2}	Low-level output voltage ^{5,6}	I _{OL} = 50 mA V _{IN} = 2.0V or 0.8V V _{DD} = 5.5V	-55°C, 25°C		0.8	V
			+125°C		1.0	
V _{OH1}	High-level output voltage ⁵	I _{OH} = -24 mA I _{OL} = -24mA I _{OH} = -100μA V _{IN} = 2.0V or 0.8V V _{DD} = 4.5V to 5.5V	-55°C, 25°C	V _{DD} - 0.64		V
			+125°C	V _{DD} - 0.8		
				V _{DD} - 0.2		
V _{OH2}	High-level output voltage ^{5, 6}	I _{OH} = -50 mA V _{IN} = 2.0V or 0.8V V _{DD} = 5.5V	-55°C, 25°C	V _{DD} - 1.1		V
			+125°C	V _{DD} - 1.3		
V _{IC+}	Positive input clamp voltage	For input under test, I _{IN} = 18mA V _{DD} = 0.0V		0.4	1.5	V
V _{IC-}	Negative input clamp voltage	For input under test, I _{IN} = -18mA V _{DD} = open		-1.5	-0.4	V
P _{total}	Power dissipation ^{7, 8, 9}	C _L = 20pF V _{DD} from 4.5V to 5.5V			1.5	mW/MHz

I_{DDQ}	Standby Supply Current V_{DD} Pre-Rad 25°C Pre-Rad -55°C to +125°C Post-Rad 25°C	$V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 5.5V$ $\overline{OEn} = V_{DD}$ $\overline{OEn} = V_{DD}$ $\overline{OEn} = V_{DD}$		10 160 160	μA
ΔI_{DDQ}	Quiescent Supply Current Delta, TTL input level	For input under test $V_{IN} = V_{DD} - 2.1V$ For other inputs $V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 5.5V$		1.6	mA
C_{IN}	Input capacitance ¹⁰	$f = 1MHz @ 0V$ V_{DD} from 4.5V to 5.5V		15	pF
C_{OUT}	Output capacitance ¹⁰	$f = 1MHz @ 0V$ V_{DD} from 4.5V to 5.5V		15	pF
V_{OLP} V_{OLV}	Low level V_{SS} bounce noise ¹¹	$V_{IN} = 3.0V$, $V_{IL} = 0.0V$, $T_A = +25^\circ C$, $V_{DD} = 5.0V$		1200 -1500	mV mV
V_{OHP} V_{OHV}	High level V_{DD} bounce noise ¹¹	See figure "Quiet Output Under Test"		V_{OH} +1500 V_{OH} -1600	mV mV

Notes:

1. All specifications valid for radiation dose $\leq 1E5$ rad(Si) per MIL-STD-883, Method 1019.
2. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(\min) + 20\%$, $- 0\%$; $V_{IL} = V_{IL}(\max) + 0\%$, $- 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(\min)$ and $V_{IL}(\max)$.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Supplied as a design limit, but not guaranteed or tested.
5. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
6. Transmission driving tests are performed at $V_{DD} = 5.5V$, only one output loaded at a time with a duration not to exceed 2ms. The test is guaranteed, if not tested, for $V_{IN} = V_{IH}$ minimum or V_{IL} maximum.
7. Guaranteed by characterization.
8. Power does not include power contribution of any CMOS output sink current.
9. Power dissipation specified per switching output.
10. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
11. This test is for qualification only. V_{SS} and V_{DD} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture.

AC ELECTRICAL CHARACTERISTICS¹

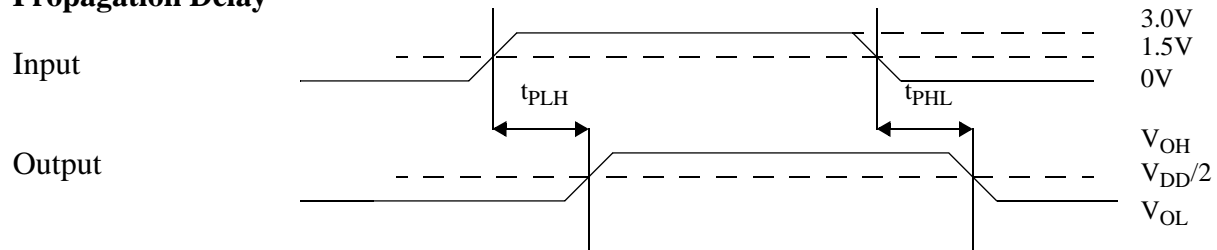
($V_{DD} = 5V \pm 10\%$, $-55^{\circ}C < T_C < +125^{\circ}C$)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
t_{PLH}	Propagation delay Data to Bus	$C_L = 40 \text{ pF}$ $R_L = 50\Omega$ See figure "Test Load"	3	8.5	ns
t_{PHL}	Propagation delay Data to Bus		3	8.5	ns
t_{PZL1}	Output enable time $\overline{OE}n$ to Bus		3	10	ns
t_{PZH1}	Output enable time $\overline{OE}n$ to Bus		3	10	ns
t_{PLZ1}	Output disable time $\overline{OE}n$ to Bus high impedance		2.5	9.5	ns
t_{PHZ1}	Output disable time $\overline{OE}n$ to Bus high impedance		2.5	9.5	ns
t_{PZL2}^2	Output enable time $T/\overline{R}n$ to Bus		2.5	13	ns
t_{PZH2}^2	Output enable time $T/\overline{R}n$ to Bus		2.5	13	ns
t_{PLZ2}^2	Output disable time $T/\overline{R}n$ to Bus high impedance		1.5	15	ns
t_{PHZ2}^2	Output disable time $T/\overline{R}n$ to Bus high impedance		1.5	15	ns
t_{SKEW}^3	Skew between outputs		-	1.0	ns
t_{DSKEW}^4	Differential skew between outputs		-	1.25	ns
$t_{SKEWPP}^{3,5}$	Part-to-Part output skew			500	ps

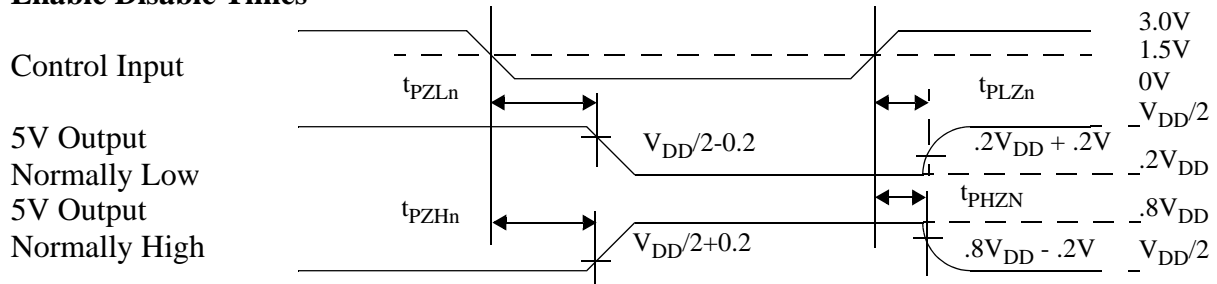
Notes:

1. All specifications valid for radiation dose $\leq 1E5 \text{ rad(Si)}$ per MIL-STD-883, Method 1019.
2. $T/\overline{R}n$ to bus times are guaranteed by design, but not tested. $\overline{OE}x$ to bus times are tested
3. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs low-to-high.
4. Differential skew is defined as a comparison of any two output transitions high-to-low vs. low-to-high and low-to-high vs high-to low.
5. Guaranteed by characterization, but not tested.

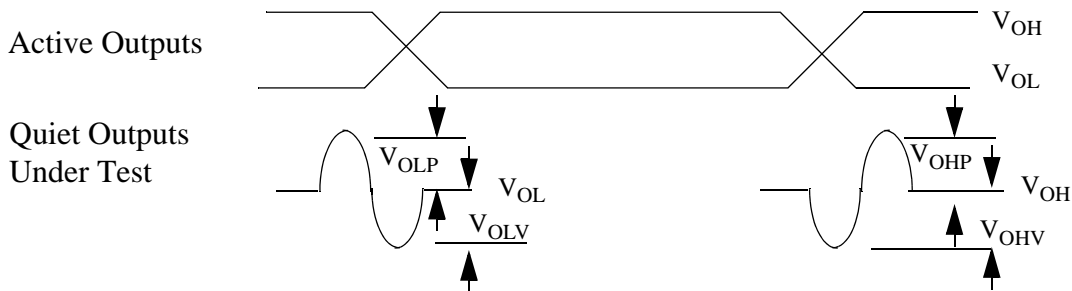
Propagation Delay



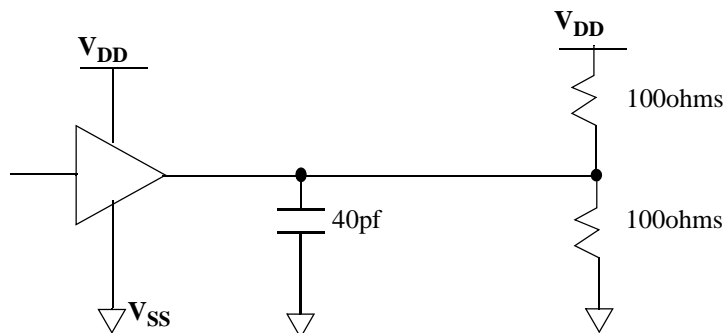
Enable Disable Times



Bounce Noise



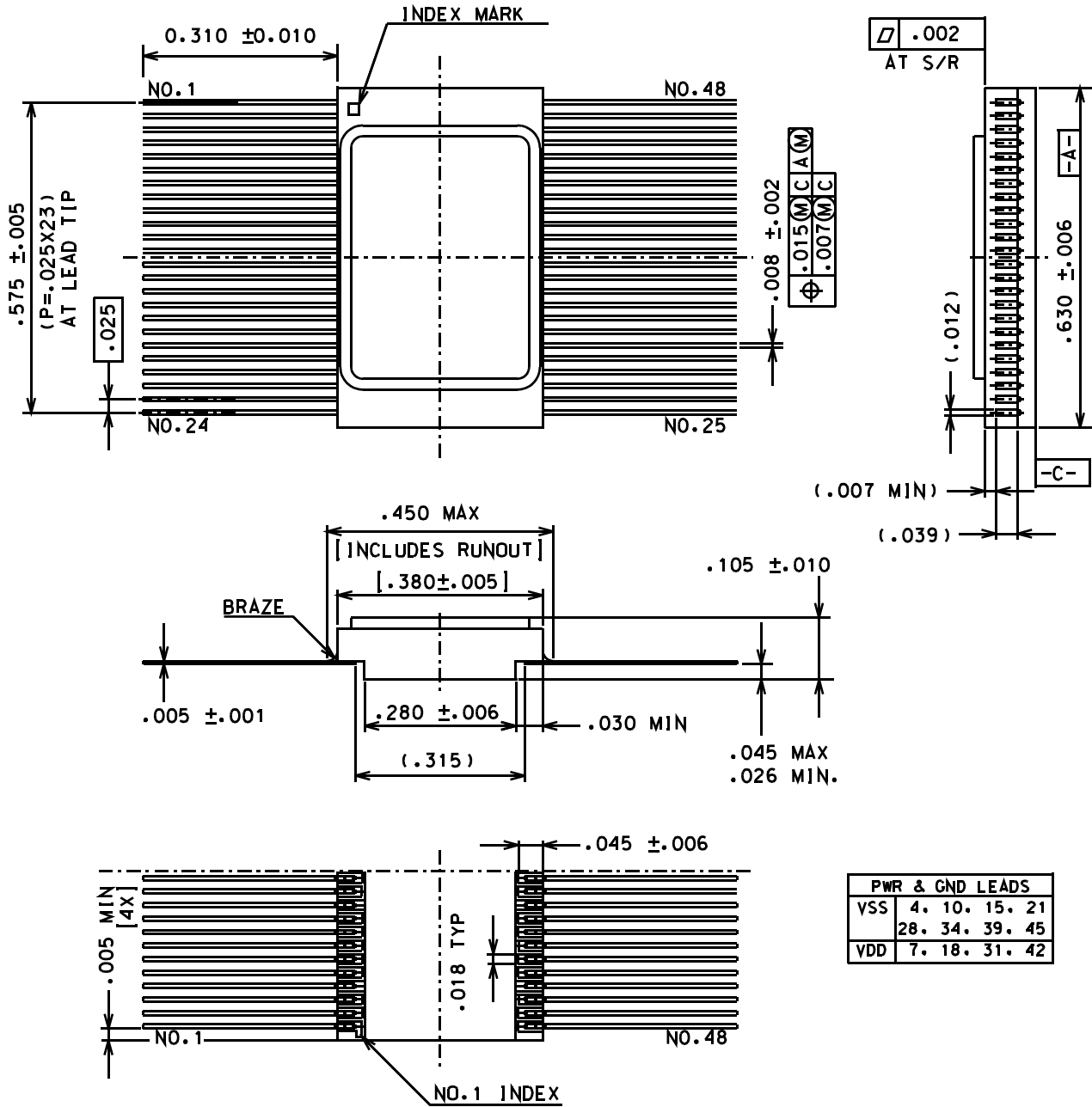
Test Load or Equivalent¹



Notes

1. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

PACKAGE



PWR & GND LEADS	
VSS	4, 10, 15, 21 28, 34, 39, 45
VDD	7, 18, 31, 42

NOTE:

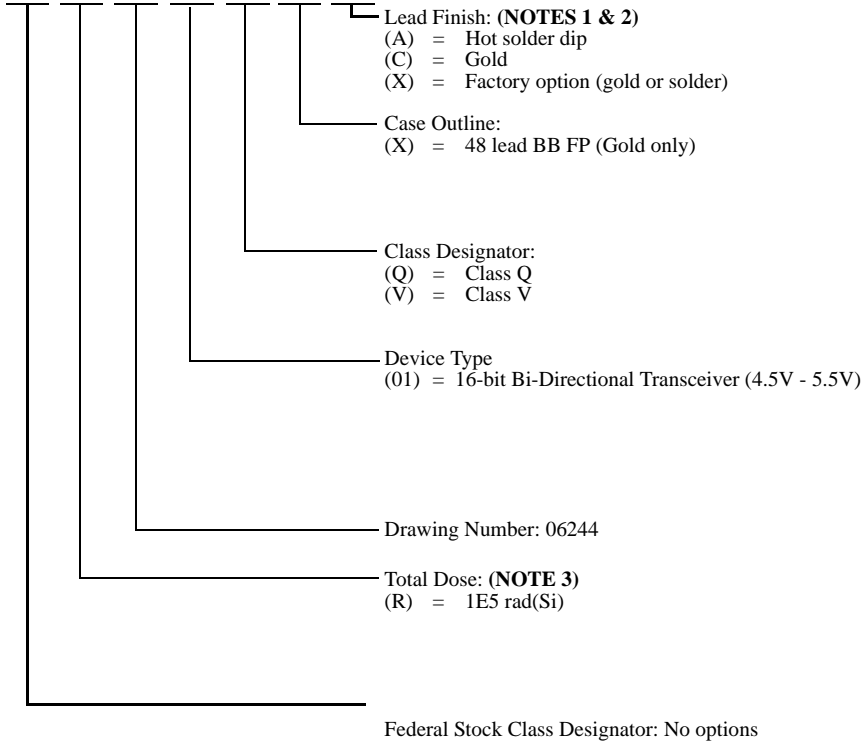
1. Seal ring is connected to V_{SS} .
2. Units are in inches.
3. All exposed metalized areas must be gold plated 100 to 225 microinches thick. Dyer electroplated nickel undercoating 100 to 350 microinches per MIL-PRF-38535.

Figure 1. 48-Lead Flatpack

ORDERING INFORMATION

UT54ACTQ16245: SMD

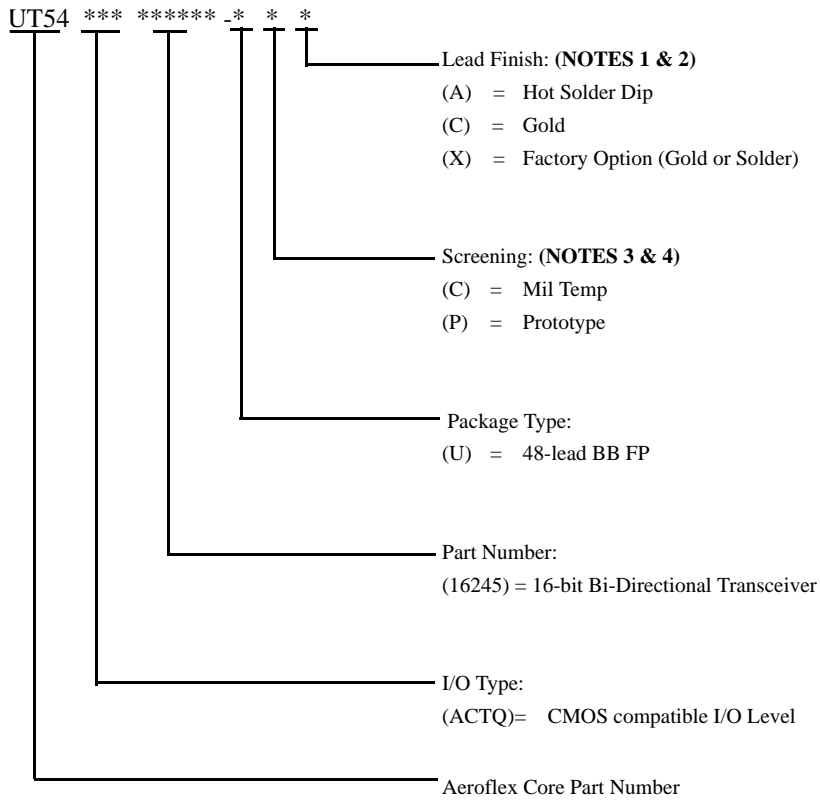
5962 R 06244 ** * * *



Notes:

- 1. Lead finish (A,C, or X) must be specified.
- 2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- 3.Total dose radiation must be specified when ordering. QML Q not available without radiation hardening.

UT54ACTQ16245



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Manufacturing Flows Document. Tested at 25°C only. Lead finish is Gold "C" only. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Aeroflex Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

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Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused