Standard Products

UT54LVDM328 Octal 400 Mbps Bus LVDS Repeater

Data Sheet

December 2008

FEATURES

- 400.0 Mbps low jitter fully differential data path
- 200MHz clock channel
- 3.3 V power supply
- 10mA LVDS output drivers
- Cold sparing all pins
- Fast propagation delay of 3.5ns max
- Receiver input threshold < ± 100 mV
- Operational environment; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300 krad(Si) and 1 Mrad(Si)
  - Latchup immune (LET > 100 MeV-cm^2/mg)
- Packaging options:
  - 48-lead flatpack
- Standard Microcircuit Drawing 5962-01536
  - QML Q and V compliant part

INTRODUCTION

The UT54LVDM328 is an Octal Bus Repeater utilizing Low Voltage Differential Signaling (LVDS) technology for low power, high speed operation. Data paths are fully differential from input to output for low noise generation and low pulse width distortion. LVDS I/O enable high speed data transmission for point-to point or multi-drop interconnects. This device is designed for use as a high speed differential repeater.

The UT54LVDM328 is a repeater designed specifically for the bridging of multiple backplanes in a system. The UT54LVDM328 utilizes low voltage differential signaling to deliver high speed while consuming minimal power with reduced EMI. The UT54LVDM328 repeats signals between backplanes and accepts or drives signals onto the local bus.

The individual LVDS outputs can be put into Tri-State by use of the enable pins.

All pins have Cold Spare buffers. These buffers will be high impedance when V_{DD} is tied to V_{SS}.

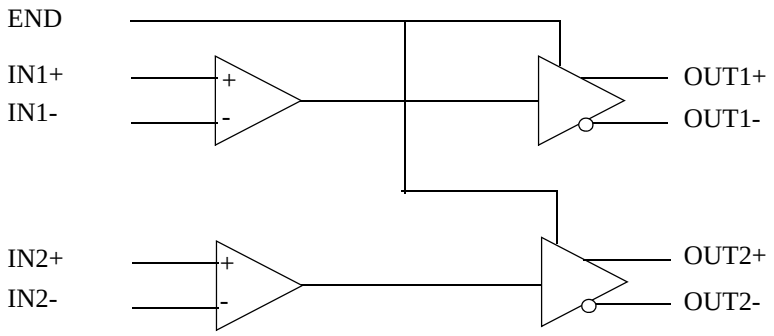

Figure 1a. UT54LVDM328 Repeater Block Diagram
(Partial - see Page 2 for complete diagram)

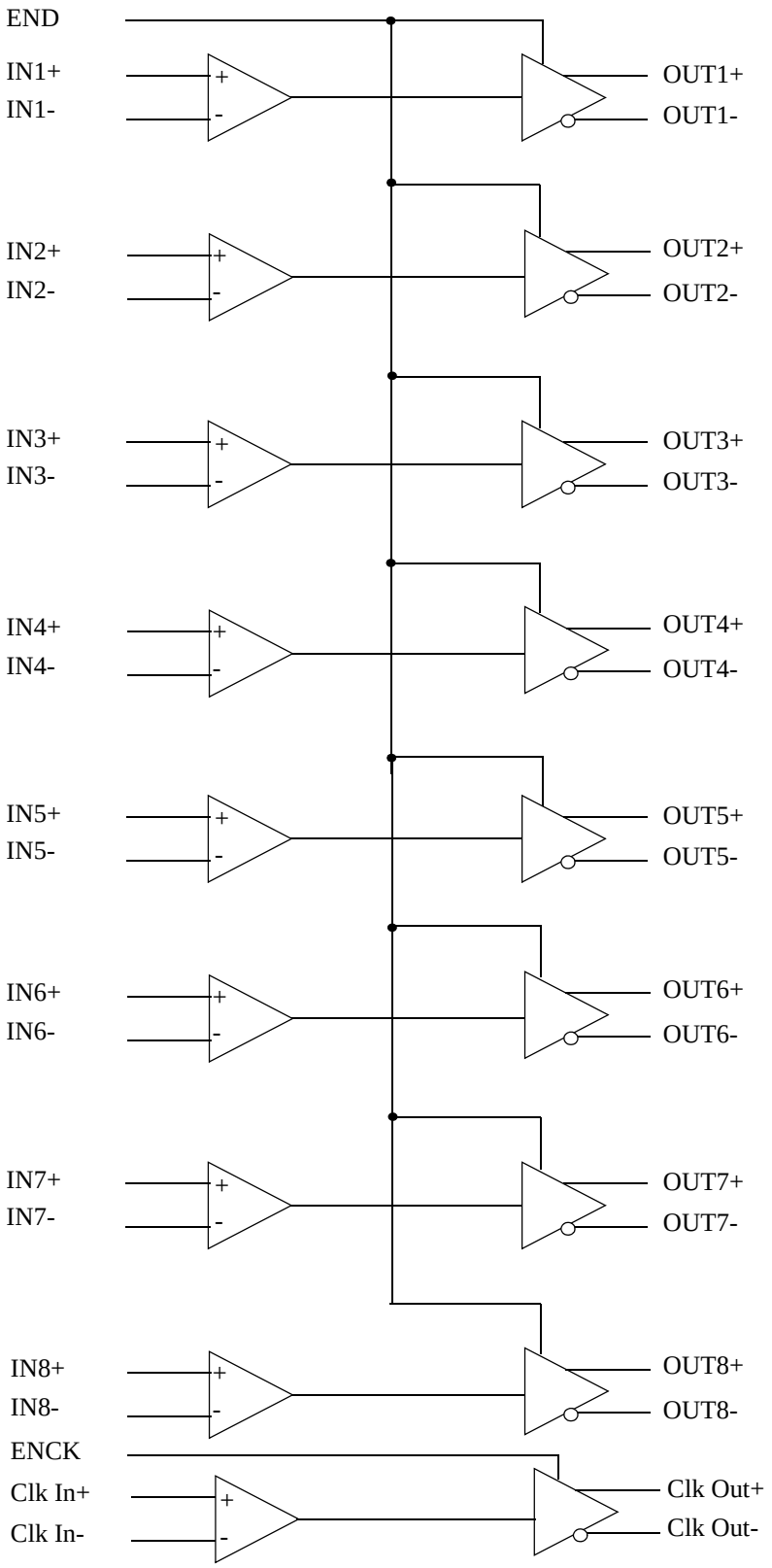

Figure 1b. UT54LVDM328 Repeater Diagram

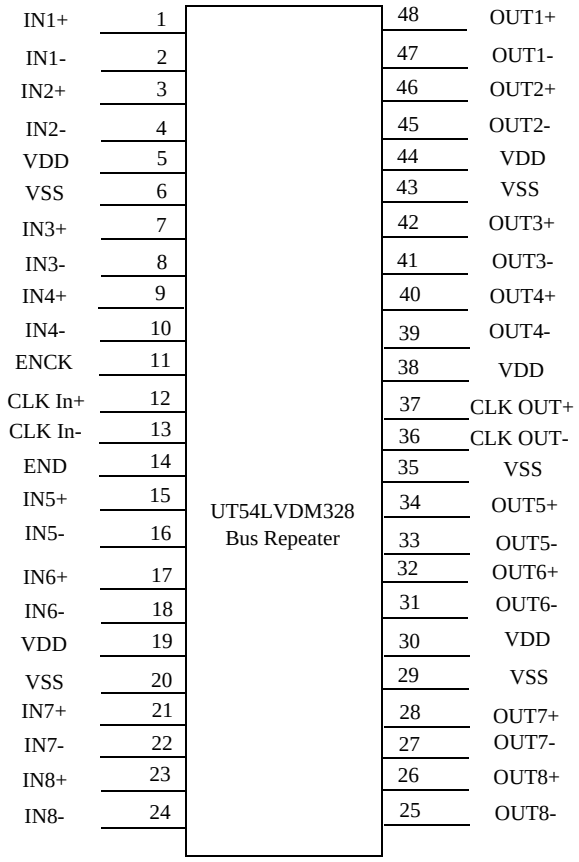

Figure 2. UT54LVDM328 Pinout

PIN DESCRIPTION

Name	# of Pins	Description
INn+	8	Non-inverting LVDS input
INn-	8	Inverting LVDS input
OUTn+	8	Non-inverting LVDS output
OUTn-	8	Inverting LVDS Output
END	1	A logic low on the enable puts the LVDS data output into Tri-State and reduces the supply current
ENCK	1	A logic low on the enable puts the LVDS clock output into Tri-State and reduces the supply current
V_{SS}	5	Ground
V_{DD}	5	Power supply
CLK IN+	1	Non-Inverting Clock LVDS Input
CLK IN-	1	Inverting clock LVDS Input
CLK OUT+	1	Non-Inverting Clock LVDS Output
CLK OUT-	1	Inverting Clock LVDS Output

APPLICATIONS INFORMATION

The UT54LVDM328 provides the basic bus repeater function. The device operates as a 9 channel LVDS buffer. Repeating the signal restores the LVDS amplitude, allowing it to drive another media segment. This allows for isolation of segments or long distance applications.

The intended application of these devices and signaling technique is for both point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.)

Input Fail-Safe:

The UT54LVDM328 also supports OPEN, shorted and terminated input fail-safe. Receiver output will be HIGH for all fail-safe conditions.

PCB layout and Power System Bypass:

Circuit board layout and stack-up for the UT54LVDM328 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01µF to 0.1µ F. Tantalum capacitors may be in the range of 2.2µF to 10µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the UT54LVDM328, as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance and extends the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation, as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity in signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

Compatibility with LVDS standard:

In backplane multidrop configurations, with closely spaced loads, the effective differential impedance of the line is reduced. If the mainline has been designed for 50Ω differential impedance, the loading effects may reduce this to the 35Ω range depending upon spacing and capacitance load. Terminating the line with a 35Ω load is a better match than with 50Ω and reflections are reduced.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 4.0V
$V_{I/O}$	Voltage on any pin	-0.3 to (V_{DD} + 0.3V)
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	800mW
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	22°C/W
I_I	DC input current	±10mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and life test.
3. Test per MIL-STD-883, Method 1012.
4. For cold spare mode ($V_{DD} = V_{SS}$), $V_{I/O}$ may be -0.3V to the maximum recommended operating V_{DD} +0.3V.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage, receiver inputs	0 to 2.4V
	DC input voltage, logic inputs	0 to V_{DD} for END or ENCK

DC ELECTRICAL CHARACTERISTICS [1]

(V_{DD} = 3.3V ± 0.3V; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
CMOS/TTL DC SPECIFICATIONS (EN)					
V_{IH}	High-level input voltage		2.0	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.8	V
I_{IH}	High-level input current	V_{IN}=3.6V; V_{DD} = 3.6V	-10	+10	µA
I_{IL}	Low-level input current	V_{IN}=0V; V_{DD} = 3.6V	-10	+10	µA
V_{CL}	Input clamp voltage	I_{CL}=-18mA		-1.5	V
I_{CS}	Cold Spare Leakage current	V_{IN}=3.6V, V_{DD}=V_{SS}	-20	+20	µA
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)					
V_{OD}	Differential Output Voltage	R_L= 35Ω (See Figure 9)	250	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states	R_L= 35Ω (See Figure 9)		35	mV
V_{OS}	Offset Voltage	R_L= 35Ω $V_{OS}=\frac{(V_{OH}+V_{OL})}{2}$	1.055	1.550	V
ΔV_{OS}	Change in V_{OS} between complimentary output states	R_L=35Ω		35	mV
I_{OZ}	Output Tri-State Current	Tri-State output, V_{DD} = 3.6V V_{OUT}=V_{DD} or GND		±10	µA
I_{CSOUT}	Cold Sparing Leakage Current	V_{OUT}=3.6V, V_{DD}=V_{SS}	-20	+20	µA
I_{OS} [2,3]	Output Short Circuit Current	V_{OUT}+ OR V_{OUT} = 0 V		-25	mA
LVDS RECEIVER DC SPECIFICATIONS (IN+, IN-)					
V_{TH} [3]	Differential Input High Threshold	V_{CM} = +1.2V		+100	mV
V_{TL} [3]	Differential Input Low Threshold	V_{CM} = +1.2V	-100		mV
V_{CMR}	Common Mode Voltage Range	V_{ID}=210mV	0.2	2.00	V
I_{IN}	Input Current	V_{IN} = +2.4V, V_{DD} = 3.6V	-10	+10	µA
		V_{IN} = 0V, V_{DD} = 3.6V	-10	+10	µA
I_{CSIN}	Cold Sparing Leakage Current	V_{IN}=3.6V, V_{DD}=V_{SS}	-20	+20	µA

DC ELECTRICAL CHARACTERISTICS [1] (CON"T)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
Supply Current					
I_{CCL}	Total Supply Current	R_L = 35Ω END, ENCK= $V_{DD,}$ V_{DD}= 3.6V		220	ma
ICCZ	Tri-State Supply Current	END, ENCK = $V_{SS,}$ V_{DD}= 3.6V		20	ma

Notes:
1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
2. Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
3. Guaranteed by characterization.

AC SWITCHING CHARACTERISTICS

(V_{DD} = +3.3V $\pm$ 0.3V, T_A = -55 °C to +125 °C)

SYMBOL	PARAMETER	Conditions	MIN	MAX	UNIT
t_{PHZ}[2]	Disable Time (Active to Tri-State) High to Z (See Figure 7)	R_L= 35Ω, C_L = 10pf		4.5	ns
t_{PLZ}[2]	Disable Time (Active to Tri-State) Low to Z (See Figure 7)	R_L= 35Ω, C_L = 10pf		4.5	ns
t_{PZH}[2]	Enable Time (Tri-State to Active) Z to High (See Figure 7)	R_L= 35Ω, C_L = 10pf		11.0	ns
t_{PZL}[2]	Enable Time (Tri-State to Active) Z to Low (See Figure 7)	R_L= 35Ω, C_L = 10pf		11.0	ns
t_{LHT}[1]	Output Low-to-High Transition Time, 20% to 80% (See Figures 4 and 5)	R_L= 35Ω, C_L = 10pf		600	ps
t_{HLT}[1]	Output High-to-Low Transition Time, 80% to 20% (See Figures 4 and 5)	R_L= 35Ω, C_L = 10pf		600	ps
t_{PLHD}	Propagation Low to High Delay (See Figures 4 and 6)	R_L= 35Ω, C_L = 10pf		3.5	ns
T_{PHLD}	Propagation High to Low Delay (See Figures 4 and 6)	R_L= 35Ω, C_L = 10pf		3.5	ns
T_{SKEW}	Differential Skew T_{PHLD} - T_{PLHD} (See Figures 4 and 6)			900	ps
T_{CCS}	Output Channel-to-Channel Skew (See Figures 4 and 6)			500	ps

Notes:
1. Guaranteed by design.
2. Guaranteed by characterization.

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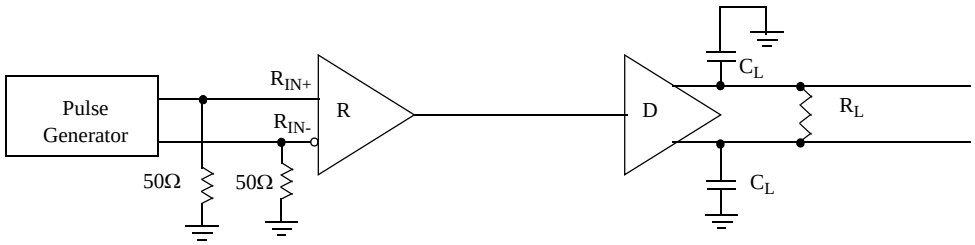


Figure 4. LVDS Output Load

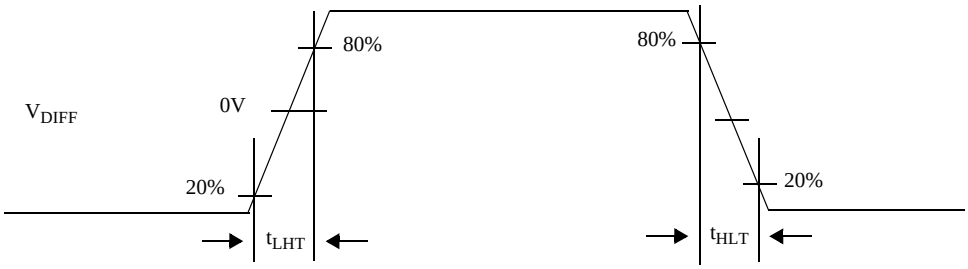


Figure 5. LVDS Output Transition Time

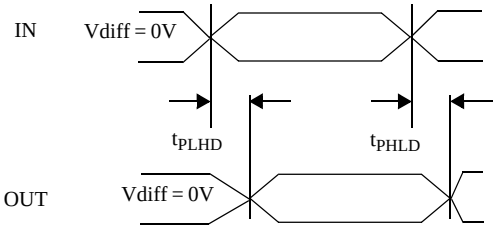


Figure 6. Propagation Delay Low-to-High and High-to-Low

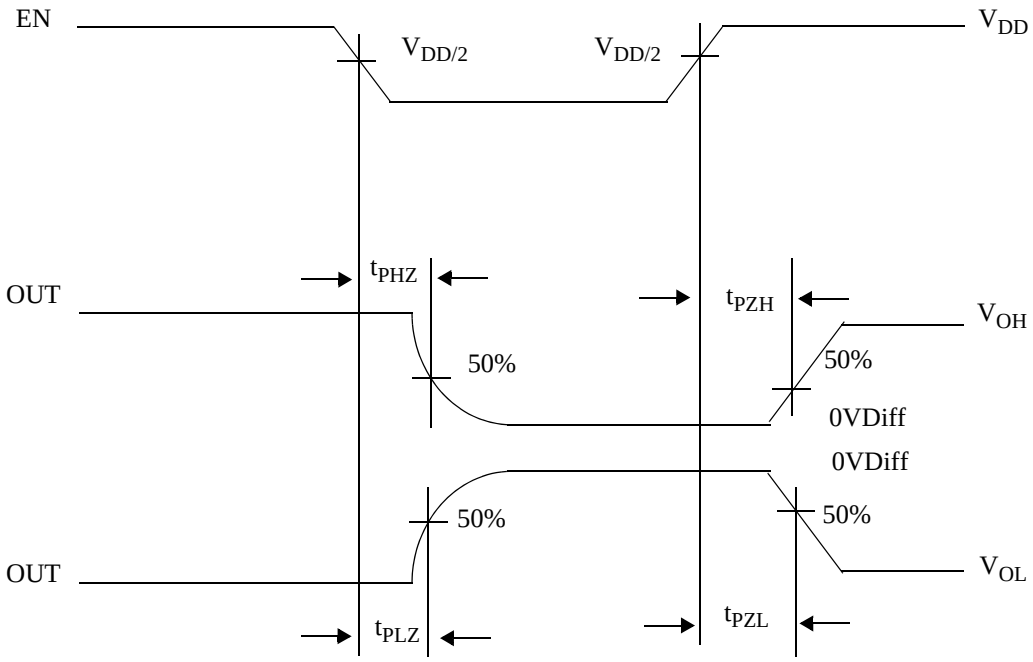


Figure 7. Output active to TRI-STATE and TRI-STATE to active

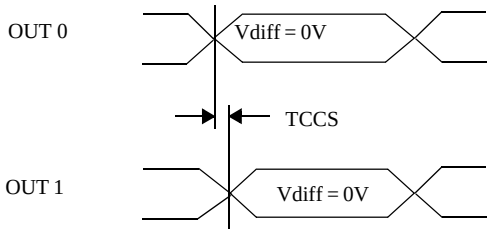


Figure 8. Output Channel-to-Channel Skew

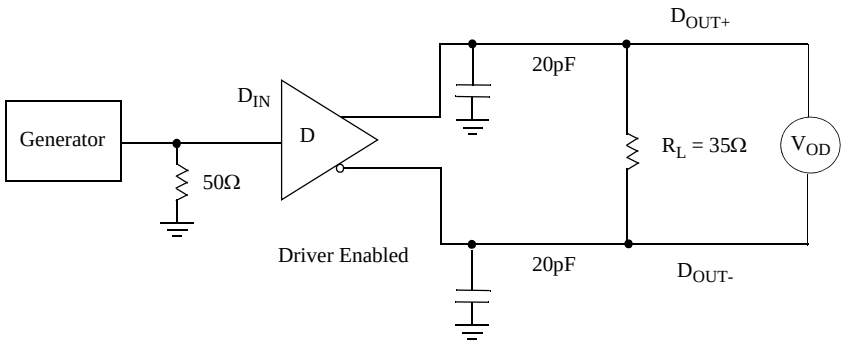
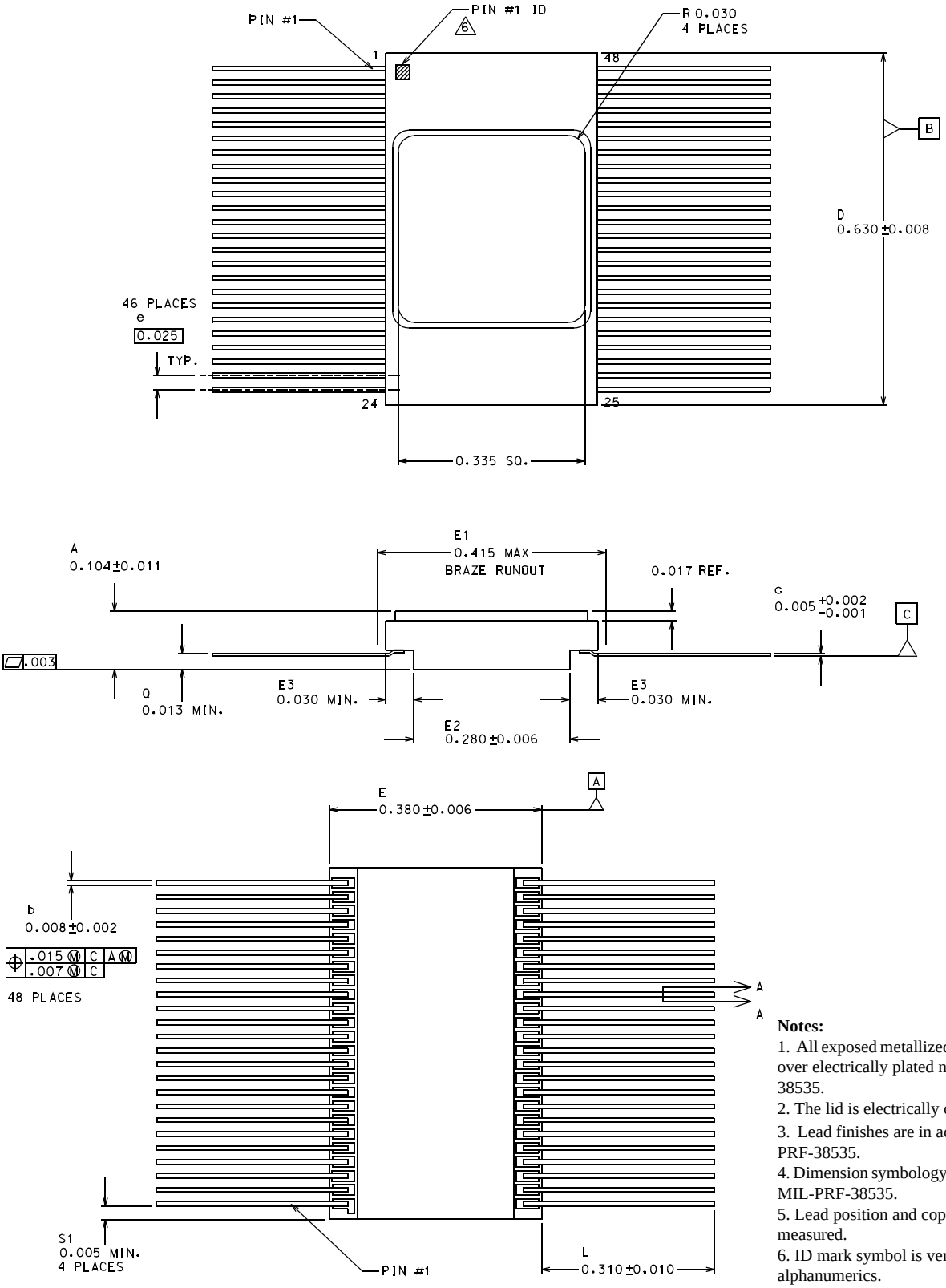


Figure 9. Driver V_{OD} and V_{OS} Test Circuit or Equivalent Circuit



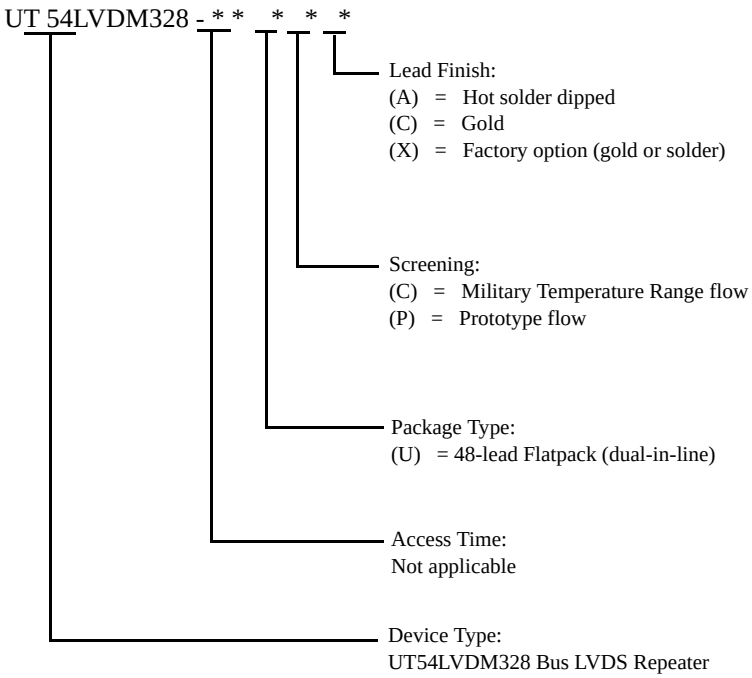
Notes:

1. All exposed metallized areas are gold plated over electrically plated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbology is in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option: no alphanumerics.

Figure 10. 48-lead Ceramic

ORDERING INFORMATION

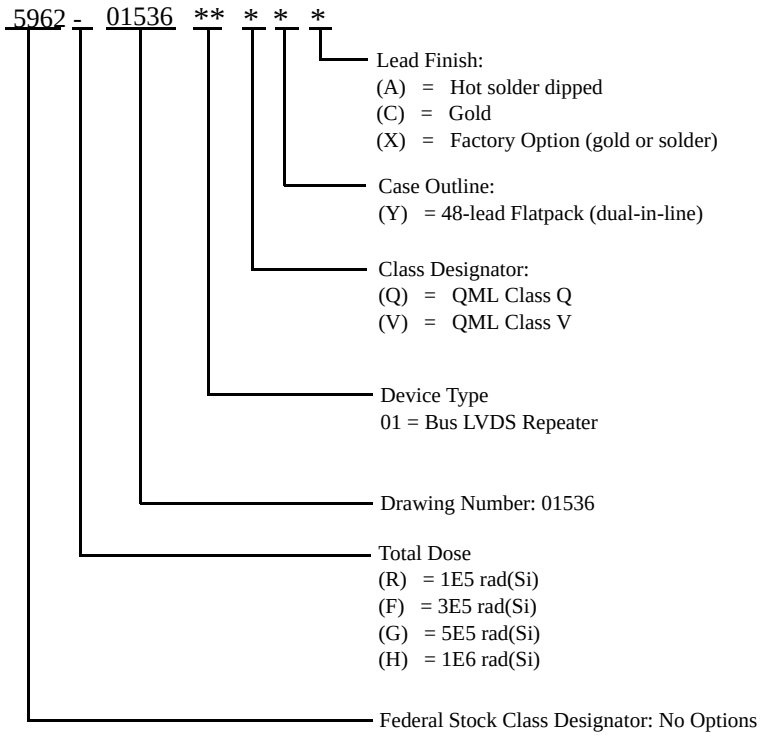
UT54LVDM328 Bus LVDS Repeater:



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

UT54LVDM328 Bus LVDS Repeater: SMD



Notes:

1.Lead finish (A,C, or X) must be specified.

2.If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).

3.Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

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