Standard Products

UT8MR8M8P 64Megabit Non-Volatile MRAM

Advanced Data Sheet
May 14, 2012
www.aeroflex.com/memories

FEATURES

- Single 3.3-V power supply
- Fast 50ns read/write access time
- Functionally compatible with traditional asynchronous SRAMs
- Equal address and chip-enable access times
- Automatic data protection with low-voltage inhibit circuitry to prevent writes on power loss
- CMOS and TTL compatible
- Data non-volatile for > 20 years at temperature
- Read/write endurance: 1E14 cycles
- 64-pin ceramic flatpack package

INTRODUCTION

The Aeroflex 64Megabit Non-Volatile magnetoresistive random access memory (MRAM) is a high-performance memory multichip module (MCM) compatible with traditional asynchronous SRAM operations, organized as four individual 2,097,152 words by 8 bits.

The MRAM is equipped with; four chip enables (/En), a single write enable (/W), and a single output enable (/G) pins, allowing for significant system design flexibility without bus contention. Data is non-volatile for > 20 year retention at temperature and data is automatically protected against power loss by a low voltage write inhibit.

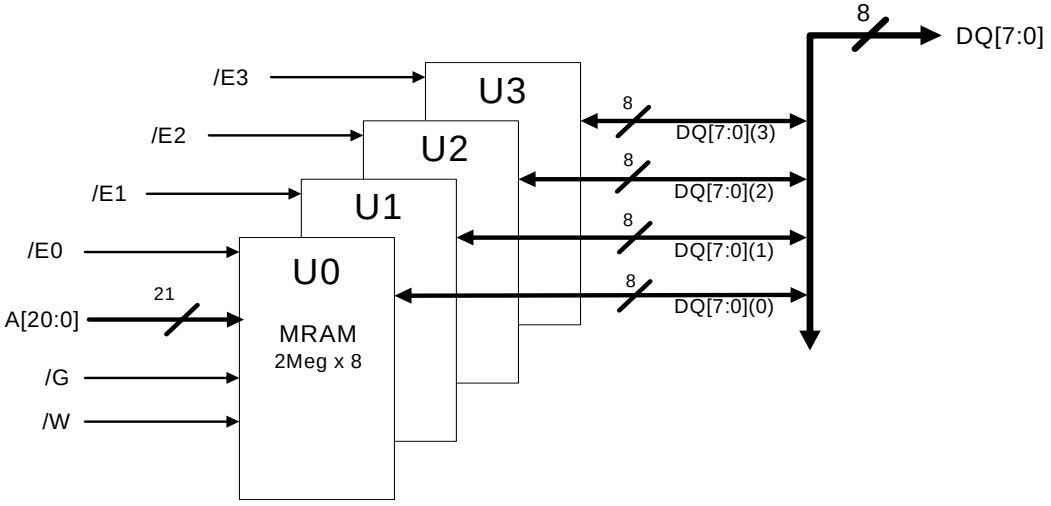


Figure 1. UT8MR8M8 MRAM Block Diagram

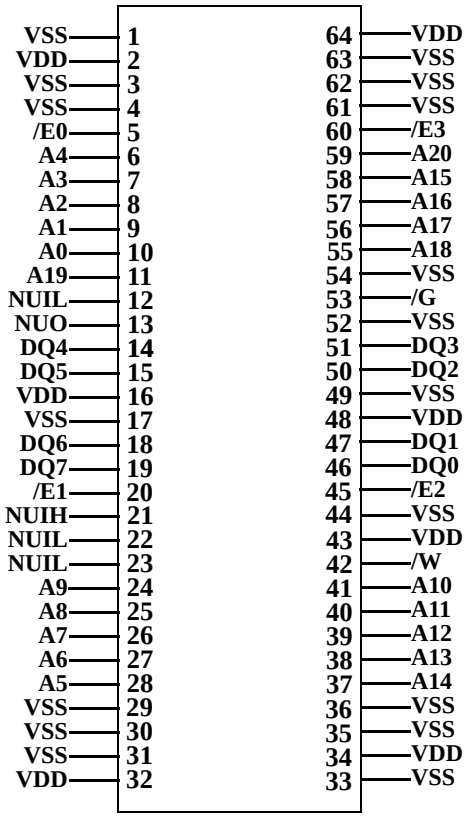


Figure 2. 40ns MRAM Pinout (64)

PIN NAMES

Table 1. 8M x 8 Pin Functions

Signal Name	Function
A[20:0]	Address Input
/E[3:0][1]	Chip Enable
/W	Write Enable
/G	Output Enable
DQ[7:0]	Data I/O
VDD	Power Supply
VSS	Ground
DC	Do Not Connect
NUIL[2]	Not Used Input Bias Low
NUIH[2]	Not Used Input Bias High
NUO[2]	Not Used Output Do Not Connect Driven internally

Notes:
1. Only one /En pin may be active at any time.
2. Reference Appendix A for future expansion options for NUIL, NUIH, and NUO pins.

DEVICE OPERATION

The UT8MR8M8 has control inputs called Chip Enable (/En), Write Enable (/W), Output Enable (/G); twenty-one address inputs, A[20:0]; and eight bidirectional data lines, DQ[7:0]. /En controls device selection, active, and standby modes. Asserting /En enables the device, causes I_{DD} to rise to its active value, and decodes the 21 address inputs to select one of 2,097,152 words in the memory. Note: Only one Chip Enable may be active at any time. /W controls read and write operations. During a read cycle, /G must be asserted to enable the outputs.

Table 2. Device Operation Truth Table

/En*	/G	/W	Mode	VDD Current	DQ[7:0]
H	X	X	Not Selected	Q_{IDD}	HI-Z
L	H	H	Output Disabled	I_{DDR}	HI-Z
L	L	H	Byte Read	I_{DDR}	D_{OUT}
L	X	L	Byte Write	I_{DDW}	D_{IN}

***Note:** Only one /En pin may be active at any time.

READ CYCLE

A combination of /W greater than V_{IH} (min) and a single /En less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

MRAM Read Cycle 1, the Address Access in Figure 4a, is initiated by a change in address inputs after a single /En is asserted, /G asserted and /W deasserted. Valid data appears on data outputs DQ[7:0] after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as a single chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

MRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 4b, is initiated by a single /En going active while /G remains asserted, /W remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A[20:0] is accessed and appears at the data outputs DQ[7:0].

WRITE CYCLE

A combination of /W and a single /En less than V_{IL}(max) defines a write cycle. The state of /G is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either /G is greater than V_{IH}(min), or when /W is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 5a, is defined by a write terminated by /W going high, with a single /En still active. The write pulse width is defined by t_{WLWH} when the write is initiated by /W, and by t_{ELWH} when the write is initiated by a single /En. Unless the outputs have been previously placed in the high-impedance state by /G, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ[7:0] to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 5b, is defined by a write terminated by a single /En going inactive. The write pulse width is defined by t_{WLEH} when the write is initiated by /W, and by t_{ELEH} when the write is initiated by a single /En going active. For the /W initiated write, unless the outputs have been previously placed in the high-impedance state by /G, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ[7:0] to avoid bus contention.

POWER UP AND POWER DOWN SEQUENCING

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DD}(min), there is a startup time of 2 ms before read or write operations can be executed. This time allows memory power supplies to stabilize. The /E and /W control signals should track V_{DD} on power up to V_{DD}- 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives /E and /W should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DD}(min).

The MRAM supports sleep mode operation using the ZZ control pin. ZZ must be high for 40ns in order to enter sleep mode. /E and /W must be high when ZZ is pulled low. As soon as ZZ is pulled low, there is a wait time of 100ns before the power supplies are within operating conditions.

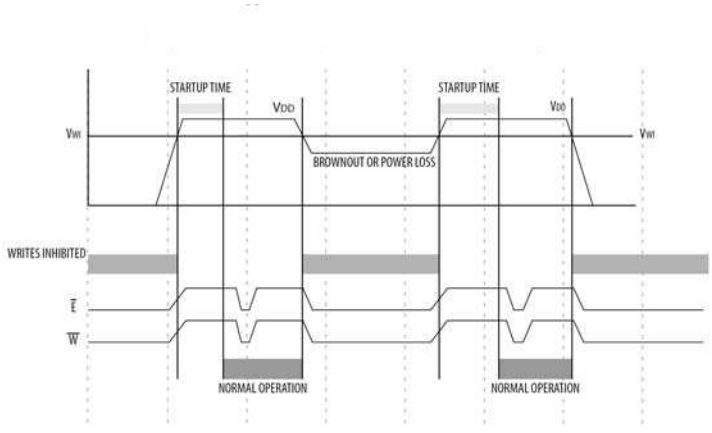


Figure 3. UT8MR8M8 Power Up and Power Down Sequencing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

The device contains protection against magnetic fields. Precautions should be taken to avoid device exposure of any magnetic field intensity greater than specified.

SYMBOL	PARAMETER	VALUE	UNIT
V_{DD}	Supply Voltage	-0.5 to 4.0	V
V_{IN}	Voltage on any pin	-0.5 to V_{DD}+0.5	V
I_{IO}	DC I/O current per pin	± 20	mA
P_D	Package power dissipation[2]	0.600	W
T_J	Maximum junction temperature	+125	^oC
θ_{JC}	Thermal resistance junction to case – Single Die	5	$^oC/W$
T_{STG}	Storage temperature	-65 to +125	^oC
ESD_{HBM}	ESD	>2000	V
H_{max_write}	Maximum magnetic field during write	5000	A/m
H_{max_read}	Maximum magnetic field during read or standby	8000	A/m

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. Power dissipation capability depends on package characteristics and use environment.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
T_C	Operating case temperature	25^oC
V_{DD}	Operating supply voltage	3.0V to 3.6V
V_{WI}	Write inhibit voltage	2.5V to 3.0V[1]
V_{IH}	Input high voltage	2.0V to V_{DD}+0.3V
V_{IL}	Input low voltage	-0.3V to 0.8V

Notes:

1. After power up or if V_{DD} falls below V_{WI}, a waiting period of 2 ms must be observed, and /E and /W must remain high for 2 ms. Memory is designed to prevent writing for all input pin conditions if V_{DD} falls below minimum V_{WI}.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0V to 3.6V; Unless otherwise noted, Tc is per the temperature ordered

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V_{IH}	High-level input voltage			2.0		V
V_{IL}	Low-level input voltage				0.8	V
V_{OL1}	Low-level output voltage	I_{OL} = 4mA,V_{DD} =V_{DD} (min)			0.4	V
V_{OL2}	Low-level output voltage	I_{OL} = + 100µA,V_{DD} =V_{DD} (min)			+0.2	V
V_{OH1}	High-level output voltage	I_{OH} = -4mA,V_{DD} =V_{DD} (min)		2.4		V
V_{OH2}	High-level output voltage	I_{OH} = -100µA,V_{DD} =V_{DD} (min)		V_{DD}-0.2		V
C_{IN}[1]	Input capacitance	*f* = 1MHz @ 0V			TBD	pF
C_{IO}[1]	Bidirectional I/O capacitance	*f* = 1MHz @ 0V			TBD	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}		-1	+1	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and $V_{SS,}$ V_{DD} = V_{DD} (max) /G = V_{DD} (max)		-1	+1	µA
I_{OS}[2, 3]	Short-circuit output current	V_{DD} = V_{DD} (max), V_O = V_{DD} V_{DD} = V_{DD} (max), V_O = V_{SS}		-100	+100	mA
I_{DDR}	Active read supply current	Read mode (I_{OUT} = 0mA; V_{DD} = max)			100	mA
I_{DDW}	Active write supply current	Write mode (V_{DD} = max)			170	mA
Q_{IDD}	Quiescent supply current	CMOS leakage current (/E = V_{DD}; all other inputs equal V_{SS} or V_{DD}; V_{DD} = max)	25°C Room		21	mA

Notes:

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Allow 100µs to exit sleep mode before performing any other operation and observe start-up time and start-up conditions for /En and /W..

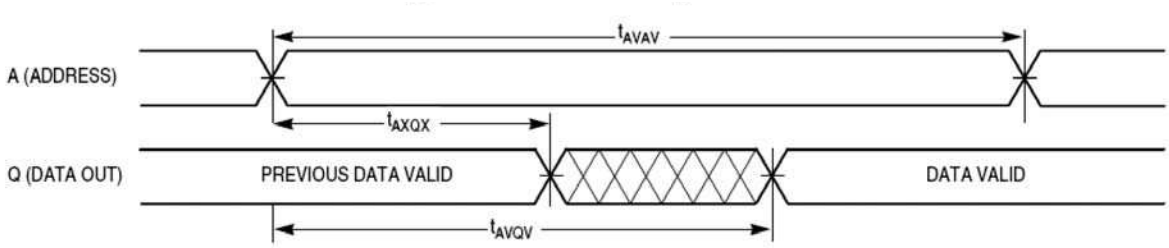
AC CHARACTERISTICS READ CYCLE[1]

$V_{DD} = V_{DD}$ (min); Unless otherwise noted, Tc is per the temperature ordered

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}	Read cycle time	50		ns
t_{AVQV}	Address access time		50	ns
t_{ELQV}[2]	Enable access time		50	ns
t_{GLQV}	Output enable access time		19	ns
t_{AXQX}	Output hold from address change	3		ns
t_{ELQX}[3]	Enable low to output active	3		ns
t_{GLQX}[3]	Output enable low to output active	0		ns
t_{EHQZ}[3]	Enable high to output Hi-Z	0	15	ns
t_{GHQZ}[3]	Output enable high to output Hi-Z	0	10	ns

Notes:o

1. /W is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
2. Address valid before or at the same time /E goes low.
3. Transition is measured at +/-200mV from the steady-state voltage.



NOTES:

Device is continuously selected **(/En ≤ V_{IL}, /G ≤ V_{IL}).**

Figure 4a. MRAM Read Cycle 1

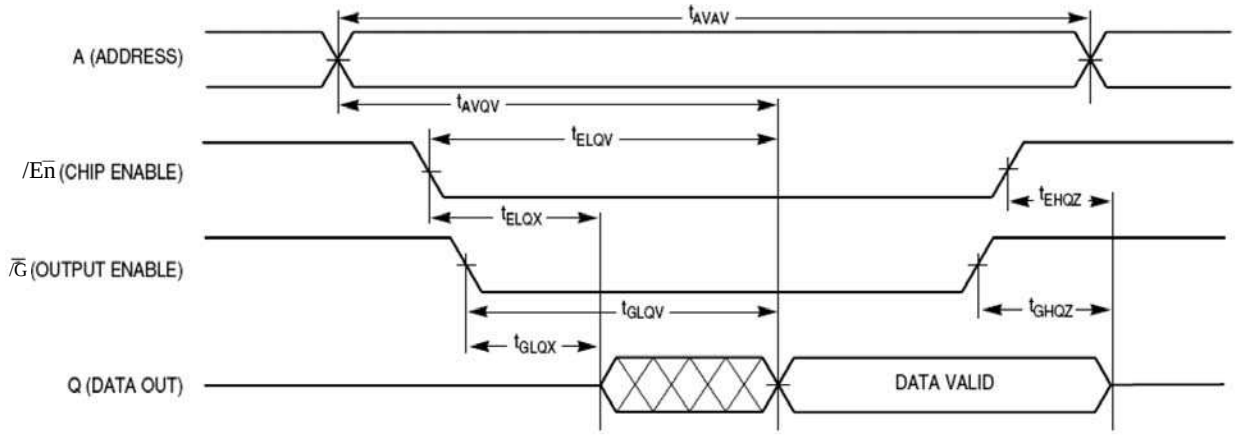


Figure 4b. MRAM Read Cycle 2

AC CHARACTERISTICS /W CONTROLLED WRITE CYCLE

V_{DD}= V_{DD} (min); Unless otherwise noted, Tc is per the temperature ordered.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}[2]	Write cycle time	50		ns
t_{AVWL}	Address set-up time	0		ns
t_{AVWH}	Address valid to end of write (/G high)	20		ns
t_{AVWH}	Address valid to end of write (/G low)	20		
t_{WLWH} t_{WLEH}	Write pulse width (/G high or low)	15		ns
t_{DVWH}	Data valid to end of write	10		ns
t_{WHDX}	Data hold time	0		ns
t_{WLQZ}[3]	Write low to data Hi-Z	0	15	ns
t_{WHQX}[3]	Write high to output active	3		ns
t_{WHAX}	Write recovery time	18		ns

Notes:

1. All write occurs during the overlap of /E low and /W low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If /G goes low at the same time or after /W goes low, the output will remain in a high impedance state.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. Transition is measured +/-200mV from the steady-state voltage.

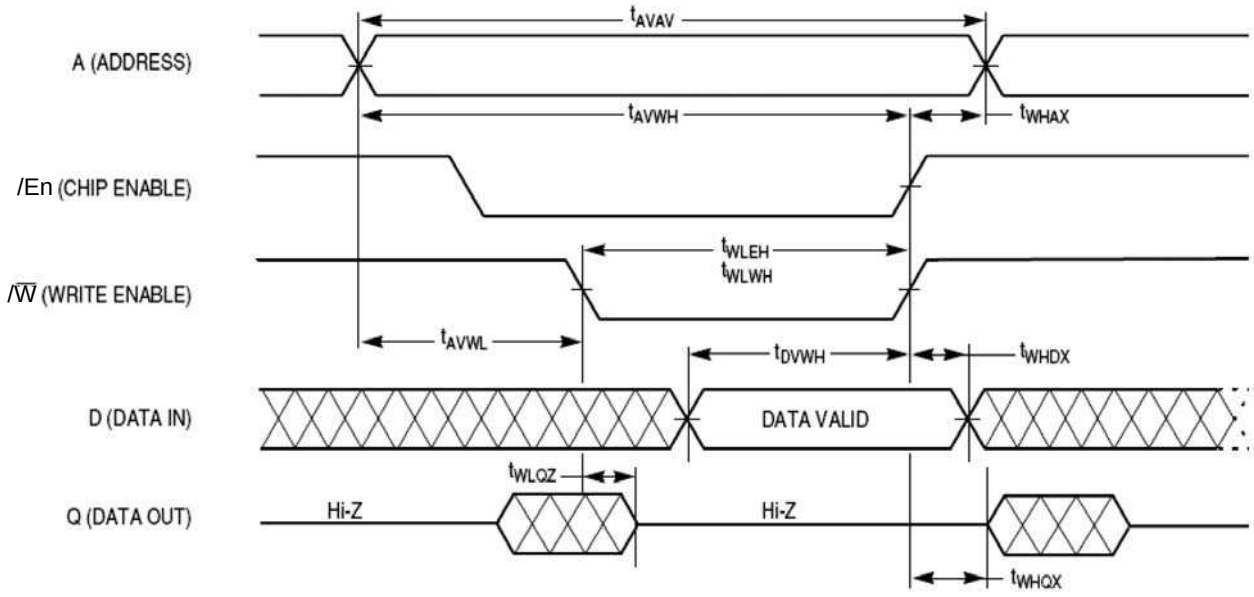


Figure 5a. MRAM Write Cycle 1 (/W Controlled Access)

AC CHARACTERISTICS /E CONTROLLED WRITE CYCLE[1]

V_{DD}= V_{DD} (min); Unless otherwise noted, Tc is per the temperature ordered.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}[2]	Write cycle time	50		ns
t_{AVEL}	Address set-up time	0		ns
t_{AVEH}	Address valid to end of write (/G high)	20		ns
t_{AVEH}	Address valid to end of write (/G low)	20		
t_{ELEH} t_{ELWH}	Enable to end of write (/G high)	15		ns
t_{ELEH}[3] t_{ELWH}[3]	Enable to end of write (/G low)	15		ns
t_{DVEH}	Data valid to end of write	10		ns
t_{EHDX}[4]	Data hold time	0		ns
t_{EHAX}[4]	Write recovery time	18		ns

Notes:

1. All write occurs during the overlap of /E low and /W low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If /G goes low at the same time or after /W goes low, the output will remain in a high impedance state.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If /E goes low at the same time or after /W goes low, the output will remain in a high-impedance state. If /E goes high at the same time or before /W goes high, the output will remain in a high-impedance state.
4. Transition is measured +/-200mV from the steady-state voltage.

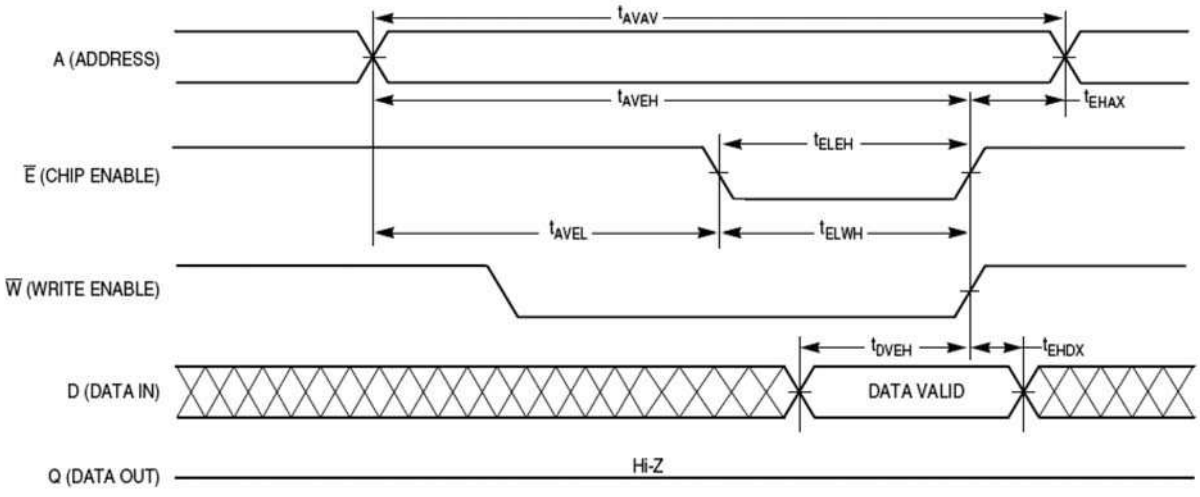
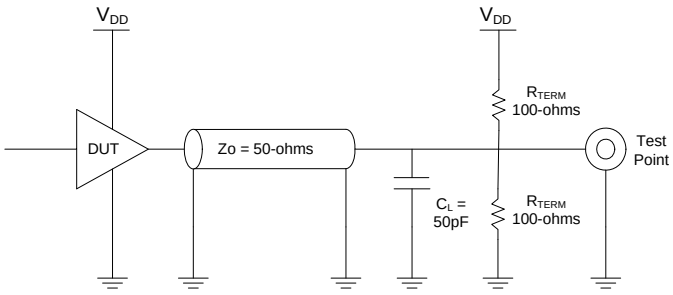


Figure 5b. MRAM Write Cycle 2 (/E Controlled)



Notes:
1. Measurement of data output occurs at the low to high or high to low transition mid-point, typically, VDD/2.

Figure 6. AC Output Test Load or Equivalent

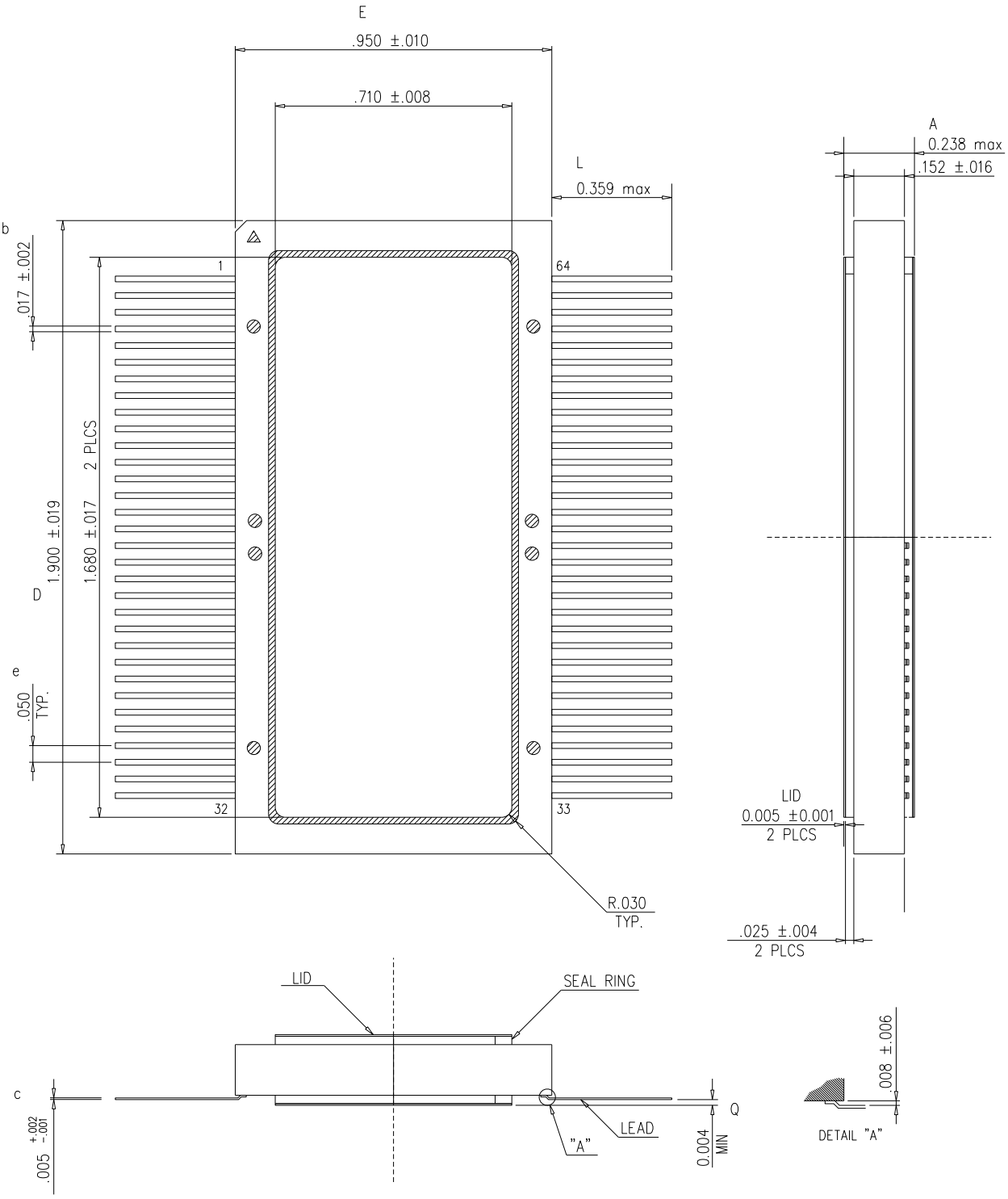
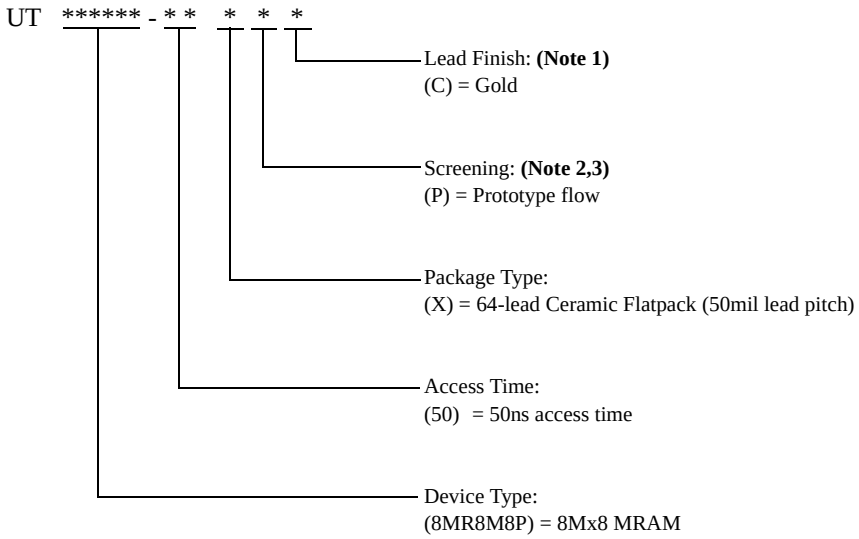


Figure 7. 64-Pin Dual-Sided, Ceramic, Bottom Brazed, Flatpack

ORDERING INFORMATION

8M x 8 MRAM:



Notes:
1. Lead finish is "C" (Gold) only.
2. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Radiation neither tested nor guaranteed.

Aeroflex Colorado Springs Application Note

APPENDIX A

Pin Functions for 64Mb Non-Volatile MRAM Multi-Chip Module (MCM)

Table 1: Cross Reference of Applicable Products

Product Name	Generation	Manufacturer Part #	SMD#	Device Type	Grades Offered
64 Mb Non-Volatile MRAM	1	UT8MR8M8P	N/A	N/A	Prototype only
64 Mb Non-Volatile MRAM	2	UT8MR8M8	TBS	TBS	Prototype, HiRel, QML-Q, QML-V

1.0 Overview

The Aeroflex 64 Megabit Non-Volatile magneto-resistive random access memories (MRAM) Multi-Chip Modules (MCMs) are offered as both a first generation, prototype only device and a second generation QML device qualified for flight applications. The first generation device is identified by the Aeroflex part number UT8MR8M8P, while the second generation device is identified by the Aeroflex part number UT8MR8M8. These part numbers are listed in Table 1 above.

Aside from radiation hardness and timing characteristics, the HiRel / QML flight version also introduces some extended pin functions beyond those available on the UT8MR8M8P. The purpose of this application note is to provide the user with the foresight to accommodate the additional features offered by the HiRel UT8MR8M8, into a circuit design that initially supports the prototype only UT8MR8M8P. The pin assignments for each MCM package type are identified in Figures 1 and 2. The extended features available with the HiRel UT8MR8M8 are defined in Table 1, with the truth table for the associated enable inputs in Table 2.

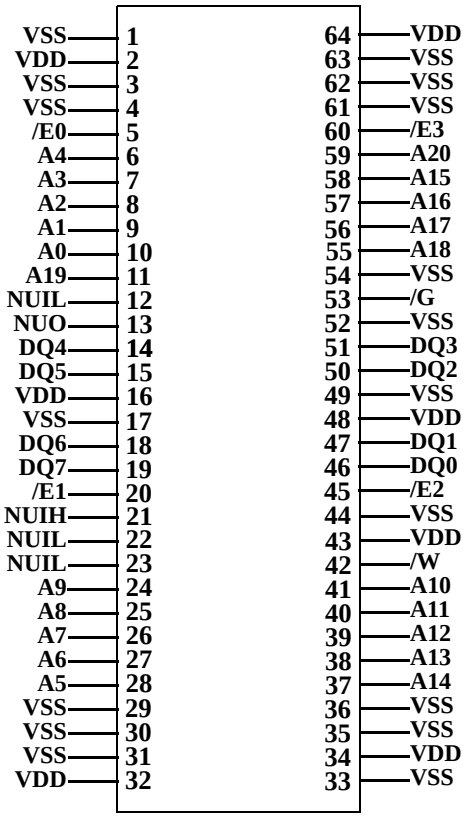


Figure 1: Signal assignments for UT8MR8M8P

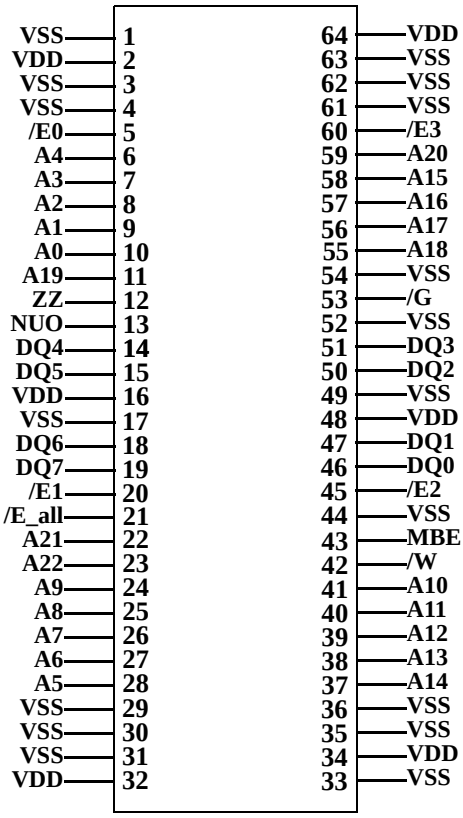


Figure 2: Signal assignments for UT8MR8M8

Table 1: Signal definitions for additional I/O available with HiRel UT8MR8M8

Pin Number	Signal Name	Activation Level	Function
12	ZZ	High	Places all die into internal low power, sleep mode even while system power is still applied to VDD.
21	/E_all	Low	Group enable for all 4 die in 64Mb MCM. Allows device to be addressed as a single, 64Mb memory and uses address bits A21 and A22 to decode and select 1 of 4 MRAM die.
22, 23	A21, A22		Extended address lines for linearly addressing the 8M addressable memory locations when /E_all is active.
43	MBE	Open drain pull-down	Multi-bit error flag. Identifies that ECC logic has detected two or more bit errors during the current read cycle. Allows for wired-or of multiple MBE when using multiple MRAMs. 1K Ohm to VDD.

Table 2: Signal definitions for Chip Enables on HiRel UT8MR8M8

Chip Enable Functions*							
/E_all	/E_0	/E_1	/E_2	/E_3	A22	A21	Comment
0	1	1	1	1	0	0	MRAM die 0 enabled
0	1	1	1	1	0	1	MRAM die 1 enabled
0	1	1	1	1	1	0	MRAM die 3 enabled
0	1	1	1	1	1	1	MRAM die 2 enabled
1	0	1	1	1	X	X	MRAM die 0 enabled
1	1	0	1	1	X	X	MRAM die 1 enabled
1	1	1	0	1	X	X	MRAM die 2 enabled
1	1	1	1	0	X	X	MRAM die 3 enabled

*Only one enable line should ever be asserted low at any given time.

2.0 Summary

Aeroflex offers both prototype-only and HiRel / QML versions of the 64Mb Non-Volatile MRAM MCMs. The prototype-only device, UT8MR8M8P, was developed as a first generation solution to allow for early system development. The second generation HiRe version, UT8MR8M8, is undergoing full QML-V qualification for flight applications. The HiRel UT8MR8M8 provides several new signal functions that enhance system capability By anticipating the new I/O functions available with the HiRel UT8MR8M8, the designer can accommodate these signals and achieve drop-in functionality of the flight version into designs originally implemented around the UT8MR8M8P.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Hi-Rel

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