Standard Products

RDC5028C 16-Bit Monolithic Tracking Rad Tolerant Resolver-To-Digital Converter

www.aeroflex.com/RDC

February 4, 2013

FEATURES

- Enhanced version of the ACT5028B
- Radiation performance
  - Total dose: 1 Mrad(Si), Dose rate = 50 - 300 rads(Si)/s
  - SEL:Immune up to 100 MeV-cm^2/mg
- +5VDC power only
- Programmable: By using a few non critical external resistors and capacitors
  - Resolution: 10, 12, 14 or 16 bit resolution
  - Bandwidth
  - Tracking rate
- Low power: +5V @ 20 mA typ
- 45 to 30,000 Hz carrier frequency range
- Accuracy:
  - 10.0 Arc Minutes if not compensated by INL correction factors.
  - 5.3 Arc Minutes using INL correction factors.
- Differential instrument amplifiers resolver input
- -55° to +125°C operating temperature
- Digital interface logic voltage of 3.3V to 5V
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic
  - 52 Pin Ceramic QUAD flat package (CQFP), .956" SQ x .100" Ht
  - Weight: 5.0g max
- Evaluation board available for test and evaluation. See Aeroflex Application note AN5028-1

- **Aeroflex Plainview's Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.**

APPLICATIONS

This single chip Resolver-to-Digital Converter (RDC) is used in shaft angle control systems, and is suitable for space or other radiation environments that require > 1 Mrad(Si) total dose tolerance. The part is latchup free in heavy ion environments (e.g., geosynchronous orbits) and is estimated to experience SEU induced errors of less than 15 minutes of arc at a rate of 1 per device per 2 years when operating dynamically.

THEORY OF OPERATION

The RDC5028 converter is a single CMOS Type II tracking resolver to digital converter monolithic chip. It is implemented using precision analog circuitry and digital logic. For flexibility, the converter bandwidth, dynamics and velocity scaling are externally set with passive components. Refer to Figure 1, RDC5028 Block Diagram.

The converter is powered from +5VDC. Analog signals are referenced to signal ground, which is nominally VCC/2. The converter consists of three main sections; the Analog Control Transformer (CT), the Analog Error Processor (EP) and the Digital Logic Interface.

The CT has two analog resolver inputs (Sin and Cos) that are buffered by high impedance input instrumentation type amplifiers and the 16 bit digital word which represents the output digital angle. The CT performs the ratiometric trigonometric computation of:

$$\mathrm{SIN(A)\sin(wt)\,COS(B) - COS(A)\sin(wt)\,SIN(B) = SIN(A\text{-}B)\sin(wt)}$$

Utilizing amplifiers, switches, logic and resistors in precision ratios. "A" represents the resolver angle, "B" represents the digital angle and sin(wt) represents the resolver reference carrier frequency.

The Error Processor is configured as a critically damped Type II loop. The AC error, SIN(A-B) sin(wt) is full wave demodulated using the reference squared off as its drive. This DC error is integrated in an analog integrator yielding a velocity voltage which in turn drives a Voltage Controlled Oscillator (VCO). Note in the block diagram, hysterisis is added to prevent dithering and disables counting when the error is less than 1 LSB. This VCO is an incremental integrator (constant voltage input to position rate output) which, together with the velocity integrator, forms a Type II loop. A lead is inserted to stabilize the loop and a lag is inserted at a higher frequency to attenuate the carrier frequency ripple. The error processor drives the 16 bit digital output until it nulls out. Then angle "A" = "B". The digital output equals angle input to the accuracy of the precision control transformer. The various error processor settings are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.The digital logic interface has a separate power line, VLI/O that sets the interface logic 1 level. It can be set anywhere from +3V to the +5V power supply.

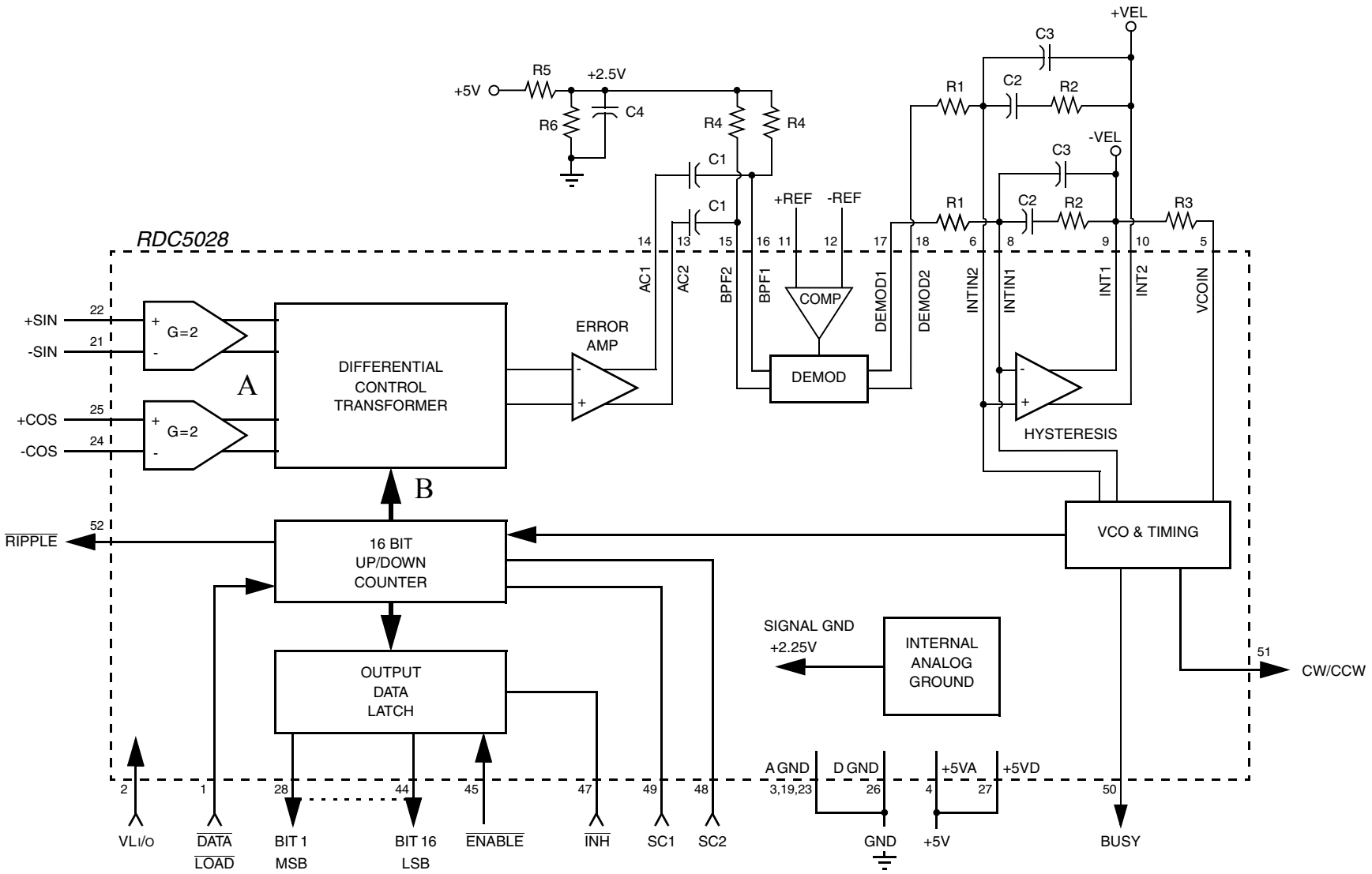


FIGURE 1 – RDC5028 BLOCK DIAGRAM

PIN DESCRIPTIONS

SIGNAL	DIRECTION	PIN	SIGNAL DESCRIPTION
+SIN -SIN	INPUT	22 21	Analog Sine input from Synchro or Resolver. 1.3Vrms nominal
+COS -COS	INPUT	25 24	Analog Cosine input from Synchro or Resolver. 1.3Vrms nominal
+REF -REF	INPUT	11 12	Analog Reference input
BIT 1 (MSB) BIT 2 BIT 3 BIT 4 BIT 5 BIT 6 BIT 7 BIT 8 BIT 9 BIT 10 BIT 11 BIT 12 BIT 13 BIT 14 BIT 15 BIT 16 (LSB)	BIDIR	28 29 30 31 32 34 35 36 37 38 39 40 41 42 43 44	Digital angle data. Parallel format. Natural binary positive logic. Bit 1, most significant bit = 180°, Bit 2 = 90°, Bit 3 = 45° and so on. In the 10 bit mode, Bit 10 is the LSB. Bits 11-16 are 0s. In the 12 bit mode, Bit 12 is the LSB. Bits 13-16 are 0s. In the 14 bit mode, Bit 14 is the LSB. Bits 15-16 are 0s. In the 16 bit mode, Bit 16 is the LSB.
SC1 SC2	INPUT	49 48	Digital input. Sets the resolution. SC1 SC2 Resolution 0 0 10 bit 0 1 12 bit 1 0 14 bit 1 1 16 bit
$\overline{\text{ENABLE}}$*	INPUT	45	Logic 0 enables digital angle output. Otherwise it is high impedance.
$\overline{\text{INH}}$*	INPUT	47	Logic 0 freezes the digital angle output so that it can be safely read.
$\overline{\text{DATALOAD}}$*	INPUT	1	Logic 0 enables the digital angle lines to be inputs to preset the angle. Logic 1 is for normal digital angle output.
BUSY	OUTPUT	50	A logic 1 pulse when the digital angle changes by 1 LSB.
CW/CCW	OUTPUT	51	For turns counting. Logic 1 = counting up (CW), logic 0 = counting down (CCW).
$\overline{\text{RIPPLE}}$*	OUTPUT	52	Ripple clock for turns counting. A logic 0 pulse = a 0° transition in either direction.
AC1 AC2	OUTPUT	14 13	Differential AC error output
BPF1 BPF2	INPUT	16 15	Differential AC error input to demodulator
DEMOD1 DEMOD2	OUTPUT	17 18	Differential DC error output
INTIN1 INTIN2	INPUT	8 6	Differential DC input to differential velocity integrator
INT1 INT 2	OUTPUT	9 10	Differential velocity output
VCOIN	INPUT	5	Input to Voltage Controlled Oscillator
V_{CC} V_{DD}	POWER	4 27	Analog Power In Digital Power In
A GND D GND	POWER	3, 19, 23 26	Analog Power ground Digital Power ground
$VL_{I/O}$	POWER	2	Digital input/output DC power supply. Sets logic 1 level. +3V to +5V

* Indicates Active Low Signal

ABSOLUTE MAXIMUM RATINGS *

PARAMETER	VALUE
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Positive Power Supply Voltage (V_{CC} = V_{DD})	-0.5 V to +7.0 V
Analog Output Current (Output Shorted to GND)	32 mA Max
Digital Output Current (Output Shorted to GND)	18.6 mA Max
Analog Input Voltage Range	-0.5 V to + (V_{CC} + 0.5 V)
Digital Input Voltage Range	-0.3 V to + (V_{DD} + 0.3 V)
Thermal Resistance $Ø_{JC}$ Specification	1.25°C/W
Maximum Junction Temperature	135°C
Lead Temperature (soldering, 10 seconds)	300°C
ESD Class 2 MIL-STD-883 Method 3015, 8	2000 V to 3999 V

* Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only; functional operation beyond these operating conditions is not recommended and extended exposure beyond these operating conditions may effect device reliability.

OPERATING CONDITIONS
(T_A = -55°C to +125°C)

POWER SUPPLY	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD} = V_{CC}	Operating Voltage	4.5	5	5.5	V_{DC}
I_{DD} + I_{CC}	Operating Current	-	20	35	mA
$VL_{I/O}$	Interface Voltage	3	3.3, 5	5.5	V_{DC}

ELECTRICAL CHARACTERISTICS 2/, 5/, 6/
(T_A = -55°C to +125°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Accuracy 4/ 8/	Add 1 LSB for total Error, Using INL correction factors.	-	+/-2	+/-5.0	Minutes
	Add 1 LSB for total Error, Not compensated by INL correction factors	-	+/-4	+/-10.0	
Repeatability		-	-	1	LSB
Resolution per LSB	10 Bit Mode	0.35	-	-	Degrees
		21.1	-	-	Minutes
	12 Bit Mode	0.09	-	-	Degrees
		5.27	-	-	Minutes
	14 Bit Mode	0.022	-	-	Degrees
		1.32	-	-	Minutes
	16 Bit Mode	0.0055	-	-	Degrees
		0.33	-	-	Minutes
Max Tracking Rate	SC1 SC2 Bits Used				
10 Bit Mode	0 0 B1 - B10	1024	-	-	RPS
12 Bit Mode	0 1 B1 - B12	256	-	-	RPS
14 Bit Mode	1 0 B1 - B14	64	-	-	RPS

ELECTRICAL CHARACTERISTICS 2/, 5/, 6/
(TA = -55°C to +125°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
16 Bit Mode	1 1 B1 - B16	16	-	-	RPS
VCO Frequency		1.05	-	-	MHz

ELECTRICAL SPECIFICATIONS 2/, 5/, 6/
(TA = -55°C to +125°C)

ANALOG SIGNAL INPUTS	SYM	PARAMETER	MIN	TYP	MAX	UNITS
SIN, COS, REF, VCOIN, INTIN1, INTIN2, BPF1, BPF2	VSIN, VCOS, VREF	Voltage measurement made between ± inputs	1.0	1.3	1.5	VRMS
	FREF	Frequency 1/	45	-	30K	Hz
		Impedance	2.5	-	-	MΩ
		Capacitance 3/	-	5	15	pF
		DC Bias on -Sin, -Cos	-	VCC/2	-	VDC
		Bias Current				
		+25°C	-100	-	+100	nA
		+125°C	-1000	-	+1000	nA
DIGITAL INPUTS						
ENABLE, DATA LOAD SC2, SC1, INH See Note 3	VIL	Logic Low 3/	-	-	0.8	VDC
	VIH	Logic High 3/	2	-	-	VDC
	IIN	Leakage Current				
		+25°C	-200	-	+200	nA
		+125°C	-2000	-	+2000	nA
		Impedance	2.5	-	-	MΩ
		Capacitance 3/	-	5	15	pF
DIGITAL OUTPUTS						
BUSY, RIPPLE CW/CCW	VOL	Logic Low @ 1.6mA	-	-	0.3	VDC
	VOH	Logic High @ -1.6mA	VLI/O - 0.8	-	-	VDC
DIGITAL I/O						
B1 - B16 7/	VIL	Logic Low 3/	-	-	0.8	VDC
	VIH	Logic High 3/	2	-	-	VDC
	VOL	Logic Low @ 1.6mA	-	-	0.3	VDC
	VOH	Logic High @ -1.6mA	VLI/O - 0.8	-	-	VDC
	IIN	Leakage Current				
		+25°C	-200	-	+200	nA
		+125°C	-2000	-	+2000	nA
	IZ	High-Z Leakage Current 3/				
		+25°C	-200	-	+200	nA
		+125°C	-2000	-	+2000	nA

TIMING SPECIFICATIONS 6/

DIGITAL OUTPUT	SYM	COMMENTS	MIN	TYP 2/	MAX	UNITS
Busy	t_{LH}	Rise Time	-	20	85	ns
	t_{HL}	Fall Time	-	20	85	ns
CW/CCW, Ripple, B1- B16	t_{LH}	Rise Time	-	45	120	ns
	t_{HL}	Fall Time	-	45	100	ns
Busy Pulse Width	t_{BPW}		300	400	600	ns
Busy to Data Stable 3/	t_{BDS}	Enable = Low	-	-	350	ns
Ripple Pulse Width	t_{RPW}		140	200	300	ns
Busy to Ripple 3/	t_{BR}		-	100	150	ns
READ DATA 3/ ($\overline{\text{Enable}}$ & $\overline{\text{INH}}$ would normally be tied together, $\overline{\text{Data Load}}$ = Logic Hi)						
$\overline{\text{Enable}}$ Low to D ata Stable	t_{ELDS}		-	-	70	ns
$\overline{\text{Enable}}$ High to Data Hi-Z	t_{EHZ}		-	-	70	ns
$\overline{\text{INH}}$ Low to Data Stable	t_{ILDS}		-	-	400	ns
$\overline{\text{INH}}$ High to Data Change	t_{IHZ}		-	-	150	ns
WRITING DATA 3/ ($\overline{\text{Enable}}$ & $\overline{\text{INH}}$ = Logic Hi)						
Data Load Pulse Width	t_{DLPW}	Transparent Trailing Edge Latch	200	-	-	ns
Data Setup to Data Load	t_{WDS}		60	-	-	ns
Data Hold	t_{WDH}		10	-	-	ns

Notes

1/ @ 10 Bits, $F_{REF} > 4 \times BW_{CL}$
@ 12 Bits, $F_{REF} > 8 \times BW_{CL}$
@ 14 Bits, $F_{REF} > 12 \times BW_{CL}$
@ 16 Bits, $F_{REF} > 16 \times BW_{CL}$

2/ All typical values are measured at +25°C.

3/ Characteristics are guaranteed by design, not production tested.

4/ Accuracy applies over the full operating Power Supply voltage range, Full operating Temperature range, Reference Frequency range, 10% Signal Amplitude variation and 10% Reference Harmonic distortion.

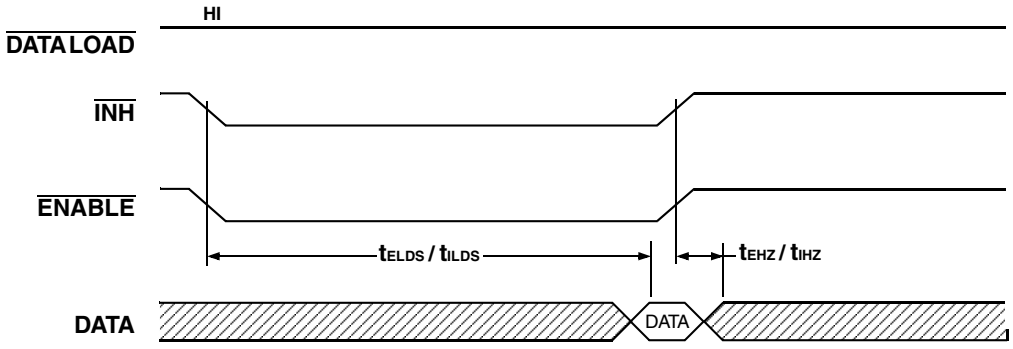
5/ For ESD protection the RDC5028 features limiting resistors in series with diodes. Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation.

6/ All testing at nominal voltage.

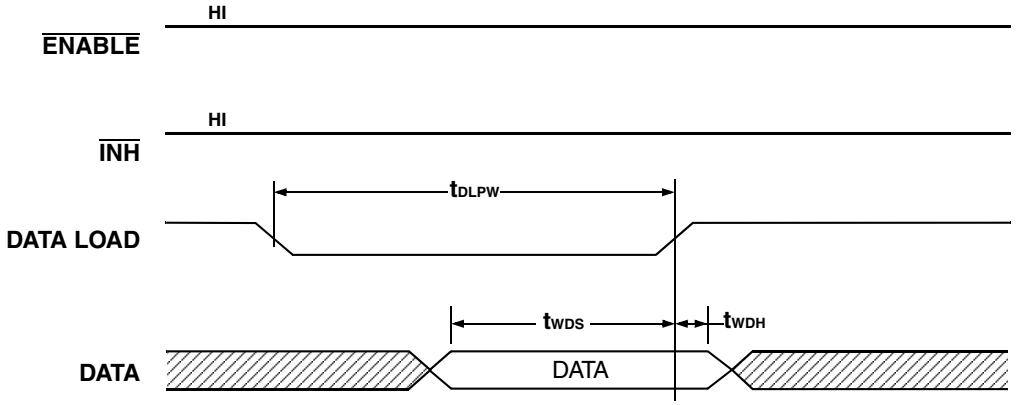
7/ All unused inputs shall be tied to Ground. Bit 1 is always the MSB.

8/ See Application Note 1, page 16 and Table II, page 19 "Using INL Error Correction Factors to Improve Accuracy"

READ CYCLE



WRITE CYCLE



BUSY TIMING

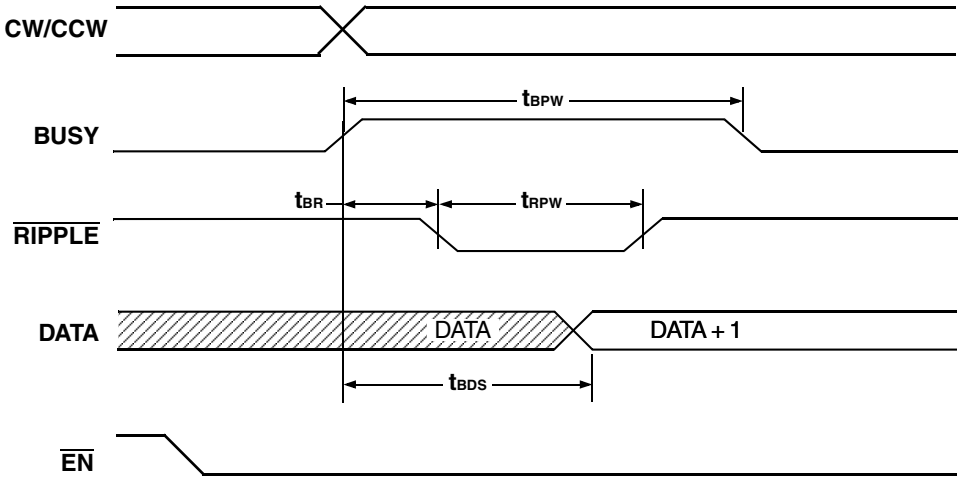


FIGURE 2 – RDC5028 TIMING DIAGRAMS

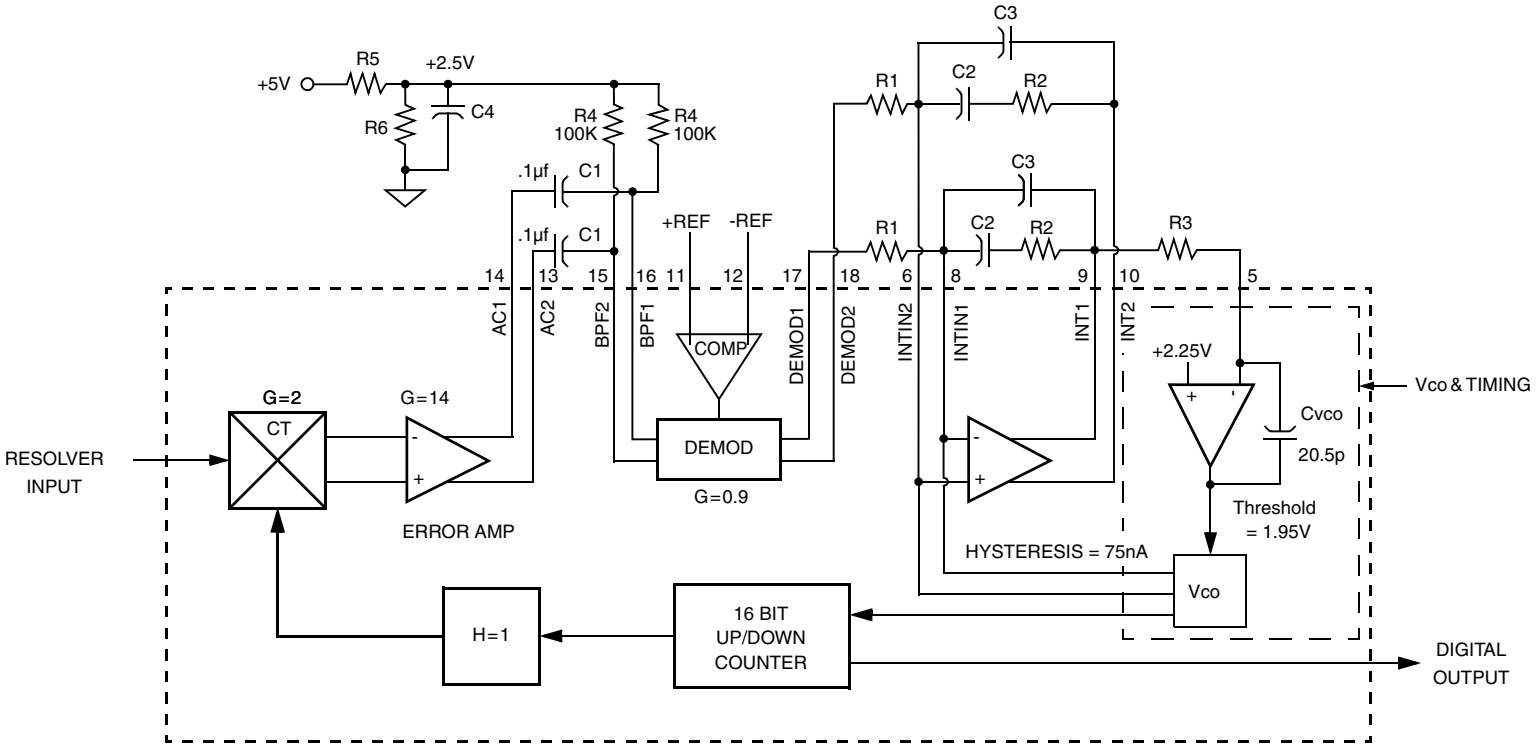


FIGURE 2 – RDC5028 FUNCTIONAL BLOCK DIAGRAM

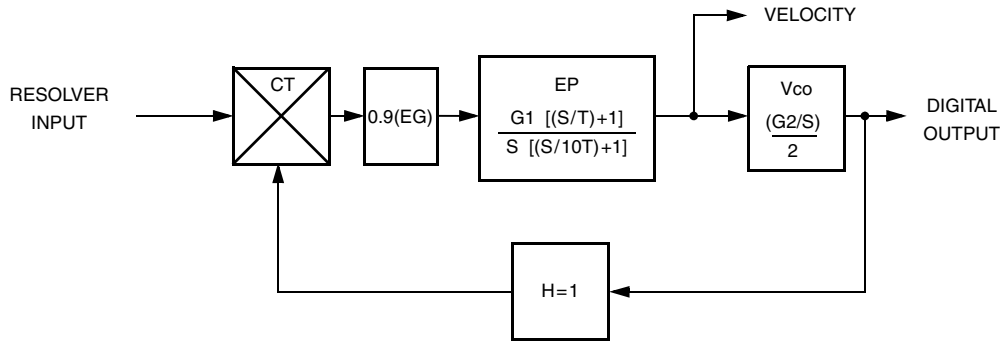


FIGURE 3 – RDC5028 TRANSFER FUNCTION DIAGRAM

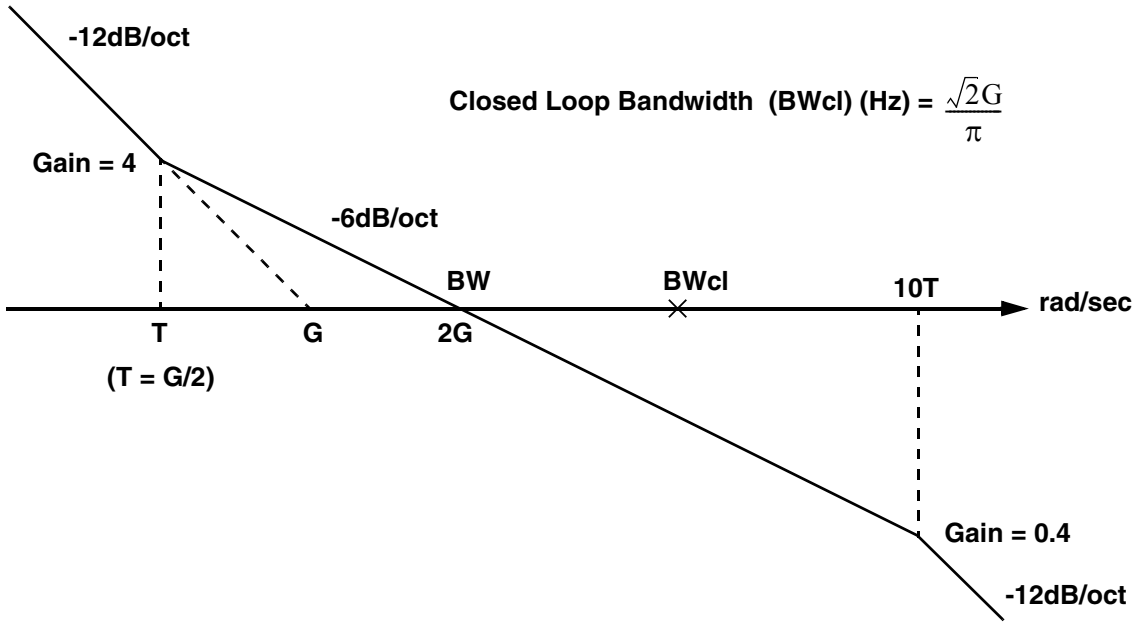


FIGURE 4 – RDC5028 OPEN LOOP BODE PLOT

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram, Transfer Function Diagram and Bode plots, as shown in Figures 2, 3 and 4.

PROCEDURE FOR SELECTING RDC BANDWIDTH COMPONENTS *

Input: Carrier Frequency (Fc) in Hz [47 to 30,000 Hz]
Input: Nominal Resolver Input Level in Vrms [1Vrms min. to 1.5Vrms max.]
Input: Resolution in bits; 10, 12, 14 or 16 bits
Input: Closed Loop Bandwidth (BWcl) in Hz [10 bit; BWcl = Fc/4 max.]
[12 bit; BWcl = Fc/8 max.]
[14 bit; BWcl = Fc/12 max.]
[16 bit; BWcl = Fc/16 max.]

Input: Maximum Tracking Rate in RPS (RPS = rotations per second)
[16 bit; 16 RPS max.]
[14 bit, 64 RPS max.]
[12 bit; 256 RPS max.]
[10 bit, 1024 RPS max.]

Input: Hysteresis in LSBs. Recommended is 1 LSB for 16 & 14 bits and 0.7 LSBs for 12 & 10 bits.

EG = Nominal Resolver Input Level • .0027 [16 bit] or
EG = Nominal Resolver Input Level • .011 [14 bit] or
EG = Nominal Resolver Input Level • .043 [12 bit] or
EG = Nominal Resolver Input Level • .17 [10 bit]

G = 2.22 • BWcl

G^2 = EG • 0.45 • G1 • G2

PROCEDURE FOR SELECTING RDC BANDWIDTH COMPONENTS * (Cont)

Hysteresis recommended values
HYS = 0.7 [10 & 12 bit] or
HYS = 1 [14 & 16 bit] or

$R1_{(ohms)} = 6 \bullet 10^6 \bullet EG \bullet HYS$

$G2 = \text{Maximum Tracking Rate} \bullet 2^{15}$ [16 bit] or
$G2 = \text{Maximum Tracking Rate} \bullet 2^{13}$ [14 bit] or
$G2 = \text{Maximum Tracking Rate} \bullet 2^{11}$ [12 bit] or
$G2 = \text{Maximum Tracking Rate} \bullet 2^{9}$ [10 bit]

$R3_{(ohms)} = (25 \bullet 10^9)/G2$

$G1 = G^2/(EG \bullet .45 \bullet G2)$

$C2_{(farads)} = 1/(G1 \bullet R1)$

$C3_{(farads)} = C2/10$

$R2_{(ohms)} = 2/(G \bullet C2)$

**** Software Program SW5028-2 available at Aeroflex WEB site.***

RDC5028 EXAMPLE CALCULATIONS

Carrier Frequency = 800 Hz
Nominal Resolver Input Level = 1.3Vrms
Resolution = 14 bits
Closed Loop Bandwidth (BWcl) = 20 Hz
Maximum Tracking Rate in RPS = 1
Hysteresis = 1 LSB

EG = Nominal Resolver Input Level • .011 [14 bit] = 1.3 • .011 = .014
G = 2.22 • BWcl = 2.22 • 20 = 44.4
HYS = 1 [14 bit]

$R1_{(ohms)} = 6 \bullet 10^6 \bullet EG \bullet HYS = 6 \bullet 10^6 \bullet .014 \bullet 1 = 84K$. Use closest standard resistor = 84.5K 1%

$G2 = \text{Maximum Tracking Rate} \bullet 2^{13} = 8192$ [2^{13} for 14 bits]

$R3_{(ohms)} = (25 \bullet 10^9)/G2 = (25 \bullet 10^9)/8192 = 3{,}050K$. Use closest standard resistor = 3.01M 1% or 3M 5%

$G^2 = EG \bullet 0.45 \bullet G1 \bullet G2$

$G1 = G^2/(EG \bullet .45 \bullet G2) = 44.4^2/(.014 \bullet .45 \bullet 8192) = 38.2$

$C2_{(farads)} = 1/(G1 \bullet R1) = 1/(38.2 \bullet 84.5K) = .31\mu F$. Use closest standard capacitor = .33µF 10%

$C3 = C2/10_{(farads)} = C2/10 = .33\mu/10 = .033\mu F$

$R2_{(ohms)} = 2/(G \bullet C2) = 2/(44.4 \bullet .33\mu) = 136.5K$. Use closest standard resistor = 137K 1%

SIGNAL AND REFERENCE INPUT CONDITIONING

Inputs to the converter should be 1.3 Vrms nominal, resolver format referenced to $V_{CC}/2$ nominal Figure 5 shows various input configurations.

REFERENCE CONDITIONING

Most resolvers have a LEADING input to output phase shift. A simple C-R leading phase shift network (Figure 5 – Reference Conditioning) from the resolver reference to the RDC's reference input will provide the compensating phase shift required to bring the signals in phase. If the resolver has a LAGGING input to output phase shift an R-C lagging phase shift network (low pass network) would be required.

Note the C-R phase lead circuit on the input to the Demodulator (BPF1 and BPF2) in Figure 2 should be considered when calculating the total system phase compensation.

The formula for calculating the phase shift network is as follows:

$$\text{Phase angle} = \text{ArcTan}\ \frac{\frac{1}{6.28 \times (R7 + R8) \times C}}{F_{REF}}$$

Select a convenient capacitor value and perform the following calculation to determine the proper resistor value.

$$R = \frac{1}{(\text{Tan}\ (\text{Phase Angle})) \times F_{REF} \times 6.28 \times C}$$

POWER UP INITIALIZATION

The RDC5028 RDC converter can provide incorrect data output if a unit step of 180° (starting at any angle) is introduced to the Sin / Cos input.

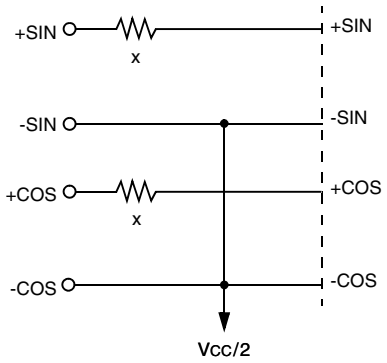
This is difficult to reproduce since a Resolver will never provide a unit step function to the RDC chip.

The only time this would be a concern is during power up, if the Resolver is set to 180°. The RDC will initialize its internal counter to 0000h which simulates the unit step function mentioned above. In practice this error condition during power up is difficult to produce because of the dynamics associated with all the variables when power is first applied.

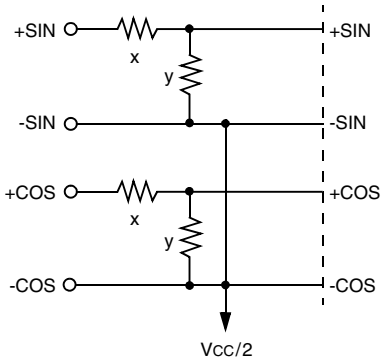
If the system designer does nothing to accommodate this potential problem the system could see an error at power on, however, this error will be self corrected once the Resolver begins to rotate. If the Resolver does not rotate, the error can be corrected by writing to the RDC5028 any angle except 180°.

VELOCITY CONTROL

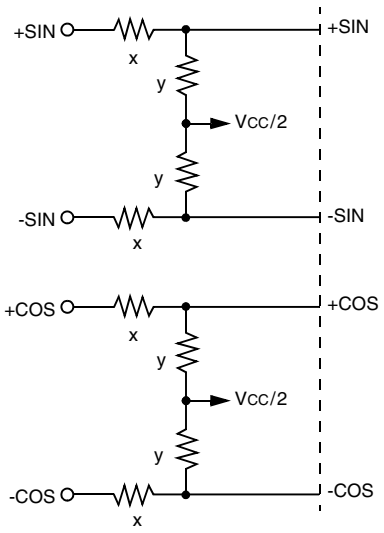
The RDC5028 RDC exhibits nonlinearity below 4 degrees/sec due to an anti-dither circuit that was added to reduce the effects of any noise condition that may exist. This result can be seen in the least significant bit or on the velocity output pins 9 & 10 on this device.



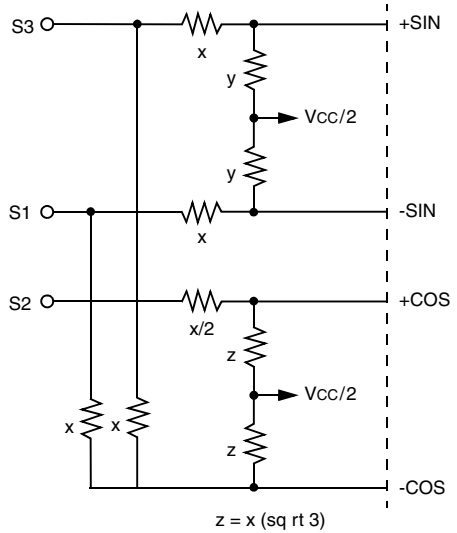
DIRECT RESOLVER



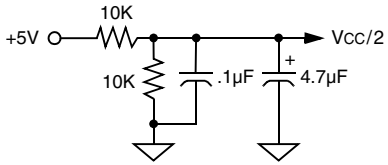
SINGLE ENDED RESOLVER CONDITIONING



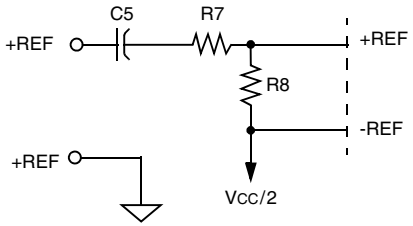
DIFFERENTIAL RESOLVER CONDITIONING



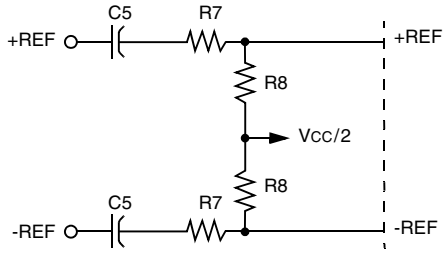
SYNCHRO CONDITIONING



2.5VDC



SINGLE ENDED REFERENCE CONDITIONING



DIFFERENTIAL REFERENCE CONDITIONING (FLOATING REFERENCE)

FIGURE 5 – RDC5028 RESOLVER, SYNCHRO AND REFERENCE INPUT CONFIGURATIONS

READING THE ACT 5028B

The Busy signal is asynchronous to the Read signal created by the interface circuit that reads it. Because of the asynchronous nature of the system (inherent with other Resolver to Digital Converters) the designer must be careful when reading the digital interface.

The implementation of reading the RDC is accomplished in one of two ways, using a CPU/MPU or using an FPGA. The best method for reading the counter may also depend on the rep rate of the counter clock that can vary from 0 to 1µS.

The Busy pulse is instrumental in reading stable data from the RDC5028. The Busy pulse will be present for the following two situations:

1) When ever data is incremented or decremented in the RDC counter.
2) Directly after the trailing positive going edge of /INH (see A within example 5 timing diagram).

Based on 1 above there are many methods that can be implemented to synchronize the reading of data from the RDC5028, below are a few examples:

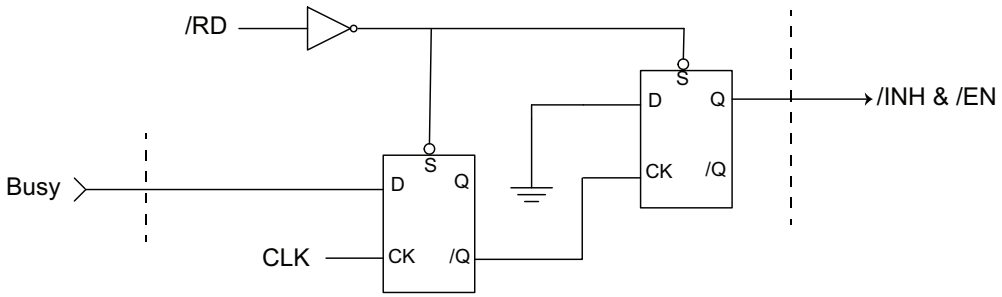
Example 1: If the only time a read will occur is after the RDC has stopped (0 rps) there will be no Busy signal to contend with.

Example 2: Knowing the Busy rep rate an Interrupt to a CPU or Logic can be developed from the Busy pulse for the system to Read the RDC chip as long as the read is guaranteed to occur prior to the next Busy pulse.

Example 3: As long as the resolver is rotating the Busy Pulse can be used to indicate stable data to be sampled on leading or trailing edge.

Example 4: Ignore Busy and perform two reads back to back and compare, if they are equal you have good data. The designer should be aware of the rep rate of Busy which is equal to the clock rate of the counter. In most cases the angular velocity is < 3 rps in which case with a 16 bit counter rep rate would be (1 / 2^{16} * 3) 5µS. In this situation the reads would like to be within 5µs of each other and the LSB would be ignored. Although this method would be easier to implement with a CPU it could also be done in an FPGA.

Example 5: The circuit below ignores the Busy signal but insures sampling of stable data. The clock should be a least 10MHz, the /RD pulse should be a minimum of 1.2µs (to insure minimum /INH pulse width of 400ns), the sampling of data should be taken on the rising edge of the signal /RD. The /RD signal is synced up with the CLK such that the sampling on the D latch occurs on the opposite edge of the /RD transition.



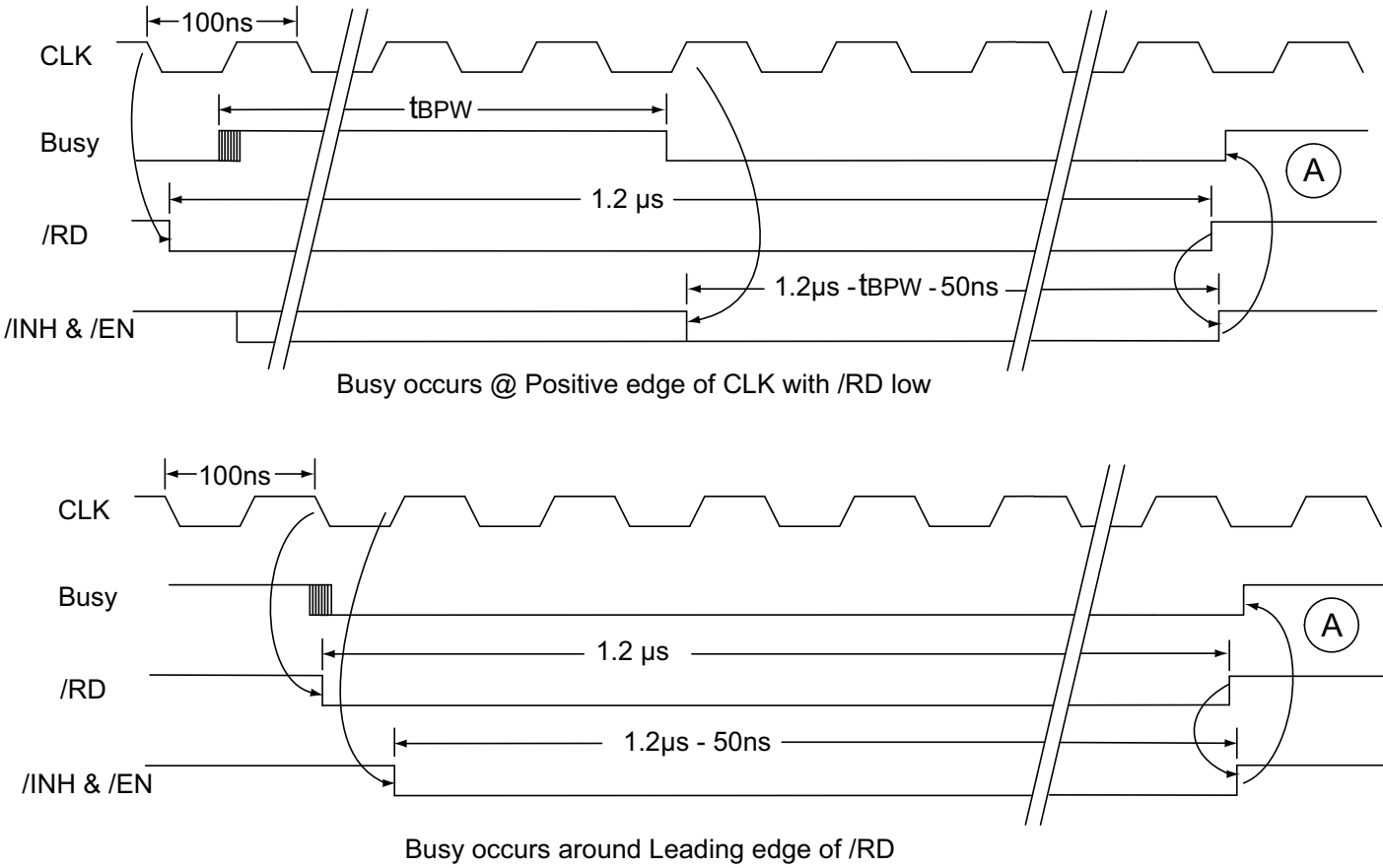


FIGURE 6 – CIRCUIT TIMING WAVEFORMS

TABLE I – RDC5028 PIN OUT DESCRIPTIONS (CQFP PACKAGE)

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	$\overline{\text{DATA LOAD}}$	19	A GND	37	BIT 9
2	VL I/O	20	N/C	38	BIT 10
3	A GND	21	-SIN	39	BIT 11
4	A +5V	22	+SIN	40	BIT 12
5	VCOIN	23	A GND	41	BIT 13
6	INTIN2	24	-COS	42	BIT 14
7	N/C	25	+COS	43	BIT 15
8	INTIN1	26	D GND	44	BIT 16 (LSB)
9	INT1	27	D +5V	45	$\overline{\text{ENABLE}}$
10	INT2	28	BIT 1 (MSB)	46	N/C
11	+REF	29	BIT 2	47	$\overline{\text{INH}}$
12	-REF	30	BIT 3	48	SC2
13	AC2	31	BIT 4	49	SC1
14	AC1	32	BIT 5	50	BUSY
15	BPF2	33	N/C	51	CW/CCW
16	BPF1	34	BIT 6	52	$\overline{\text{RIPPLE}}$
17	DEMOD1	35	BIT 7		
18	DEMOD2	36	BIT 8		

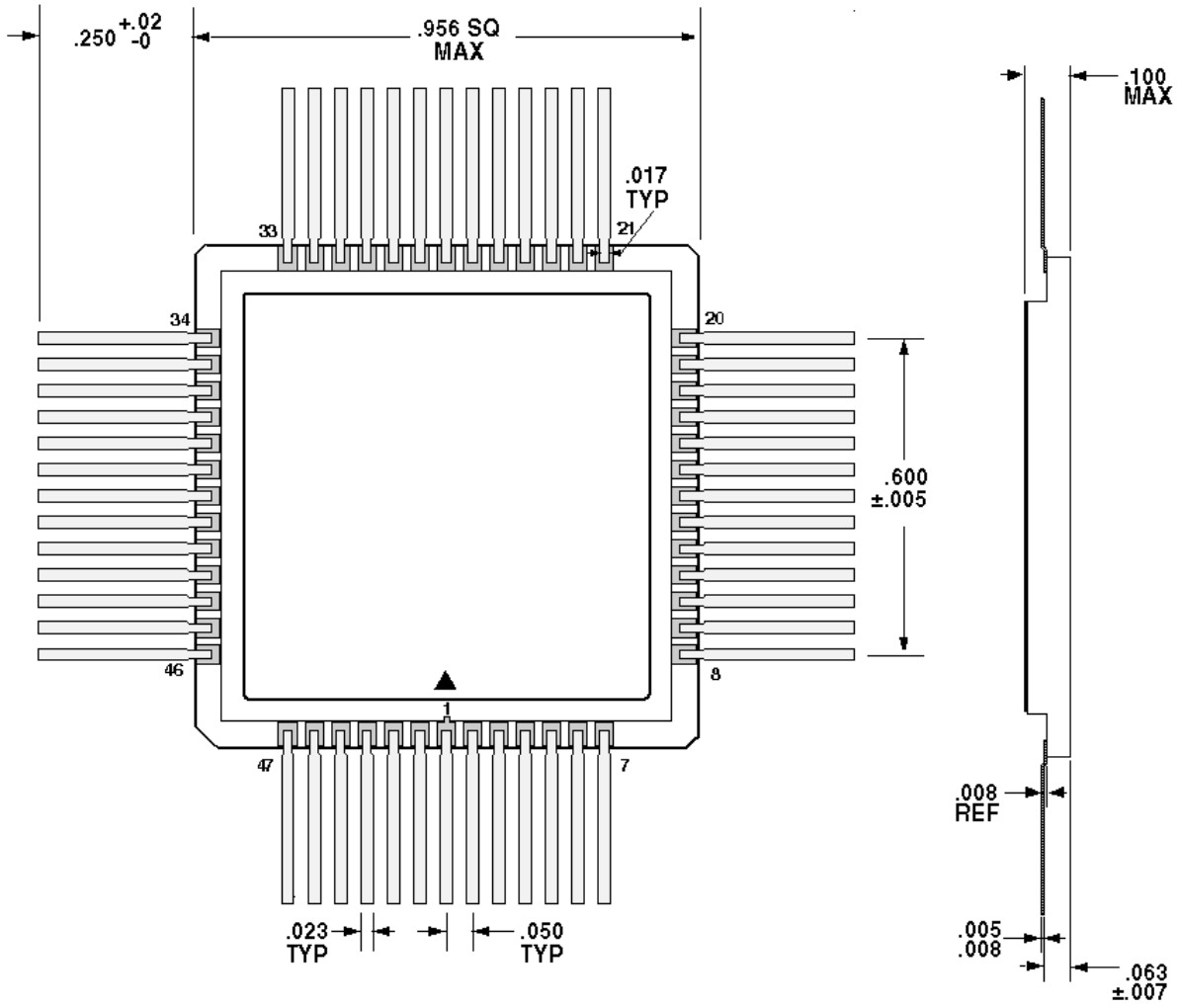


FIGURE 7 – 52 PIN CERAMIC QUAD FLAT PACKAGE (CQFP) OUTLINE

USING INL ERROR CORRECTION FACTORS TO IMPROVE ACCURACY:

The information provided in this section is to address the constant Integral Nonlinearity (INL) that exists at each angle of the RDC5028 Resolver to Digital Converter (RDC). This error is repeatable from chip to chip and provides a look up Table of offsets that can be added to the output of the Resolver to Digital Converter to obtain the 5.3 minute accuracy.

Figure 8 shows the error in Minutes that exists at 2^o increments for the full 360^o. Note that the INL error from 0^o to 180^o is basically the same as the error between 180^o and 360^o. Table II has the angle and correction factor (in Minutes) that must be added to zero out the INL error.

A simple calculation can be performed to derive a correction factor for angles that fall between the angles listed in Table II herein.

AL = Larger Angle
AS = Smaller Angle
CL = Correction Factor associated with larger Angle
CS = Correction Factor associated with smaller Angle
NA = New Angle
NCF = New Correction Factor

Formula:

NCF = CS + (((NA - AS) / (AL - AS)) * (CL - CS))

Example:

Require the correction factor @ 15^o

NCF = 10.17114258 + (((15 – 14) / (16 – 14)) * (11.11376953 - 10.17114258))
NCF = 10.17114258 + (((1) / (2)) * .94262695)
NCF = 10.17114258 + (.5 * .94262695)
NCF = 10.17114258 + .471313475
NCF = 10.64245606 minutes

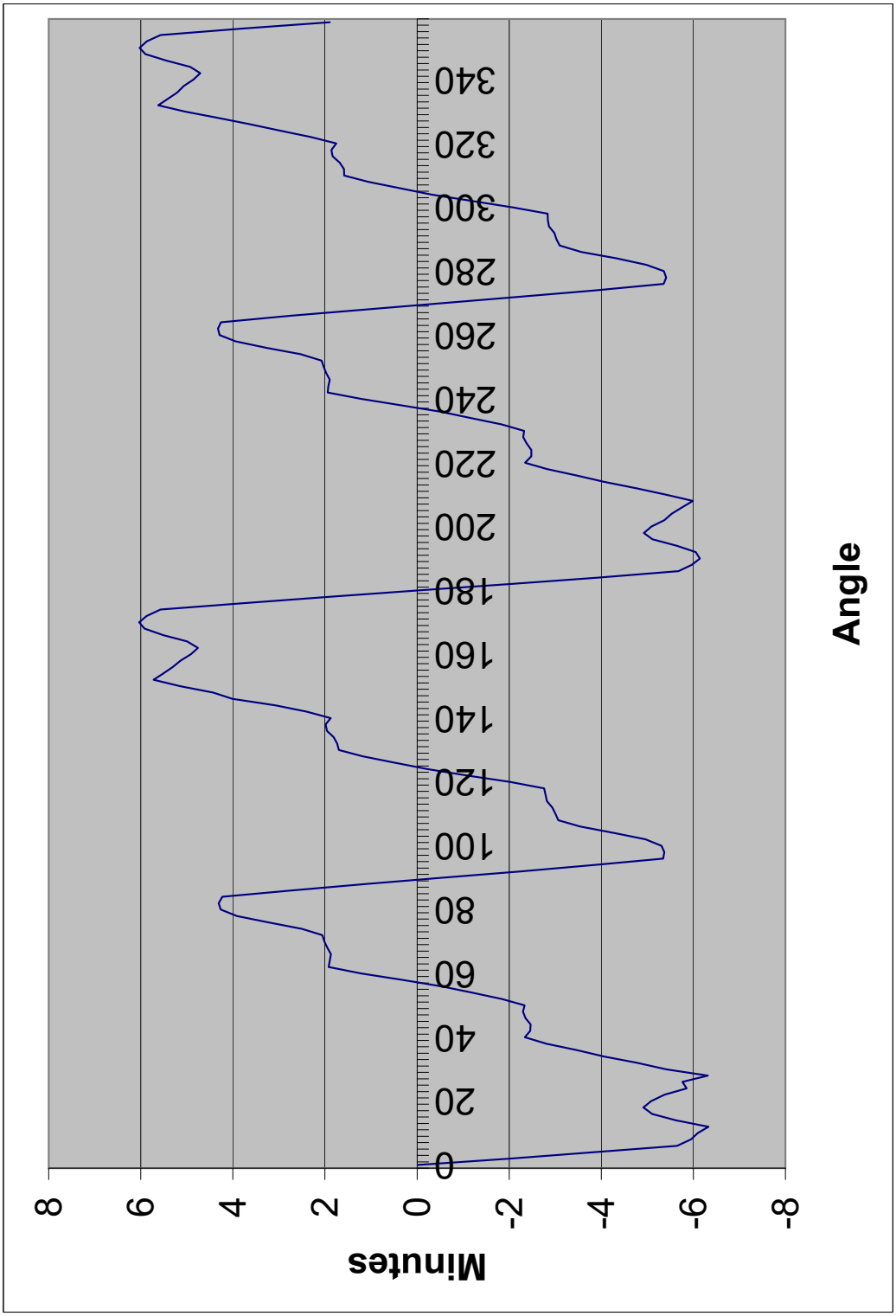


FIGURE 8 – ANGLE ERROR CHART

TABLE II – CORRECTION FACTORS (MINUTES)

Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor
0	0.020387	90	0.557245	180	0.018688	270	0.535159
2	2.013632	92	2.253179	182	2.047610	272	2.242985
4	3.864167	94	3.867565	184	3.923629	274	3.864167
6	5.646746	96	5.342640	186	5.679026	276	5.356231
8	5.951268	98	5.370238	188	5.963160	278	5.411012
10	6.097790	100	5.311191	190	6.140263	280	5.360460
12	6.327559	102	4.961630	192	6.050635	282	4.982017
14	5.617827	104	4.284177	194	5.641612	284	4.331747
16	5.106868	106	3.543865	196	5.111965	286	3.572746
18	4.917005	108	3.066884	198	4.923800	288	3.095766
20	5.080516	110	3.004440	200	5.094107	290	3.026526
22	5.374844	112	2.936898	202	5.368048	292	2.981070
24	5.856053	114	2.821787	204	5.533258	294	2.864260
26	5.761329	116	2.789923	206	5.751135	296	2.840891
28	6.313892	118	2.758059	208	5.989399	298	2.836209
30	5.408785	120	2.010951	210	5.400290	300	2.075510
32	4.777203	122	1.092252	212	4.768708	302	1.180596
34	4.060675	124	0.222822	214	4.062374	304	0.317962
36	3.463072	126	-0.47841	216	3.471566	306	-0.38497
38	2.811103	128	-1.18305	218	2.821297	308	-1.06413
40	2.339220	130	-1.69741	220	2.346015	310	-1.58528
42	2.458559	132	-1.73267	222	2.480645	312	-1.58996
44	2.467469	134	-1.81210	224	2.479361	314	-1.67959
46	2.354057	136	-1.95779	226	2.381239	316	-1.83547
48	2.300107	138	-1.98626	228	2.305203	318	-1.86054
50	2.332801	140	-1.87711	230	2.326006	320	-1.75479
52	1.849025	142	-2.40166	232	1.837133	322	-2.29293
54	1.188562	144	-3.07912	234	1.171573	324	-2.97718
56	0.523002	146	-4.01311	236	0.497518	326	-3.61556
58	-0.33114	148	-4.43062	238	-0.34473	328	-4.32699
60	-1.21076	150	-5.13696	240	-1.22435	330	-5.04352
62	-1.92219	152	-5.72437	242	-1.94088	332	-5.62413
64	-1.89799	154	-5.51329	244	-1.92687	334	-5.40795
66	-1.87039	156	-5.30390	246	-1.89418	336	-5.20707
68	-1.94813	158	-5.13530	248	-1.97361	338	-5.06734
70	-2.01057	160	-4.91062	250	-2.02926	340	-4.86136
72	-2.05603	162	-4.76070	252	-2.07132	342	-4.70974
74	-2.50413	164	-4.99474	254	-2.52961	344	-4.92339
76	-3.23255	166	-5.51759	256	-3.26992	346	-5.45983
78	-3.90830	168	-5.92152	258	-3.94058	348	-5.90113
80	-4.26466	170	-6.03663	260	-4.29014	350	-6.02644
82	-4.31011	172	-5.87312	262	-4.32540	352	-5.86972
84	-4.22645	174	-5.57369	264	-4.25703	354	-5.57199
86	-2.72929	176	-3.78432	266	-2.75308	356	-3.78602
88	-1.10131	178	-1.88282	268	-1.11321	358	-1.89811

ORDERING INFORMATION

MODEL	DLA SMD #	SCREENING	PACKAGE
RDC5028-3-1-7 1/	-	Commercial Flow, +25°C testing only	CQFP
RDC5028-3-1-S 1/		Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
RDC5028-301-1S RDC5028-301-2S	5962-0423503KXC 5962-0423503KXA	In accordance with DLA SMD	
RDC5028-931-1S RDC5028-931-2S	5962H0423503KXC 5962H0423503KXA	In accordance with DLA Certified RHA Program Plan to RHA Level "H", 1 Mrad(Si)	
RDC5028, Evaluation board 2/	-	-	-

Notes

1/ Dash #'s:

The first dash number indicates the revision of silicon:

-3 = Rev. C

The second dash number indicates the wafer lot run.

-1 = First diffusion lot

2/ See Application note AN5028-1

EXPORT CONTROL:

This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Department of State is required prior to the export of this product from the United States.

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