Standard Products

VRG8691/92
Adjustable 7.5A Positive LDO Regulator
Radiation Tolerant

www.aeroflex.com/voltreg

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FEATURES

- Radiation performance
  - Total dose: 100 krads(Si), Dose rate = 50 - 300 rads(Si)/s
- Output voltage adjustable: 1.0V to 3.3V
- Output current: 7.5A
- Dropout voltage: 0.5V at 7.5Amps
- Voltage reference: 1.0V ±0.5%
- Load regulation: 0.5% max
- Line regulation: 0.2% max
- Ripple rejection: >80dB
- Enable Input - TTL / CMOS Compatible
- Slow Start capability
- Stable with multiple ceramic output capacitors
- Packaging – Hermetic metal
  - Thru-hole or Surface mount
  - 12 Leads, 0.900"L x 1.000"W x .205"Ht
  - Power package
  - Weight - 18 gm max
- Designed for aerospace and high reliability space applications
- **Aeroflex Plainview's Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.**

DESCRIPTION

The Aeroflex Plainview VRG8691/92 is capable of supplying in excess of 7.5Amps over the output voltage range as defined under recommended operating conditions. The regulator is exceptionally easy to set-up, requiring only 2 external resistors to set the output voltage. The module design has been optimized for excellent regulation and low drop-out voltage. Figures 2 through 5 illustrate setting output voltage, setting current limits and choosing a slow start capacitor. The VRG8691/92 serves a wide variety of applications including local on-card regulation, programmable output voltage regulation or precision current regulation.

The VRG8691/92 has been specifically designed to meet exposure to radiation environments. The VRG8691 is configured for a Thru-Hole 12 lead metal power package and the VRG8692 is configured for a Surface Mount 12 lead metal power package. It is guaranteed operational from -55°C to +125°C. Available screened to MIL-STD-883, the VRG8691/92 is ideal for demanding military and space applications.

CURRENT LIMIT (ICL)

The VRG8691/92 features internal current limiting making them virtually blowout-proof against overloads. The limit is nominally 11.5A @ Vin = 5V (see Table 2), but may be increased or decreased with the addition of one external resistor (see Application Note 2). When the load current exceeds the ICL setting, the output of the VRG8691/92 will be latched in an OFF state. To reset the latch condition, the $\overline{\text{ENABLE}}$ function (pin 5) can be cycled, enabled - disabled - enabled, or the VBIAS may be cycled ON - OFF - ON (if the Figure 5 configuration is being utilized).

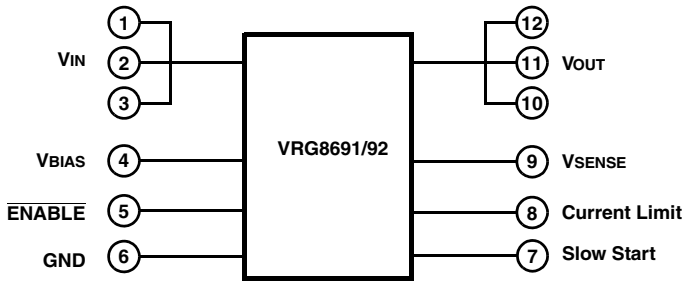


FIGURE 1 – BLOCK DIAGRAM / SCHEMATIC

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RANGE	UNITS
Operating (Junction) Temperature Range	-55 to +150	℃
Lead Temperature (soldering, 10 sec)	300	℃
Storage Temperature Range	-65 to +150	℃
V_{BIAS}, V_{IN}	7	V
Thermal Resistance (Junction to case Θ_{JC})	1	°C/W
Power	25 1/	W

1/ Based on pass transistor limitations of (V_{IN} - V_O) x I_O and Θ_{JC} < 1℃/W with 25℃ max T_J rise and T_C = +125℃.

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may effect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RANGE	UNITS
Output Voltage Range	1.0 to 3.3	V_{DC}
Case Operating Temperature Range	-55 to +125	℃
Output Current	0 to 7.5	A
V_{BIAS}	3.3 to 5.5 1/	V_{DC}
V_{IN}	1.8 to 5.5 2/	V_{DC}

1/ V_{BIAS} must maintain a level equal or above V_{IN} but not fall below 3.3V
2/ Depending upon V_{OUT} setting.

ELECTRICAL PERFORMANCE CHARACTERISTICS 1/

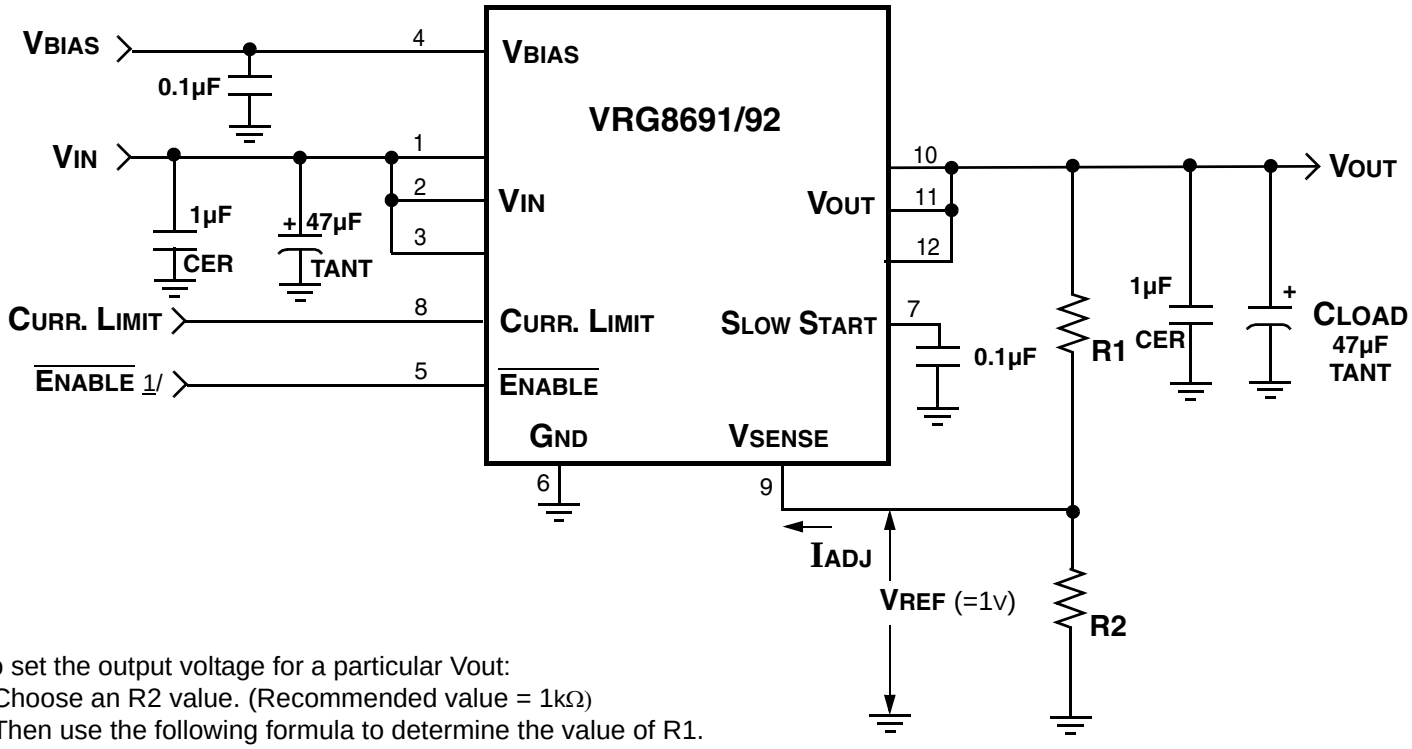
PARAMETER	SYM	CONDITIONS	MIN	MAX	UNITS
Reference Voltage	V_{REF}	V_{IN} = V_{BIAS} = 5V, $\overline{ENABLE}$ = 0, 0A ≤ I_{OUT} ≤ 7.5A	0.995	1.005	V
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	2V ≤ V_{IN} ≤ 3V, V_{OUT} = 1.0V, C_{IN} ≥ 47µF, 4.3V ≤ V_{IN} ≤ 5.3V, V_{OUT} = 3.3V, C_{OUT} ≥ 47µF,	-	0.2	%/V
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	0A ≤ I_{OUT} ≤ 7.5A, C_{IN} ≥ 47µF, C_{OUT} ≥ 47µF,	-	0.5	%
Ripple Rejection Ratio		f = 120Hz, C_{LOAD} = 47µF, V_{IN} + V_{RIP} ≥ V_{OUT} + $V_{DROP(MAX)}$ @ 5A, V_{IN} = 4.3V, V_{RIP} = 1V_{P-P}, V_{OUT} = 3.3V	80	-	dB
Dropout Voltage	V_{DROP}	@ΔV_{OUT} = 1%, 0A ≤ I_{OUT} ≤ 7.5A	-	0.5	V
Adjustment Pin Current	I_{ADJ}		-	3	µA
Minimum Load Current	I_{MIN}		-	0	mA
Current Limit 2/	I_{CL}		9.5	13.5	A
Long Term Stability 3/	$\frac{\Delta V_{OUT}}{\Delta TIME}$		-	1	%
Supply Current (V_{BIAS})	I_{BIAS}		-	15	mA

Notes:
1/ Unless otherwise specified, these specifications apply for post radiation: V_{BIAS} = V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 7.5A and -55℃ < Tc <+125℃, Min Input/Output capacity of 47µF Tant with 1µF ceramic in parallel.
2/ Current Limit is adjustable as shown in Application Note 2, Figures 3 and 4.
3/ Not tested. Shall be guaranteed to the specified limits after 1000hr life test.

APPLICATION NOTE 1

BASIC SET-UP

Setting the output voltage (VOUT):



To set the output voltage for a particular Vout:
- Choose an R2 value. (Recommended value = 1kΩ)
- Then use the following formula to determine the value of R1.

$$R1 = R2 \times \frac{V_{OUT} - V_{REF}}{(R2 \times I_{ADJ}) + V_{REF}}$$, where V_{REF} = 1v, I_{ADJ} typ = 0.2uA

Table 1 shows example values for R1 and R2 to achieve some standard voltages.
Table 2 shows the nominal current limit settings if the 'CURR. LIMIT' function (pin 8) is left open.

Table 1
Example R1 & R2 for typical VOUT

VOUT	R2	R1
3.3V	1kΩ	2.3kΩ
2.5V	1kΩ	1.5kΩ
1.8V	1kΩ	800Ω
1.0V	1kΩ	0Ω

Table 2
2/

VIN	ICL NOM
5V	11.5A
3.3V	7.5A
2.5V	5.7A
1.8V	4.1A

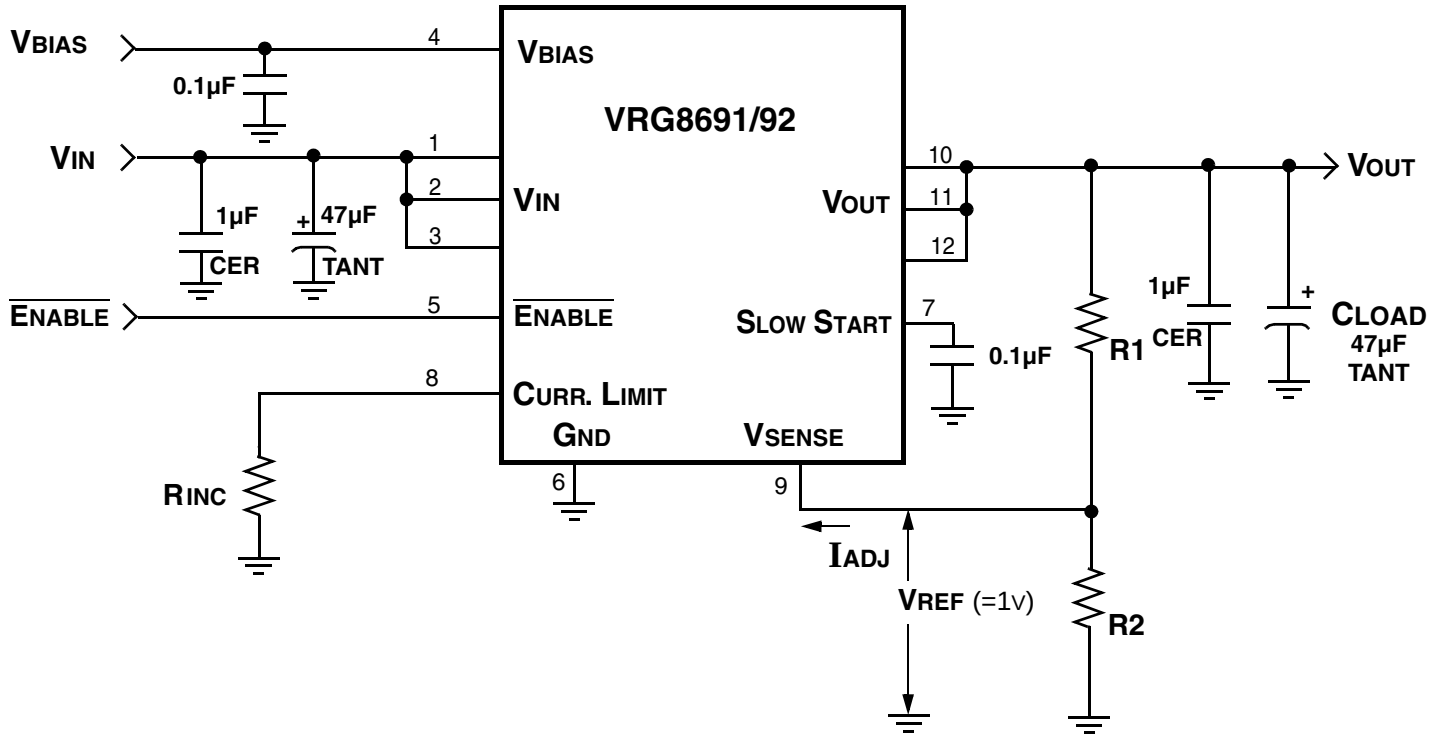
Notes:
1/ $\overline{\text{ENABLE}}$ should be asserted after both VIN and VBIAS are applied.
(See Application Note 3, Figure 5 for the configuration where a separate $\overline{\text{ENABLE}}$ control line is NOT required).
2/ ICL varies directly with VIN.
(See Application Note 2 for adjusting the Current Limit, ICL).

FIGURE 2 –SETTING OUTPUT VOLTAGE

APPLICATION NOTE 2

SETTING THE CURRENT LIMIT

To Increase the Current Limit (ICL):



- If the 'CURR. LIMIT' function (pin 8) is left open, the ICL decreases from 11.5 A(NOM) as VIN is decreased from 5V (Table 3).

Table 3

VIN	RINC	ICL NOM
5V	Open	11.5 A
3.3V	Open	7.5 A
2.5V	Open	5.7 A
1.8V	Open	4.1 A

- To increase the current limit above the nominal setting for any VIN and ICL combination, use the following formula:

$$R_{INC}(\text{K-OHMS}) = \frac{30 \times V_{IN}}{\left(\frac{30 \times I_{CL}}{69}\right) - V_{IN}}$$

- To maintain ICL at the 11.5 A setting, for commonly found VIN voltages, apply RINC value found in Table 4.

Table 4

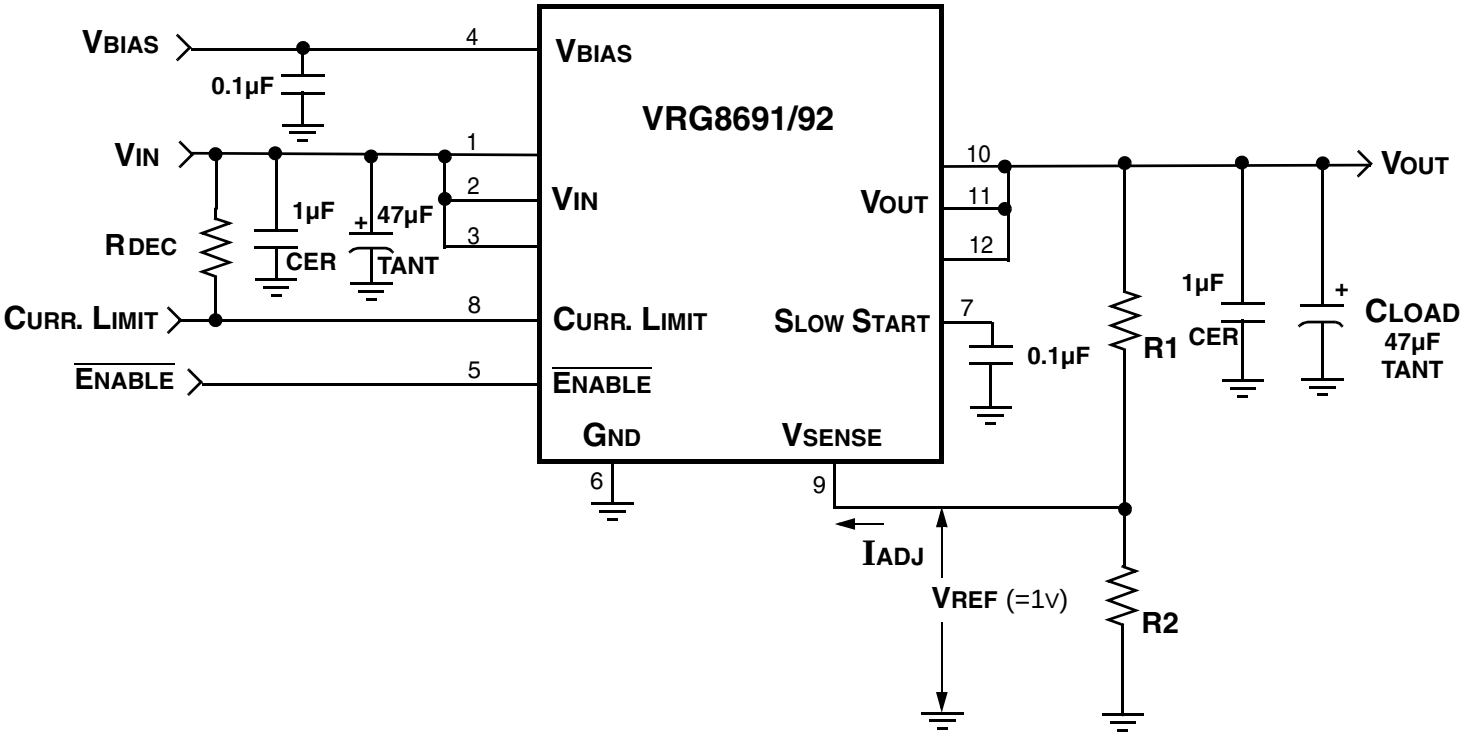
VIN	RINC	ICL NOM
5V	Open	11.5 A
3.3V	56kΩ	11.5 A
2.5V	30kΩ	11.5 A
1.8V	16kΩ	11.5 A

FIGURE 3 – INCREASING THE CURRENT LIMIT (ICL)

APPLICATION NOTE 2 (CONTINUED)

SETTING THE CURRENT LIMIT

To Decrease the Current Limit (ICL):



- As shown in Table 3, if the 'CURR. LIMIT' function (pin 8) is left open, the ICL decreases from 11.5 A(NOM) as VIN is decreased from 5V.

- To achieve any ICL, less than nominal, use RDEC which can be calculated using the following formula:

$$R_{DEC(K\text{-}OHMS)} = \frac{31 \times V_{IN}}{\left(\frac{69 \times V_{IN}}{30}\right) - I_{CL}}$$

FIGURE 4 – DECREASING THE CURRENT LIMIT (ICL)

APPLICATION NOTE 3

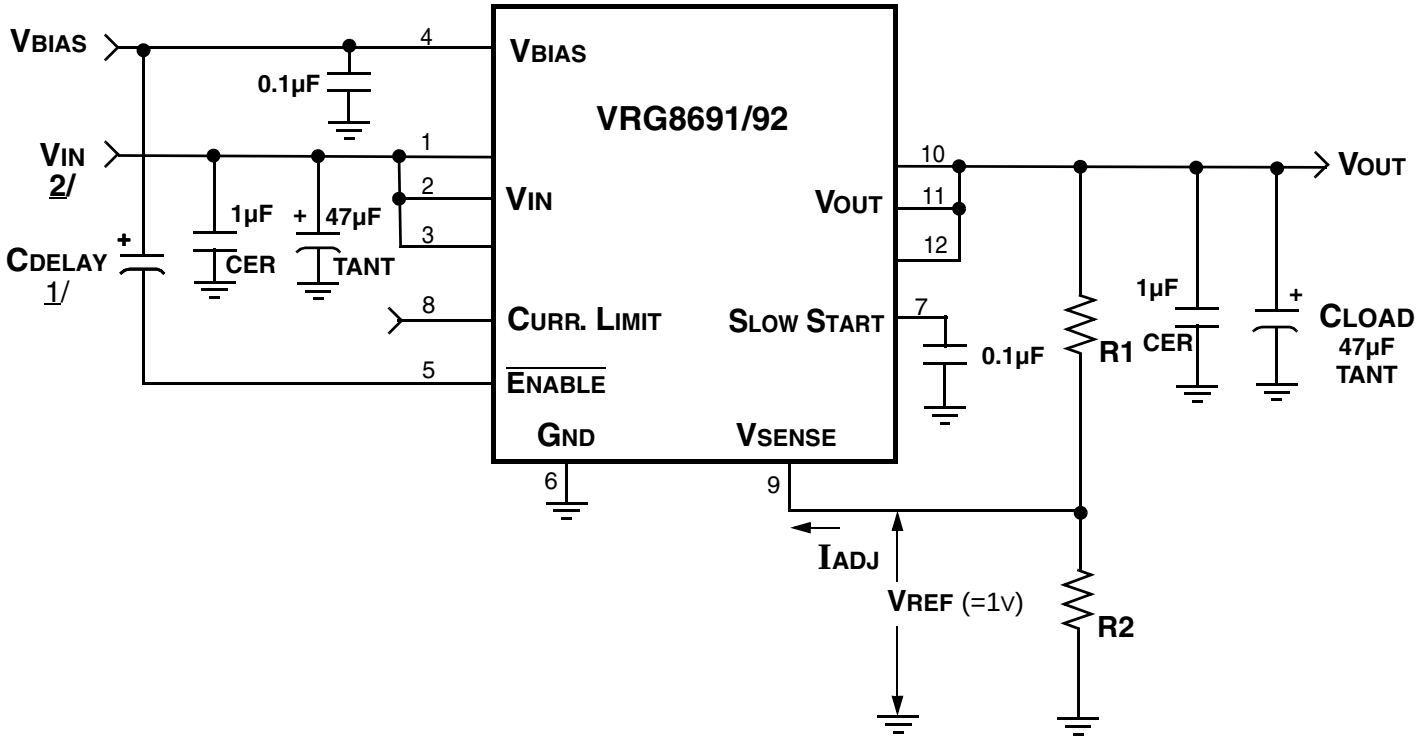
START UP SEQUENCE

Recommended Power Supply Sequencing Options:

- OPTION 1: Controlling the $\overline{\text{ENABLE}}$ line with a Digital signal (TTL / CMOS compatible).
  - Prior to applying power, disable the regulator by setting the $\overline{\text{ENABLE}}$ control line to a HIGH state.
  - Apply V_{IN} and V_{BIAS}. 1/
  - Wait until both V_{IN} and V_{BIAS} supplies have reached their operating levels.
  - Toggle the $\overline{\text{ENABLE}}$ control line to a LOW state to turn on V_{OUT} of the regulator.

- OPTION 2: Controlling the $\overline{\text{ENABLE}}$ line using the C_{DELAY} feature.
  - Connect a C_{DELAY} capacitor between V_{BIAS} and the $\overline{\text{ENABLE}}$ as shown in Figure 5 below. 2/
  - Apply V_{IN} and V_{BIAS}. 1/
  - C_{DELAY} causes the regulator to self-enable after V_{BIAS} has reached operating level.

NOTE: The $\overline{\text{ENABLE}}$ should always be asserted AFTER V_{IN} and V_{BIAS} have reached operating level.



NOTES:

1/ V_{IN} should be applied before V_{BIAS} if the Slow Start feature is used.

2/ C_{DELAY} capacitor of 10uF is adequate for V_{BIAS} rise times of up to 50ms.

FIGURE 5 – DELAYED ENABLE

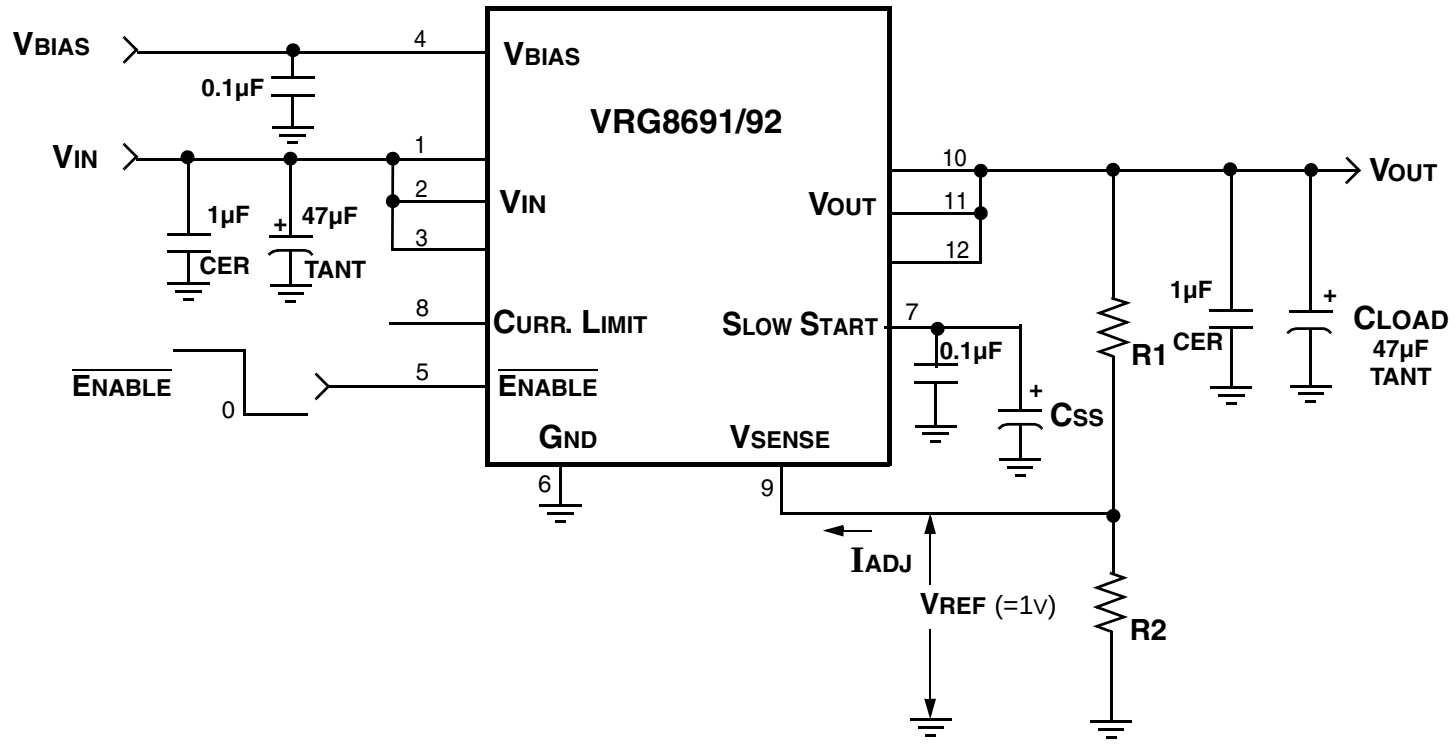
APPLICATION NOTE 4

VOUT START UP RISE TIME CONTROL

Utilizing the Slow Start option:

When the VRG8691/92 is first powered up, using the Slow Start function controls the rate at which VOUT rises to the required voltage set by R1 and R2.

Note: VIN should be applied before VBIAS when the Slow Start feature is used.



If it is desirable to control the output rise time, a capacitor (CSS) can be asserted on the Slow Start pin to adjust the rise time for the following:

A. Large load capacitance will cause high surge currents which will trip the current limit circuitry.
The use of CSS will allow the output voltage to rise slowly thus mitigate the surge current phenomenon.

$$\frac{C_{SS}}{C_{LOAD}} > \frac{V_{OUT\ NOM}}{I_{CL} - I_{LOAD\ NOM}} \times \frac{0.4 \times V_{BIAS}}{1300}$$

B. CSS may be used solely to control VOUT RISE TIME (Tr), when CLOAD is not an issue.

$$T_R = C_{SS} \times 1300 \times LN\left(\frac{V_{BIAS}}{V_{BIAS} - 2.5}\right)$$

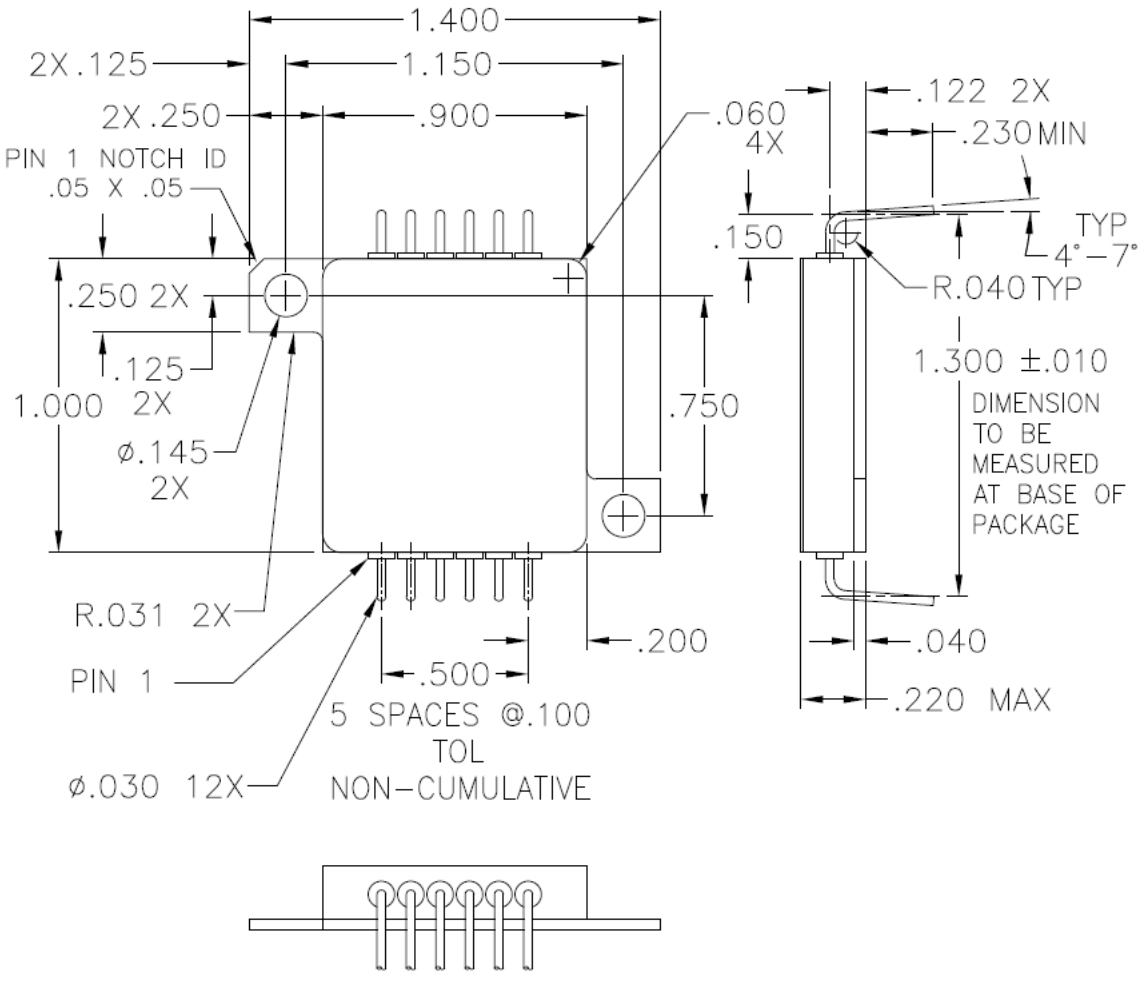
Note: CSS in Farads and TR in seconds.

C. CSS is effective only when VIN is applied prior to VBIAS or $\overline{\text{ENABLE}}$.

FIGURE 6 – SLOW START

PIN NUMBERS vs FUNCTION

PIN	FUNCTION	PIN	FUNCTION
1	VIN	7	Slow Start
2	VIN	8	Current Limit
3	VIN	9	VSENSE
4	VBIAS	10	VOUT
5	$\overline{\text{ENABLE}}$	11	VOUT
6	GROUND	12	VOUT

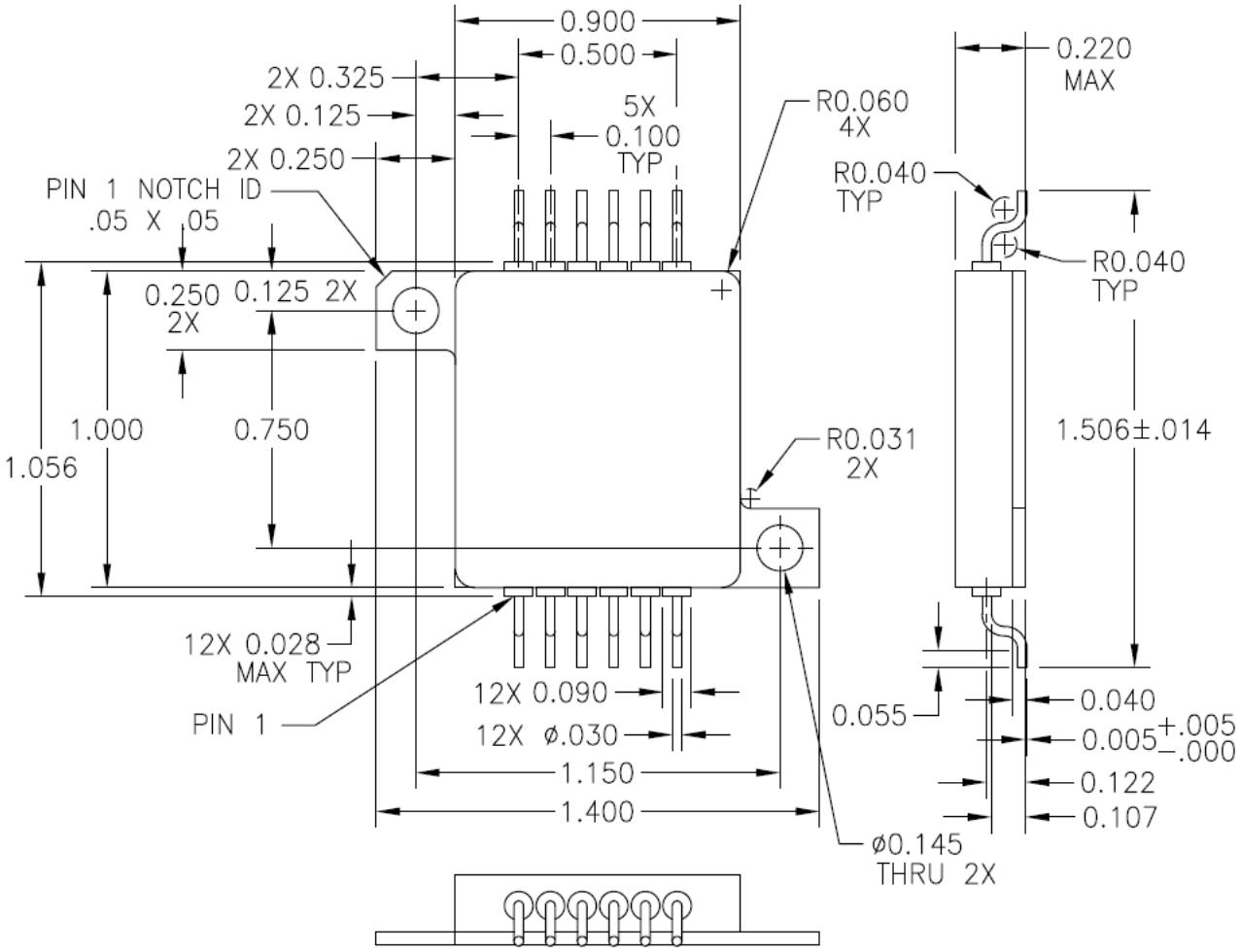


Notes:
1. Dimension Tolerance: ±.005 inches
2. Package contains BeO substrate
3. Case electrically isolated

FIGURE 3 – PACKAGE OUTLINE — VRG8691 THRU-HOLE POWER PACKAGE

PIN NUMBERS vs FUNCTION

PIN	FUNCTION	PIN	FUNCTION
1	VIN	7	Slow Start
2	VIN	8	Current Limit
3	VIN	9	VSENSE
4	VBIAS	10	VOUT
5	$\overline{\text{ENABLE}}$	11	VOUT
6	GROUND	12	VOUT



Notes:
1. Dimension Tolerance: ±.005 inches
2. Package contains BeO substrate
3. Case electrically isolated

FIGURE 4 – PACKAGE OUTLINE — VRG8692 SURFACE MOUNT POWER PACKAGE

ORDERING INFORMATION

MODEL	DLA SMD #	SCREENING	PACKAGE
VRG8691-7	-	Commercial Flow, +25℃ testing only	12 Lead Thru-Hole Power Pkg
VRG8691-S	-	Military Temperature, -55℃ to +125℃ Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
VRG8691-201-1S	5962-0923701KXC	DLA SMD Pending	
VRG8691-201-2S	5962-0923701KXA		
VRG8692-7	-	Commercial Flow, +25℃ testing only	12 Lead Surface Mount Power Pkg
VRG8692-S	-	Military Temperature, -55℃ to +125℃ Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
VRG8692-201-1S	5962-0923701KYC	DLA SMD Pending	
VRG8692-201-2S	5962-0923701KYA		

EXPORT CONTROL:

This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Department of State is required prior to the export of this product from the United States.

EXPORT WARNING:

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PLAINVIEW, NEW YORK
Toll Free: 800-THE-1553
Fax: 516-694-6715

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC
Tel: 321-951-4164
Fax: 321-951-4254

WEST COAST
Tel: 949-362-2260
Fax: 949-362-2266

CENTRAL
Tel: 719-594-8017
Fax: 719-594-8468

www.aeroflex.com info-ams@aeroflex.com

AEROFLEX
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Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused