IS61WV20488ALL
IS61/64WV20488BLL

2M x 8 HIGH-SPEED CMOS STATIC RAM

AUGUST 2010

FEATURES

- High-speed access times:
  8, 10, 20 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- $\overline{CE}$ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single power supply
  - V_{DD} 1.65V to 2.2V (IS61WV20488ALL)
    speed = 20ns for Vcc = 1.65V to 2.2V
  - V_{DD} 2.4V to 3.6V (IS61/64WV20488BLL)
    speed = 10ns for Vcc = 2.4V to 3.6V
    speed = 8ns for Vcc = 3.3V $\pm$ 5%
- Packages available:
  - 48-ball miniBGA (9mm x 11mm)
  - 44-pin TSOP (Type II)
- Industrial and Automotive Temperature Support
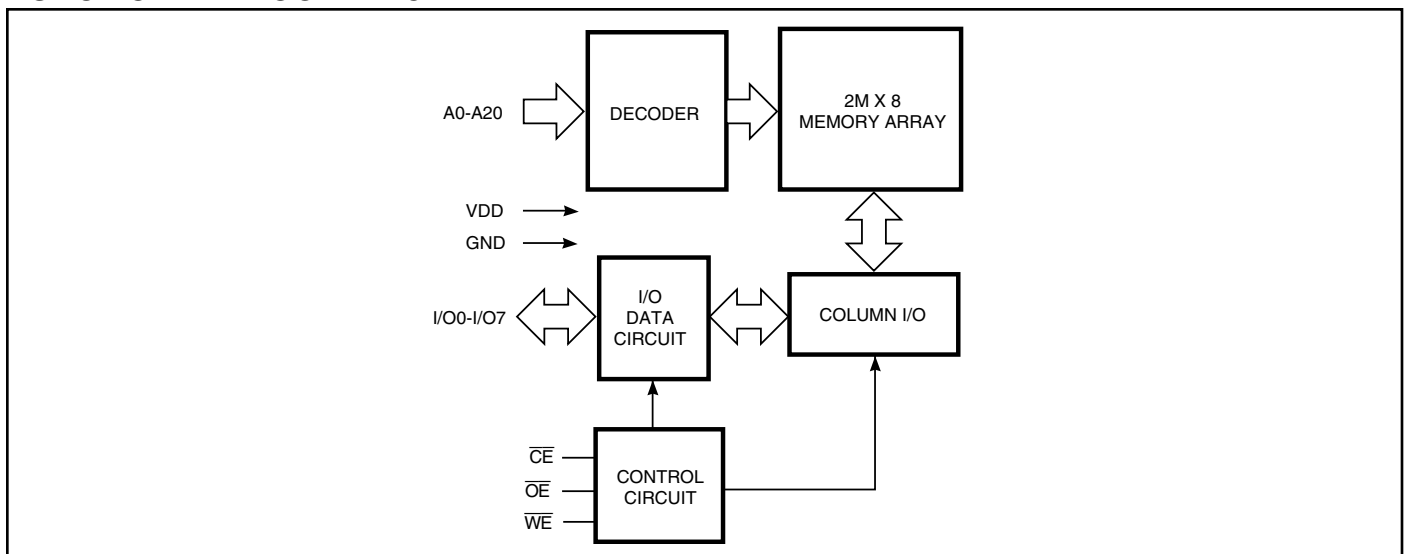- Lead-free available

DESCRIPTION

The *ISSI* IS61WV20488ALL/BLL and IS64WV20488BLL are very high-speed, low power, 2M-word by 8-bit CMOS static RAM. The IS61WV20488ALL/BLL and IS64WV20488BLL are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

The IS61WV20488ALL/BLL and IS64WV20488BLL operate from a single power supply and all inputs are TTL-compatible.

The IS61WV20488ALL/BLL and IS64WV20488BLL are available in 48 ball mini BGA and 44-pin TSOP (Type II) packages.
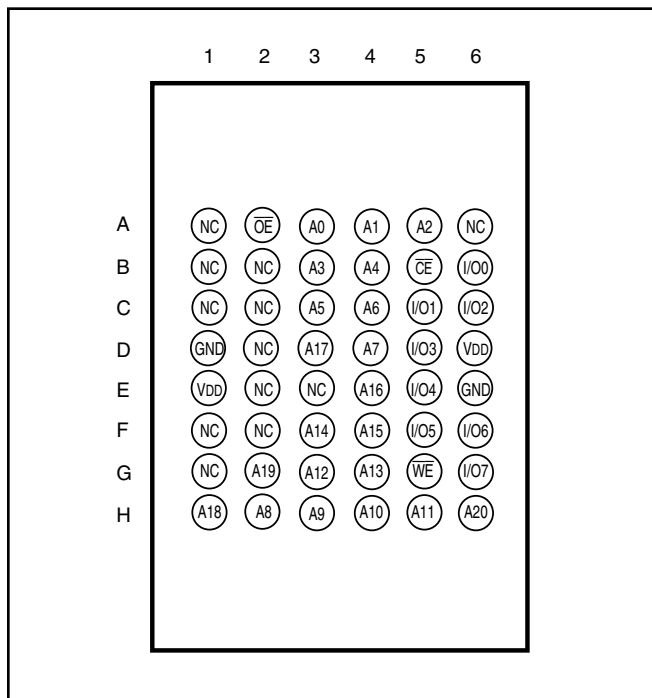
FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

48-pin Mini BGA (M) (9mm x 11mm)

	1	2	3	4	5	6
A	NC	$\overline{OE}$	A0	A1	A2	NC
B	NC	NC	A3	A4	$\overline{CE}$	I/O0
C	NC	NC	A5	A6	I/O1	I/O2
D	GND	NC	A17	A7	I/O3	VDD
E	VDD	NC	NC	A16	I/O4	GND
F	NC	NC	A14	A15	I/O5	I/O6
G	NC	A19	A12	A13	$\overline{WE}$	I/O7
H	A18	A8	A9	A10	A11	A20

44-pin TSOP (Type II)

Left	Pin		Pin	Right
NC	1		44	NC
NC	2		43	NC
A0	3		42	A20
A1	4		41	A18
A2	5		40	A17
A3	6		39	A16
A4	7		38	A15
$\overline{CE}$	8		37	$\overline{OE}$
I/O0	9		36	I/O7
I/O1	10		35	I/O6
VDD	11		34	GND
GND	12		33	VDD
I/O2	13		32	I/O5
I/O3	14		31	I/O4
$\overline{WE}$	15		30	A14
A5	16		29	A13
A6	17		28	A12
A7	18		27	A11
A8	19		26	A10
A9	20		25	A19
NC	21		24	NC
NC	22		23	NC

PIN DESCRIPTIONS

A0-A20	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Data Input / Output
V_{DD}	Power
GND	Ground
NC	No Connection

TRUTH TABLE

Mode	$\overline{\text{WE}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to V_{DD} + 0.5	V
V_{DD}	V_{DD} Relates to GND	−0.3 to 4.0	V
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

OPERATING RANGE (V$_{DD}$) (IS61WV20488ALL)

Range	Ambient Temperature	V$_{DD}$ (20 ns)
Commercial	0°C to +70°C	1.65V-2.2V
Industrial	−40°C to +85°C	1.65V-2.2V
Automotive	−40°C to +125°C	1.65V-2.2V

OPERATING RANGE (V$_{DD}$) (IS61WV20488BLL)[1]

Range	Ambient Temperature	V$_{DD}$ (8 ns)	V$_{DD}$ (10 ns)
Commercial	0°C to +70°C	3.3V $\pm$ 5%	2.4V-3.6V
Industrial	−40°C to +85°C	3.3V $\pm$ 5%	2.4V-3.6V

Note:
1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V $\pm$ 5%, the device meets 8ns.

OPERATING RANGE (V$_{DD}$) (IS64WV20488BLL)

Range	Ambient Temperature	V$_{DD}$ (10 ns)
Automotive	−40°C to +125°C	2.4V-3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width 2.0 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width 2.0 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	1.8	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width 2.0 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width 2.0 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.65V-2.2V

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
V_{IL}[1]	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width 2.0 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width 2.0 ns). Not 100% tested.

AC TEST CONDITIONS (HIGH SPEED)

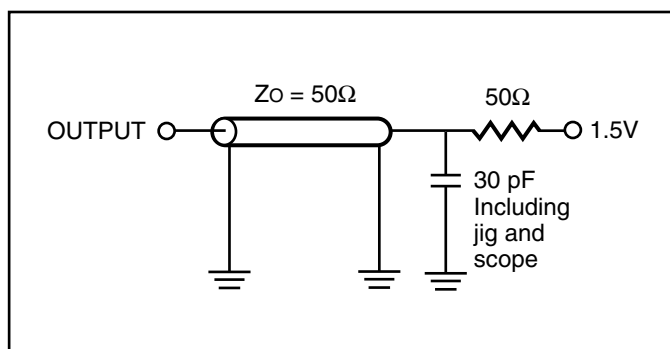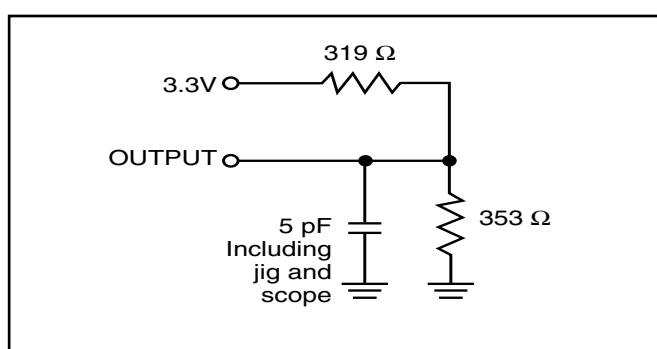| Parameter	Unit (2.4V-3.6V)	Unit (3.3V $\pm$ 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to V_{DD}-0.3V	0.4V to V_{DD}-0.3V	0.4V to V_{DD}-0.2V
Input Rise and Fall Times	1.5ns	1.5ns	1.5ns
Input and Output Timing and Reference Level (V_{Ref})	$V_{DD}/2$	$V_{DD}/2 + 0.05$	$V_{DD}/2$
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2

AC TEST LOADS

Figure 1.

Figure 2.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 Min.	-8 Max.	-10 Min.	-10 Max.	-20 Min.	-20 Max.	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	120	—	95	—	90	mA
			Ind.	—	125	—	100	—	100	
			Auto.	—	—	—	140	—	140	
			typ.[2]		60					
I_{CC1}	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = 0	Com.	—	35	—	30	—	30	mA
			Ind.	—	35	—	40	—	40	
			Auto.	—	—	—	60	—	70	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	30	—	30	—	30	mA
			Ind.	—	35	—	35	—	35	
			Auto.	—	—	—	70	—	70	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD}$ – 0.2V, $V_{IN} \geq V_{DD}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com.	—	20	—	20	—	15	mA
			Ind.	—	25	—	25	—	20	
			Auto.	—	—	—	70	—	70	
			typ.[2]		4					

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8 Min.	-8 Max.	-10 Min.	-10 Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	ns
t_{AA}	Address Access Time	—	8	—	10	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5.5	—	6.5	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	3	—	4	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	3	0	4	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{PU}	Power Up Time	0	—	0	—	ns
t_{PD}	Power Down Time	—	8	—	10	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

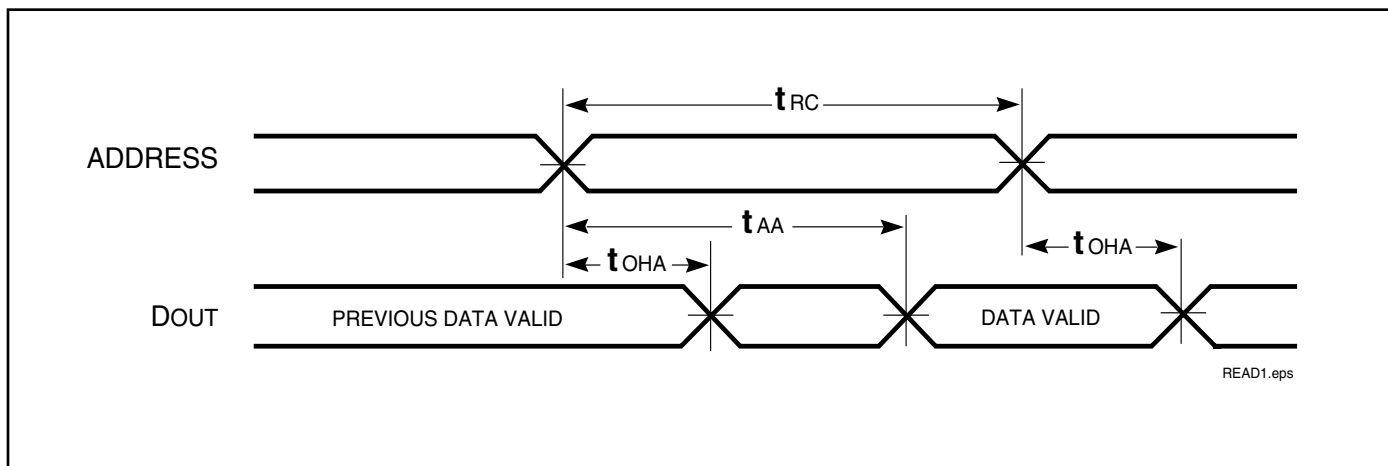## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

| Symbol	Parameter	-20 ns Min.	Max.	Unit
t_{RC}	Read Cycle Time	20	—	ns
t_{AA}	Address Access Time	—	20	ns
t_{OHA}	Output Hold Time	2.5	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	8	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	ns
t_{PU}	Power Up Time	0	—	ns
t_{PD}	Power Down Time	—	20	ns

Notes:
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS
READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)

READ1.eps

READ CYCLE NO. 2[1,3] ($\overline{CE}$ and $\overline{OE}$ Controlled)

CE_RD2.eps
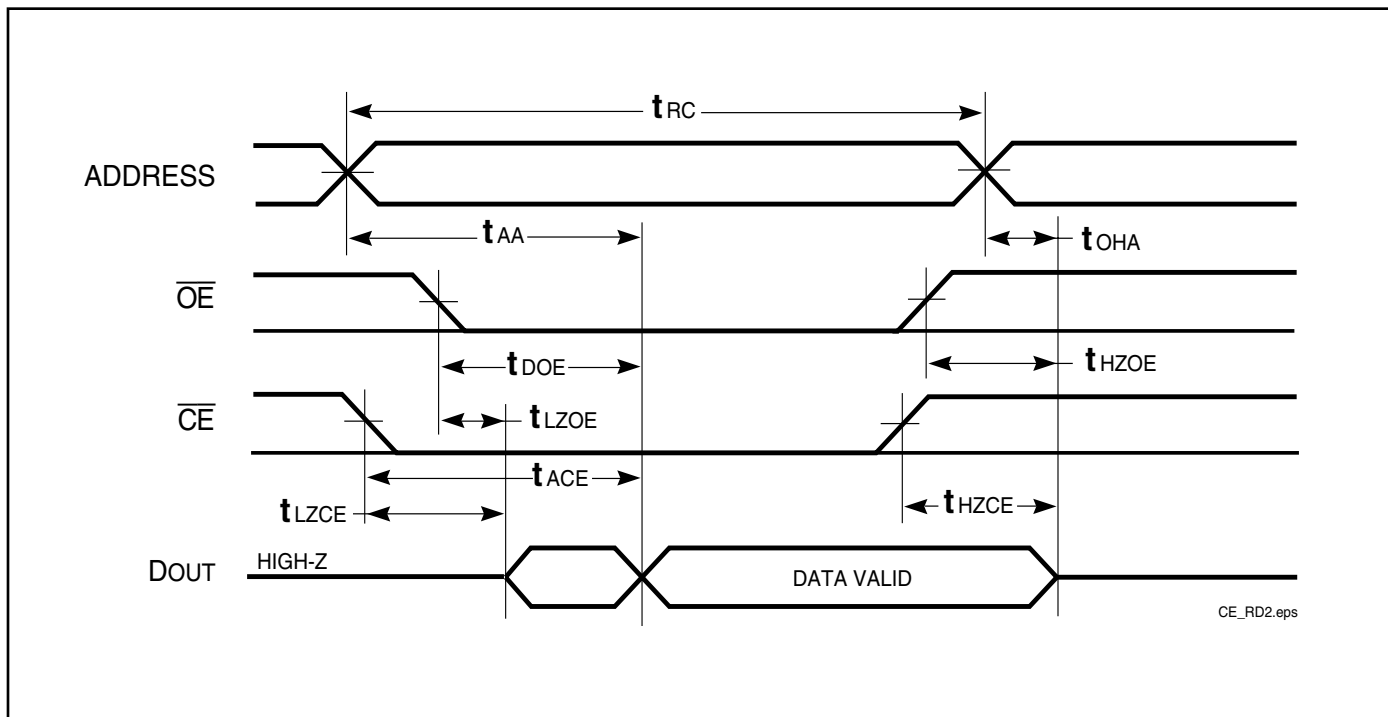
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-8		-10		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	8	—	10	—	ns
t_{SCE}	$\overline{CE}$ to Write End	6.5	—	8	—	ns
t_{AW}	Address Setup Time to Write End	6.5	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	6.5	—	8	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	8.0	—	10	—	ns
t_{SD}	Data Setup to Write End	5	—	6	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

## WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-20 ns Min.	-20 ns Max.	Unit
t_{WC}	Write Cycle Time	20	—	ns
t_{SCE}	$\overline{CE}$ to Write End	12	—	ns
t_{AW}	Address Setup Time to Write End	12	—	ns
t_{HA}	Address Hold from Write End	0	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	12	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	17	—	ns
t_{SD}	Data Setup to Write End	9	—	ns
t_{HD}	Data Hold from Write End	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	9	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	3	—	ns

Notes:
1. Test conditions assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

CE_WR1.eps
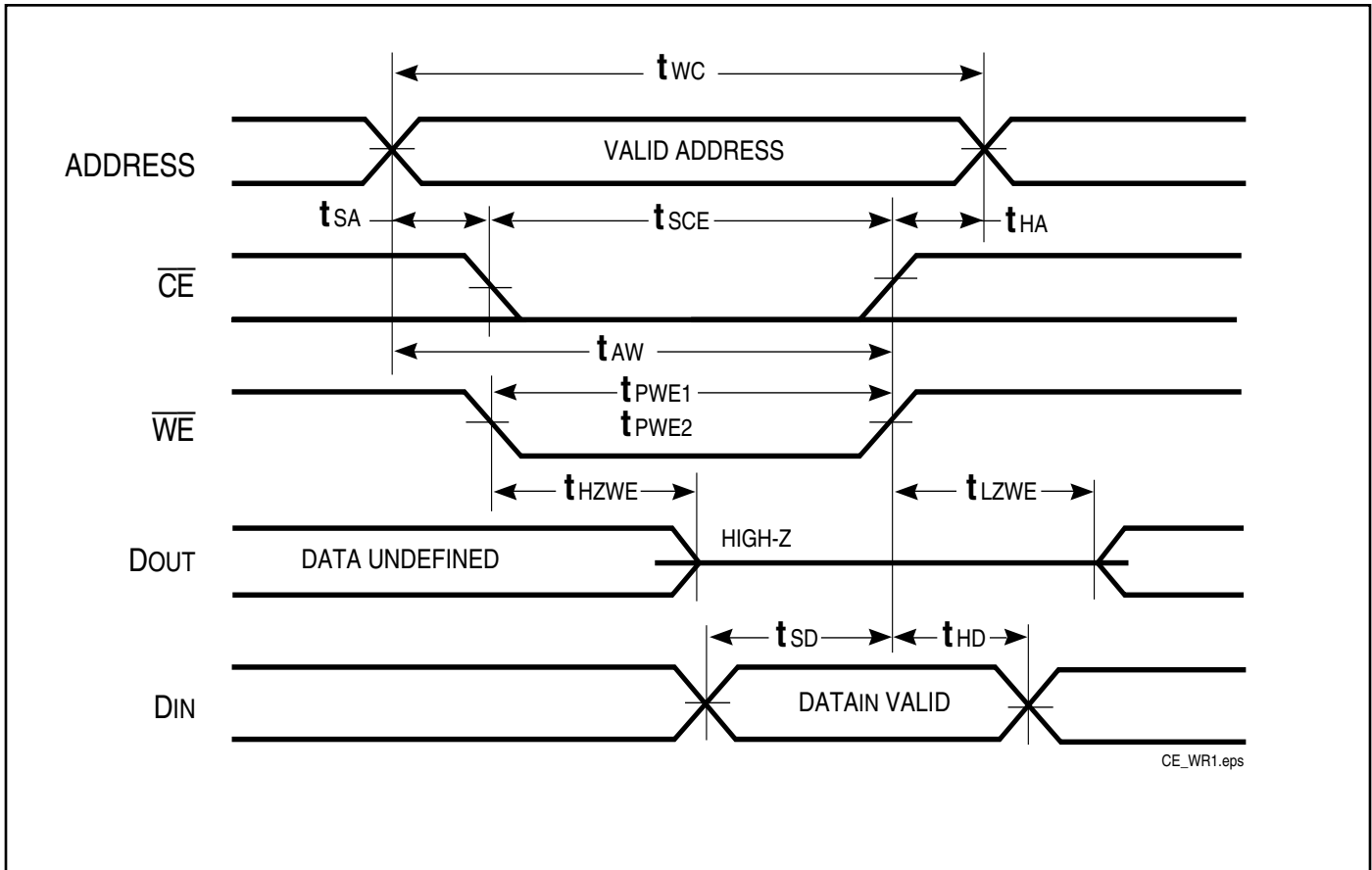
AC WAVEFORMS

WRITE CYCLE NO. 2[1,2] ($\overline{\text{WE}}$ Controlled: $\overline{\text{OE}}$ is HIGH During Write Cycle)

CE_WR2.eps

Notes:
1. The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
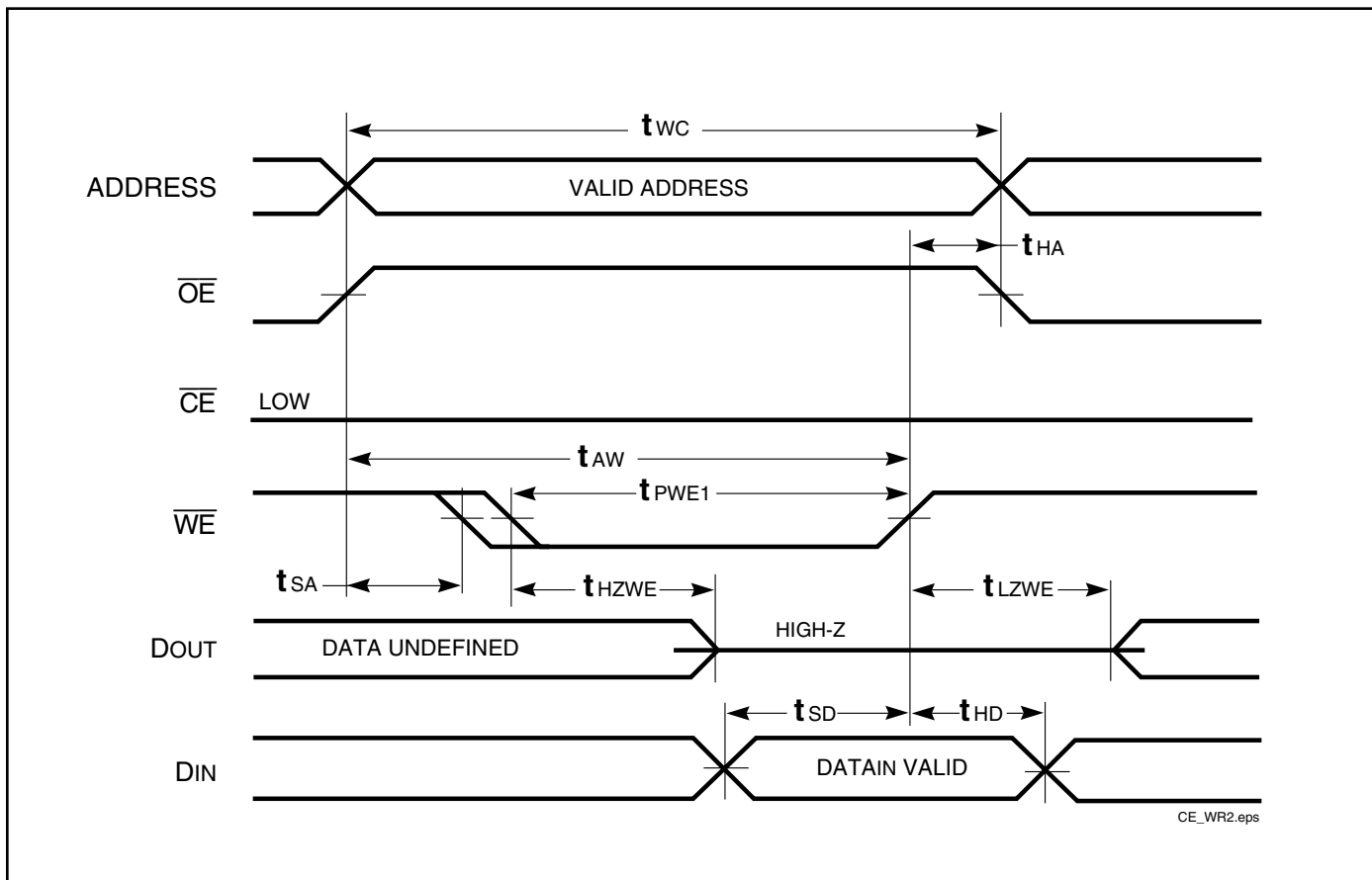2. I/O will assume the High-Z state if $\overline{\text{OE}}$ > V_{IH}.

AC WAVEFORMS

WRITE CYCLE NO. 3 ($\overline{\text{WE}}$ Controlled: $\overline{\text{OE}}$ is LOW During Write Cycle)

CE_WR3.eps
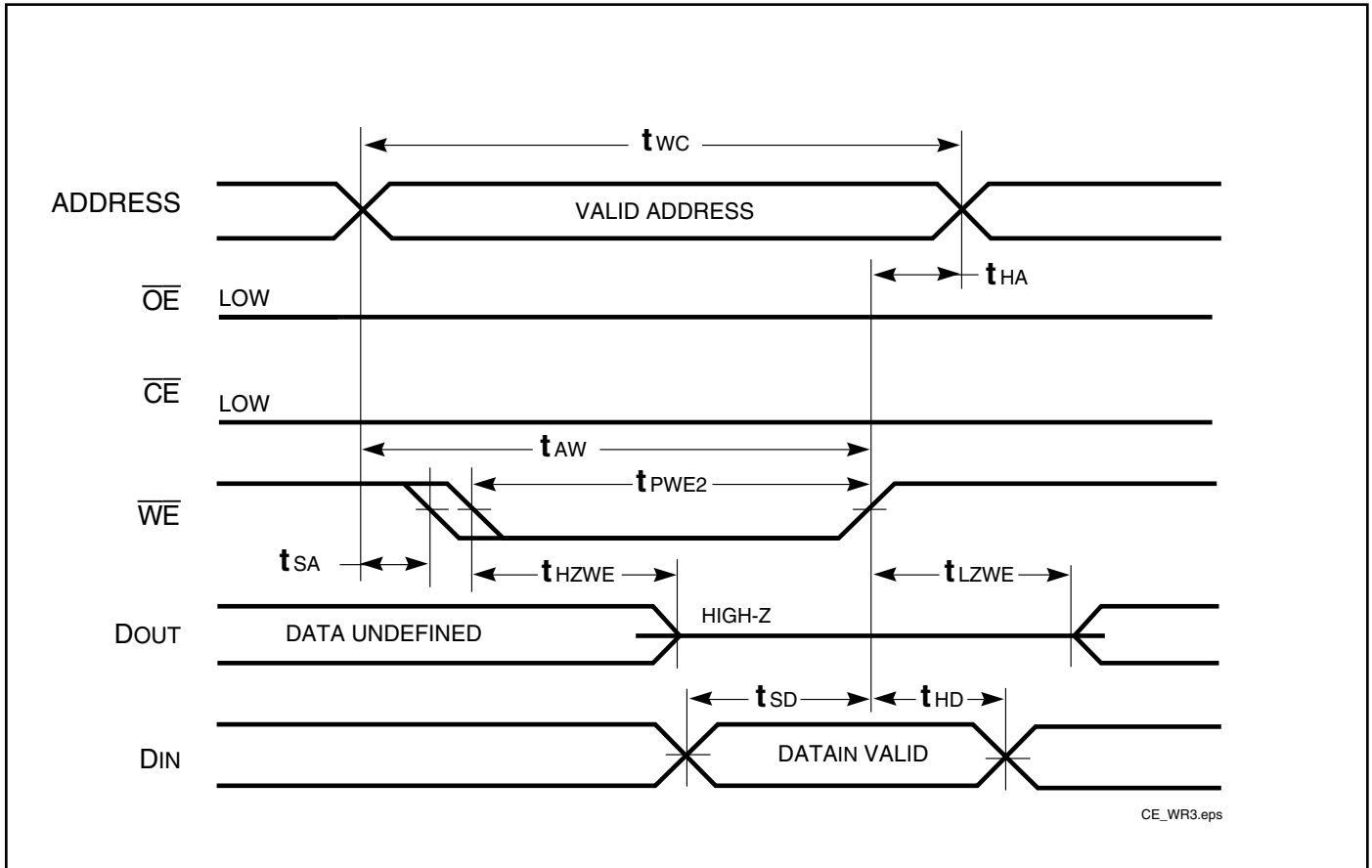
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.2V$, $\overline{CE} \geq V_{DD} - 0.2V$	Ind.	—	25	mA
			Auto.	—	60	
			typ.[1]		3	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

Note:

1. Typical values are measured at $V_{DD} = 3.0V$, $T_A = 25^{\circ}C$ and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)
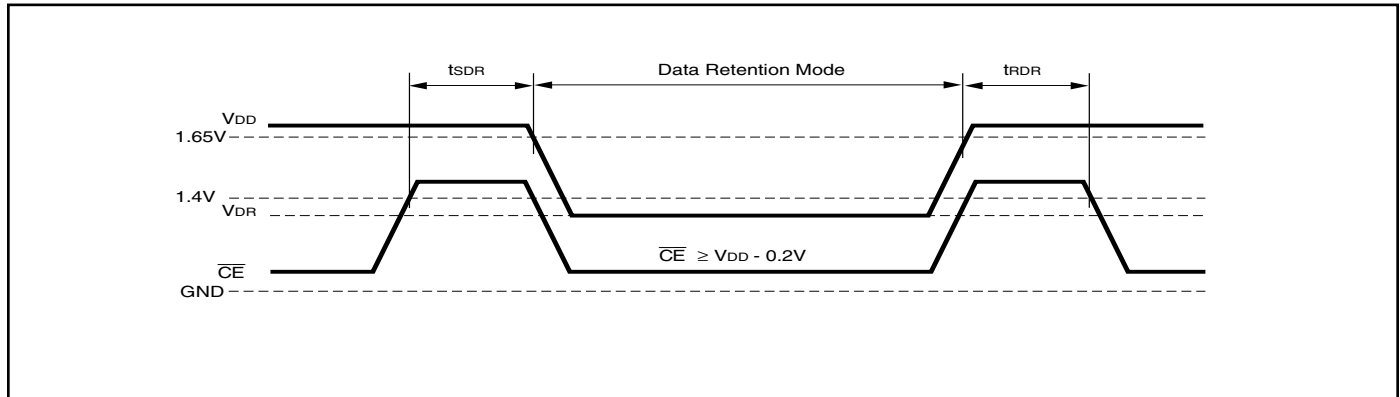
ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10 (8[1])	IS61WV20488BLL-10MI	48 mini BGA (9mm x 11mm)
	IS61WV20488BLL-10MLI	48 mini BGA (9mm x 11mm), Lead-free
	IS61WV20488BLL-10TI	TSOP (Type II)
	IS61WV20488BLL-10TLI	TSOP (Type II), Lead-free

Note:
1. Speed = 8ns for V_{DD} = 3.3V $\pm$ 5%. Speed = 10ns for V_{DD} = 2.4V to 3.3V.

Industrial Range: -40°C to +85°C

Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
20	IS61WV20488ALL-20MI	48 mini BGA (9mm x 11mm)
	IS61WV20488ALL-20TI	TSOP (Type II)

Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10	IS64WV20488BLL-10MA3	48 mini BGA (9mm x 11mm)
	IS64WV20488BLL-10MLA3	48 mini BGA (9mm x 11mm), Lead-free
	IS64WV20488BLL-10TA3	TSOP (Type II)

SYM.	DIMENSION (mm)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
b	0.30	0.35	0.40	0.012	0.014	0.016
D	10.90	11.00	11.10	0.429	0.433	0.437
D1	5.25 BSC			0.207 BSC		
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC			0.030 BSC		
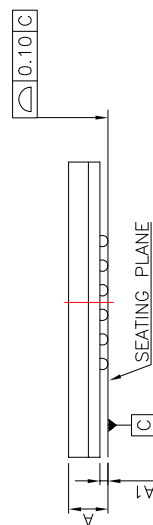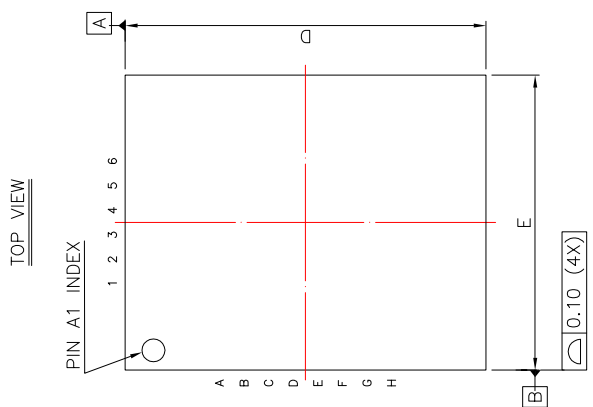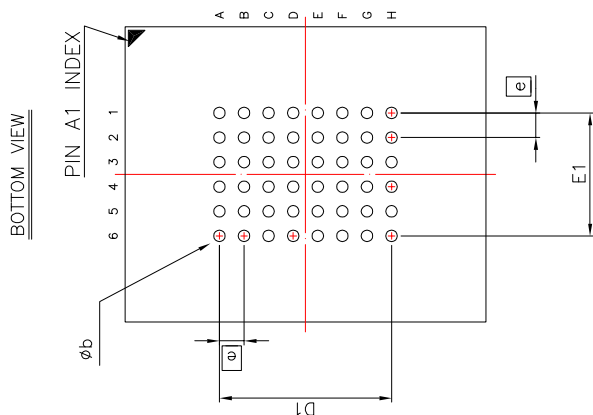
NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

BOTTOM VIEW

PIN A1 INDEX

TOP VIEW

PIN A1 INDEX

SEATING PLANE

TITLE	48L 9x11mm TF-BGA Package Outline	
	REV.	**B**
	DATE	08/21/2008

Rev. B
08/04/2010

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40		0.69	0.016		0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
Θ	0		8°	0		8°

DETAIL A

A

E1 E

D

ZD

A2

A1

e

b

DETAIL A

GAUGE PLANE

SAETING PLANE

L1

L

Θ

NOTE :

1. CONTROLLING DIMENSION : MM

2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

ISSI

TITLE **44L 400mil TSOP-2** Package Outline

REV. **F**

DATE 06/04/2008