32Mx8, 16Mx16, 8Mx32
256Mb Mobile Synchronous DRAM

APRIL 2012

FEATURES

- Fully synchronous; all signals referenced to a positive clock edge
- Internal bank for hiding row access and pre-charge
- Programmable CAS latency: 2, 3
- Programmable Burst Length: 1, 2, 4, 8, and Full Page
- Programmable Burst Sequence:
- Sequential and Interleave
- Auto Refresh (CBR)
- TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Arrays Self Refresh): 1/16, 1/8, 1/4, 1/2, and Full
- Deep Power Down Mode (DPD)
- Driver Strength Control (DS): 1/4, 1/2, and Full

OPTIONS

- Configurations:
  – 32M x 8
  – 16M x 16
  – 8M x 32
- Power Supply
  IS42VMxxx – V_{DD}/V_{DDQ} = 1.8V
- Packages:
  x8 –TSOP II (54)
  x16 –TSOP II (54), BGA (54)
  x32 – TSOP II (86), BGA (90)
- Temperature Range:
  Commercial (0°C to +70°C)
  Industrial (–40 °C to 85 °C)

DESCRIPTION

ISSI's 256Mb Mobile Synchronous DRAM achieves high-speed data transfer using pipeline architecture. All input and output signals refer to the rising edge of the clock input. Both write and read accesses to the SDRAM are burst oriented. The 256Mb Mobile Synchronous DRAM is designed to minimize current consumption making it ideal for low-power applications. Both TSOP and BGA packages are offered, including industrial grade products.

KEY TIMING PARAMETERS

Parameter	-8(1)	-12(2)	Unit
CLK Cycle Time			
$\overline{CAS}$ Latency = 3	8	12	ns
$\overline{CAS}$ Latency = 2	10	-	ns
CLK Frequency			
$\overline{CAS}$ Latency = 3	125	83	Mhz
$\overline{CAS}$ Latency = 2	100	-	Mhz
Access Time from CLK			
$\overline{CAS}$ Latency = 3	6	10	ns
$\overline{CAS}$ Latency = 2	9	-	ns

Notes:
1. Available for x8/x16 only
2. Available for x32 only

ADDRESSING TABLE

Parameter	32M x 8	16M x 16	8M x 32
Configuration	8M x 8 x 4 banks	4M x 16 x 4 banks	2M x 32 x 4 banks
Refresh Count	8K/64ms	8K/64ms	4K/64ms
Row Addressing	A0-A12	A0-A12	A0-A11
Column Addressing	A0-A9	A0-A8	A0-A8
Bank Addressing	BA0, BA1	BA0, BA1	BA0, BA1
Precharge Addressing	A10	A10	A10

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a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
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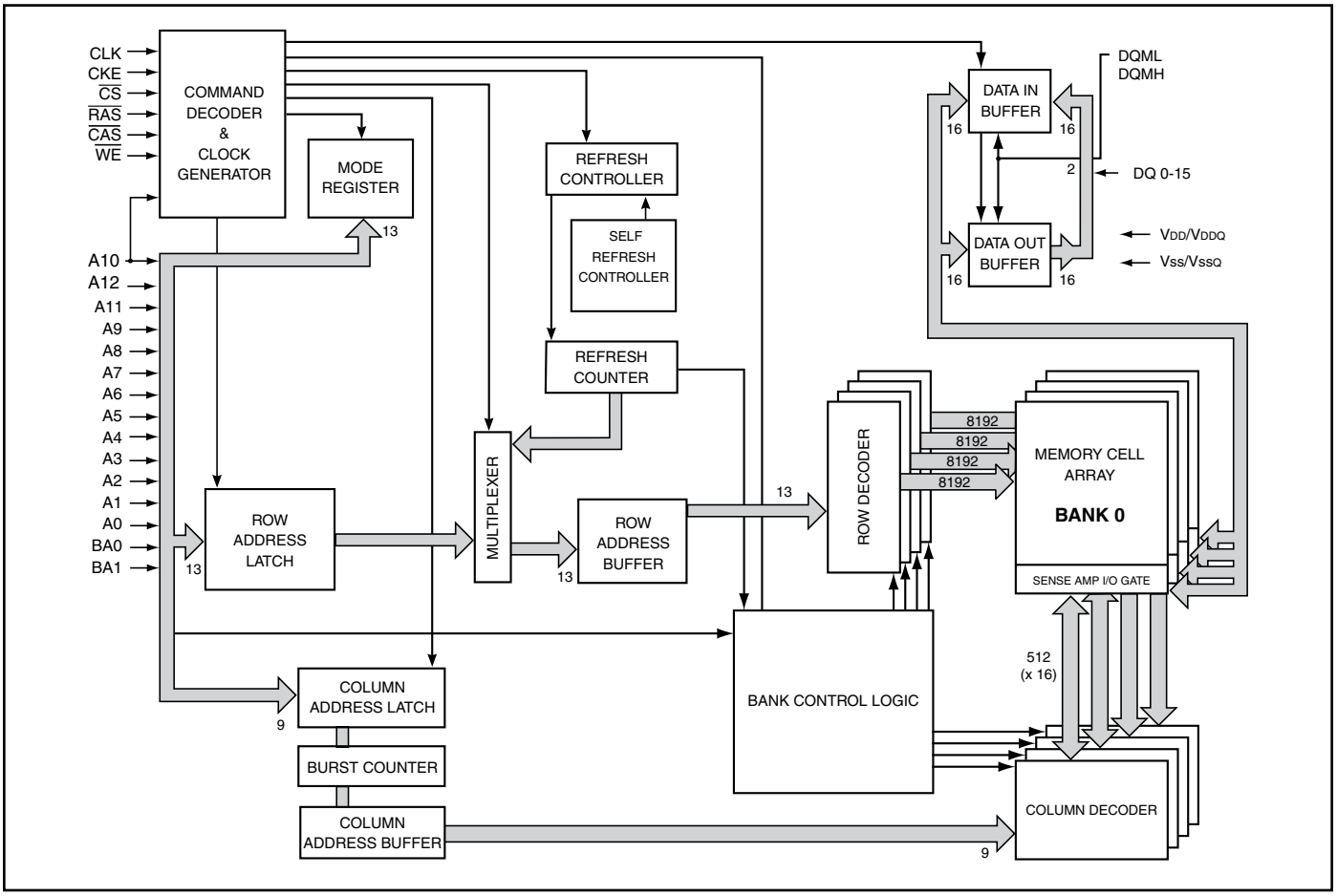
General Description

ISSI's 256Mb SDRAM is a high speed CMOS, dynamic random-access memory designed to operate in 1.8V V_{DD}/V_{DDQ} memory systems containing 268,435,456 bits. Internally configured as a quad-bank DRAM with a synchronous interface. The 256Mb SDRAM includes an AUTO REFRESH MODE, and a power-saving, power-down mode. All signals are registered on the positive edge of the clock signal, CLK. All inputs and outputs are LVCMOS (VDD = 1.8V) compatible. The 256Mb SDRAM has the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during burst access.

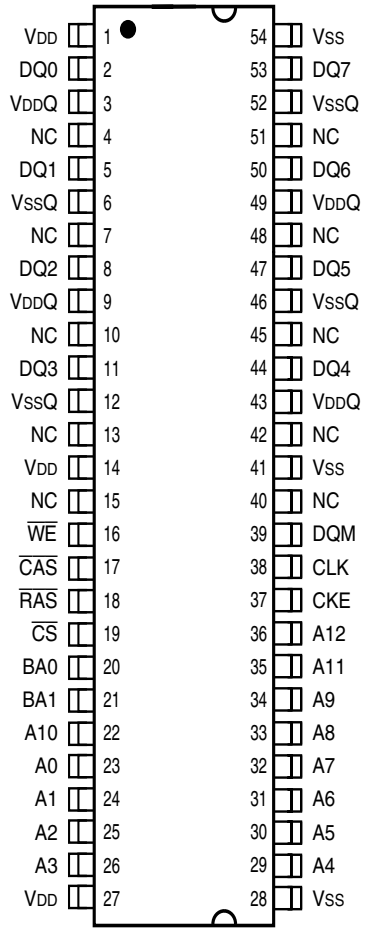
A self-timed row precharge initiated at the end of the burst sequence is available with the AUTO PRECHARGE function enabled. Precharge one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation. SDRAM read and write accesses are burst oriented starting at a selected location and continuing for a programmed number of locations in a programmed sequence. The registration of an Active command begins accesses, followed by a Read or Write command. The ACTIVE command in conjunction with address bits registered are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 (x8 and x16) and A0-A11 (x32) select the row). The READ or WRITE commands in conjunction with address bits registered are used to select the starting column location for the burst access. Programmable READ or WRITE burst lengths consist of 1, 2, 4 and 8 locations, or full page, with a burst terminate option.

FUNCTIONAL BLOCK DIAGRAM (FOR 16Mx16 BANKS SHOWN)



PIN CONFIGURATIONS

54 pin TSOP – Type II for x8



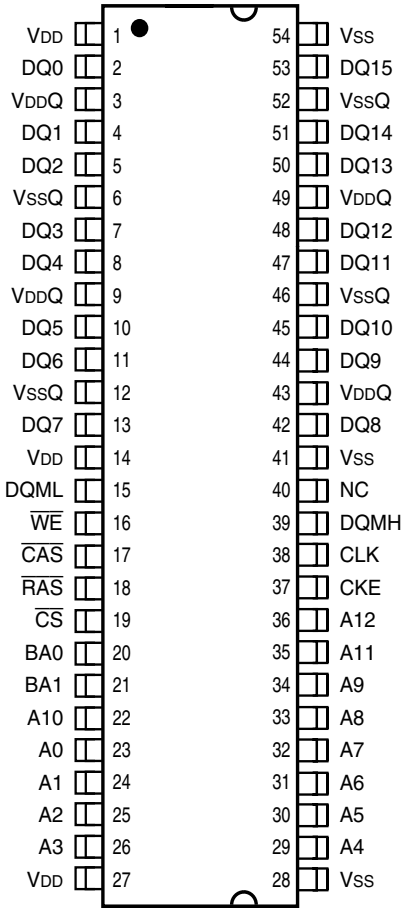
PIN DESCRIPTIONS

32M x 8	Pin Name
A0–A12	Row Address Input
A0–A9	Column Address Input
BA0, BA1	Bank Select Address
DQ0–DQ7	Data Input/Output
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command

32M x 8	Pin Name
$\overline{CAS}$	Column Address Strobe Command
$\overline{WE}$	Write Enable
DQM	Data Input/Output Mask
VDD	Power
VSS	Ground
VDDQ	Power Supply for I/O Pin
VSSQ	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

54 pin TSOP – Type II for x16



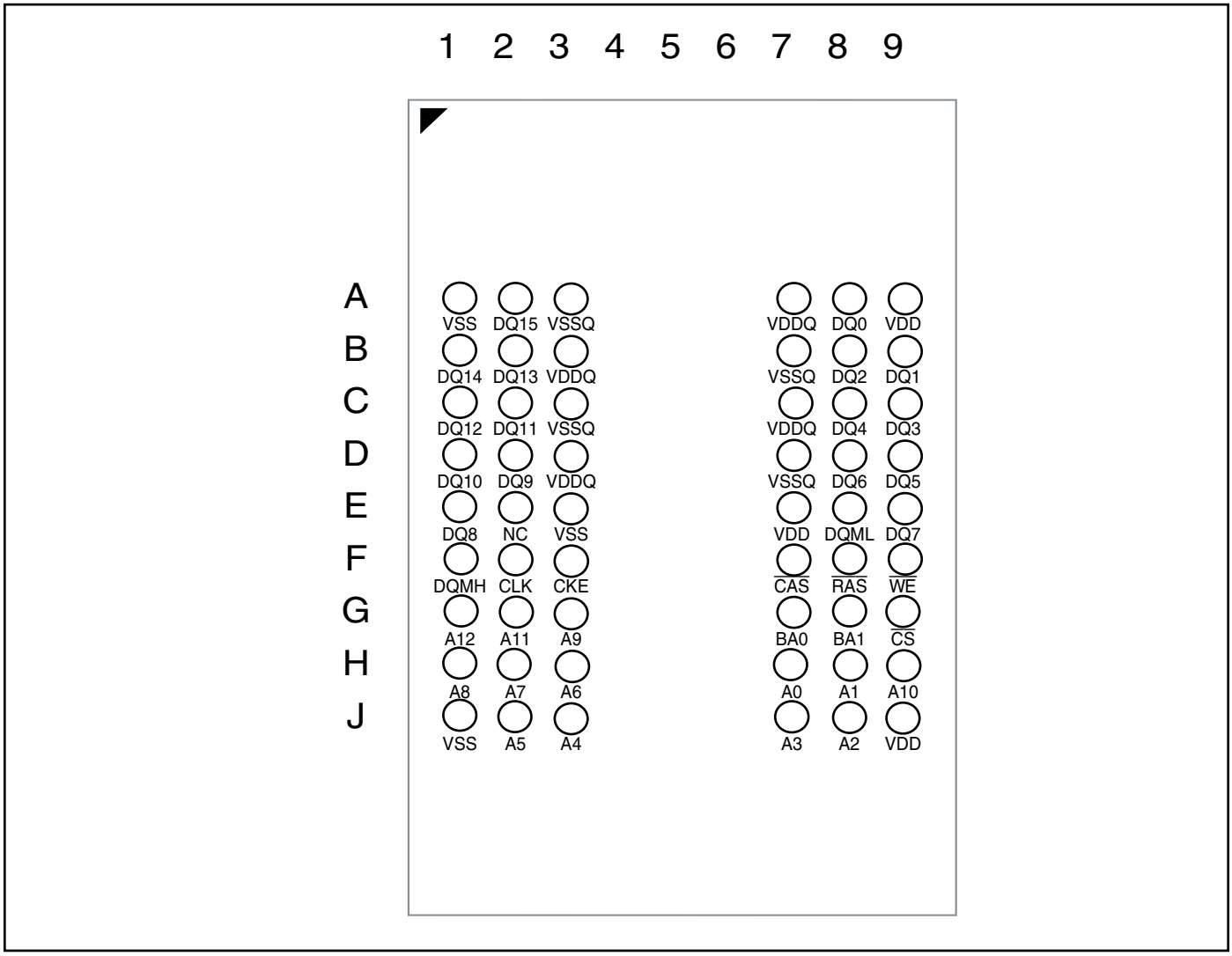
PIN DESCRIPTIONS

16M x16	Pin Name
A0–A12	Row Address Input
A0–A8	Column Address Input
BA0, BA1	Bank Select Address
DQ0–DQ15	Data Input/Output
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

16M x16	Pin Name
$\overline{WE}$	Write Enable
DQML / DQMH	Data Input/Output Mask
VDD	Power
VSS	Ground
VDDQ	Power Supply for I/O Pin
VSSQ	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

54-ball FBGA for x16 (Top View) (8.00mm x 13.00mm Body, 0.8mm Ball Pitch)



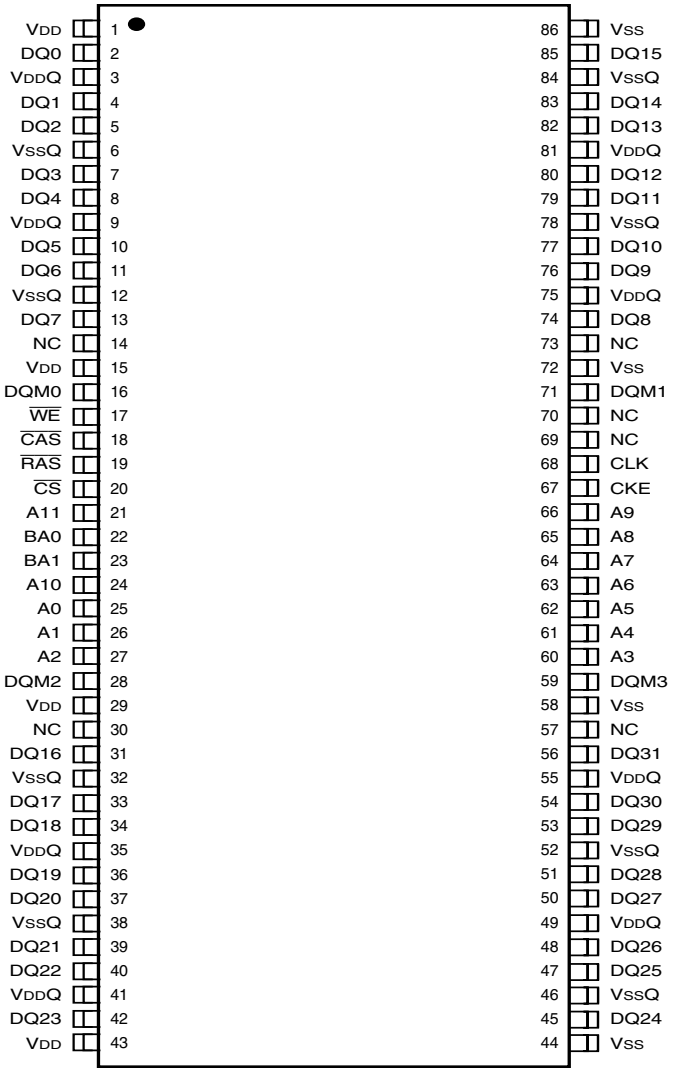
PIN DESCRIPTIONS

16M x16	Pin Name
A0–A12	Row Address Input
A0–A8	Column Address Input
BA0, BA1	Bank Select Address
DQ0–DQ15	Data Input/Output
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command

16M x16	Pin Name
$\overline{CAS}$	Column Address Strobe Command
$\overline{WE}$	Write Enable
DQML / DQMH	Data Input/Output Mask
VDD	Power
VSS	Ground
VDDQ	Power Supply for I/O Pin
VSSQ	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

86 pin TSOP – Type II for x32



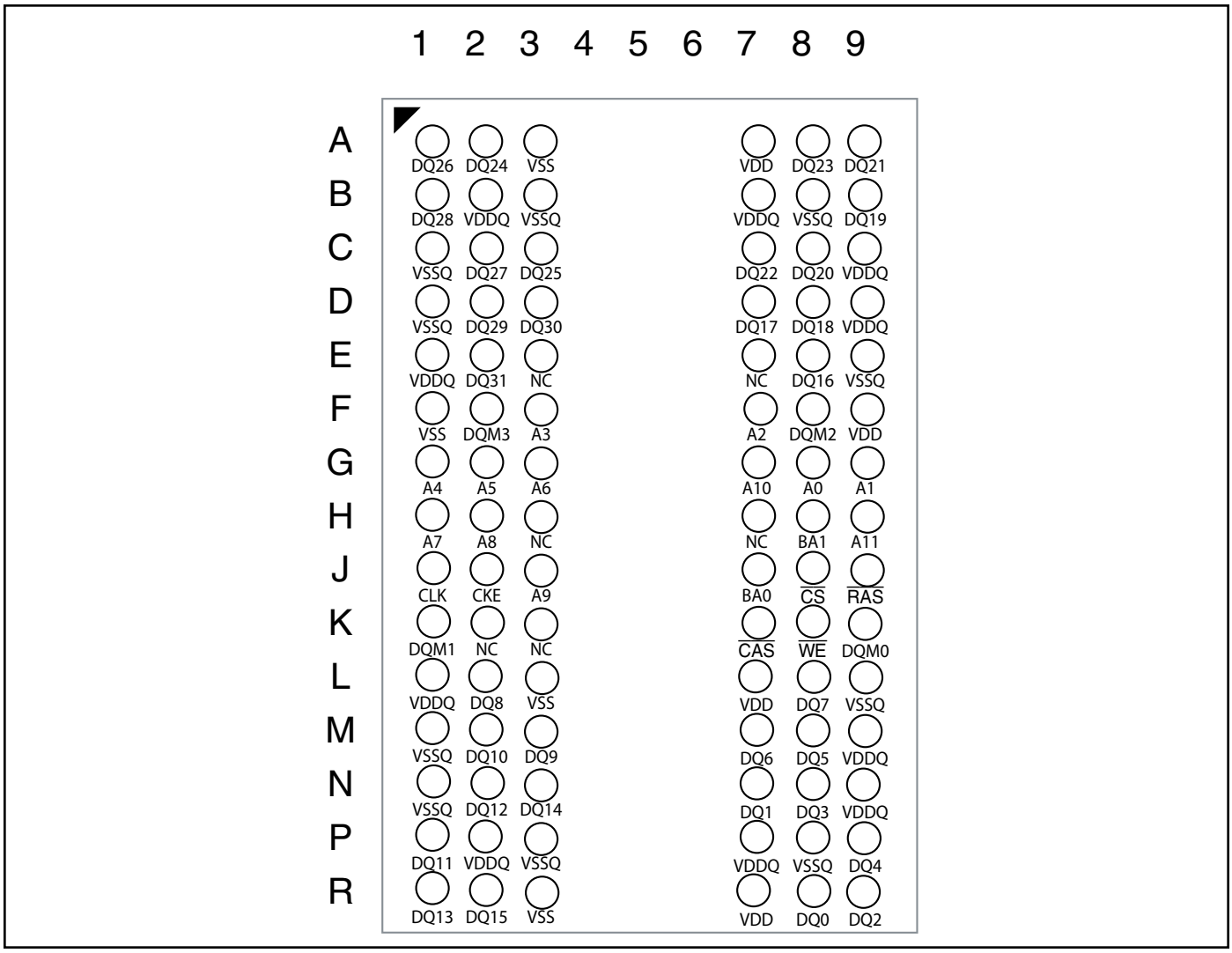
PIN DESCRIPTIONS

8M x32	Pin Name
A0–A11	Row Address Input
A0–A8	Column Address Input
BA0, BA1	Bank Select Address
DQ0–DQ31	Data Input/Output
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

8M x32	Pin Name
$\overline{WE}$	Write Enable
DQM0 - DQM3	Data Input/Output Mask
VDD	Power
VSS	Ground
VDDQ	Power Supply for I/O Pin
VSSQ	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

90-ball FBGA for x32 (Top View) (8.00mm x 13.00mm Body, 0.8mm Ball Pitch)



PIN DESCRIPTIONS

8M x32	Pin Name
A0–A11	Row Address Input
A0–A8	Column Address Input
BA0, BA1	Bank Select Address
DQ0–DQ31	Data Input/Output
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

8M x32	Pin Name
$\overline{WE}$	Write Enable
DQM0 - DQM3	Data Input/Output Mask
VDD	Power
VSS	Ground
VDDQ	Power Supply for I/O Pin
VSSQ	Ground for I/O Pin
NC	No Connection

Mobile SDRAM Functionality

ISSI's 256Mb Mobile SDRAMs are pin compatible and have similar functionality with ISSI's standard SDRAMs, but offer lower operating voltages and power saving features. For detailed descriptions of pin functions, command truth tables, functional truth tables, device operation as well as timing diagrams please refer to ISSI document "Mobile Synchronous DRAM Device Operations & Timing Diagrams" listed at www.issi.com

REGISTER DEFINITION

Mode Register (MR) & Extended Mode Register (EMR)

There are two mode registers in the Mobile SDRAM; Mode Register (MR) and Extended Mode Register (EMR). The Mode Register is discussed below, followed by the Extended Mode Register. The Mode Register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of burst length, a burst type, CAS Latency, operating mode, and a write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

The EMR controls the functions beyond those controlled by the MR. These additional functions are special features of the Mobile SDRAM. They include temperature-compensated self refresh (TCSR) control, partial-array self refresh (PASR), and output drive strength. The EMR is programmed via the MODE REGISTER SET command with BA1 = 1 and BA0 = 0 and retains the stored information until it is programmed again or the device loses power. Not programming the extended mode register upon initialization will result in default settings for the low-power features. The extended mode will default with the temperature sensor enabled, full drive strength, and full array (all 4 banks) refresh.

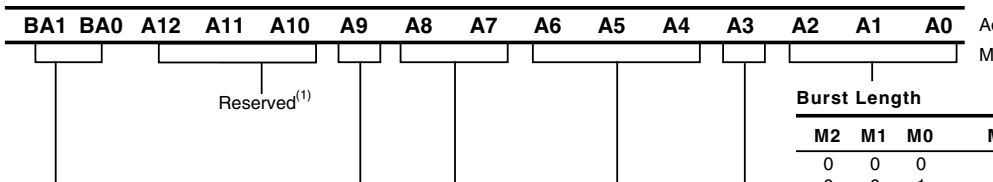
Mode Register Definition

The MR is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure MODE REGISTER DEFINITION. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0 - M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4 - M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the WRITE burst mode, and M10, M11, and M12 are reserved for future use.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

MODE REGISTER DEFINITION



Burst Length

M2	M1	M0	M3=0	M3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Burst Type

M3	Type
0	Sequential
1	Interleaved

Latency Mode

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Operating Mode

M8	M7	M6-M0	Mode
0	0	Defined	Standard Operation
—	—	—	All Other States Reserved

Write Burst Mode

M9	Mode
0	Programmed Burst Length
1	Single Location Access

BA1	BA0	Mode Register Definition
0	0	Program Mode Register
0	1	Reserved
1	0	Program Extended Mode Register
1	1	Reserved

1. Note: A12 x8 and x16, A11 x32
2. To ensure compatibility with future devices, should program A12, A11, A10 = "0"

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in MODE REGISTER DEFINITION. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A8 (x32), A1-A8 (x16) or A1-A9 (x8) when the burst length is set to two; by A2-A8 (x32), A2-A8 (x16) or A2-A9 (x8) when the burst length is set to four; and by A3-A8 (x32), A3-A8 (x16) or A3-A9 (x8) when the burst length is set to eight. The remaining (least significant) address bit(s) are used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in BURST DEFINITION table.

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
			A 0		
2			0	0-1	0-1
			1	1-0	1-0
		A 1	A 0		
		0	0	0-1-2-3	0-1-2-3
4		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
	A 2	A 1	A 0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
8	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A8 (x16, x32) n = A0-A9 (x8) (location 0-y)			Cn + 3, Cn + 4... …Cn - 1, Cn…	Cn, Cn + 1, Cn + 2 Not Supported

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge n + m. The DQs will start driving as a result of the clock edge one cycle earlier (n + m - 1), and provided that the relevant access times are met, the data will be valid by clock edge n + m. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in CAS Latency diagrams.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

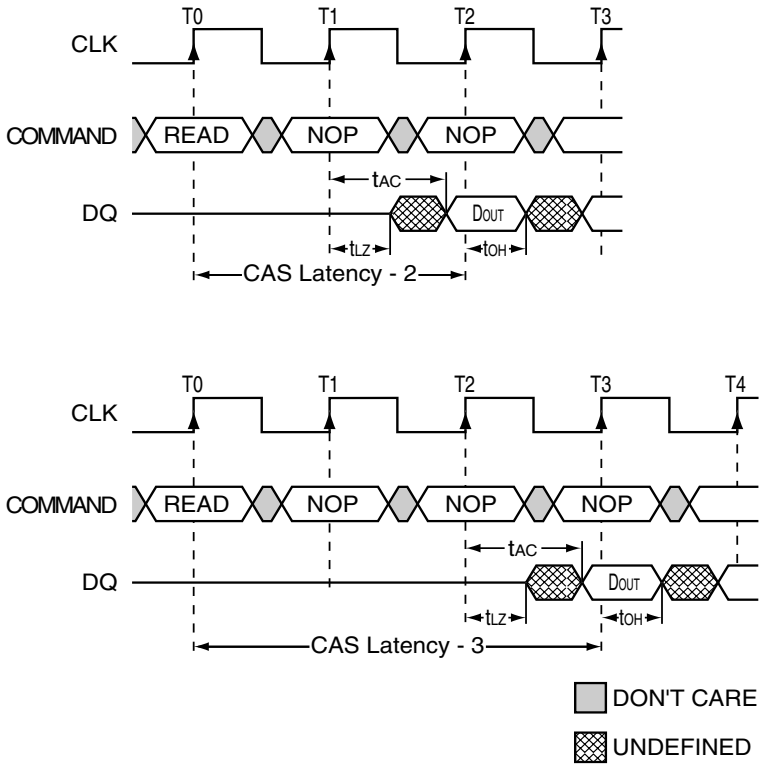
The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

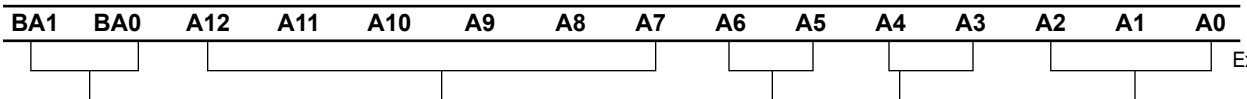
Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

CAS LATENCY



EXTENDED MODE REGISTER DEFINITION



PASR

E2	E1	E0	Partial Array Self Refresh Coverage
0	0	0	Fully array (4 banks) - (Default)
0	0	1	Half array (banks 0, 1)
0	1	0	Quarter array (bank 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One-eighth array (1/2 bank 0)
1	1	0	One-sixteenth array (1/4 bank 0)
1	1	1	Reserved

TCSR

E4	E3	Max. Case Temp.
0	0	70°C
0	1	45°C
1	0	15°C
1	1	85°C (Default)

DS

E6	E5	Driver Strength
0	0	Full strength driver (Default)
0	1	Half strength driver
1	0	Quarter strength driver
1	1	Reserved

set to "0"

E12	E11	E10	E9	E8	E7	E6-E0	
0	0	0	0	0	0	Valid	Normal operation
–	–	–	–	–	–	–	All other states reserved

BA1	BA0	Mode Register Definition
0	0	Program Mode Register
0	1	Reserved
1	0	Program Extended mode Register
1	1	Reserved

The extended mode register is programmed via the MODE REGISTER SET command (BA1 = 1, BA0 = 0) and retains the stored information until it is programmed again or the device loses power. The extended mode register must be programmed with E7 through E11 (or E12 for x8 & x16) set to “0.” The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation. The extended mode register must be programmed to ensure proper operation.

Temperature-Compensated Self Refresh (TCSR)

TCSR allows the controller to program the refresh interval during self refresh mode, according to the case temperature of the mobile device. This allows great power savings during self refresh during most operating temperature ranges. Only during extreme temperatures would the controller have to select a higher TCSR level that will guarantee data during self refresh.

Every cell in the DRAM requires refreshing due to the capacitor losing its charge over time. The refresh rate is dependent on temperature. At higher temperatures a capacitor loses charge quicker than at lower temperatures, requiring the cells to be refreshed more often. Historically, during self refresh, the refresh rate has been set to accommodate the worst case, or highest temperature range, expected. Thus, during ambient temperatures, the power consumed during refresh was unnecessarily high because the refresh rate was set to accommodate the higher temperatures. Setting E4 and E3 allows the DRAM to accommodate more specific temperature regions during self refresh. The default for ISSI 256Mb Mobile SDRAM is TCSR = 85°C to guarantee refresh operation. This mode of operation has a higher current consumption because the self refresh oscillator is set to refresh the SDRAM cells more often than needed. By using an external temperature sensor to determine the operating temperature the Mobile SDRAM can be programmed for lower temperature and refresh rates, effectively reducing current consumption by a significant amount. There are four temperature settings, which will vary the self refresh current according to the selected temperature. This selectable refresh rate will save power when the Mobile DRAM is operating at normal temperatures.

Partial-Array Self Refresh (PASR)

For further power savings during self refresh, the PASR feature allows the controller to select the amount of memory that will be refreshed during self refresh. The refresh options are all banks (banks 0, 1, 2, and 3); two banks (banks 0 and 1); and one bank (bank 0). In addition partial amounts of bank 0 (half or quarter of the bank) may be selected. WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during self refresh. It's important to note that data in banks 2 and 3 will be lost when the two-bank option is used. Data will be lost in banks 1, 2, and 3 when the one-bank option is used.

Driver Strength (DS)

Bits E5 and E6 of the EMR can be used to select the driver strength of the DQ outputs. This value should be set according to the application's requirements. The default is Full Driver Strength.

Deep Power Down (DPD)

Deep power down mode is for maximum power savings and is achieved by shutting down power to the entire memory array of the mobile device. Data will be lost once deep power down mode is executed.

DPD mode is entered by having all banks idle, CS and WE held low, with RAS and CAS HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW during DPD mode. To exit DPD mode, CKE must be asserted HIGH. Upon exit from DPD mode, at least 200µs of valid clocks with either NOP or COMMAND INHIBIT commands are applied to the command bus, followed by a full Mobile SDRAM initialization sequence, is required.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
$V_{DD\ MAX}$	Maximum Supply Voltage		–0.35 to +2.8	V
$V_{DDQ\ MAX}$	Maximum Supply Voltage for Output Buffer		–0.35 to +2.8	V
V_{IN}	Input Voltage		–0.35 to V_{DDQ} + 0.5	V
V_{OUT}	Output Voltage		–0.35 to V_{DDQ} + 0.5	V
$P_{D\ MAX}$	Allowable Power Dissipation		1	W
I_{CS}	Output Shorted Current		50	mA
T_{OPR}	Operating Temperature	Com.	0 to +70	°C
		Ind.	–40 to +85	°C
T_{STG}	Storage Temperature		–65 to +150	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to Vss.

CAPACITANCE CHARACTERISTICS - x8, x16

Symbol	Parameters	Min.	Max.	Unit
$C_{IN}1$	Input Capacitance: CLK	2.5	3.5	pF
$C_{IN}2$	Input Capacitance: All Other Input Pins	2.5	3.8	pF
$C_{I/O}$	Data Input/Output Capacitance: I/Os	4.0	6.0	pF

CAPACITANCE CHARACTERISTICS - x32

Symbol	Parameters	Min.	Max.	Unit
$C_{IN}1$	Input Capacitance: CLK	2.5	3.5	pF
$C_{IN}2$	Input Capacitance: All Other Input Pins	2.5	3.8	pF
$C_{I/O}$	Data Input/Output Capacitance: I/Os	4.0	6.5	pF

DC RECOMMENDED OPERATING CONDITIONS
IS42VMxxx - 1.8V Operation

Symbol	Parameters	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	1.7	1.8	1.95	V
V_{DDQ}	I/O Supply Voltage	1.7	1.8	1.95	V
V_{IH}(1)	Input High Voltage	0.8xV_{DDQ}	–	V_{DDQ}+0.3	V
V_{IL}(2)	Input Low Voltage	-0.3	–	0.8	V
I_{IL}	Input Leakage Current (0V ≤ V_{IN} ≤ V_{DD})	-1	–	+1	µA
I_{OL}	Output Leakage Current (Output disabled, 0V ≤ V_{OUT} ≤ V_{DD})	-1.5	–	+1.5	µA
V_{OH}	Output High Voltage Current (I_{OH} = -100µA)	0.9xV_{DDQ}	–	–	V
V_{OL}	Output Low Voltage Current (I_{OL} = 100µA)	–	–	0.2	V

Notes:
1. V_{IH} (overshoot): V_{IH} (max) = V_{DDQ} +1.2V (pulse width < 3ns).
2. V_{IL} (undershoot): V_{IH} (min) = -1.2V (pulse width < 3ns).
3. All voltages are referenced to Vss.

DC ELECTRICAL CHARACTERISTICS VDD = 1.8V (x8 and x16)

Symbol	Parameter	Test Condition	–8	Unit
$I_{DD}1$(1)	Operating Current	One Bank Active, CL = 3, BL = 2, tCLK = tCLK(min), tRC = tRC(min)	90	mA
$I_{DD}2P$(4)	Precharge Standby Current (In Power-Down Mode)	CKE ≤ V_{IL} (max), tCK = 15ns $\overline{CS}$ ≥ V_{DD} - 0.2V	1	mA
$I_{DD}2PS$(4)	Precharge Standby Current With Clock Stop (In Power-Down Mode)	CKE ≤ V_{IL} (max), CLK ≤ V_{IL} (max) $\overline{CS}$ ≥ V_{DD} - 0.2V	1	mA
$I_{DD}2N$(2)	Precharge Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) tCK = 15 ns	20	mA
$I_{DD}2NS$	Precharge Standby Current With Clock Stop (In Non-Power Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) All Inputs Stable	7	mA
$I_{DD}3P$(2)	Active Standby Current (In Power-Down Mode)	CKE ≤ V_{IL} (max), $\overline{CS}$ ≥ V_{DD} - 0.2V tCK = 15 ns, All Banks Active	3	mA
$I_{DD}3PS$	Active Standby Current With Clock Stop (In Power-Down Mode)	CKE ≤ V_{IL} (max), CLK ≤ V_{IL} (max) $\overline{CS}$ ≥ V_{DD} - 0.2V, All Banks Active	3	mA
$I_{DD}3N$(2)	Active Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) tCK = 15 ns, All Banks Active	25	mA
$I_{DD}3NS$	Active Standby Current With Clock Stop (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) All Inputs Stable, All Banks Active	10	mA
$I_{DD}4$	Operating Current	All Banks Active, BL = Full, CL = 3 tCK = tCK(min)	115	mA
$I_{DD}5$	Auto-Refresh Current	tRC = tRC(min), tCLK = tCLK(min)	130	mA
$I_{DD}6$	Self-Refresh Current	CKE ≤ 0.2V	1.2	mA
$I_{DD}7$	Self-Refresh: CKE = LOW; t_{CK} = t_{CK} (MIN); Address, Control, and Data bus inputs are stable	Full Array, 85°C Full Array, 45°C Half Array, 85°C Half Array, 45°C 1/4th Array, 85°C 1/4th Array, 45°C 1/8th Array, 85°C 1/8th Array, 45°C 1/16th Array, 85°C 1/16th Array, 45°C	1200 800 1000 670 800 540 700 470 600 400	µA
I_{ZZ}(3,4)	Deep Power Down Current	CKE ≤ 0.2V	20	µA

Notes:
1. I_{DD} (max) is specified at the output open condition.
2. Input signals are changed one time during 30ns.
3. Izz values shown are nominal at 25°C. Izz is not tested.
4. Tested after 500ms delay

DC ELECTRICAL CHARACTERISTICS VDD = 1.8V (x32)

Symbol	Parameter	Test Condition	–12	Unit
$I_{DD}1$ (1)	Operating Current	One Bank Active, CL = 3, BL = 2, tCLK = tCLK(min), tRC = tRC(min)	90	mA
$I_{DD}2P$ (4)	Precharge Standby Current (In Power-Down Mode)	CKE ≤ V_{IL} (max), tCK = 15ns $\overline{CS}$ ≥ V_{DD} - 0.2V	1	mA
$I_{DD}2PS$ (4)	Precharge Standby Current With Clock Stop (In Power-Down Mode)	CKE ≤ V_{IL} (max), CLK ≤ V_{IL} (max) $\overline{CS}$ ≥ V_{DD} - 0.2V	1	mA
$I_{DD}2N$ (2)	Precharge Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) tCK = 15 ns	20	mA
$I_{DD}2NS$	Precharge Standby Current With Clock Stop (In Non-Power Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) All Inputs Stable	7	mA
$I_{DD}3P$ (2)	Active Standby Current (In Power-Down Mode)	CKE ≤ V_{IL} (max), $\overline{CS}$ ≥ V_{DD} - 0.2V tCK = 15 ns, All Banks Active	3	mA
$I_{DD}3PS$	Active Standby Current With Clock Stop (In Power-Down Mode)	CKE ≤ V_{IL} (max), CLK ≤ V_{IL} (max) $\overline{CS}$ ≥ V_{DD} - 0.2V, All Banks Active	3	mA
$I_{DD}3N$ (2)	Active Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) tCK = 15 ns, All Banks Active	25	mA
$I_{DD}3NS$	Active Standby Current With Clock Stop (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) All Inputs Stable, All Banks Active	10	mA
$I_{DD}4$	Operating Current	All Banks Active, BL = Full, CL = 3 tCK = tCK(min)	90	mA
$I_{DD}5$	Auto-Refresh Current	tRC = tRC(min), tCLK = tCLK(min)	165	mA
$I_{DD}6$	Self-Refresh Current	CKE ≤ 0.2V	1.2	mA
$I_{DD}7$	Self-Refresh: CKE = LOW; t_{CK} = t_{CK} (MIN); Address, Control, and Data bus inputs are stable	Full Array, 85°C Full Array, 45°C Half Array, 85°C Half Array, 45°C 1/4th Array, 85°C 1/4th Array, 45°C 1/8th Array, 85°C 1/8th Array, 45°C 1/16th Array, 85°C 1/16th Array, 45°C	1200 800 1000 670 800 540 700 470 600 400	µA
I_{ZZ} (3,4)	Deep Power Down Current	CKE ≤ 0.2V	20	µA

Notes:
1. I_{DD} (max) is specified at the output open condition.
2. Input signals are changed one time during 30ns.
3. Izz values shown are nominal at 25°C. Izz is not tested.
4. Tested after 500ms delay

AC ELECTRICAL CHARACTERISTICS (1, 2, 3)

			-8		-12		
Symbol	**Parameter**		**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
tCK3	Clock Cycle Time	CAS Latency = 3	8	–	12	–	ns
tCK2		CAS Latency = 2	10	–	–	–	ns
tAC3	Access Time From CLK	CAS Latency = 3	–	6	–	10	ns
tAC2		CAS Latency = 2	–	9	–	–	ns
tCHI	CLK HIGH Level Width		2.5	–	2.5	–	ns
tCL	CLK LOW Level Width		2.5	–	2.5	–	ns
tOH3	Output Data Hold Time	CAS Latency = 3	2.7	–	2.7	–	ns
tOH2		CAS Latency = 2	2.7	–	–	–	ns
tLZ	Output LOW Impedance Time		0	–	0	–	ns
tHZ3	Output HIGH Impedance Time	CAS Latency = 3	2.7	6	2.7	10	ns
tHZ2		CAS Latency = 2	2.7	9	–	–	
tDS	Input Data Setup Time (2)		1.5	–	1.5	–	ns
tDH	Input Data Hold Time (2)		1.0	–	1.0	–	ns
tAS	Address Setup Time (2)		1.5	–	1.5	–	ns
tAH	Address Hold Time (2)		1.0	–	1.0	–	ns
tCKS	CKE Setup Time (2)		1.5	–	1.5	–	ns
tCKH	CKE Hold Time (2)		1.0	–	1.0	–	ns
tCS	Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)(2)		1.5	–	1.5	–	ns
tCH	Command Hold Time (($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)(2)		1.0	–	1.0	–	ns
tRC	Command Period (REF to REF / ACT to ACT)		80	–	120	–	ns
tRAS	Command Period (ACT to PRE)		56	100K	84	100K	ns
tRP	Command Period (PRE to ACT)		24	–	36	–	ns
tRCD	Active Command to Read/ Write Command Delay Time		22	–	36	–	ns
tRRD	Command Period (ACT [0] to ACT [1])		16	–	20	–	ns
tDPL	Input Data to Precharge Command Delay Time		16	–	20	–	ns
tDAL	Input Data to Active/Refresh Command Delay Time (During Auto-Precharge)		40	–	50	–	ns
tMRD	Mode Register Program Time		15	–	20	–	ns
tDDE	Power Down Exit Setup Time		8	–	10	–	ns
tXSR	Exit Self-Refresh to Active Time		80	–	100	–	ns
tT	Transition Time		0.3	1.2	0.3	1.2	ns
tREF	Refresh Cycle Time	8K times (x8/x16)	–	–	–	64	ms
		4K times (x32)	–	64	–	64	ms

Notes:
1. The power-on sequence must be executed before starting memory operation.
2. Measured with tT = 1 ns. If clock rising time is longer than 1ns, (tT/2 - 0.5) ns should be added to the parameter.
3. The reference level is 0.9V when measuring input signal timing. Rise and fall times are measured between V_{IH}(min.) and V_{IL} (max).

OPERATING FREQUENCY / LATENCY RELATIONSHIPS

SYMBOL	PARAMETER	-8	-12	UNITS
—	Clock Cycle Time	8	12	ns
—	Operating Frequency	125	83	MHz
t_{CAC}	$\overline{CAS}$ Latency	3	3	cycle
t_{RCD}	Active Command To Read/Write Command Delay Time	3	3	cycle
t_{RAC}	$\overline{RAS}$ Latency (t_{RCD} + t_{CAC}) $\overline{CAS}$ Latency = 3	6	6	cycle
t_{RC}	Command Period (REF to REF / ACT to ACT)	10	10	cycle
t_{RAS}	Command Period (ACT to PRE)	7	7	cycle
t_{RP}	Command Period (PRE to ACT)	3	3	cycle
t_{RRD}	Command Period (ACT[0] to ACT [1])	2	2	cycle
t_{CCD}	Column Command Delay Time (READ, READA, WRIT, WRITA)	1	1	cycle
t_{DPL}	Input Data To Precharge Command Delay Time	2	2	cycle
t_{DAL}	Input Data To Active/Refresh Command Delay Time (During Auto-Precharge)	5	5	cycle
t_{RBD}	Burst Stop Command To Output in HIGH-Z Delay Time (Write) $\overline{CAS}$ Latency = 3	3	3	cycle
t_{WBD}	Burst Stop Command To Input in Invalid Delay Time (Write)	0	0	cycle
t_{RQL}	Precharge Command To Output in HIGH-Z Delay Time (Read) $\overline{CAS}$ Latency = 3	3	3	cycle
t_{WDL}	Precharge Command To Input in Invalid Delay Time (Write)	0	0	cycle
t_{PQL}	Last Output To Auto-Precharge Start Time (Read) $\overline{CAS}$ Latency = 3	-2	-2	cycle
t_{QMD}	DQM To Output Delay Time (Read)	2	2	cycle
t_{DMD}	DQM To Input Delay Time (Write)	0	0	cycle
t_{MRD}	Mode Register Set To Command Delay Time	2	2	cycle

Ordering Information – V_{DD} = 1.8V

Commercial Range: (0°C to +70°C)

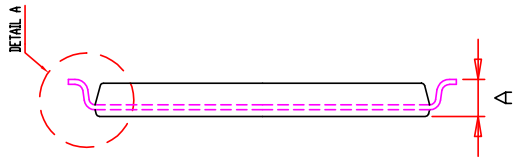
Configuration	Frequency (MHz)	Speed (ns)	Order Part No.	Package
16Mx16	125	8	IS42VM16160D-8BL	54-Ball BGA, Lead-free
8Mx32	83	12	IS42VM32800D-12BL	90-Ball BGA, Lead-free

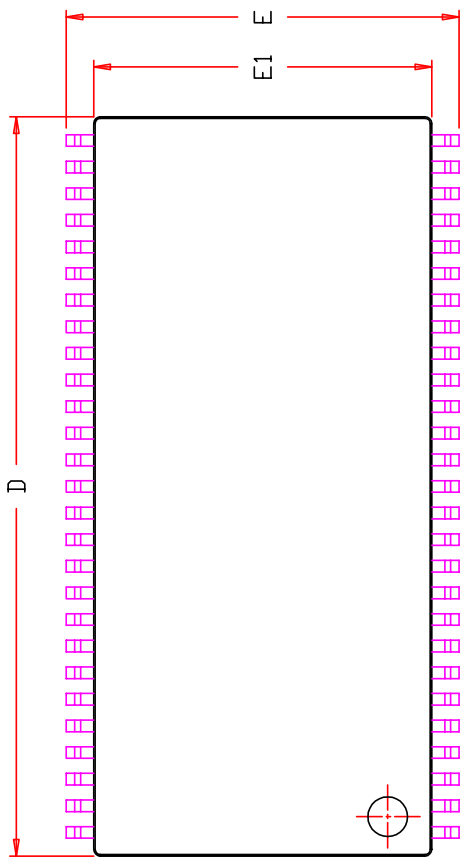
Industrial Range: (–40ºC to 85ºC)

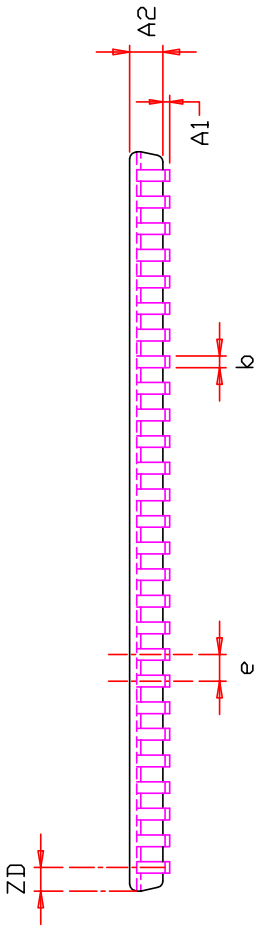
Configuration	Frequency (MHz)	Speed (ns)	Order Part No.	Package
32Mx8	125	8	IS42VM83200D-8TLI	54-pin TSOP II, Lead-free
16Mx16	125	8	IS42VM16160D-8TLI	54-pin TSOP II, Lead-free
			IS42VM16160D-8BLI	54-Ball BGA, Lead-free
8Mx32	83	12	IS42VM32800D-12TLI	86-pin TSOP II, Lead-free
			IS42VM32800D-12BLI	90-Ball BGA, Lead-free

Note: Contact ISSI for leaded parts support.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
C	0.12		0.21	0.005		0.008
D	22.02	22.22	22.42	0.867	0.875	0.883
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BSC.			0.010 BSC.		
ZD	0.71 REF.			0.028 REF.		
θ	0		8°	0		8°

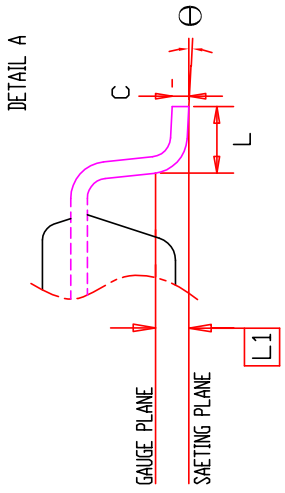




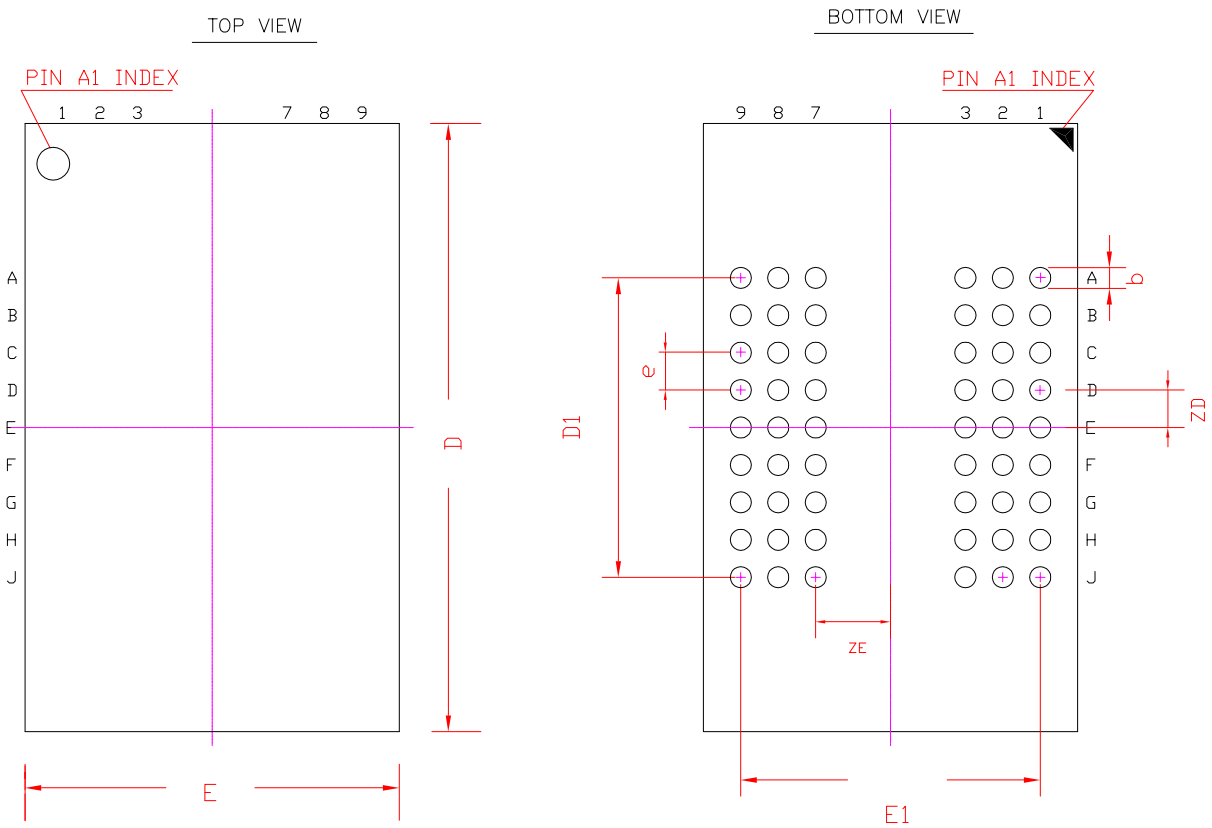


NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.



	TITLE	REV.	DATE
ISSI	54L 400mil TSOP-2 Package Outline	F	03/24/2009

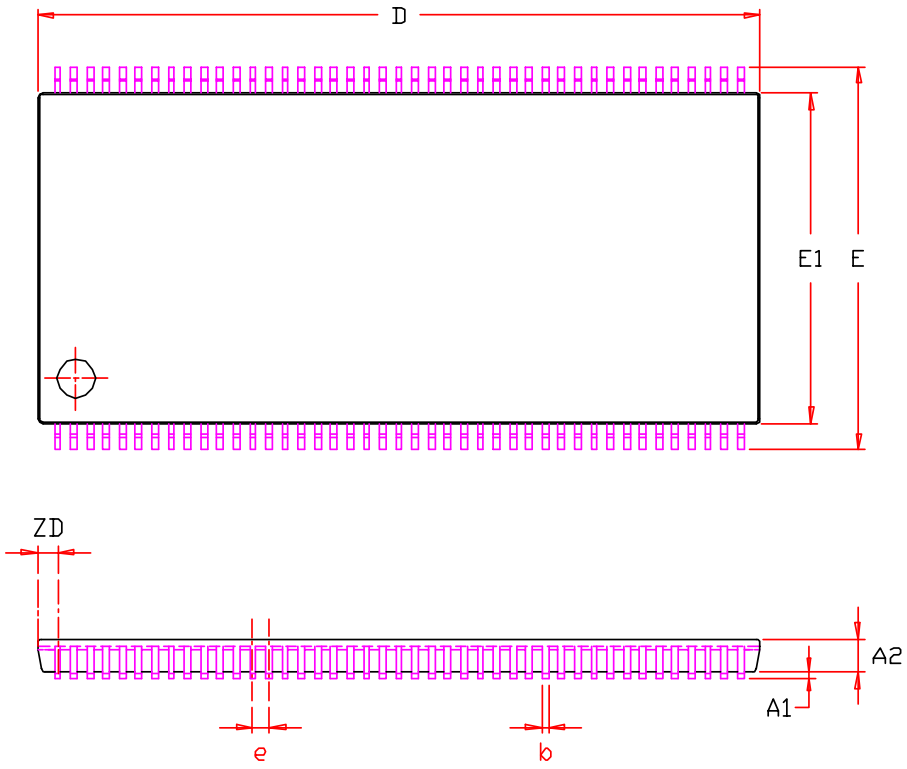


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.25		0.40	0.010		0.016
øb	0..40	0.45	0.50	0.016	0.018	0.020
D	12.90	13.00	13.10	0.508	0.512	0.516
D1	6.40 BSC.			0.252 BSC.		
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.40 BSC.			0.252 BSC.		
e	0.80 BSC.			0.031 BSC.		
ZD	0.80 REF.			0.031 REF.		
ZE	1.60 REF.			0.063 REF.		
y	0.10			0.004		

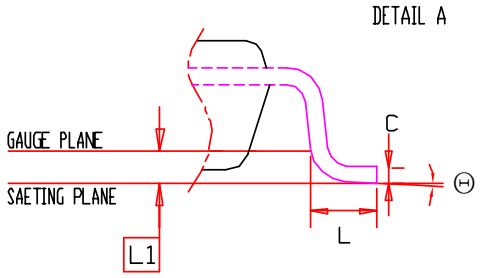
NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MS-207

	TITLE	54L 8x13mm TF-BGA Package Outline	REV.	B	DATE	08/29/2008



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A			1.20
A1	0.05		0.20
A2	0.95	1.00	1.05
b	0.17		0.27
C	0.12		0.21
D	22.02	22.22	22.42
E	11.56	11.76	11.96
E1	10.03	10.16	10.29
e	0.50 BSC.		
L	0.40	0.50	0.60
L1	0.25 BSC.		
ZD	0.61 REF.		
θ	0		8°

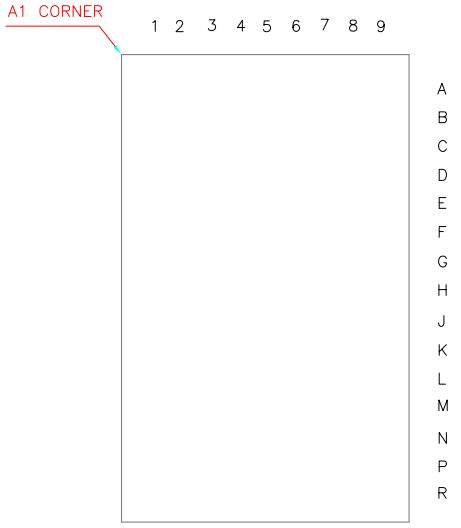


NOTE :

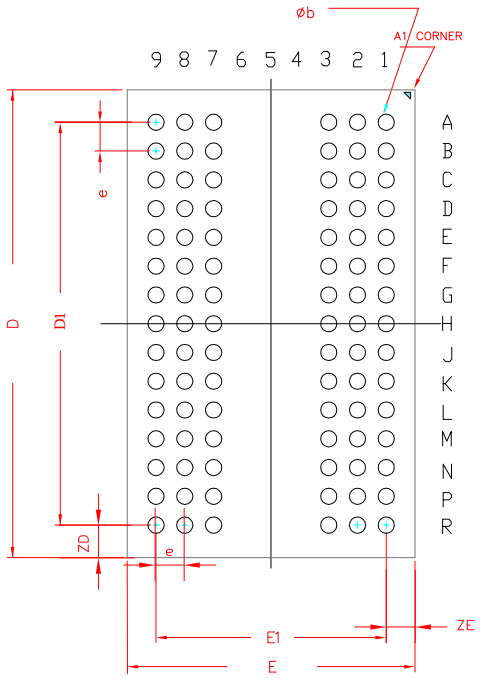
1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

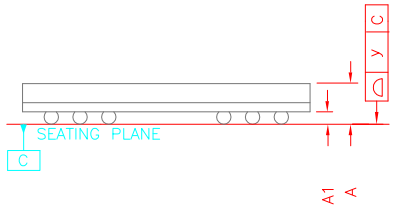
ISSI®	TITLE	86L 400mil TSOP-2 Package Outline	REV.	E	DATE	09/26/2006

TOP VIEW



BOTTOM VIEW





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.25		0.40	0.010		0.016
øb	0.40	0.45	0.50	0.016	0.018	0.020
D	12.90	13.00	13.10	0.508	0.512	0.516
D1	11.20 BSC.			0.441 BSC.		
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.40 BSC.			0.252 BSC.		
e	0.80 BSC.			0.315 BSC.		
ZD	0.9 REF.			0.035 REF.		
ZE	0.8 REF.			0.032 REF.		
y	0.10			0.004		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

Ball Pitch :	Ball Diameter :
0.80	0.45

	TITLE	90L 8x13mm TF-BGA Package Outline	REV.	B	DATE	08/14/2008