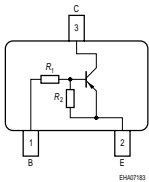


**PNP Silicon Digital Transistor**

- Switching circuit, inverter, interface circuit, driver circuit
- Built in bias resistor ( $R_1 = 4.7 \text{ k}\Omega$  ,  $R_2 = 47 \text{ k}\Omega$  )
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101


**BCR166  
BCR166W**


Type	Marking	Pin Configuration						Package
BCR166	WTs	1=B	2=E	3=C	-	-	-	SOT23
BCR166W	WTs	1=B	2=E	3=C	-	-	-	SOT323

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Collector-emitter voltage	$V_{CEO}$	50	V
Collector-base voltage	$V_{CBO}$	50	
Input forward voltage	$V_{i(fwd)}$	30	
Input reverse voltage	$V_{i(rev)}$	5	
Collector current	$I_C$	100	mA
Total power dissipation- BCR166, $T_S \leq 102^\circ\text{C}$ BCR166W, $T_S \leq 124^\circ\text{C}$	$P_{tot}$	200 250	mW
Junction temperature	$T_j$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-65 ... 150	

**Thermal Resistance**

Parameter	Symbol	Value	Unit
Junction - soldering point <sup>1)</sup>	$R_{thJS}$		K/W
BCR166		≤ 240	
BCR166W		≤ 105	

**Electrical Characteristics at  $T_A = 25^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

**DC Characteristics**

Collector-emitter breakdown voltage $I_C = 100 \mu\text{A}, I_B = 0$	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10 \mu\text{A}, I_E = 0$	$V_{(BR)CBO}$	50	-	-	
Collector-base cutoff current $V_{CB} = 40 \text{ V}, I_E = 0$	$I_{CBO}$	-	-	100	nA
Emitter-base cutoff current $V_{EB} = 5 \text{ V}, I_C = 0$	$I_{EBO}$	-	-	155	$\mu\text{A}$
DC current gain <sup>2)</sup> $I_C = 5 \text{ mA}, V_{CE} = 5 \text{ V}$	$h_{FE}$	70	-	-	-
Collector-emitter saturation voltage <sup>2)</sup> $I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$	$V_{CEsat}$	-	-	0.3	V
Input off voltage $I_C = 100 \mu\text{A}, V_{CE} = 5 \text{ V}$	$V_{i(off)}$	0.4	-	0.8	
Input on voltage $I_C = 2 \text{ mA}, V_{CE} = 0.3 \text{ V}$	$V_{i(on)}$	0.5	-	1.4	
Input resistor	$R_1$	3.2	4.7	6.2	$\text{k}\Omega$
Resistor ratio	$R_1/R_2$	0.09	0.1	0.11	-

**AC Characteristics**

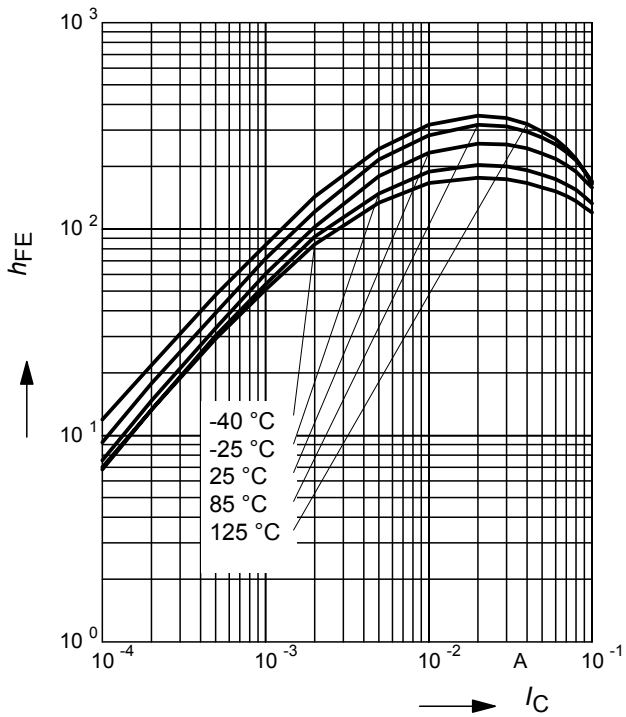
Transition frequency $I_C = 10 \text{ mA}, V_{CE} = 5 \text{ V}, f = 100 \text{ MHz}$	$f_T$	-	160	-	MHz
Collector-base capacitance $V_{CB} = 10 \text{ V}, f = 1 \text{ MHz}$	$C_{cb}$	-	3	-	pF

<sup>1)</sup>For calculation of  $R_{thJA}$  please refer to Application Note AN077 (Thermal Resistance Calculation)

<sup>2)</sup>Pulse test:  $t < 300 \mu\text{s}; D < 2\%$

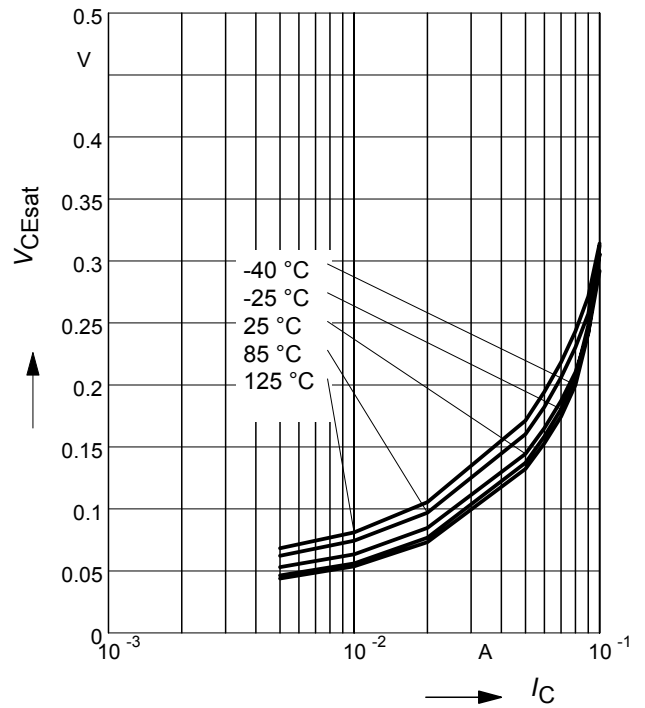
**DC current gain  $h_{FE} = f(I_C)$**

$V_{CE} = 5\text{ V}$  (common emitter configuration)



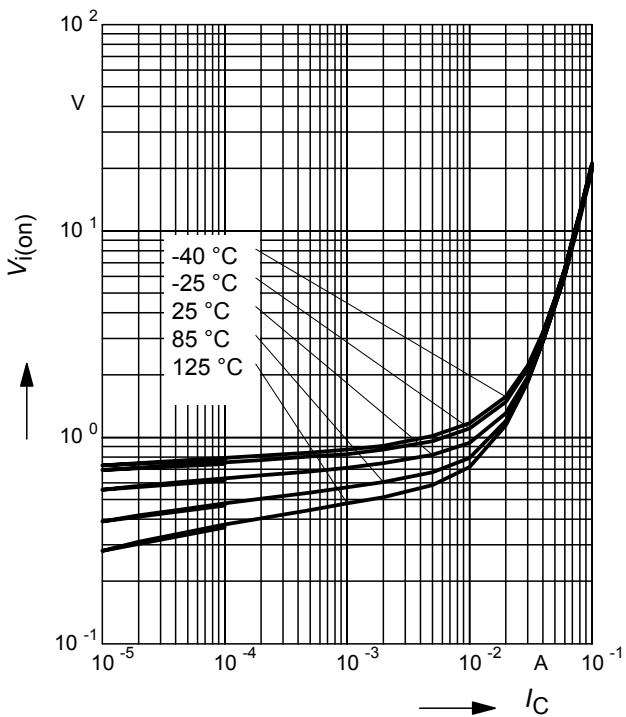
**Collector-emitter saturation voltage**

$V_{CEsat} = f(I_C), I_C/I_B = 20$



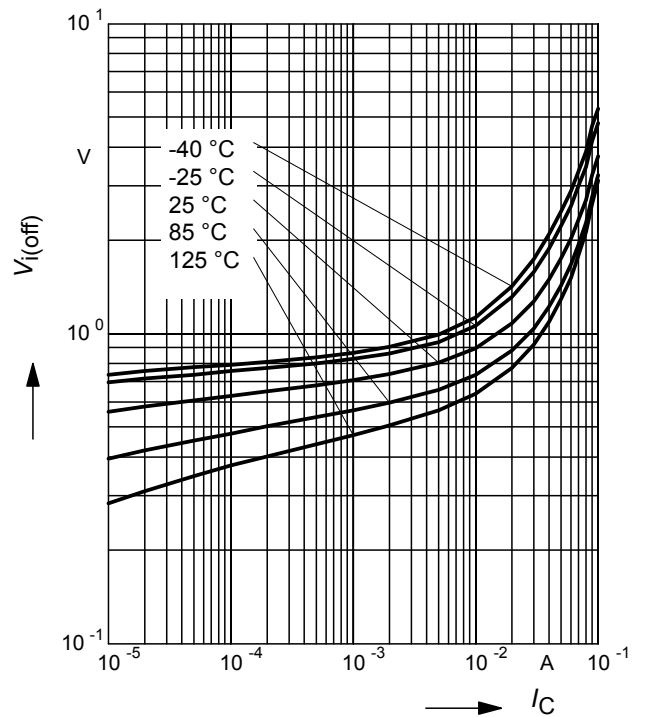
**Input on Voltage  $V_{i(on)} = f(I_C)$**

$V_{CE} = 0.3\text{ V}$  (common emitter configuration)



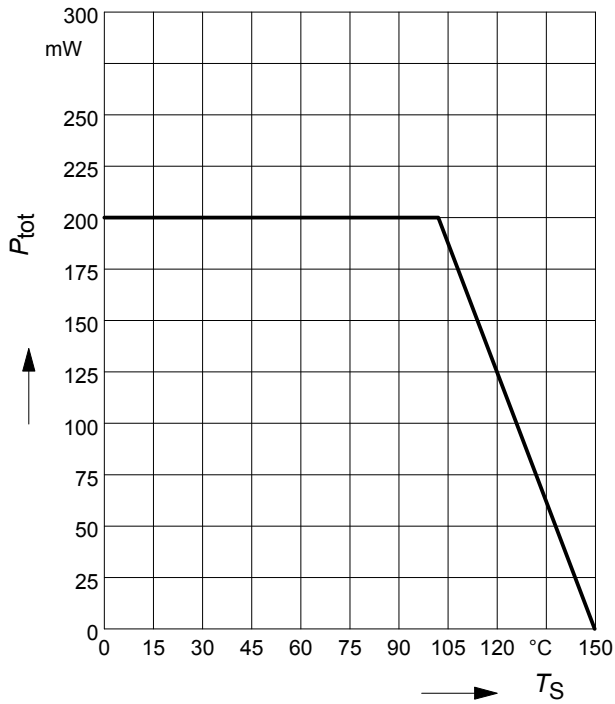
**Input off voltage  $V_{i(off)} = f(I_C)$**

$V_{CE} = 5\text{ V}$  (common emitter configuration)



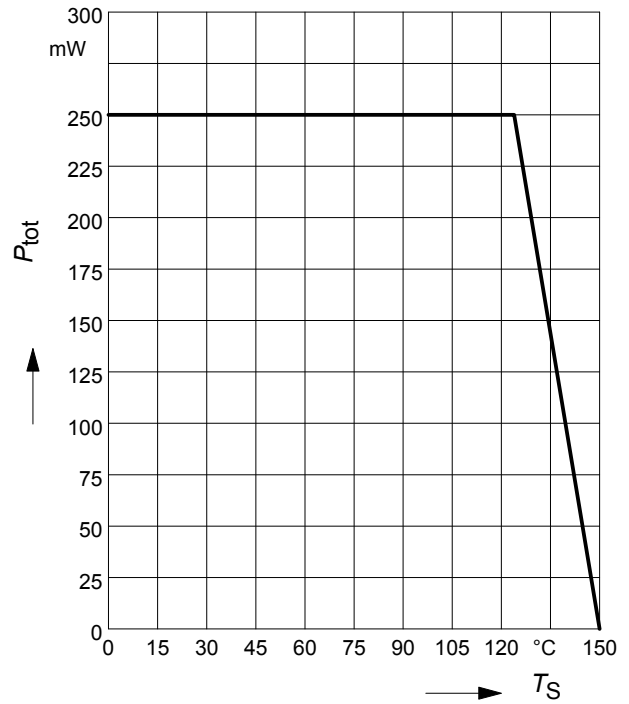
**Total power dissipation  $P_{tot} = f(T_S)$**

BCR166



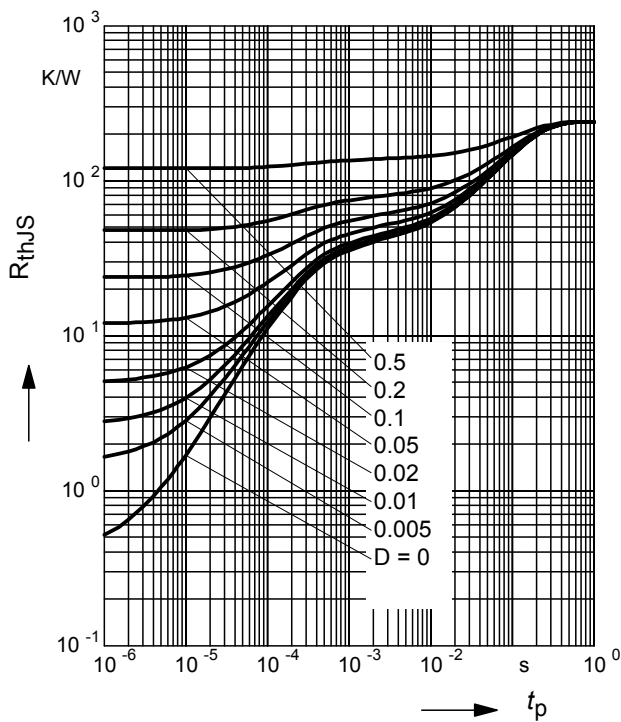
**Total power dissipation  $P_{tot} = f(T_S)$**

BCR166W



**Permissible Pulse Load  $R_{thJS} = f(t_p)$**

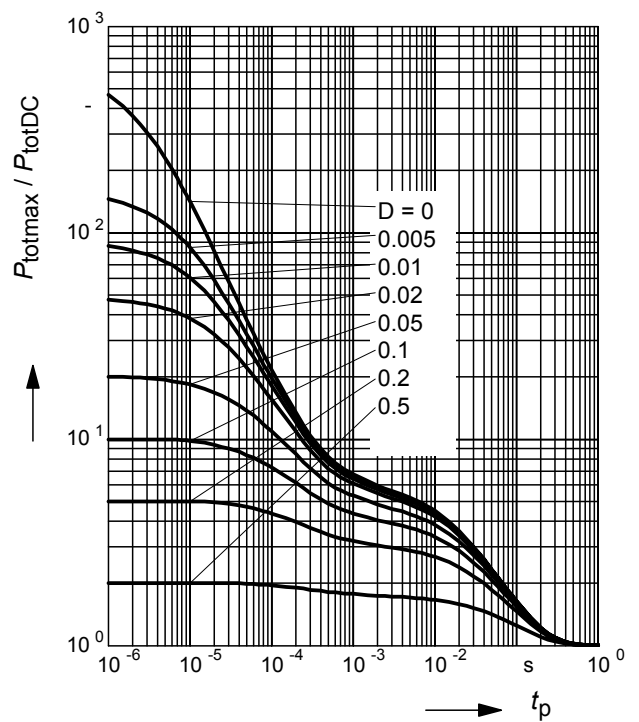
BCR166



**Permissible Pulse Load**

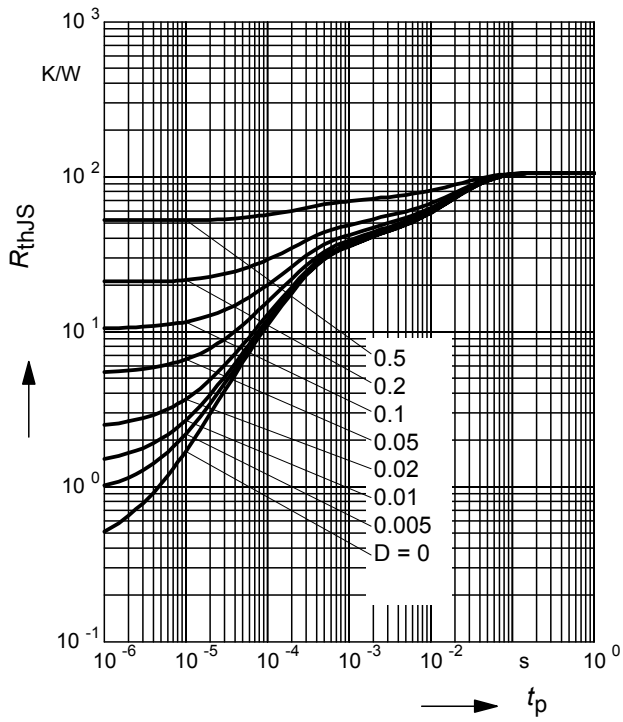
$P_{totmax}/P_{totDC} = f(t_p)$

BCR166



**Permissible Puls Load  $R_{thJS} = f(t_p)$**

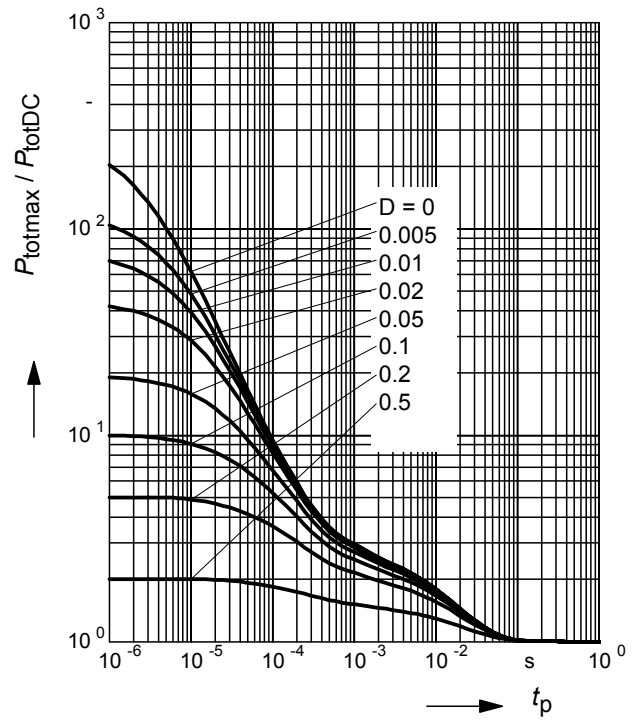
BCR166W



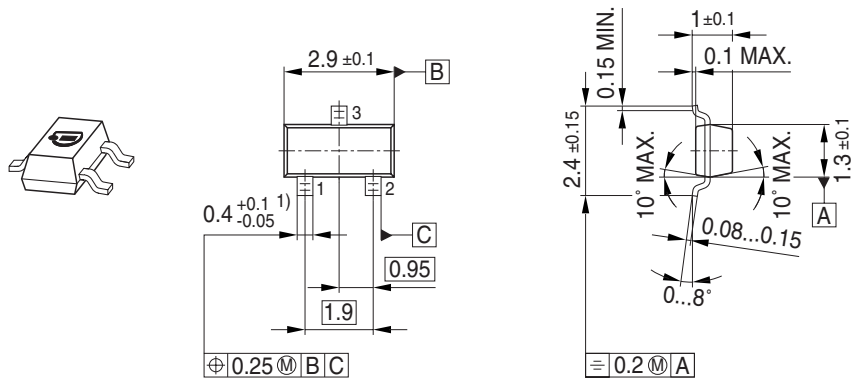
**Permissible Pulse Load**

$P_{totmax}/P_{totDC} = f(t_p)$

BCR166W

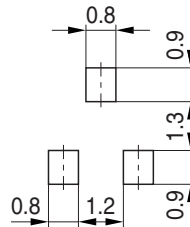


Package Outline

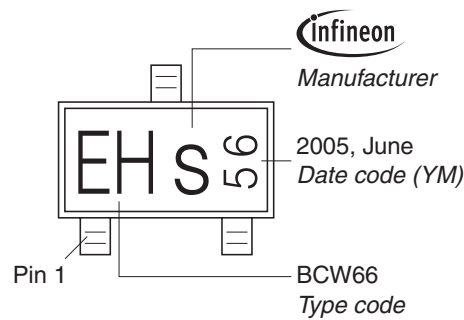


1) Lead width can be 0.6 max. in dambar area

Foot Print

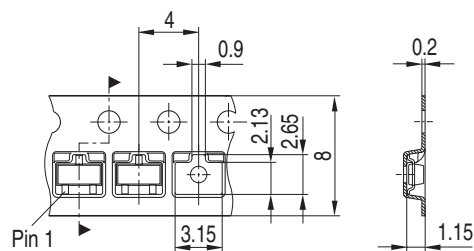


Marking Layout (Example)

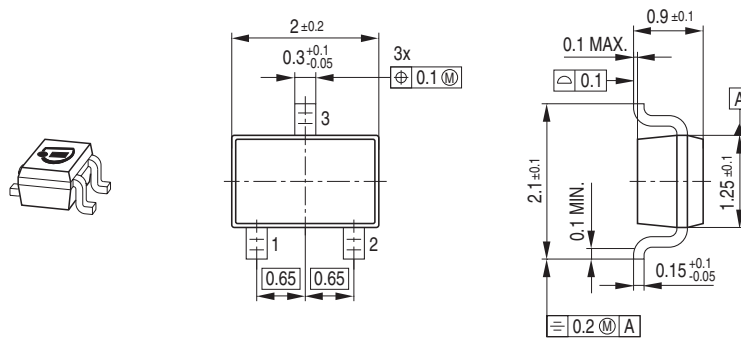


Standard Packing

Reel  $\varnothing$ 180 mm = 3.000 Pieces/Reel  
 Reel  $\varnothing$ 330 mm = 10.000 Pieces/Reel



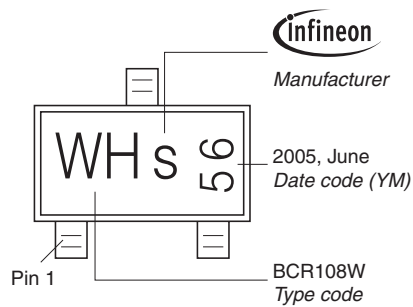
Package Outline



Foot Print

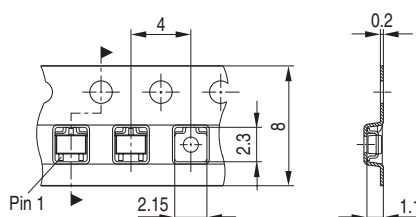


Marking Layout (Example)



Standard Packing

Reel  $\varnothing$ 180 mm = 3.000 Pieces/Reel  
 Reel  $\varnothing$ 330 mm = 10.000 Pieces/Reel



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