

**OptiMOS™3 Power-Transistor**
**Features**

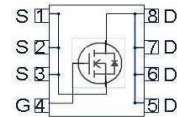
- Very low gate charge for high frequency applications
- Optimized for dc-dc conversion
- N-channel, normal level
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target application
- Halogen-free according to IEC61249-2-21


**Product Summary**

$V_{DS}$	100	V
$R_{DS(on),max}$	44	mΩ
$I_D$	18	A

**PG-TSDSON-8**


Type	Package	Marking
BSZ440N10NS3 G	PG-TDSON-8	440N10N


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C=25\text{ °C}$	18	A
		$T_C=100\text{ °C}$	11	
		$T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}^2)$	5.3	
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	72	
Avalanche energy, single pulse	$E_{AS}$	$I_D=12\text{ A}$ , $R_{GS}=25\text{ Ω}$	17	mJ
Gate source voltage	$V_{GS}$		±20	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	29	W
Operating and storage temperature	$T_j$ , $T_{stg}$		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{thJC}$		-	-	4.3	K/W
Thermal resistance, junction - ambient	$R_{thJA}$	6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	50	

**Electrical characteristics, at  $T_j=25$  °C, unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0$ V, $I_D=1$ mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=12$ $\mu$ A	2	2.7	3.5	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=100$ V, $V_{GS}=0$ V, $T_j=25$ °C	-	0.01	1	$\mu$ A
		$V_{DS}=100$ V, $V_{GS}=0$ V, $T_j=125$ °C	-	10	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20$ V, $V_{DS}=0$ V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10$ V, $I_D=12$ A	-	38	44	m $\Omega$
		$V_{GS}=6$ V, $I_D=6$ A	-	48	86	
Gate resistance	$R_G$		-	1.5	-	$\Omega$
Transconductance	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=12$ A	8	15	-	S

<sup>1)</sup>J-STD20 and JESD22

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu$ m thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> see figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V},$ $f=1\text{ MHz}$	-	480	640	pF
Output capacitance	$C_{oss}$		-	87	120	
Reverse transfer capacitance	$C_{rss}$		-	6	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V},$ $I_D=6\text{ A}, R_G=1.6\ \Omega$	-	4.3	-	ns
Rise time	$t_r$		-	1.8	-	
Turn-off delay time	$t_{d(off)}$		-	9.1	-	
Fall time	$t_f$		-	2.0	-	

**Gate Charge Characteristics<sup>4)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=50\text{ V}, I_D=6\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	2.2	-	nC
Gate to drain charge	$Q_{gd}$		-	1.3	-	
Switching charge	$Q_{sw}$		-	2.0	-	
Gate charge total	$Q_g$		-	6.8	9.1	
Gate plateau voltage	$V_{plateau}$		-	4.5	-	
Output charge	$Q_{oss}$	$V_{DD}=50\text{ V}, V_{GS}=0\text{ V}$	-	9.0	12	nC

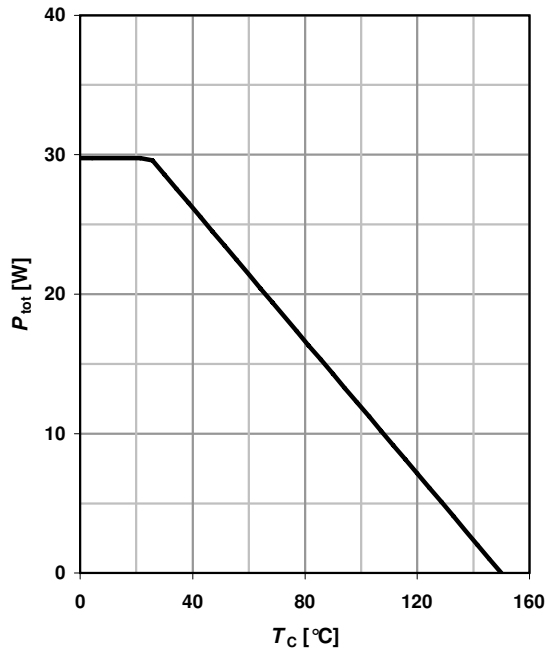
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	18	A
Diode pulse current	$I_{S,pulse}$		-	-	72	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=18\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	1	1.2	V
Reverse recovery time	$t_{rr}$	$V_R=50\text{ V}, I_F=6\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	tbd	-	ns
Reverse recovery charge	$Q_{rr}$		-	tbd	-	nC

<sup>4)</sup> See figure 16 for gate charge parameter definition

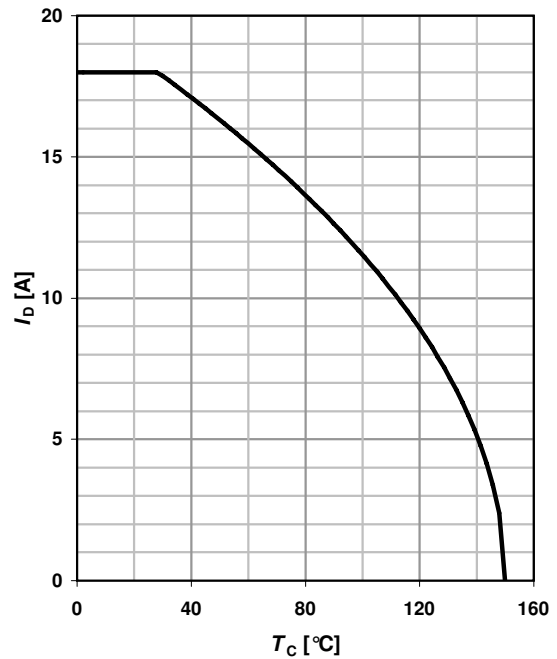
**1 Power dissipation**

$P_{tot}=f(T_C)$



**2 Drain current**

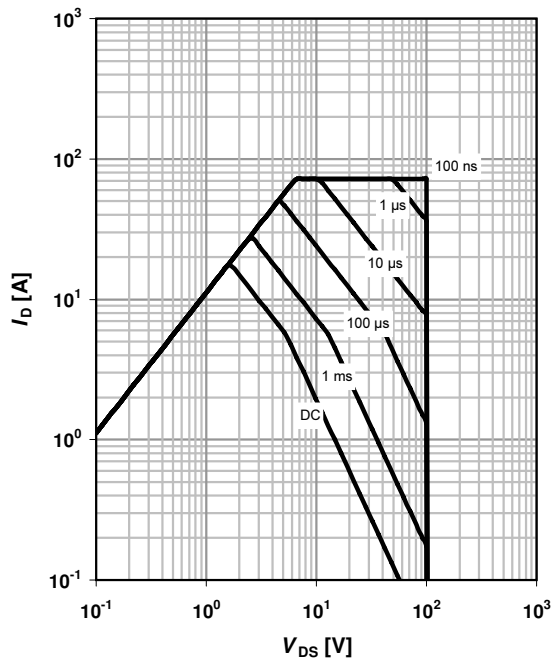
$I_D=f(T_C); V_{GS} \geq 10 V$



**3 Safe operating area**

$I_D=f(V_{DS}); T_C=25^\circ C; D=0$

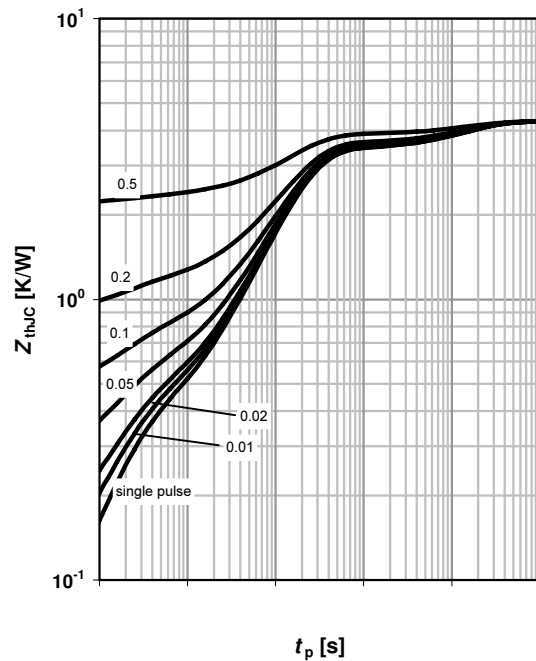
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

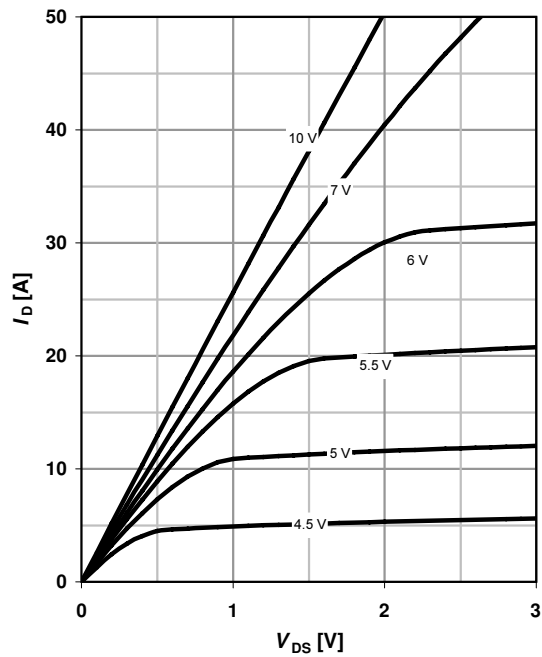
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

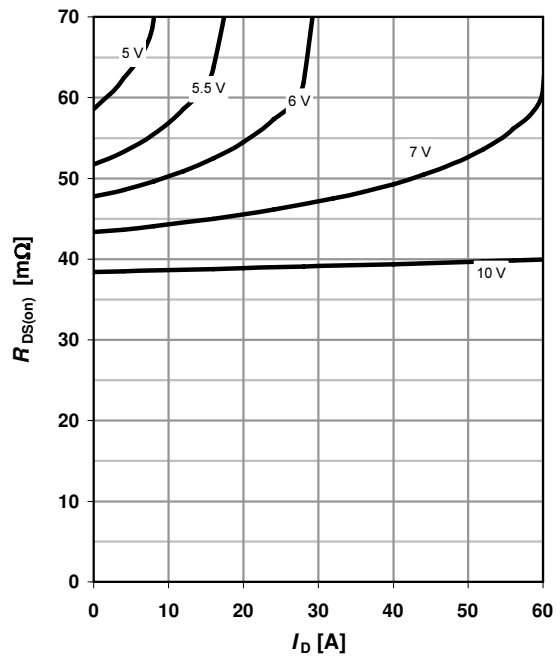
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

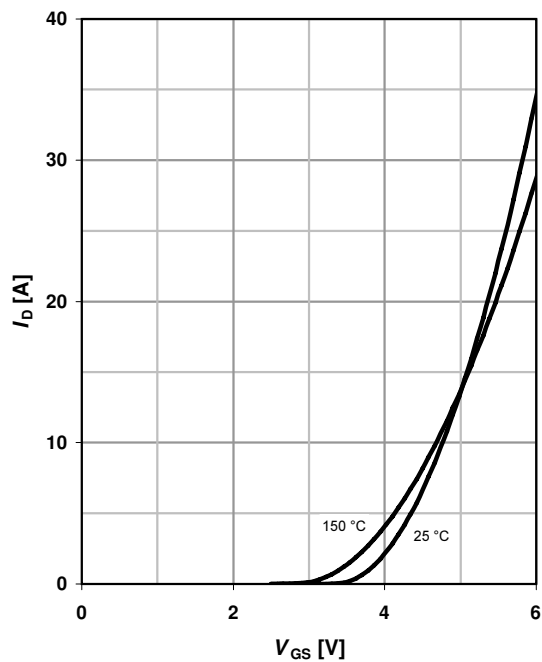
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

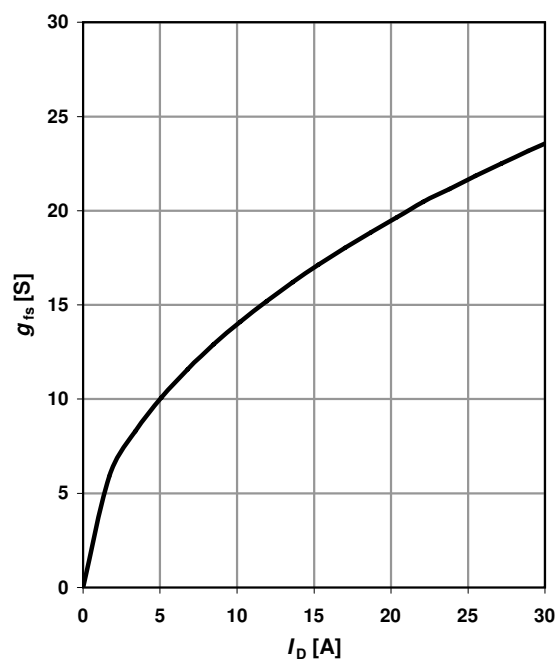
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



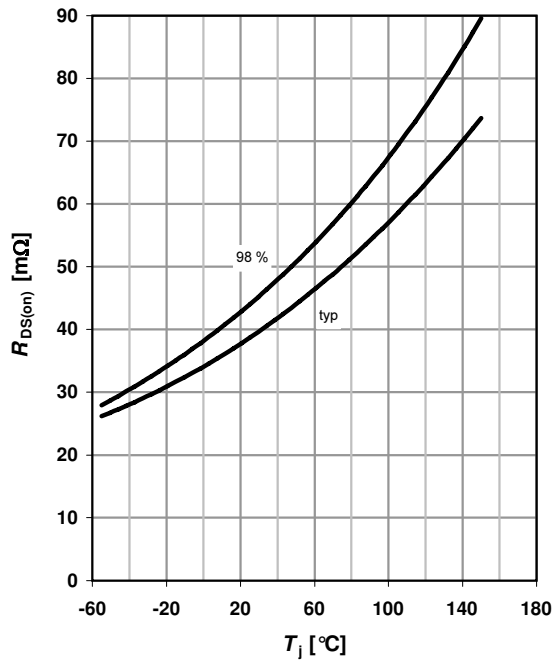
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



**9 Drain-source on-state resistance**

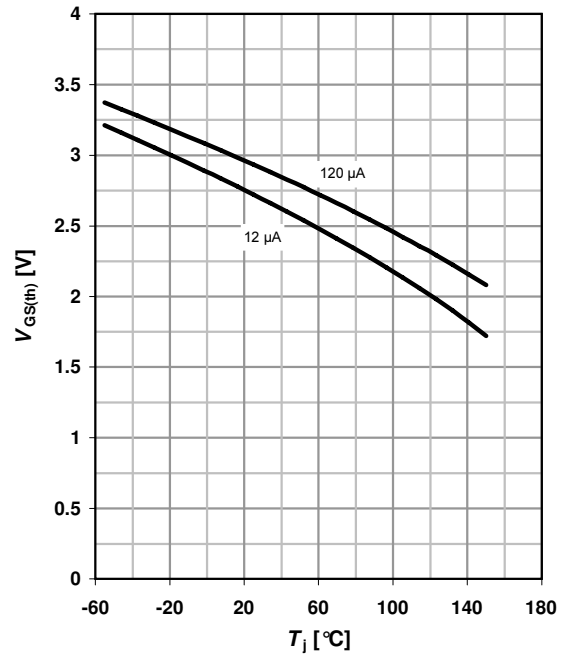
$R_{DS(on)} = f(T_j); I_D = 12 \text{ A}; V_{GS} = 10 \text{ V}$



**10 Typ. gate threshold voltage**

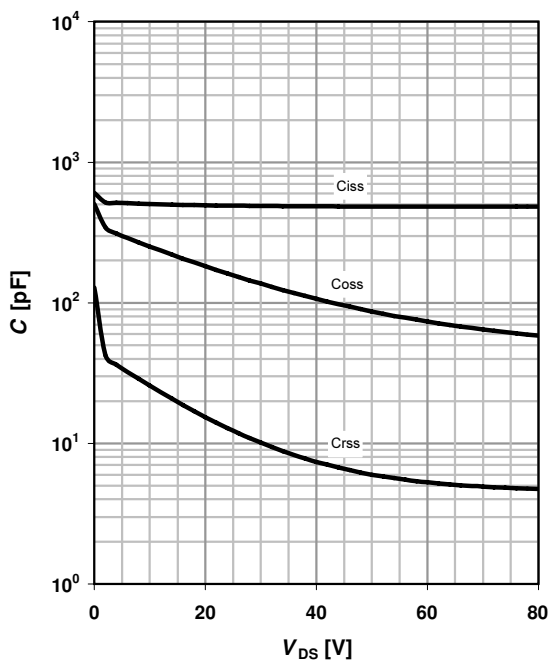
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $I_D$



**11 Typ. capacitances**

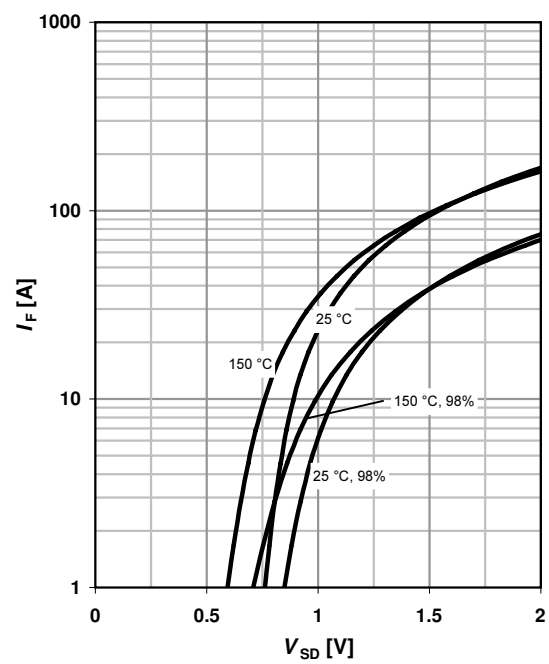
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F = f(V_{SD})$

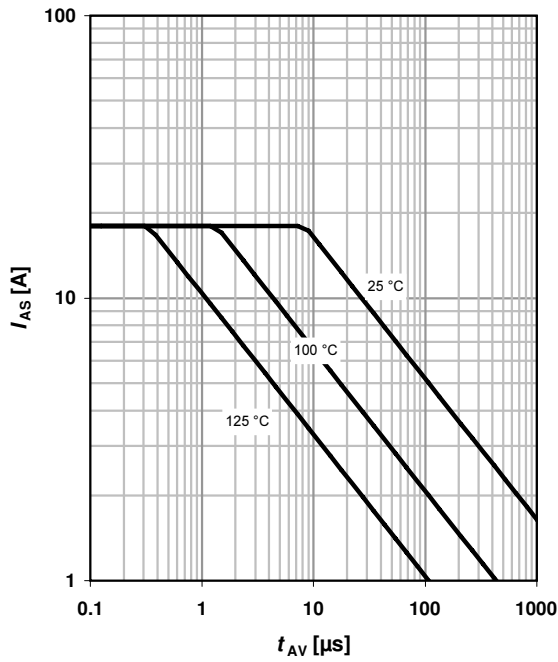
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

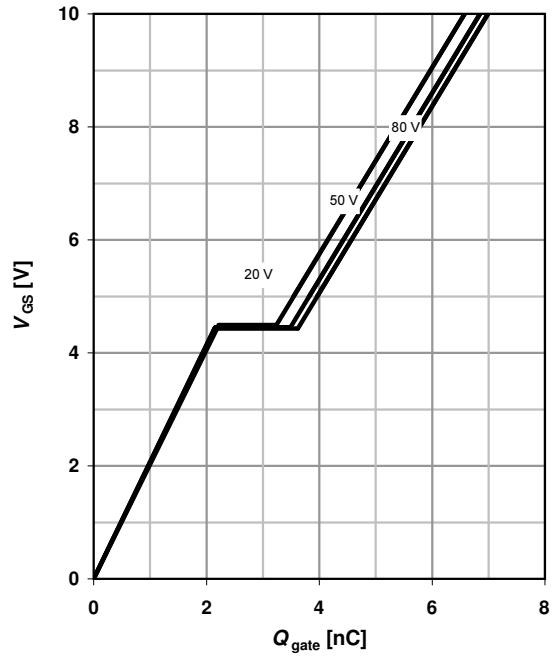
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

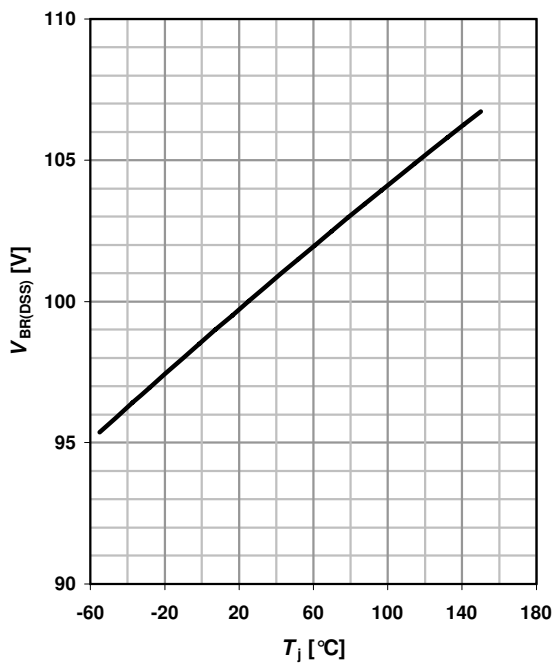
$V_{GS}=f(Q_{gate}); I_D=6 \text{ A pulsed}$

parameter:  $V_{DD}$

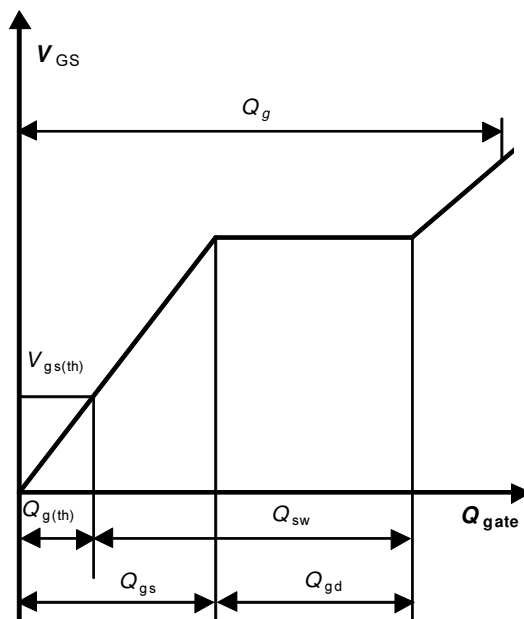


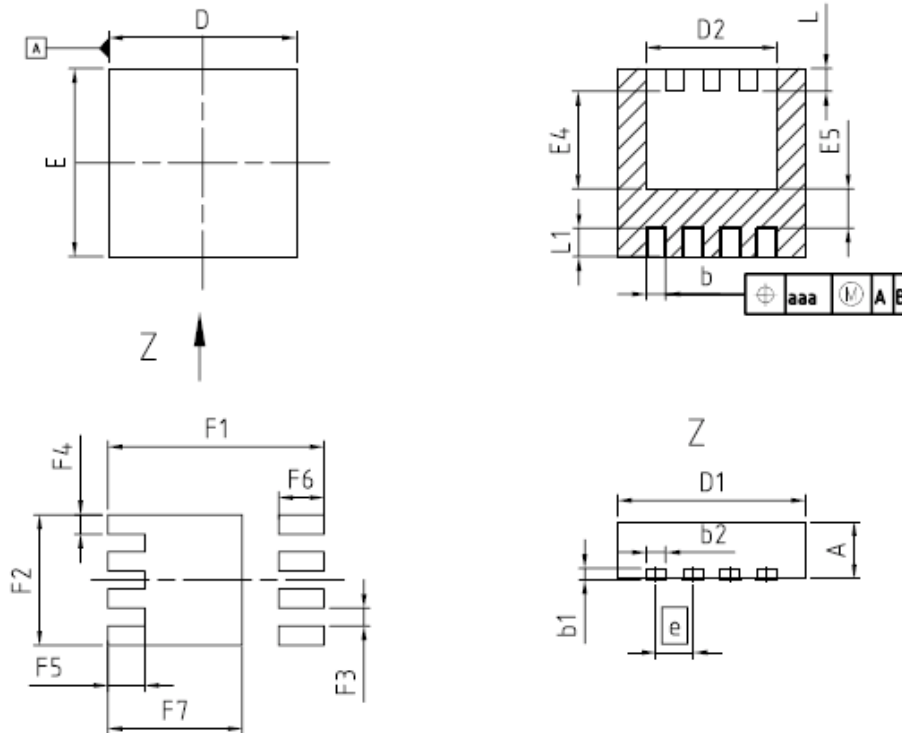
**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



**16 Gate charge waveforms**



**Package Outline: PG-TSDSON-8**


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0,90	1,10	0,035	0,043
b	0,24	0,44	0,009	0,017
b1	0,10	0,30	0,004	0,012
b2	0,20	0,44	0,008	0,017
D=D1	3,20	3,40	0,126	0,134
D2	2,15	2,45	0,085	0,096
E	3,20	3,40	0,126	0,134
E4	1,60	1,81	0,063	0,071
E5	0,59	0,86	0,023	0,034
e	0,65		0,026	
N	8		8	
L	0,30	0,56	0,012	0,022
L1	0,33	0,60	0,013	0,024
aaa	0,25		0,010	
F1	3,80		0,150	
F2	2,29		0,090	
F3	0,31		0,012	
F4	0,34		0,013	
F5	0,65		0,026	
F6	0,80		0,031	
F7	2,36		0,093	

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