HIGH-SPEED 4K x 8 FourPort™ STATIC RAM

IDT7054S/L

Features

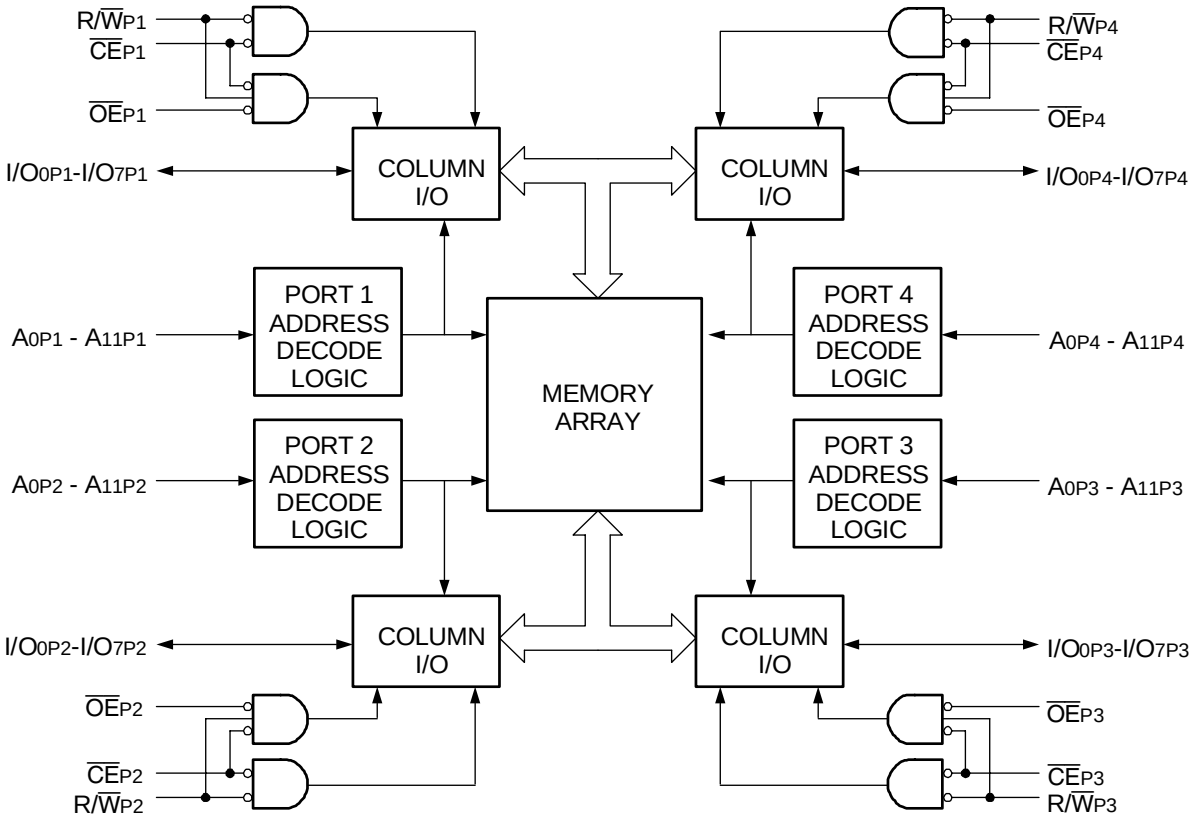
- **High-speed access**
  - *Commercial: 20/25/35ns (max.)*
  - *Industrial: 25ns (max.)*
  - *Military: 25/35ns (max.)*
- **Low-power operation**
  - *IDT7054S*
    Active: 750mW (typ.)
    Standby: 7.5mW (typ.)
  - *IDT7054L*
    Active: 750mW (typ.)
    Standby: 1.5mW (typ.)
- **True FourPort memory cells which allow simultaneous access of the same memory locations**
- **Fully asynchronous operation from each of the four ports: P1, P2, P3, and P4**
- **TTL-compatible; single 5V (±10%) power supply**
- **Available in 128 pin Thin Quad Flatpack and 108 pin PGA packages**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**

Description

The IDT7054 is a high-speed 4K x 8 FourPort™ Static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort Static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT7054 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to

Functional Block Diagram



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externally arbitrated or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7054 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CMOS high-performance technology, this FourPort SRAM typically operates on only 750mW of power. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50µW from a 2V battery.

The IDT7054 is packaged in a ceramic 108-pin Pin Grid Array (PGA) and a 128-pin Thin Quad Flatpack (TQFP). The military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations[1,2,3]

11/14/01

	A	B	C	D	E	F	G	H	J	K	L	M	
12	81 R/$\overline{W}$ P2	80 A_{11} P2	77 A_7 P2	74 A_5 P2	72 A_3 P2	69 A_0 P2	68 A_0 P3	65 A_3 P3	63 A_5 P3	60 A_7 P3	57 A_{11} P3	54 R/$\overline{W}$ P3	12
11	84 NC	83 $\overline{OE}$ P2	78 A_8 P2	76 A_{10} P2	73 A_4 P2	70 A_1 P2	67 A_1 P3	64 A_4 P3	61 A_{10} P3	59 A_8 P3	56 $\overline{OE}$ P3	53 NC	11
10	87 A_2 P1	86 A_1 P1	82 $\overline{CE}$ P2	79 A_9 P2	75 A_6 P2	71 A_2 P2	66 A_2 P3	62 A_6 P3	58 A_9 P3	55 $\overline{CE}$ P3	51 A_1 P4	50 A_2 P4	10
09	90 A_5 P1	88 A_3 P1	85 A_0 P1							52 A_0 P4	49 A_3 P4	47 A_5 P4	09
08	92 A_{10} P1	91 A_6 P1	89 A_4 P1							48 A_4 P4	46 A_6 P4	45 A_{10} P4	08
07	95 A_8 P1	94 A_7 P1	93 V_{CC}			IDT7054G G108-1[4]				44 GND	43 A_7 P4	42 A_8 P4	07
06	96 A_9 P1	97 A_{11} P1	98 $\overline{CE}$ P1			108-Pin PGA Top View[5]				39 $\overline{CE}$ P4	40 A_{11} P4	41 A_9 P4	06
05	99 R/$\overline{W}$ P1	100 $\overline{OE}$ P1	102 I/O_0 P1							35 GND	37 $\overline{OE}$ P4	38 R/$\overline{W}$ P4	05
04	101 NC	103 I/O_1 P1	106 GND							31 GND	34 I/O_7 P4	36 NC	04
03	104 I/O_2 P1	105 I/O_3 P1	1 I/O_6 P1	4 V_{CC}	8 GND	12 V_{CC}	17 V_{CC}	21 GND	25 V_{CC}	28 I/O_2 P4	32 I/O_5 P4	33 I/O_6 P4	03
02	107 I/O_4 P1	2 I/O_7 P1	5 I/O_0 P2	7 I/O_2 P2	10 I/O_4 P2	13 I/O_6 P2	16 I/O_1 P3	19 I/O_3 P3	22 I/O_5 P3	24 I/O_7 P3	29 I/O_3 P4	30 I/O_4 P4	02
01	108 I/O_5 P1	3 NC	6 I/O_1 P2	9 I/O_3 P2	11 I/O_5 P2	14 I/O_7 P2	15 I/O_0 P3	18 I/O_2 P3	20 I/O_4 P3	23 I/O_6 P3	26 I/O_0 P4	27 I/O_1 P4	01

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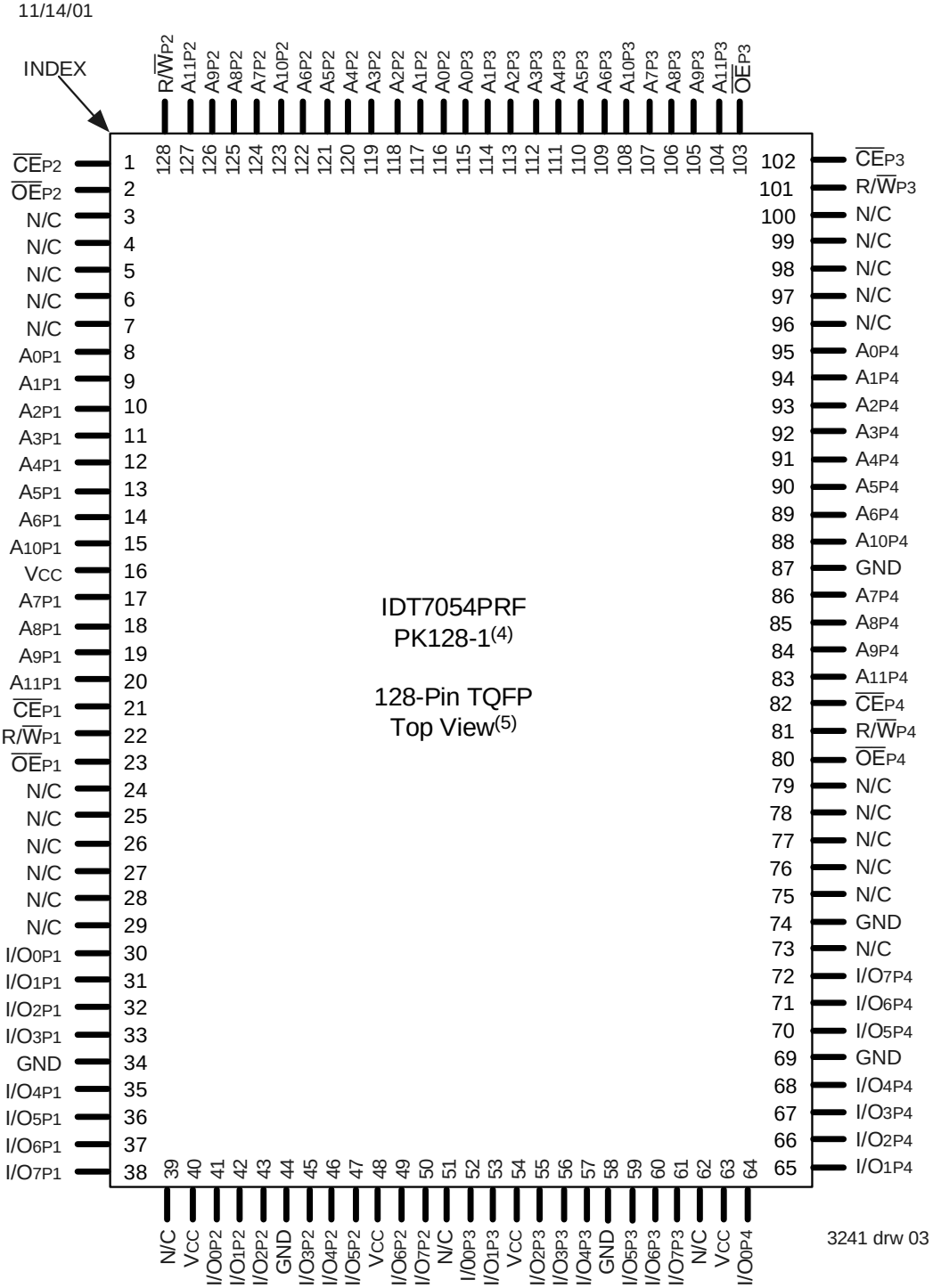
NOTES:
1. All V_{CC} pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately 1.21 in x 1.21 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations[1,2,3] (con't.)

11/14/01



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NOTES:

1. All VCC pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately 14mm x 20mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations[1,2]

NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0[2]	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

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NOTES:
1. VIL ≥ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 10%.

Capacitance[1]

(TA = +25°C, f = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions[2]	Max.	Unit
CIN	Input Capacitance	VIN = 0V	9	pF
COUT	Output Capacitance	VOUT = 0V	10	pF

3241 tbl 03

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and the output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage[1]

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3241 tbl 04

NOTES:
1. This is the parameter TA. This is the "instant on" case temperature.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-65 to +150	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

3241 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,5] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Condition	Version		7054X20 Com'l Only TYP.[2]	7054X20 Com'l Only Max.	7054X25 Com'l, Ind & Military TYP.[2]	7054X25 Com'l, Ind & Military Max.	7054X35 Com'l & Military TYP.[2]	7054X35 Com'l & Military Max.	Unit
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE}$ = V_{IL} Outputs Disabled f = 0[3]	COM'L.	S	150	300	150	300	150	300	mA
				L	150	250	150	250	150	250	
			MIL. & IND.	S	—	—	150	360	150	360	mA
				L	—	—	150	300	150	300	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE}$ = V_{IL} Outputs Disabled f = f_{MAX}[4]	COM'L.	S	240	370	225	350	210	335	mA
				L	210	325	195	305	180	290	
			MIL. & IND.	S	—	—	225	400	210	395	mA
				L	—	—	195	340	180	330	
I_{SB}	Standby Current (All Ports - TTL Level Inputs)	$\overline{CE}$ = V_{IH} f = f_{MAX}[4]	COM'L.	S	70	95	60	85	40	75	mA
				L	60	80	50	70	35	60	
			MIL. & IND.	S	—	—	60	115	40	110	mA
				L	—	—	50	85	35	80	
I_{SB1}	Full Standby Current (All Ports - All CMOS Level Inputs)	All Ports $\overline{CE} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[3]	COM'L.	S	1.5	15	1.5	15	1.5	15	mA
				L	0.3	1.5	0.3	1.5	0.3	1.5	
			MIL. & IND.	S	—	—	1.5	30	1.5	30	mA
				L	—	—	0.3	4.5	0.3	4.5	

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NOTES:
1. 'X' in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C and are not production tested.
3. f = 0 means no address or control lines change.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
5. For the case of one port, divide the appropriate current above by four.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7054S Min.	7054S Max.	7054L Min.	7054L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2674 tbl 07

NOTE:
1. At $V_{CC} \leq$ 2.0V input leakages are undefined.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

3241 tbl 08

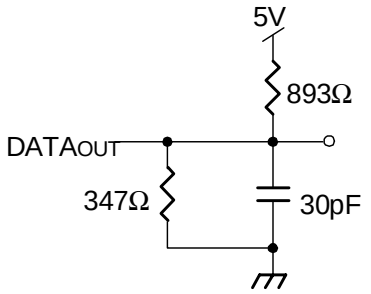

Figure 1. AC Output Test Load

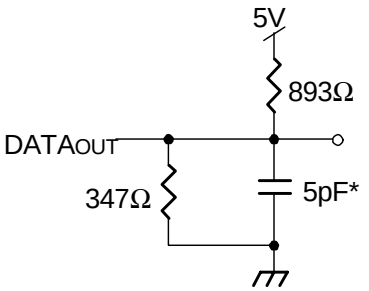

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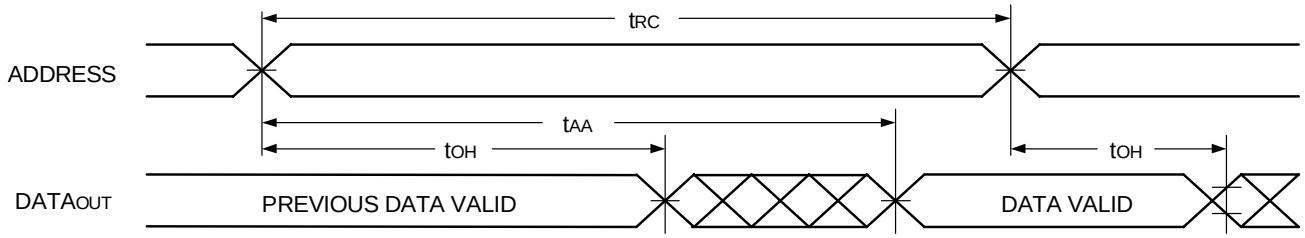
Figure 2. Output Test Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig

Timing Waveform of Read Cycle No. 1, Any Port(1)



3241 drw 05

NOTE:
1. R/$\overline{W}$ = V_{IH}, $\overline{OE}$ = V_{IL}, and $\overline{CE}$ = V_{IL}.

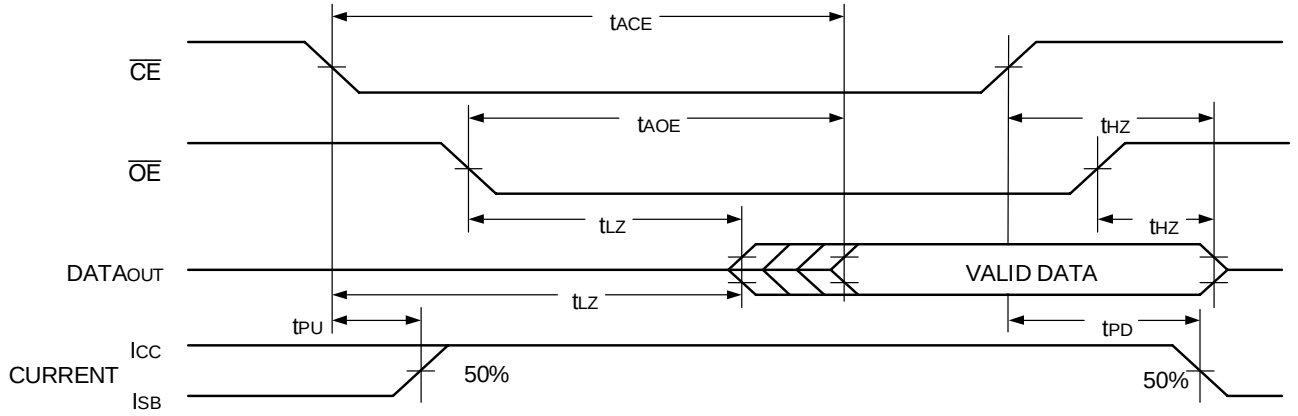
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[3]

Symbol	Parameter	7054X20 Com'l Only		7054X25 Com'l, Ind & Military		7054X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	10	—	15	—	25	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1,2]	5	—	5	—	5	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	12	—	15	—	15	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	20	—	25	—	35	ns

3241 tbl 09

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. 'X' in part number indicates power rating (S or L).

Timing Waveform of Read Cycle No. 2, Any Port[1, 2]



3241 drw 06

NOTES:
1. R/$\overline{W}$ = V_{IH} for Read Cycles.
2. Addresses valid prior to or coincident with $\overline{CE}$ transition LOW.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[5]

Symbol	Parameter	7054X20 Com'l Only		7054X25 Com'l, Ind & Military		7054X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{EW}	Chip Enable to End-of-Write	15	—	20	—	30	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width[3]	15	—	20	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	15		20	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	15	—	15	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	12	—	15	—	15	ns
t_{OW}	Output Active from End-of-Write[1,2]	0	—	0	—	0	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	35	—	45	—	55	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	30	—	35	—	45	ns

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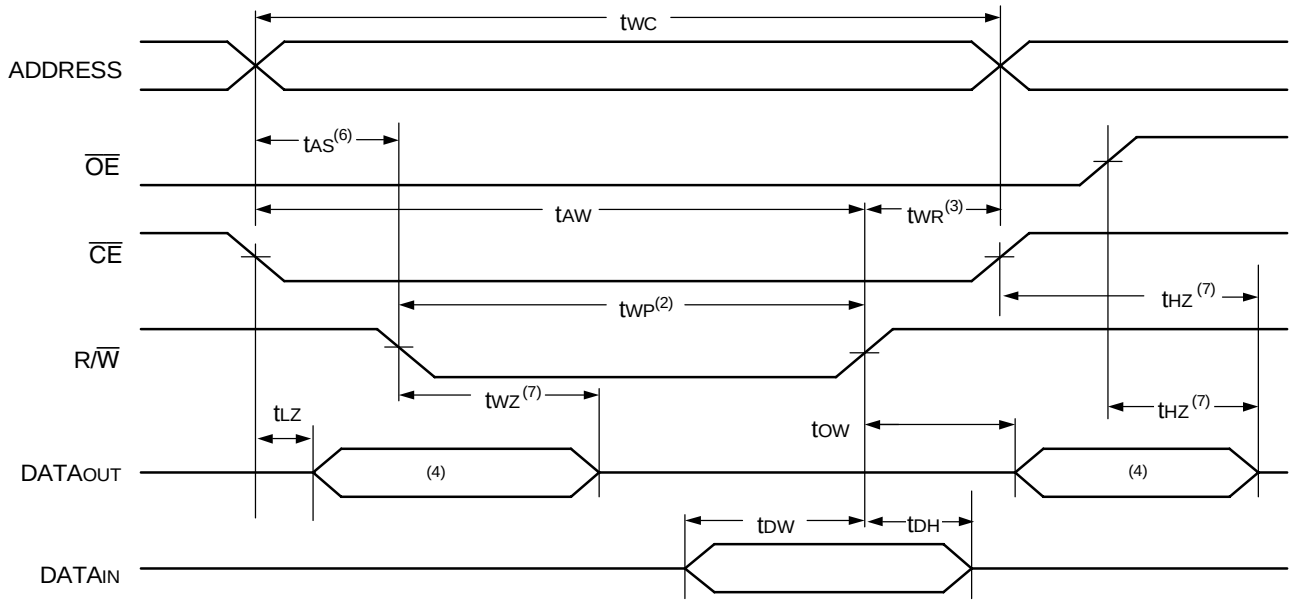
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. If $\overline{OE}$ = V_{IL} during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ = V_{IH} during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}. Specified for $\overline{OE}$ = V_{IH} (refer to "Timing Waveform of Write Cycle", Note 8).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. 'X' in part number indicates power rating.

Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(5,8)



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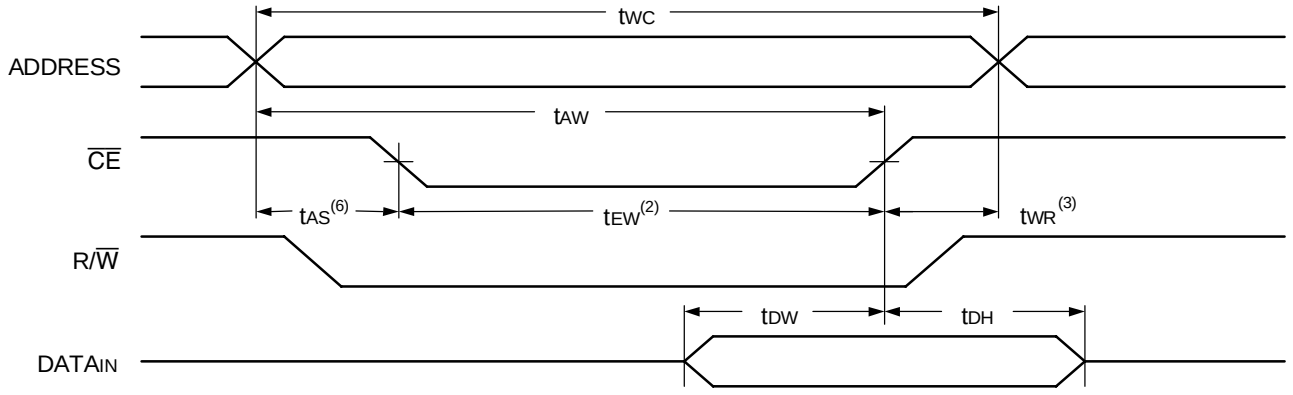
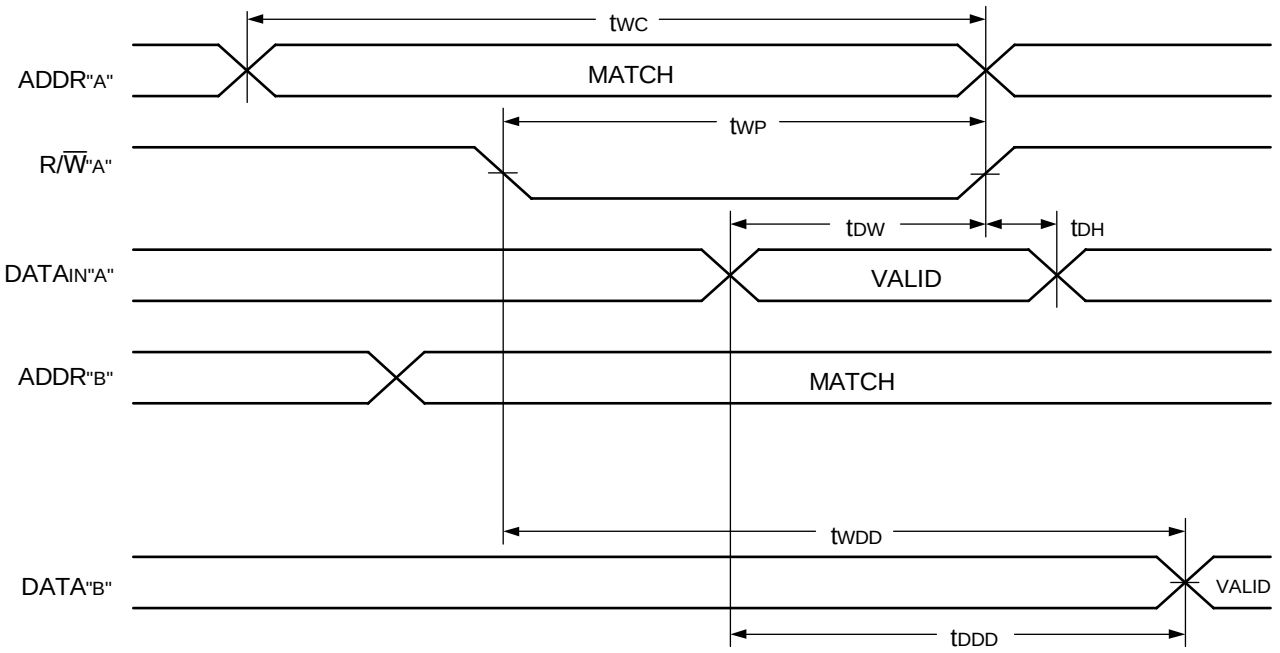
Timing Waveform of Write Cycle No. 2, $\overline{CE}$ Controlled Timing(1,5)



3241 drw 08

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ = VIH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a $\overline{CE}$ = VIL and a R/$\overline{W}$ = VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ = VIH to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ = VIL transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed but is not production tested.
8. If $\overline{OE}$ = VIL during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ = VIH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

Timing Waveform of Write with Port-to-Port Read(1, 2)



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NOTES:
1. $\overline{OE}$ = VIL for the reading ports.
2. All timing is the same for left and right ports. Port "A" may be either of the four ports and Port "B" is any other port.

Functional Description

The IDT7054 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ = VIH). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table.

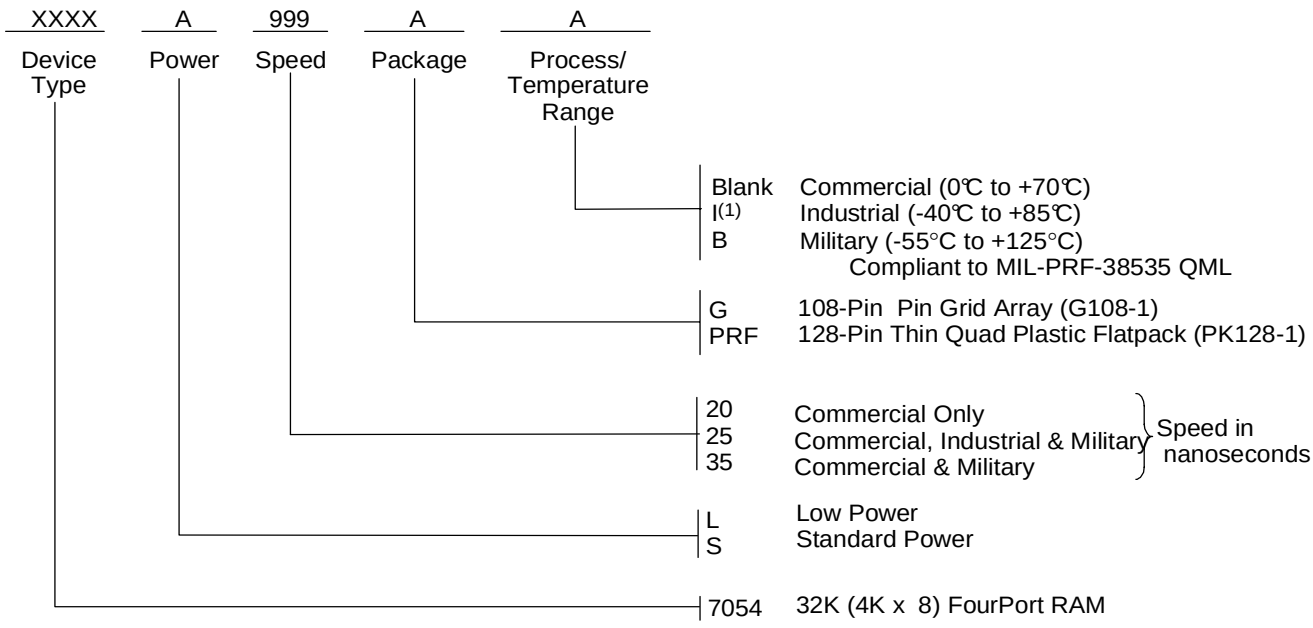
Table I – Read/Write Control

Any Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D0-7	Function
X	H	X	Z	Port Deselected: Power-Down
X	H	X	Z	$\overline{CE}_{P1}$=$\overline{CE}_{P2}$=$\overline{CE}_{P3}$=$\overline{CE}_{P4}$=VIH Power Down Mode ISB or ISB1
L	L	X	DATAIN	Data on port written into memory(2)
H	L	L	DATAOUT	Data in memory output on port
X	X	H	Z	Outputs Disabled

3241 tbl 11

NOTES:
1. "H" = VIH, "L" = VIL, "X" = Don't Care, "Z "= High Impedance
2. For valid write operation, no more than one port can write to the same address location at the same time.

Ordering Information



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NOTE:
1. Industrial temperature range is available.
   For other speeds, packages and powers contact your sales office.

Datasheet Document History

1/18/99:	Initiated datasheet document history
	Converted to new format
	Cosmetic typographical corrections
	Added additional notes to pin configurations
6/4/99:	Changed drawing format
	Page 1 Corrected DSC number
9/1/99:	Removed Preliminary
11/10/99:	Replaced IDT logo
5/23/00:	Page 4 Increased storage temperature parameter
	Clarified T_A parameter
	Page 5 DC Electrical parameters–changed wording from "open" to "disabled"
	Changed ±200mV to 0mV in notes
10/22/01:	Page 2 & 3 Added date revision for pin configurations
	Page 5, 7 & 8 Added Industrial temp to column heading for 25ns speed to DC & AC Electrical Characteristics
	Page 11 Added Industrial temp offering to 25ns ordering information
	Page 4, 5, 7 & 8 Removed Industrial temp footnote from all tables
	Page 6 Changed 5ns to 3ns in AC Test Conditions table
	Page 1 & 11 Replace ™ logo with ® logo
01/29/09:	Page 11 Removed "IDT" from orderable part number

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