IDT
256K X 36, 512K X 18
3.3V Synchronous SRAMs
3.3V I/O, Burst Counter
Flow-Through Outputs, Single Cycle Deselect

IDT71V67703
IDT71V67903

Features

- **256K x 36, 512K x 18 memory configurations**
- **Supports fast access times:**
  - *7.5ns up to 117MHz clock frequency*
  - *8.0ns up to 100MHz clock frequency*
  - *8.5ns up to 87MHz clock frequency*
- **$\overline{LBO}$ input selects interleaved or linear burst mode**
- **Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BW}$x)**
- **3.3V core power supply**
- **Power down controlled by ZZ input**
- **3.3V I/O supply (V_{DDQ})**
- **Packaged in a JEDEC Standard 100-pin thin plastic quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA).**

Description

The IDT71V67703/7903 are high-speed SRAMs organized as 256K x 36/512K x 18. The IDT71V67703/7903 SRAMs contain write, data, address and control registers. There are no registers in the data output path (flow-through architecture). Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V67703/7903 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will flow-through from the array after a clock-to-data access time delay from the rising clock edge of the same cycle. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71V67703/7903 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Pin Description Summary

A_0-A_{18}	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS}_1$	Chip Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$[1]	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	N/A
V_{SS}	Ground	Supply	N/A

5309 tbl 01

NOTE:

1. $\overline{BW}_3$ and $\overline{BW}_4$ are not applicable for the IDT71V67903.

DSC-5309/05

Pin Definitions[1]

Symbol	Pin Function	I/O	Active	Description
A_0-A_{18}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combi-nation of the rising edge of CLK and $\overline{ADSC}$ Low or $\overline{ADSP}$ Low and $\overline{CE}$ Low.
$\overline{ADSC}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{ADSC}$ is an active LOW input that is used to load the address registers with new addresses.
$\overline{ADSP}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{ADSP}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSP}$ is gated by $\overline{CE}$.
$\overline{ADV}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{ADV}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{BWE}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{BW}_1$-$\overline{BW}_4$. If $\overline{BWE}$ is LOW at the rising edge of CLK then $\overline{BW}x$ inputs are passed to the next stage in the circuit. If $\overline{BWE}$ is HIGH then the byte write inputs are blocked and only $\overline{GW}$ can initiate a write cycle.
$\overline{BW}_1$-$\overline{BW}_4$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{BW}_1$ controls I/O$_{0-7}$, I/O$_{P1}$, $\overline{BW}_2$ controls I/O$_{8-15}$, I/O$_{P2}$, etc. Any active byte write causes all outputs to be disabled.
$\overline{CE}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{CE}$ is used with CS$_0$ and $\overline{CS}_1$ to enable the IDT71V67703/7903. $\overline{CE}$ also gates $\overline{ADSP}$.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS$_0$	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS$_0$ is used with $\overline{CE}$ and $\overline{CS}_1$ to enable the chip.
$\overline{CS}_1$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{CS}_1$ is used with $\overline{CE}$ and CS$_0$ to enable the chip.
$\overline{GW}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{GW}$ supersedes individual byte write enables.
I/O$_0$-I/O$_{31}$ I/O$_{P1}$-I/O$_{P4}$	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. The data input path is registered, triggered by the rising edge of CLK. The data output path is flow-through (no output register).
$\overline{LBO}$	Linear Burst Order	I	LOW	Asynchronous burst order selection input. When $\overline{LBO}$ is HIGH, the inter-leaved burst sequence is selected. When $\overline{LBO}$ is LOW the Linear burst sequence is selected. $\overline{LBO}$ is a static input and must not change state while the device is operating.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{OE}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedance state.
V$_{DD}$	Power Supply	N/A	N/A	3.3V core power supply.
V$_{DDQ}$	Power Supply	N/A	N/A	3.3V I/O Supply.
V$_{SS}$	Ground	N/A	N/A	Ground.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the device.
ZZ	Sleep Mode	1	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V67703/7903 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

5309 tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram
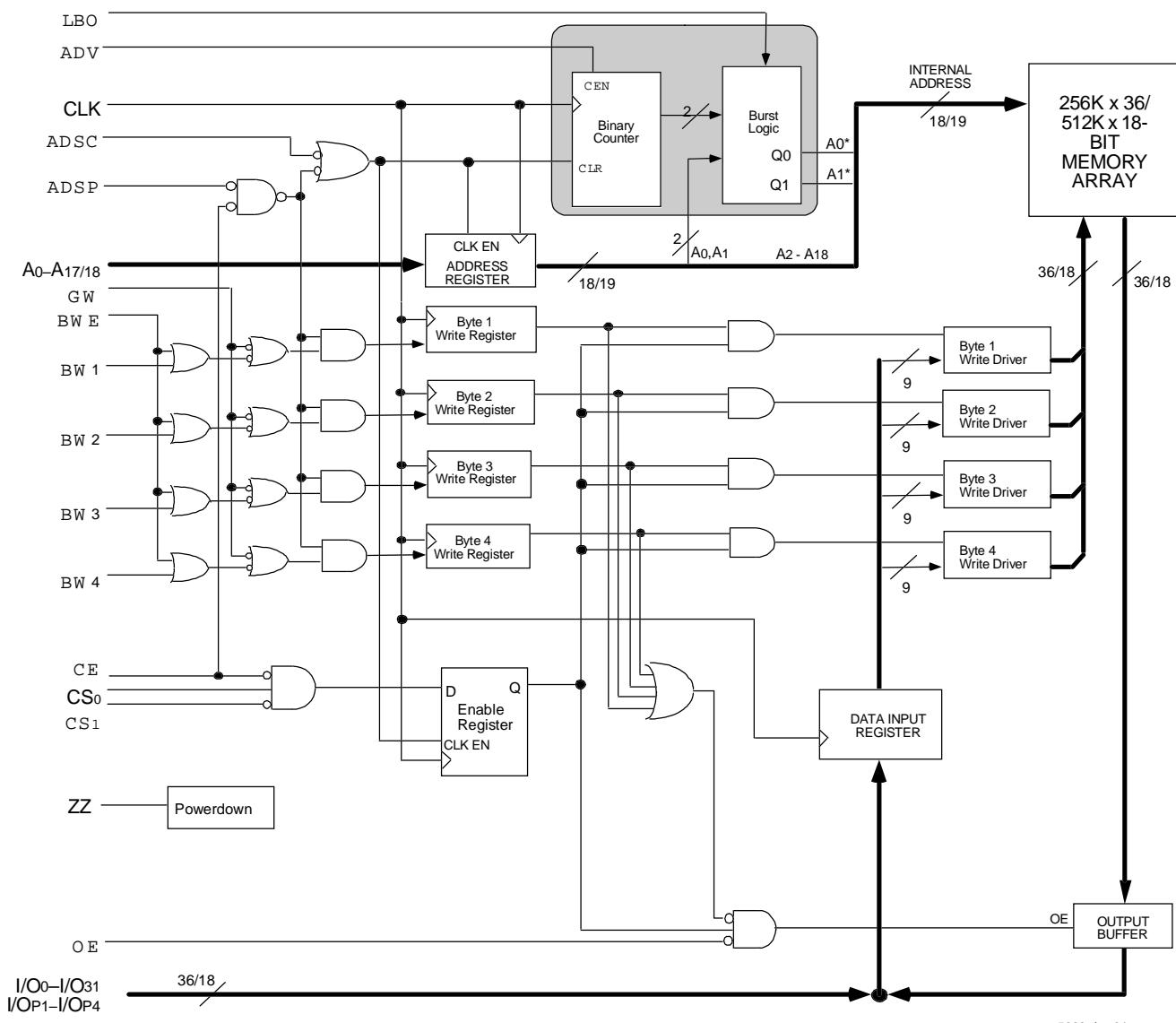
5309 drw 01

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}[3,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}[4,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}[5,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A[7]	Operating Temperature	-0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5309 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. T_A is the "instant on" case temperature.

Recommended Operating Temperature Supply Voltage

Grade	Temperature[1]	V_{SS}	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

5309 tbl 04

NOTE:
1. T_A is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD} +0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ} +0.3	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

5309 tbl 05

NOTE:
1. V_{IL} (min) = -1.0V for pulse width less than $t_{CYC/2}$, once per cycle.

100-Pin TQFP Capacitance
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5309 tbl 07

119 BGA Capacitance
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5309 tbl 07a

165 fBGA Capacitance
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5309 tbl 07b

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Pin Configuration – 256K x 36, 100-Pin TQFP

Top pins (100–81): A6, A7, $\overline{CE}$, $\overline{CS_0}$, $\overline{BW_4}$, $\overline{BW_3}$, $\overline{BW_2}$, $\overline{BW_1}$, CS1, VDD, VSS, CLK, $\overline{GW}$, $\overline{BWE}$, $\overline{OE}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, A8, A9

Left pins (1–30):
1 I/OP3
2 I/O16
3 I/O17
4 VDDQ
5 VSS
6 I/O18
7 I/O19
8 I/O20
9 I/O21
10 VSS
11 VDDQ
12 I/O22
13 I/O23
14 VSS(1)
15 VDD
16 NC
17 VSS
18 I/O24
19 I/O25
20 VDDQ
21 VSS
22 I/O26
23 I/O27
24 I/O28
25 I/O29
26 VSS
27 VDDQ
28 I/O30
29 I/O31
30 I/OP4

Right pins (80–51):
80 I/OP2
79 I/O15
78 I/O14
77 VDDQ
76 VSS
75 I/O13
74 I/O12
73 I/O11
72 I/O10
71 VSS
70 VDDQ
69 I/O9
68 I/O8
67 VSS
66 NC
65 VDD
64 ZZ(2)
63 I/O7
62 I/O6
61 VDDQ
60 VSS
59 I/O5
58 I/O4
57 I/O3
56 I/O2
55 VSS
54 VDDQ
53 I/O1
52 I/O0
51 I/OP1

Bottom pins (31–50): $\overline{LBO}$, A5, A4, A3, A2, A1, A0, NC, NC, VSS, VDD, NC, A17, A10, A11, A12, A13, A14, A15, A16

5309 drw 02a

Top View

NOTES:
1. Pin 14 does not have to be directly connected to VSS as long as the input voltage is $\leq V_{IL}$.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 512K x 18, 100-Pin TQFP

Top side pins (100–81): A6, A7, $\overline{CE}$, CS0, NC, NC, $\overline{BW_2}$, $\overline{BW_1}$, CS1, VDD, VSS, CLK, GW, $\overline{BWE}$, $\overline{OE}$, $\overline{ADSC}$, $\overline{ADSP}$, ADV, A8, A9

Pin	Left side		Pin	Right side
1	NC		80	A10
2	NC		79	NC
3	NC		78	NC
4	VDDQ		77	VDDQ
5	VSS		76	VSS
6	NC		75	NC
7	NC		74	I/OP1
8	I/O8		73	I/O7
9	I/O9		72	I/O6
10	VSS		71	VSS
11	VDDQ		70	VDDQ
12	I/O10		69	I/O5
13	I/O11		68	I/O4
14	VSS(1)		67	VSS
15	VDD		66	NC
16	NC		65	VDD
17	VSS		64	ZZ(2)
18	I/O12		63	I/O3
19	I/O13		62	I/O2
20	VDDQ		61	VDDQ
21	VSS		60	VSS
22	I/O14		59	I/O1
23	I/O15		58	I/O0
24	I/OP2		57	NC
25	NC		56	NC
26	VSS		55	VSS
27	VDDQ		54	VDDQ
28	NC		53	NC
29	NC		52	NC
30	NC		51	NC

Bottom side pins (31–50): $\overline{LBO}$, A5, A4, A3, A2, A1, A0, NC, NC, VSS, VDD, NC, A18, A11, A12, A13, A14, A15, A16, A17

5309 drw 02b

Top View

NOTES:
1. Pin 14 does not have to be directly connected to VSS as long as the input voltage is ≤ VIL.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 256K x 36, 119 BGA

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	$\overline{ADSP}$	A8	A16	VDDQ
B	NC	CS_0[4]	A3	$\overline{ADSC}$	A9	A17	NC
C	NC	A7	A2	VDD	A12	A15	NC
D	I/O16	I/OP3	VSS	NC	VSS	I/OP2	I/O15
E	I/O17	I/O18	VSS	$\overline{CE}$	VSS	I/O13	I/O14
F	VDDQ	I/O19	VSS	$\overline{OE}$	VSS	I/O12	VDDQ
G	I/O20	I/O21	$\overline{BW3}$	$\overline{ADV}$	$\overline{BW2}$	I/O11	I/O10
H	I/O22	I/O23	VSS	$\overline{GW}$	VSS	I/O9	I/O8
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	I/O24	I/O26	VSS	CLK	VSS	I/O6	I/O7
L	I/O25	I/O27	$\overline{BW4}$	NC	$\overline{BW1}$	I/O4	I/O5
M	VDDQ	I/O28	VSS	$\overline{BWE}$	VSS	I/O3	VDDQ
N	I/O29	I/O30	VSS	A1	VSS	I/O2	I/O1
P	I/O31	I/OP4	VSS	A0	VSS	I/OP1	I/O0
R	NC	A5	$\overline{LBO}$	VDD	VSS[1]	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ[2]
U	VDDQ	DNU[3]	DNU[3]	DNU[3]	DNU[3]	DNU[3]	VDDQ

5309 drw 02c

Top View

Pin Configuration – 512K x 18, 119 BGA

|	1	2	3	4	5	6	7
A	VDDQ	A6	A4	$\overline{ADSP}$	A8	A16	VDDQ
B	NC	CS_0[4]	A3	$\overline{ADSC}$	A9	A18	NC
C	NC	A7	A2	VDD	A13	A17	NC
D	I/O8	NC	VSS	NC	VSS	I/OP1	NC
E	NC	I/O9	VSS	$\overline{CE}$	VSS	NC	I/O7
F	VDDQ	NC	VSS	$\overline{OE}$	VSS	I/O6	VDDQ
G	NC	I/O10	$\overline{BW2}$	$\overline{ADV}$	VSS	NC	I/O5
H	I/O11	NC	VSS	$\overline{GW}$	VSS	I/O4	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	I/O12	VSS	CLK	VSS	NC	I/O3
L	I/O13	NC	VSS	NC	$\overline{BW1}$	I/O2	NC
M	VDDQ	I/O14	VSS	$\overline{BWE}$	VSS	NC	VDDQ
N	I/O15	NC	VSS	A1	VSS	I/O1	NC
P	NC	I/OP2	VSS	A0	VSS	NC	I/O0
R	NC	A5	$\overline{LBO}$	VDD	VSS[1]	A12	NC
T	NC	A10	A15	NC	A14	A11	ZZ[2]
U	VDDQ	DNU[3]	DNU[3]	DNU[3]	DNU[3]	DNU[3]	VDDQ

5309 drw 02d

Top View

NOTES:
1. R5 does not have to be directly connected to Vss as long as the input voltage is $\leq$ V$_{IL}$.
2. T7 can be left unconnected and the device will always remain in active mode.
3. DNU= Do not use; these signals can either be left unconnected or tied to Vss.
4. On future 18M devices CS_0 will be removed, B2 will be used for address expansion.

Pin Configuration – 256K x 36, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	$NC^{(3)}$	A_7	$\overline{CE}$	$\overline{BW}_3$	$\overline{BW}_2$	$\overline{CS}_1$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A_8	NC
B	NC	A_6	CS_0	$\overline{BW}_4$	$\overline{BW}_1$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A_9	$NC^{(3)}$
C	I/O_{P3}	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	I/O_{P2}
D	I/O_{17}	I/O_{16}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_{15}	I/O_{14}
E	I/O_{19}	I/O_{18}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_{13}	I/O_{12}
F	I/O_{21}	I/O_{20}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_{11}	I/O_{10}
G	I/O_{23}	I/O_{22}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_9	I/O_8
H	$V_{SS}^{(1)}$	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	$ZZ^{(2)}$
J	I/O_{25}	I/O_{24}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_7	I/O_6
K	I/O_{27}	I/O_{26}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_5	I/O_4
L	I/O_{29}	I/O_{28}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_3	I/O_2
M	I/O_{31}	I/O_{30}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_1	I/O_0
N	I/O_{P4}	NC	V_{DDQ}	V_{SS}	NC	$NC^{(3)}$	NC	V_{SS}	V_{DDQ}	NC	I/O_{P1}
P	NC	$NC^{(3)}$	A_5	A_2	$DNU^{(4)}$	A_1	$DNU^{(4)}$	A_{10}	A_{13}	A_{14}	A_{17}
R	$\overline{LBO}$	$NC^{(3)}$	A_4	A_3	$DNU^{(4)}$	A_0	$DNU^{(4)}$	A_{11}	A_{12}	A_{15}	A_{16}

5309tbl 17a

Pin Configuration – 512K x 18, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	$NC^{(3)}$	A_7	$\overline{CE}$	$\overline{BW}_2$	NC	$\overline{CS}_1$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A_8	A_{10}
B	NC	A_6	CS_0	NC	$\overline{BW}_1$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A_9	$NC^{(3)}$
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	I/O_{P1}
D	NC	I/O_8	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	I/O_7
E	NC	I/O_9	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	I/O_6
F	NC	I/O_{10}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	I/O_5
G	NC	I/O_{11}	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	I/O_4
H	$V_{SS}^{(1)}$	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	$ZZ^{(2)}$
J	I/O_{12}	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_3	NC
K	I/O_{13}	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_2	NC
L	I/O_{14}	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_1	NC
M	I/O_{15}	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O_0	NC
N	I/O_{P2}	NC	V_{DDQ}	V_{SS}	NC	$NC^{(3)}$	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	$NC^{(3)}$	A_5	A_2	$DNU^{(4)}$	A_1	$DNU^{(4)}$	A_{11}	A_{14}	A_{15}	A_{18}
R	$\overline{LBO}$	$NC^{(3)}$	A_4	A_3	$DNU^{(4)}$	A_0	$DNU^{(4)}$	A_{12}	A_{13}	A_{16}	A_{17}

5309 tbl 17b

NOTES:
1. H1 does not have to be directly connected to V_{SS}, as long as the input voltage is $\leq V_{IL}$.
2. H11 can be left unconnected and the device will always remain in active mode.
3. Pin N6, B11, A1, R2 and P2 are reserved for 18M, 36M, 72M, and 144M and 288M respectively.
4. DNU= Do not use; these signals can either be left unconnected or tied to V_{SS}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (VDD = 3.3V ± 5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{ILI}	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
I_{ILI}	$\overline{LBO}$ Input Leakage Current[1]	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
I_{ILO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V

5309 tbl 08

NOTE:

1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ in will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range [1]

Symbol	Parameter	Test Conditions	7.5ns		8ns		8.5ns		Unit
			Com'l	Ind	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	265	285	210	230	190	210	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2,3]	50	70	50	70	50	70	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX} [2,3]	145	165	140	160	135	155	mA
I_{ZZ}	Full Sleep Mode Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	50	70	50	70	50	70	mA

5309 tbl 09

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V.

AC Test Conditions
(VDDQ = 3.3V/2.5V)

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

5309 tbl 10

AC Test Load
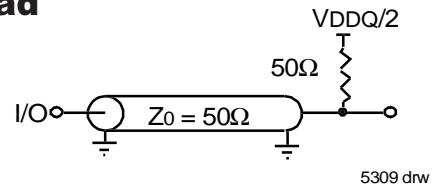
5309 drw 03

Figure 1. AC Test Load
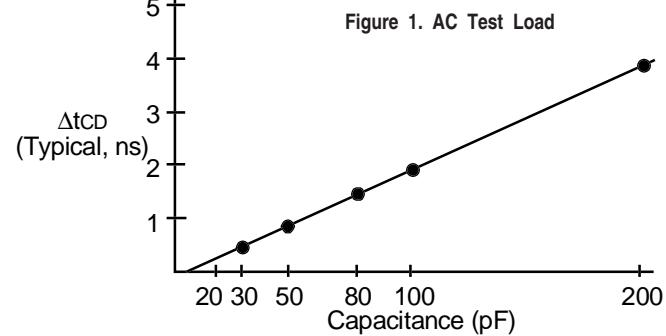
5309 drw 05

Figure 2. Lumped Capacitive Load, Typical Derating

Synchronous Truth Table [1,3]

| Operation	Address Used	$\overline{CE}$	CS_0	$\overline{CS}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_x$	$\overline{OE}$ [2]	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	↑	D$_{OUT}$
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	↑	D$_{OUT}$
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	↑	D$_{OUT}$
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	↑	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	↑	D$_{IN}$
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	↑	D$_{IN}$
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	↑	D$_{OUT}$
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	↑	D$_{OUT}$
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	↑	D$_{OUT}$
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	↑	D$_{OUT}$
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	↑	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	↑	D$_{IN}$
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	↑	D$_{IN}$
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	↑	D$_{IN}$
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	↑	D$_{IN}$
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	↑	D$_{OUT}$
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	↑	D$_{OUT}$
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	↑	D$_{OUT}$
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	↑	D$_{OUT}$
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	↑	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	↑	D$_{IN}$
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	↑	D$_{IN}$
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	↑	D$_{IN}$
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	↑	D$_{IN}$

5309 tbl 11

NOTES:
1. L = V$_{IL}$, H = V$_{IH}$, X = Don't Care.
2. $\overline{OE}$ is an asynchronous input.
3. ZZ - low for the table.

Synchronous Write Function Truth Table [1, 2]

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$	$\overline{BW}_4$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1[3]	H	L	L	H	H	H
Write Byte 2[3]	H	L	H	L	H	H
Write Byte 3[3]	H	L	H	H	L	H
Write Byte 4[3]	H	L	H	H	H	L

5309 tbl 12

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{BW}_3$ and $\overline{BW}_4$ are not applicable for the IDT71V67903.
3. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table [1]

Operation[2]	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z – Data In	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

5309 tbl 13

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LBO}$=V$_{DD}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address[1]	1	1	1	0	0	1	0	0

5309 tbl 14

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LBO}$=V$_{SS}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address[1]	1	1	0	0	0	1	1	0

5309 tbl 15

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

AC Electrical Characteristics (V$_{DD}$ = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	7.5ns Min.	7.5ns Max.	8ns Min.	8ns Max.	8.5ns Min.	8.5ns Max.	Unit
Clock Parameter								
t$_{CYC}$	Clock Cycle Time	8.5	—	10	—	11.5	—	ns
t$_{CH}$[1]	Clock High Pulse Width	3	—	4	—	4.5	—	ns
t$_{CL}$[1]	Clock Low Pulse Width	3	—	4	—	4.5	—	ns
Output Parameters								
t$_{CD}$	Clock High to Valid Data	—	7.5	—	8	—	8.5	ns
t$_{CDC}$	Clock High to Data Change	2	—	2	—	2	—	ns
t$_{CLZ}$[2]	Clock High to Output Active	0	—	0	—	0	—	ns
t$_{CHZ}$[2]	Clock High to Data High-Z	2	3.5	2	3.5	2	3.5	ns
t$_{OE}$	Output Enable Access Time	—	3.5	—	3.5	—	3.5	ns
t$_{OLZ}$[2]	Output Enable Low to Output Active	0	—	0	—	0	—	ns
t$_{OHZ}$[2]	Output Enable High to Output High-Z	—	3.5	—	3.5	—	3.5	ns
Set Up Times								
t$_{SA}$	Address Setup Time	1.5	—	2	—	2	—	ns
t$_{SS}$	Address Status Setup Time	1.5	—	2	—	2	—	ns
t$_{SD}$	Data In Setup Time	1.5	—	2	—	2	—	ns
t$_{SW}$	Write Setup Time	1.5	—	2	—	2	—	ns
t$_{SAV}$	Address Advance Setup Time	1.5	—	2	—	2	—	ns
t$_{SC}$	Chip Enable/Select Setup Time	1.5	—	2	—	2	—	ns
Hold Times								
t$_{HA}$	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t$_{HS}$	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t$_{HD}$	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t$_{HW}$	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t$_{HAV}$	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns
t$_{HC}$	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
Sleep Mode and Configuration Parameters								
t$_{ZZPW}$	ZZ Pulse Width	100	—	100	—	100	—	ns
t$_{ZZR}$[3]	ZZ Recovery Time	100	—	100	—	100	—	ns
t$_{CFG}$[4]	Configuration Set-up Time	34	—	40	—	50	—	ns

5309 tbl 16

NOTES:
1. Measured as HIGH above V$_{IH}$ and LOW below V$_{IL}$.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t$_{CFG}$ is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.

Timing Waveform of Flow-Through Read Cycle (1,2)

IDT71V67703, IDT71V67903, 256K x 36, 512K x 18, 3.3V Synchronous SRAMS with
3.3V I/O, Flow-Through Outputs, Single Cycle Deselect
Commercial and Industrial Temperature Ranges

13

CLK

tCYC

tSS
tHS
ADSP

tCH   tCL

ADSC   (1)

tSA
tHA
ADDRESS   Ax   Ay

tSW   tHW

GW, BW E, BW x

tSC
tHC
CE, CS1
(Note 3)

tSAV
tHAV
ADV

ADV HIGH suspends burst

tOE
O E

tCD

tOHZ
tOLZ

tCDC

(Burst wraps around
to its initial state)   tCHZ

DATAOUT   O1(Ax)   O1(Ay)   O2(Ay)   O3(Ay)   O4(Ay)   O1(Ay)   O2(Ay)

Output
Disabled

Flow-through
Read

Burst Flow-through Read

5309 drw 06

NOTES:
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base
   address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}$1 signals. For example, when $\overline{CE}$ and $\overline{CS}$1 are LOW on this waveform, CS0 is HIGH.

IDT71V67703, IDT71V67903, 256K x 36, 512K x 18, 3.3V Synchronous SRAMS with
3.3V I/O, Flow-Through Outputs, Single Cycle Deselect

Commercial and Industrial Temperature Ranges

Timing Waveform of Combined Flow-Through Read and Write Cycles (1,2,3)

Single Read   Write   Flow-through Burst Read
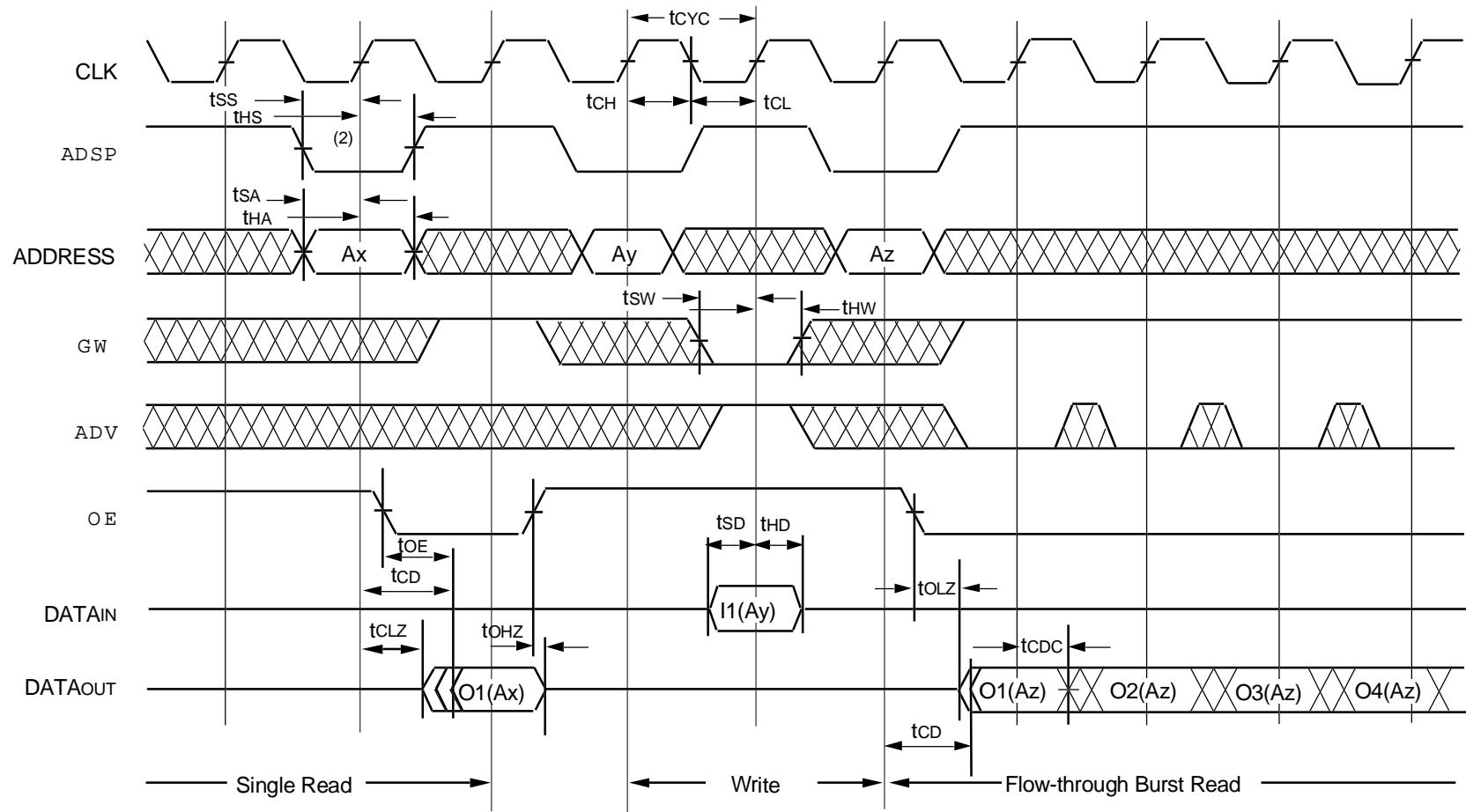
5309 drw 07

NOTES:
1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS}1$ are LOW, CS0 is HIGH.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay; O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

IDT71V67703, IDT71V67903, 256K x 36, 512K x 18, 3.3V Synchronous SRAMS with
3.3V I/O, Flow-Through Outputs, Single Cycle Deselect
Commercial and Industrial Temperature Ranges

Timing Waveform of Write Cycle No. 1 - $\overline{GW}$ Controlled (1,2,3)

15

CLK

tCYC

tSS
tHS

ADSP
(1)

tCH tCL

ADSC

tSA
tHA

ADDRESS   Ax   Ay   Az

tHW
tSW

GW is ignored when ADSP initiates a cycle and is sampled on the next cycle rising edge

GW

tSC
tHC

CE, CS1
(Note 3)

tSAV   tHAV

ADV

(ADV suspends burst)

OE

tSD   tHD

DATAIN   I1(Ax)   I1(Ay)   I2(Ay)   I2(Ay) (2)   I3(Ay)   I4(Ay)   I1(Az)   I2(Az)   I3(Az)

tOHZ

DATAOUT   O3(Aw)   O4(Aw)

5309 drw 08
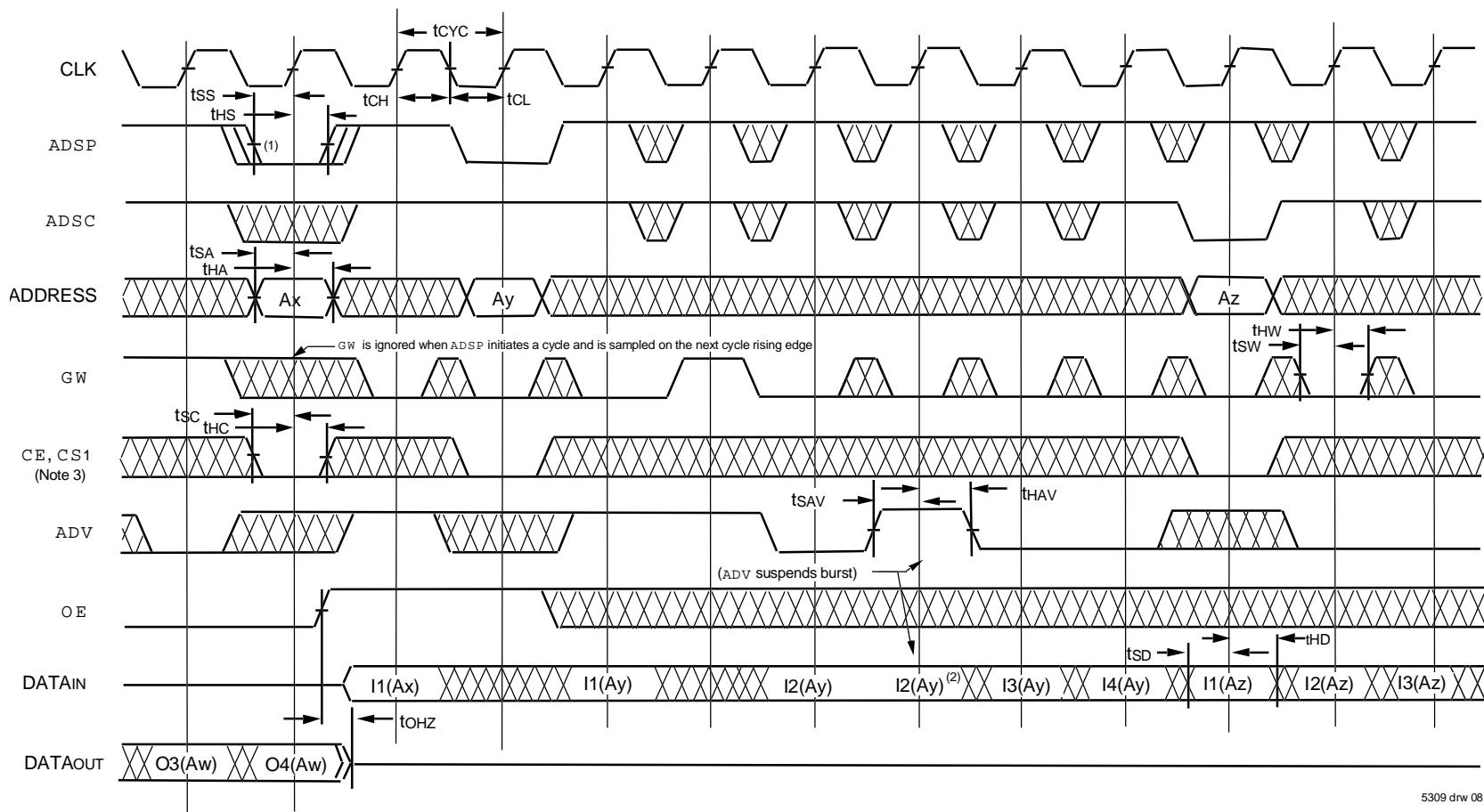
NOTES:

1. ZZ input is LOW, $\overline{BWE}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}1$ signals. For example, when $\overline{CE}$ and $\overline{CS}1$ are LOW on this waveform, CS0 is HIGH.

IDT71V67703, IDT71V67903, 256K x 36, 512K x 18, 3.3V Synchronous SRAMS with 3.3V I/O, Flow-Through Outputs, Single Cycle Deselect

Commercial and Industrial Temperature Ranges

Timing Waveform of Write Cycle No. 2 - Byte Controlled (1,2,3)

16

5309 drw 09
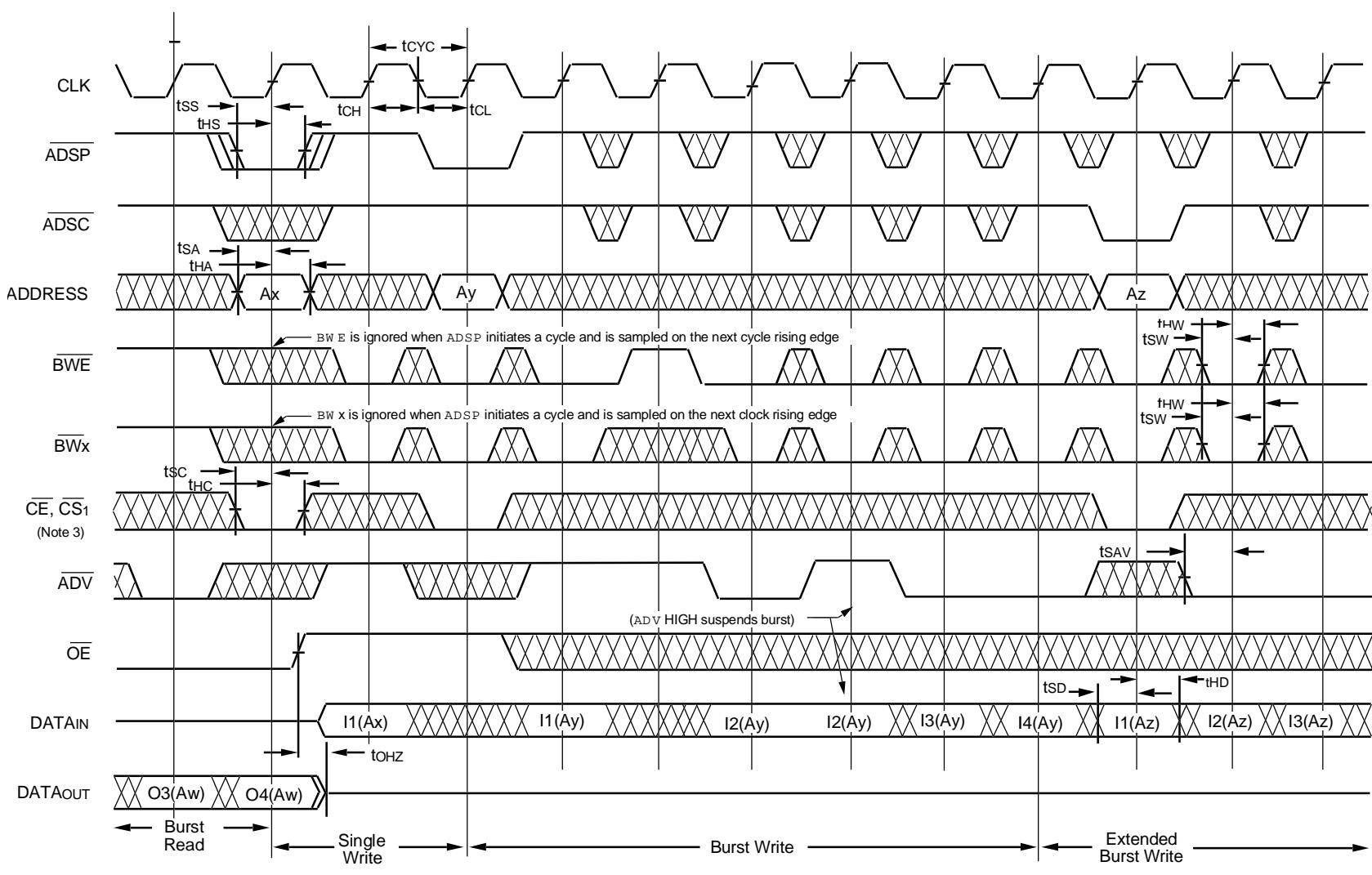
NOTES:

1. ZZ input is LOW, $\overline{GW}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, CS0 is HIGH.

IDT71V67703, IDT71V67903, 256K x 36, 512K x 18, 3.3V Synchronous SRAMS with
3.3V I/O, Flow-Through Outputs, Single Cycle Deselect

Commercial and Industrial Temperature Ranges

Timing Waveform of Sleep (ZZ) and Power-Down Modes (1,2,3)

17

5309 drw 13
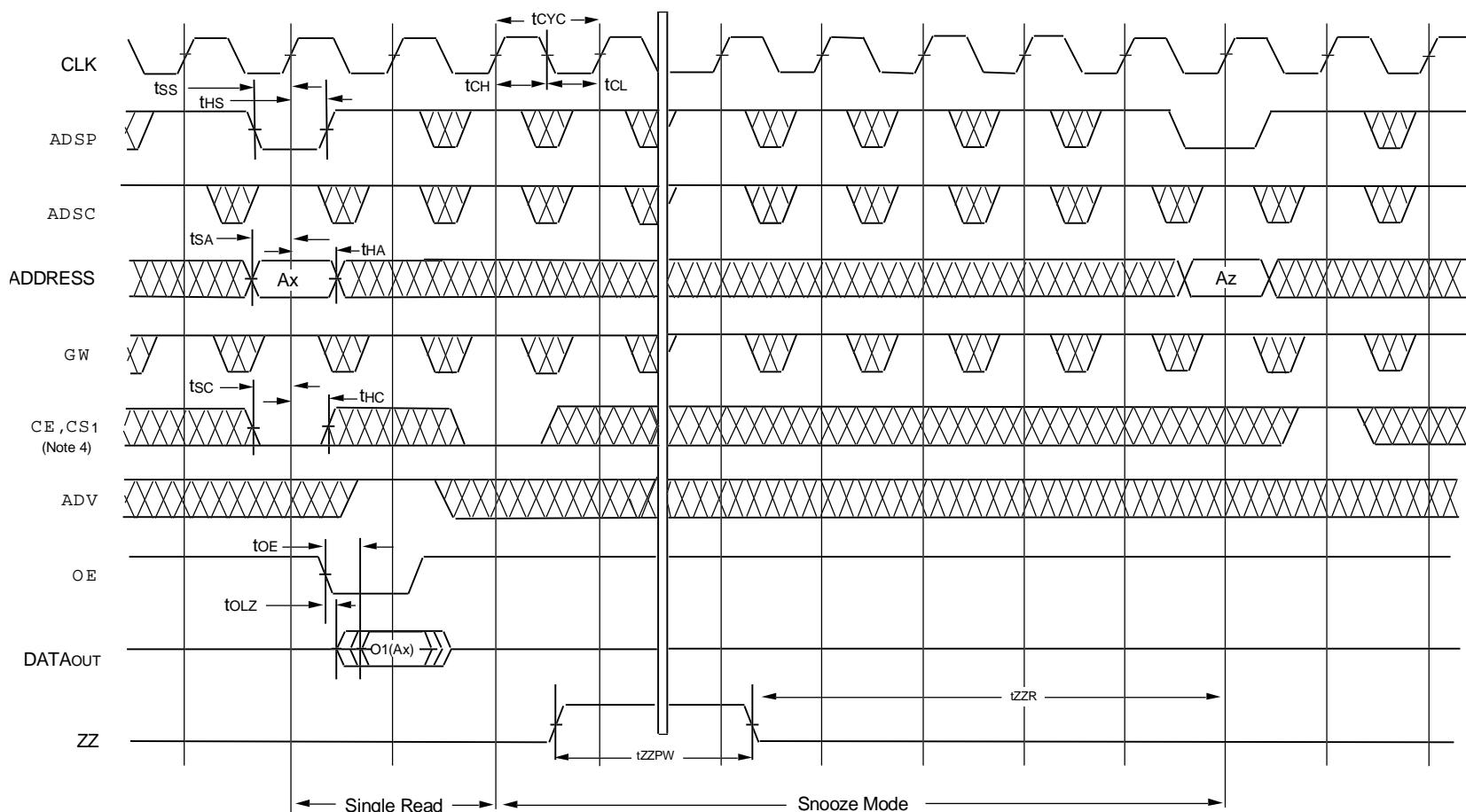
NOTES:
1. Device must power up in deselected Mode.
2. $\overline{LBO}$ is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}$1 signaals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Non-Burst Read Cycle Timing Waveform
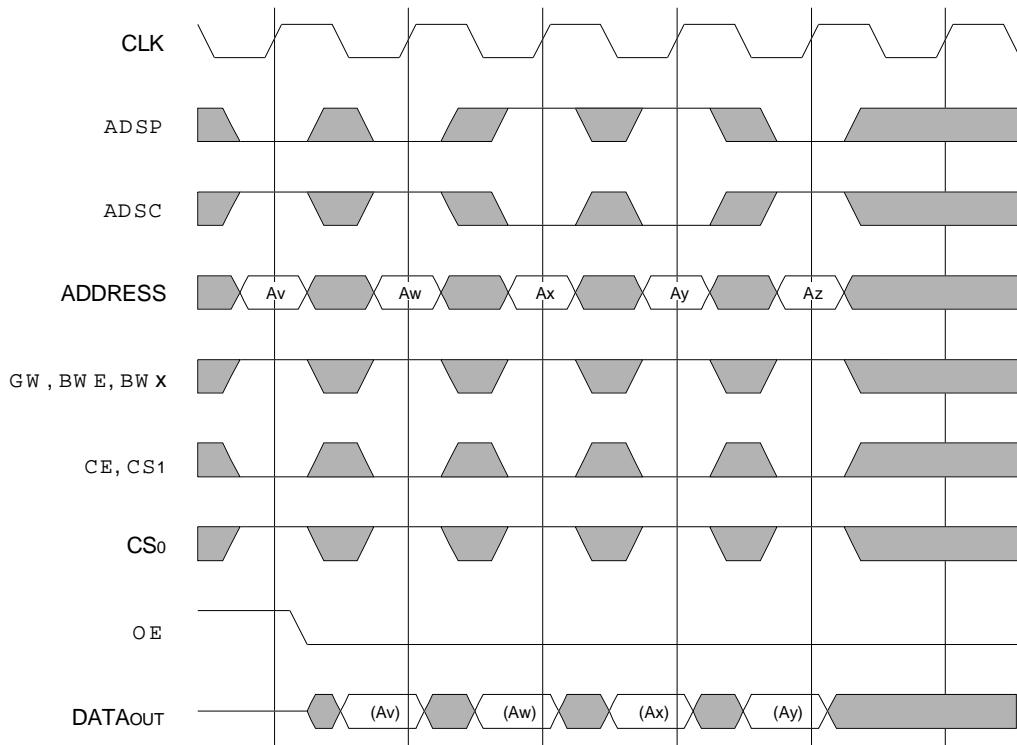
5309 drw 10

NOTES:
1. ZZ input is LOW, $\overline{ADV}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, $\overline{ADSP}$ and $\overline{ADSC}$ function identically and are therefore interchangable.

Non-Burst Write Cycle Timing Waveform

5309 drw 11
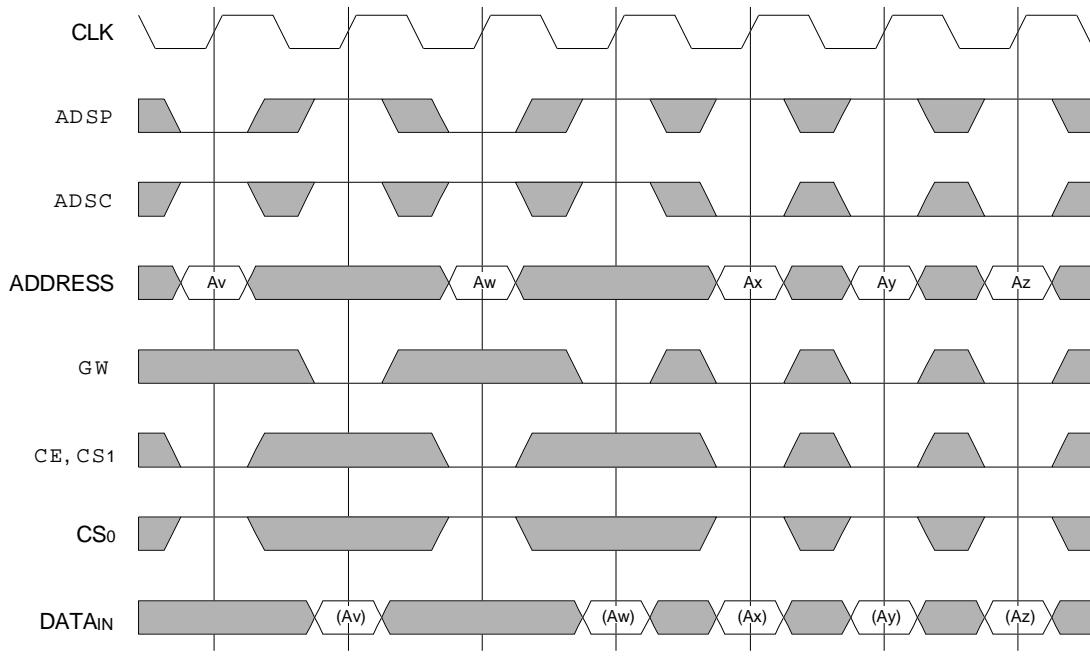
NOTES:
1. ZZ input is LOW, $\overline{ADV}$ and $\overline{OE}$ are HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only $\overline{GW}$ writes are shown, the functionality of $\overline{BWE}$ and $\overline{BWx}$ together is the same as $\overline{GW}$.
4. For write cycles, $\overline{ADSP}$ and $\overline{ADSC}$ have different limitations.

100-Pin Thin Plastic Quad Flatpack (TQFP) Package Diagram Outline

EVEN LEAD SIDES   ODD LEAD SIDES

DETAIL A

DETAIL B

SEE DETAIL A

SEE DETAIL B

SEE DETAIL C

DETAIL C

WITH PLATING

BASE METAL

TOLERANCES
UNLESS SPECIFIED
DECIMAL   ANGULAR
XX±   ±
XXX.±
XXXX.±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727–6116
FAX: (408) 492–8074   TWX: 910–338–2070

TITLE   PK PACKAGE OUTLINE
14.0 X 20.0 X 1.4 mm TQFP
1.00/.10 FORM

SIZE C DRAWING No. PSC–4045 REV

DO NOT SCALE DRAWING   SHEET 1 OF 2

LAND PATTERN DIMENSIONS

SYMBOL	JEDEC VARIATION DJ			NOTE
	MIN	NOM	MAX	
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D		22.00 BSC		4
D1		20.00 BSC		5,2
E		16.00 BSC		4
E1		14.00 BSC		5,2
N		100		
ND		30		
NE		20		
e		.65 BSC		
b	.22	.32	.38	7
b1	.22	.30	.33	
ccc	–	–	.10	
ddd	–	–	.13	

	MIN	MAX
P	22.80	23.00
P1	19.80	20.00
P2	18.85 BSC	
Q	16.80	17.00
Q1	13.80	14.00
Q2	12.35 BSC	
X	.30	.50
e	.65 BSC	
N	100	

NOTES:

1   ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982

2   TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3   DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–

4   DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE –C–

5   DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION, ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6   DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7   DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8   EXACT SHAPE OF EACH CORNER IS OPTIONAL

9   THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10   ALL DIMENSIONS ARE IN MILLIMETERS

11   THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–136, VARIATION DJ AND BX

119 Ball Grid Array (BGA) Package Diagram Outline

(119 BALL SHOWN)

(119 BALL)

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982

2 SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

3 "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION
   "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION
   "N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS

4 PACKAGE MAY EXTEND TO EDGE PERIPHERY AND MAY CONSIST OF MOLDING COMPOUND, EPOXY, METAL, CERAMIC OR OTHER MATERIAL

5 DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-

6 "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE

7 ACTUAL SHAPE OF THIS FEATURE IS OPTIONAL.

8 ALL DIMENSIONS ARE IN MILLIMETERS

9 THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-028, VARIATION AA

SYMBOL	JEDEC VARIATION AA			NOTE
	MIN	NOM	MAX	
A	–	2.15	2.36	
A1	.50	.60	.70	
A2	–	–	1.20	
D	22.00 BSC			
D1	20.32 BSC			
E	14.00 BSC			
E1	7.62 BSC			
MD	17			3
ME	7			3
N	119			3
e	1.27 BSC			
b	.60	.75	.90	5
c	.51	.56	.61	
aaa	–	–	.15	
bbb	–	–	.25	
ccc	–	–	.35	
ddd	–	–	.30	
eee	–	–	.10	

Revisions (Sheet 1 of 2):

DCN	REV	DESCRIPTION	DATE	APPROVED
60626	00	INITIAL RELEASE	10/16/97	T. VU
	01	SWITCH E & D DIMENSIONS	04/25/00	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
TITLE: BG PACKAGE OUTLINE 14.0 X 22.0 mm BODY PBGA
SIZE: C DRAWING No. PSC-4063 REV 01
DO NOT SCALE DRAWING SHEET 1 OF 2

Revisions (Sheet 2 of 2):

DCN	REV	DESCRIPTION	DATE	APPROVED
60626	00	INITIAL RELEASE	10/16/97	T. VU
	01	SWITCH E & D DIMENSIONS	04/25/00	T. VU
	02	CHANGE PACKAGE THICKNESS	08/05/00	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
TITLE: BG PACKAGE OUTLINE 14.0 X 22.0 mm BODY PBGA
SIZE: C DRAWING No. PSC-4063 REV 02
DO NOT SCALE DRAWING SHEET 2 OF 2

165 Fine Pitch Ball Grid Array (fBGA) Package Diagram Outline

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH

3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE

4. "N" REPRESENTS THE BALLCOUNT NUMBER

5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-

6. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

7. "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY

8. IF "A1" ID CORNER IS ON PACKAGE BODY, IT MUST BE LOCATED WITHIN THE ZONE INDICATED

9. ALL DIMENSIONS ARE IN MILLIMETERS

(165 BALL)

SYMBOL	JEDEC VARIATION NOT YET REGISTERED			NOTE
	MIN	NOM	MAX	
A	–	–	1.20	
A1	.30	.35	.40	
A2	.78	.85	.92	
D	15.00 BSC			
E	13.00 BSC			
M	11 X 15			3
N	165			4
e	1.00 BSC			
b	.35	.45	.50	5
CENTER BALL MATRIX	N/A			

TITLE: BQ PACKAGE OUTLINE 13.0 X 15.0 mm BODY FPBGA

DRAWING No. PSC-4086   REV 00

Ordering Information

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XXX      S      X      XX      X
Device   Power  Speed  Package Process/
Type                           Temperature Rance
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Blank — Commercial (0°C to +70°C)
I — Industrial (-40°C to +85°C)

PF — 100-Pin Plastic Thin Quad Flatpack (TQFP)
BG — 119 Ball Grid Array (BGA)
BQ — 165 fine pitch Ball Grid Array (fBGA)

75
80 — Access Time in Tenths of Nanoseconds
85

71V67703 — 256K x 36 Flow-Through Burst Synchronous SRAM
71V67903 — 512K x 18 Flow-Through Burst Synchronous SRAM

5309 drw 12

Datasheet Document History

12/31/99		Created Datasheet from 71V677 and 71V679 Datasheets
		For 2.5V I/O offering, see 71V67702 AND 71V67902 Datasheets.
04/26/00	Pg. 4	Add capacitance for BGA package; Insert clarification note to Absolute Max Ratings and Recommended Operating Temperature tables.
	Pg. 7	Replace Pin U6 with $\overline{TRST}$ pin in BGA pin configuration; Add pin description note in pinout
	Pg. 18	Inserted 100 pin TQFP Package Diagram Outline
05/24/00	Pg. 1,4,8,21 22	Add new package offering, 13 x 15 fBGA
	Pg. 5,6,7,8	Correct note 2 on BGA and TQFP pin configuration
	Pg. 20	Correction in the 119 BGA Package Diagram Outline
07/12/00	Pg. 5,6,8	Remove note from TQFP and BQ165 pinouts
	Pg. 7	Add/Remove note from BG119 pinout
	Pg. 20	Update BG 119 pinout
12/18/00	Pg. 9	Updated ISB2 levels for 7.5-8.5ns.
10/29/01	Pg. 1,2	Remove JTAG pins
	Pg. 7	Changed U2-U6 pins to DNU.
	Pg. 8	Changed P5,P7,R5 & R7 to DNU pins.
	Pg. 9	Raised specs by 10mA on 7.5ns, 8ns and 8.5ns.
10/22/02	Pg. 1-23	Changed datasheet from Advanced to Final Release.
	Pg. 4,9,12, 22	Added I temp to datasheet.
04/15/03	Pg. 4	Updated 165 fBGA table from TBD to 7.
12/20/03	Pg. 7	Updated 119BGS pin configurations- reordered I/O signals on P6, P7 (128K x 36) and P7, N6, L6, K7, H6, G7, F6, E7, D6 (256K x 18).
02/20/09	Pg. 22	Removed "IDT" from orderable part number.