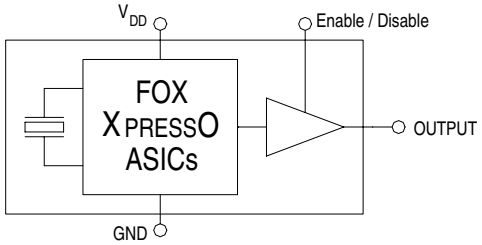
XPRESSO for FIBRE CHANNEL Model: FXO-LC735RFC-212.5

LVDS 7 x 5mm 3.3V 50ppm XO Freq: 212.5MHz

Features

- Low Jitter
- Low Cost
- Tri-State Enable / Disable Feature
- Industry Standard Package
- Gold over Nickel Termination Finish



Need a Sample

Pb

RoHS Compliant

Electrical Characteristics

Parameters	Symbol	Condition	Maximum Value (unless otherwise noted)
Frequency	F_O		212.5 MHz
Frequency Stability 1			50 ppm
Temperature Range	T_O T_{STG}	Standard operating Storage	*-40℃ to +85℃* -55°C to +125°C
Supply Voltage	V_{DD}	Standard	3.3V ± 5%
Input Current	I_{DD}	Standard Load	100 mA
Output Load	Differential	Standard	100 ohms Typ.
Start-Up Time	T_S		10 mS
Output Enable / Disable Time			100 nS
Moisture Sensitivity Level	MSL		1
Termination Finish			Au

Note 1 – Stability is inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock and vibration.

Output Wave Characteristics

Parameters	Symbol	Condition	Maximum Value (unless otherwise noted)
Differential Output Voltage	V_{OD}	Standard Load	0.6V Typ.
Output Offset Voltage	V_{OS}	Standard Load	1.3V Typ.
Output Symmetry		@ 50% Vp-p Level	45% ~ 55%
Output Enable (PIN # 1) Voltage	V_{IH}		≥70% V_{DD}
Output Disable (PIN # 1) Voltage	V_{IL}		≤ 30% V_{DD}
Cycle Rise Time	T_R	20% ~ 80% Vp-p	400 pS
Cycle Fall Time	T_F	80% ~ 20% Vp-p	400 pS

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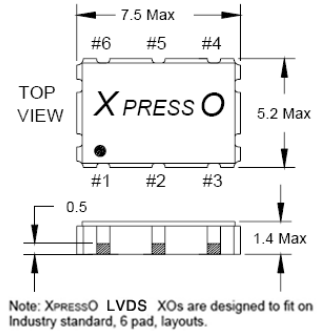
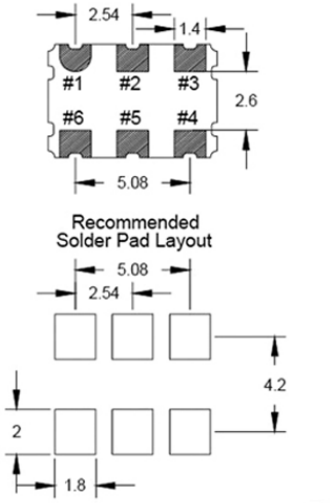
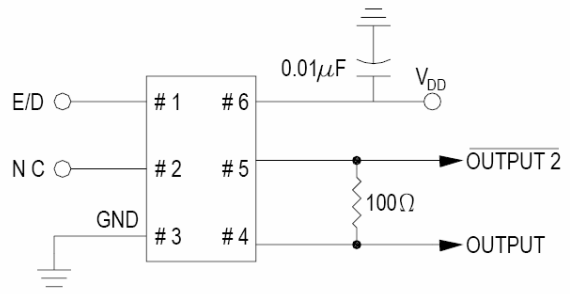
Dimensional Drawing & Pad Layout







Drawing is for reference to critical specifications defined by size measurements.
Certain non-critical visual attributes, such as side castellations, reference pin shape, etc. may vary

Phase Jitter & Time Interval Error (TIE) (Typical Measurements)

Frequency	Phase Jitter (12kHz to 20MHz)	T I E (Sigma of Jitter Distribution)	Units
212.5 MHz	0.89	3.9	pS RMS

Phase Jitter is integrated from HP3048 Phase Noise Measurement System; measured directly into 50 ohm input; V_{DD} = 3.3V.
TIE was measured on LeCroy LC684 Digital Storage Scope, directly into 50 ohm input, with Amherst M1 software; V_{DD} = 3.3V.
*Per **MJSQ** spec (Methodologies for Jitter and Signal Quality specifications)*

Random & Deterministic Jitter Composition (Typical Measurements)

Frequency	Random (Rj) (pS RMS)	Deterministic (Dj) (pS P-P)	Total Jitter (Tj) (14 x Rj) + Dj
212.5 MHz	0.9	6.7	18.7 pS

Rj and Dj, measured on LeCroy LC684 Digital Storage Scope, directly into 50 ohm input, with Amherst M1 software.
*Per **MJSQ** spec (Methodologies for Jitter and Signal Quality specifications)*

Pin Functional Description

Pin #	Name	Type	Function
1	E / D [1]	Logic	Enable / Disable Control of Output (0 = Disabled)
2	NC		*No Connection – Leave Open*
3	GND	Ground	Electrical Ground for V_{DD}
4	Output	Output	LVDS Oscillator Output
5	Output 2	Output	Complementary LVDS Output
6	V_{DD} [2]	Power	Power Supply Source Voltage

NOTES:
[1] Includes pull-up resistor to V_{DD} to provide output when the pin (1) is No Connect.
[2] Installation should include a 0.01µF bypass capacitor placed between V_{DD} (Pin 6) and GND (Pin 3) to minimize power supply line noise.