AS3514

Stereo Audio Codec with System Power Management

1 General Description

The AS3514 is a low power stereo audio codec and is designed for Portable Digital Audio Applications. It allows playback in CD quality and recording in FM-stereo quality. It has a variety of audio inputs and outputs to directly connect electret microphones, 16Ω headset, 4Ω speaker and auxiliary signal sources via a 10-channel mixer. It only consumes 22mW in playback mode.

Further the device offers advanced power management functions. All necessary ICs and peripherals in a flash based Digital Audio Player are supplied by the AS3514. The power management block generates 9 different supply voltages out of the battery supply. CPU, NAND flash, SRAM, memory cards, LCD back-light, USB RX/TX can be powered. The different supply voltages are programmable via the serial control interface. It also contains a charger and is designed for battery supplies from 1V to 5V.

The AS3514 has an on-chip, phase locked loop (PLL) controlled, clock generator. It generates 44.1kHz, 48kHz and other sample rates defined in MP3, AAC, WMA, OGG VORBIS etc. No additional external crystal or PLL is needed. Further the AS3514 has an independent 32kHz real time clock (RTC) on chip which allows a complete power down of the system CPU.

2 Key Features

Multi-bit Sigma Delta Converters
– DAC: 18bit with 94dB SNR ('A' weighted) , 48kHz
– ADC: 14bit with 82dB SNR ('A' weighted), 16kHz

2 Microphone Inputs
– 3 gain pre-setting (28dB/34dB/40dB) with AGC
– 32 gain steps @1.5dB and MUTE
– supply for electret microphone
– microphone detection
– remote control by switch

2 Line Inputs
– volume control via serial interface
– 32 steps @1.5dB and MUTE
– stereo or 2x mono or mono differential

Line Outputs
– volume control via serial interface
– 32 steps @1.5dB and MUTE
– 1Vp @10kΩ

Audio Mixer
– 10 channel input/output mixer with AGC
– mixes line inputs and microphones with DAC
– left and right channels independent

High Efficiency Headphone Amplifier
– volume control via serial interface
– 32 steps @1.5dB and MUTE
– 2x40mW @16Ω driver capability
– headphone and over-current detection
– phantom ground eliminates large capacitors

High Power Speaker Amplifier
– volume control via serial interface
– 32 steps @1.5dB and MUTE
– 2x500mW @8Ω driver capability
– over-current detection

Power Management
– step up for system supply (3.0V – 3.6V)
– step down for CPU core (0.85V – 1.8V, 200mA)
– step up for backlight (15V, 38.5mA)
– LDO for digital supply (2.9V, 200mA)
– LDO for analogue supply (2.9V, 200mA)
– LDO for peripherals (1.7V-3.3V, 200mA)
– LDO for peripherals (3.1V-3.3V, 200mA)
– LDO for RTC (1.0V-2.5V, 2mA)
– LDO for USB 1.1 transceiver (3.26V, 10mA)
– battery supervision
– 10sec emergency shut-down

Battery Charger
– automatic trickle charge (50mA)
– prog. constant current charging (100-400mA)
– prog. constant voltage charging (3.9V-4.25V)

Real Time Clock
– ultra low power 32kHz oscillator
– 32bit RTC sec counter
– selectable alarm (seconds or minutes)

General Purpose ADC
– 10bit resolution
– 16 inputs analogue multiplexer

Interfaces
– I²S digital audio interface
– 2 wire serial control interface
– watchdog via serial interface
– power good pin
– 128bit unique ID (OTP)
– 17 different interrupts

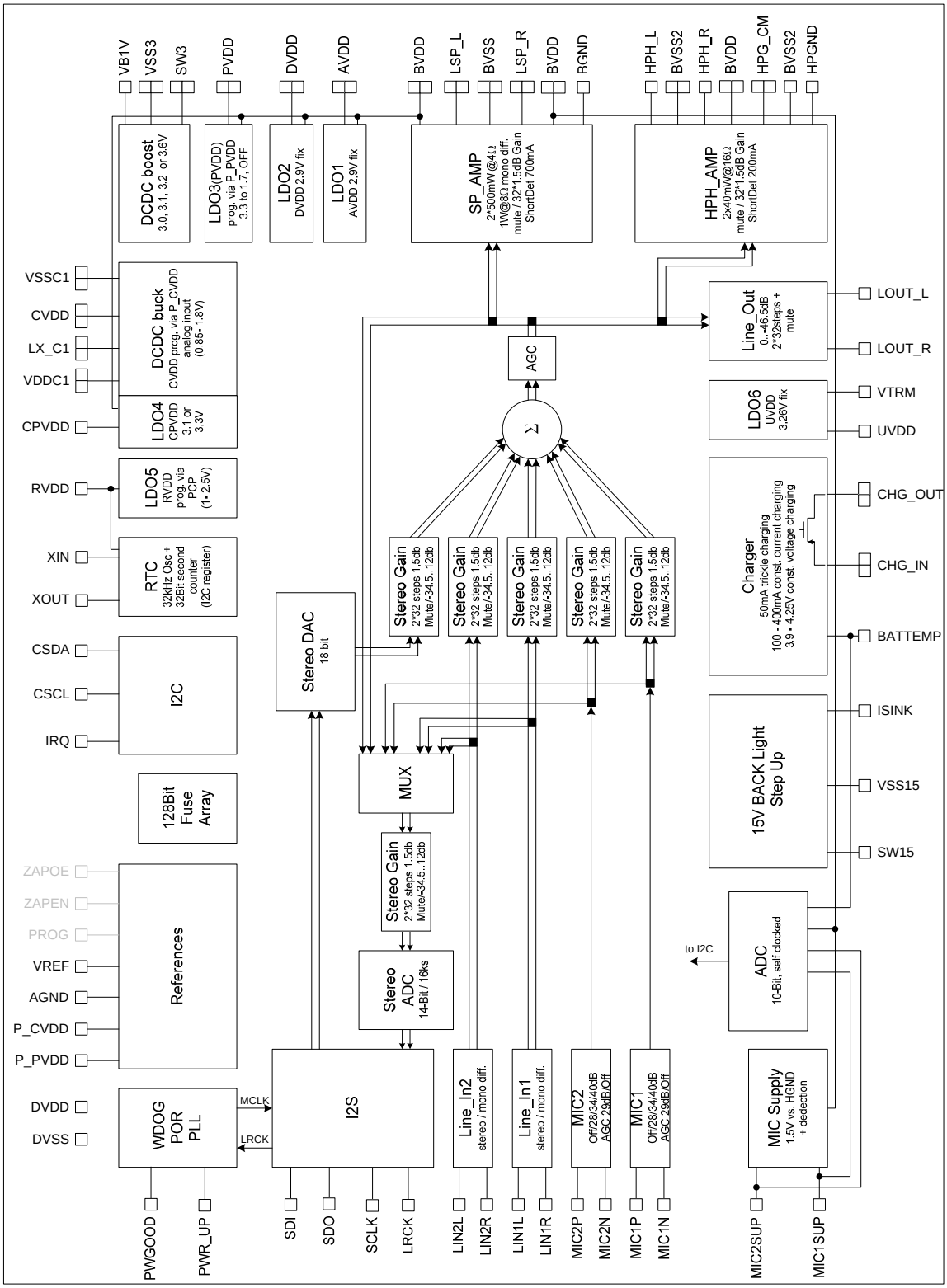
Package CTBGA64 [7.0x7.0x1.1mm] 0.8mm pitch

3 Application

Portable Digital Audio Player and Recorder
PDA, Smartphone

4 Block Diagram

Figure 1 AS3514 Block Diagram



Contents

Revision History

Revision	Date	Owner	Description
0.1	17.1.2005	pkm	first public release
0.2	15.4.2005	pkm	new LQFP pinning (chapter 8.2.2)
0.2	18.4.2005	pkm	added P_CVDD description as pin is missing now in the LQFP package (chapter 8.1)
0.2	19.4.2005	pkm	new PLL description, audio in/out chapters combined (chapter 6.6)
0.2	20.4.2005	pkm	new ordering information (chapter 9)
0.2	22.4.2005	pkm	added additional audio and performance parameter (chapter 6, 7)
0.2	3.5.2005	pkm	new DCDC buck description (chapter 0, 6.12)
0.21	5.5.2005	pkm	updated audio and performance parameter (chapter 6, 7)
0.21	5.5.2005	pkm	added AGC information for audio mixer (chapter 6.7)
0.21	5.5.2005	pkm	updated power up timing (chapter 6.12)
0.21	5.5.2005	pkm	updated absolute maximum ratings and operating conditions (chapter 5)
0.3	19.5.2005	pkm	changed power up sequence for chip version V12 (chapter 6.12)
0.3	20.5.2005	pkm	updated audio performance parameter (chapter 7)
0.3	20.5.2005	pkm	updated 15 DCDC description (chapter 6.14)
0.31	9.6.2005	pkm	updated soldering conditions (chapter 5)
0.31	9.6.2005	pkm	added ESD note to pin description (chapter 8.1)
0.9	15.3.2006	pkm	bug fix in left line in register (chapter 6.5)
0.91	12.5.2006	pkm	updated PMU block diagrams (chapter 6.x) updated BGA ball list and assignment (chapter 8.x)
0.92	20.11.2006	pkm	updated absolute maximum ratings (chapter 5)

5 Absolute Maximum Ratings (Non-Operating)

Stresses beyond the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or beyond those listed is not implied.

Caution: Exposure to absolute maximum rating conditions may affect device reliability.

Table 1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{IN_VB1V}	single cell supply voltage	-0.5	5.0	V	Applicable for pin VB1V
V_{IN_5V}	5V pins	-0.5	7.0	V	Applicable for pins BVDD, CHGIN, VBUS, BVDDC1
V_{IN_SW15}	15V pin	-0.5	17	V	Applicable for pins SW15
V_{IN_VSS}	Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins VSS3, VSS15, BVSS, BVSS2, AVSS, DVSS, VSSC1
V_{IN_DVDD}	3.3V pins with diode to DVDD	-0.5	5.0 DVDD+0.5	V	Applicable for pins MCLK, LRCK, SCLK, SDI, P_PVDD, P_CVDD, BATTEMP, ISINK, IRQ, PWGOOD
V_{IN_xDVDD}	pins with no diode to DVDD	-0.5	7.0V	V	Applicable for pins CSCL, CSDA, PWR_UP
V_{IN_AVDD}	3.3V pins with diode to AVDD	-0.5	5.0 AVDD+0.5	V	Applicable for pins BGND, HPH_CM, HPGND, LOUT_L/R, VREF, AGND, LIN1L/R, LIN2L/R, MIC1P/N, MIC2P/N, MIC1SUP, MIC2SUP
V_{IN_REG}	voltage regulator pins with diodes to BVDD	-0.5	5.0 BVDD+0.5	V	Applicable for pins AVDD, DVDD, PVDD, CPVDD, CVDD, UVDD
V_{IN_RTC}	voltage regulator pin with diode to BVDD	-0.5	3.6 BVDD+0.5	V	Applicable for pins RVDD, XIN, XOUT
V_{IN_BVDD}	pins with diode to BVDD	-0.5	7.0 BVDD+0.5	V	Applicable for pins LSP_R/L, HPH_R/L, CHGOUT, SW3
I_{scr}	Input Current (latchup immunity)	-100	100	mA	Norm: JEDEC JESD78 A
ESD	Electrostatic Discharge HBM		+/-1	kV	Norm: MIL 883 E method 3015
P_t	Total Power Dissipation (all supplies and outputs)		1000	mW	CTBGA64, T_{amb}=70°C
T_{strg}	Storage Temperature	-55	125	°C	
H	Humidity non-condensing	5	85	%	

Table 2 Soldering Conditions

Symbol	Parameter	Min	Max	Unit	Note
T_{body}	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
T_{peak}	Solder Profile*	235	245	°C	
D_{well}		30	45	s	above 217 °C

* austriamicrosystems AG strongly recommends to use underfill.

5.1 Operating Conditions

Table 3 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Battery Supply Voltage	BVDD	3.0	5.5	V	
DCDC 3V Supply Voltage	VB1V	1.0	4.5	V	
USB Supply Voltage	UVDD	-	5.5	V	
Digital Supply Voltage	DVDD	2.8	3.6	V	
Analoge Supply Voltage	AVDD	2.8	3.6	V	
Charger Supply Voltage	CHG_IN	4.5	5.5	V	
Difference of Positive Supplies	AVDD-DVDD	-0.25	0.25	V	
Difference of Negative Supplies DVSS, AVSS, VSS3, VSS15, VSSC1, BVSS	Any Combination	-0.1	0.1	V	To achieve good performance, the negative supply terminals should be connected to low ohmic ground plane.
Ambient Temperature	T_{amb}	-20	85	°C	
Supply Current	BVDD	6.8	20	mA	In Audio Loop Mode
System Clock Frequency	LRCLK	8	48	kHz	According to 8-48kSps Audio Data

6 Detailed Functional Block Description

6.1 Line Output

6.1.1 General

The line output is designed to provide the audio signal with typical 1Vp at a load of minimum 10kΩ, which is a minimum value for line inputs. Additional this output amplifier is capable to drive a 32Ω load (e.g. an earpiece of a mobile phone. To achieve this the operation mode can be switched from single ended stereo to mono differential.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB.

6.1.2 Register Description

Enabling the output stage is done via a control bit in the audio settings register (AudioSet1 register 0x14h). The line out driver itself is controlled by the following two registers.

Right Line Out Register (00h)

Table 4 LINE_OUT_R Register

Bit	Name	Description
7,6	reserved	For testing purpose only, must be set to 0h
5	-	not used
4..0	LOR_VOL	volume settings for right line output, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

Left Line Out Register (01h)

Table 5 LINE_OUT_L Register

Bit	Name	Description
7,6	LO_SES_DM	Single ended stereo or differential mono selection 11: tbd. 10: output switched to single ended stereo 01: output switched to differential mono **00: output switched to mute**
5	-	not used
4..0	LOL_VOL	volume settings for left line output, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

6.1.3 Parameter

Table 6 Line Output Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
R_L	Output Load	stereo mode	10k			Ohm
		differential mode	32			Ohm
A0	Gain	programmable gain	-40.5		6	dB
$\triangle$Ax	Gain Step-Size			1.5		dB
SNR	Signal to Noise Ratio	stereo mode		100		dB
	Mute Attenuation			100		dB

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

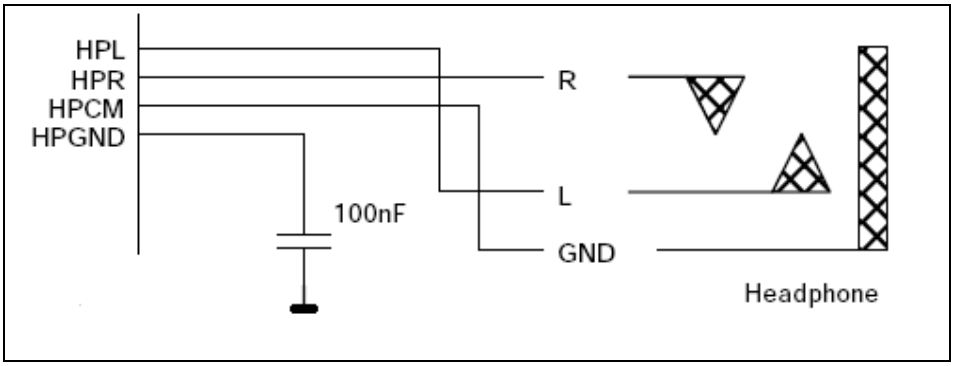
6.2 Headphone Output

6.2.1 General

The headphone output is designed to provide the audio signal with 2x40mW @ 16Ω or 2x20mW @32Ω, which are typical values for headphones.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –43.43dB to +1.07dB. The maximum output power of 40mW @ 16Ω is achieved, by setting the mixer output to 1Vp and using the gain of 1.07dB.

Figure 2 Headphone-Output



6.2.2 Phantom Ground

HPCM pin is the buffered HPGND output. It can be used to drive the loads without external blocking capacitors between HPL / HPR and HPCM. If the load is between HPR / HPL and BVSS, 100uF of de-coupling capacitors are needed. The phantom ground can be switched off to save power if not needed.

6.2.3 No-Pop Function

To avoiding click and pop noise during power-up and shutdown, the output is automatically set to mute when the output stage is disabled.

HPGND pin, which needs a 100nF capacitor outside, gets charged on power-up with 2uA to AGND=1.45V. After start-up the DC level of the following pins are the same: HPR=HPL=HPCM=HPGND=AGND=1.45V. The Start-up time before releasing mute is about 90ms. To avoid pop-noise 150ms discharging time of HPGND after a shutdown, have to be waited before starting up again.

6.2.4 Over-current Protection

This output stage has an over-current protection, which disables the output for 256ms or 512ms. This value can be set in the headphone registers. The over-current protection limit of HPR and HPL pin is typical 145mA while HPCM pin has a 210mA threshold. If needed, the over-current condition can also be signalled via an interrupt to the controlling microprocessor.

6.2.5 Headphone Detection

With a control bit the headphone detection can be enabled. The detection is only working as long as the headphone stage is in power down mode and the load is applied between HPR / HPL and HPCM. the headphone detection can also trigger a corresponding interrupt.

6.2.6 Power Save Options

To save power, especially when driving 32 Ohm loads, a reduction of the bias current can be selected. Together with switching off the phantom ground this gives 4 possible operating modes.

Table 7 Headphone Power-Save Options

HPCM_OFF	IBR_HPH	IDD_HPH (typ.)	Load
0	0	2.2mA	16 Ohm
1	0	1.5mA	16 Ohm
0	1	1.5mA	32 Ohm
1	1	1.0mA	32 Ohm

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

6.2.7 Parameter

Table 8 Power Amplifier Block Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
R_L	Output Load	stereo mode	16			Ohm
Pout	Maximum Output Power	R_L= 32Ω		20		mW
		R_L= 16Ω		40		mW
A0	Gain	programmable gain	-43.43		1.07	dB
$\triangle$Ax	Gain Step-Size		0.8	1.5	2.2	dB
PSRR	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, R_L= 16Ω		90		dB
	Short Current Protection Level			145		mA
I_{OUT_pd}	I_{OUT} power down	HPGND is forced high	-20		20	uA
T_{power_up}				90		ms
SNR	Signal to Noise Ratio			100		dB
	Mute Attenuation			100		dB

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

6.2.8 Register Description

To get an interrupt on an over-current event, the corresponding bit in the IRQ_ENRD1 register (0x26h) has to be set. Also the interrupt request for HP detection has to be set in this register. The power-save options are controlled via AudioSet3 register (0x16h). All other headphone driver settings are controlled by the following two registers.

Right Headphone Register (02h)

Table 9 HPH_OUT_R Register

Bit	Name	Description
7,6	HP_OVC_TO	speaker over current time out: 11: 0 ms 10: 512 ms 01: 128 ms **00: 256 ms**
5	-	-
4..0	HPR_VOL	volume settings for right headphone output, adjustable in 32 steps @ 1.5dB 11111: 1.07 dB gain 11110: -0.43 dB gain .. 00001: -43.93dB gain **00000: -45.43 dB gain**

The register is R/W; default value is 00h

Left Headphone Register (03h)

Table 10 HPH_OUT_L Register

Bit	Name	Description
7	HP_Mute	**0: normal operation** 1: headphone output set to mute (mute is on during power-up)
6	HP_ON	**0: speaker stage not powered** 1: power up headphone stage
5	HPdetON	**0: no headphone detection** 1: enable headphone detection
4..0	HPL_VOL	volume settings for left headphone output, adjustable in 32 steps @ 1.5dB 11111: 1.07 dB gain 11110: -0.43 dB gain .. 00001: -43.93dB gain **00000: -45.43 dB gain**

The register is R/W; default value is 00h

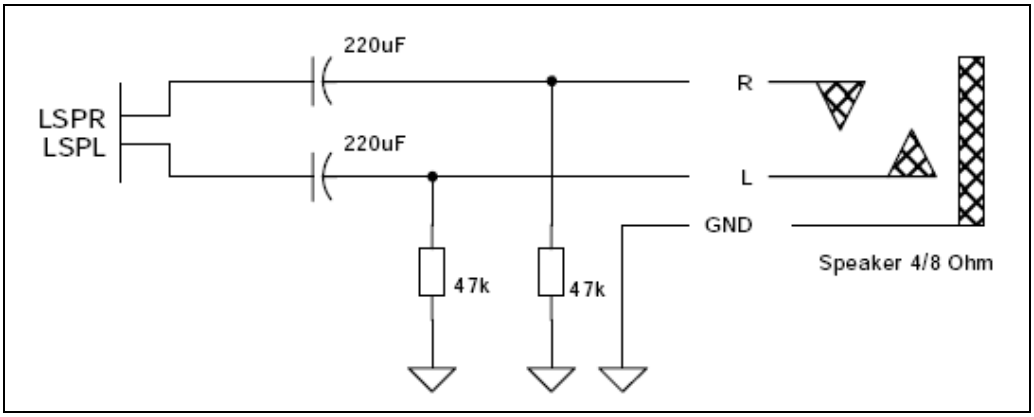
6.3 Speaker Output

6.3.1 General

The speaker output is designed to provide the stereo audio signal with 2x500mW @ 4Ω.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The maximum output power of 500mW @ 4Ω is achieved, by setting the mixer output to 1Vp and using the gain of +6dB.

Figure 3 Speaker Output



6.3.2 No-Pop Function

BGND pin, which needs a 100nF capacitor outside, gets charged on power-up to BVDD/2.To avoiding click and pop noise during power-up and shutdown, the output is automatically set to mute when the output stage is disabled.

The Start-up time before releasing mute is about 100ms. To avoid pop-noise the 150ms discharging time of SPR / SPL after a shutdown (220µF capacitor in stereo single ended mode assumed), have to be waited before starting up again.

6.3.3 Over-current Protection

This output stage has an over-current protection, which disables the output for 0 to 512ms. This value can be set in the speaker registers. The over-current protection limit of SPR and SPL pin is typical 700mA. To get an interrupt on an over-current event, the corresponding bit in the IRQ_ENRD1 register (0x26h) has to be set.

6.3.4 Power Save Options

When driving > 4Ω, two power save options can be chosen.

The output driver stage can be set to only 25% drive capacity, which will reduce the maximum output power. Additionally the bias currents can be reduced to 50% in 3 steps.

Table 11 Speaker Power-Save Options

LSP_LP	IBR_LSP	IDD_HPH (typ.)	Load
0	00	8mA	4 Ohm
1	00	2.8mA	16-32 Ohm
1	01	2.4mA	16-32 Ohm
1	10	1.9mA	16-32 Ohm
1	11	1.5mA	16-32 Ohm

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

6.3.5 Parameter

Table 12 Speaker Amplifier Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
R_L	Output Load	stereo mode	4			Ohm
		mono differential mode	8			Ohm
Pout	Maximum Output Power	R_L= 8Ω		1		W
A0	Gain	programmable gain	-40.5		6	dB
∆Ax	Gain Step-Size		0.8	1.5	2.2	dB
PSRR	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, no load		75		dB
	Short Current Protection Level			700		mA
I_{OUT_pd}	I_{OUT} power down	BGND is forced high	-20		20	uA
T_{power_up}				100		ms
SNR	Signal to Noise Ratio			100		dB
	Mute Attenuation			100		dB

BVDD = 5V, T_A= 25°C unless otherwise mentioned

6.3.6 Register Description

To get an interrupt on an over-current event, the corresponding bit in the IRQ_ENRD1 register (0x25h) has to be set. Changing the bias current or the output driver strength is done via AudioSet2 register (0x15h). All other speaker driver settings are controlled by the following two registers.

Right Speaker Register (04h)

Table 13 LSP_OUT_R Register

Bit	Name	Description
7,6	SP_OVC_TO	speaker over current time out: 11: 0 ms 10: 512 ms 01: 128 ms **00: 256 ms**
5	-	not used
4..0	SPR_VOL	volume settings for right speaker output, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

Left Speaker Register (05h)

Table 14 LSP_OUT_L Register

Bit	Name	Description
7	SP_Mute	**0: normal operation** 1: speaker output set to mute (mute is on during power-up)
6	SP_ON	**0: speaker stage not powered** 1: power up speaker stage
5	-	not used
4..0	SPR_VOL	volume settings for left speaker output, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

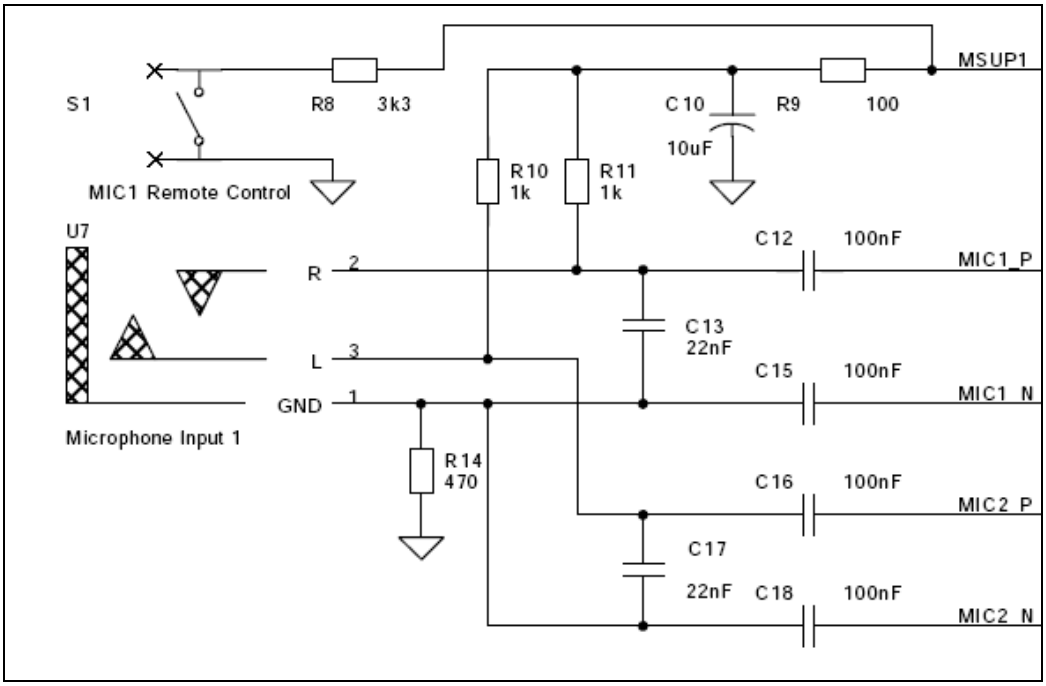
6.4 Microphone Inputs (2x)

6.4.1 General

AS3514 includes two identical microphone inputs. The blocks have differential inputs to a microphone amplifier with adjustable gain. This stage also includes an AGC.

The following volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the microphone input is not enabled, the volume settings are set to their default values. Changing of volume and mute control can only be done after enabling the input.

Figure 4 Microphone Input



6.4.2 AGC

The microphone amplifier includes an AGC, which is limiting the signal to 1Vp. The AGC has 15 steps with a dynamic range of about 29dB. The AGC is ON by default but can be disabled by a microphone register bit.

6.4.3 Supply & Detection

Each microphone input generates a supply voltage of 1.5V above HPHCM. The supply is designed for ≤2mA and has a 10mA current limit. In OFF mode the MICSUP terminal is pulled to AVDD with 30kohm. A current of typically 50uA generates an interrupt to inform the CPU, that a circuit is connected. When using HPHCM as headset ground the HPH–stage gives the interrupt. After enabling the HPH-stage through the CPU the microphone detection interrupt will follow.

6.4.4 Remote Control

Fast changes of the supply current of typically 500uA are detected as a remote button press, and an interrupt is generated. Then the CPU can start the measurement of the microphone supply current with the internal 10-bit ADC to distinguish which button was pressed. As the current measurement is done via an internal resistor, only two buttons generating a current of about 0.5mA and 1mA can be detected. With this 1mA as microphone bias is still available.

6.4.5 Parameter

Table 15 Microphone Inputs Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
A0	Gain	programmable gain	-40.5		6	dB
$\triangle$Ax	Gain Step-Size			1.5		dB
R_{inMIC}	Input Resistance	differential		15		kOhm
$A_{MIC}0$	MicAmp_Gain0			28		dB
$A_{MIC}1$	MicAmp_Gain1			34		dB
$A_{MIC}2$	MicAmp_Gain2			40		dB
	SoftClip_AGC_Range			15*2.0		dB
	Attack_Time			60		us
	Release_Time			120		ms
$V_{Innom}0$	Nominal_Input_Voltage0	MicInGain = 0dB, MicAmp_Gain0		40		mVp
$V_{Innom}1$	Nominal_Input_Voltage1	MicInGain = 0dB, MicAmp_Gain1		20		mVp
$V_{Innom}2$	Nominal_Input_Voltage2	MicInGain = 0dB, MicAmp_Gain2		10		mVp
SNR	Signal to Noise Ratio			100		dB
	Mute Attenuation			100		dB
Microphone Supply						
V_{MICsup}	Microphone Supply Voltage	0-2mA		2.95		V
I_{MIClim}	Mic. Supply Current Limit			10		mA
I_{MICdet}	Mic. Detection Current			50		uA
I_{REMdet}	Remote Detection Current				500	uA
V_{noise}	Voltage Noise			5.7		uV

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

6.4.6 Register Description

Enabling a microphone input is done via a control bit in the audio settings register (AudioSet1 register 0x14h). To get an interrupt on an microphone detection event, the corresponding bit in the IRQ_ENRD1 register (0x26h) has to be set, while a remote detection interrupt is controlled via IRQ_ENRD2 register (0x27h). All other microphone input settings are controlled by the following registers.

Right Microphone Registers (06h & 08h)

Table 16 MIC1_R & MIC2_R Register

Bit	Name	Description
7	M1_AGC_off M2_AGC_off	**0: automatic gain control enabled** 1: automatic gain control disabled
6,5	M1_Gain M2_Gain	**00: gain set to 28 dB** 01: gain set to 34 dB 10: gain set to 40 dB 11: gain set to tbd.
4..0	M1R_VOL M2R_VOL	volume settings for right microphone input, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The registers are R/W; default value is 00h

Left Microphone Register (07h & 09h)

Table 17 MIC1_L & MIC2_L Register

Bit	Name	Description
7	M1_Sup_off M2_Sup_off	**0: microphone supply enabled** 1: microphone supply disabled
6	M1_Mute_off M2_Mute_off	**0: microphone input set to mute** 1: normal operation
5	-	Not used
4..0	M1L_VOL M2L_VOL	Volume settings for left microphone input, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The registers are R/W; default value is 00h

6.5 Line Inputs (2x)

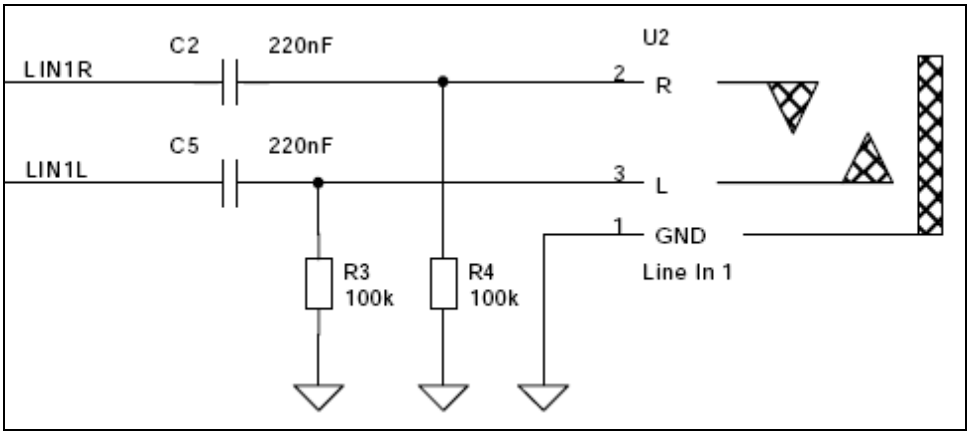
6.5.1 General

AS3514 includes two identical line inputs. The blocks can work in mono differential, 2x mono single ended or in stereo single ended mode.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the line input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

If using the inputs as mono differential, the volume setting for the right channel should be set to 0dB.

Figure 5 Line Input



6.5.2 Parameter

Figure 6 Line Input Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
A0	Gain	programmable gain	-34.5		12	dB
▵Ax	Gain Step-Size			1.5		dB
R_{inLINE}	Input Resistance	Mute		49		kOhm
		Min Gain, single ended stereo		100		kOhm
SNR	Signal to Noise Ratio			100		dB
	Mute Attenuation			100		dB

BVDD = 3.3V, T_A= 25ºC, fs=48kHz unless otherwise mentioned

6.5.3 Register Description

Enabling a line-input is done via a control bit in the audio settings register (AudioSet1 register 0x14h). All other line input settings are controlled by the following registers.

Right Line In Registers (0Ah & 0Ch)

Table 18 LINE_IN1_R & LINE_IN2_R Register

Bit	Name	Description
7,6	-	
5	LI1R_Mute_off LI2R_Mute_off	**0: right line input is set to mute** 1: normal operation
4..0	LI1R_VOL LI2R_VOL	volume settings for right line input, adjustable in 32 steps @ 1.5dB 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

The registers are R/W; default value is 00h

Left Line In Register (0Bh & 0Dh)

Table 19 LINE_IN1_L & LINE_IN2_L Register

Bit	Name	Description
7,6	LI1_Mode LI2_Mode	Single ended stereo or differential mono selection **00: inputs switched to single ended stereo** 01: inputs switched to differential mono 10: inputs switched to single ended mono 11: tbd.
5	LI1L_Mute_off LI2L_Mute_off	**0: left line input is set to mute** 1: normal operation
4..0	LI1L_VOL LI2L_VOL	Volume settings for left line input, adjustable in 32 steps @ 1.5dB 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

The registers are R/W; default value is 00h

6.6 Digital Audio Interface

6.6.1 Input

Digital audio data can be fed into the AS3514 via the I2S interface These input data are then used by the 18-bit DAC to generate the analog audio signal.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the DAC input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

6.6.2 Output

This block consists of an audio multiplexer where the signal, which should be recorded, can be selected. The output is then fed through a volume control to the 14 bit ADC. The digital output is done via an I2S interface.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the ADC output is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

The I2S output uses the same clocks as the I2S input. The sampling rate therefore depends also on the input sampling rate.

6.6.3 Signal Description

The digital audio interface uses the standard I2S format:

- left justified
- MSB first
- one additional leading bit

The first 18 bits are taken for DAC conversion. The on-chip synchronization circuit allows any bit-count up 32bit. When there are less than 18 bits sampled, the data sample is completed with “0”s. The ADC output is always 16 bit. If more SCLK pulses are provided, only the first 16 will be significant. All following bit will be “0”.

SCLK has not to be necessarily synchronous to LRCK but the high going edge has to be separate from LRCK edges. The LRCK signal has to be derived from a jitter-free clock source, because the on-chip PLL is generating a clock for the digital filter, which has to be always in correct phase lock condition to the external LRCK.

Figure 7 I2S_Timing

Error! Not a valid link.

6.6.4 Power Save Options

The bias current of the DAC block can be reduced in three steps down to 50% to reduce the power consumption.

6.6.5 Clock Supervision

The digital audio interface automatically checks the LRCK. An interrupt can be generated when the state of the LRCK input changes. A bit in the interrupt register represents the actual state (present or not present) of the LRCK.

6.6.6 Parameter

Table 20 DAC Block Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
A0	Gain	programmable gain DAC input	-43.43		1.07	dB
		programmable gain ADC output	-34.5		12	dB
$\triangle$Ax	Gain Step-Size			1.5		dB
	Mute Attenuation			100		dB
I2S inputs / outputs						
V_{IL}		SCLK, LRCK, SDI (30%DVDD/2)	-	-	0.42	V
V_{IH}		SCLK, LRCK, SDI (70%DVDD/2)	1.02	-	DVDD	V
V_{OL}		SDO @ 2mA	-	-	0.3	V
V_{OH}		SDO @ 2mA	2.6	-	-	V
t_{su}	Set-up Time	SDI versus high going edge of SCLK	80			ns
t_{hd}	Hold Time	SDI versus high going edge of SCLK	80			ns
t_{s1}, t_{s2}	Separation Time	SCLK high going edges separation from LRCK edges	80			ns
t_{jitter}	clock Jitter	LRCK	-20		20	ns

BVDD = 3.3V, DVDD = 2.9V, T_A= 25°C unless otherwise mentioned

6.6.7 Register Description

Enabling the DAC or ADC is done via a control bit in the audio settings register (AudioSet1 register 0x14h). To get an interrupt on a LRCK state change, the corresponding bit in the IRQ_ENRD1 register (0x25h) has to be set. Changing the bias current and adding a dither signal is done via AudioSet2 register (0x15h). All other DAC or ADC settings are controlled by the following two registers.

Right DAC Register (0Eh)

Table 21 DAC_R Register

Bit	Name	Description
7..5	-	
4..0	DAR_VOL	volume settings for right DAC input, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

Left DAC Register (0Fh)

Table 22 DAC_R Register

Bit	Name	Description
7	-	
6	DAC_Mute_off	**0: DAC input is set to mute** 1: normal operation
5	-	
4..0	DAL_VOL	volume settings for left DAC input, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

Right ADC Register (10h)

Table 23 ADC_R Register

Bit	Name	Description
7,6	ADCmux	**00: Stereo Microphone** 01: Line_IN1 10: Line_IN2 11: Audio SUM
5	-	
4..0	ADR_VOL	volume settings for right ADC input, adjustable in 32 steps @ 1.5dB 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

The register is R/W; default value is 00h

Left ADC Register (11h)

Table 24 ADC_L Register

Bit	Name	Description
7	AD_FS2	Divider selection for ADC clock **0: ADC sample clock is I2S LRCK / 2** 1: ADC sample clock is I2S LRCK / 4
6	ADC_Mute_off	**0: ADC input is set to mute** 1: normal operation
5	-	
4..0	ADL_VOL	Volume settings for left ADC input, adjustable in 32 steps @ 1.5dB 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

The register is R/W; default value is 00h

PLL Mode Register (1Dh)

Table 25 PLLMode Register

Bit	Name	Description
7..3	-	Not used
2,1	PLLmode<1:0>	Sets the MCLK generation for different LRCK speeds: **00: LRCK: 24-48kHz** 01: reserved 10: LRCK: 8-23kHz 11: reserved
0	-	Not used

The register is R/W; default value is 00h

6.7 Audio Output Mixer

6.7.1 General

The mixer stage sums up the audio signals of the following stages

- Microphone Input 1
- Microphone Input 2
- Line Input 1
- Line Input 2
- Digital Audio Input (DAC)

The mixing ratios have to be with the volume registers of the corresponding input stages. Please be sure that the input signals of the mixer stage are not higher than 1Vp. If summing up several signals, each has of course to be lower.

This shall insure that the output signal is also not higher than 1Vp to get a proper signal for the output amplifier. This stage has an automatic gain control, which automatically avoids clipping.

6.7.2 AGC

The audio mixer includes an AGC, which is limiting the signal to 1Vp. The AGC has 12 steps with a dynamic range of about 18dB. The AGC is ON by default but can be disabled by a register bit.

6.7.3 Register Description

The mixer stage has no direct associated registers.

Enabling the Summing / Mixer stage is done via a control bit in the audio settings register (AudioSet1 register 0x14h). Disabling the AGC is done via AudioSet2 register (0x15h).

6.8 Audio Settings

6.8.1 Register Description

First AudioSet Register (14h)

Table 26 AudioSet1 Register

Bit	Name	Description
7	ADC_on	1: ADC for recording is enables **0: ADC disabled**
6	SUM_on	1: Summing / Mixing stage is enabled **0: Summing / Mixing stage is disabled (no audio output possible)**
5	DAC_on	1: DAC enabled **0: DAC disabled**
4	LOUT_on	1: Line output enabled **0: Line output disabled**
3	LIN2_on	1: Line input 2 enabled **0: Line input 2 disabled**
2	LIN1_on	1: Line input 1 enabled **0: Line input 1 disabled**
1	MIC2_on	1: Microphone input 2 enabled **0: Microphone input 2 disabled**
0	MIC1_on	1: Microphone input 1 enabled **0: Microphone input 1 disabled**

The register is R/W; default value is 00h

Second AudioSet Register (15h)

Table 27 AudioSet2 Register

Bit	Name	Description
7	BIAS_off	1: Bias disabled **0: Bias enabled**
6	DITH_off	1: no dither added **0: add dither to the audio stream**
5	AGC_off	1: Automatic gain control for summing stage disabled 0**: Automatic gain control for summing stage enabled**
4,3	IBR_DAC<1:0>	Bias current reduction settings for DAC: **00: 0%** 01: 25% 10: 40% 11: 50%
2	LSP_LP	Low power mode for speaker output: 1: speaker output driver set for 16Ohm load or more (25%) **0: speaker output driver set for 4Ohm to 16Ohm load (100%)**
1,0	IBR_LSP<1:0>	Bias current reduction settings for speaker output: **00: 0%** 01: 17% 10: 34% 11: 50%

The register is R/W; default value is 00h

Third AudioSet Register (16h)

Table 28 AudioSet3 Register

Bit	Name	Description
7..3	-	Not used
2	ZCU_off	Zero cross gain update of audio outputs 1: zero cross update disabled **0: zero cross update enabled**
1	IBR_HPH	Bias current reduction settings for headphone output: 1: headphone output driver set for 32Ohm load or more (68%) **0: headphone output driver set for 16Ohm load (100%)**
0	HPCM_off	Headphone common mode buffer settings: 1: headphone CM buffer is switched off **0: headphone CM buffer is switched on**

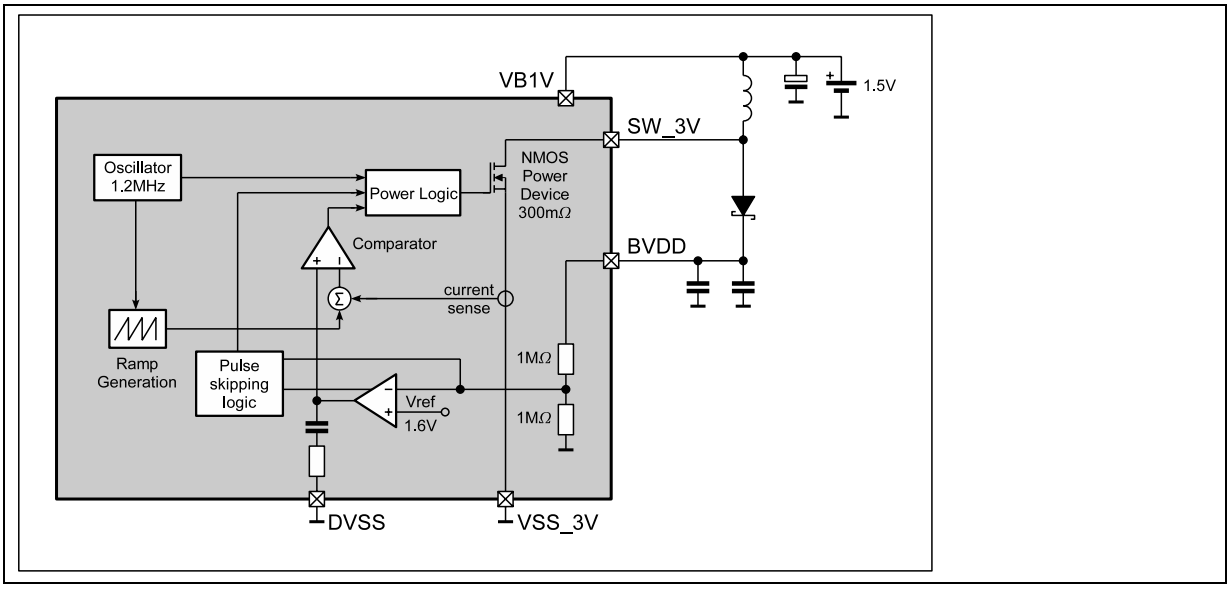
The register is R/W; default value is 00h

6.9 3V Step-Up Converter

6.9.1 General

- Output voltage 3V to 3.6V (BVDD) programmable in 4 steps via DCDC3p bit to save power
- Input voltage 1V (1.2V) to 3V, voltages higher than that can be connected to BVDD directly
- Maximum output current to BVDD: 150mA
- Current mode operation
- On-chip compensation and feedback network
- On chip 300mΩ NMOS switch
- PWM mode with 1.2MHz switching frequency
- Inductor current limitation 850mA
- Pulse skipping capability
- Low quiescent current: 40µA in PFM-mode, 300µA in PWM mode
- ≤1µA shutdown current
- uses external coil (6.8uH) and Schottky diode (500mA)

Figure 8 DCDC Block Diagram



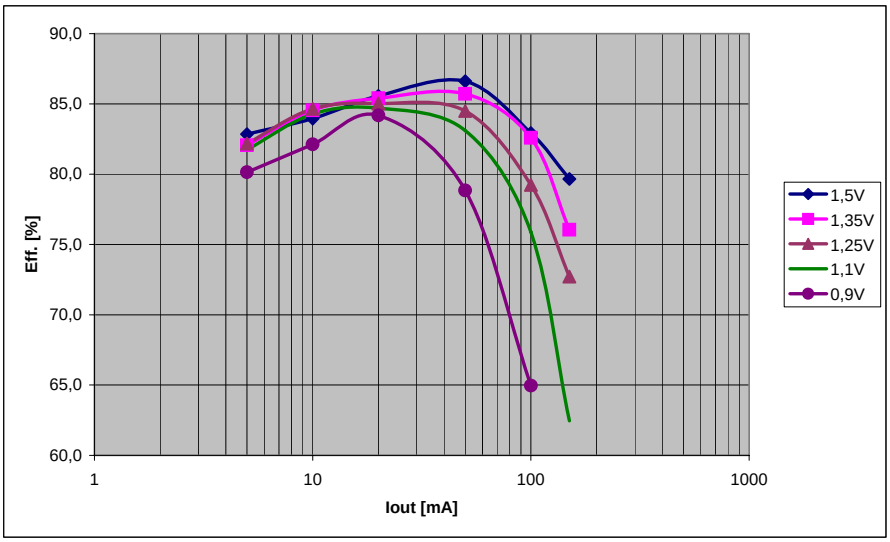
6.9.2 Parameter

Table 29 DCDC Boost Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
$I_{VDD2.9}$	Supply Current	Power down mode			5	µA
		PFM mode operation		40		µA
		PWM mode (low output load)		300		µA
$V_{STARTUP}$	Minimum Startup Voltage	R_{Load}>220Ω		1.0		V
V_{HOLD}	Hold-on Voltage	I_{OUT}=1mA, VBAT falling from 1.5 to 0V		0.5		V
R_{SW_on}	Internal Switch R_{DS_ON}			300		mΩ
f_{SW}	Switching Frequency	Start-up, X3VOK=1	100	250	500	kHz
		PWM mode operation, X3VOK=0	0.9	1.2	1.42	MHz
t_{ON_min}	Minimum On-time			100		ns
t_{OFF_min}	Minimum Off-time			100		ns
η_{eff}	Efficiency	I_{OUT}=20mA, Vin=1.35		85		%
		I_{OUT}=50mA, Vin=1.5		87		%
I_{SW_LIM}	Current Limit	1.0V ≤ VB1V ≤ 3.0V		0.85		A
I_{OUT}	Maximum Load Current	VB1V=1.0V		150		mA
ΔV_{OUT}	Output Voltage Ripple	ΔI_{OUT}=100mA in 100µs			tbd.	mV

Vin=1.0..2.0V, C(Vbat) = 2.2µF ceramic || 2000µF elko, C(Vreg) = 3 x 2.2µF ceramic, L=DS1608 4.7µH, Temp = 25deg

Figure 9 DCDC Boost Typical Performance Characteristics



BVDD=3.1V, L=DS1608 4.7µH, Temp = 25deg

6.10 Low Drop Out Regulators

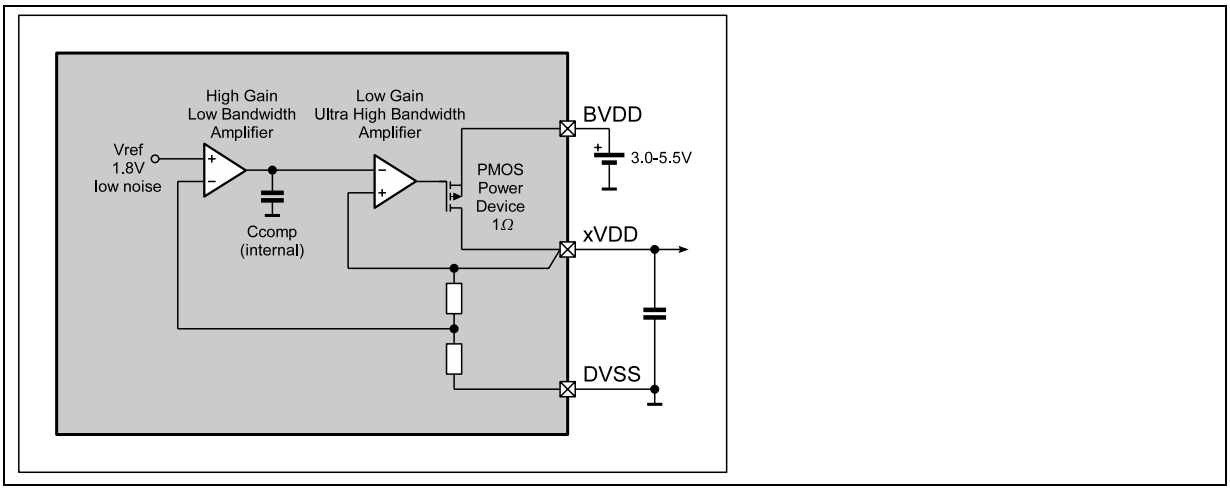
6.10.1 General

These LDO's are designed to supply sensitive analogue circuits, audio devices, AD and DA converters, micro-controller and other peripheral devices.

The design is optimised to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF +/-20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress high ripple on the battery at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

Figure 10 LDO Block Diagram



6.10.2 LDO1

This LDO generates the analog supply voltage used for the AS3514 itself.

- Input voltage is BVDD
- Output voltage is AVDD (typ. 2.9V)

6.10.3 LDO2

This LDO generates the digital supply voltage used for the AS3514 itself, microprocessor peripheral supply and external components like SD-Cards, Nand-Flashes, FM-Radio…

- Input Voltage is BVDD
- Output Voltage is DVDD (typ. 2.9V)
- Driver strength: 200mA

6.10.4 LDO3

This LDO will be used to supply the periphery voltage for a microprocessor.

- Input Voltage BVDD
- Output Voltage is PVDD 1.7 to 3.3V
- Driver strength: 200mA
- Programmable via P_PVDD pin and PVDDp bit in 8 steps

Table 30 PVDD programming

P_PVDD	PVDDp=0	PVDDp=1
VSS	OFF	OFF
150k to VSS	2.50V	2.36V
Open	3.33V	3.15V
150k to DVDD	2.90V	2.74V
DVDD	1.80V	1.70V

6.10.5 LDO4

This LDO will be used to supply peripheral circuits. Default value is 3.3V, but it can be manually programmed to 3.1V if needed.

- Input Voltage BVDD
- Output Voltage is CPVDD (3.1 or 3.3)
- Programmable via CPVDDp bit.
- Driver strength: 200mA

6.10.6 Parameter

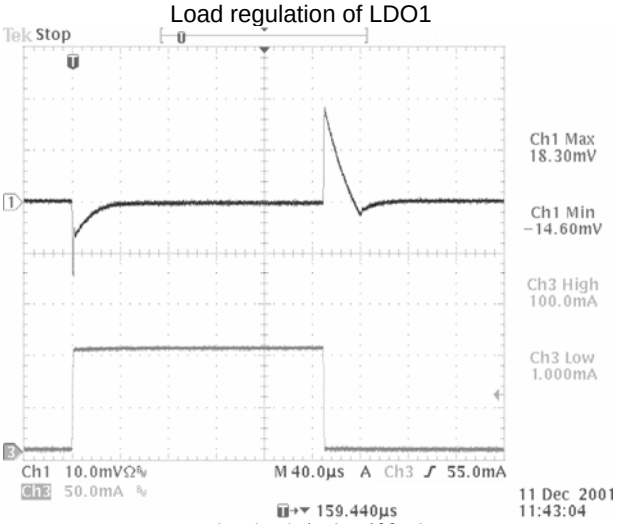
Table 31 LDOs Block Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
R_{ON}	On resistance				1	Ω
PSRR	Power supply rejection ratio	f=1kHz		70		dB
		f=100kHz		40		
I_{OFF}	Shut down current				100	nA
I_{VDD}	Supply current	without load			50	µA
Noise	Output noise	10Hz < f < 100kHz			50	μV_{rms}
t_{start}	Startup time				200	µs
V_{out_tol}	Output voltage tolerance		-50		50	mV
$V_{LineReg}$	Line regulation	LDO1, Static		<1		mV
		LDO1, Transient;Slope: t_r=10µs		<10		
$V_{LoadReg}$	Load regulation	LDO1, Static		<1		mV
		LDO1, Transient;Slope: t_r=10µs		<10		
I_{LIMIT}	Current limitation	LDO1, LDO2, LDO3, LDO4		400		mA

BVDD=4V; I_{LOAD}=150mA; T_{amb}=25ºC; C_{LOAD} =2.2µF (Ceramic); unless otherwise specified

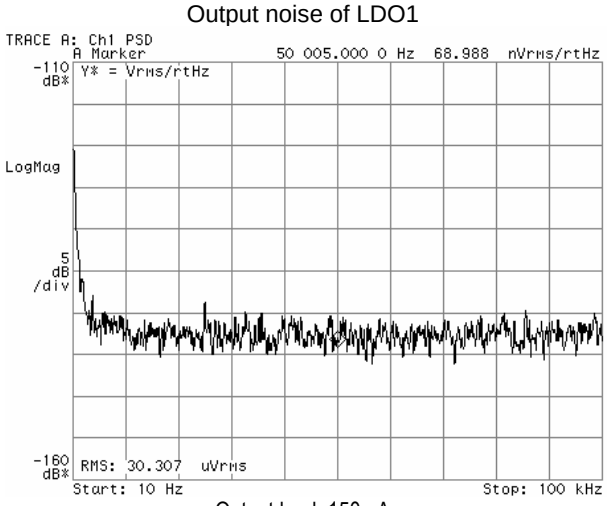
Figure 11 LDO Typical Performance Characteristics

Load regulation of LDO1



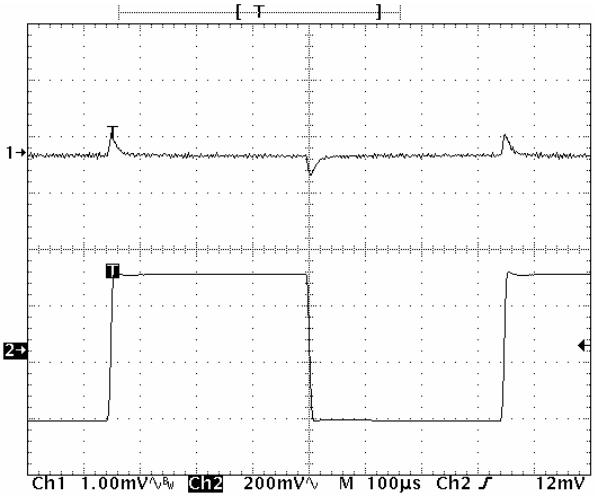
transient load: 1mA – 100mA
slope: 1µs

Output noise of LDO1



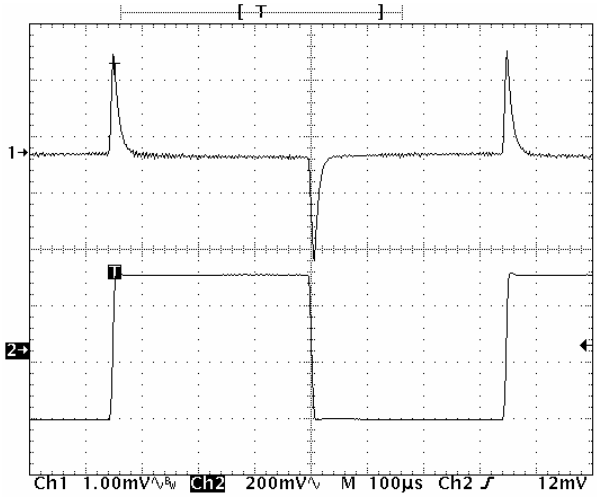
Output load: 150mA

LDO1



output load: 10mA
transient input voltage ripple: 500mV

LDO1



output load: 150mA
transient input voltage ripple: 500mV

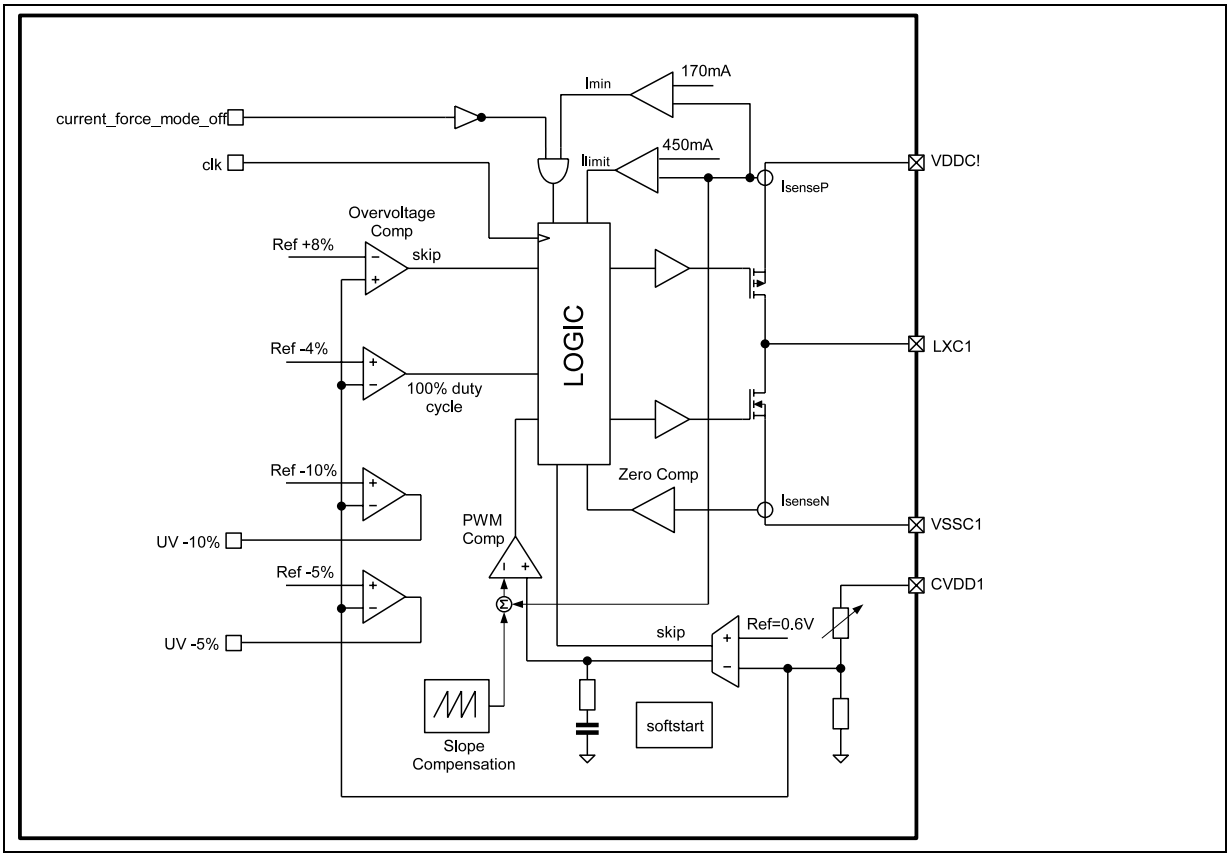
6.11 DCDC Step-Down Converter

6.11.1 General

This converter will be used to supply the core voltage for a microprocessor.

- Input Voltage BVDD
- Output Voltage 0.85 to 1.8 V
- Voltage setting via P_CVDD and CVDDp<1:0> bits in 16 steps
- driver strength 250mA

Figure 12 DCDC buck Block Diagram



6.11.2 Functional Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 97% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 250mA, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

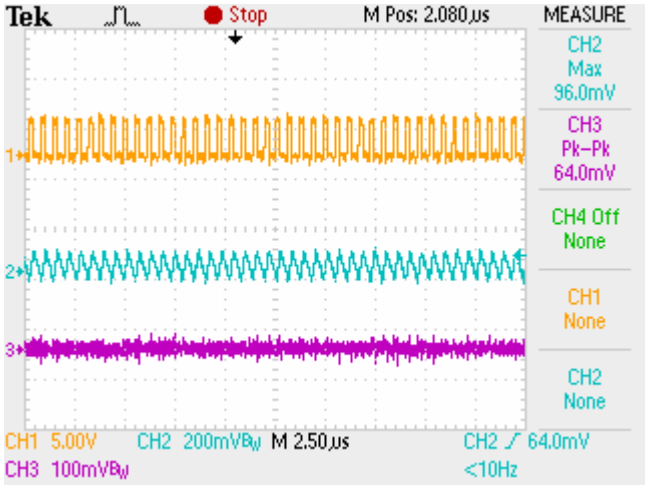
To achieve optimised performance in different applications, adjustable settings allow to compromise between high efficiency and low input, output ripple:

Low ripple, low noise operation:

Bit settings: cfm_off = 1 (disable current force mode)

In this mode there is no minimum coil current necessary before switching off the PMOS. As result, the ON time of the PMOS will be reduced down to tmin_on at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences. Especially in the case of an inverted coil current the regulator will not operate in pulse skip mode.

Figure *13 –DCDC buck with disabled current force mode*



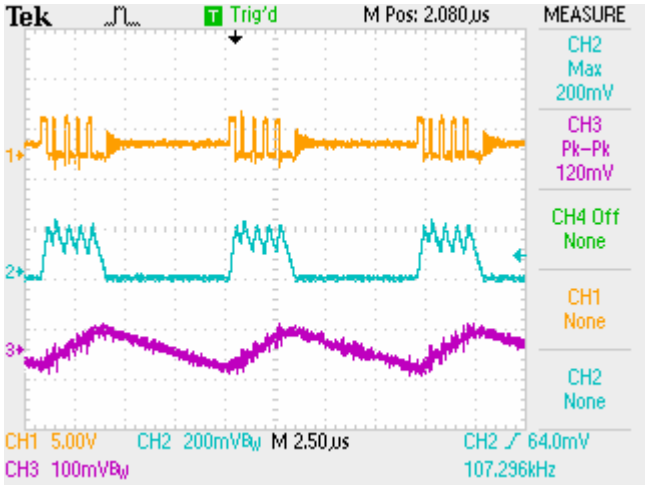
1: LXC1 voltage, 2:coil current (1mV=1mA) 3: output voltage

High efficiency operation:

Bit settings: cfm_off = 0 (enable current force mode)

In this mode there is a minimum coil current necessary before switching off the PMOS. As result, fewer pulses at low output loads are necessary, and therefore the efficiency at low output load is increased. On the other hand the output voltage ripple increases, and the noisy pulse skip operation is on up to a higher output current.

Figure *14 –DCDC buck with enabled current force mode*



1: LXC1 voltage, 2:coil current (1mV=1mA) 3: output voltage

It's also possible to switch between these two modes during operation:

E.g.:

cfm_off = 0: System is in idle state. No audio, RF signal. Decreased supply current preferred. Increase ripple doesn't effect system performance.

cfm_off = 1: System is operating. Audio signal on and/or RF signal used. Decreased ripple and noise preferred. Increased power supply current can be tolerated.

100% PMOS ON mode for low dropout regulation:

For low input to output voltage difference the pmos_mode bit can be cleared (default), to allow 100% duty cycle of the PMOS transistor, if the output voltage drops by more than 5%.

Table 32 CVDD programming

P_CVDD	CVDD
VSS	OFF
150k to VSS	1.0V
Open	1.2V
150k to DVDD	1.5V
DVDD	1.8V

Please note that on the LQFP package the P_CVDD is not accessible and "open". CVDD is therefore always set to 1.2V per default.

Additional the CVDD voltage can be trimmed with two register bits in the range of 0mV to -150mV

Table 33 CVDD trimming 1

CVDDp<1:0>	CVDD
00	Vnom (see Table 32)
01	Vnom – 50mV
10	Vnom - 100mV
11	Vnom - 150mV

This gives 0.85V to 1.8V as total range of the CVDD voltage.

Table 34 CVDD programming range

P_CVDD	CVDDp=11	CVDDp=10	CVDDp=01	CVDD=00
VSS	OFF	OFF	OFF	OFF
150k to VSS	0.85V	0.90V	0.95V	1.00V
Open	1.15V	1.10V	1.15V	1.20V
150k to DVDD	1.35V	1.40V	1.45V	1.50V
DVDD	1.65V	1.70V	1.75V	1.80V

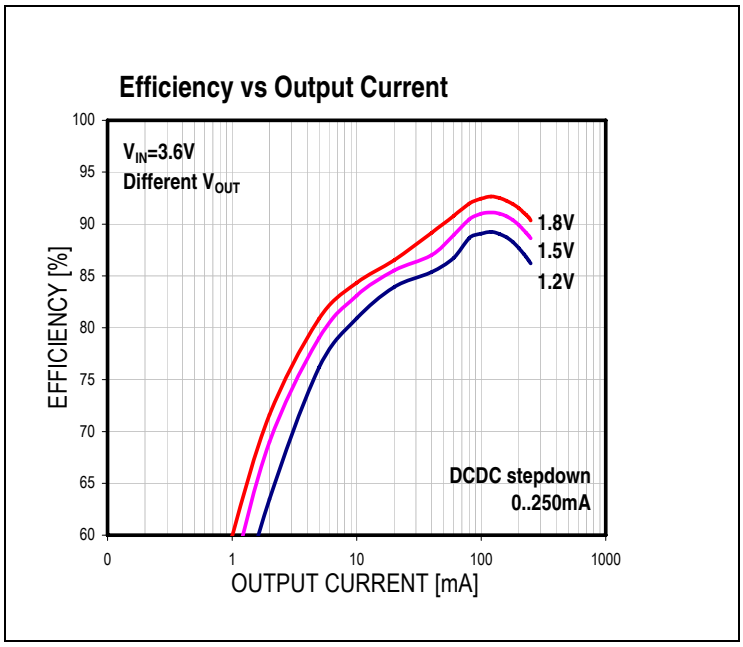
6.11.3 Parameter

Table 35 DCDC Buck Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
V_{IN}	Input voltage	BVDD	3.0		5.5	V
V_{OUT}	Regulated output voltage		0.85		1.8	V
V_{OUT_tol}	Output voltage tolerance		-50		50	mV
I_{LIMIT}	Current limit			450		mA
R_{PSW}	P-Switch ON resistance	BVDD=3.0V		0.5	0.7	Ω
R_{NSW}	N-Switch ON resistance	BVDD=3.0V		0.5	0.7	Ω
I_{load}	Maximum Load current			250		mA
f_{SW}	Switching frequency			1.2		MHz
C_{out}	Output capacitor	Ceramic, +/- 10% tolerance		10		µF
Lx	Inductor	+/- 10% tolerance	3.3		4.7	µH
η_{eff}	Efficiency	Iout=100mA, Vout=1.8V		92.5		%
I_{VDD}	Current consumption	Operating current without load Low power mode current Shutdown current		220 100 0.1		µA
t_{MIN_ON}	Minimum on time			80		ns
t_{MIN_OFF}	Minimum off time			40		ns
$V_{LineReg}$	Line regulation	Static		tbd		mV
		Transient;Slope: t_r=10µs		tbd		
$V_{LoadReg}$	Load regulation	Static		tbd		mV
		Transient;Slope: t_r=10µs		tbd		

BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

Figure 15 DCDC Buck Performance Characteristics



6.12 SYSTEM

6.12.1 General

The system block handles the power up and power down of the AS3514.

6.12.2 Power Up

The AS3514 powers up when on of the following condition is true:

- High signal on the PWR_UP pin (>80ms, >1V)
- Input voltage on the UVDD pin (USB plug in: >80ms, BVDD>3V, UVDD>4.5V)
- Input voltage on the CHG_IN pin (charger plug in: >80ms, BVDD>3V, CHG_IN>4.0V)
- Input voltage on RTCSUP pin (battery change: >1.35V)

To hold the chip in power up mode the PwrUpHld bit in the SYSTEM register (0x20h)is set.

6.12.3 Power Down

The chip automatically shuts off if one of the following conditions arises:

- Clearing the PwrUpHld bit in SYSTEM register (0x20h)
- I2C watchdog power down if enabled
- BVDD drops below the minimum threshold voltage (2.6V)
- Junction temperature reaches maximum threshold, set in SUPERVISOR register (0x24h)
- High signal on the PWR_UP pin for more than 11s.

Figure 16 Power Up Timing

Error! Not a valid link.

6.12.4 Parameter

Table 36 Supply Regulator Block Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
	DVDD_POR_OFF			2.15		V
	DVDD_POR_ON			2.0		V
	POR_ON/OFF_HYST			100		mV
LRCK WATCHDOG						
	F(LRCK)_WD_OFF		2	4.1	8	kHz
	ON_Delay			50		us
Digital Outputs						
	IRQ, PWGOOD @ 8 mA	-	-	0.3	V	
	IRQ @ 8 mA, push/pull mode only	2.6	-	-	V	
	IRQ, PWGOOD		10		uA	

DVDD=2.9V; T_{amb}=25ºC; unless otherwise specified

6.12.5 Register Description

SYSTEM Register (20h)

Table 37 System Register

Bit	Name	Description
7..4	Version <3:0>	Unique number to identify the design version **0010: revision 2**
3	PVDDp	PVDD trimming: **0: Vnom** 1: Vnom *17/18
2	CPVDDp	CPVDD trimming: **0: Vnom 3.3** 1: 3.1V
1	EnWDogPwdn	**0: forced power down through watchdog is disabled** 1: forced power down through watchdog is enabled
0	PwrUpHld	0: power up hold is cleared and supply is switched off **1: set to on after power on**

The register is R/W (bits 7 to 4 are read only); default value is 21h

CVDD / DCDC3 Register (21h)

Table 38 CVDD / DCDC3 Register

Bit	Name	Description
7	cfm_off	CVDD DCDC current force mode **0: force current mode is enabled (higher efficency)** 1: force current mode is disabled (lower noise)
6	pmos_mode	CVDD DCDC PMOS 100% on mode **0: PMOS can operate at 100% duty cycle (LDO mode possible)** 1: PMOS 100% duty cycle disabled
5	Reserved	For testing purpose only, must be set to 0h
4,3	DCDC3p	DCDC3 Vout programminig **00: 3.6V** 01: 3.2V 10: 3.1V 11: 3.0V
2	Reserved	For testing purpose only, must be set to 0h
0,1	CVDDp1	CVDD trimming: **00: Vnom** 01: Vnom –50mV 10: Vnom –100mV 11: Vnom – 150mV

The register is R/W; default value is 00h

6.13 Charger

6.13.1 General

This block can be used to charge a 4V Li-Io accumulator. It supports constant current and constant voltage charging modes with adjustable charging currents (50 to 400mA) and maximum charging voltage (3.9 to 4.25V).

6.13.2 Trickle Charge

If the battery voltage is below 3V, the charger goes automatically in trickle charge mode with 50mA charging current and 3.9V endpoint voltage. In this mode charging current and voltage are not precise, but provide a charger function also for deep discharged batteries. Also the temperature supervision

6.13.3 Temperature Supervision

This charger block also features a supply for an external 100k NTC resistor to measure the battery temperature while charging. If the temperature is too high, an interrupt can be generated.

6.13.4 Parameter

Table 39 Charger Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
I_{CHG_trick}	Charging Current (trickle charge)	BVDD<=3V, CHG_IN = 5.5V	30	50	100	mA
V_{CHG_trick}	Charger Endpoint Voltage (trickle charge)	BVDD<=3V, CHG_IN = 4.4V		0.72* CHG_IN	4.1	V
I_{CHG} (0-7)	Charging Current	BVDD > 3V	I_{NOM} -20%	I_{NOM}	I_{NOM} +20%	mA
V_{CHG} (0-7)	Charging Voltage	BVDD > 3V, end of charge is true	V_{NOM} -50mV	V_{NOM}	V_{NOM} +30mV	V
V_{ON_ABS}	Charger On Voltage IRQ	BVDD = 3V		3.1	4.0	V
V_{ON_REL}	Charger On Voltage IRQ	CHG_IN-CHG_OUT		170	240	mV
V_{OFF_REL}	Charger Off Voltage IRQ	CHG_IN-CHG_OUT	40	77		mV
V_{BATEMP_ON}	Battery Temp. high level	BVDD >3V	380	400	420	mV
V_{BATEMP_OFF}	Battery Temp. low level	BVDD >3V	480	500	520	mV
I_{CHG_OFF}	End Of Charge current level	BVDD >3V	5% I_{NOM}	10% I_{NOM}	15% I_{NOM}	mA
I_{REV_OFF}	Reverse current shut down	CHG_OUT = 5V, CHG_IN = VSS		<1		uA

BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

6.13.5 Register Description

End of charge and battery over-temperature interrupts can be generated with the corresponding bits in the IRQ_ENRD0 register (0x25h). Also the status of the charger (supply present or not) can be monitored via this register and if needed an interrupt is generated on a status change.

All other charger functions are controlled in the following register.

Charger Register (22h)

Table 40 Charger Register

Bit	Name	Description
7	TMPSup_off	**0: enables supply for external 100k NTC resistor** 1: disables supply
6..4	CHG_I	set maximum charging current 111: 400 mA 110: 350 mA .. 001: 100 mA **000: 50 mA**
3..1	CHG_V	set maximum charger voltage 111: 4.25 V 110: 4.2 V .. 001: 3.95 V **000: 3.9 V**
0	CHG_OFF	**0: enables Charger** 1: disables Charger

The register is R/W; default value is 00h

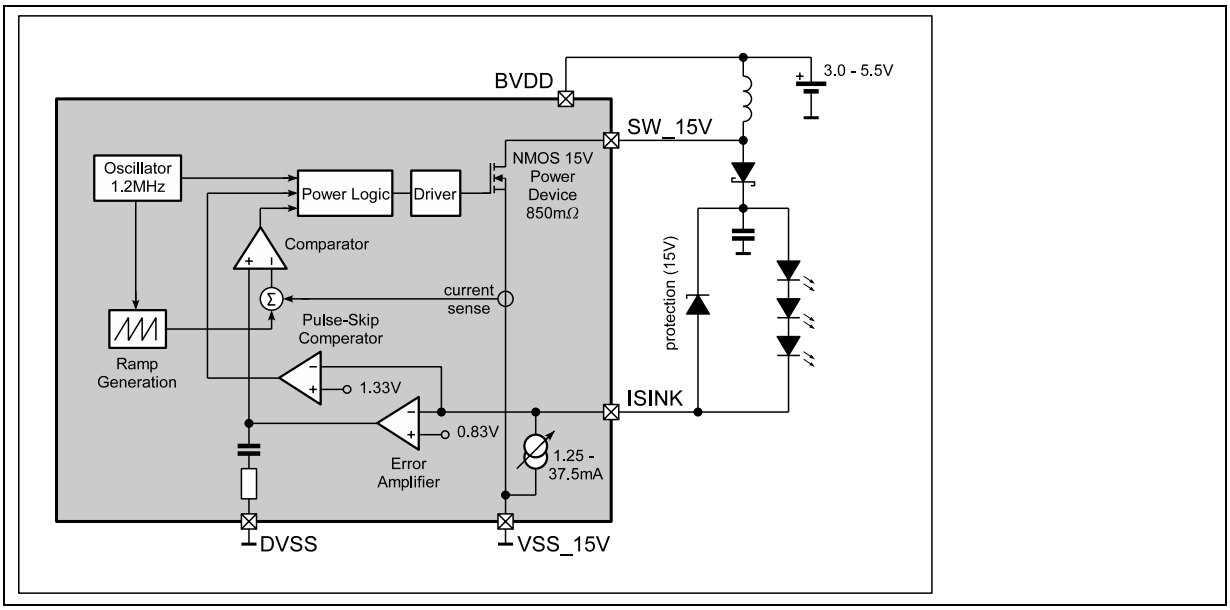
6.14 15V Step-Up Converter

6.14.1 General

The integrated Step-Up DC/DC Converter is a high efficiency current-mode PWM regulator, providing an output voltage up to 15V. A constant switching-frequency results in a low noise on supply and output voltages.

It has an adjustable sink current (1.25 to 38.75mA) to provide e.g. dimming function when driving white LEDs as back-light.

Figure 17 15V Step-Up converter Block Diagram



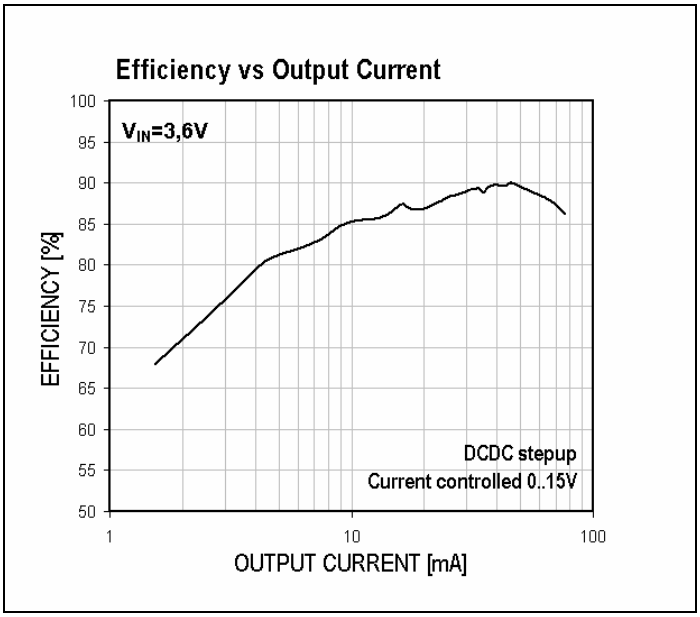
6.14.2 Parameter

Table 41 15V Step-Up Converter Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
V_{SW}	High Voltage Pin	Pin SW15	0		15	V
I_{VDD}	Quiescent Current	Pulse Skipping mode		140		µA
V_{FB}	Feedback Voltage, Transient	Pin ISINK	0		5.5	V
V_{FB}	Feedback Voltage, during Regulation	Pin ISINK		0.83		V
I_{SW_MAX}	Current Limit	V15_ON = 1		510		mA
R_{SW}	Switch Resistance	V15_ON = 0		0.85		Ω
I_{LOAD}	Load Current	@ 15V output voltage	0		40	mA
$V_{PULSESKIP}$	Pulse-skip Threshold	Voltage at pin ISINK, pulse skips are introduces when load current becomes too low.		1.33		V
F_{IN}	Fixed Switching Frequency			0.6		MHz
C_{OUT}	Output Capacitor	Ceramic		1		µF
L (Inductor)	I_{LOAD} > 20mA	Use inductors with small $C_{PARASITIC}$ (<100pF) for high efficency	17	22	27	µH
	I_{LOAD} < 20mA		8	10	27	
t_{MIN_ON}	Minimum On-Time		90		180	ns
MDC	Maximum Duty Cycle	Guaranteed per design	88	91	94	%

BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

Figure 18 15V Step-Up Performance Characteristics



6.14.3 Register Description

All functions can be controlled via the following register.

DCDC15 Register (23h)

Table 42 DCDC15 Register

Bit	Name	Description
7..5	Reserved	For testing purpose only, must be set to 0h
4..0	I_V15<4..0>	Defines the current through the LED = 1.25mA * I_V15 00000: off 00001: 1.25mA 00010: 2.5mA .. 11110: 37.5mA 11111: 38.75mA

The register is R/W; default value is 00h

6.15 Supervisor

6.15.1 General

This supervisor function can be used for automatic detection of BVDD brown out or junction over-temperature condition.

6.15.2 BVDD Supervision

The supervision level can be set in 8 steps @ 60mV from 2.74 to 3.16V. If the level is reached an interrupt can be generated. If BVDD reaches 2.6V the AS3514 shuts down automatically.

6.15.3 Junction Temperature Supervision

The temperature supervision level can also be set by 5 bits (120 to –15°C). If the temperature reaches this level, an interrupt can be generated. The over-temperature shutdown level is always 20°C higher. If the IRQ level is set to 120°C the shutdown is disabled.

6.15.4 Register Description

Interrupts for battery supervision has to be enabled in the IRQ_ENRD0 register (0x25h), while the over-temperature interrupt is controlled via the IRQ_ENRD1 register (0x26h). All other functions can be set via the following register.

SUPERVISOR Register (24h)

Table 43 Supervisor Register

Bit	Name	Description
7..5	BVDD_Sup<2:0>	Supervision of BVDD brown out V_BrownOut=2.74+x*60mV 000: 2.74V 001: 2.80V ... 110: 3.10V 111: 3.16V
4..0	JT_Sup<4:0>	Junction temperature supervision: Temp_ShutDown=140-x*5°C Temp_IRQ=120-x*5°C **Error! Not a valid link.**

The register is R/W; default value is 00h

6.16 Interrupt Generation

6.16.1 General

All interrupt sources can get enabled or disabled by corresponding bits in the 3 IRQ-bytes. By default no IRQ source is enabled.

The IRQ output can get configured to be PUSH/PULL or OPEN_DRAIN and ACTIVE_HIGH or ACTIVE LOW with 2 bits in IRQ_ENRD2 register (0x27h). Default state is push/pull and active_high.

6.16.2 IRQ Source Interpretation

There are 3 different modules to process interrupt sources:

LEVEL

The IRQ output is kept active as long as the interrupt source is present and this IRQ-Bit is enabled

EDGE

The IRQ gets active with a high going edge of this source. The IRQ stays active until the corresponding IRQ-Register gets read.

STATUS CHANGE

The IRQ gets active when the source-state changes. The change bit and the status can be read to notice which interrupt was the source. The IRQ stays active until the corresponding interrupt register gets read.

6.16.3 De-bouncer

There is a de-bouncer function implemented for USB and CHARGER. Since these 2 signals can be unstable for the phase of plug-in or unplug, a de-bounce time of 512ms/256ms/128ms/0ms can be selected by 2 bits in the IRQ_ENRD2 register (0x27h).

6.16.4 Register Description

First Interrupt Register (25h)

Table 44 IRQ_ENRD0 Register

Bit	Name	Int. Type	Description
7	CHG_tmphigh	Level	1: battery temperature was too high and the charger was turned off
6	CHG_endofch	Edge	1: charging is complete, turn charger off After turning off the charger, IRQ will be released.
5	CHG_status		1: charger connected, also valid if charger is connected during wakeup
4	CHG_changed	Status change	1: charger status changed, check CHG_status
3	USB_status		1: USB connected, also valid if USB is connected during wakeup
2	USB_changed	Status change	1: USB status changed, check UB_status
1	RVDD_waslow	Level	1: if RTC supply was low, RTC not longer valid IRQ will be released by any I2C action.
0	BVDD_islow	Level	1:BVDD has reached brown out level

The register is R/W; default value is 00h

By writing to the register the corresponding interrupt is enabled, reading the register delivers the interrupt source.

Second Interrupt Register (26h)

Table 45 IRQ_ENRD1 Register

Bit	Name	Int. Type	Description
7	JTEMP_high	Level	1: Junction temperature has reached supervision level
6	LSP_overcurr	Level	1: LSP output is in over-current off mode
5	HPH_overcurr	Level	1: HPH output is in over-current off mode
4	I2S_status		1: LRCK of I2S interface is present
3	I2S_changed	Status change	1: I2S LRCK clock was started or stopped, check I2S_status
2	MIC2_connect	Level	1: Microphone was connected to MIC port 2 IRQ will be released after enabling the microphone stage. Detecting a microphone during operation has to be done by measuring the supply current.
1	MIC1_connect	Level	1: Microphone was connected to MIC port 1 IRQ will be released after enabling the microphone stage. Detecting a microphone during operation has to be done by measuring the supply current.
0	HPH_connect	Level	1: Headphone was connected to HHP port IRQ will be released after enabling the headphone output. Detecting a headphone during operation is not possible.

The register is R/W; default value is 00h

By writing to the register the corresponding interrupt is enabled, reading the register delivers the interrupt source.

Third Interrupt Register (27h)

Table 46 IRQ_ENRD2 Register

Bit	Name	Int. Type	Description
7..6	T_deb<1:0>	-	USB and charger debounce time control 00: 512ms 01: 256ms 10: 128ms 00: 0ms
5	IRQ_Acthigh	-	1: IRQ is active high 0: IRQ is active low
4	IRQ_PushPull	-	1: IRQ output is push pull 0: IRQ output is open drain
3	Remote_Det2	Edge	1: Mic2 supply current got increased, Remote detection ➔ measure Mic2 supply current
2	Remote_Det1	Edge	1: Mic1 supply current got increased, Remote detection ➔ measure Mic1 supply current
1	RTC_update	Edge	1: RTC timer IRQ occured
0	ADC_EndCon	Edge	1: 8-bit ADC conversion completed

The register is R/W; default value is 00h

By writing to bit 0 to 3, the corresponding interrupt is enabled, reading these bits delivers the interrupt source.

6.17 Real Time Clock

6.17.1 General

The real time clock block is an independent block, which is still working even the AS3514, is shut down. The block uses a standard 32kHz crystal that is connected to a low power oscillator. An internal 32bit second register stores the current time.

The RTC block has special functions for trimming the time base and generating interrupts every second or minute.

6.17.2 RTC supply

The internal RTC is supplied via the RTCSUP pin. The block has an internal LDO to generate the RTC supply voltage on RVDD pin. This voltage can be programmed via the RTCV register (0x28h). If the internal RTC is not used, RVDD can be used to supply an external RTC block.

If the supply voltage on RTCSUP pin rises, the whole AS3514 gets powered up.

6.17.3 Register Description

A RTCSUP low condition can be signalled by an interrupt request, if the corresponding bit in the IRQ_ENRD0 register (0x25h) is set. To get a second or minute interrupt the enable bit in IRQ_ENRD2 register (0x27h) All other RTC functions can be controlled and accessed via the following registers.

RTCV Register (28h)

Table 47 RTCV Register

Bit	Name	Description
7..4	VRTC<3..0>	Sets the RTC supply voltage, 16 steps @ 0.1V, default is 1.2V 0000: 1V 0001: 1.1V **0010: 1.2V** ... 1110: 2.4V 1111: 2.5V
3,2	Reserved	For testing purpose only, must be set to 0h
1	RTC_ON	0: Disable clock for RTC **1: Enables clock for RTC**
0	OSC_ON	0: Disables RTC oscillator **1: Enables RTC oscillator**

The register is R/W; default value is 23h

RTCT Register (29h)

Table 48 RTCT Register

Bit	Name	Description
7	IRQ_MIN	**0: generates an interrupt every second** 1: generates an interrupt every minute
6..0	TRTC<6..0>	Trimming register for RTC, 128 steps @ 7.6ppm 000000: 1 (7.6ppm) 000001: 2 (15.2ppm) ... **100000: 64 (488ppm)** ... 111110: 126 (960.8ppm) 111111: 127 (968.4ppm)

The register is R/W; default value is 40h

RTC Registers (2Ah to 2Dh)

Table 49 RTC_0 to RTC_3 Register

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
2Ah	RTC_0	Qrtc<7>	Qrtc<6>	Qrtc<5>	Qrtc<4>	Qrtc<3>	Qrtc<2>	Qrtc<1>	Qrtc>0>	second register 0
2Bh	RTC_1	Qrtc<15>	Qrtc<14>	Qrtc<13>	Qrtc<12>	Qrtc<11>	Qrtc<10>	Qrtc<9>	Qrtc<8>	second register 1
2Ch	RTC_2	Qrtc<23>	Qrtc<22>	Qrtc<21>	Qrtc<20>	Qrtc<19>	Qrtc<18>	Qrtc<17>	Qrtc<16>	second register 2
2Dh	RTC_3	Qrtc<31>	Qrtc<30>	Qrtc<29>	Qrtc<28>	Qrtc<27>	Qrtc<26>	Qrtc<25>	Qrtc<24>	second register 3

The registers are R/W; default value is 00h

6.18 10-Bit ADC

6.18.1 General

This general purpose ADC can be used for measuring several voltages and currents to perform functions like battery monitor, temperature supervision, button press detection, etc..

6.18.2 Input Sources

Table 50 ADC10 Input Sources

Nr.	Source	Range	LSB	Description
0	BVDD	5.120V	5mV	check battery voltage of 4V LiIo accumulator
1	RTCSUP	5.120V	5mV	check RTC backup battery voltage
2	UVDD	5.120V	5mV	check USB host voltage
3	CHG_IN	5.120V	5mV	check charger input voltage
4	CVDD	2.560V	2.5mV	check charge pump output voltage
5	BatTemp	2.560V	2.5mV	check battery charging temperature
6	MicSup1	2.560V	2.5mV	check voltage on MicSup1 for remote control or external voltage measurement
7	MicSup2	2.560V	2.5mV	check voltage on MicSup2 for remote control or external voltage measurement
8	VBE1	1.024	1mV	measuring junction temperature @ 2uA
9	VBE2	1.024	1mV	measuring junction temperature @ 1uA
10	I_MicSup1	2.048mA typ.	2.0uA	check current of MicSup1 for remote control detection
11	I_MicSup2	2.048mA typ.	2.0uA	check current of MicSup2 for remote control detection
12	VBAT	2.560V	2.5mV	check single cell battery voltage
13..15	Reserved	1.024V	1mV	for testing purpose only

BVDD, RTCSUP, UVDD, CHG_IN

These sources are fed into a 1/5 voltage divider (180kΩ typ.) and further amplified by 2.5.

CVDD, BatTemp, MicSup1, MicSup2

These sources are fed directly to the ADC input multiplexer.

VBE1, VBE2

These inputs are first amplified by 2.5 and than fed to the ADC input multiplexer.

I_MicSup1, I_MicSup2

The measurement of the microphone supply LDOs is not very accurate, as the current-voltage conversion is only done by a single resistor which shows wide process and temperature variations. These measurements should be only used for remote function detection.

VBAT

This source is divided by 2.5 with a voltage divider (180kΩ typ.) and than amplified by 2.5. This has to be done, as VBAT can represent voltages up to 3.6V. Please note, that the maximum measurement rage will be still 2.560V

6.18.3 Reference

AVDD=2.9V is used as reference to the ADC. AVDD is trimmed to +/-20mV with over all precision of +/-29mV. So the absolute accuracy is +/-1%.

6.18.4 Parameter

Table 51 ADC10 Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
R_{DIV}	Input Divider Resistance	BVDD, RTCSUP, UVDD, CHG_IN, VBAT	138k	180k	234k	Ω
ADC_{FS}	ADC Full Scale Range		2.534	2.56	2.586	V
Ratio1	Divition Factor 1	BVDD, RTCSUP, UVDD, CHG_IN	0.198	0.2	0.202	1
Ratio2	Divition Factor 2	VBAT	0.396	0.4	0.404	1
Gain	ADC Gain Stage		2.475	2.5	2.525	V
T_{CON}	Conversion Time		-	34	50	µs
I_MIC_{FS}	I_MicSup1/2 Full Scale Range		1.4	2	2.8	mA

BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

6.18.5 Register Description

The conversion gets started by writing to the ADC_0 register (0x2Eh). After finishing the conversion an interrupt request can be generated if the corresponding bit in the IRQ_ENRD2 register (0x27h) is set. Conversion source and result can be set / read with the following two registers.

ADC_0 Register (2Eh)

Table 52 ADC_0 Register

Bit	Name	Description
7..4	ADC_Source	0000: BVDD 0001: RTCSUP 0010: UVDD 0011: CHG_IN 0100: CVDD 0101: BatTemp 0110: MicSup1 0111: MicSup2 1000: VBE_1uA 1001: VBE_2uA 1010: I_MicSup1 1011: I_MicSup2 1100: VBAT 1101: reserved 1110: reserved 1101: reserved
3,2	-	Not used
1	ADC<9>	ADC result bit 10
0	ADC<8>	ADC result bit 9

The register is R/W; default value is 000000xxb

ADC_1 Register (2Fh)

Table 53 ADC_1 Register

Bit	Name	Description
7	ADC<7>	ADC result bit 8
6	ADC<6>	ADC result bit 7
5	ADC<5>	ADC result bit 6
4	ADC<4>	ADC result bit 5
3	ADC<3>	ADC result bit 4
2	ADC<2>	ADC result bit 3
1	ADC<1>	ADC result bit 2
0	ADC<0>	ADC result bit 1

The register is R/W; default value is xxh

6.19 128 bit Fuse Array

6.19.1 General

This fuse array is used to store a unique identification number, which can be used for DRM issues. The number is randomly generated and programmed during the production process.

6.19.2 Register Description

UID Registers (30h to 3Fh)

Table 54 UID_0 to UDI15_3 Register

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
30h	UID_0	ID<7>	ID<6>	ID<5>	ID<4>	ID<3>	ID<2>	ID<1>	ID<0>	Unique ID byte 0
31h	UID_1	ID<15>	ID<14>	ID<13>	ID<12>	ID<11>	ID<10>	ID<9>	ID<8>	Unique ID byte 1
32h	UID_2	ID<23>	ID<22>	ID<21>	ID<20>	ID<19>	ID<18>	ID<17>	ID<16>	Unique ID byte 2
33h	UID_3	ID<31>	ID<30>	ID<29>	ID<28>	ID<27>	ID<26>	ID<25>	ID<24>	Unique ID byte 3
34h	UID_4	ID<39>	ID<38>	ID<37>	ID<36>	ID<35>	ID<34>	ID<33>	ID<32>	Unique ID byte 4
35h	UID_5	ID<47>	ID<46>	ID<45>	ID<44>	ID<43>	ID<42>	ID<41>	ID<40>	Unique ID byte 5
36h	UID_6	ID<55>	ID<54>	ID<53>	ID<52>	ID<51>	ID<50>	ID<49>	ID<48>	Unique ID byte 6
37h	UID_7	ID<63>	ID<62>	ID<61>	ID<60>	ID<59>	ID<58>	ID<57>	ID<56>	Unique ID byte 7
38h	UID_8	ID<71>	ID<70>	ID<69>	ID<68>	ID<67>	ID<66>	ID<65>	ID<64>	Unique ID byte 8
39h	UID_9	ID<79>	ID<78>	ID<77>	ID<76>	ID<75>	ID<74>	ID<73>	ID<72>	Unique ID byte 9
3Ah	UID_10	ID<87>	ID<86>	ID<85>	ID<84>	ID<83>	ID<82>	ID<81>	ID<80>	Unique ID byte 10
3Bh	UID_11	ID<95>	ID<94>	ID<93>	ID<92>	ID<91>	ID<90>	ID<89>	ID<88>	Unique ID byte 11
3Ch	UID_12	ID<103>	ID<102>	ID<101>	ID<100>	ID<99>	ID<98>	ID<97>	ID<96>	Unique ID byte 12
3Dh	UID_13	ID<111>	ID<110>	ID<109>	ID<108>	ID<107>	ID<106>	ID<105>	ID<104>	Unique ID byte 13
3Eh	UID_14	ID<119>	ID<118>	ID<117>	ID<116>	ID<115>	ID<114>	ID<113>	ID<112>	Unique ID byte 14
3Fh	UID_15	ID<127>	ID<126>	ID<125>	ID<124>	ID<123>	ID<122>	ID<121>	ID<120>	Unique ID byte 15

The register is read only.

6.20 VTRM-LDO

6.20.1 General

This LDO is generating a supply voltage for an external USB 1.1 transceiver out of the 5V USB master supply.

- Input Voltage is UVDD (4.5 to 5.5V)
- Output Voltage is VTRM (typ. 3.2V)
- Driver strength: ~10mA

6.21 I2C Control Interface

6.21.1 General

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr_Group8 - audioprocessors

- 8Ch_write
- 8Dh_read

Figure 19 I2C timing

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6.21.2 Parameter

Table 55 I2C Operating Conditions

Symbol	Parameter	Notes	Min	Typ	Max	Unit
VIL	CSCL, CSDA (max 30%DVDD)		0	-	0.87	V
VIH	CSCL, CSDA (min 70%DVDD)		2.03	-	5.5	V
HYST	CSCL, CSDA		200	450	800	mV
VOL	CSDA @3mA		-	-	0.4	V
Tsp	Spike insensitivity		50	100	-	ns
Speed	Frequency at CSCL		-	-	1	MHz
Tsetup		CSDA has to change Tsetup before rising edge of CSCL	100	-	-	ns
Thold		No hold time needed for CSDA relative to rising edge of CSCL	0	-	-	ns
TS		CSDA H hold time relative to CSDA edge for start/stop/rep_start	200	-	-	ns
Tdata		CSDA prop delay relative to lowgoing edge of CSCL	24	50	80	ns

DVDD =2.9V, T_{amb}=25ºC; unless otherwise specified

6.21.3 Register Description

Registers Overview (00h to 3Fh)

Table 56 I2C Register Overview

Addr	Name	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
00h	LINE_OUT_R	reserved		-	LOR_Vol<4:0> Gain from Mixer_Out to Line_Out= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
01h	LINE_OUT_L	LO_SES_DM<1:0>		-	LOL_Vol<4:0> Gain from Mixer_Out to Line_Out= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
02h	HPH_OUT_R	HP_OVC_TO<1:0>		-	HPR_Vol<4:0> Gain from Mixer_Out to HPH_Out= (-45.43dB ... +1.07dB)				
		0	0	0	0	0	0	0	0
03h	HPH_OUT_L	HP_Mute	HP_ON	HPdetON	HPL_Vol<4:0> Gain from Mixer_Out to HPH_Out= (-45.43dB ... +1.07dB)				
		0	0	0	0	0	0	0	0
04h	LSP_OUT_R	SP_OVC_TO<1:0>		-	SPR_Vol<4:0> Gain from Mixer_Out to LSP_Out= (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
05h	LSP_OUT_L	SP_Mute	SP_ON	-	SPL_Vol<4:0> Gain from Mixer_Out to LSP_Out= (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
06h	MIC1_R	M1_AGC_off	M1_Gain<1:0>		M1R_Vol<4:0> Gain from MicAmp_Out to Mixer_In= (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
07h	MIC1_L	M1_Sup_off	M1_Mute_off	-	M1L_Vol<4:0> Gain from MicAmp_Out to Mixer_In= (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
08h	MIC2_R	M2_AGC_off	M2_Gain<1:0>		M2R_Vol<4:0> Gain from MicAmp_Out to Mixer_In= (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
09h	MIC2_L	M2_Sup_off	M2_Mute_off	-	M2L_Vol<4:0> Gain from MicAmp_Out to Mixer_In= (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
0Ah	Line_IN1_R	-	-	LI1R_Mute_off	LI1R_Vol<4:0> Gain from LineIn_Pin to Mixer_In=-34.5dB+LI1R_VOL*1.5dB (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Bh	Line_IN1_L	LI1_Mode<1:0>		LI1L_Mute_off	LI1L_Vol<4:0> Gain from LineIn_Pin to Mixer_In= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Ch	Line_IN2_R	-	-	LI2R_Mute_off	LI2R_Vol<4:0> Gain from LineIn_Pin to Mixer_In= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Dh	Line_IN2_L	LI2_Mode<1:0>		LI2L_Mute_off	LI2L_Vol<4:0> Gain from LineIn_Pin to Mixer_In= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Eh	DAC_R	-	-	-	DAR_Vol<4:0> Gain from DAC_Out to Mixer_In= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
0Fh	DAC_L	-	DAC_Mute_off	-	DAL_Vol<4:0> Gain from DAC_Out to Mixer_In= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0

Addr	Name	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
10h	ADC_R	ADCmux<1:0>		-	ADR_Vol<4:0> Gain from ADCMux_Out to ADC_In= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
11h	ADC_L	AD_FS2	ADC_Mute_off	-	ADL_Vol<4:0> Gain from ADCMux_Out to ADC_In= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
14h	AudioSet1	ADC_on	SUM_on	DAC_on	LOUT_on	LIN2_on	LIN1_on	MIC2_on	MIC1_on
		0	0	0	0	0	0	0	0
15h	AudioSet2	BIAS_off	DITH_off	AGC_off	IBR_DAC<1:0>		LSP_LP	IBR_LSP<1:0>	
		0	0	0	0	0	0	0	0
16h	AudioSet3	-	-	-	-	-	ZCU_OFF	IBR_HPH	HPCM_off
		0	0	0	0	0	0	0	0
1Dh	PLL_MODE	-	-	-	-	-	PLLmode<2:0>		-
		0	0	0	0	0	0	0	0
20h	SYSTEM	Design_Version<3:0>				PVDDp	CVDDp	EnWDogPwdn	PwrUPHld
		0	0	1	0	0	0	0	1
21h	CVDD/DCDC3	cfm_off	pmos_mode	For testing only	DCDC3p<1:0>		For testing only	CVDDp<1:0>	
		0	0	0	0	0	0	0	0
22h	CHARGER	TmpSup_off	CHGI<2:0>			CHGV<2:0>			CHG_off
		0	0	0	0	0	0	0	0
23h	DCDC15	For testing purpose only, must be set to 0h			I_V15<4:0>				
		0	0	0	0	0	0	0	0
24h	SUPERVISOR	BVDD_Sup<2:0>			JT_Sup<4:0>				
		0	0	0	0	0	0	0	0
25h	IRQ_ENRD0	CHG tmphigh	CHG endofch	CHG status	CHG changed	USB status	USB changed	RVDD was low	BVDD Is low
		0	0	0	0	0	0	0	0
26h	IRQ_ENRD1	JTEMP high	LSP overcurr	HPH overcurr	I2S status	I2S changed	Mic2 connect	Mic1 connect	HeadPh Connect
		0	0	0	0	0	0	0	0
27h	IRQ_ENRD2	T_deb<1:0>		IRQ_ActHigh	IRQ_PushPull	Remote_Det2	Remote_Det1	RTC_Update	ADC_EndCon
		0	0	0	0	0	0	0	0
28h	RTCV	VRTC<3:0>				For testing purpose only, must be set to 0h		RTC_ON	OSC_ON
		0	0	1	0	0	0	1	1
29h	RTCT	IRQ_MIN	TRTC<6:0>						
		0	1	0	0	0	0	0	0
2Ah	RTC_0	Qrtc<7:0>							
		0	0	0	0	0	0	0	0
2Bh	RTC_1	Qrtc<15:8>							
		0	0	0	0	0	0	0	0
2Ch	RTC_2	Qrtc<23:16>							
		0	0	0	0	0	0	0	0
2Dh	RTC_3	Qrtc<31:24>							
		0	0	0	0	0	0	0	0
2Eh	ADC_0	ADC_Source<3:0>				-	-	ADC<9:8>	
		0	0	0	0	0	0	X	X
2Fh	ADC_1	ADC<7:0>							
		X	X	X	X	X	X	X	X

Addr	Name	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
30-3F	UID_0 .. 15	ID<7:0> ... ID>127:120>							

7 Electrical Specification

Table 57 Audio Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
DAC Input to Line Output						
FS	Full Scale Output	1kHz FS input		0.985		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		92		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS 1kHz input		89		dB
THD	Total Harmonic Distortion	1kHz FS input		-90		dB
SINAD	Signal to Noise and Distortion	A-weighted, 1kHz FS input		83		dB
Line Input to Line Output						
FS	Full Scale Output	1kHz 1V_{RMS} (FS) input		0.95		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		93		dB
THD	Total Harmonic Distortion	1kHz 1V_{RMS} (FS) input		-85		dB
SINAD	Signal to Noise and Distortion	A-weighted, 1kHz FS input		80		dB
CS	Channel Separation			89		dB
DAC Input to HP Output						
FS	Full Scale Output	R_L= 32Ω		0.950		V_{RMS}
		R_L= 16Ω		0.944		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		91		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS 1kHz input		90		dB
THD	Total Harmonic Distortion	no load, 1kHz FS input		-90		dB
		Pout=20mW, R_L= 32Ω, f=1kHz FS input		-73		dB
		Pout=40mW, R_L= 16Ω, f=1kHz FS input		-66		dB
SINAD	Signal to Noise and Distortion	A-weighted, no load, 1kHz FS input		84		dB
		A-weighted,Pout=20mW, R_L= 32Ω, f=1kHz FS input		73		dB
		A-weighted,Pout=40mW, R_L= 16Ω, f=1kHz FS input		66	-60	dB
CS	Channel Separation	R_L = 32Ω		73		dB
		R_L = 16Ω		67		dB
Line Input to HP Output						
FS	Full Scale Output	R_L= 32Ω, 1kHz 1V_{RMS}(FS) input		0.930		V_{RMS}
		R_L= 16Ω, 1kHz 1V_{RMS} (FS) input		0.929		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		95		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS 1kHz (FS) input		95		dB
THD	Total Harmonic Distortion	no load, 1kHz 1$V_{RMS\ input}$		-85		dB
		Pout=20mW, R=32Ω, 1kHz 1V_{RMS} (FS) input		-73		dB
		Pout=40mW, R=16Ω, 1kHz 1V_{RMS} (FS) input		-68	-60	dB
SINAD	Signal to Noise and Distortion	A-weighted, no load, 1kHz 1$V_{RMS\ input}$		84		dB
		A-weighted, Pout=20mW, R=32Ω, 1kHz 1V_{RMS} (FS) input		73		dB
		A-weighted, Pout=40mW, R=16Ω, 1kHz 1V_{RMS} (FS) input		68		dB
CS	Channel Separation	R_L = 32Ω		73		dB
		R_L = 16Ω		68		dB

DAC to SP Output						
FS	Full Scale Output	R_L= 32Ω, 1kHz 1V_{RMS} (FS) input		1.036		V_{RMS}
		R_L= 16Ω, 1kHz 1V_{RMS} (FS) input		1.023		V_{RMS}
		R_L= 4Ω, 1kHz 1V_{RMS} (FS) input		0.950		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		91		dB
THD	Total Harmonic Distortion	no load, 1kHz 1V_{RMS} (FS) input		-88		dB
		R=32Ω, 1kHz 1V_{RMS} (FS) input		-78		dB
		R=16Ω, 1kHz 1V_{RMS} (FS) input		-71		dB
		R=4Ω, 1kHz 1V_{RMS} (FS) input, BVDD=5V		-60	-58	dB
SINAD	Signal to Noise and Distortion	A-weighted, no load, 1kHz 1V_{RMS} (FS) input		85		dB
		A-weighted, R=32Ω, 1kHz 1V_{RMS} (FS) input		77		dB
		A-weighted, R=16Ω, 1kHz 1V_{RMS} (FS) input		71		dB
		A-weighted, R=4Ω, 1kHz 1V_{RMS} (FS) input, BVDD=5V		60		dB
CS	Channel Separation	R_L = 32Ω		60		dB
MIC Input to ADC Output						
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		81		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS 1kHz input		80		dB
THD	Total Harmonic Distortion	1kHz 27mV_{RMS} (-3dB FS) input		-62		dB
SINAD	Signal to Noise and Distortion	A-weighted, 1kHz 27mV_{RMS} (-3dB FS) input		61		dB
Line Input to ADC Output						
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		83		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS 1kHz input		82		dB
THD	Total Harmonic Distortion	1kHz 1V_{RMS} (-3dB FS) input		-62		dB
SINAD	Signal to Noise and Distortion	A-weighted, 1kHz 1V_{RMS} (-3dB FS) input		61		dB

BVDD = 3.3V, T_A= 25°C, fs=48kHz, R_L= 10kΩ unless otherwise mentioned

8 Pinout and Packaging

8.1 Pin Description

Please observe that pin assignment may change in preliminary data sheet

Table 58 Pinlist CTBGA64 & LQFP64

CTBGA64 ball #	LQFP64 pin #	PinName	Type	Function
A1	1	BVDDC1	Supply	DCDC1V Battery terminal
B1	2	LXC1	Aout	DCDC1V Coil terminal
C3	3	VSSC1	Supply	DCDC1V Neg. Supply terminal
C2	4	CVDD	Ai/o	DCDC1V Output for CPU supply progr. 0.85-1.8V
D2	5	VB1V	Supply	Battery supply input for single cell application
C1	6	VSS3	Supply	DCDC3V Neg. Supply terminal
D1	7	SW3	Aout	DCDC3V Switch terminal
F1	8	SW15	Aout	DCDC15V Switch terminal
E1	9	VSS15	Supply	DCDC15V Neg. Supply terminal
D3	10	ISINK	Aout	DCDC15V Load Current Sink terminal
E2	11	DVSS	Supply	Digital Circuit Neg. Supply terminal
E3	12	BATTEMP	Ai/o	Charger Battery Temperature Sensor input (RNTC 100k)
D4	13	VTRM	Aout	USB1.1 VTRM Regulator output 3.25V
F2	14	UVDD	Ain	USB1.1 USB supply input
G1	15	CHGOUT	Aout	Charger Output prog. Ichg 50-400mA Vchg 3.9-4.25V
H1	16	CHGIN	Ain	Charger Input
G2	17	P_PVDD	Ain	5 State Prog Input of PVDD regulator
H2		P_CVDD	Ain	5 State Prog Input of CVDD regulator
F3	18	PWR_UP	Din Pull_dn	Power Up input
G3	19	CSDA	Di/o pull_up	Data I/O of two wire interface
G4	20	CSCL	Din pull_up	Clock Input of two wire interface
F5	21	Q32k	Dout OD	32kHz RTC clock output, default open drain
H3	22	LRCK	Din pull_dn	I2S Left/Right Clock
H4	23	SCLK	Din pull_dn	I2S Shift Clock
E4	24	SDI	Din pull_dn	I2S Data Input to DAC
H5	25	SDO	Dout	I2S Data output from ADC
F4	26	PWGOOD	Dout	Goes high when power up sequence is completed (XRES)
G5	27	IRQ	Dout OD	Interrupt Request Output, default open drain
	28	DVDD	Aout	Analog Circuit Pos. Supply terminal, to be supplied via pin 62 on LQFP
H6	29	XOUT	Ai/o	32kHz RTC Oscillator Crystal terminal
G6	30	RVDD	Aout	RTC Supply Regulator Output prog. to 1.0-2.5V
H7	31	XIN	Ai/o	32kHz RTC Oscillator Crystal terminal
G7	32	RTCSUP	Supply	RTC Pos. Supply terminal 5.5V max
H8	33	MIC1SUP	Ai/o	Microphone Supply 1 (2.95V) / Remote Input 1
G8	34	MIC1N	Ain	Microphone Input 1N
F6	35	MIC1P	Ain	Microphone Input 1P
F7	36	MIC2P	Ain	Microphone Input 2P
E7	37	MIC2N	Ain	Microphone Input 2N
F8	38	MIC2SUP	Ai/o	Microphone Supply 2 (2.95V) / Remote Input 2
E8	39	LIN1R	Ain	Line Input 1 Right Channel
E5	40	LIN1L	Ain	Line Input 1 Left Channel

CTBGA64 ball #	LQFP64 pin #	PinName	Type	Function
D8	41	LIN2R	Ain	Line Input 2 Right Channel
E6	42	LIN2L	Ain	Line Input 2 Left Channel
D7	43	AGND	Ai/o	Analog Reference (AVDD/2) decoupling cap terminal (10uF)
D6	44	VREF	Ai/o	Analog Reference (filtered AVDD) decoupling cap terminal (10uF)
C8	45	AVSS	Supply	Analog Circuit Neg Supply terminal
C7	46	LOUT_R	Aout	Line Output Right Channel / Ear Piece diff output N
B8	47	LOUR_L	Aout	Line Output Left Channel / Ear Piece diff output P
B7	48	AVDD	Supply	Analog Circuit Pos. Supply terminal
A8	49	HPGND	Ai/o	Headphone Amplifier Reference decoupling cap terminal (100nF)
A7	50	BVSS2	Supply	Headphone Amplifier Neg. Supply terminal
C6	51	HPH_CM	Aout	Headphone Common GND Output for DC-coupled speakers
B6	52	BVSS	Supply	Loudspeaker Amplifier Neg. Supply terminal
B5	53	HPH_R	Aout	Headphone Output Right Channel
A6	54	BVSS2	Supply	Headphone Amplifier Neg. Supply terminal
A5	55	HPH_L	Aout	Headphone Output Left Channel
D5	56	BGND	Ai/o	Loudspeaker Amplifier Reference decoupling cap terminal (100nF)
A4	57	BVDD	Supply	Pos. Supply Terminal 5.5V max.
C5	58	LSP_R	Aout	Loudspeaker Output Right Channel
B4	59	BVDD	Supply	Pos. Supply Terminal 5.5V max.
C4	60	LSP_L	Aout	Loudspeaker Output Left Channel
A3	61	BVDD	Supply	Pos. Supply Terminal 5.5V max.
B3	62	DVDD	Aout	LDO2 Regulator Output fixed 2.9V to be connected to pin 28 on LQFP
A2	63	PVDD	Aout	LDO3 Regulator Output prog. to 1.7-3.3V
B2	64	CPVDD	Aout	LDO4 Regulator Output limiter to 3.56V as ChargePump Input

Please observe that pin assignment may change in preliminary data sheet.

Note: The guarantee ESD robustness pin VSSC1 (double bond of 2 VSSC1 pads) and pin VSS3 (triple bond of 2x VSS3 and 1x SUB pad) have to be connected together inside the package (e.g. package substrate)

8.2 Ball & Pin Assignment

8.2.1 CTBGA64

please observe that pin assignment may change in preliminary data sheet

Figure 20 Ball Assignment CTBGA64

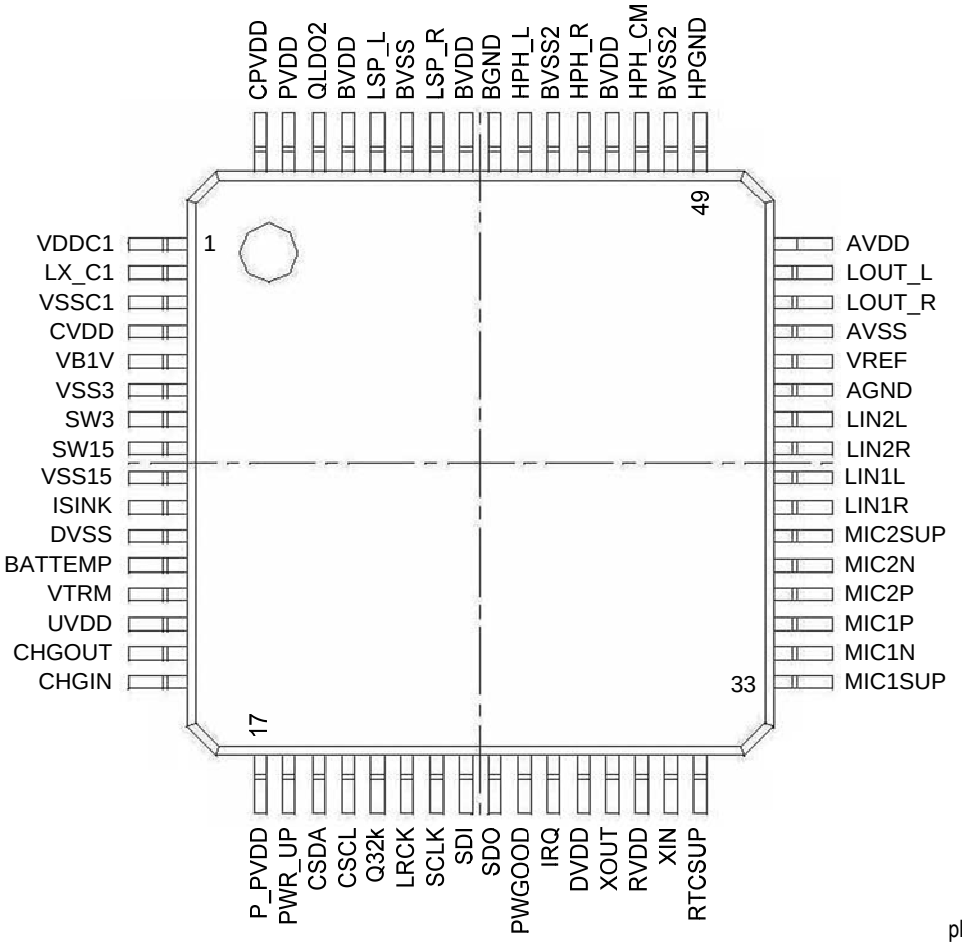
	1	2	3	4	5	6	7	8
A	VDDC1	PVDD	BVDD	BVDD	HPH_L	BVSS2	BVSS2	HPGND
B	LXC1	CPVDD	DVDD	BVDD	HPH_R	BVSS	AVDD	LOUT_L
C	VSS3	CVDD	VSSC1	LSP_L	LSP_R	HPH_CM	LOUT_R	AVSS
D	SW3	VB1V	ISINK	VTRM	BGND	VREF	AGND	LIN2R
E	VSS15	DVSS	BATTEMP	SDI	LIN1L	LIN2L	MIC2N	LIN1R
F	SW15	UVDD	PWR_UP	PWGOOD	Q32k	MIC1P	MIC2P	MIC2SUP
G	CHGOUT	P_PVDD	CSDA	CSCL	IRQ	RVDD	RTCSUP	MIC1N
H	CHGIN	P_CVDD	LRCK	SCLK	SDO	XOUT	XIN	MIC1SUP

please observe that pin assignment may change in preliminary data sheet

8.2.2 LQFP64

please observe that pin assignment may change in preliminary data sheet

Figure 21 Pin Assignment LQFP64

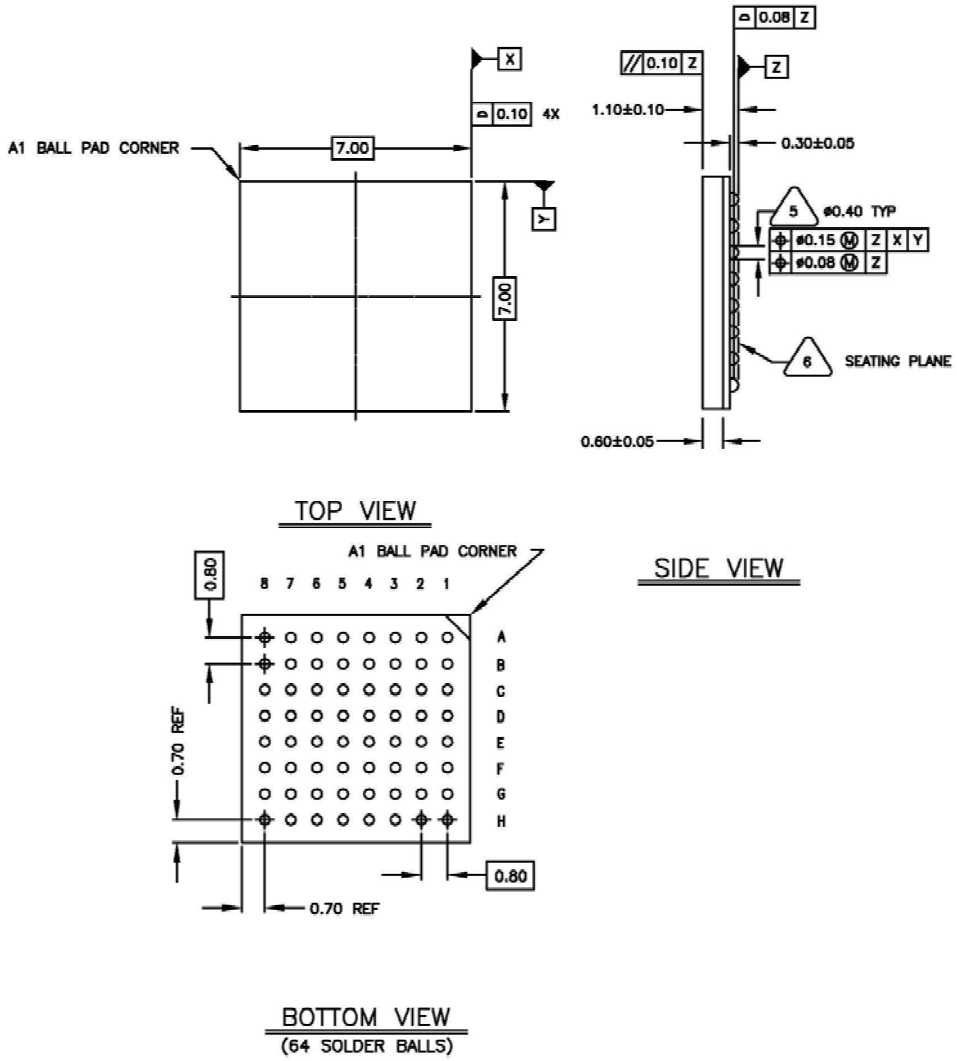


please observe that pin assignment may change in preliminary data sheet

8.3 Package Drawings

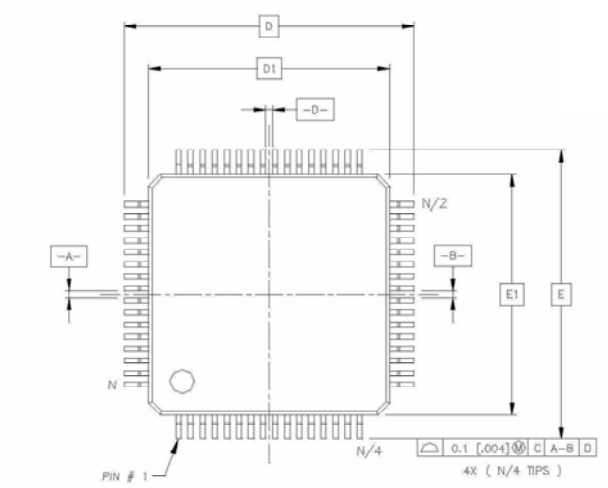
8.3.1 CTBGA64

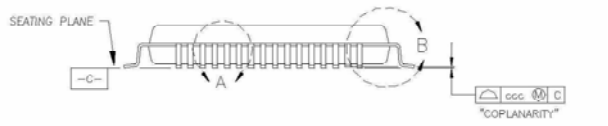
Figure 22 CTBGA64 7x7mm 0.8mm pitch



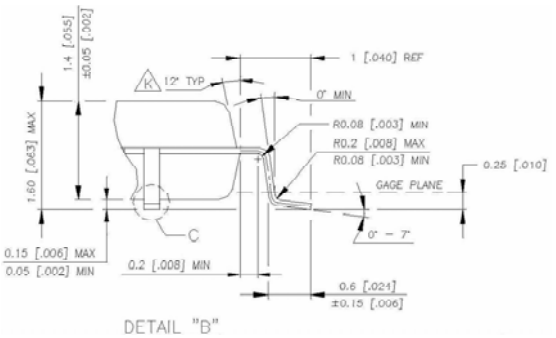
8.3.2 LQFP64

Figure 23 LQFP 10x10mm 0.5mm pitch

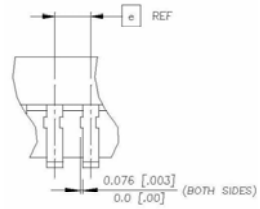




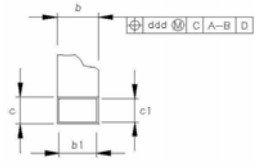
SYMBOL	10x10								
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
D	11.8	12	12.2	11.8	12	12.2	11.8	12	12.2
	.464	.472	.480	.464	.472	.480	.464	.472	.480
D1	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1
	.390	.394	.398	.390	.394	.398	.390	.394	.398
E	11.8	12	12.2	11.8	12	12.2	11.8	12	12.2
	.464	.472	.480	.464	.472	.480	.464	.472	.480
E1	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1
	.390	.394	.398	.390	.394	.398	.390	.394	.398
b	0.3	0.37	0.45	0.22	0.32	0.38	0.17	0.22	0.27
	.012	.015	.018	.009	.013	.015	.007	.009	.011
b1	0.3	0.35	0.4	0.22	0.3	0.33	0.17	0.2	0.23
	.012	.014	.016	.009	.012	.013	.007	.008	.009
c	0.09		0.2	0.09		0.2	0.09		0.2
	.004		.008	.004		.008	.004		.008
c1	0.09		0.16	0.09		0.16	0.09		0.16
	.004		.006	.004		.006	.004		.006
e	0.8			0.65			0.5		
	.031			.026			.020		
ccc	0.10			0.10			0.08		
	.004			.004			.003		
ddd	0.20			0.13			0.08		
	.008			.005			.003		
N	44			52			64		
N/2	22			26			32		
N/4	11			13			16		



DETAIL "B"



DETAIL "A"



DETAIL "C"

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 [.010] PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM BODY SIZE BY AS MUCH AS 0.15 [.006].
3. DRAWING CONFORMS TO JEDEC MS-026 REV. A.
4. COTROLLING DIMENSION IN MM.

9 Ordering Information

Device ID	Number	Package Type	Delivery Form	Description
AS3514[V]-XY[Z]	AS3514-QT	LQFP 64	Tray	evaluation only
	AS3514-BTZ	CTBGA 64	Tray	Package Size = 7x7mm
	AS3514-BRZ	CTBGA 64	Tape and Reel	Pitch = 0.8mm
	AS3514-WD	8" Wafer	Dies on Foil	

Where

V = **Version**

X = **Package Type**:

Q = LQFP 64 Thin Quad Flat Pack

B = CTBGA 64, Thin ChipArray Ball Grid Array 7x7mm

W = 8" Wafer

Y = **Delivery Form**:

T = Tray

R = Tape and Reel

D = Dies on Foil

Z = **Pb-free Status:**

Z = Pb-free/ RoHS package type

10 Copyright

11 Disclaimer

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