AS3518

Stereo Audio Codec with enhanced System Power Management

1 General Description

The AS3518 is an ultra low power stereo audio codec and is designed for Portable Digital Audio Applications.

It allows playback and recording in CD quality. With one microphone (including pre-amplifier and supply for an electret microphone) and three line inputs, it allows connecting a variety of audio inputs. The different audio signals can be mixed via an 8-channel mixer and fed to either a headphone output for 16Ω/32Ω headsets or a line output.

Further the device offers advanced power management functions. All necessary ICs and peripherals in a Digital Audio Player are supplied by the AS3518. It features 2 DCDC converters for core and memory/periphery supply as well as 4 LDOs. The different regulated supply voltages are programmable via the serial control interface.

The step-up converter for the backlight can operate up to 15V (with an external transistor even higher) in voltage and current control mode. An internal voltage protection is limiting the output voltage in the case of external component failures.

AS3518 also contains a Li-Ion battery charger with constant current, constant voltage and trickle charging. The maximum charging current is 460mA.

The AS3518 has an on-chip, phase locked loop (PLL) which generates the needed internal CODEC master clock. I2S Frame and shift-clock have to be applied from the processor for playback and recording.

Further the AS3518 has an independent 32kHz real time clock (RTC) on chip which allows a complete power down of the system CPU while only consuming less than 1µA. An internal switch automatically switches between the RTC backup-battery and main battery supply.

The single supply voltage may vary from 1.0V to 5.5V. For operations below 3.0V the integrated step-up converter is used to generate a 3V supply rail.

2 Key Features

2.1 Audio

- Audio power consumption:
  - 17mW: 95dB DAC to Headphone @ 2.9V, 32Ω
- Sigma Delta Converters
  - DAC:
    - 95dB SNR (‘A’ weighted) @ 2.9V
  - ADC:
    - 92dB SNR (‘A’ weighted) @ 2.9V
  - Sampling Frequency:
    - DAC: 8-48kHz
    - ADC: 8-48kHz
- 1 Microphone Input
  - 3 gain pre-setting (28dB/34dB/40dB) and AGC
  - 32 gain steps @1.5dB and MUTE
  - supply for electret microphone
  - microphone detection
  - remote control by switch
- 3 Line Inputs
  - volume control via serial interface
  - 32 steps @1.5dB and MUTE
  - stereo or 2x mono or mono differential
- Audio Mixer
  - 8 channel input/output mixer with AGC
  - mixes line inputs and microphones with DAC
  - left and right channels independent
- Line Output
  - volume control via serial interface
  - 32 steps @1.5dB and MUTE
  - 1Vp @10kΩ
  - Stereo 2*5mW to 16ohm
  - Differential 10mW to 32ohm (earpiece)
- High Efficiency Headphone Amplifier
  - volume control via serial interface
  - 32 steps @1.5dB and MUTE
  - 2x60mW @16Ω driver capability@ 2.9V supply
  - THD -72dB @32Ω; 2.9V
  - headphone and over-current detection
  - phantom ground eliminates large capacitors

2.2 Power Management

- Voltage Generation
  - step up for system supply (3.0-3.6V, 150mA)
  - step down for CPU core (0.65V-3.4V, 250mA)
  - step down for peripheral (0.65V-3.4V, 250mA)
  - LDO1 for AFE supply (2.9V, 100mA)
  - LDO2 for AFE supply (2.9V, 100mA)
  - LDO3 for peripherals (1.2V-3.5V, 100/200mA)
  - LDO4 for peripherals (1.2V-3.5V, 100/200mA)
  - VBUS comparator
  - separate input for LDO3
  - power supply supervision
  - hibernation modes
  - 5sec and 10sec emergency shut-down
- Backlight Driver
  - step up for backlight (15V (25V))
  - current control mode (1.2-36mA)
  - voltage control mode
  - 1 current sink
  - automatic dimming
  - over-voltage protection
- Battery Charger
  - automatic trickle charge (55mA)
  - prog. constant current charging (55-460mA)
  - prog. constant voltage charging (3.9V-4.25V)
  - current limitation for USB mode

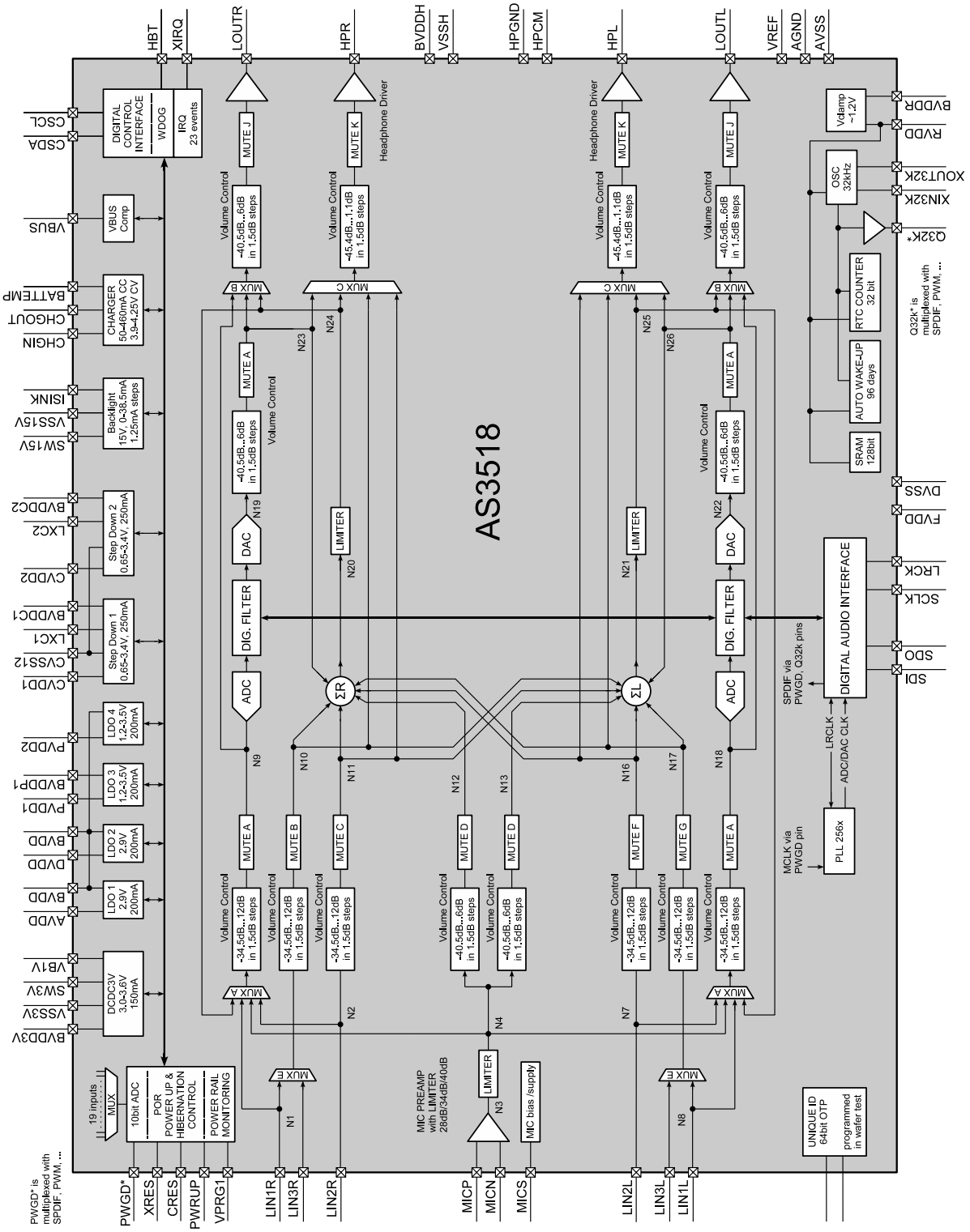
2.3 General

- Supervisor
  - automatic battery monitoring with interrupt generation and selectable warning level
  - automatic temperature monitoring with interrupt generation and selectable warning and shutdown levels
- Real Time Clock
  - ultra low power 32kHz oscillator
  - 32bit RTC sec counter, 96 days auto wake-up
  - selectable alarm (seconds or minutes)
  - 128bit free SRAM for random settings
  - 32kHz clock output to peripheral
  - voltage generation
  - trim able oscillator
  - <1uA total power consumption
- General Purpose ADC
  - 10bit resolution
  - 19 inputs analog multiplexer
- Interfaces
  - 2 wire serial control interface
  - reset pin with selectable delay, power good pin
  - 64bit unique ID (OTP)
  - 25 different interrupts
- Package CTBGA64 [7x7x1.1mm] 0.8mm pitch

3 Applications

Portable Digital Audio/Video Player and Recorder
PDA, Smartphone

Figure 1 AS3518 Block Diagram



Contents

Revision History

Revision	Date	Owner	Description
1.0	5.10.2007	pkm	changed chip version to V22, in system register and ordering information
			changed PVDD1 start-up voltage to 3.3V
			added audio block typical current consumptions
			extended features description
			added PMOS description for DCDC3V
			extended ordering information for tray delivery
			updated application information
1.1	13.8.2007	pkm	changed chip version to V23, in system register and ordering information

4 Pinout

4.1 Pin Assignment CTBGA64

Figure 2 Ball Assignment CTBGA64

	1	2	3	4	5	6	7	8	
A	SW15V	VSS3V	SW3V	BVDD3V	HPL	VSSH	HPCM	LOUTR	A
B	BVDDC1	VSS15V	VB1V	CRES	HPR	BVDDH	HPGND	LOUTL	B
C	LXC1	CVDD1	ISINK	VBUS	LIN1R	MICS	MICP	MICN	C
D	CVSS12	HBT	Q32K	PWGD	LIN1L	LIN2R	LIN3R	AGND	D
E	LXC2	CVDD2	XIRQ	LRCK	SDI	LIN2L	LIN3L	VREF	E
F	BVDDC2	BVDD	BVDDP1	SCLK	SDO	VPRG1	AVDD	AVSS	F
G	PVDD2	PVDD1	BATTEMP	DVDD	CSDA	XRES	RVDD	BVDDR	G
H	CHGOUT	CHGIN	DVSS	FVDD	CSCL	PWRUP	XIN32K	XOUT32K	H
	1	2	3	4	5	6	7	8	

4.2 Pin Description CTBGA64

Table 1 Pinlist CTBGA64

Ball	PinName	Type	Function
D8	AGND	Analog I/O	Analog Reference Voltage (AVDD/2) buffer cap terminal
F7	AVDD	Supply	Analog Circuit VDD, connected to LDO1 on BGA substrate
F8	AVSS	Supply	Analog Circuit VSS
G3	BATTEMP	Analog I/O	Charger Battery Temperature Sensor input (100kΩ NTC)
A4	BVDD3V	Supply	Positive (Battery) Supply Terminal, 5.5V max.
F2	BVDD	Supply	Positive (Battery) Supply Terminal, 5.5V max.
B6	BVDDH	Supply	Positive (Battery) Supply Terminal of HP Amplifier, 5.5V max.
B1	BVDDC1	Supply	Positive (Battery) Supply Terminal of DCDC1, 5.5V max.
F1	BVDDC2	Supply	Positive (Battery) Supply Terminal of DCDC2, 5.5V max.
F3	BVDDP1	Supply	Positive (Battery) Supply Terminal of LDO3, 5.5V max.
G8	BVDDR	Supply	RTC Positive (Battery) Supply terminal, 5.5V max
H2	CHGIN	Analog Input	Charger Positive Supply Terminal, 5.5V max
H1	CHGOUT	Analog Output	Charger Output prog. for Ichg 50-480mA or Vchg 3.9-4.25V
B4	CRES	Analog I/O	Capacitor input for setting detect delay
H5	CSCL	Digital input with pull up	Clock Input of two wire interface
G5	CSDA	Digital I/O with pull up	Data I/O of two wire interface
C2	CVDD1	Analog Input	CVDD1 and Feedback pin
E2	CVDD2	Analog Input	CVDD2 and Feedback Pin
D1	CVSS12	Supply	CVDD1+2 StepDown Neg. Supply terminal
G4	DVDD	Supply	Digital Circuit VDD, connected to LDO2 on BGA substrate
H3	DVSS	Supply	Digital Circuit VSS
H4	FVDD	Supply	ADC&DAC Digital Circuit VDD (1.8-3.6V)
D2	HBT	Digital input with pull down	Heartbeat Input for CPU supervision
A7	HPCM	Analog Output	Headphone Common GND Output for DC-coupled speakers
B7	HPGND	Analog I/O	Headphone Amplifier reference buffer cap terminal
A5	HPL	Analog Output	Headphone Amplifier Output Left Channel
B5	HPR	Analog Output	Headphone Amplifier Output Right Channel
C3	ISINK	Analog Output	DCDC15V Load Current Sink terminal (e.g. white LED)
D5	LIN1L	Analog Input	Line Input 1 Left Channel
C5	LIN1R	Analog Input	Line Input 1 Right Channel
E6	LIN2L	Analog Input	Line Input 2 Left Channel
D6	LIN2R	Analog Input	Line Input 2 Right Channel
E7	LIN3L	Analog Input	Line Input 3 Left Channel
D7	LIN3R	Analog Input	Line Input 3 Right Channel
B8	LOUTL	Analog Output	Line Output Left Channel
A8	LOUTR	Analog Output	Line Output Right Channel
E4	LRCLK	Digital input with pull down	I2S Left/Right Clock
C1	LXC1	Digital output	CVDD1 StepDown switch output to coil
E1	LXC2	Digital output	CVDD2 StepDown switch output to coil
C8	MICN	Analog Input	Microphone Input N
C7	MICP	Analog Input	Microphone Input P
C6	MICS	Analog I/O	Microphone Supply (2.95V) / Remote Input
G2	PVDD1	Analog Output	LDO3 Regulator Output
G1	PVDD2	Analog Output	LDO4 Regulator Output
D4	PWGD	Digital I/O multiplexed	Power Good, SPDIF, PLL clock, PWM digital output. Configurable as open drain or push pull. Master CLK digital input (e.g. from CPU)
H6	PWRUP	Digital input with pull down	Power Up input
D3	Q32K	Digital output multiplexed	32kHz Clock output, SPDIF, PLL clock, PWM. Configurable as

Ball	PinName	Type	Function
			open drain or push pull.
G7	RVDD	Analog Output	RTC Supply Regulator Output prog. to 1.0-2.5V
F4	SCLK	Digital input with pull down	I2S Shift Clock
E5	SDI	Digital input with pull down	I2S Data Input to DAC
F5	SDO	Digital output	I2S Data output from ADC
A1	SW15V	Analog Output	DCDC15V switch terminal
A3	SW3V	Aout	DCDC3V Switch terminal
B3	VB1V	Supply	Battery supply input for single cell application
F6	VPRG1	Analog Input	5 State Prog Input to define power up sequence
E8	VREF	Analog I/O	Analog Reference (filtered AVDD) decoupling cap terminal
C4	VBUS	Analog I/O	USB supply terminal for supervision
B2	VSS15V	Supply	DCDC15V Neg. Supply terminal
A2	VSS3V	Supply	DCDC3V Neg. Supply terminal
A6	VSSH	Supply	Headphone Amplifier Neg. Supply terminal
H7	XIN32K	Analog I/O	32kHz RTC Oscillator Crystal terminal
E3	XIRQ	Digital output	Interrupt Request Output. Configurable as open drain or push pull, active high or active low
H8	XOUT32K	Analog I/O	32kHz RTC Oscillator Crystal terminal
G6	XRES	Digital output open drain	Reset Output

5 Absolute Maximum Ratings (Non-Operating)

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Electrical Characteristics” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comments
V_{IN_VB1V}	single cell supply voltage	-0.5	5.0	V	Applicable for pin VB1V
V_{IN_5V}	5V pins	-0.5	7.0	V	Applicable for pins BVDD, BVDDH, BVDDC1, BVDDC2, BVDDR, BVDDP1, CHGIN, CHGOUT, VBUS
V_{IN_3V}	3V pins	-0.5	5.0	V	Applicable for pin FVDD
V_{IN_SW15}	15V pin	-0.5	17	V	Applicable for pin SW15V
V_{IN_VSS}	Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins CVSS15V, CVSS12, VSSH, AVSS, DVSS
V_{IN_DVDD}	3.3V pins with diode to DVDD	-0.5	5.0 DVDD+0.5	V	Applicable for pins LRCK, SCLK, SDI, VPRG1, BATTEMP, XIRQ, XRES, PWGD, Q32K, HBT
V_{IN_xDVDD}	pins with no diode to DVDD	-0.5	7.0V	V	Applicable for pins CSCL, CSDA, PWRUP
V_{IN_AVDD}	3.3V pins with diode to AVDD	-0.5	5.0 AVDD+0.5	V	Applicable for pins HPCM, HPGND, LOUTL/R, VREF, AGND, LIN1L/R, LIN2L/R, LIN3L/R, MICP/N, MICS
V_{IN_REG}	voltage regulator pins with diodes to BVDD	-0.5	5.0 BVDD+0.5	V	Applicable for pins AVDD, DVDD, PVDD1/2, CVDD1/2
V_{IN_RVDD}	3.3V pins with diode to RVDD	-0.5	5.0 RVDD+0.5	V	Applicable for pins XIN32K, XOUT32K
V_{IN_BVDD}	pins with diode to BVDD	-0.5	7.0 BVDD+0.5	V	Applicable for pins HPR/L, SW3, ISINK, RVDD
I_{scr}	Input Current (latchup immunity)	-100	100	mA	Norm: JEDEC 17
ESD	Electrostatic Discharge HBM		+/-1	kV	Norm: JEDEC JESD22-A114C
P_t	Total Power Dissipation (all supplies and outputs)		640	mW	Valid for CTBGA64 package
H	Humidity non-condensing	5	85	%	

Table 3 Soldering Conditions

Symbol	Parameter	Min	Max	Unit	Comments
T_{body}	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
T_{peak}	Solder Profile*	235	245	°C	
D_{well}		30	45	s	above 217 °C
MSL	Moisture Sensitive Level	3		1	Represents a max. floor live time of 168h

* austriamicrosystems AG strongly recommends to use underfill.

6 Electrical Characteristics

6.1 General Parameter

Table 4 Operating conditions for supply voltages

Symbol	Parameter	Contition	Min	Typ	Max	Unit
VB1V	DCDC Supply Voltage		1.0	1.5	3.6	V
BVDDx	Battery Supply Voltage BVDD, BVDDH, BVDDC1, BVDDC2, BVDDP1		3.0	3.6	5.5	V
BVDDR	RTC Supply Voltage		1.35	3.6	5.5	V
FVDD	Filter Supply Voltage		1.8		3.6	V
VBUS	USB VBUS Voltage			5.0	5.5	V
CHGIN	Charger Supply Voltage		4.5		5.5	V
DVDD	Digital Supply Voltage	Digital Audio Supply Voltage (LDO2)	2.8	2.9	3.6	V
AVDD	Analogue Supply Voltage	Analog Audio Supply Voltage (LDO1)	2.8	2.9	3.6	V
AGND	Analogue Ground Voltage	Internally generated		AVDD/2		
V_{DELTA-}	Difference of Negative Supplies VSS3V, VSS15V, VSSH, AVSS, DVSS	To achieve good performance, the negative supply terminals should be connected to low impedance ground plane.	-0.1		0.1	V
V_{DELTA+}	Difference of Positive Supplies	AVDD-DVDD	-0.25		0.25	V

Table 5 Electrical Specification of other function blocks

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{POR_ON}	Power-on Reset Activation Level	Power-on Reset activation level when DVDD decreases		2.15		V
V_{POR_OFF}	Power-on Reset Release Level	Power-on Reset release when DVDD increases		2.0		V
V_{POR_HY}	Power-on Hysteresis			100		mV
f_{LRCLK_WD}	LRCLK Watchdog		2	4.1	8	kHz
t_{ON_DELAY}	Delay Time of pin PWRUP	Minimum key press time		80		ms
V_{DO_DL}	Digital Output Driver Capability (drive LOW)	Pins XRES, XIRQ, PWGD @ 8mA, SDO			0.3	V
V_{DO_DH}	Digital Output Driver Capability (drive HIGH)	Pins XRES, XIRQ @ 8mA, push/pull mode only, SDO	2.6			V
I_{PU}	Internal Pull-up Current Source	Pins XRES, XIRQ, PWGD, Q32K; @0V	6	10	18	µA
V_{PWRUP_L}	Input Level LOW,	Pin PWRUP, BVDD>3V			0.5	V
V_{PWRUP_H}	Input Level HIGH	Pin PWRUP, BVDD>3V	BVVD/ 3			V
		Pin PWRUP, BVDD<=3V	1			V
R_{PWRUP}	Internal Pull-down Current Source	Pin PWRUP; @2.9V	2.5	7	19	uA
V_{DI_L}	Digital Input Level LOW	Pin HBT, SDI, SCLK, MCLK, LRCK		DVDD /2*0.3	0.42	V
V_{DI_H}	Digital Input Level HIGH	Pin HBT, SDI, SCLK, MCLK, LRCK	1.02	DVDD /2*0.7		V
I_{PD}	Internal Pull-down current source	Pin HBT; @2.9V	7	10	30	µA
fCLK	Audio Clock Frequency	LRCK according to streamed audio data	8		48	kHz

6.2 Operating Currents

Table 6 Supply currents

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{REF}	Reference supply current	all blocks off, only LDO1 & 2 on		350		uA
I_{BIAS}	Audio Bias current			130		uA
I_{SUM}	Summing stage current			135		uA
I_{LIN}	Line input stage current	no signal		140		uA
I_{MIC}	Mic input stage current	no signal		715		uA
I_{MICS}	Mic Supply stage current	no load		215		uA
I_{LOUT}	Line output stage current	no load		450		uA
I_{DAC_GS}	DAC gain stage current	no signal		143		uA
I_{ADC_GS}	ADC gain stage current	no signal		143		uA
I_{HPH}	Headphone stage current	no load		1.65		mA
		Bias reduction on, no load		1.12		
		CM buffer off, no load		1.12		
		Bias reduction on, CM buffer off, no load		0.77		
I_{DAC}	DAC supply current	LRCK=48kHz		4.25		mA
		LRCK=44.1kHz		4.24		
		LRCK=32kHz		3.77		
		LRCK=16kHz		3.17		
		LRCK=8kHz		2.88		
I_{ADC}	ADC supply current	LRCK=48kHz, mono		4.24		mA
		LRCK=48kHz, stereo		6.77		
		LRCK=44.1kHz		6.50		
		LRCK=32kHz		5.64		
		LRCK=16kHz		4.52		
		LRCK=8kHz		3.96		
$I_{DAC->HP}$	DAC playback current	no load, 44.1kHz, including PMU		6.1		mA
$I_{Line->HP}$	Line Input playback current	no load, including PMU		1.7		mA
I_{RTC}	RTC supply current			650		nA

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

6.3 Temperature Range

Table 7 Temperature Range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	Operating temperature range		-20	25	85	°C
T_j	Junction temperature range		0		110	°C
R_{th}	Thermal Resistance	For CTBGA64 package		39		°C/W

6.4 Audio Specification

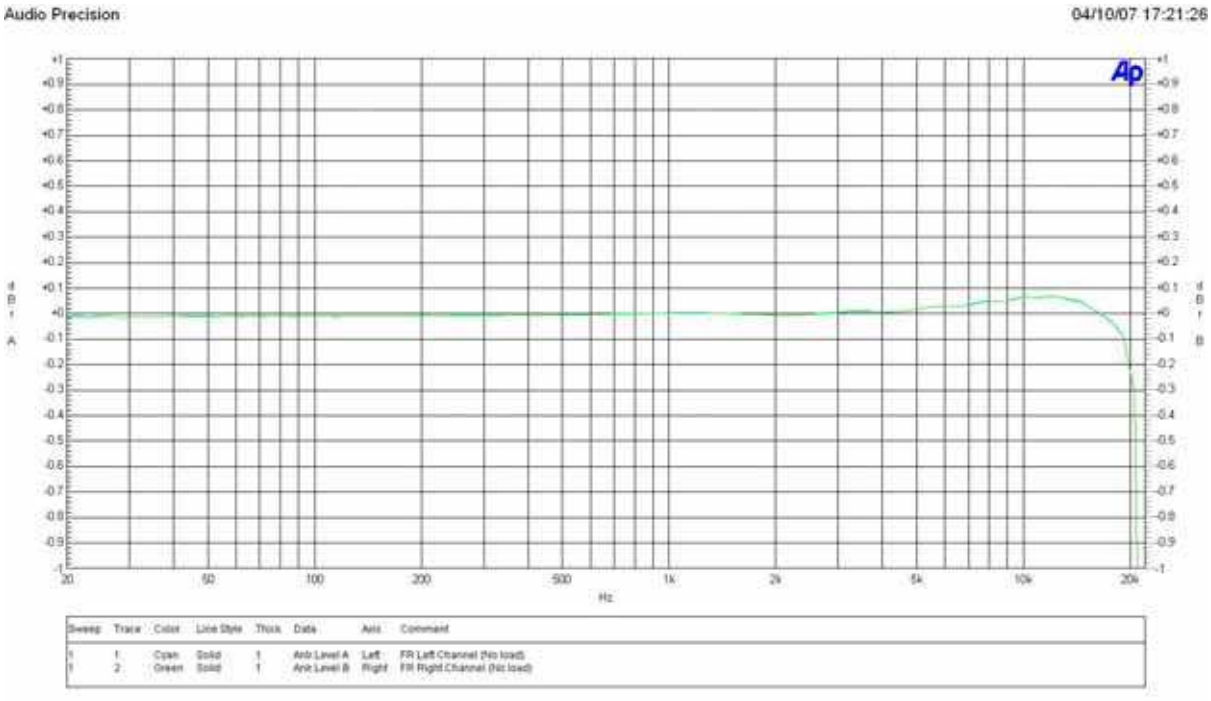
Table 8 Audio Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DAC Input to Line Output						
FS	Full Scale Output	1kHz FS input		0.85		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		93		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS 1kHz input		91		dB
THD	Total Harmonic Distortion	1kHz -1dB FS input		-90		dB
Line Input to Line Output						
FS	Full Scale Output	1kHz $1V_{RMS}$ (-3dB FS) input		0.88		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		92		dB
THD	Total Harmonic Distortion	1kHz $1V_{RMS}$ (-3dB FS) input		-92		dB
CS	Channel Separation			90		dB
DAC Input to HP Output						
FS	Full Scale Output	R_L= 32Ω		0.79		V_{RMS}
		R_L= 16Ω		0.78		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		95		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS 1kHz input		93		dB
THD	Total Harmonic Distortion	no load, 1kHz FS input		-91		dB
		Pout=20mW, R_L= 32Ω, f=1kHz -1dB FS input		-72		dB
		Pout=40mW, R_L= 16Ω, f=1kHz -1dB FS input		-68	-60	dB
CS	Channel Separation	R_L = 32Ω		75		dB
		R_L = 16Ω		60		dB
Line Input to HP Output						
FS	Full Scale Output	R_L= 32Ω, 1kHz $1V_{RMS}$(FS) input		0.84		V_{RMS}
		R_L= 16Ω, 1kHz $1V_{RMS}$ (FS) input		0.83		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		96		dB
THD	Total Harmonic Distortion	no load, 1kHz $1V_{RMS\ input}$		-92		dB
		Pout=20mW, R=32Ω, 1kHz $1V_{RMS}$ (FS) input		-75		dB
		Pout=40mW, R=16Ω, 1kHz $1V_{RMS}$ (-3dB FS) input		-70	-60	dB
CS	Channel Separation	R_L = 32Ω		77		dB
		R_L = 16Ω		71		dB
MIC Input to Line Output						
FS	Full Scale Output	1kHz FS input		0.93		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		84		dB
THD	Total Harmonic Distortion	1kHz 27mV_{RMS} (-3dB FS) input		-83		dB
Line Input to ADC Output						
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		94		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS 1kHz input		92		dB
THD	Total Harmonic Distortion	1kHz $1V_{RMS}$ (-3dB FS) input		-70		dB

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

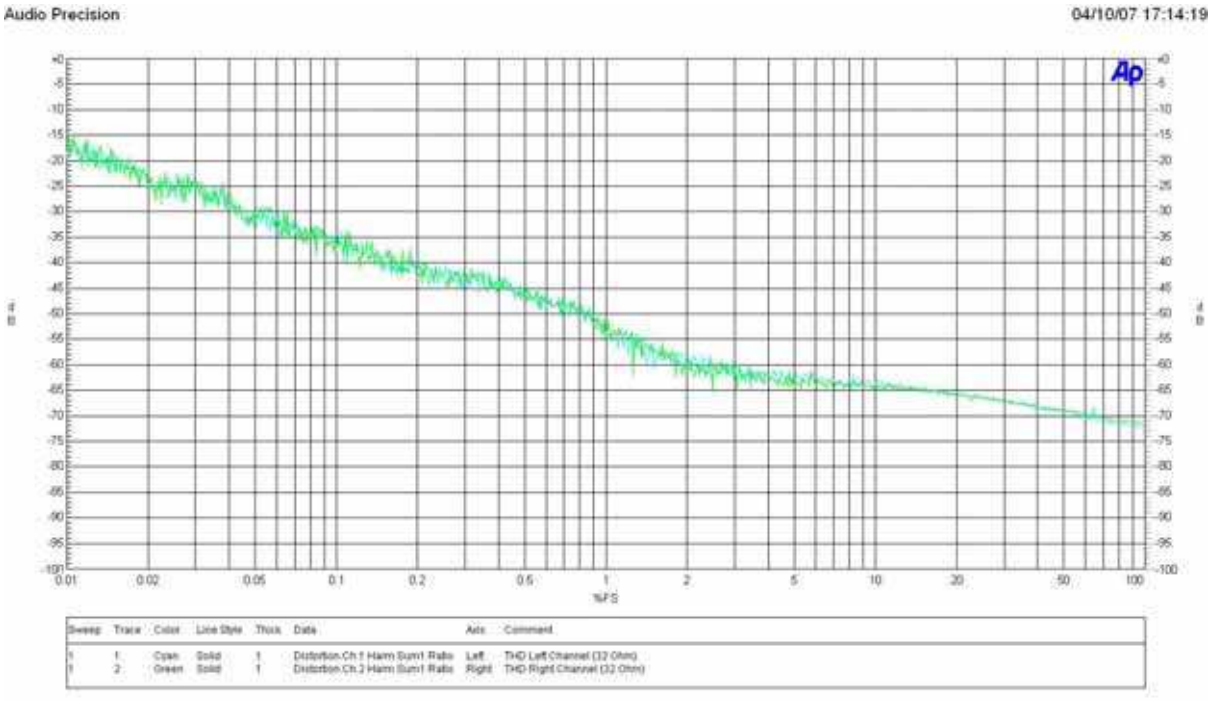
7 Typical Operating Characteristics

Figure 3 Typical Frequency Response



DAC to HP output, no load

Figure 4 Typical THD



DAC to HP output, 32Ohm load

8 Detailed Description

8.1 Audio Functions

8.1.1 Audio Line Inputs (3x)

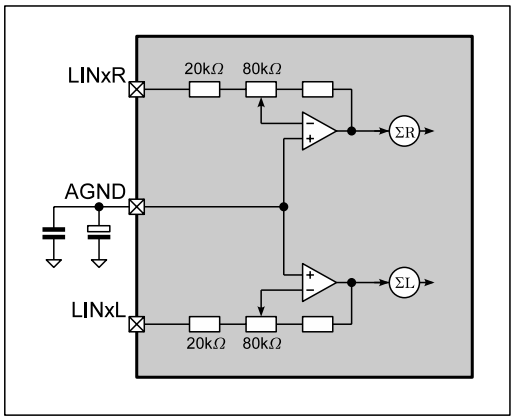
General

The chip features two identical line inputs. The blocks can work in mono differential, 2x mono single ended or in stereo single ended mode. An additional third line input features a stereo single ended mode only.

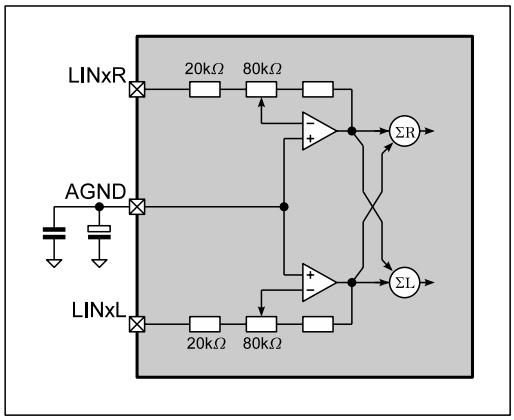
The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each and MUTE. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the line input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Line Input 3 has no dedicated gain stage but is multiplexed with Line input 1 for playback.

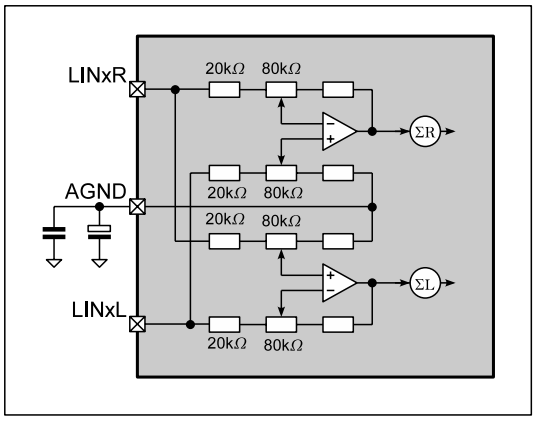
Figure 5 Line Inputs



Stereo Mode



Mono Single Ended Mode (not supported for LineIn 3)



Mono Differential Mode (not supported for LineIn 3)

Parameter

Table 9 Line Input Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LIN}	Input Signal Level	Pls observe gain settings. Max. peak levels at any node within the circuit shall not exceed AVDD		1.0		V_{PEAK}
R_{LIN}	Input Impedance	depending on gain setting		20-100		kΩ
Δ_{RLIN}	Input Impedance Tolerance			±30		%
C_{LIN}	Input Capacitance			5		pF
A_{LIN}	Programmable Gain		-34.5		+12	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Accuracy			±0.25		dB
$A_{LINMUTE}$	Mute Attenuation			100		dB

BVDD = 3.3V, T_A= 25°C, fs=48kHz unless otherwise mentioned

Register Description

Table 10 Line Input Related Register

Name	Base	Offset	Description
LINE_IN1_R	2-wire serial	0Ah	Right Line Input 1 settings, Line Input 3 selection
LINE_IN1_L	2-wire serial	0Bh	Left Line Input 1 settings
LINE_IN2_R	2-wire serial	0Ch	Right Line Input 2 settings
LINE_IN2_L	2-wire serial	0Dh	Left Line Input 2 settings
AudioSet_1	2-wire serial	14h	Enable/disable driver stage
AudioSet_3	2-wire serial	16h	Enable/disable mixer input

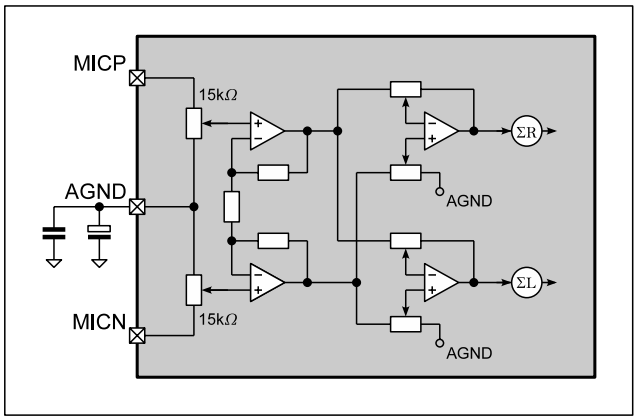
Line inputs have to be enabled in register 14h first before other settings in register 0Ah to 0Dh can be programmed.

8.1.2 Microphone Input

General

The AFE offers one microphone input and one low noise microphone voltage supply (microphone bias), voice activation, microphone connect detection and push button remote control.

Figure 6 Microphone Input



Microphone Preamplifier and Gain Stage

Gain Stage & Limiter

The integrated pre-amplifier allows 3 preset gain settings. There is also a limiter which attenuates high input signals from e.g. electret microphones signal to 1Vp. The AGC has 15 steps with a dynamic range of about 29dB. The AGC is ON by default but can be disabled by a microphone register bit.

Apart from the microphone pre-amplifier the microphone input signal can further be amplified with 32 @1.5dB programmable logarithmic gain steps and MUTE. All gains and MUTE are independently programmable. The gain can be set from –40.5dB to +6dB.

The stage is set to mute by default. If the microphone input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Supply & Detection

Each microphone input generates a supply voltage of 1.5V above HPCM. The supply is designed for ≤2mA and has a 10mA current limit. In OFF mode the MICS terminal is pulled to AVDD with 30kOhm. A current of typically 50uA generates an interrupt to inform the CPU, that a circuit is connected. When using HPCM as headset ground the HP–stage gives the interrupt. After enabling the HP-stage through the CPU the microphone detection interrupt will follow.

When using the MICS terminal as ADC-10 input to monitor external voltages the 30kOhm pull-up can be disabled.

Remote Control

Fast changes of the supply current of typically 500uA are detected as a remote button press, and an interrupt is generated. Then the CPU can start the measurement of the microphone supply current with the internal 10-bit ADC to distinguish which button was pressed. As the current measurement is done via an internal resistor, only two buttons generating a current of about 0.5mA and 1mA can be detected. With this 1mA as microphone bias is still available.

Voice Activation

Further a built-in voice activation comparator can actuate an interrupt if microphone input voltage of about 5mVRMS is detected.

Parameter

Table 11 Microphone Input Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{MICIN}0$	Input Signal Level	A_{MICPRE} = 28dB; AMIC = 0dB		40		mV_P
$V_{MICIN}1$		A_{MICPRE} = 34dB; AMIC = 0dB		20		mV_P
$V_{MICIN}2$		A_{MICPRE} = 40dB; AMIC = 0dB		10		mV_P
R_{MICIN}	Input Impedance	MICP, MICN to AGND		15		kΩ
Δ_{MICIN}	Input Impedance Tolerance			±15		%
C_{MICIN}	Input Capacitance			5		pF
A_{MICPRE}	Microphone Preamplifier Gain	Preamplifier has 3 selectable (fixed) gain settings		28 34 40		dB dB dB
A_{MIC}	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Precision			±0.25		dB
$V_{MICLIMIT}$	Limiter Activation Level			1		V_{PEAK}
$A_{MICLIMIT}$	Limiter Gain Overdrive			15*2		dB
t_{ATTACK}	Limiter Attack Time			50		µs/6dB
t_{DECAY}	Limiter Decay Time			120		ms/6dB
$A_{MICMUTE}$	Mute Attenuation			100		dB
V_{MICSUP}	Microphone Supply Voltage			2.9		V
I_{MICMAX}	Max. Microphone Supply Current	microphones nominally need a bias current of 0.5mA-1mA		10		mA
V_{NOISE}	Microphone Supply Voltage Noise			5		µV
I_{MICDET}	Microphone Detection Current			50		µA
I_{REMDET}	Max. Remote Detection Current			500		µA

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

Register Description

Table 12 Microphone Related Register

Name	Base	Offset	Description
MIC_R	2-wire serial	06h	Right Microphone Input volume settings, AGC control
MIC_L	2-wire serial	07h	Left Microphone Input volume settings, MIC supply control
AudioSet_1	2-wire serial	14h	Enable/disable driver stage
AudioSet_3	2-wire serial	16h	Enable/disable mixer input
IRQ_ENRD_1	2-wire serial	24h	Interrupt settings for microphone voice activation
IRQ_ENRD_3	2-wire serial	26h	Interrupt settings for microphone detection
IRQ_ENRD_4	2-wire serial	27h	Interrupt settings for remote button press detection

Microphone input has to be enabled in register 14h first before other settings in register 06h and 07h can be programmed.

8.1.3 Line Output

General

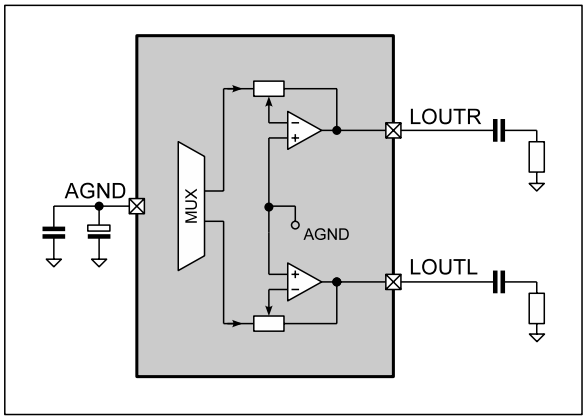
The line output is designed to provide the audio signal with typical $1V_{PEAK}$ at a load of minimum 10kΩ, which is a minimum value for line inputs. If the limiters (N20/N21) are deactivated the peak output voltage is $1.45V_{PEAK}$. The load however can decrease to 64Ohm. In addition these line output can be configured as mono differential to drive 10mW @ 32Ω load (e.g. an earpiece of a mobile phone).

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB. A zero cross detection allows to control the actual execution of new gain settings.

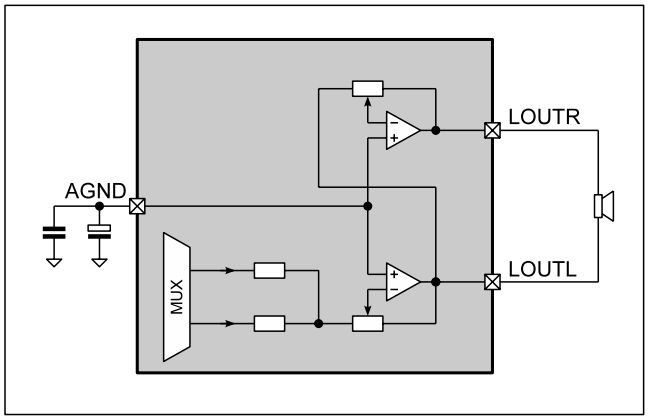
If the line output is not enabled, the volume settings are set to their default values. Changing of volume and mute control can only be done after enabling the output.

If using the output in mono differential mode, the volume setting for the right channel should be set to 0dB.

Figure 7 Line Output



Stereo Mode



Mono Differential Mode (please observe that gain of right channel amplifier has to best to 0dB)

Parameter

Table 13 Line Output Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{L_LO}	Load Impedance (Stereo Mode)	line inputs nominally have 10kΩ	64			Ω
C_{L_LO}	Load Capacitance (Stereo Mode)				100	pF
A_{LO}	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Accuracy			±0.25		dB
A_{LOMUTE}	Mute Attenuation			100		dB

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

Register Description

Table 14 Line Output Related Register

Name	Base	Offset	Description
LINE_OUT_R	2-wire serial	00h	Right Line Output volume settings, MUX control
LINE_OUT_L	2-wire serial	01h	Left Line Output volume settings
AudioSet_1	2-wire serial	14h	Enable/disable driver stage
AudioSet_3	2-wire serial	16h	Enable/disable mixer input

Line output has to be enabled in register 14h first before other settings in register 00h and 01h can be programmed.

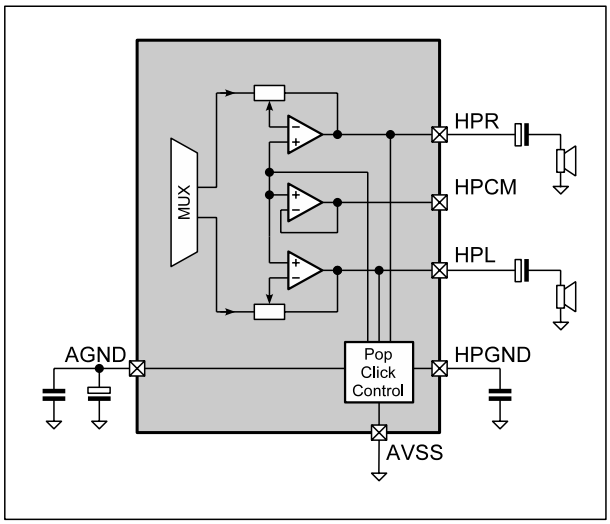
8.1.4 Headphone Output

General

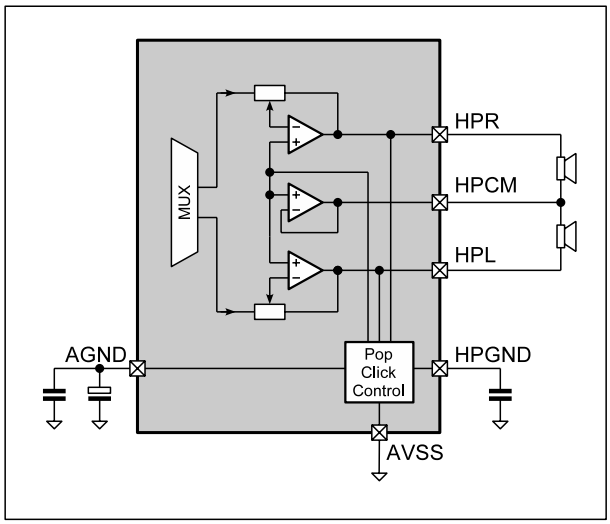
The headphone output is designed to provide the audio signal with 2x40mW @ 16Ω or 2x20mW @32Ω, which are typical values for headphones. If the limiters (N20/N21) are disabled a maximum output of 2x60mW@16Ω or 2x30mW@32Ω can be achieved.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –43.43dB to +1.07dB. A zero cross detection allows to control the actual execution of new gain settings.

Figure 8 Headphone Output



Headphones connected via decoupling capacitors



Headphones connected to Phantom Ground (Common Mode)

Phantom Ground

There are 2 ways to connect a headphone to the AFE. In order to spare the bulky ac/dc decoupling capacitors at pins HPR/HPL a buffered ground (Phantom Ground) is provided. This Common Mode Buffer needs to be switched on if utilized. If form factor considerations are less stringent, the headphones can be conventionally connected via 2x100µF capacitors.

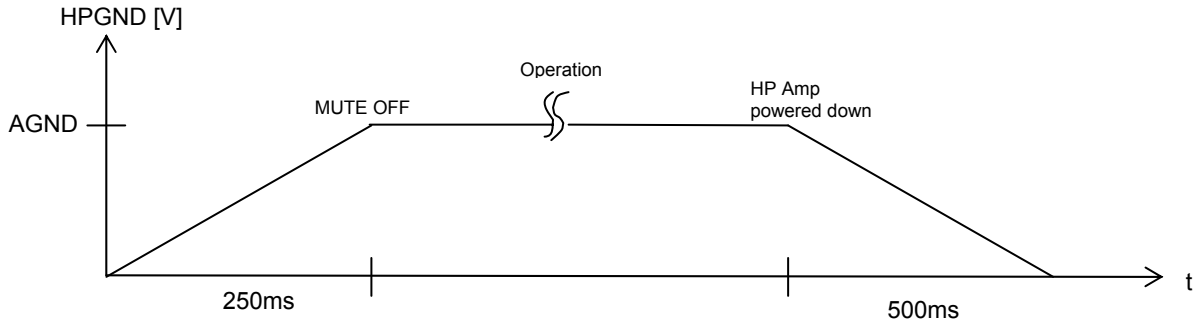
No-Pop Function

The output is automatically set to mute when the output stage is disabled.

To avoid Pop-Click noise during power-up and shut-down of the headphone amplifier, a charge/discharge control of HPGND (0V-1.45V-0V) at pins HPR/HPL is incorporated into the AFE. The 470nF capacitor at pin HPGND is used to form the charge/discharge slope. Pls observe that pin HPGND is a high impedance node which must not be connected to any other external device than the 470nF buffer capacitor. To avoid Pop-Click noise one has to wait for 750ms in between a power-down (switch-off) and a power-up (switch-on) of the headphone amplifier.

The output is automatically set to mute when the output stage is disabled.

Figure 9 HP POP-Click Suppression



Over-current Protection

The headphone amplifier has an over-current protection (e.g. HPR/HPL is shorted). This over-current protection will power down the headphone amplifier for a programmable timeout period (256ms, 0ms). The current threshold is at 150mA for HPR/HPL and 300mA for HPCM. There is a corresponding interrupt available to be enabled.

Headphone Detection

When the headphone amplifier is powered down, one can detect the connection of a headset. It only work if the headset is connected between pins HPR/HPL and HPCM. As long as the headphone amplifier is powered down, HPCM is biased to 150mV and acting as the sense pin. There is a corresponding interrupt available to be enabled.

Power Options

To save power, especially when driving 32 Ohm loads, a reduction of the bias current is selected, for 16Ohm loads the bias current can be increased.

Parameter

Table 15 Power Amplifier Block Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{L_HP}	Load Impedance	stereo mode	16			Ω
C_{L_LO}	Load Capacitance	stereo mode			100	pF
P_{HP}	Nominal Output Power	RL=16Ω, limiter enabled RL=32Ω, limiter enabled		40 20		mW
P_{HP_MAX}	Max. Output Power	RL=16Ω RL=32Ω		60W 30W		mW
A_{HP}	Programmable Gain		-45.5		+1	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Accuracy			±0.25		dB
	Over current limit	HPR/HPL pins HPCM pin		150 300		mA mA
P_{SRRHP}	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, RL=16Ω		90		dB
A_{HPMUTE}	Mute Attenuation			100		dB

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

Register Description

Table 16 Headphone Related Register

Name	Base	Offset	Description
HPH_OUT_R	2-wire serial	02h	Right HP Output volume and over-current settings
HPH_OUT_L	2-wire serial	03h	Left HP Output volume settings, enable and detection control
AudioSet_3	2-wire serial	16h	Power save options, common mode buffer
IRQ_ENRD_3	2-wire serial	26h	Interrupt settings for over current and HP detection

8.1.5 DAC, ADC and I2S Digital Audio Interface

Input

The AFE receives serialized audio data for the DAC via pin SDI. The output of the DAC is fed through a volume control to the mixer stage and to the multiplexers of line output and headphone amplifiers.

This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCK the alignment clock is input to the DAC digital filters. LRCK (Left Right Clock) indicates whether the serial bit-stream received via pin SDI, represents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDI and LRCK are synchronous with SCLK. SDI, LRCK and SCLK are inputs; SDO is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the DAC input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Output

This block consists of an audio multiplexer where the signal, which should be recorded, can be selected. The output is then fed through a volume control to the audio ADC. The digital output is done via an I2S interface.

The AFE sends serialized audio data from the ADC via pin SDO. This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCK the alignment clock is signalled to the connected devices (e.g. CPU). LRCLK (Left Right Clock) indicates whether the serial bit-stream sent via pin SDI, presents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDO and LRCK are synchronous with SCLK. SDO is an output; LRCK and SCK are inputs; SDI is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the ADC output is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

The I2S output uses the same clocks as the I2S input. The sampling rate therefore depends also on the input sampling rate.

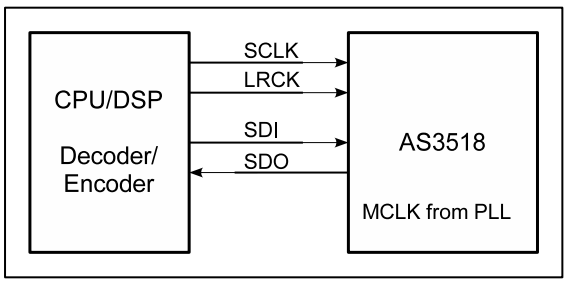
I2S Modes

The AFE can be operated either in Slave Mode or in Slave Mode with the master clock directly signalled via pin PWGD (pin PWGD is multiplexed for I2S Direct Mode). The master clock (MCLK) is the necessary internal over-sampling clock for the DAC and ADC (e.g. 256*fs, fs=audio sampling frequency)

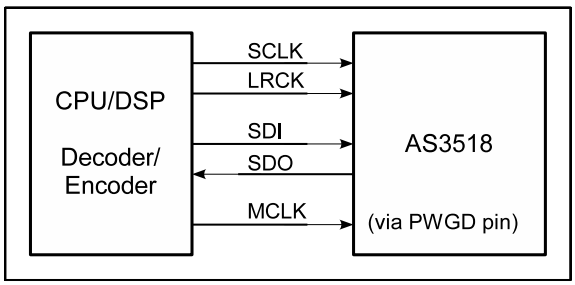
Due to the internal structure left and right audio samples are exchanged in I2S Direct Mode.

In Slave mode the PLL generates the master clock based on LRCK. Thus the PLL needs to be preset to the expected sampling frequency. The ranges are 8kS-12kS (8kHz-12kHz) and 16kS-48kS (16kHz-48kHz). Please refer to register 1Ah.

Table 17 I2S Modes



Slave Mode, internal PLL of the AS3518 generates MCLK



Slave Mode with I2S direct, the master clock is signalled via pin PWGD

Clock Supervision

The digital audio interface automatically checks the LRCK. An interrupt can be generated when the state of the LRCK input changes. A bit in the interrupt register represents the actual state (present or not present) of the LRCK.

Signal Description

The digital audio interface uses the standard I2S format:

- left justified
- MSB first
- one additional leading bit

The first 18 bits are taken for DAC conversion. The on-chip synchronization circuit allows any bit-count up 32bit. When there are less than 18 bits sampled, the data sample is completed with “0”s. In I2S direct mode the data length has to be minimum 18 bits.

The ADC output is always 20 bit. If more SCLK pulses are provided, only the first 20 will be significant. All following bits will be “0”.

SCLK has not to be necessarily synchronous to LRCK but the high going edge has to be separate from LRCK edges. The LRCK signal has to be derived from a jitter-free clock source, because the on-chip PLL is generating a clock for the digital filter, which has to be always in correct phase lock condition to the external LRCK.

Please observe that LRCK has to be activated before enabling the ADC.

Figure 10 I2S Left Justified Mode

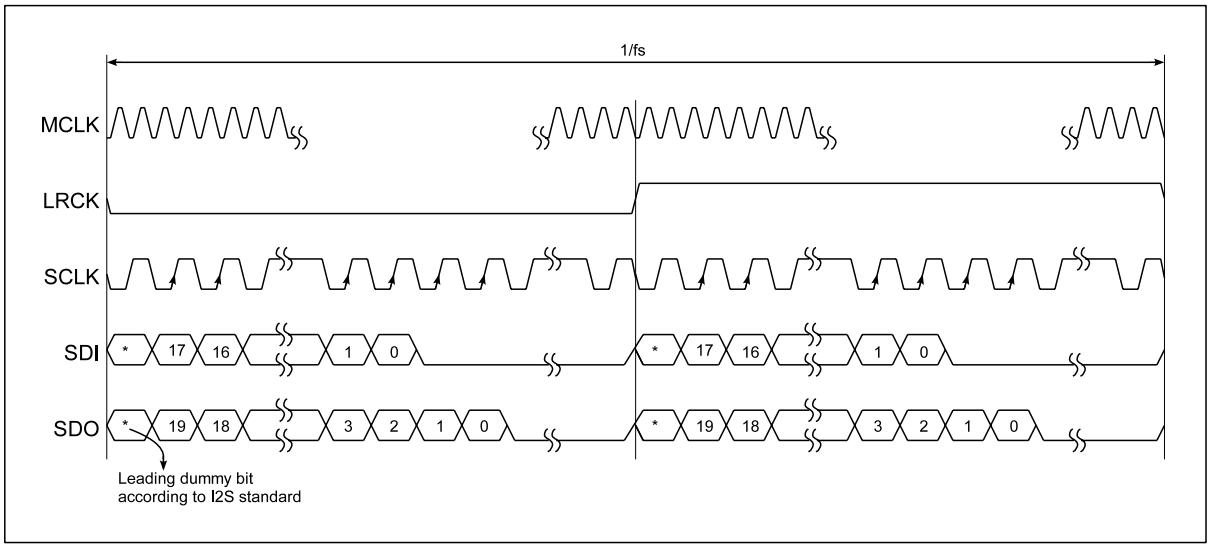
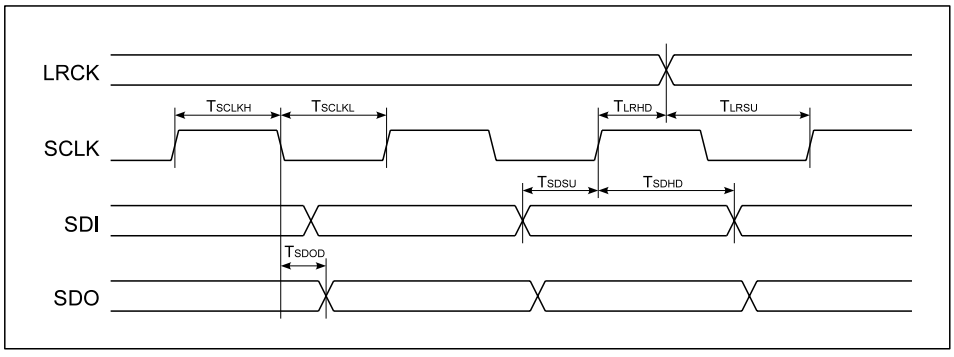


Figure 11 I2S Timing



Parameter

Table 18 I2S Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SCLK}	SCLK Cycle Time		160			ns
t_{SCLKH}	SCLK Pulse Width High		80			ns
t_{SCLKL}	SCLK Pulse Width Low		80			ns
T_{LRSU}	LRCK Setup Time before SCLK rising edge		80			ns
T_{LRHD}	LRCK Hold Time after SCLK rising edge		80			ns
t_{SDSU}	SDI setup time before SCLK rising edge		25			ns
t_{SDHD}	SDI hold time after SCLK rising edge		25			ns
t_{SDOD}	SDO Delay from SCLK falling edge				25	ns
t_{JITTER}	Jitter of LRCK	internal PLL generates MCLK from LRCK	-20		20	ns
I2S Direct mode						
T_{SCD}	SCLK delay after MCLK rising edge		0.5		1.5	ns
T_{LRD}	LRLCK delay after SCLK rising edge		0.5		1.5	ns
t_{SDSU}	SDI setup time before SCLK rising edge		5			ns
t_{SDHD}	SDI hold time after SCLK rising edge		5			ns
t_{SDOD}	SDO Delay from SCLK falling edge				15	ns

Register Description

Table 19 Audio Converter Related Register

Name	Base	Offset	Description
DAC_R	2-wire serial	0Eh	DAC input volume settings
DAC_L	2-wire serial	0Fh	DAC input volume settings
ADC_R	2-wire serial	10h	ADC output volume settings, source multiplexer settings
ADC_L	2-wire serial	11h	ADC output volume settings
MISC	2-wire serial	1Ah	I2S MCLKand PLL settings
AudioSet_1	2-wire serial	14h	Enable/disable ADC
AudioSet_2	2-wire serial	15h	Enable/disable DAC and power save options
AudioSet_3	2-wire serial	16h	Enable/disable mixer input
IRQ_ENRD_1	2-wire serial	25h	Interrupt settings for LRCK changes

DAC and ADC have to be enabled in register 14h first before other settings in register 0Eh to 11h can be programmed.

8.1.6 Audio Output Mixer

General

The mixer stage sums up the audio signals of the following stages

- Microphone Input 1
- Line Input 1/3
- Line Input 2
- Digital Audio Input (DAC)

The mixing ratios have to be set within the volume registers of the corresponding input stages. Please be sure that the input signals of the mixer stage are not higher than 1Vp. If summing up several signals, each individual signal has of course to be accordingly lower. This shall insure that the output signal is also not higher than 1Vp to get a proper signal for the output amplifier.

This stage features an automatic gain control (AGC), which automatically avoids clipping.

Register Description

Audio Mixer Related Register

Name	Base	Offset	Description
AudioSet_2	2-wire serial	15h	Enable/disable mixer stage and AGC
AudioSet_3	2-wire serial	16h	Enable/disable DAC, MIC or Line Inputs to mixer stage

8.1.7 2-Wire-Serial Control Interface

General

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr_Group8 - audio processors

- 8Ch_write
- 8Dh_read

Protocol

Table 20 2-Wire Serial Symbol Definitions

Symbol	Definition	R/W	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 1100b (8Ch)
DR	Device address for read	R	1000 1101b 8Dh)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	During acknowledge
	AS3518 (=slave) receives data		
	AS3518 (=slave) transmits data		

Figure 12 Byte Write

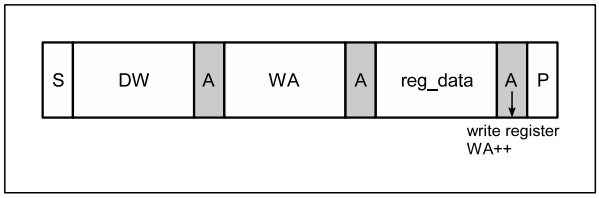
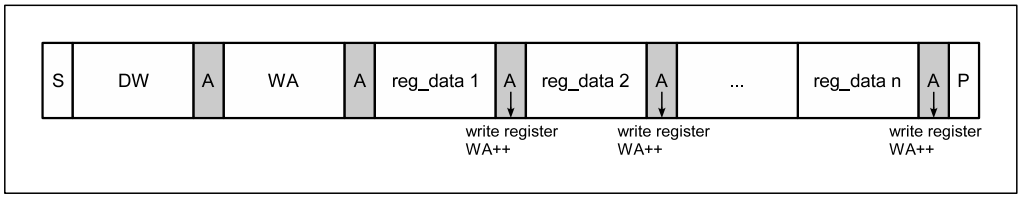


Figure 13 Page Write

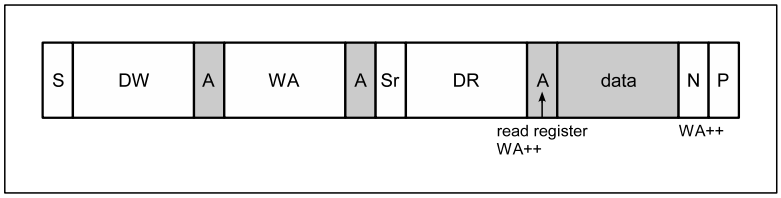


Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 14 Random Read

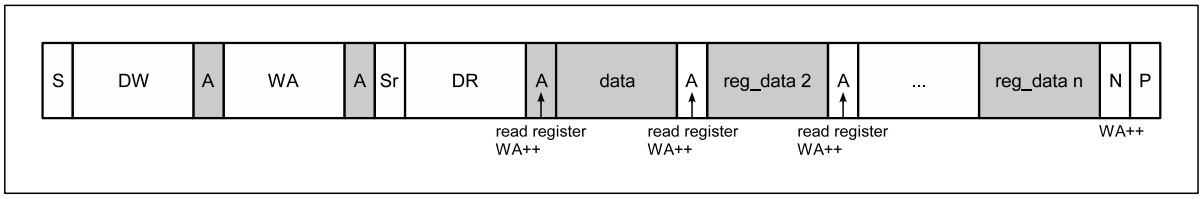


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

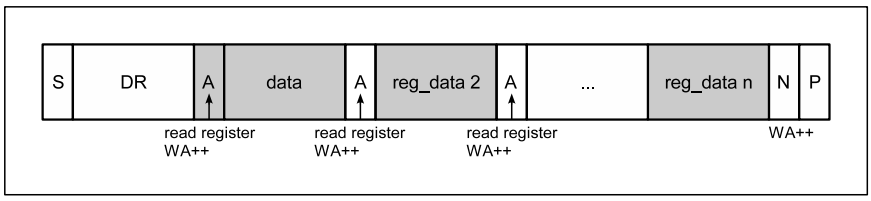
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 15 Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behaviour of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 16 Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

Parameter

Figure 17 I2C timing

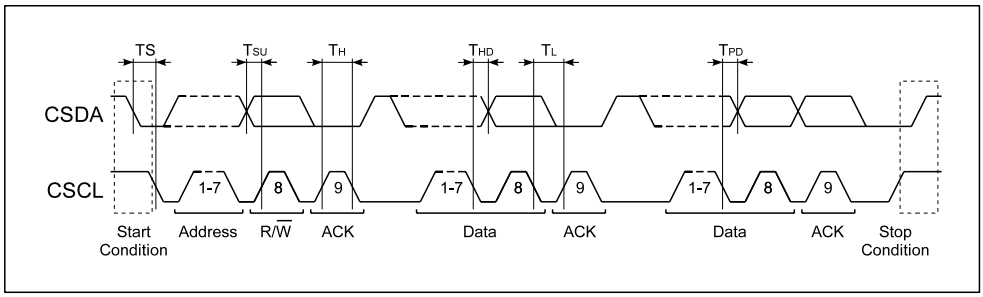


Table 21 I2C Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CSL}	CSCL, CSDA Low Input Level	(max 30%DVDD)	0	-	0.87	V
V_{CSH}	CSCL, CSDA High Input Level	CSCL, CSDA (min 70%DVDD)	2.03	-	5.5	V
HYST	CSCL, CSDA Input Hysteresis		200	450	800	mV
V_{OL}	CSDA Low Output Level	at 3mA	-	-	0.4	V
Tsp	Spike insensitivity		50	100	-	ns
T_H	Clock high time	max. 400kHz clock speed	500			ns
T_L	Clock low time	max. 400kHz clock speed	500			ns
T_{SU}		CSDA has to change Tsetup before rising edge of CSCL	250	-	-	ns
T_{HD}		No hold time needed for CSDA relative to rising edge of CSCL	0	-	-	ns
TS		CSDA H hold time relative to CSDA edge for start/stop/rep_start	200	-	-	ns
T_{PD}		CSDA prop delay relative to lowgoing edge of CSCL		50		ns

DVDD =2.9V, T_{amb}=25ºC; unless otherwise specified

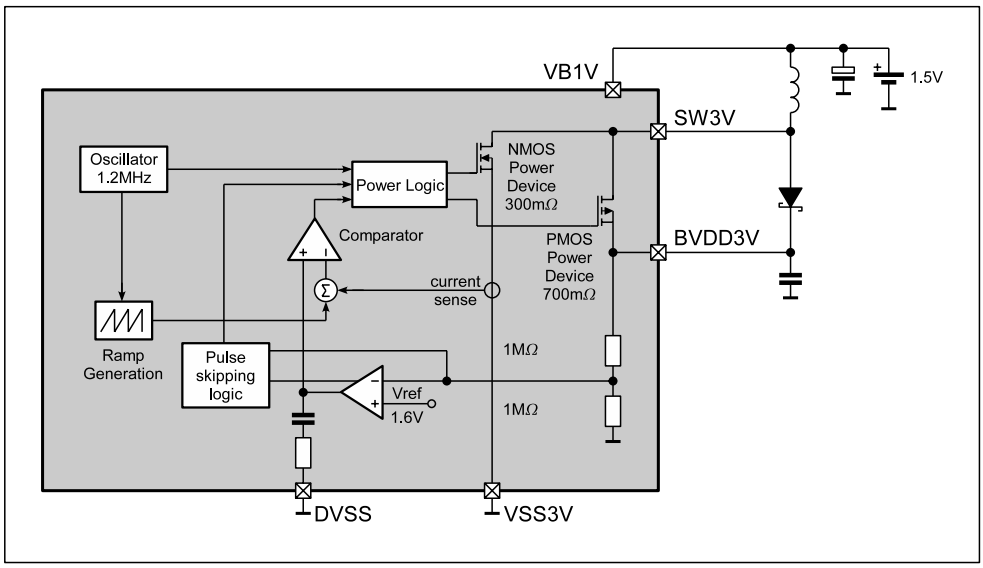
8.2 Power Management Functions

8.2.1 3V Step-Up Converter

General

- Output voltage 3V to 3.6V (BVDD) programmable in 4 steps via DCDC3p bit to save power
- Input voltage 1V (1.2V) to 3V, voltages higher than that can be connected to BVDD directly
- Maximum output current to BVDD: 150mA
- On chip 300mΩ NMOS switch
- On chip 700mΩ PMOS switch
- PWM mode with 1.2MHz switching frequency, Pulse skipping capability
- Inductor current limitation 850mA
- On-chip PMOS switch
- Low quiescent current: 40µA in PFM-mode, 300µA in PWM mode
- ≤1µA shutdown current
- uses external coil (6.8µH) and Schottky diode (500mA)

Figure 18 DCDC 3V Block Diagram



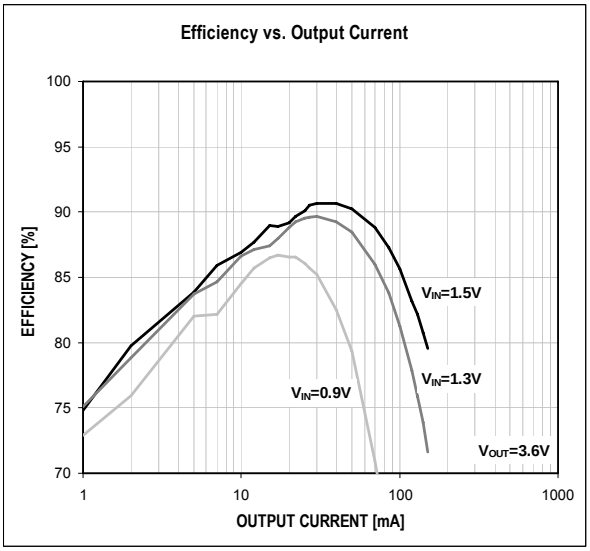
Parameter

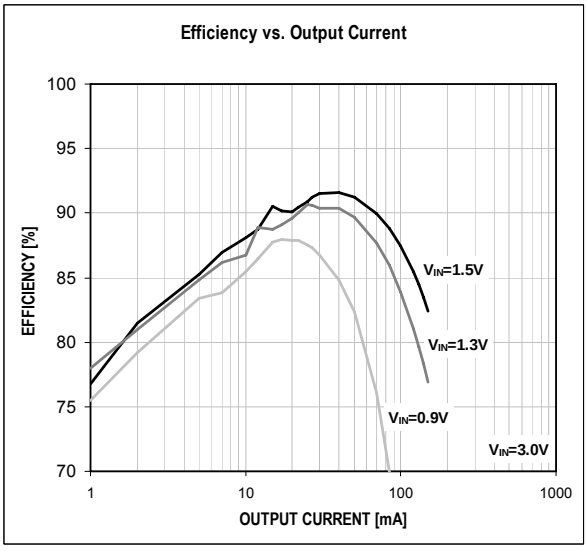
Table 22 DCDC Boost Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDD2.9}$	Quiescent Current	Power down mode			5	µA
		PFM mode operation		40		µA
		PWM mode		300		µA
$V_{STARTUP}$	Startup Voltage	R_{Load}>220Ω	1.0			V
V_{HOLD}	Hold-on Voltage	I_{OUT}=1mA, VBAT falling from 1.5 to 0V		0.5		V
R_{SWN_on}	Internal N-Switch R_{DS_ON}				500	mΩ
R_{SWP_on}	Internal P-Switch R_{DS_ON}				900	mΩ
f_{SW}	Switching Frequency	Start-up, X3VOK=1	100	250	500	kHz
		PWM mode operation, X3VOK=0		1.2		MHz
t_{ON_min}	Minimum On-time			100		ns
t_{OFF_min}	Minimum Off-time			100		ns
η_{eff}	Efficiency	I_{OUT}=20mA, Vin=1.35		85		%
		I_{OUT}=50mA, Vin=1.5		87		%
I_{SW_LIM}	Current Limit	1.0V ≤ VB1V ≤ 3.0V	0.60	0.85	1.10	A
I_{OUT}	Load Current	VB1V=1.0V			150	mA

Vin=1.0..2.0V, C(VBAT_1V) = 2.2µF ceramic || 2000µF Elko, C(BVDD) = 3 x 2.2µF ceramic, L=DS1608 6.8µH, Temp = 25deg

Figure 19 DCDC Boost Typical Performance Characteristics





L=DS1608 6.8µH, Temp = 25deg

Register Description

Table 23 DCDC3V Related Register

Name	Base	Offset	Description
DCDC3V	2-wire serial	17h-7	DCDC3 output voltage settings
PMU ENABLE	2-wire serial	18h	Enables writings to extended register 17h-7

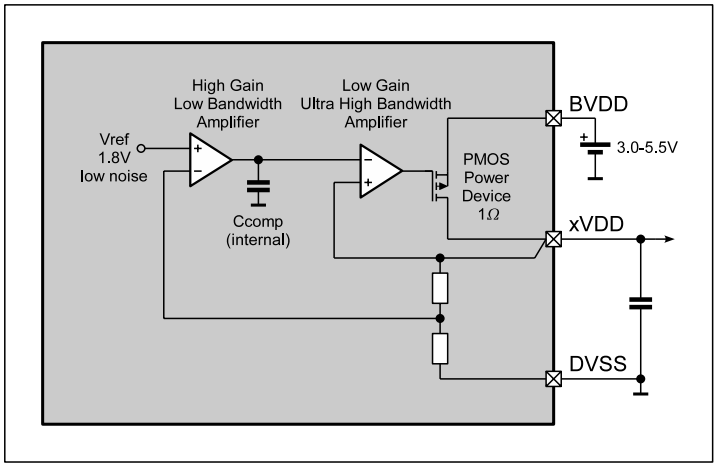
8.2.2 Low Drop Out Regulators

General

These LDO's are designed to supply sensitive analogue circuits, audio devices, AD and DA converters, micro-controller and other peripheral devices. The design is optimised to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF +/-20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress high ripple on the battery at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

Figure 20 LDO Block Diagram



LDO1

This LDO generates the analog supply voltage used for the AFE itself.

- Input voltage is BVDD
- Output voltage is AVDD (typ. 2.9V)
- Driver strength: 100mA

It is set to a fixed output voltage of 2.9V, 100mA$_{max}$. It supplies the analog part of the AFE. Additional external loads are possible but most not exceed the supply ratings in total together with the operating internal blocks. Further the external load must not induce noise to the sensitive AVDD supply pin.

LDO2

This LDO generates the digital supply voltage used for the AFE itself.

- Input Voltage is BVDD
- Output Voltage is DVDD (typ. 2.9V)
- Driver strength: 100mA

It is set to a fixed output voltage of 2.9V, 100mA$_{max}$. It supplies the digital part of the AFE. Additional external loads are possible but most not exceed the supply ratings in total together with the operating internal blocks. Further the external load must not induce noise to the DVDD supply pin but is not as critical as AVDD.

LDO3 & LDO4

These LDOs can used to generate the periphery voltage for the digital processor or other external components (e.g. ext. DAC, USB-PHY, SD-Cards, NAND-Flashes, FM-Tuner …)

LDO3 has a separate input pin (BVDDP1) which can be connected to either the battery or a DCDC converter output.

- Input Voltage BVDDP1 or BVDD
- Output Voltage is PVDD1 & PVDD2 (1.2 to 3.5V)
- Default value at start-up is defined by VPRG1 pin
- Driver strength: 100mA, can be programmed to 200mA

Parameter

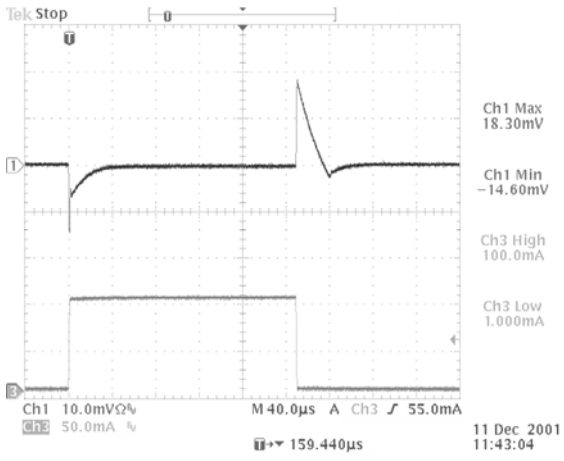
Table 24 LDOs Block Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ON}	On resistance				1	Ω
PSRR	Power supply rejection ratio	f=1kHz		70		dB
		f=100kHz		40		
I_{OFF}	Shut down current			100		nA
I_{VDD}	Supply current	without load		50		µA
Noise	Output noise	10Hz < f < 100kHz		50		$µV_{rms}$
t_{start}	Startup time			200		µs
V_{out_tol}	Output voltage tolerance	minimum +/- 50mV	-2.5%		2.5%	mV
$V_{LineReg}$	Line regulation	LDO1, Static		<1		mV
		LDO1, Transient;Slope: t_r=10µs		<10		
$V_{LoadReg}$	Load regulation	LDO1, Static		<1		mV
		LDO1, Transient;Slope: t_r=10µs		<10		
I_{LIMIT}	Current limitation	LDO1, LDO2, LDO3, LDO4		200		mA
		LDO 3 and LDO4, has to be enabled via register 17h-1, 17h-2		350		

BVDD=4V; I_{LOAD}=150mA; T_{amb}=25ºC; C_{LOAD} =2.2µF (Ceramic); unless otherwise specified

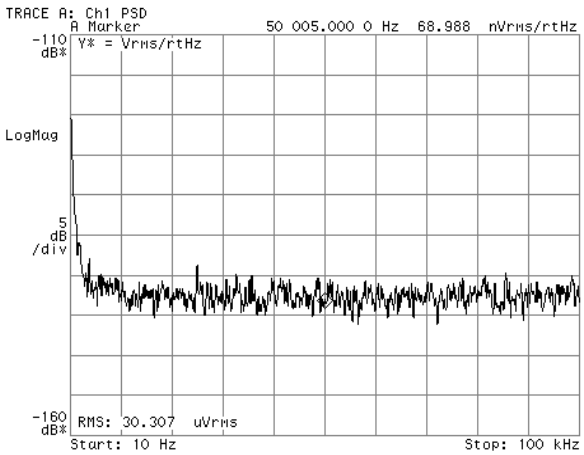
Figure 21 Typical Performance Characteristics

Load regulation



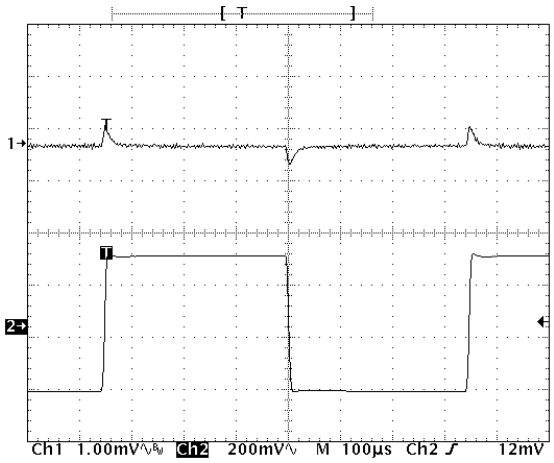
transient load: 1mA – 100mA
slope: 1µs

Output noise



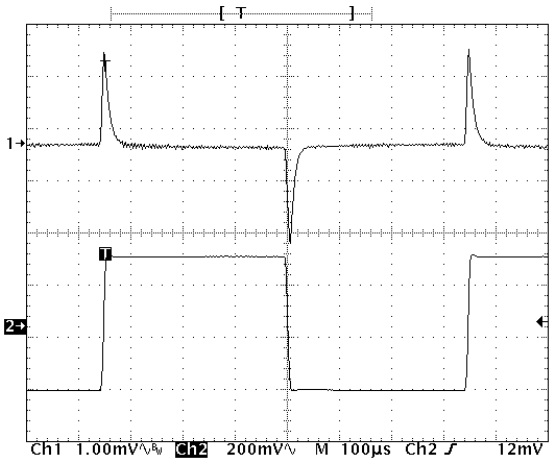
Output load: 150mA

Load Regulation



output load: 10mA
transient input voltage ripple: 500mV

Load Regulation



output load: 150mA
transient input voltage ripple: 500mV

Register Description

Table 25 LDO Related Register

Name	Base	Offset	Description
PMU PVDD1	2-wire serial	17h-1	PVDD1 (LDO3) control and voltage settings
PMU PVDD2	2-wire serial	17h-2	PVDD2 (LDO4) control and voltage settings
PMU ENABLE	2-wire serial	18h	Enables writings to extended registers 17h-1, 17h-2

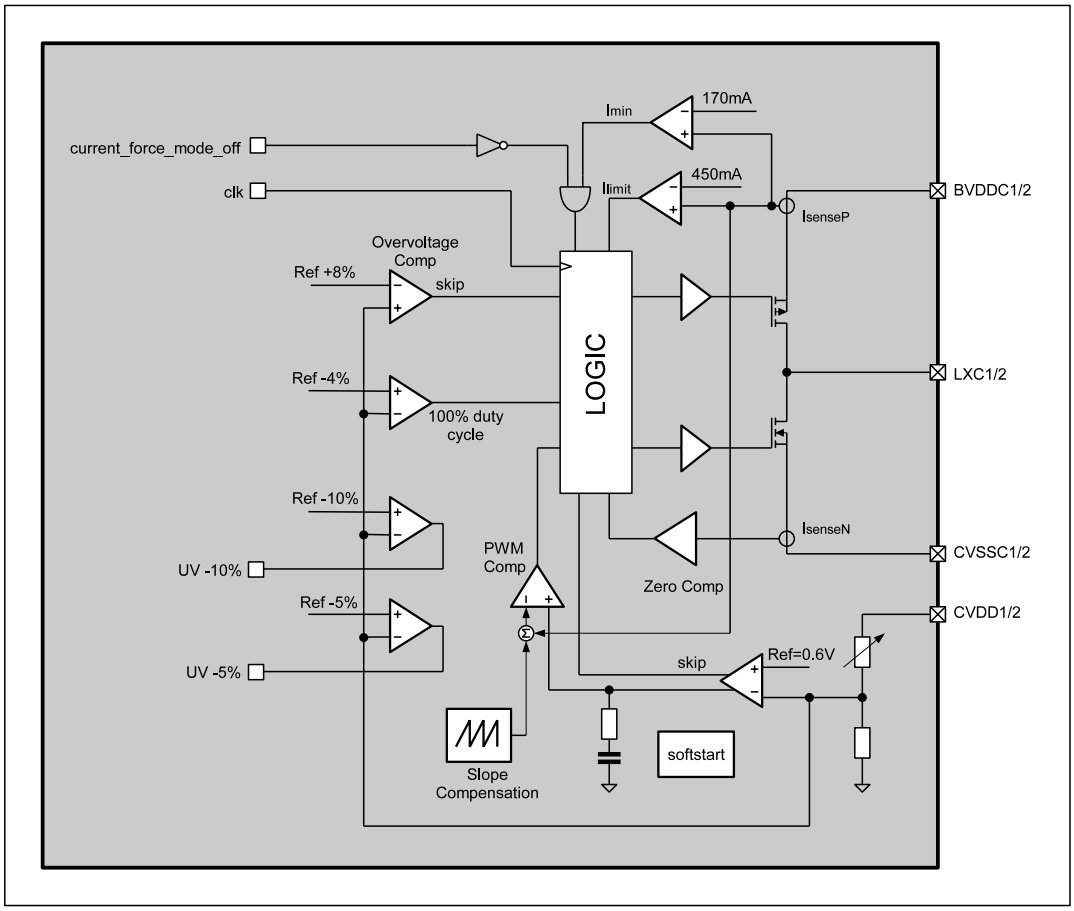
8.2.3 DCDC Step-Down Converter (2x)

General

These converters are meant to convert the battery voltage down to voltages which fit to the core and peripheral supply voltage requirements for microprocessors.

- Input Voltage BVDDC1/2 (usually connected to the battery)
- Output Voltage CVDD1 & CVDD2
- output voltage levels can be programmed independently form 0.65V to 3.4V
- the default value at start-up is defined by VPRG1 pin
- driver strength 250mA

Figure 22 DCDC Step-Down Block Diagram



Functional Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 97% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 250mA, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

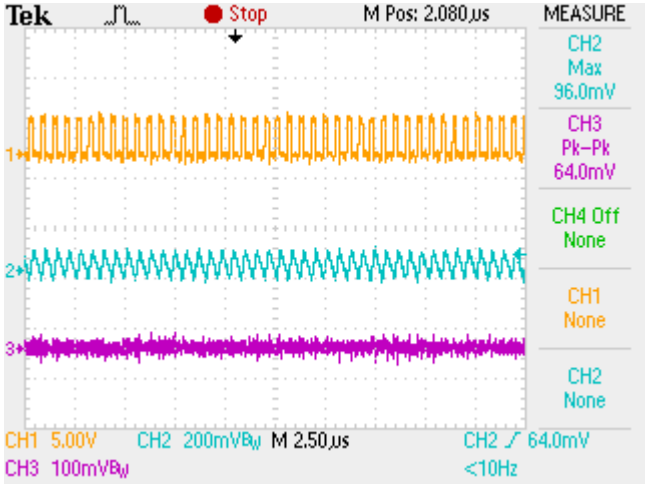
To achieve optimised performance in different applications, adjustable settings allow to compromise between high efficiency and low input, output ripple:

Low ripple, low noise operation:

In this mode there is no minimum coil current necessary before switching off the PMOS. As result, the ON time of the PMOS will be reduced down to tmin_on at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise, but decreased efficiency, at light loads,

especially at low input to output voltage differences. In the case of an inverted coil current the regulator will not operate in pulse skip mode.

Figure 23 DCDC buck with disabled current force / pulse skip mode

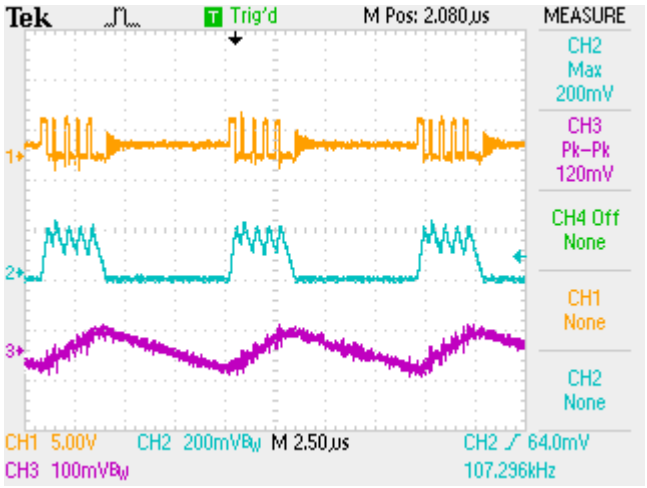


1: LXC1 voltage, 2:coil current (1mV=1mA) 3: output voltage

High efficiency operation:

In this mode there is a minimum coil current necessary before switching off the PMOS. As result, fewer pulses at low output loads are necessary, and therefore the efficiency at low output load is increased. On the other hand the output voltage ripple increases, and the noisy pulse skip operation is on up to a higher output current.

Figure 24 DCDC buck with enabled current force / pulse skip mode



1: LXC1 voltage, 2:coil current (1mV=1mA) 3: output voltage

It's also possible to switch between these two modes dynamically during operation:

100% PMOS ON mode for low dropout regulation:

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is than in LDO mode. This feature is enabled if the output voltage drops by more than 4%.

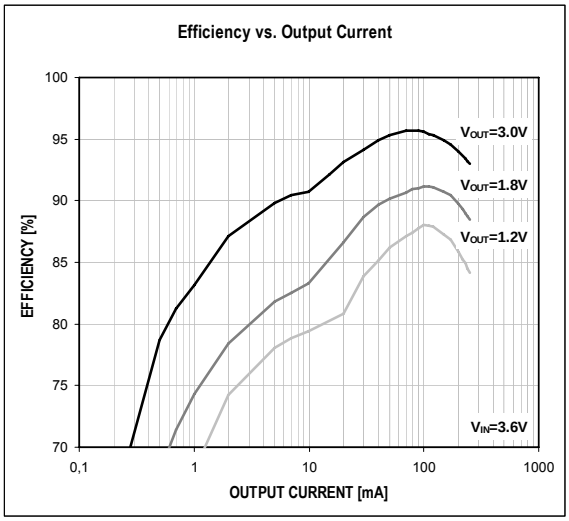
Parameter

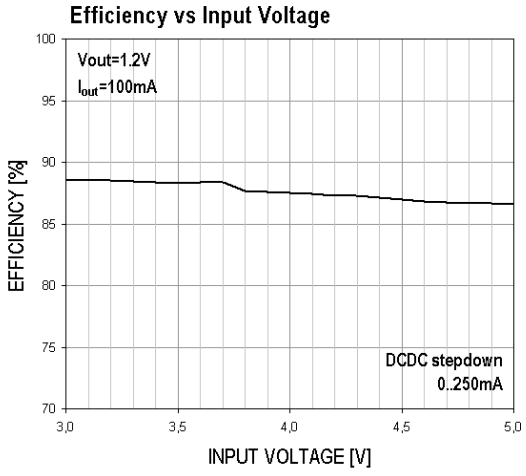
Table 26 DCDC Buck Typical Performance Parameter

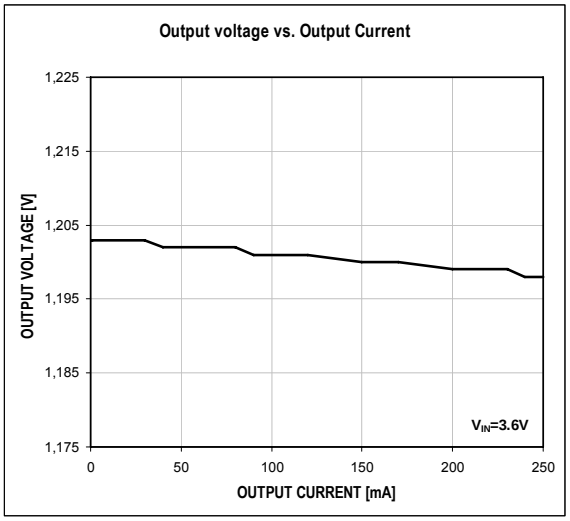
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage	BVDD	3.0		5.5	V
V_{OUT}	Regulated output voltage		0.65		3.4	V
V_{OUT_tol}	Output voltage tolerance	minimum +/- 50mV	-3%		3%	mV
I_{load}	Maximum Load current			250		mA
I_{LIMIT}	Current limit			450		mA
R_{PSW}	P-Switch ON resistance	BVDD=3.0V		0.5	0.7	Ω
R_{NSW}	N-Switch ON resistance	BVDD=3.0V		0.5	0.7	Ω
f_{SW}	Switching frequency			1.2		MHz
f_{SWsc}	Switching frequency	in shortcut case		0.6		MHz
C_{out}	Output capacitor	Ceramic, +/- 10% tolerance		10		µF
Lx	Inductor	+/- 10% tolerance	3.3		4.7	µH
η_{eff}	Efficiency	Iout=100mA, Vout=3.0V		97		%
I_{VDD}	Current consumption	Operating current without load Low power mode current Shutdown current		220 100 0.1		µA
t_{MIN_ON}	Minimum on time			80		ns
t_{MIN_OFF}	Minimum off time			40		ns
$V_{LineReg}$	Line regulation	Static		2		mV
		Transient; Slope: t_r=10µs, 100mV step, 200mA load		10		
$V_{LoadReg}$	Load regulation	Static		5		mV
		Transient; Slope: t_r=10µs, 100mA step		50		

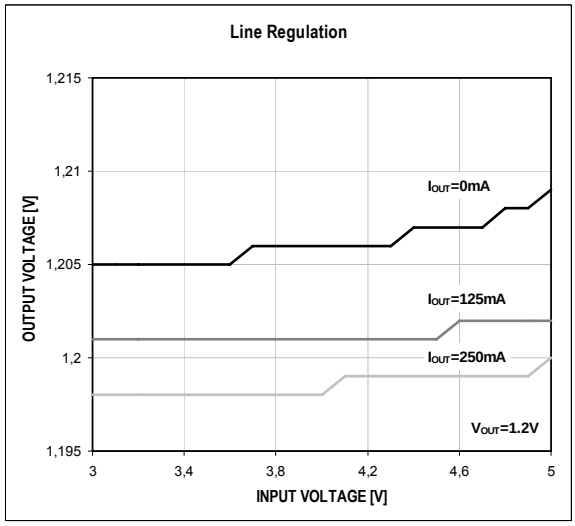
BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

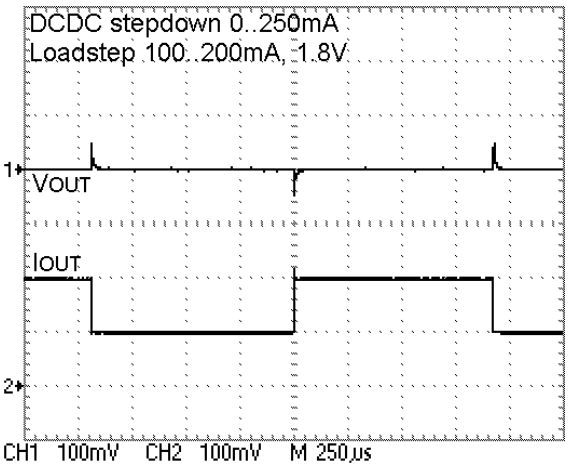
Figure 25 DCDC Step-down Performance Characteristics

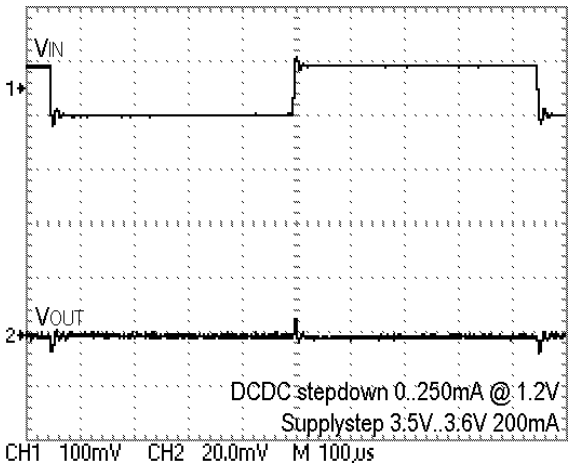












Register Description

Table 27 DCDC Buck Related Register

Name	Base	Offset	Description
PMU CVDD1	2-wire serial	17h-3	CVDD1 (DCDC1) control and voltage settings
PMU CVDD2	2-wire serial	17h-4	CVDD2 (DCDC2) control and voltage settings
PMU ENABLE	2-wire serial	18h	Enables writings to extended registers 17h-3, 17h-4

8.2.4 Charger

General

This block can be used to charge a 4V Li-Ion accumulator. It supports constant current and constant voltage charging modes with adjustable charging currents (55 to 460mA) and maximum charging voltage (3.9 to 4.25V).

An internal protection circuit will limit the charging current when a CHGIN voltage drop is detected.

Figure 26 Charger Block Diagram

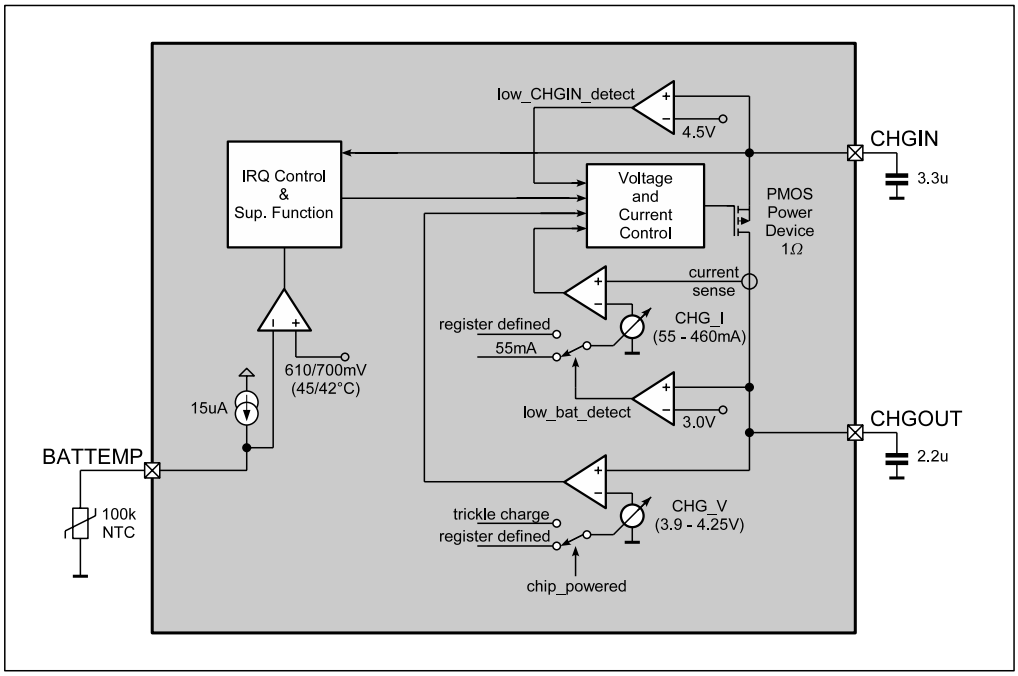
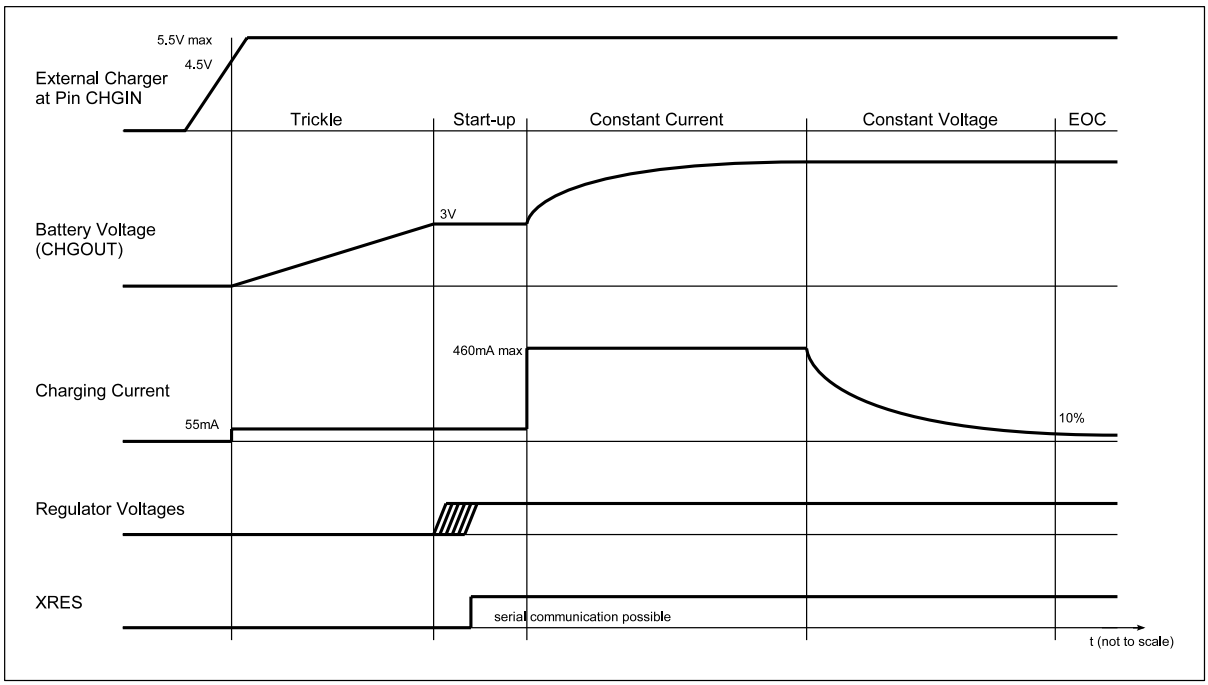


Figure 27 Charger States



Trickle Charge

If BVDD is below 3V in systems where the battery is not separated from BVDD, the charger goes automatically in trickle charge mode with 50mA charging current and 3.9V endpoint voltage. In this mode charging current and voltage are not precise, but provide a charger function also for deep discharged batteries. The temperature supervision is not enabled in trickle charge mode.

As soon as BVDD reaches 3V the AFE switches on and starts-up the regulators with the power-up sequence selected by pin VPRG1. Afterwards the CPU can set the modes and the charging currents via the 2-wire serial interface.

If the battery (CHGOUT) voltage is below 3V the charging current cannot be set higher than 55mA, this is also true when using a battery separation circuit to supply the AFE (BVDD) from USB or another voltage source.

Temperature Supervision

This charger block also features a 15uA supply for an external 100k NTC resistor to measure the battery temperature while charging. If the temperature is too high (>45°C), an interrupt can be generated. If the battery temperature drops below 42°C the charger will start charging again. The temperature supervision is not enabled in trickle charge mode.

If the NTC resistor does not have 100kΩ its value can be corrected with a resistor in series or in parallel.

Parameter

Table 28 Charger Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CHG_trick}	Charging Current (trickle charge)	BVDD<=3V, CHGIN = 5.5V	37	68	111	mA
		BVDD<=3V, CHGIN = 4.0V	17	32	55	
V_{CHG_trick}	Charger Endpoint Voltage (trickle charge)	BVDD<=3V, CHGIN = 4.4V	0.70* CHGIN	0.72* CHGIN	0.74* CHGIN	V
I_{CHG} (0-7)	Charging Current	BVDD > 3V, I_{CHG} > 60mA	I_{NOM} -8%	I_{NOM}	I_{NOM} +8%	mA
V_{CHG} (0-7)	Charging Voltage	BVDD > 3V, end of charge is true	V_{NOM} -50mV	V_{NOM}	V_{NOM} +30mV	V
V_{ON_ABS}	Charger On Voltage IRQ	BVDD = 3V		3.1	4.0	V
V_{ON_REL}	Charger On Voltage IRQ	CHGIN-CHGOUT		170	240	mV
V_{OFF_REL}	Charger Off Voltage IRQ	CHGIN-CHGOUT	40	77		mV
V_{BATEMP_ON}	Battery Temp. high level (45°C)	BVDD >3V		610		mV
V_{BATEMP_OFF}	Battery Temp. low level (42°C)	BVDD >3V		700		mV
I_{CHG_OFF}	End Of Charge current level	BVDD >3V	5% I_{NOM}	10% I_{NOM}	15% I_{NOM}	mA
I_{REV_OFF}	Reverse current shut down	BVDD = 5V, CHGIN open		<1		uA

BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

Register Description

Table 29 Charger Related Register

Name	Base	Offset	Description
CHARGER	2-wire serial	22h	Charger voltage, current and temp. supervision control
IRQ_ENRD_2	2-wire serial	25h	Enable/disable EOC and battery over-temperature interrupt Read out charger status

8.2.5 15V Step-Up Converter

General

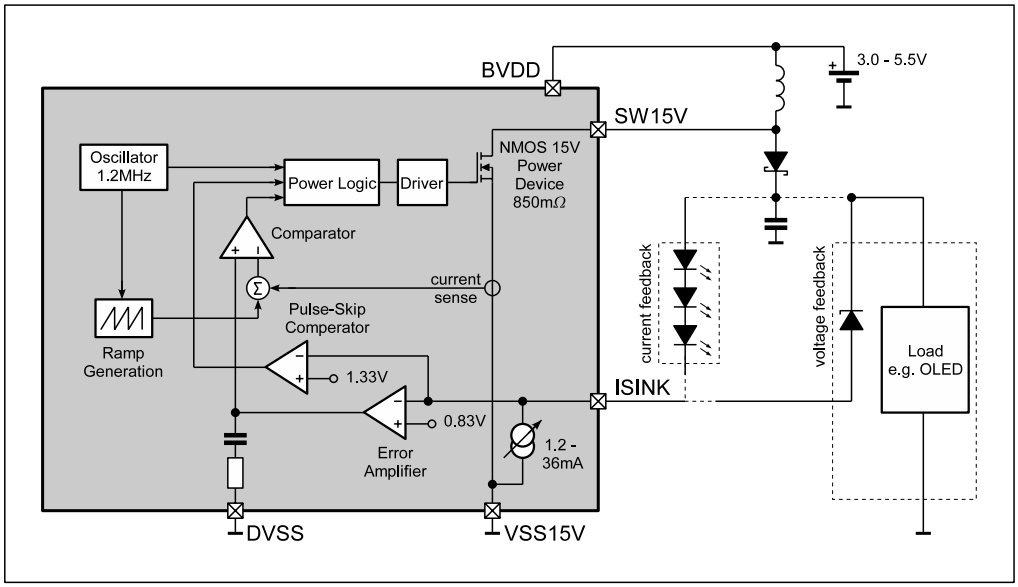
The integrated Step-Up DC/DC Converter is a high efficiency current-mode PWM regulator, providing an output voltage up to 15V. A constant switching-frequency results in a low noise on supply and output voltages. When using an additional transistor the output voltage can be up to 25V to drive 6 white LED in series.

It has an adjustable sink current (1.2 to 36mA) to provide e.g. dimming function when driving white LEDs as back-light.

A voltage feedback mode allows generating constant supply voltages for e.g. OLEDs by using an external Zener diode. To bias the diode ISINK is sinking about 10uA in this voltage feedback mode.

An internal protection circuit will shut down the regulator if the voltage on SW15 exceeds 15V. No more external protection has to be used to avoid an exceeding of the operation conditions in a no load situation.

Figure 28 DCDC15 Block Diagram



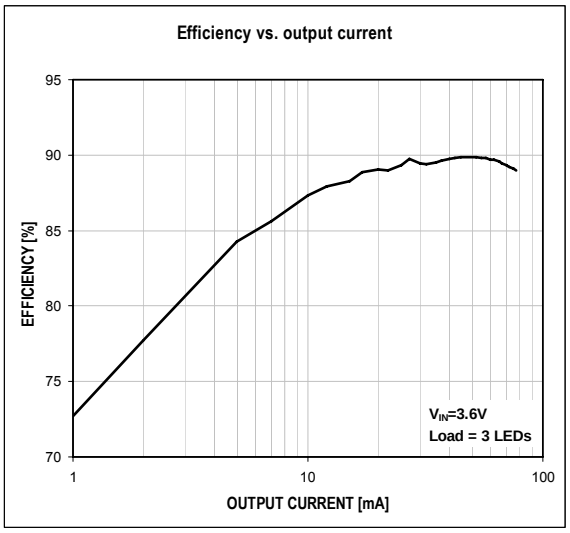
Parameter

Table 30 15V Step-Up Converter Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SW}	High Voltage Pin	Pin SW15	0		15	V
I_{VDD}	Quiescent Current	Pulse Skipping mode		140		µA
V_{FB}	Feedback Voltage, Transient	Pin ISINK	0		5.5	V
V_{FB}	Feedback Voltage, during Regulation	Pin ISINK	0.65	0.83	1.0	V
I_{SW_MAX}	Current Limit	V15_ON = 1	350	510	750	mA
R_{SW}	Switch Resistance	V15_ON = 0		0.85	1.54	Ω
I_{LOAD}	Load Current	@ 15V output voltage	0		45	mA
I_{FB}	Current into ISINK during voltage feedback mode			10		uA
$V_{PULSESKIP}$	Pulse-skip Threshold	Voltage at pin ISINK, pulse skips are introduces when load current becomes too low.	1.2	1.33	1.5	V
F_{IN}	Fixed Switching Frequency		0.45	0.6	0.75	MHz
C_{OUT}	Output Capacitor	Ceramic		1		µF
L (Inductor)	I_{LOAD} > 20mA	Use inductors with small $C_{PARASITIC}$ (<100pF) for high efficency	17	22	27	µH
	I_{LOAD} < 20mA		8	10	27	
t_{MIN_ON}	Minimum On-Time	Guaranteed per design	90		180	ns
MDC	Maximum Duty Cycle	Guaranteed per design	85	91	98	%

BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

Figure 29 15V Step-Up Performance Characteristics



Register Description

Table 31 15V Step-Up Related Register

Name	Base	Offset	Description
DCDC15	2-wire serial	1Bh	DCDC15 current and dimming control

8.3 SYSTEM Functions

8.3.1 SYSTEM

General

The system block handles the power up, power down and regulator voltage settings of the AFE.

The PWGD output is able to drive also the PLL clock, the SPDIF output or a PWM signal. The output can be configured to be push/pull (3 different driver strengths) or open-drain.

Power Up Conditions

The chip powers up when one of the following condition is true:

- High signal on the PWR_UP pin (>80ms, >1V & >1/3 BVDD)
- Rising edge on the VBUS pin (USB plug in: BVDD>3V or VB1V >1V, VBUS>4.5V)
- Rising edge on the CHGIN pin (charger plug in: BVDD>3V or VB1V >1V, CHGIN>4.0V)
- RTC wake-up: The auto wake-up timer is internally connected to the Power-up and Hibernation Control block.

To hold the chip in power up mode the PWR_HOLD bit in the SYSTEM register (0x20h) is set.

Power Down Conditions

The chip automatically shuts off if one of the following conditions arises:

- Clearing the PWR_HOLD bit in SYSTEM register (0x20h)
- I2C watchdog power down(no serial reading for >1s, has to be enabled)
- Heartbeat watchdog via pin HBT(no watchdog reset via HBT pin for > 500ms, has to be enabled)
- BVDD drops below the minimum threshold voltage (<2.7V)
- LDO or step down converter output voltage drop below a programmable level (has to be enabled)
- Junction temperature reaches maximum threshold, set in SUPERVISOR register (0x24h)
- High signal on the PWR_UP pin for more than (>6s, >1V & >1/3 BVDD).
  With setting SD_TIME bit in register 24h the time can be doubled.

Start-up Sequence

The AFE offers 5 different power-up sequences. The specific start-up sequence can be selected via VPRG1 pin. These pin detects 5 logical input states which shall come from an external resistor divider network.

At first, LDO1 (AVDD) and LDO2 (DVDD) is powering up. This cannot be influenced with the selection of specific sequences below. LDO1 and LDO2 are necessary for the internal supply of the AFE.

After power-up sequence selected by pin VPRG1, all voltage settings and power on/off conditions of the described regulators can be programmed via the serial interface.

Table 32 Start-up Modes

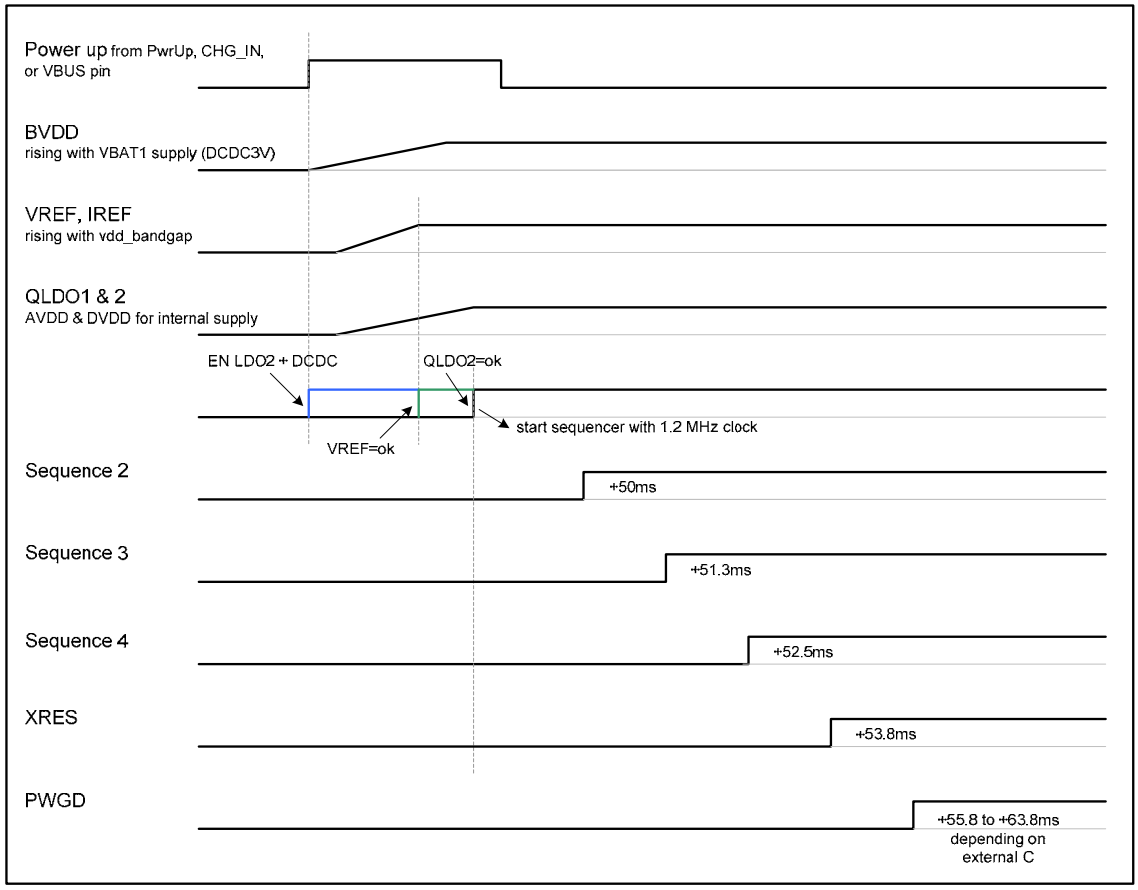
#	VPRG1	DCDC1		DCDC2		LDO3		LDO4		DCDC3V		XRES/ PWGD	
		CVDD1		CVDD2		PVDD1		PVDD2		BVDD			
1	**vss**	1,2V	2nd	2,8V	3rd	1,8V	4th		x	3,6V	1st	5th	6th
2	**vdd**	1,2V	4th	1,8V	3rd	3,3V	2nd		x	3,6V	1st	5th	6th
3	**150k-PU**	1,2V	2nd	1,8V	3rd	3,3V	4th		x	3,6V	1st	5th	6th
4	**reserved**												
5	**reserved**												

x … means that this regulator is not started with the start-up sequencer but has to be turned on by the 2-wire serial interface when needed.

PWGD delay with CRES pin

With using an external capacitor on CRES, the PWGD signal can be delayed. This delay can be calculated with the 5uA pull-up current and a comparator threshold of 1.5V. Using a 33nF capacitance will give a delay of 10ms.

Figure 30 Power Up Timing



Register Description

Table 33 System Related Register

Name	Base	Offset	Description
OutContr	2-wire serial	12h-1	Control of PWGD signal and drive
PMU ENABLE	2-wire serial	18h	Enables writings to extended registers 12h-1
SYSTEM	2-wire serial	20h	Watchdog and Over-temperature control, Power down enable
IRQ_ENRD_1	2-wire serial	24h	Enable/disable wake-up interrupts, set shut-down time
IRQ_ENRD_3	2-wire serial	26h	Enable/disable junction temperature interrupt

8.3.2 Hibernation

General

Hibernation allows shutting down a part or the complete system. Hibernation can be terminated by every possible interrupt of the AFE. E.g. one can use the RTC for a time triggered wake-up. The interrupt has to be enabled before going to hibernation

Table 34 Hibernation Modes

Action	KeepBit	LDO3	DCDC1/2
Hib. with Default	OFF	OFF	OFF
Cancel Hibernation	OFF	Default	Default
Hib. with Modif Settings	OFF	OFF	OFF
Cancel Hibernation	OFF	As Before	As Before
Hib. with Modif Settings	ON	No Change	No Change
Cancel Hibernation	ON	No Change	No Change

“Hibernation with Default” means that, the voltage of the power supply is determined by VPRG1 pin.

“Hibernation with Modified Settings” means, that the voltage of the power supply is controlled by register settings.

Register Description

Table 35 Hibernation Related Register

Name	Base	Offset	Description
PMU Hibernate	2-wire serial	17h-6	Hibernation control
PMU ENABLE	2-wire serial	18h	Enables writings to extended register 17h-6

8.3.3 Supervisor

General

This supervisor function can be used for automatic detection of BVDD brown out or junction over-temperature condition.

BVDD Supervision

The supervision level can be set in 8 steps @ 60mV from 2.74 to 3.16V. If the level is reached an interrupt can be generated. If BVDD reaches 2.7V the AFE shuts down automatically.

Junction Temperature Supervision

The temperature supervision level can also be set by 5 bits (120 to –15°C). If the temperature reaches this level, an interrupt can be generated. The over-temperature shutdown level is always 20°C higher.

Pls note that the temp supervision might be influenced by a VBE reading of the general purpose ADC.

Power Rail Monitoring

The 4 main regulators have an extra monitor which observes the output voltage of the regulators. This power rail monitors are independent from the 10bit ADC. To activate these please see related registers.

Register Description

Table 36 Supervisor Related Register

Name	Base	Offset	Description
SUPERVISOR	2-wire serial	21h	Battery and junction temperature supervision threshold levels
IRQ_ENRD_0	2-wire serial	23h	Enable/disable PVDD/CVDD monitoring interrupt and shutdown
IRQ_ENRD_1	2-wire serial	24h	Enable/disable PVDD/CVDD monitoring interrupt and shutdown
IRQ_ENRD_2	2-wire serial	25h	Enable/disable battery brown out interrupt
IRQ_ENRD_3	2-wire serial	26h	Enable/disable junction temperature interrupt

8.3.4 Interrupt Generation

General

All interrupt sources can get enabled or disabled by corresponding bits in the 5 IRQ-bytes. By default no interrupt source is enabled.

The XIRQ output can get configured to be PUSH/PULL or OPEN_DRAIN and ACTIVE_HIGH or ACTIVE LOW with 2 bits in IRQ_ENRD_4 register (27h). Default state is open drain and active_low.

IRQ Source Interpretation

There are 3 different modules to process interrupt sources:

LEVEL

The IRQ output is kept active as long as the interrupt source is present and this IRQ-Bit is enabled

EDGE

The IRQ gets active with a high going edge of this source. The IRQ stays active until the corresponding IRQ-Register gets read.

STATUS CHANGE

The IRQ gets active when the source-state changes. The change bit and the status can be read to notice which interrupt was the source. The IRQ stays active until the corresponding interrupt register gets read.

De-bouncer

There is a de-bounce function implemented for USB and CHARGER. Since these 2 signals can be unstable for the phase of plug-in or unplug, a de-bounce time of 512ms/256ms/128ms/8ms can be selected.

Interrupt Sources

25 IRQ events will activate the XIRQ pin:

- Headphone connected
- Headphone over-current
- Microphone connected
- Microphone remote control
- Voice activation threshold reached
- RTC sec/min elapsed
- 10bit ADC end of conversion
- I²S changed
- USB changed
- Charger changed
- End of charge (at 10% of programmed current)
- Battery temperature high (at 45°C with 100kΩ NTC)
- Junction temperature high
- RVDD low (e.g. after battery was changed)
- Battery low (Brown-out voltage reached)
- Wake-up from hibernation
- Power-up key (pin PWRUP) pressed
- Power rail monitor: over-voltage PVDD1, PVDD2, CVDD1, CVDD2
- Power rail monitor: under-voltage PVDD1, PVDD2, CVDD1, CVDD2

8.3.5 Real Time Clock

General

The real time clock block is an independent block, which is still working even when the chip is shut down. The only condition for this operation is that BVDDR has a voltage of above 1.0V. The block uses a standard 32kHz crystal that is connected to a low power oscillator. The total power consumption is typ. 650nA. (Q32k clock buffer not operating)

An internal supply switch will supply the RTC as long as possible form the single-cell or Li-Ion battery and only switch to BVDDR if the main battery is empty or has been removed.

The RTC seconds counter is 32bit wide and can be programmed via the 2-wire serial interface. The RTC can deliver a second or minute interrupt.

Another 23bit wide counter allows auto wake-up (max. after 96 days). This counter is internally connected to the power-up and hibernation control block.

The RTC voltage regulator (RVDD) further supplies a 128bit SRAM. It can be used to store settings or data before shutdown.

The Q32K output is able to drive also the PLL clock, the SPDIF output or a PWM signal. The output can be configured to be push/pull (3 different driver strengths) or open-drain.

Clock adjustment

The RTC clock is adjustable in steps of 7.6ppm which allows the use of inexpensive 32kHz crystals. The nominal frequency shall be 32.768Hz. This frequency is divided down to 0.25Hz:
f = 32.768 / (4*32*1024)

At the input of this divider one can add corrective counts, which allow to correct an inaccurate crystal in a range from –64 counts (=-488ppm) to +63 counts (=+480ppm):
$f_{corrected} = f_{crystal} / [(4*32*1024)-64+RTC\_TBC]$

Register Description

Table 37 RTC Related Register

Name	Base	Offset	Description
OutContr	2-wire serial	12h-1	Control of Q32K signal and drive
PMU ENABLE	2-wire serial	18h	Enables writings to extended registers 12h-1
RTC_WakeUp	2-wire serial	19h	RTC wake-up settings and SDRAM access
IRQ_ENRD_2	2-wire serial	25h	Interrupt settings for RVDD under-voltage detection
IRQ_ENRD_4	2-wire serial	27h	Interrupt settings for getting a second or minute interrupt
RTCC	2-wire serial	28h	RTC oscillator and counter enable
RTCT	2-wire serial	29h	RTC interrupt and time correction settings
RTC_0 to RTC_3	2-wire serial	2Ah to 2Dh	RTC time-base seconds registers

8.3.6 10-Bit ADC

General

This general purpose ADC can be used for measuring several voltages and currents to perform functions like battery monitor, temperature supervision, button press detection, etc..

Input Sources

Table 38 ADC10 Input Sources

Nr.	Source	Range	LSB	Description
0	CHGOUT	5.120V	5mV	check battery voltage of 4V Li-Ion accumulator
1	BVDDR	5.120V	5mV	check RTC backup battery voltage (connected to BVDD inside the package)
2		5.120V	5mV	Source defined by DC_TEST in register 0x18
3	CHGIN	5.120V	5mV	check charger input voltage
4				reserved
5	BatTemp	2.560V	2.5mV	check battery charging temperature
6	MICS	2.560V	2.5mV	check voltage on MICS for remote control or external voltage measurement
7				reserved
8	VBE_1uA	1.024	1mV	measuring basis-emitter voltage of temperature sense transistor; Tj = (674 - [ADC_bit0:bit9]) / 2
9	VBE_2uA	1.024	1mV	measuring basis-emitter voltage of temperature sense transistor; Tj = (694 - [ADC_bit0:bit9]) / 2
10	I_MICS	1.024mA typ.	2.0uA	check current of MICS for remote control detection
11				reserved
12	VB1V	2.560V	2.5mV	check single cell battery voltage
13	VBUS	5.120V	5mV	check USB input voltage
14..15	Reserved	1.024V	1mV	for testing purpose only

Reference

AVDD=2.9V is used as reference to the ADC. AVDD is trimmed to +/-20mV with over all precision of +/-29mV. So the absolute accuracy is +/-1%. Including divider and gain stages an overall accuracy of 3% is achieved.

Parameter

Table 39 ADC10 Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{DIV}	Input Divider Resistance	CHGOUT, BVDDR, VBUS, CHGIN	138k	180k	234k	Ω
ADC_{FS}	ADC Full Scale Range		2.534	2.56	2.586	V
Ratio1	Division Factor 1	CHGOUT, BVDDR, VBUS, CHGIN	0.198	0.2	0.202	1
Ratio2	Division Factor 2	VB1V, RVDD, BATTEMP, MICS	0.396	0.4	0.404	1
Gain	ADC Gain Stage		2.475	2.5	2.525	
T_{CON}	Conversion Time		-	34	50	µs
I_MIC_{FS}	I_MICS Full Scale Range		0.7	1.0	1.4	mA

BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

Register Description

Table 40 ADC10 Related Register

Name	Base	Offset	Description
PMU_ENABLE	2-wire serial	18h	Extended ADC source selection
IRQ_ENRD_4	2-wire serial	27h	Interrupt settings for end of conversion interrupt
ADC_0	2-wire serial	2Eh	ADC source selection, ADC result<9:8>
ADC_1	2 wire serial	2Fh	ADC result <7:0>

8.3.7 Unique ID Code (64 bit OTP ROM)

General

This fuse array is used to store a unique identification number, which can be used for DRM issues. The number is generated and programmed during the production process.

Register Description

Table 41 UID Related Register

Name	Base	Offset	Description
UID_0 to UID_7	2-wire serial	38h to 3Fh	Unique ID register 0 to 7

8.4 Register Description

Table 42 I2C Register Overview

Addr	Name	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
00h	LINE_OUT_R	LO_MUX_B 0:SUM_Stereo;1:SUM_MDiff 2:ADC_IN; 3:DAC_OUT		-	LOR_VOL Gain from MUX_B to LOUT1R= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
01h	LINE_OUT_L	-	MUTE_OFF_J	-	LOL_VOL Gain from MUX_B to LOUT1L= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
02h	HPH_OUT_R	HP_OVC_TO_OFF 0: 256ms	HP_MUTE_C 0:SUM_Stereo;1: DAC_OUT 2:LineIn 1/3; 3: LineIn 2		HPR_VOL Gain from MUX_C to HPR= (-45.43dB ... +1.07dB)				
		0	0	0	0	0	0	0	0
03h	HPH_OUT_L	MUTE_ON_K	HP_ON	HPDET_ON	HPL_VOL Gain from MUX_C to HPL= (-45.43dB ... +1.07dB)				
		0	0	0	0	0	0	0	0
06h	MIC_R	MIC_AGC_OFF	PRE_GAIN 0: 28dB; 1: 34dB 2: 40dB		MR_VOL Gain from MicAmp (N6) to Mixer (N12) = (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
07h	MIC_L	MSUP_OFF	MUTE_OFF_D	RDET_OFF	ML_VOL Gain from MicAmp (N6) to Mixer (N13) = (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
0Ah	LINE_IN1_R	-	LI_MUX_E 0: LI1; 1: LI3	MUTE_OFF_B	LI1R_VOL Gain from LIN1R to Mixer (N10)= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Bh	LINE_IN1_L	LI1_MODE 00: SE_Sterep; 01: MonoDiff 10: SE_Mono		MUTE_OFF_G	LI1L_VOL Gain from LIN1L to Mixer (N17)= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Ch	LINE_IN2_R	-	-	MUTE_OFF_C	LI2R_VOL Gain from LIN2R to Mixer (N11)= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Dh	LINE_IN2_L	LI2_MODE 00: SE_Sterep; 01: MonoDiff 10: SE_Mono		MUTE_OFF_F	LI2L_VOL Gain from LIN2L to Mixer (N16)= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Eh	DAC_R	-	-	-	DAR_VOL Gain from DAC (N19) to Mixer/MUX (N23)= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
0Fh	DAC_L	-	MUTE_OFF_H	-	DAL_VOL Gain from DAC (N22) to Mixer/MUX (N26) = (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
10h	ADC_R	ADC_MUX_A 0: Stereo_Mic; 1:LineIN_1/3 2: LineIN_2; 3: AudioSUM		-	ADR_VOL Gain from MUX_A to ADC (N9) = (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
11h	ADC_L	-	MUTE_OFF_A	-	ADL_VOL Gain from MUX_A to ADC (N18) = (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0

Addr	Name	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
12h-1	OutContr	DRIVE_PWGD 0: 12mA OD; 1: 12mA PP 2: 4mA PP; 3: 2mA PP		MUX_PWGD 0: PWGD; 1: PWM 2: SPDIF; 3: PLL clock		DRIVE_Q32K 0: 12mA PP; 1: 12mA OD 2: 4mA PP; 3: 2mA PP		MUX_Q32K 0: Q32K; 1: PWM 2: SPDIF; 3: PLL clock	
		0	0	0	0	0	0	0	0
12h-2	SPDIF	-		-	SPDIF_ COPY_OK	SPDIF_ MCLK_INV	SPDIF_ INVALID	SPDIF_CNTR 0: OFF; 1: 32kS 2: 44.1kS; 3: 48kS	
		0	0	0	0	0	0	0	0
12h-3	PWM	PWM_ INVERTED	PWM_CYCLE 0: no pulses; DytyCycle = PWM_CYCLE * 0.3937%						
		0	0	0	0	0	0	0	0
14h	AudioSet_1	ADC_R_ON	ADC_L_ON	-	LOUT_ON	LIN2_ON	LIN1_ON	-	MIC_ON
		0	0	0	0	0	0	0	0
15h	AudioSet_2	BIAS_OFF	SUM_OFF	AGC_OFF	-		DAC_ON	-	
		0	0	0	0	0	0	0	0
16h	AudioSet_3	LIN1MIX_O FF	LIN2MIX_O FF	MICMIX_O FF	-	DACMIX_O FF	-	IBR_HPH	HPCM_ON
		0	0	0	0	0	0	0	0
17h-1	PMU PVDD1	LDO_PVDD 1_OFF	ILIM_HIGH _PVDD1	PROG_ PVDD1	VSEL_PVDD1 0h – Fh:1.2V+VSEL*50mV (1.2V – 1.95V) 10h – 1Fh: 2.0V+(VSEL-10h)*100mV (2.0V – 3.5V)				
		0	0	0	0	0	0	0	0
17h-2	PMU PVDD2	LDO_PVDD 2_OFF	ILIM_HIGH _PVDD2	PROG_ PVDD2	VSEL_PVDD2 0h – Fh:1.2V+VSEL*50mV (1.2V – 1.95V) 10h – 1Fh: 2.0V+(VSEL-10h)*100mV (2.0V – 3.5V)				
		0	0	0	0	0	0	0	0
17h-3	PMU CVDD1	SKIP_OFF_ CVDD1	PROG_ CVDD1	VSEL_CVDD1 0h: OFF; 1h - 38h .... 0.6V+VSEL*50mV ➔ 0.65V – 3.40V; (38h – 3Fh .... 3.4V)					
		0	0	0	0	0	0	0	0
17h-4	PMU CVDD2	SKIP_OFF_ CVDD2	PROG_ CVDD2	VSEL_CVDD2 0h: OFF; 1h - 38h .... 0.6V+VSEL*50mV ➔ 0.65V – 3.40V; (38h – 3Fh .... 3.4V)					
		0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0
17h-6	PMU Hibernate	-	-	KEEP_ PVDD1			-	KEEP_ CVDD2	KEEP_ CVDD1
		0	0	0	0	0	0	0	0
17h-7	DCDC	-						DCDC3p 0: 3.6V; 1: 3.2V 2: 3.1V; 3: 3.0V	
		0	0	0	0	0	0	0	0
18h	PMU Enable	-	DC_TEST_MUX 0: unused; 1: AVDD; 2: DVDD; 3: PVDD1 4: PVDD2; 5: CVDD1; 6; CVDD2; 7:RVDD			PMU_GATE	PMU_WR_ENABLE 0: unused 1: prog 17h-1 / 12h-1 (PVDD1, OutContr1) 2: prog 17h-2 / 12h-2 (PVDD2, OutContr2) 3: prog 17h-3 / 12h-3 (CVDD1, PWM) 4: prog 17h-4 (CVDD2) 5: unsused 6: prog 17h-6 (Hibernate) 7: prog 17h-7 (DCDC3);		
		0	0	0	0	0	0	0	0
19h	RTC_WakeUp	1st write/read: WAKEUP_BYTE_1							
		128s	64s	32s	16s	8s	4s	2s	1s
		2nd write/read: WAKEUP_BYTE_2							
		32ks	16ks	8ks	4ks	2ks	1ks	512s	256s
		3rd wirte/read: WAKEUP_BYTE_3							
		WAKEUP_ON	4k*1ks	2k*1ks	1k*1Ks	512ks	256ks	128ks	64ks
		4th to 19th write/read: non volatile memory bytes<0:15> (128bit)							
1Ah	MISC	-		-	-	VBUS_COMP_TH 0: 4.5V; 1: 3.18V 2: 1.5V; 3: 0.6V		I2S_ DIRECT	PLL_MODE 0: 16-48kS; 1: 8-12kS
		0	0	0	0	0	0	0	0
1Bh	DCDC15	DIM_UP_ xDOWN	DIM_RATE 0: no dimming; 1: 150ms 2: 300ms; 3: 500ms		I_BACKLIGHT 0 ... OFF 1-30 ... LED current = 1.25mA*I_BACKLIGHT (1.2mA ... 36mA) 31 ... voltage feedback mode				
		0	0	0	0	0	0	0	0

Addr	Name	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
20h	SYSTEM	Design_Version<3:0>				HBT_WD_ON	JTEMP_OFF	I2C_WD_ON	PWR_HOLD
		1	1	0	0	0	0	0	1
21h	SUPERVISOR	BVDD_SUP V_BrownOut = 2..74V+BVDD_SUP*60mV (2.74V .. 3.16V)			JTEMP_SUP Temp_ShutDown = 140C – JTEMP_SUP*5C (+140C..-15C) Temp_IRQ = 120C – JTEMP_SUP*5C (+120C .. -35C)				
		0	0	1	0	0	0	0	0
22h	CHARGER	BAT_TEMP_OFF	CHG_I 0..3: 55, 70, 140, 210mA 4..7: 280, 350, 420, 460mA			CHG_V Vchg=3.9V+50mV*CHG_V (3.9V ... 4.25V)			CHG_OFF
		0	0	0	0	0	0	0	0
23h	IRQ_ENRD_0	CVDD2_EN_SD	CVDD2_EN_IRQ	CVDD1_EN_SD	CVDD1_EN_IRQ	PDD2_EN_SD	PDD2_EN_IRQ	PDD1_EN_SD	PDD1_EN_IRQ
		CVDD2_UNDER	CVDD2_OVER	CVDD1_UNDER	CVDD1_OVER	PDD2_UNDER	PDD2_OVER	PDD1_UNDER	PDD1_OVER
		0	0	0	0	0	0	0	0
24h	IRQ_ENRD_1	SD_TIME 0: 5.4s 1: 10.9s	-	PWRUP_IRQ	WAKEUP_IRQ	-	VOXM_IRQ	-	-
		0	0	0	0	0	0	0	0
25h	IRQ_ENRD_2	BATTEMP_HIGH	-	-	CHG_IRQ	-	USB_IRQ	RVDD_LOW	BVDD_LOW
			CHG_EOC	CHG_CON	CHG_changed	USB_CON	USB_changed		
		0	0	0	0	0	0	0	0
26h	IRQ_ENRD_3	JTEMP_HIGH	-	HP_OVC	I2S_STATUS	I2S_CHANGED		MIC_CONNECT	HPH_CONNECT
		0	0	0	0	0	0	0	0
27h	IRQ_ENRD_4	T_DEB 0: 512ms; 1: 256ms 2: 128ms; 3: 0ms		XIRQ_AH	XIRQ_PP		REM_DET	RTC_UPDATE	ADC_EOC
		0	0	0	0	0	0	0	0
28h	RTC_Cntr	-				-		RTC_ON	OSC32_ON
		0	0	1	0	0	0	1	1
29h	RTC_Time	IRQ_MIN	TRTC<6:0>						
		0	1	0	0	0	0	0	0
2Ah	RTC_0	QRTC<7:0>							
		0	0	0	0	0	0	0	0
2Bh	RTC_1	QRTC<15:8>							
		0	0	0	0	0	0	0	0
2Ch	RTC_2	QRTC<23:16>							
		0	0	0	0	0	0	0	0
2Dh	RTC_3	QRTC<31:24>							
		0	0	0	0	0	0	0	0
2Eh	ADC10_0	ADC10_MUX<3:0> 0: CHGOUT; 1: BVDDR; 2: DC_TEST; 3: CHG_IN; 4:reserved; 5: BatTemp; 6: MICS; 7: reserved; 8: VBE_1uA; 9: VBE_2uA; 10: I_MICS; 11: reserved; 12: VB1V; 13: VBUS; 14, 15: reserved				-	-	ADC10<9:8>	
		0	0	0	0	0	0	X	X
2Fh	ADC10_1	ADC10<7:0>							
		X	X	X	X	X	X	X	X
38-3F	UID_0 .. 7	ID<7:0> ... ID<63:56>							

Table 43 LINE_OUT_R Register

Name		Base		Default
LINE_OUT_R		**2-wire serial**		**00h**
Offset: 00h		**Right Line Output Register** Configures MUX_B and the audio gain from MUX_B output to LOUTR output. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	LO_MUX_B	00	R/W	Multiplexes the analog audio inputs to MUX_B output at LOUTR and at LOUTL **00: SUM Stereo: ΣR to LOUT1R and ΣL to LOUT1L** 01: SUM Mono Differential: ΣR+ ΣL to LOUT1L and -LOUT1L to LOUT1R. The gain of LOUT1R shall be 0dB to hold signals in symmetry 10b = ADC (N9/N18) 11b = DAC (N23/N26)
5		0	n/a	
4:0	LOR_VOL	00000	R/W	volume settings for right line output, adjustable in 32 steps @ 1.5dB; gain from MUX_B to LOUTR 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 44 LINE_OUT_L Register

Name		Base		Default
LINE_OUT_L		**2-wire serial**		**00h**
Offset: 01h		**Left Line Output Register** Configures the audio gain from MUX_B output to LOUTL output and controls MUTE switch J This register is reset when the stage is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	n/a	
6	MUTE_OFF_J	0b	R/W	Control of MUTE switch J **0:line output set to mute** 1: normal operation
5		0	n/a	
4:0	LOL_VOL	00000	R/W	volume settings for left line output, adjustable in 32 steps @ 1.5dB; gain from MUX_B to LOUTL 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 45 HPH_OUT_R Register

Name		Base		Default
HPH_OUT_R		**2-wire serial**		**00h**
Offset: 02h		**Right Headphone Output Register** Configures MUX_C and the audio gain from MUX_C output to HPR output. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	HP_OVC_TO_OFF	00	R/W	Headphone amplifier over current time out. The headphone amplifier is powered down if a over-current is detected. The current thresholds are 150mA at pins HPR / HPL pin or 300mA at pin HPCM (e.g. shorted headphone outputs) 1: 0 ms (no power down) **0: 256 ms**
6:5	HP_MUX_C	00	R/W	00: MUX_C output connected to limiter (N24/N25) 01: MUX_C output connected to DAC (N23/N26) 10: MUX_C output connected to LineIn 1/3 (N10/N17) 11: MUX_C output connected to LineIn 2 (N11/N16)
4:0	HPR_VOL	00000	R/W	volume settings for right headphone output, adjustable in 32 steps @ 1.5dB; gain from MUX_C to HPR output 11111: 1.07 dB gain 11110: -0.43 dB gain .. 00001: -43.93 dB gain **00000: -45.43 dB gain**

Table 46 HPH_OUT_L Register

Name		Base		Default
HPH_OUT_L		**2-wire serial**		**00h**
Offset: 03h		**Left Headphone Output Register** Configures the audio gain from MUX_C output to HPL output and controls MUTE switch K This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MUTE_ON_K	0	R/W	Control of MUTE switch K **0: normal operation** 1: headphone output set to mute (mute is on during power-up)
6	HP_ON	0	R/W	**0: headphone stage not powered** 1: power up headphone stage
5	HPDET_ON	0	R/W	Enables the detection when a headset gets connected. HPCM is used as a sense pin and is biased to 150mV **0: no headphone detection** 1: enable headphone detection
4:0	HPL_VOL	00000	R/W	volume settings for left headphone output, adjustable in 32 steps @ 1.5dB; gain from MUX_C output to HPL output 11111: 1.07 dB gain 11110: -0.43 dB gain .. 00001: -43.93 dB gain **00000: -45.43 dB gain**

Table 47 MIC_R Register

Name		Base		Default
MIC_R		**2-wire serial**		**00h**
Offset: 06h		**Right Microphone Input Register** Configures the gain from microphone amplifier output up to mixer input (Σ). This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MIC_AGC_OFF	0	R/W	Control of limiter AGC (automatic gain control). Limits high dynamic range of electrete/MEMS microphone (e.g. user shouts or blows into microphone) **0: automatic gain control enabled** 1: automatic gain control disabled
6:5	PRE_Gain	00	R/W	Sets the gain of the microphone preamplifier (gain from microphone inputs to N3) **00: gain set to 28 dB** 01: gain set to 34 dB 10: gain set to 40 dB 11: reserved, do not use.
4:0	MR_VOL	00000	R/W	volume settings for right microphone input, adjustable in 32 steps @ 1.5dB; gain from microphone amplifier (N4) to mixer input (N12) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 48 MIC_L Register

Name		Base		Default
MIC_L		**2-wire serial**		**00h**
Offset: 07h		**Left Microphone Input Register** Configures the gain from microphone amplifier output up to mixer input (Σ) and controls MUTE switch D. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MSUP_OFF	0	R/W	**0: microphone supply enabled** 1: microphone supply disabled
6	MUTE_OFF_D	0	R/W	Control of MUTE switch D **0: microphone input set to mute** 1: normal operation
5	RDET_OFF	0	R/W	Disables the microphone detect function (30kOhm pull-up from MICS to AVDD) to use the terminal as ADC-10 input **0: microphone detection enabled** 1: microphone detection disabled
4:0	ML_VOL	00000	R/W	volume settings for left microphone input, adjustable in 32 steps @ 1.5dB; gain from microphone amplifier (N4) to mixer input (N13) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 49 LINE_IN1_R Register

Name		Base		Default
LINE_IN1_R		**2-wire serial**		**00h**
Offset: 0Ah		**Right Line Input 1 Registers** Configures the gain from analog line input pin LIN1R to mixer input (Σ) and controls MUTE switch B. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	n/a	
6	LI_MUX_E	0	R/W	0: MUX_E output connected to Line Input 1 1: MUX_E output connected to Line Input 3
5	MUTE_OFF_B	0	R/W	Control of MUTE switch B **0: right line input is set to mute** 1: normal operation
4:0	LI1R_VOL	00000	R/W	volume settings for right line input 1, adjustable in 32 steps @ 1.5dB; gain from line input pin (LIN1R) to mixer input (N10) 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

Table 50 LINE_IN1_L Register

Name		Base		Default
LINE_IN1_L		**2-wire serial**		**00h**
Offset: 0Bh		**Left Line Input 1 Registers** Configures the gain from analog line input pin LIN1L to mixer input (Σ) and controls MUTE switch G. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	LI1_MODE	00	R/W	Configures Line Input 1 (right and left channel) in accordance with the connected input sources **00: inputs switched to single ended stereo** 01: inputs switched to differential mono 10: inputs switched to single ended mono 11: reserved, do not use.
5	MUTE_OFF_G	0	R/W	Control of MUTE switch G **0: left line input is set to mute** 1: normal operation
4:0	LI1L_VOL	00000	R/W	volume settings for right line input 1, adjustable in 32 steps @ 1.5dB; gain from line input pin (LIN1L) to mixer input (N17) 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

Table 51 LINE_IN2_R Register

Name		Base		Default
LINE_IN2_R		**2-wire serial**		**00h**
Offset: 0Ch		**Right Line Input 2 Register** Configures the gain from analog line input pin LIN2R to mixer input (Σ) and controls MUTE switch C. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6		00	n/a	
5	MUTE_OFF_C	0	R/W	Control of MUTE switch C **0: right line input is set to mute** 1: normal operation
4:0	LI2R_VOL	00000	R/W	volume settings for right line input, adjustable in 32 steps @ 1.5dB; gain from line input pin (LIN2R) to mixer input (N11) 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

Table 52 LINE_IN2_L Register

Name		Base		Default
LINE_IN2_L		**2-wire serial**		**00h**
Offset: 0Dh		**Left Line Input 2 Registers** Configures the gain from analog line input pin LIN2L to mixer input (Σ) and controls MUTE switch F. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	LI2_MODE	00	R/W	Configures Line Input 2 (right and left channel) in accordance with the connected input sources **00: inputs switched to single ended stereo** 01: inputs switched to differential mono 10: inputs switched to single ended mono 11: reserved, do not use.
5	MUTE_OFF_F	0	R/W	Control of MUTE switch F **0: left line input is set to mute** 1: normal operation
4:0	LI2L_VOL	00000	R/W	volume settings for right line input, adjustable in 32 steps @ 1.5dB; gain from line input pin (LIN2L) to mixer input (N16) 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

Table 53 DAC_R Register

Name		Base		Default
DAC_R		**2-wire serial**		**00h**
Offset: 0Eh		**Right DAC Output Registers**		
		Configures the gain from DAC output to mixer input (Σ) / MUX input. This register is reset when the block is disabled in AudioSet2 register (15h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5		000	n/a	
4:0	DAR_VOL	00000	R/W	Volume settings for right DAC output, adjustable in 32 steps @ 1.5dB; gain from DAC output (N19) to mixer/MUX input (N23). 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 54 DAC_L Register

Name		Base		Default
DAC_L		**2-wire serial**		**00h**
Offset: 0Fh		**Left DAC output Registers**		
		Configures the gain from DAC output to mixer input (Σ) / MUX input and controls MUTE switch H. This register is reset when the block is disabled in AudioSet2 register (15h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	n/a	
6	MUTE_OFF_H	0	R/W	Control of MUTE switch H **0: DAC output is set to mute** 1: normal operation
5		0	n/a	
4:0	DAL_VOL	00000	R/W	Volume settings for left DAC output, adjustable in 32 steps @ 1.5dB: gain from DAC output (N22) to mixer/MUX input (N26). 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 55 ADC_R Register

Name		Base		Default
ADC_R		**2-wire serial**		**00h**
Offset: 10h		**Right ADC input Registers** Configures MUX_A and the gain from MUX_A output to the ADC input This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	ADC_MUX_A	00	R/W	Connect MUX A output to following inputs **00: Microphone (N4/N4)** 01: Line_IN1/3 (N1/N8) 10: Line_IN2 (N2/N7) 11: Audio SUM (N24/N25)
5		0	n/a	
4:0	ADR_VOL	00000	R/W	Volume settings for right ADC input, adjustable in 32 steps @ 1.5dB; gain from MUX_A output to ADC input (N9). 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

Table 56 ADC_L Register

Name		Base		Default
ADC_L		**2-wire serial**		**00h**
Offset: 11h		**Left ADC input Registers** Configures the gain from MUX_A output to the ADC input and controls MUTE switch A. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	n/a	
6	MUTE_OFF_A	0	R/W	Control of MUTE switch A **0: ADC input is set to mute** 1: normal operation
5		0	n/a	
4:0	ADL_VOL	00000	R/W	Volume settings for left ADC input, adjustable in 32 steps @ 1.5dB, gain from MUX_A output to ADC input (N18). 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

Table 57 Output Control Register

Name		Base		Default
OutContr		**2-wire serial**		**00h**
Offset: 12h-1		**Q32k and PWGD Output Control Register**		
		Configures PWGD pin (Power Good) and Q32k pin (output of 32kHz oscillator). This is an extended register and needs to be enabled by writing 001b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	DRIVE_PWGD	00	R/W	Enables the PWGD output pin either to open-drain or push-pull and sets various driving strengths **00: 12mA push-pull output** 01: 12mA open-drain output 10: 4mA push-pull output 11: 2mA push-pull output
5:4	MUX_PWGD	00	R/W	Multiplexes various digital signals to the PWGD output pin **00: PowerGood control signal** 01: PWM signal to dim LEDs etc. 10: SPDIF converted from SDI to DAC 11: PLL output clock
3:2	DRIVE_Q32K	00	R/W	Enables the Q32k output pin either to open-drain or push-pull and sets various driving strengths **00: 12mA push-pull output** 01: 12mA open-drain output 10: 4mA push-pull output 11: 2mA push-pull output
1:0	MUX_Q32K	00	R/W	Multiplexes various digital signals to the Q32k output pin 00: **32kHz RTC clock** 01: PWM signal to dim LEDs etc. 10: SPDIF converted from SDI to DAC 11: PLL output clock

Table 58 SPDIF Register

Name		Base		Default
SPDIF		**2-wire serial**		**00h**
Offset: 12h-2		**SPDIF Output Control Register**		
		Adds status bits to the SPDIF bitstream and configures the SPDIF output. This is an extended register and needs to be enabled by writing 010b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5		000	n/a	
4	SPDIF_COPY_OK	0		SPDIF copy control bit **0: copy not permitted** 1: copy permitted
3	SPDIF_MCLK_INV	0		SPDIF master clock control bit **0: master clock** 1: master clock inverted
2	SPDIF_INVALID	0		SPDIF sample status bit **0: sample valid** 1: sample invalid
1:0	SPDIF_CNTR	00	R/W	SPDIF output ON/OFF control and sample rate status bits **00: SPDIF output OFF** 01: SPDIF output ON (32kS) 10: SPDIF output ON (44.1kS) 11: SPDIF output ON (48kS)

Table 59 PWM Register

Name		Base		Default
PWM		**2-wire serial**		**00h**
Offset: 12h-3		**PWM Output Control Register** Sets the PWM output duty cycle and signal polarity. This is an extended register and needs to be enabled by writing 011b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PWM_INVERTED	0	R/W	PWM output polarity **0: not inverted** 1: inverted
6:0	PWM_CYCLE	0000000	R/W	Sets the PWM duty cycle Duty Cycle = PWM_CYCLE * 0.3937% **PWM_CYCLE = 0 means no pulse**

Table 60 AudioSet_1 Register

Name		Base		Default
AudioSet_1		**2-wire serial**		**00h**
Offset: 14h		**First Audio Set Register** Powers the various audio inputs and outputs UP or DOWN. **Attention:** This control register resets and holds microphone, line out, and ADC related registers in reset. After activation the required register settings need to be re-programmed. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ADC_R_ON	0	R/W	**0: ADC right channel powered down** 1: ADC right channel enabled for recording
6	ADC_L_ON	0	R/W	**0: ADC left channel powered down** 1: ADC left channel enabled for recording
5		0	n/a	
4	LOUT_ON	0	R/W	**0: Line output powered down** 1: Line output enabled
3	LIN2_ON	0	R/W	**0: Line input 2 powered down** 1: Line input 2 enabled
2	LIN1_ON	0	R/W	**0: Line input 1 powered down** 1: Line input 1 enabled
1		0	n/a	
0	MIC_ON	0	R/W	**0: Microphone input powered down** 1: Microphone input 1 enabled

Table 61 AudioSet_2 Register

Name		Base		Default
AudioSet_2		**2-wire serial**		**00h**
Offset: 15h		**Second Audio Set Register**		
		Powers various internal audio blocks UP or DOWN and controls bias current. **Attention:** This control register resets and holds DAC related registers in reset. After activation the required register settings need to be re-programmed. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BIAS_OFF	0	R/W	Power-down of the AGND bias. This bit can be set, if the AFE is used for digital data transfer and PMU functions only and all the analog audio blocks are not used. **0: bias enabled** 1: bias disabled, for power saving in non audio mode
6	SUM_OFF	0	R/W	Power-down of ΣR and ΣL **0: Mixer stage enabled (limits output signal to 1Vp)** 1: Mixer stage powered down
5	AGC_OFF	0	R/W	Switches the signal limiter OFF (N20/N21) **0: automatic gain control for summing stage enabled** 1: automatic gain control for summing stage disabled
4:3		00	n/a	
2	DAC_ON	0	R/W	**0: DAC powered down** 1: DAC enabled
1:0		00	n/a	

Table 62 AudioSet_3 Register

Name		Base		Default
AudioSet_3		**2-wire serial**		**00h**
Offset: 16h		**Third Audio Set Register** Sets headphone output bias currents and operation modes and enables audio signal inputs to ΣR and ΣL. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LIN1MIX_OFF	0	R/W	Input from line input 1 to ΣR and ΣL **0: ON** 1: OFF
6	LIN2MIX_OFF	0	R/W	Input from line input 2 to ΣR and ΣL **0: ON** 1: OFF
5	MICMIX_OFF	0	R/W	Input from microphone 1 to ΣR and ΣL **0: ON** 1: OFF
4		0	n/a	
3	DACMIX_OFF	0	R/W	Input from DAC to ΣR and ΣL **0: ON** 1: OFF
2		0	n/a	
1	IBR_HPH	0	R/W	Bias current increase for the headphone amplifier depending on load conditions **0: 100%** 1: 150%
0	HPCM_ON	0	R/W	Power-up of the headphone common mode buffer: **0: headphone CM buffer is switched off** 1: headphone CM buffer is switched on

Table 63 PMU PVDD1 Register

Name		Base		Default
PMU PVDD1		**2-wire serial**		**00h**
Offset: 17h-1		**PVDD1 Low Drop-Out Regulator (LDO3) Control Register** This is an extended register and needs to be enabled by writing 001b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LDO_PVDD1_OFF	0	R/W	Power-down of LDO for PVDD1 **0: PVDD1 (LDO3) enable** 1: PVDD1 (LDO3) power-down
6	ILIM_HIGH_PVDD1	0	R/W	Sets the current limit for PVDD1 **0: 200mA current limit** 1: 350mA current limit
5	PROG_PVDD1	0	R/W	Enables settings either selected by external pin (VPRG1) or settings stored in the 17h-1 register **0: VPRG1 pin controlled** 1: Register controlled
4:0	VSEL_PVDD1	00000	R/W	The voltage select bits set the LDO output in 2 different resolution ranges Range: 00h until 0Fh in 50mV steps PVDD1=1.2V+VSEL_PVDD1*50mV (**1.2V** until 1.95V) Range: 10h until 1Fh in 100mV steps PVDD1=2.0V+VSEL_PVDD1*100mV (2.0V until 3.5V)

Table 64 PMU PVDD2 Register

Name		Base		Default
PMU PVDD2		**2-wire serial**		**00h**
Offset: 17h-2		**PVDD2 Low Drop-Out Regulator (LDO4) Control Register** This is an extended register and needs to be enabled by writing 010b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LDO_PVDD2_OFF	0	R/W	Power-down of LDO for PVDD2 **0: PVDD2 (LDO4) enable** 1: PVDD2 (LDO4) power-down
6	ILIM_HIGH_PVDD2	0	R/W	Sets the current limit for PVDD2 **0: 200mA current limit** 1: 350mA current limit
5	PROG_PVDD2	0	R/W	Enables settings either selected by external pin (VPRG1) or settings stored in the 17h-2 register **0: VPRG1 pin controlled** 1: Register controlled
4:0	VSEL_PVDD2	00000	R/W	The voltage select bits set the LDO output in 2 different resolution ranges Range: 00h until 0Fh in 50mV steps PVDD2=1.2V+VSEL_PVDD1*50mV (**1.2V** until 1.95V) Range: 10h until 1Fh in 100mV steps PVDD2=2.0V+VSEL_PVDD1*100mV (2.0V until 3.5V)

Table 65 PMU CVDD1 Register

Name		Base		Default
PMU CVDD1		**2-wire serial**		**00h**
Offset: 17h-3		**CVDD1 DC/DC Buck Regulator Control Register** This is an extended register and needs to be enabled by writing 011b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	SKIP_OFF_CVDD1	0	R/W	Disables pulse skip mode **0: 170mA current force / pulse skip mode enabled** 1: current force / pulse skip mode disabled (only ON without load)
6	PROG_CVDD1	0	R/W	Enables settings either selected by external pin (VPRG1) or settings stored in the 17h-3 register **0: VPRG1 pin controlled** 1: Register controlled
5:0	VSEL_CVDD1	00000	R/W	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00000: DC/DC powered down** 01h until 38h in 50mV steps CVDD1=0.6V+VSEL_CVDD1*50mV (0.65V until 3.4V) 38h until 3Fh = 3.4V (no change)

Table 66 PMU CVDD2 Register

Name		Base		Default
PMU CVDD2		**2-wire serial**		**0x00**
Offset: 17h-4		**CVDD2 DC/DC Buck Regulator Control Register**		
		This is an extended register and needs to be enabled by writing 100bto Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	SKIP_OFF_CVDD2	0	R/W	Disables pulse skip mode **0: 170mA current force / pulse skip mode enabled** 1: current force / pulse skip mode disabled (only ON without load)
6	PROG_CVDD2	0	R/W	Enables settings either selected by external pin (VPRG1) or settings stored in the 17h-4 register **0: VPRG1 pin controlled** 1: Register controlled
5:0	VSEL_CVDD2	00000	R/W	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00000b: DC/DC powered down** 01h until 38h in 50mV steps CVDD2=0.6V+VSEL_CVDD1*50mV (0.65V until 3.4V) 38h until 3Fh = 3.4V (no change)

Table 67 PMU Hibernate Register

Name		Base		Default
PMU Hibernate		**2-wire serial**		**00h**
Offset: 17h-6		**PMU Hibernation Control Register (PVDD1, CVDD1/2)**		
		Hibernation is started when writing to this register. This is an extended register and needs to be enabled by writing 110b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6		0	n/a	
5	KEEP_PVDD1	0	R/W	Keeps the programmed PVDD1 level during hibernation **0: power down PVDD1** 1: keep PVDD1
4:2		0	n/a	
1	KEEP_CVDD2	0	R/W	Keeps the programmed CVDD2 level during hibernation **0: power down CVDD2** 1: keep CVDD2
0	KEEP_CVDD1	0	R/W	Keeps the programmed CVDD1 level during hibernation **0: power down CVDD1** 1: keep CVDD1

Table 68 PMU DCDC 3V Register

Name		Base		Default
PMU Hibernate		**2-wire serial**		**00h**
Offset: 17h-7		**BVDD DC/DC Boost Regulator Control Register** This is an extended register and needs to be enabled by writing 111b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2		0	n/a	
1:0	DCDC3p	00	R/W	DCDC 3V output voltage programming (BVDD) **00: 3.6V** 01: 3.2V 10: 3.1V 11: 3.0V

Table 69 PMU ENABLE Register

Name		Base		Default
PMU ENABLE		**2-wire serial**		**00h**
Offset: 18h		**PMU Extension Enable Register** Enables 12h and 17h to write into extended registers and allows multiplexing supply voltages for monitoring via ADC10. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	n/a	
6:4	DC_TEST	000	R/W	Allows multiplexing internal and external supply voltages to one DC test node which can be further multiplexed to ADC10. The accuracy is 5mV/LSB (see reg. 2Eh) 000: not used 001: AVDD 010: DVDD 011: PVDD1 100: PVDD2 101: CVDD1 110: CVDD2 111: RVDD
3	PMU_GATE	0	R/W	Enables all settings made in registers 0x17-x at once. If this bit is set, changes are activated as soon as they are written to the related register. **0: no change** 1: change at once
0:2	PMU_WR_ENABLE	000	R/W	Enables extended registers 12h-x and 17h-x **000: not used** 001: enables 17h-1 for PVDD1 settings enables 12h-1 for OutCntr settings 010: enables 17h-2 for PVDD2 settings enables 12h-2 for SPDIF settings 011: enables 17h-3 for CVDD1 settings enables 12h-3 for PWM_Cntr settings 100: enables 17h-4 for CVDD2 settings 101: not used 110: enables 17h-6 for hibernation settings 111: enables 17h-7 for BVDD settings

Table 70 RTC_WakeUp Register

Name		Base		Default
RTC_WakeUp		**2-wire serial**		**n/a**
Offset: 19h		**RTC Wake-Up and SRAM Register** Sets and enables the RTC wake-up counter and programs the 128bit SRAM. 3 bytes need to be written in a sequence to set the counter. The 3-byte sequence allows to set the counter to every value between 1sec and 8388608sec (=97 days). The MSB of the 3rd byte enables the wake-up counter. Byte 4 ...19 will program the static 128bit SRAM which is supplied by RVDD. This register is reset at a RVDD-POR.		
Adr.	**Byte Name**	**Default**	**Access**	**Bit Description**
7:0	WAKE_UP_BYTE0 (1st write to 0x19 is byte 0)	00h	R/W	0000 0001: 1sec 0000 0010: 2sec 0000 0100: 4sec 0000 1000: 8sec 0001 0000: 16sec 0010 0000: 32sec 0100 0000: 64sec 1000 0000: 128sec
7:0	WAKE_UP_BYTE1 (2nd write to 0x19 is byte 1)	00h	R/W	0000 0001: 256sec 0000 0010: 512sec 0000 0100: 1 024sec 0000 1000: 2 048sec 0001 0000: 4 096sec 0010 0000: 8 192sec 0100 0000: 16 384sec 1000 0000: 32 768sec
7:0	WAKE_UP_BYTE2 (3rd write to 0x19 is byte 2)	00h	R/W	000 0001: 65 536sec 000 0010: 131 072sec 000 0100: 262 144sec 000 1000: 524 288sec 001 0000: 1 048 576sec 010 0000: 2 097 152sec 100 0000: 4 194 304sec 0xxx xxxxxb = wake-up disabled 1xxx xxxxxb = wake-up enabled
7:0	SRAM_128 (4th ... 19th write to 0x19 programs the 128bit static SRAM)	00000000	R/W	xxxx xxxxb = byte 4 : xxxx xxxxb = byte 19

Table 71 USB_UTIL Register

Name		Base		Default
MISC		2-wire serial		00h
Offset: 1Ah		Miscellaneous Register		
		Comparator settings to read back VBUS voltage levels for supporting USB OTG and USB Host protocols. I2S mode settings This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4:7		0000	n/a	
3:2	VBUS_COMP_TH	00	R/W	Sets the threshold for the VBUS comparator. The output can be read in register 25h. **00: 4.5V** 01: 3.18V 10: 1.5V 11: 0.6V
1	I2S_DIRECT	0	R/W	Switches the PWGD pin to an input for an external master clock (e.g. coming form the CPU). This bit overwrites prior setting for the PWGD pin. **0: disabled** 1: enabled
0	PLL_MODE	0	R/W	Preset of PLL bias for the following sampling frequencies **0: 16-48kS** 1: 8-12kS

Table 72 DCDC15 Register

Name		Base		Default
DCDC15		2-wire serial		00h
Offset: 1Bh		15V DCDC Step-up Control Register		
		Controls the back-light current and back-light dim rate. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	DIM_UP_xDOWN	0	R/W	Starts dimming UP/DOWN or switches LED back-light ON/OFF when DIM_RATE = 00b **0: dim DOWN** 1: dim UP
6:5	DIM_RATE	00	R/W	Sets the dim rate of the LED back-light current from 0mA to I_BACKLIGHT and vice versa **00: no dimming (immediate ON/OFF)** 01: 150ms 10: 300ms 11: 500ms
4:0	I_BACKLIGHT	00000	R/W	Sets the current into pin ISINK in 1.20mA steps (internal current source to control LED backlight current). Setting 11111b enables the voltage feedback mode to supply e.g. OLEDs with a constant voltage supply. **00000: DCDC15 switched off** 00001: 1.2mA 00010: 2.4mA .. 11110: 36mA 11111: voltage feedback mode

Table 73 System Register

Name		Base		Default
System		2-wire serial		C1h
Offset: 20h		System Settings Register Controls the powering down conditions of the AFE. The IC can also be emergency shut down by a high level for 5.4sec (or 10.9sec see reg. 24h) at the PWRUP input pin This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Version <3:0>	1100	R	AFE number to identify the design version **1011: revision 4**
3	HBT_WD_ON	0	R/W	Heartbeat (HBT) Watchdog The watchdog counter will be reset by a rising edge at the HBT input pin which has to occur at least every 500ms. If the watchdog counter is not reset, the AFE will be powered down. **0: HBT watchdog is disabled** 1: HBT watchdog is enabled
2	JTEMP_OFF	0	R/W	Junction temperature supervision (level can be set in register 21h) **0: temperature supervision enabled** 1: temperature supervision disabled
1	I2C_WD_ON	0	R/W	2-wire serial interface watchdog To reset the watchdog counter a 2-wire serial read operation has to be performed at least every 500ms. If the watchdog counter is not reset, the AFE will be powered down. **0: watchdog is disabled** 1: watchdog is enabled
0	PWR_HOLD	1	R/W	0: power up hold is cleared and AFE will power down **1: is automatically set to on after power on**

Table 74 Supervisor Register

Name		Base		Default
SUPERVISOR		2-wire serial		00h
Offset: 21h		Supervisor Register Sets the threshold levels of battery supply and junction temperature supervision. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	BVDD_SUP<2:0>	000	R/W	Sets the threshold (brown-out voltage) at the BVDD input pin for an interrupt at low battery condition V_BrownOut=2.74+BVDD_Sup*60mV **000: 2.74V** 001: 2.80V ... 110: 3.10V 111: 3.16V
4:0	JTEMP_SUP<4:0>	00000	R/W	Sets the threshold for junction temperature emergency shutdown and junction temperature interrupt Invoke shutdown at: JTemp_SD=140-JTEMP_Sup*5°C Invoke interrupt at: JTemp_IRQ=120-JTEMP_Sup*5°C JT_Sup | IRQ | Shutdown **00000 | 120°C | 140°C** 00001 | 115°C | 135°C . | . | . . | . | . 11110 | -30°C | -10°C 11111 | -35°C | -15°C

Table 75 Charger Register

Name		Base		Default
CHARGER		**2-wire serial**		**00h**
Offset: 22h		**Charger Control Register** Sets the charging current, end of charge voltage and battery temp. supervision. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BAT_TEMP_OFF	0	R/W	**0: enables 15uA supply for external 100k NTC resistor** 1: disables supply
6:4	CHG_I	000	R/W	set maximum charging current 111: 460 mA 110: 420 mA 101: 350 mA 100: 280 mA 011: 210 mA 010: 140 mA 001: 70 mA **000: 55 mA**
3:1	CHG_V	000	R/W	set maximum charger voltage in 50mV steps 111: 4.25 V 110: 4.2 V .. 001: 3.95 V **000: 3.9 V**
0	CHG_OFF	0	R/W	**0: enables Charger** 1: disables Charger

Table 76 First Interrupt Register

Name		Base		Default
IRQ_ENRD_0		2-wire serial		00h
Offset: 23h		First Interrupt Register Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	CVDD2_EN_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at CVDD2 occurs **0: disable** 1: enable
	CVDD2_UNDER	x	R	This bit is set when a –5% under-voltage at CVDD1 occurs
6	CVDD2_EN_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of CVDD2 **0: disable** 1: enable
	CVDD2_OVER	x	R	This bit is set when a +8% over-voltage at CVDD1 occurs
5	CVDD1_EN_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at CVDD1 occurs **0: disable** 1: enable
	CVDD1_UNDER	x	R	This bit is set when a –5% under-voltage at CVDD1 occurs
4	CVDD1_EN_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of CVDD1 **0: disable** 1: enable
	CVDD1_OVER	x	R	This bit is set when a +8% over-voltage at CVDD1 occurs
3	PVDD2_EN_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at PVDD2 occurs **0: disable** 1: enable
	PVDD2_UNDER	x	R	This bit is set when a –5% under-voltage at PVDD2 occurs
2	PVDD2_EN_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of PVDD2 **0: disable** 1: enable
	PVDD2_OVER	x	R	This bit is set when a +5% over-voltage at PVDD2 occurs
1	PVDD1_EN_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at PVDD1 occurs **0: disable** 1: enable
	PVDD1_UNDER	x	R	This bit is set when a –5% under-voltage at PVDD1 occurs
0	PVDD1_EN_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of PVDD1 **0: disable** 1: enable
	PVDD1_OVER	x	R	This bit is set when a +5% over-voltage at PVDD1 occurs

Table 77 Second Interrupt Register

Name		Base		Default
IRQ_ENRD_1		2-wire serial		00h
Offset: 24h		Second Interrupt Register		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	SD_TIME_5	0	R/W	Control bit which sets the emergency shut-down time from 5.4sec to 10.9sec. The shut-down of AS3518 is invoked by a high signal at the PWRUP input pin. 0: 5.4sec 1: 10.9sec
6		0	n/a	
5	PWRUP_IRQ	0	W	Enables interrupt which is invoked whenever a high signal at the PWRUP input pin occurs 0: disable 1: enable
		x	R	This bit is set whenever a high level of min. BVDD/3 at the PWRUP input pin occurs (PWRUP pin is commonly connected to the power-up button)
4	WAKEUP_IRQ	0	W	Enables interrupt which is invoked whenever a wake-up from RTC wake-up counter occurs 0: disable 1: enable
		X	R	This bit is set when a wake-up has been invoked by the RTC wake-up counter.
3		0	n/a	
2	VOXM_IRQ	0	W	Enables interrupt which is invoked by reaching a voltage threshold at the MIC input (voice activation) 0: disable 1: enable
		x	R	This bit is set when a voltage threshold of 5mV$_{RMS}$ (unfiltered) at the MIC has been reached (voice activation)
0:1		00	n/a	

Table 78 Third Interrupt Register

Name		Base		Default
IRQ_ENRD_2		2-wire serial		00h
Offset: 25h		Third Interrupt Register Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BATTEMP_HIGH (level)	0	W	Battery over-temperature interrupt setting. **0: disable** 1: enable interrupt if battery temperature exceeds 45°C The interrupt must not be enabled if the charger block and battery temperature supervision is disabled
		x	R	Battery over-temperature interrupt reading 0: battery temperature below 45°C 1: battery temperature was too high and the charger was turned off. The charger will be turned on again, when the temperature gets below 42°C
6	CHG_EOC	x	R	Battery end of charge interrupt reading 0: battery charging in progress 1: charging is complete, charging current is below 10% of nominal current, turn off charger
5	CHG_CON	x	R	0: no charger input source connected 1: charger input source connected, also valid if charger is connected during wakeup
4	CHG_CHANGED (status change)	0	W	Charger status change interrupt setting **0: disable** 1: enables an interrupt on a low to high or high to low change of CHGIN pin or on an EOC condition
		x	R	Charger input status change interrupt reading 0: charger status not changed 1: charger status changed, check CHG_CON and CHG_EOC
3	USB_CON	x	R	0: no USB input connected 1: USB input connected, also valid if USB is connected during wakeup. The threshold can be set in the USB_UTIL register (1Ah)
2	USB_CHANGED (status change)	0	W	USB input status change interrupt setting **0: disable** 1: enables an interrupt on a low to high or high to low change of VBUS pin. The threshold can be set in the USB_UTIL register (1Ah)
		x	R	USB input status change interrupt reading 0: USB input status not changed 1: USB input status changed, check USB_CON

1	RVDD_LOW (level)	0	W	Real time clock supply (RVDD) under-voltage interrupt setting **0: disable** 1: enable
		x	R	Real time clock supply interrupt reading **0: RTC supply o.k.** 1: RTC supply (RVDD) was low, RTC not longer valid The interrupt gets set in hibernation or during power-up even if the interrupt is not enabled thus allowing to recognise a change of the battery connected to BVDDR during hibernation or shutdown. For a valid reading, the interrupt has to be enabled first.
0	BVDD_LOW (level)	0	W	BVDD under-voltage supervisor interrupt setting **0: disable** 1: enable
		x	R	BVDD supervisor interrupt setting 0: BVDD is above brown out level 1: BVDD has reached brown out level The threshold can be set in the SUPERVISOR register (21h)

Table 79 Fourth Interrupt Register

Name		**Base**		**Default**
IRQ_ENRD_3		**2-wire serial**		**0x00**
Offset: 0x26		**Fourth Interrupt Register** Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	JTEMP_HIGH (level)	0	W	Supervisor junction over-temperature interrupt setting **0: disable** 1: enable
		x	R	Supervisor junction over-temperature interrupt reading 0: chip temperature below threshold 1: chip temperature has reached the threshold The threshold can be set in the SUPERVISOR register (21h)
6		0	n/a	
5	HP_OVC (level)	0	W	Headphone over-current interrupt setting **0: disable** 1: enable The interrupt must not be enabled if the headphone block is disabled
		x	R	Headphone over-current interrupt reading 0: no over-current detected 1: headphone over-current detected, headphone amplifier was shut down. The current thresholds are 150mA at HPR / HPL pin or 300mA at HPCM pin. The shut-down time can be set in HPH_OUT_R register (0x02)
4	I2S_status	x	R	0: no LRCK on I2S interface detected 1: LRCK on I2S interface present
3	I2S_changed (status change)	0	W	I2S input status change interrupt setting **0: disable** 1: enable
		x	R	I2S input status change interrupt reading 0: I2S input status not changed 1: I2S input status changed, check I2S_status
2		0	n/a	

Name		Base	Default
IRQ_ENRD_3		2-wire serial	0x00
Offset: 0x26		Fourth Interrupt Register Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.	

Bit	Bit Name	Default	Access	Bit Description
1	MIC_CONNECT (level)	0	W	Microphone connect detection interrupt setting **0: disable** 1: enable
		x	R	Microphone connect detection interrupt reading 0: no microphone connected to MIC input 1: microphone connected at MIC input. This interrupt is only invoked when the microphone stage is powered down. The IRQ will be released after enabling the microphone stage. Detecting a microphone during operation has to be done by measuring the supply current.
0	HPH_CONNECT (level)	0	W	Headphone connect detection interrupt setting **0: disable** 1: enable
		x	R	Headphone connect detection interrupt reading 0: no headphone connected 1: headphone connected This interrupt is only invoked when the headphone stage is powered down. The IRQ will be released after enabling the headphone stage. Detecting a headphone during operation is not possible.

Table 80 Fifth Interupt Register

Name		Base		Default
IRQ_ENRD_4		2-wire serial		0x00
Offset: 0x27		Fifth Interrupt Register		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	T_DEB<1:0>	00	R/W	Sets the USB and Charger connect de-bounce time: **00: 512ms** 01: 256ms 10: 128ms 11: 0ms
5	XIRQ_AH	0	R/W	Sets the active output state of the XIRQ line: **0: IRQ is active low** 1: IRQ is active high
4	XIRQ_PP	0	R/W	Sets the XIRQ output buffer type: **0: IRQ output is open drain** 1: IRQ output is push pull
3		0	n/a	
2	REM_DET (edge)	0	W	Microphone remote key press detection interrupt setting **0: disable** 1: enable
		x	R	Microphone remote key press detection interrupt reading 0: no key press detected 1: Microphone supply current got increased, remote key press detected -> measure MICS supply current
1	RTC_UPDATE (edge)	0	W	RTC timer interrupt setting **0: disable** 1: enable
		x	R	RTC timer interrupt reading 0: no RTC interrupt occurred 1: RTC timer interrupt occurred. Selecting minute or second interrupt can be done via RTCT register (29h)
0	ADC_EOC (edge)	0	W	ADC end of conversion interrupt setting **0: disable** 1: enable
		x	R	ADC end of conversion interrupt reading 0: ADC conversion not finished 1: ADC conversion finished. Read out ADC_0 and ADC_1 register to get the result (2Eh & 2Fh)

Table 81 RTC_Cntr Register

Name		Base		Default
RTC_Cntr		**2-wire serial**		**03h**
Offset: 28h		**RTC Control Register**		
		This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2		000000	n/a	
1	RTC_ON	1	R/W	RTC counter clock control: 0: Disable clock for RTC counter **1: Enables clock for RTC counter**
0	OSC_ON	1	RW	RTC oscillator control: 0: Disable RTC oscillator **1: Enable RTC oscillator**

Table 82 RTC_Time Register

Name		Base		Default
RTC_Time		**2-wire serial**		**40h**
Offset: 29h		**RTC Timing Register**		
		This register is reset at a RVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	IRQ_MIN	0	R/W	**0: generates an interrupt every second** 1: generates an interrupt every minute The interrupt has to be enable in IRQ_ENRD_4 (27h)
6:0	RTC_TBC<6:0>	1000000	R/W	These bits are used to correct the inaccuracy of the used 32kHz crystal. Trimming register for RTC, 128 steps @ 7.6ppm 000000: 1 (7.6ppm) 000001: 2 (15.2ppm) ... **100000: 64 (488ppm)** ... 111110: 126 (960.8ppm) 111111: 127 (968.4ppm)

Table 83 RTC_0 to RTC_3 Register

Name		Base		Default
RTC_0 to RTC_3		**2-wire serial**		**00 00 00 00h**
Offset: 2Ah to 2Dh		**RTC Time-base Seconds Register**		
		This register is reset at a RVDD-POR.		
Adr.	**Byte Name**	**Default**	**Access**	**Bit Description**
2Ah	RTC_0	00h	R/W	QRTC<7:0>; RTC seconds bits 0 to 7
2Bh	RTC_1	00h	R/W	QRTC<15:8>; RTC seconds bits 8 to 15
2Ch	RTC_2	00h	R/W	QRTC<23:9>; RTC seconds bits 9 to 23
2Dh	RTC_3	00h	R/W	QRTC<31:24>; RTC seconds bits 24 to 31

Table 84 ADC10_0 Register

Name		Base		Default
ADC10_0		**2-wire serial**		**0000 00xx**
Offset: 2Eh		**First 10-bit ADC Register** Writing to this register will start the measurement of the selected source. This register is reset at a DVDD-POR, exception are bit 8 and 9.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	ADC10_MUX	00000000	R/W	Selects ADC input source **0000: CHGOUT** 0001: BVDDR 0010: defined by DC_TEST in register 0x18 0011: CHGIN 0100: reserved 0101: BatTemp 0110: MICS 0111: reserved 1000: VBE_1uA 1001: VBE_2uA 1010: I_MICS 1011: reserved 1100: VB1V 1101: VBUS 1110: reserved 1101: reserved
3:2		00	n/a	
1:0	ADC10<9:8>	xx	R/W	ADC result bit 9 to 8

Table 85 ADC10_1 Register

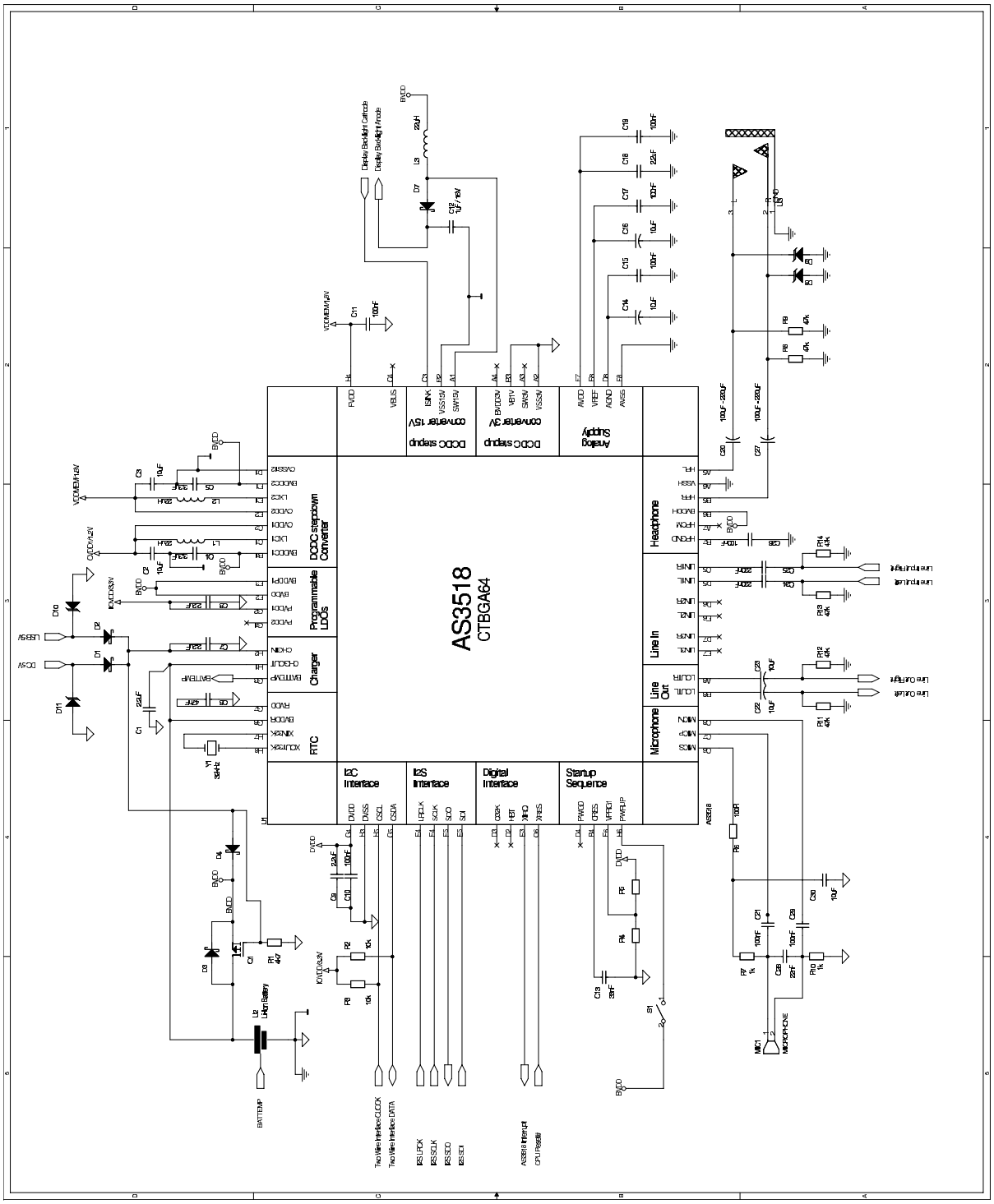
Name		Base		Default
ADC10_1		**2-wire serial**		**xxxx xxxx**
Offset: 2Fh		**Second 10-bit ADC Register** This register is not reset.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ADC10<7:0>	xxxx xxxx	R/W	ADC result bit 7 to 0

Table 86 UID_0 to UID_7 Register

Name		Base		Default
UID_0 to UID_7		**2-wire serial**		**n/a**
Offset: 38h to 3Fh		**Unique ID Register** This register is read only and is not reset.		
Adr.	**Byte Name**	**Default**	**Access**	**Bit Description**
38h	UID_0	n/a	R	Unique ID byte 0
39h	UID_1	n/a	R	Unique ID byte 1
3Ah	UID_2	n/a	R	Unique ID byte 2
3Bh	UID_3	n/a	R	Unique ID byte 3
3Ch	UID_4	n/a	R	Unique ID byte 4
3Dh	UID_5	n/a	R	Unique ID byte 5
3Eh	UID_6	n/a	R	Unique ID byte 6
3Fh	UID_7	n/a	R	Unique ID byte 7

9 Application Information

Figure 31 Typical Application Schematic



10 Package Drawings and Marking

10.1 CTBGA64

Figure 32 CTBGA64 Marking

Table 87 Package Code AYWWZZZ

A	Y	WW	ZZZ
A ... for PB free	Year	Working week assembly/packaging	Free choice

Figure 33 CTBGA64 7x7mm 0.8mm pitch

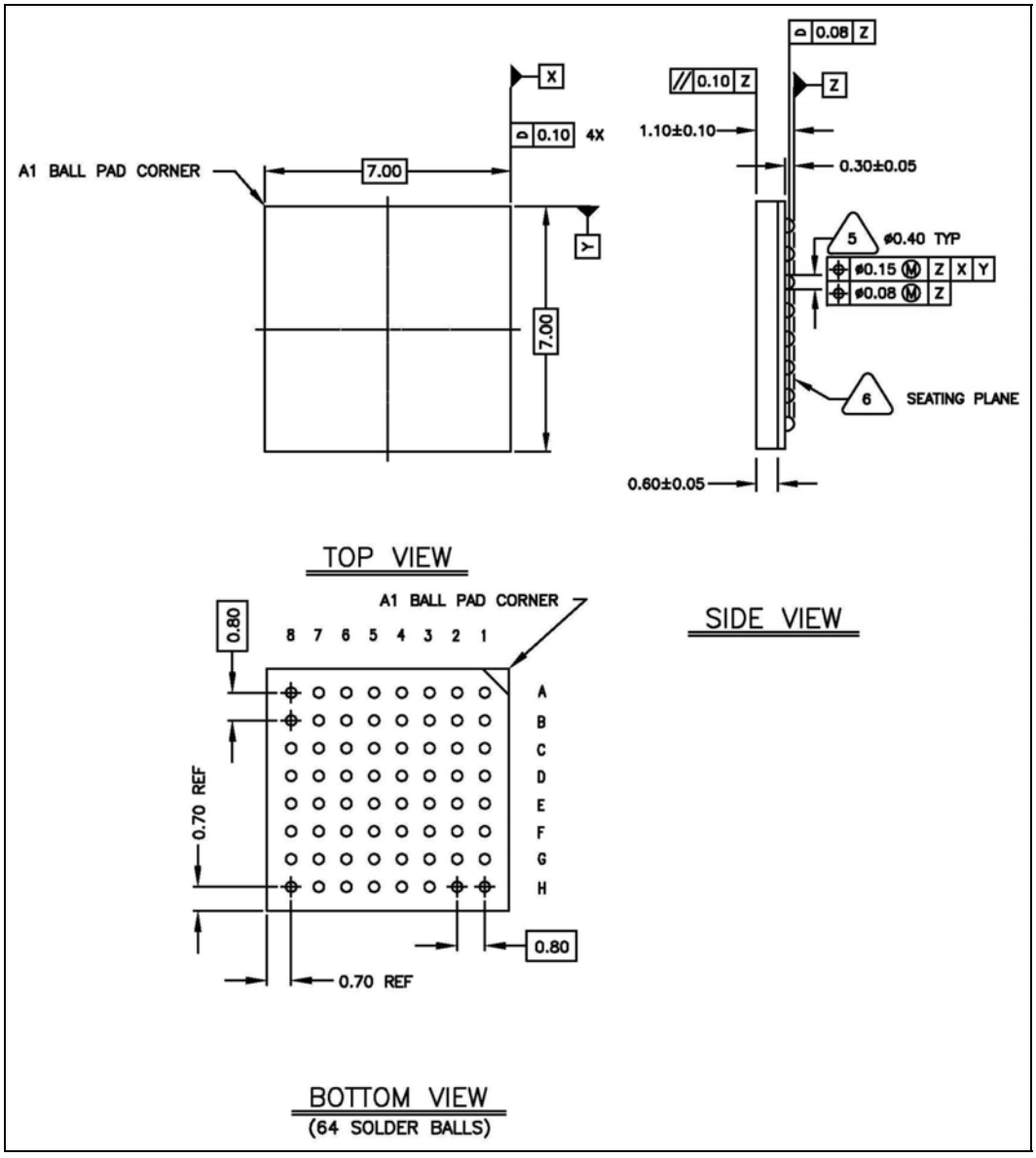


Figure 34 Reel Specification

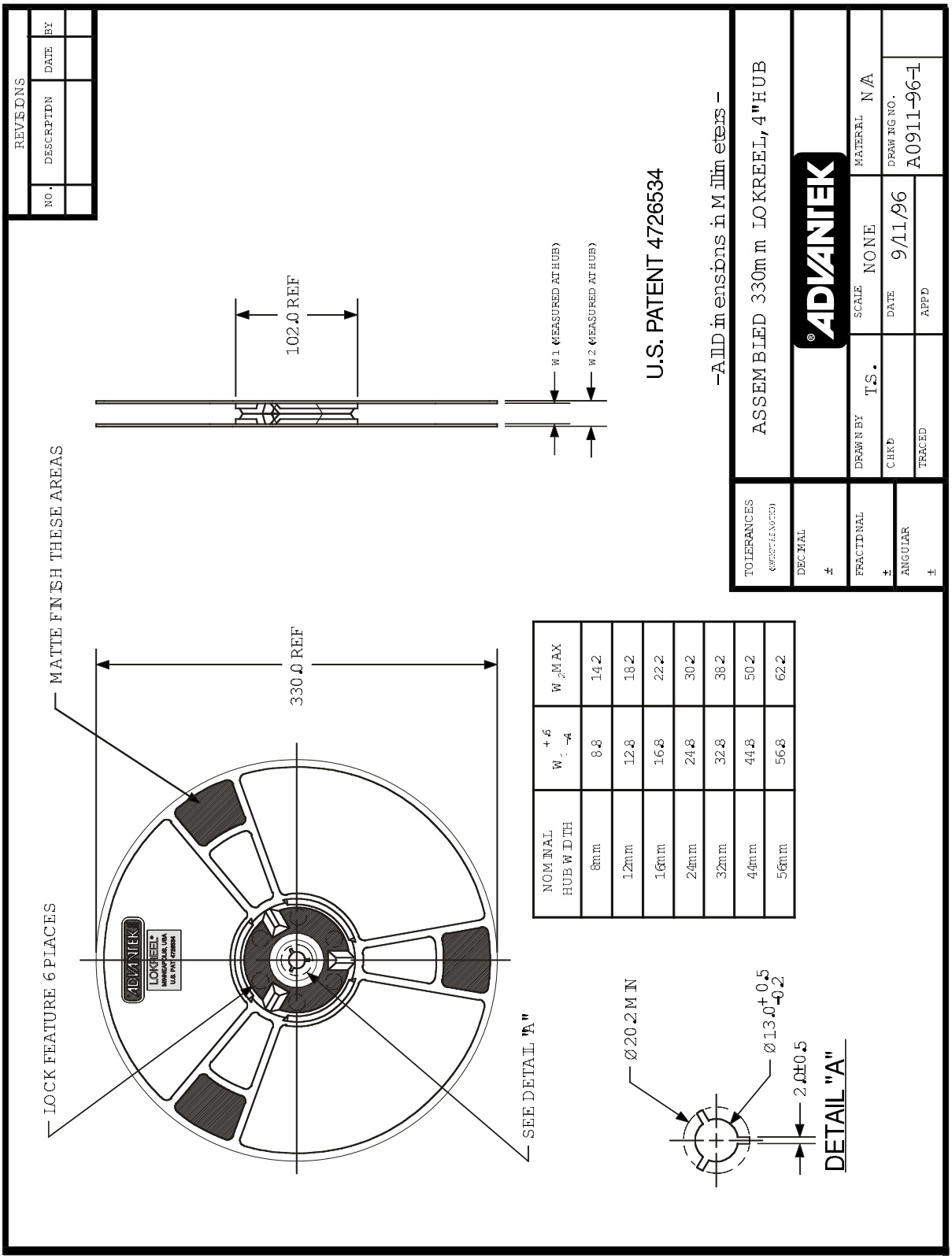
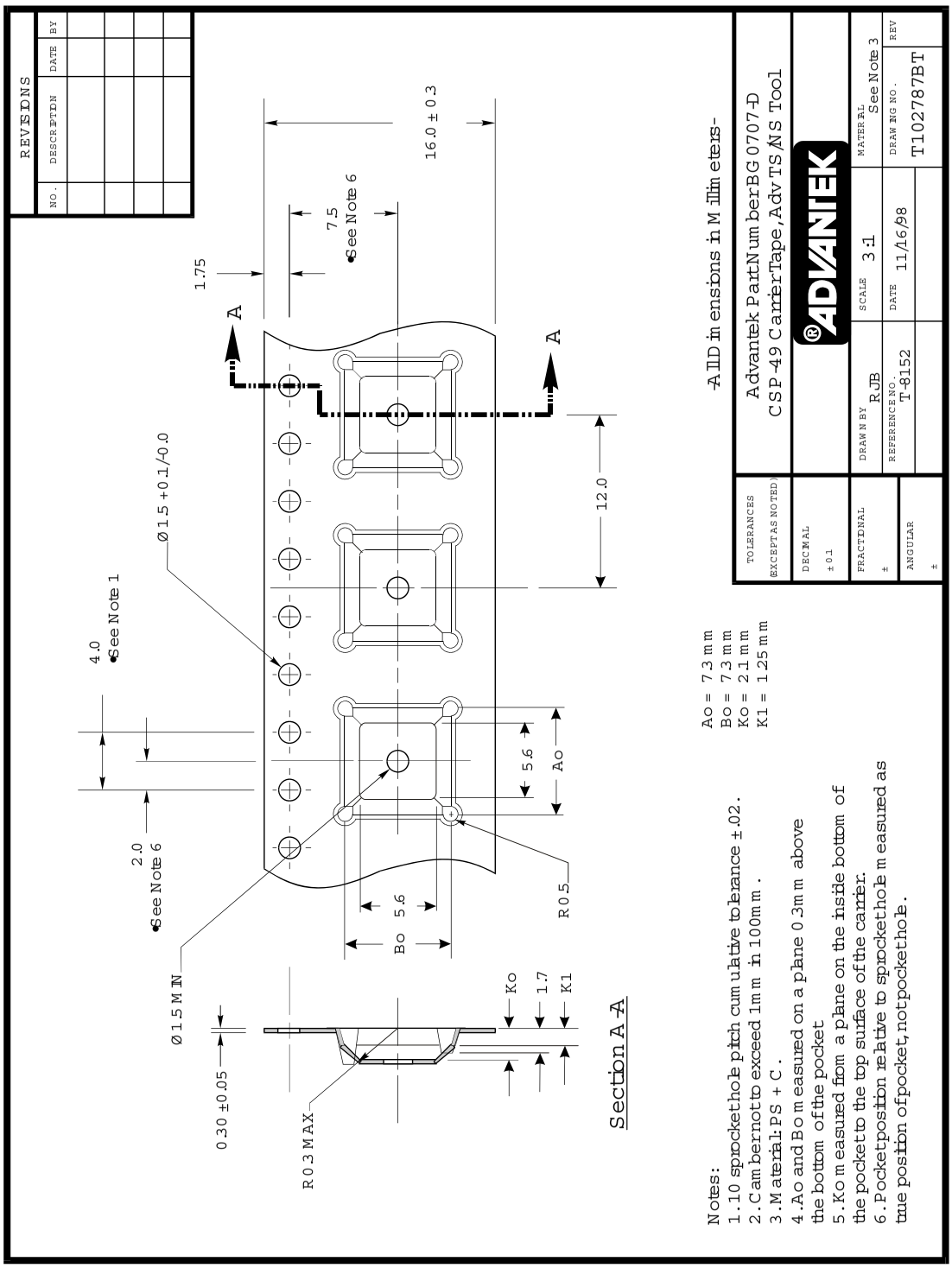
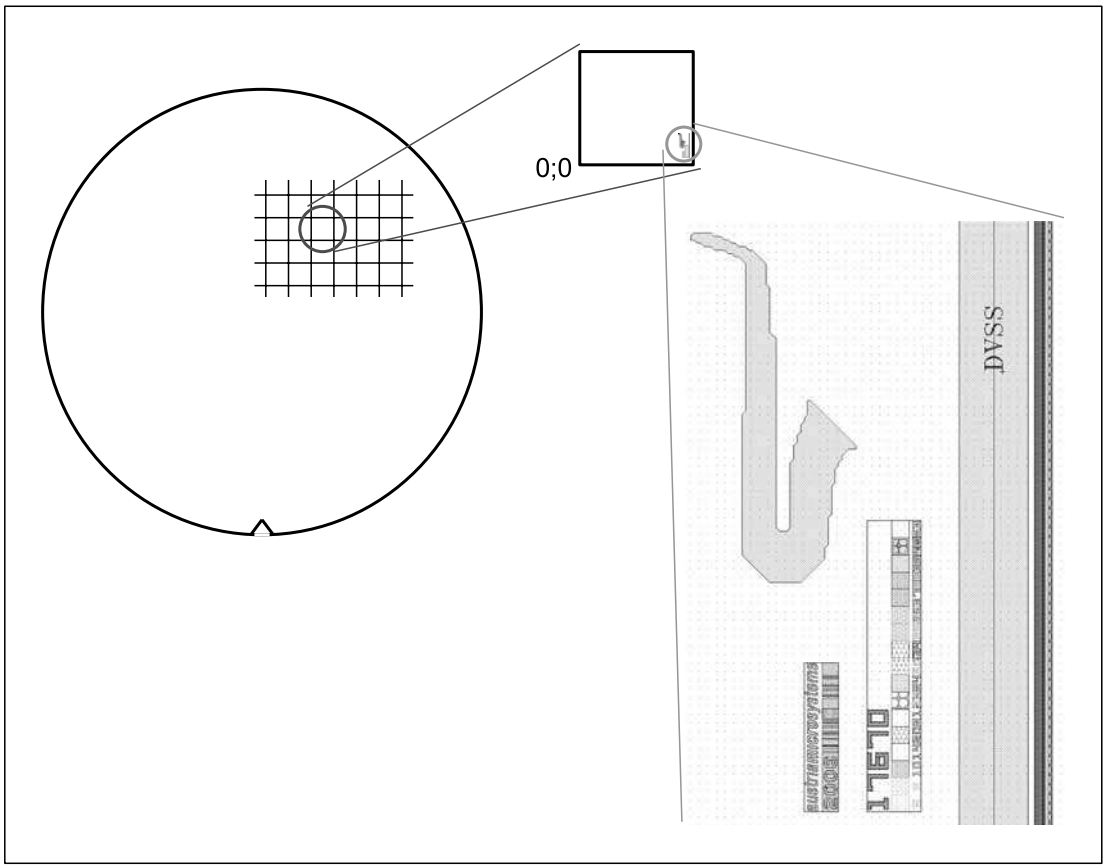


Figure 35 Tape Specification



10.2 Wafer & Die

Figure 36 Die Orientation



11 Ordering Information

Table 88 Ordering Information

Device ID	Version	Temperature Range	Package Type	Delivery Form
AS3518D-ECTP	V23	-20 to +85 °C	CTBGA64; 7x7mm package size, 0.8mm ball pitch	Tape & Reel (Dry Pack)
AS3518D-ECTS	V23	-20 to +85 °C	CTBGA64; 7x7mm package size, 0.8mm ball pitch	Tray (Dry Pack)

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