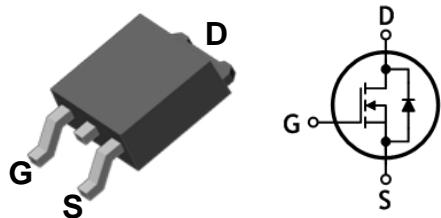


## Power Switching Application

### Features

- Drain-source breakdown voltage:  $BV_{DSS}=100V$
- Low gate charge device
- Low drain-source On resistance:  $R_{DS(on)}=25m\Omega$  (Typ.)
- Advanced trench process technology
- High avalanche energy, 100% test

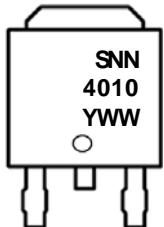


TO-252

### Ordering Information

Part Number	Marking	Package
<b>SNN4010D</b>	<b>SNN4010</b>	<b>TO-252</b>

### Marking Information



Column 1, 2: Device Code  
Column 3: Production Information  
e.g.) YWW  
-. YWW: Date Code (year, week)

### Absolute maximum ratings ( $T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	$V_{DSS}$		100	V
Gate-source voltage	$V_{GSS}$		$\pm 20$	V
Drain current (DC) *	$I_D$	$T_c=25^\circ C$	45	A
		$T_c=100^\circ C$	35	A
Drain current (Pulsed) *	$I_{DM}$		180	A
Single pulsed avalanche energy <sup>(Note 1)</sup>	$E_{AS}$		163	mJ
Single avalanche current	$I_{AS}$		25.5	A
Power dissipation	$P_D$		84	W
Operating junction temperature	$T_J$		150	$^\circ C$
Storage temperature range	$T_{stg}$		-55 to 150	$^\circ C$

\* Limited only maximum junction temperature

**Thermal Characteristics**

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1.48	$^{\circ}\text{C}/\text{W}$
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62	

**Electrical Characteristics ( $T_c=25^{\circ}\text{C}$  unless otherwise noted)**

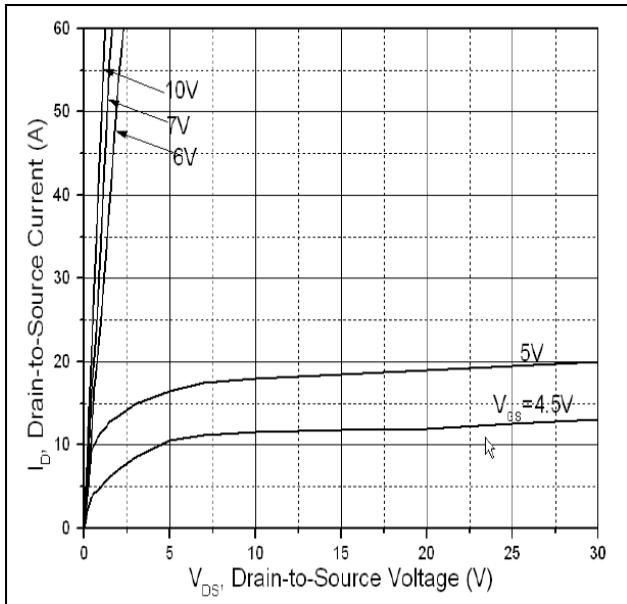
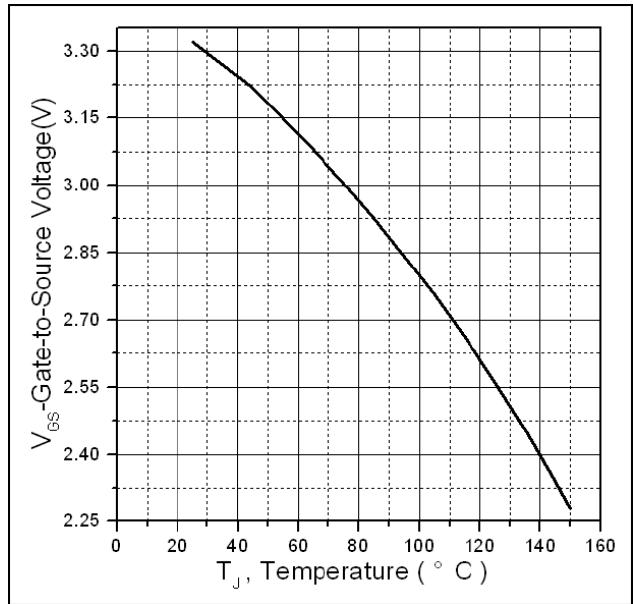
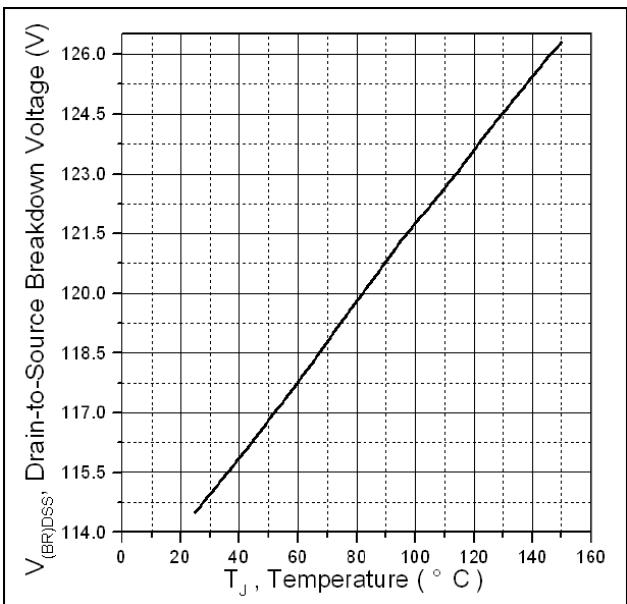
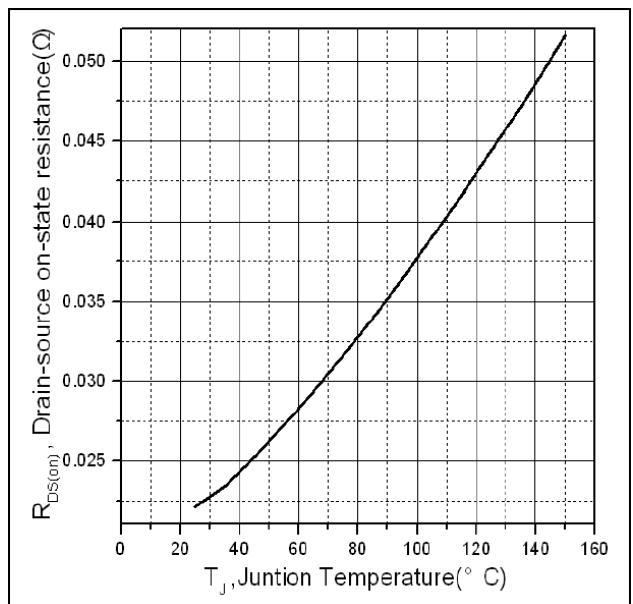
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$\text{BV}_{\text{DSS}}$	$I_D=250\mu\text{A}, V_{GS}=0$	100	-	-	V
Gate threshold voltage	$V_{GS(\text{th})}$	$I_D=250\mu\text{A}, V_{DS}=V_{GS}$	2	-	4	V
Drain-source cut-off current	$I_{\text{DSS}}$	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS}=100\text{V}, V_{GS}=0\text{V}, (@T_J=125^{\circ}\text{C})$	-	-	50	
Gate leakage current	$I_{GSS}$	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	-	-	$\pm 100$	nA
Drain-source on-resistance	$R_{DS(\text{ON})}$	$V_{GS}=10\text{V}, I_D=30\text{A}$	-	25	30	$\text{m}\Omega$
Forward transfer conductance <sup>(Note 2)</sup>	$g_{fs}$	$V_{DS}=5\text{V}, I_D=30\text{A}$	-	50	-	S
Input capacitance	$C_{iss}$	$V_{DS}=25\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	-	2042	-	pF
Output capacitance	$C_{oss}$		-	144	-	
Reverse transfer capacitance	$C_{rss}$		-	114	-	
Turn-on delay time <sup>(Note 2, 3)</sup>	$t_{d(on)}$	$V_{DD}=30\text{V}, I_D=2\text{A}$ $R_G=2.5\Omega, V_{GS}=10\text{V}$	-	13.9	-	ns
Rise time <sup>(Note 2, 3)</sup>	$t_r$		-	13.2	-	
Turn-off delay time <sup>(Note 2, 3)</sup>	$t_{d(off)}$		-	37.8	-	
Fall time <sup>(Note 2, 3)</sup>	$t_f$		-	11.1	-	
Total gate charge <sup>(Note 2, 3)</sup>	$Q_g$	$V_{DS}=30\text{V}, V_{GS}=10\text{V}$ $I_D=30\text{A}$	-	46.3	-	nC
Gate-source charge <sup>(Note 2, 3)</sup>	$Q_{gs}$		-	12	-	
Gate-drain charge <sup>(Note 2, 3)</sup>	$Q_{gd}$		-	16.9	-	

**Source-Drain Diode Ratings and Characteristics ( $T_c=25^{\circ}\text{C}$  unless otherwise noted)**

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_s$	Integral reverse diode in the MOSFET	-	-	45	A
Source current (Pulsed)	$I_{SM}$		-	-	180	A
Forward voltage	$V_{SD}$	$V_{GS}=0\text{V}, I_s=30\text{A}$	-	-	1.3	V
Reverse recovery time <sup>(Note 2, 3)</sup>	$t_{rr}$	$I_s=30\text{A}, V_{GS}=0\text{V}$ $dI_s/dt=-100\text{A}/\mu\text{s}$	-	57	-	ns
Reverse recovery charge <sup>(Note 2, 3)</sup>	$Q_{rr}$		-	107	-	$\mu\text{C}$

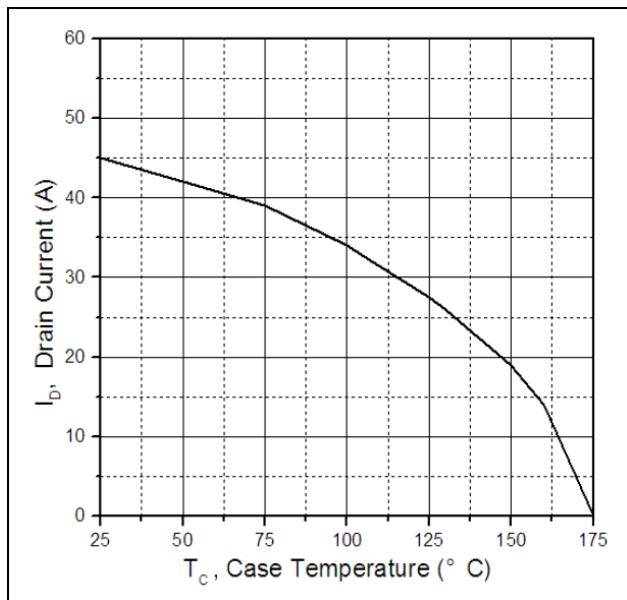
Note:

1.  $L=0.27\text{mH}, I_{AS}=25.5\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$ , Starting  $T_J=25^{\circ}\text{C}$
2. Pulse test: Pulse width  $\leq 300\text{us}$ , Duty cycle  $\leq 1.5\%$
3. Essentially independent of operating temperature typical characteristics

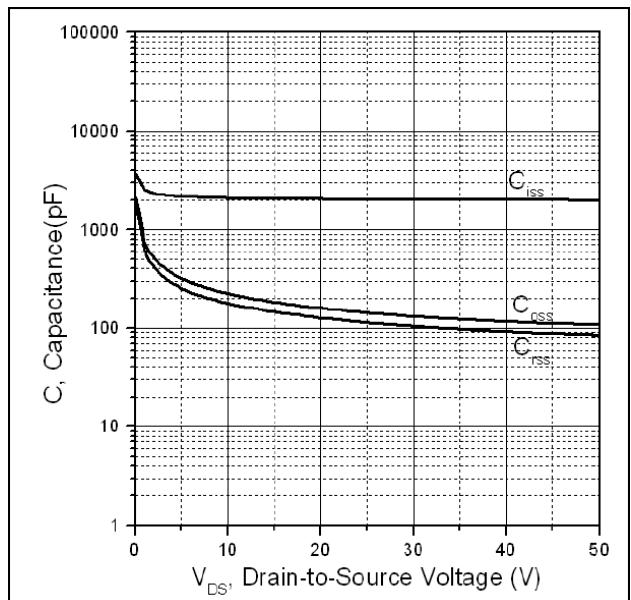
**Electrical Characteristics Curves****Fig. 1 Typical output characteristics****Fig. 2 Gate to source cut-off voltage****Fig. 3 Drain to source breakdown voltage vs. Case temperature****Fig. 4 Normalized On-resistance vs. Case temperature**

## Electrical Characteristics Curves

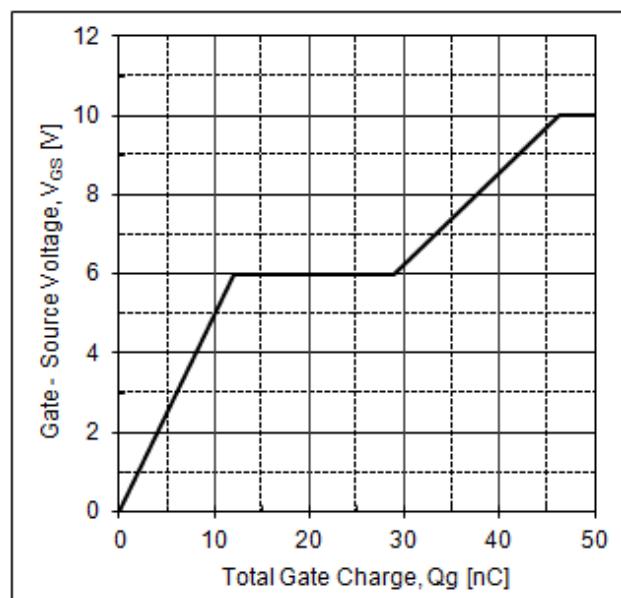
**Fig. 5 Maximum drain current vs.  
Case temperature**



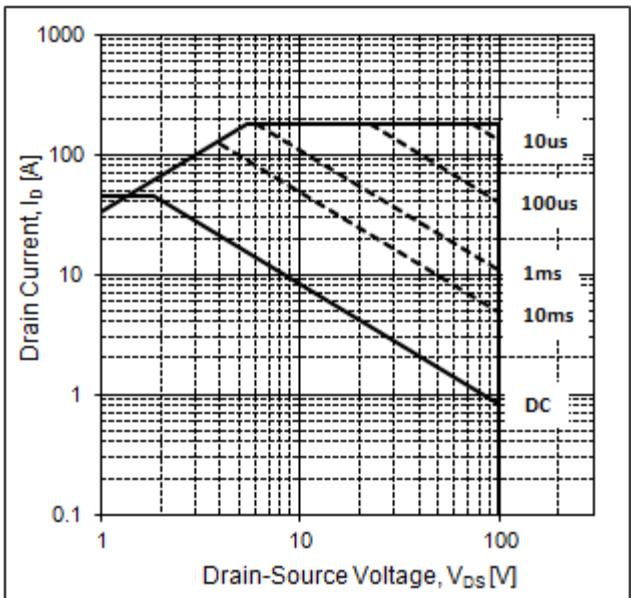
**Fig. 6 Typical capacitance vs.  
Drain to source voltage**

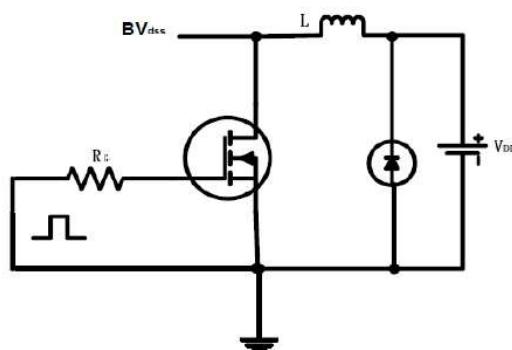
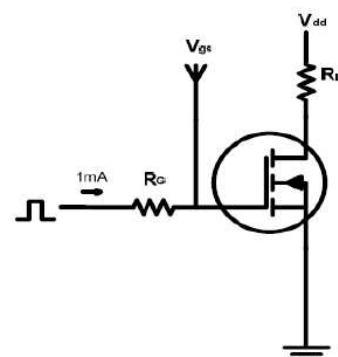
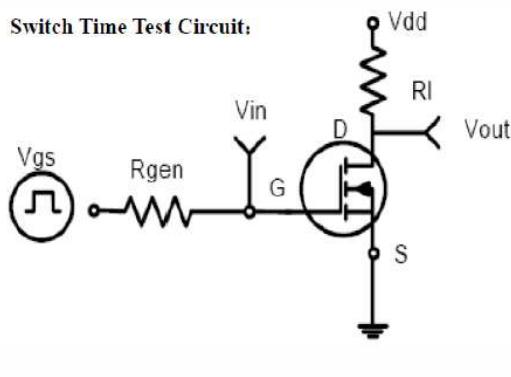
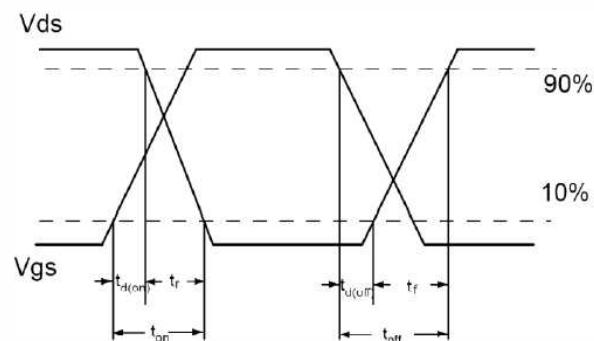


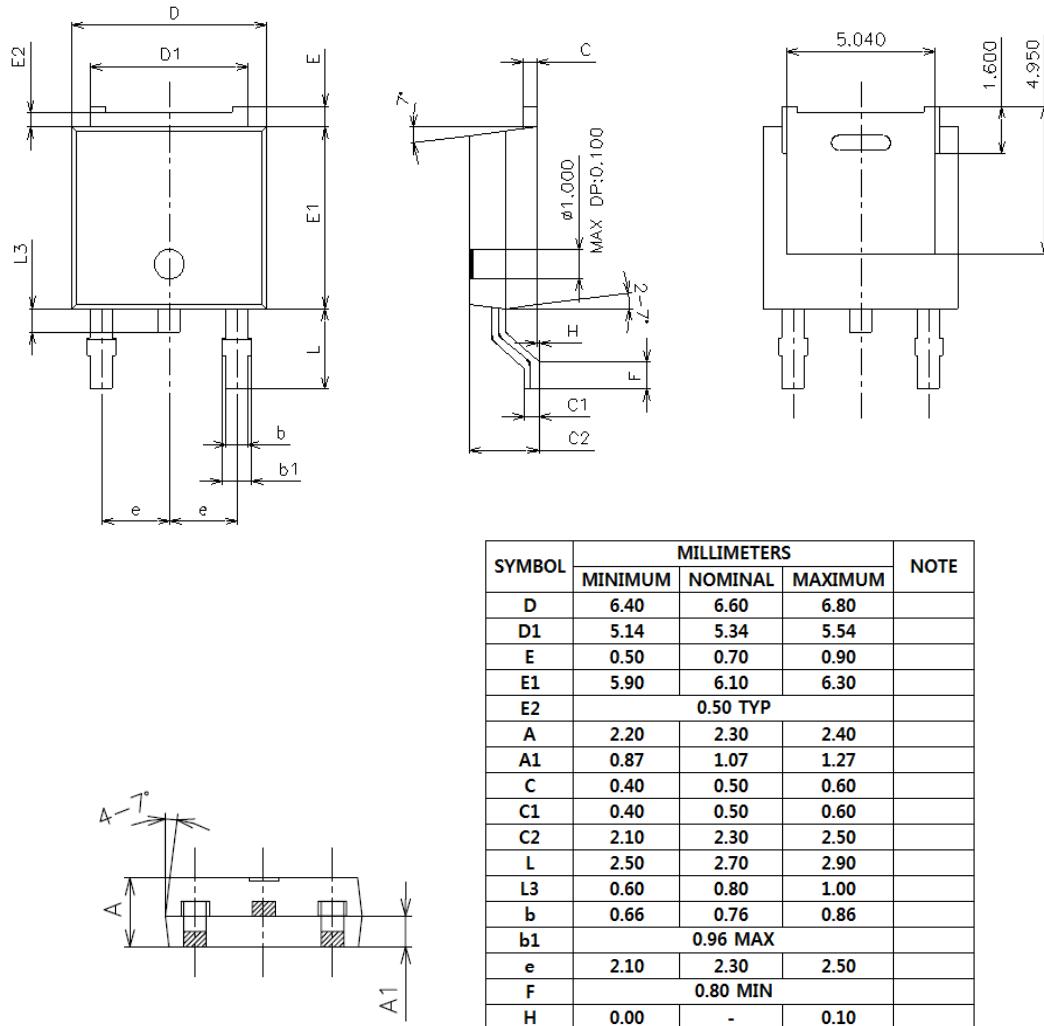
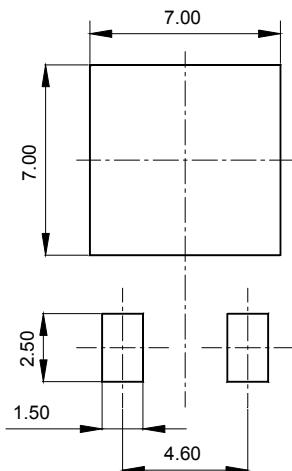
**Fig. 7 Typical total gate charge vs.  
Gate to source voltage**



**Fig. 6 Maximum Safe Operating Area**



**Test circuit****EAS test circuits:****Gate charge test circuit:****Switch Time Test Circuit:****Switch Waveforms:**

**Package Outline Dimensions****Recommended Land Pattern [unit: mm]**

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