AS1534

Data Sheet

12-bit, 8-Channel, Low-Power, 200ksps A/D Converter

1 General Description

The AS1534 is a low-power, 8-channel, 200ksps, 12-bit analog-to-digital (A/D) converter specifically designed to operate with single-supply devices. Superior AC characteristics, very low power-consumption, and highly-reliable packaging make the AS1534 perfect for battery-powered remote-sensor and data-acquisition devices.

The successive-approximation register (SAR), high-speed sampling, high-bandwidth track/hold circuitry, and configurable inputs combine to make the AS1534 highly-flexible and configurable.

Internal registers are used to control the AS1534 features, report on the status of the device, and hold the A/D conversion results.

The device requires very low supply-current at the 200ksps max sampling speed, and features flexible power-down modes to reduce power consumption at slower throughput rate.

The AS1534 operates from a single +3 to +5V supply and contains an internal 2.5V reference and integrated reference buffer. The device also supports an external reference.

Data accesses are made via the fast 8-/16-bit parallel interface in support of a wide range of microprocessors.

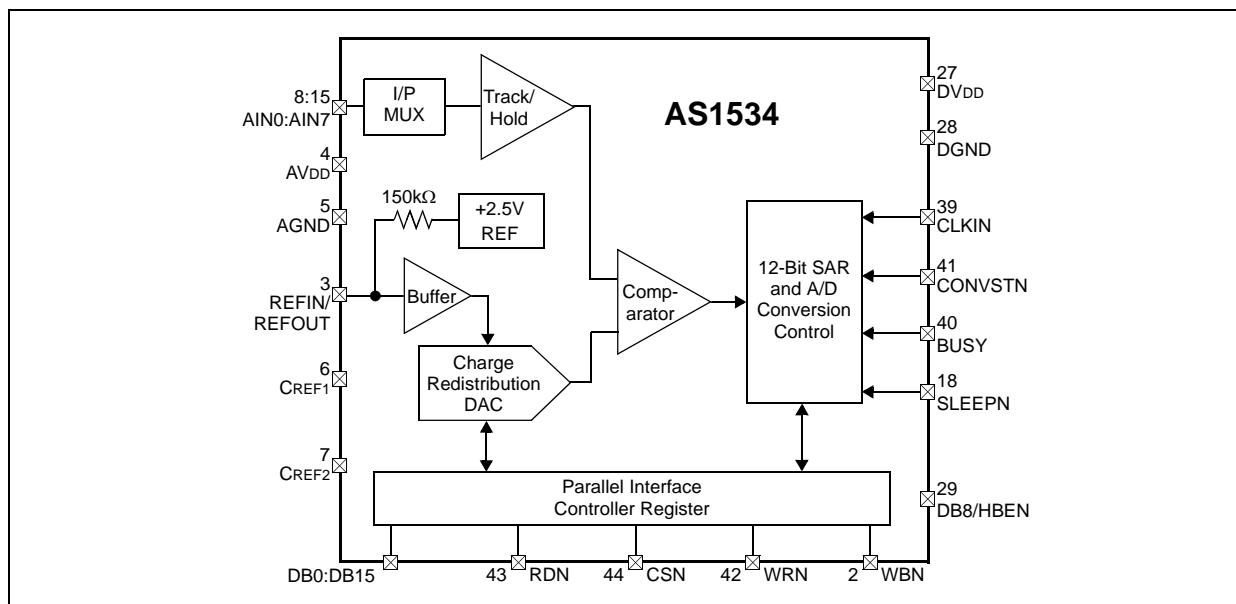The AS1534 is available in a 44-pin PQFP package.

2 Key Features

- Sampling Rate: 200ksps

- 8- and 16-Bit Parallel Interface

- Analog Input Types:
  - 8-Channel Single-Ended
  - 4-Channel Pseudo-Differential
  - 4-Channel Fully-Differential

- Software-Configurable Unipolar or Bipolar Inputs

- Internal +2.5V Reference

- External Reference: 1.2V to V_{DD}

- Low-Power Operation:
  - 7.5mW (V_{DD} = 3 V)
  - 1.5mW (Using Automatic Power-Down after Conversion; V_{DD} = 3 V, 10ksps)

- Single-Supply Operation: +3 to +5V

- 44-pin PQFP Package

3 Applications

The device is ideal for remote sensors, data-acquisition and data-logging devices, pen-digitizers, process control, or any other space-limited A/D application with low power-consumption requirements.

Figure 1. Block Diagram

Contents

4 Absolute Maximum Ratings

Stresses beyond those listed in Table 1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 5 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
AV$_{DD}$ to AGND	-0.3	+7	V	
DV$_{DD}$ to DGND	-0.3	+7	V	
AV$_{DD}$ to DV$_{DD}$	-0.3	+0.3	V	
AINx to AGND	-0.3	AV$_{DD}$ + 0.3	V	
Digital Input Voltage to DGND	-0.3	DV$_{DD}$ + 0.3	V	
Digital Output Voltage to DGND	-0.3	DV$_{DD}$ + 0.3	V	
REFIN/REFOUT to AGND	-0.3	AV$_{DD}$ + 0.3	V	
Input Current to All Pins Except AV$_{DD}$ or DV$_{DD}$	0	20	mA	
Electro-Static Discharge		>1	kV	
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

5 Electrical Characteristics

$AV_{DD} = DV_{DD} = +3.0$ to $+5.5$ V, REFIN/REFOUT = 2.5V External Reference, $f_{CLKIN} = 4MHz$ (–40 to +85ºC)); $f_{SAMPLE} = 200kHz$, SLEEPN = 1; $T_{AMB} = T_{MIN}$ to T_{MAX} (unless otherwise specified).

Table 2. Electrical Characteristics

Symbol	Parameter [1]		Conditions	Min	Typ	Max	Unit
Dynamic Performance							
SNR	Signal-to-Noise + Distortion Ratio [2]		V_{IN} = 10kHz Sinewave, f_{SAMPLE} = 200 kHz	70			dB
THD	Total Harmonic Distortion		V_{IN} = 10kHz Sinewave, f_{SAMPLE} = 200 kHz			−78	dB
	Peak Harmonic or Spurious Noise		V_{IN} = 10kHz Sinewave, f_{SAMPLE} = 200 kHz			−78	dB
IMD	Intermodulation Distortion	Second Order Terms	f_A = 9.983kHz, f_B = 10.05kHz, f_{SAMPLE} = 200kHz		-78		dB
		Third Order Terms	f_A = 9.983kHz, f_B = 10.05kHz, f_{SAMPLE} = 200kHz		-78		
	Channel-to-Channel Isolation		V_{IN} = 25kHz		-80		dB
DC Accuracy							
	Resolution					12	Bits
	Integral Nonlinearity					±1	LSB
	Differential Nonlinearity		Guaranteed no missed codes to 12 bits			±1	LSB
	Unipolar Offset Error				±2	±6	LSB
	Unipolar Offset Error Match					2	LSB
	Unipolar Gain Error				±2	±6	LSB
	Unipolar Gain Error Match					1	LSB
Analog Input							
	Input Voltage Ranges		(AIN+ - AIN–) = 0 to V_{REF}, AIN– can be biased-up but AIN+ should not go below AIN–	0		V_{REF}	V
			(AIN+ - AIN–) = -V_{REF}/2 to +V_{REF}/2, AIN– should be biased to +V_{REF}/2 and AIN+ can go below AIN– but cannot go below 0V	-V_{REF}/2		+V_{REF}/2	
I_{LEAK}	Leakage Current					±1	µA
C_{IN}	Input Capacitance				30		pF
Reference Input/Output							
REFIN	Input Voltage Range		Functional from 1.2V	2.3		V_{DD}	V
R_{IN}	Input Impedance				150		kΩ
REFOUT	Output Reference Voltage			2.45		2.55	V
REFOUT TEMPCO	Output Reference Voltage Temperature Coefficient				20		ppm/ºC
Conversion Rate							
$t_{CONVERT}$	Conversion Time		t_{CLKIN} x 18			4.5	µs
t_{ACQ}	Track/Hold Acquisition Time		t_{CLKIN} x 18	0.5			µs

Table 2. *Electrical Characteristics (Continued)*

Symbol	Parameter [1]			Conditions	Min	Typ	Max	Unit
Logic Inputs								
V_{IH}	Input High Voltage			$AV_{DD} = DV_{DD}$ = 4.5 to 5.5V	2.4			V
				$AV_{DD} = DV_{DD}$ = 3.0 to 3.6V	2.1			
V_{IL}	Input Low Voltage			$AV_{DD} = DV_{DD}$ = 4.5 to 5.5V			0.8	V
				$AV_{DD} = DV_{DD}$ = 3.0 to 3.6V			0.6	
I_{IN}	Input Current			V_{IN} = 0 V or V_{DD}		.01	±10	µA
C_{IN}	Input Capacitance [3]						10	pF
Logic Outputs								
V_{OH}	Output High Voltage			$AV_{DD} = DV_{DD}$ = 4.5 to 5.5V	4			V
				$AV_{DD} = DV_{DD}$ = 3.0 to 3.6V	2.4			
V_{OL}	Output Low Voltage			I_{SINK} = 1.6mA			0.4	V_{OH}
	Floating-State Leakage Current						±10	µA
	Floating-State Output Capacitance [3]						15	pF
	Output Coding			Straight binary (unipolar)				
				Two's complement (bipolar)				
Power Requirements								
AV_{DD}	Analog Input Voltage				+3.0		+5.5	V
DV_{DD}	Digital Input Voltage				+3.0		+5.5	V
I_{DD}	Input Current	Normal Mode [4]		$AV_{DD} = DV_{DD}$ = 4.5 to 5.5V		2.75	3.5	mA
				$AV_{DD} = DV_{DD}$ = 3.0 to 3.6V		2.5	3.5	
		Sleep Mode [5]	With External Clock On	Full power-down, bits PMGT1 = 1, PMGT0 = 0 (see page 16).		10		µA
				Partial power-down, bits PMGT1 = 1, PMGT0 = 1 (see page 16).		500		
			With External Clock Off	Full power-down, bits PMGT1 = 1, PMGT0 = 0 (see page 16).		1	5	
				Partial power-down, bits PMGT1 = 1, PMGT0 = 1 (see page 16).		500		
	Normal Mode Power Dissipation			V_{DD} = 5.5V, SLEEPN = V_{DD}		15	19.25	mW
				V_{DD} = 3.6V, SLEEPN = V_{DD}		9	12.6	
	Sleep Mode Power Dissipation	With External Clock On		V_{DD} = 5.5V; SLEEPN = 0V		55		µW
				V_{DD} = 3.6V; SLEEPN = 0V		36		
		With External Clock Off		V_{DD} = 5.5V, SLEEPN = 0V		5.5	27.5	
				V_{DD} = 3.6V; SLEEPN = 0V		3.6	18	

1. Temperature range is -40 to +85ºC.
2. SNR calculation includes distortion and noise components.
3. Not production tested, guaranteed by characterization at initial product release.
4. All digital inputs @ DGND except CONVSTN, and SLEEPN @ DVDD. No load on the digital outputs. Analog inputs @ AGND.
5. CLKIN @ DGND when external clock off. All digital inputs @ DGND except for CONVSTN, and SLEEPN @ DVDD. No load on the digital outputs. Analog inputs @ AGND.

Timing Characteristics

$AV_{DD} = DV_{DD} = +3.0\ to\ +5.5V,\ f_{CLKIN} = 4\ MHz,\ T_{AMB} = T_{MIN}\ to\ T_{MAX}$ *(unless otherwise specified).*

Table 3. Timing Characteristics

Parameter [1]	Limit at T_{MIN}, T_{MAX}		Unit	Min/Typ/Max	Description
	5V	3V			
f_{CLKIN} [2]	500	500	kHz	Min	Master Clock Frequency
	4	4	MHz	Max	
t_1 [3]	100	100	ns	Min	CONVSTN Pulse Width
t_2	50	90	ns	Max	CONVSTN Rising Edge to BUSY Rising Edge
$t_{CONVERT}$	4.5	4.5	µs	Max	Conversion Time = 18 t_{CLKIN}
t_3	15	15	ns	Min	DB8/HBEN to RDN Setup Time
t_4	5	5	ns	Min	DB8/HBEN to RDN Hold Time
t_5	0	0	ns	Min	CSN to RDN to Setup Time
t_6	0	0	ns	Min	CSN to RDN Hold Time
t_7	55	55	ns	Min	RDN Pulse Width
t_8 [4]	50	50	ns	Max	Data Access Time After RDN
t_9 [5]	5	5	ns	Min	Bus Relinquish Time After RDN
	40	40	ns	Max	
t_{10}	60	70	ns	Min	Minimum Time Between Reads
t_{11}	0	0	ns	Min	DB8/HBEN to WRN Setup Time
t_{12}	5	6	ns	Max	DB8/HBEN to WRN Hold Time
t_{13}	0	0	ns	Min	CSN to WRN Setup Time
t_{14}	0	0	ns	Max	CSN to WRN Hold Time
t_{15}	55	70	ns	Min	WRN Pulse Width
t_{16}	10	10	ns	Min	Data Setup Time Before WRN
t_{17}	5	5	ns	Min	Data Hold Time After WRN
t_{18}	1/2 t_{CLKIN}	1/2 t_{CLKIN}	ns	Min	New Data Valid Before Falling Edge of BUSY

1. Sample tested at +25°C to ensure complian ce. All input signals are specified with $t_R = t_F = 5ns$ (10 to 90% of V_{DD}) and timed from a voltage level of 1.6V.
2. Mark/space ratio for the master clock input is 40:60 to 60:40.
3. The CONVSTN pulse width will here only apply for normal operation. When the AS1534 is in power-down mode, a different CONVSTN pulse width will apply (see DC and AC Application Notes on page 29).
4. Measured with a load of 50pF and defined as the time required for the output to cross 0.8 or 2.4 V.
5. t_9 is derived from the measured time taken by the data outputs to change 0.5V when loaded. The measured number is then extrapolated back to remove the effects of charging or discharging a 50pF capacitor. Thus, time t_9, listed in Table 3 is the true bus relinquish-time of the AS1534 and is independent of bus loading. This parameter is guaranteed by design.

6 Typical Operating Characteristics

Figure 2. FFT vs. Frequency; F_{IN} = 10kHz,
F_{SAMPLE} = 200 kSPS, V_{DD} = 5V, T = 25ºC
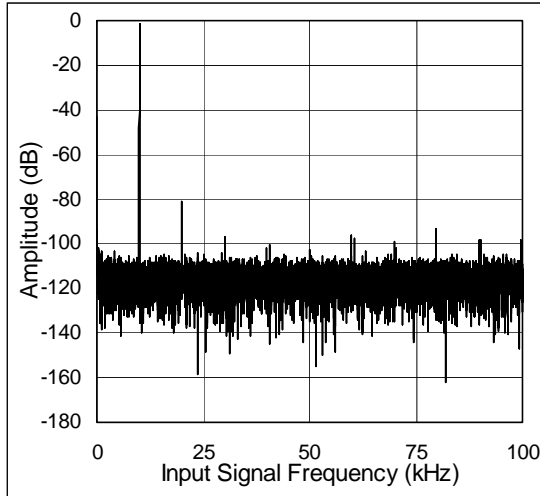
Figure 3. INL vs. Code;
F_{SAMPLE} = 200 kSPS, V_{DD} = 5V, T = 25ºC
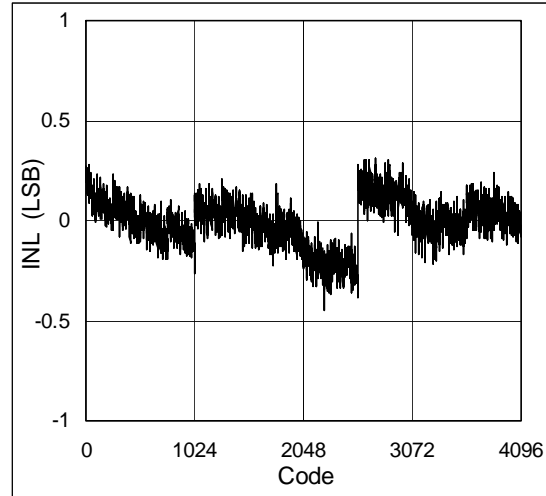
Figure 4. DNL vs. Code;
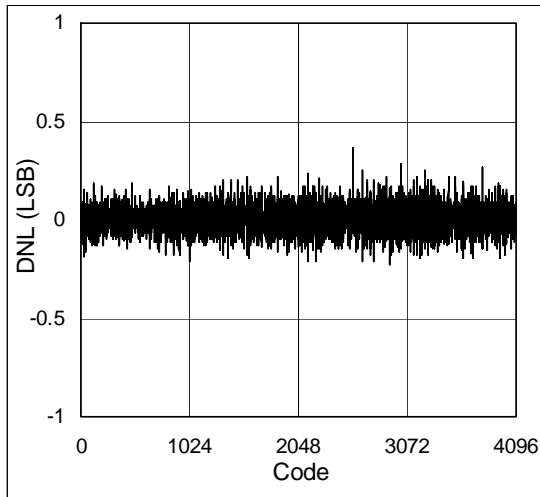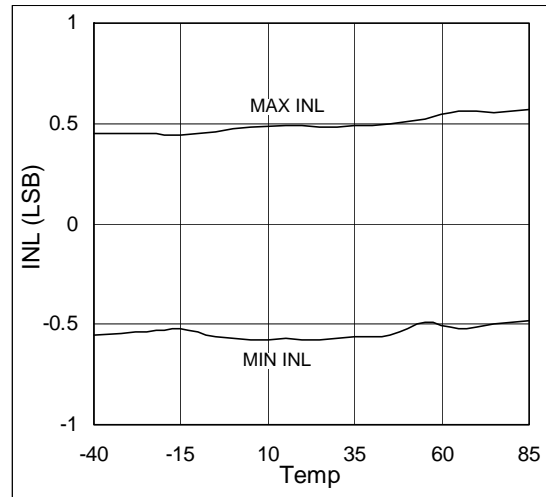*F_{SAMPLE} = 200 kSPS, V_{DD} = 5V, T = 25ºC*

Figure 5. INL vs. Temperature;
V_{DD} = 5.5V, AMODE = 1, SGL/DIFF = 1.

Figure 6. DNL vs. Temperature;
VDD = 5.5V, AMODE = 1, SGL/DIFF = 1.
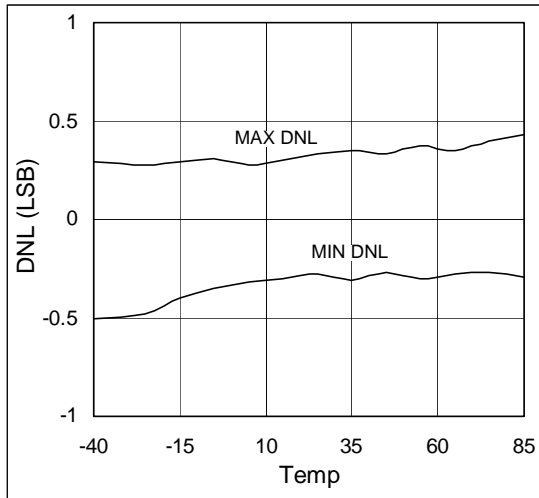
Figure 7. THD vs. Temperature;
VDD = 5.5V, AMODE = 1, SGL/DIFF = 1.

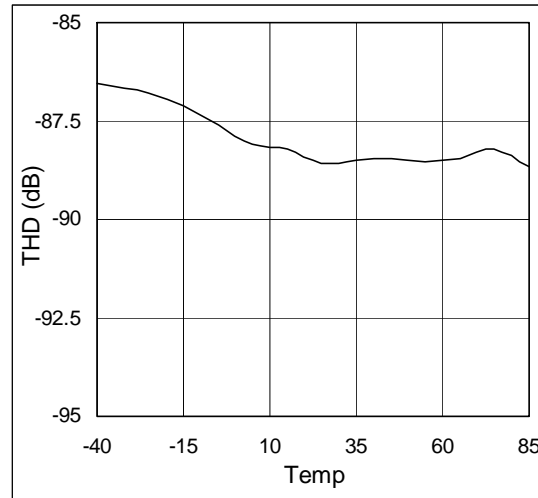*Figure 8. SINAD vs. Temperature;*
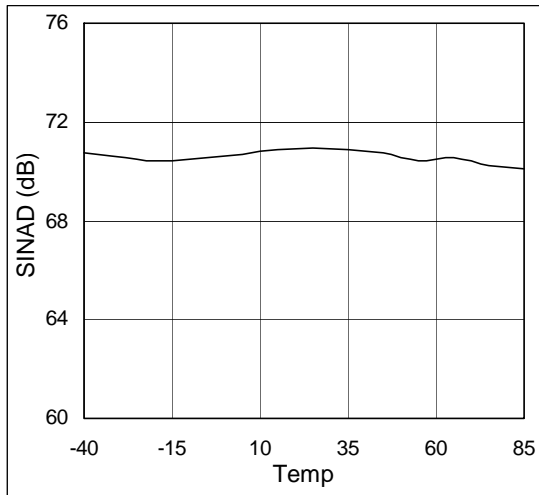*VDD = 5.5V, AMODE = 1, SGL/DIFF = 1.*

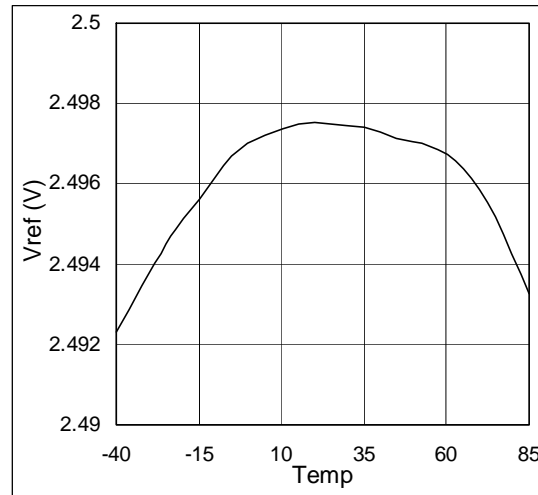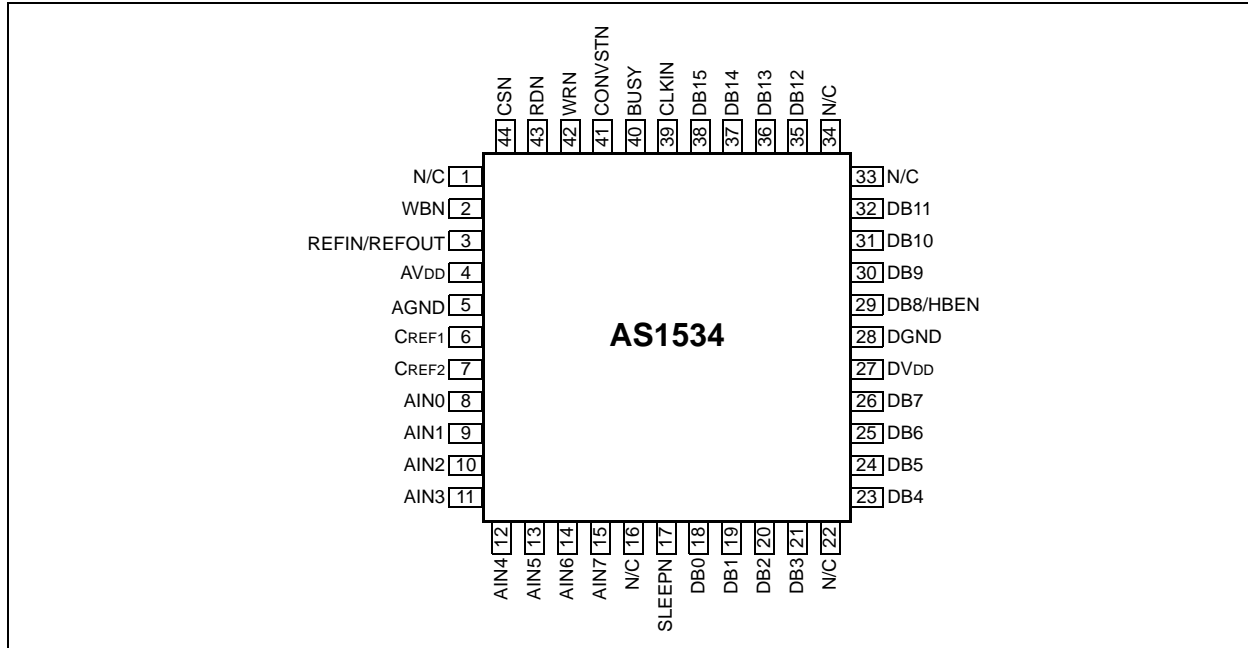*Figure 9. VREF vs. Temperature;*
VDD = 5.5V, AMODE = 1, SGL/DIFF = 1.

7 Pinout and Packaging

Pin Assignments

Figure 10. Pin Assignments (Top View)

Pin Descriptions

Table 4. Pin Descriptions

Pin Number	Pin Name	Description
1, 16, 22, 33, 34	N/C	These pins are not used and should not be connected.
2	WBN	**Word/Byte Mode**. This pin selects the type of data transfer: 1 = Selects word-mode data transfer. Data is transferred to and from the AS1534 in 16-bit words on pins DB0:DB15. 0 = Selects byte-mode data transfer. Data is transferred on pins DB0:DB7 in two 8-bit bytes; pin DB8/HBEN selects the high- or low-byte.
3	REFIN/ REFOUT	**Reference Input/Output**. This pin is connected to the internal reference through a series resistor and is the reference source for the AS1534. The nominal reference voltage is 2.5V and appears at the pin. This pin can be over-driven by an external reference or can be taken as high as AV_{DD}. **Note:** When this pin is tied to AV_{DD}, pin C_{REF1} should also be tied to AV_{DD}.
4	AV_{DD}	**Analog Supply Voltage**. +3.0 to +5.5 V.
5	AGND	**Analog Ground**. Ground reference for track/hold, reference, and DAC circuits.
6	C_{REF1}	**Reference Capacitor 1**. C_{REF1} should be a 0.1µF multi-layer ceramic capacitor and used as a charge source for the internal DAC. **Note:** Capacitor C_{REF1} should be tied between this pin and AGND.
7	C_{REF2}	**Reference Capacitor 2**. C_{REF2} should be a 0.1µF multi-layer ceramic capacitor and used in with the internal 2.5V reference. **Note:** Capacitor C_{REF2} should be tied between this pin and AGND.

Table 4. Pin Descriptions (Continued)

Pin Number	Pin Name	Description
8:15	AIN0:AIN7	**Analog Inputs**. These analog inputs can be used as eight single-ended inputs (referenced to AGND) or four differential inputs. Channel configuration is selected by writing to bits CHSLT0:CHSTL2 (page 16). **Note:** These inputs should never go below AGND or above AV$_{DD}$.
17	SLEEPN	**Sleep Input**. This pin is used in conjunction with bits PMGT0:PMGT1 (page 16) to select the power-down mode.
18:21, 23:26	DB0:DB7	**Data Bits 0 to 7**. Tri-state data I/O pins controlled by CSN, RDN, and WRN. Data output is straight binary (unipolar mode) or two's complement (bipolar mode).
27	DV$_{DD}$	**Digital Supply Voltage**. +3.0 to +5.5 V.
28	DGND	**Digital Ground**. Ground reference point for digital portion of the AS1534.
29	DB8/HBEN	**Data Bit 8/High Byte Enable**. When pin WBN is high (word-mode transfers enabled), this pin acts as Data Bit 7, a tri-state data I/O pin that is controlled by CSN, RDN, and WRN. When WBN is low (byte-mode transfers enabled), this pin selects the byte (high-byte or low-byte) to be written/read: 0 = The low-byte of data written-to or read-from the AS1534 is on pins DB0:DB7. 1 = The high-byte of data written-to or read-from the AS1534 is on pins DB0:DB7.
30:32, 35:38	DB9:DB15	**Data Bits 9 to 15**. Tri-state data I/O pins that are controlled by CSN, RDN, and WRN. Data output is straight binary (unipolar mode) or two's complement (bipolar mode).
39	CLKIN	**Master Clock Signal**. 4MHz clock for the AS1534 sets the conversion time.
40	BUSY	**Busy Output**. This pin is triggered high when a conversion is initiated and remains high until the conversion has completed.
41	CONVSTN	**Conversion Start Logic input**. A low-to-high transition on this pin puts the track/hold circuit into hold mode and starts an A/D conversion. **Note:** When this input is not used it should be tied to DGND.
42	WRN	**Write Input**. Active-low logic input. Used with CSN to write to internal registers.
43	RDN	**Read Input**. Active-low logic input. Used with CSN to read internal registers.
44	CSN	**Chip Select Input**. Active-low logic input. The AS1534 is selected when this pin is active.

8 Detailed Description

The AS1534 is a fast, 8-channel (eight single-ended , four pseudo-differential or four fully-differential), 12-bit, single supply A/D converter, that requires an external 4MHz master clock (CLKIN), two reference capacitors (C$_{REF1}$ and C$_{REF2}$), and power supply decoupling capacitors.

The AS1534 features track/hold circuitry, integrated 2.5V reference, A/D converter circuitry, and parallel interface logic functions on a single die. The A/D converter of the AS1534 consists of a conventional successive-approximation converter based around a capacitive DAC as shown in Figure 1 on page 1.

The AS1534 accepts an analog input range of 0 to +V$_{REF}$ in unipolar mode or -V$_{REF}$/2 to V$_{REF}$/2 in bipolar mode; V$_{REF}$ can also be tied to V$_{DD}$. The reference input pin (REFIN/REFOUT) connects via a 150kΩ resistor to the internal 2.5 V reference and to the internal buffer.

Table 5. Feature Selection

| Feature	Settings
Power-Down Mode	Bits PMGT0:PMGT1 (see page 16), pin SLEEPN (see page 22)
Input Type	Table 11 and Table 12
Channel Selection	Bits CHSLT0:CHSTL2 (see page 16)
Data Transfer Mode	Pin WBN (see page 9)

Figure 11. Operational Diagram
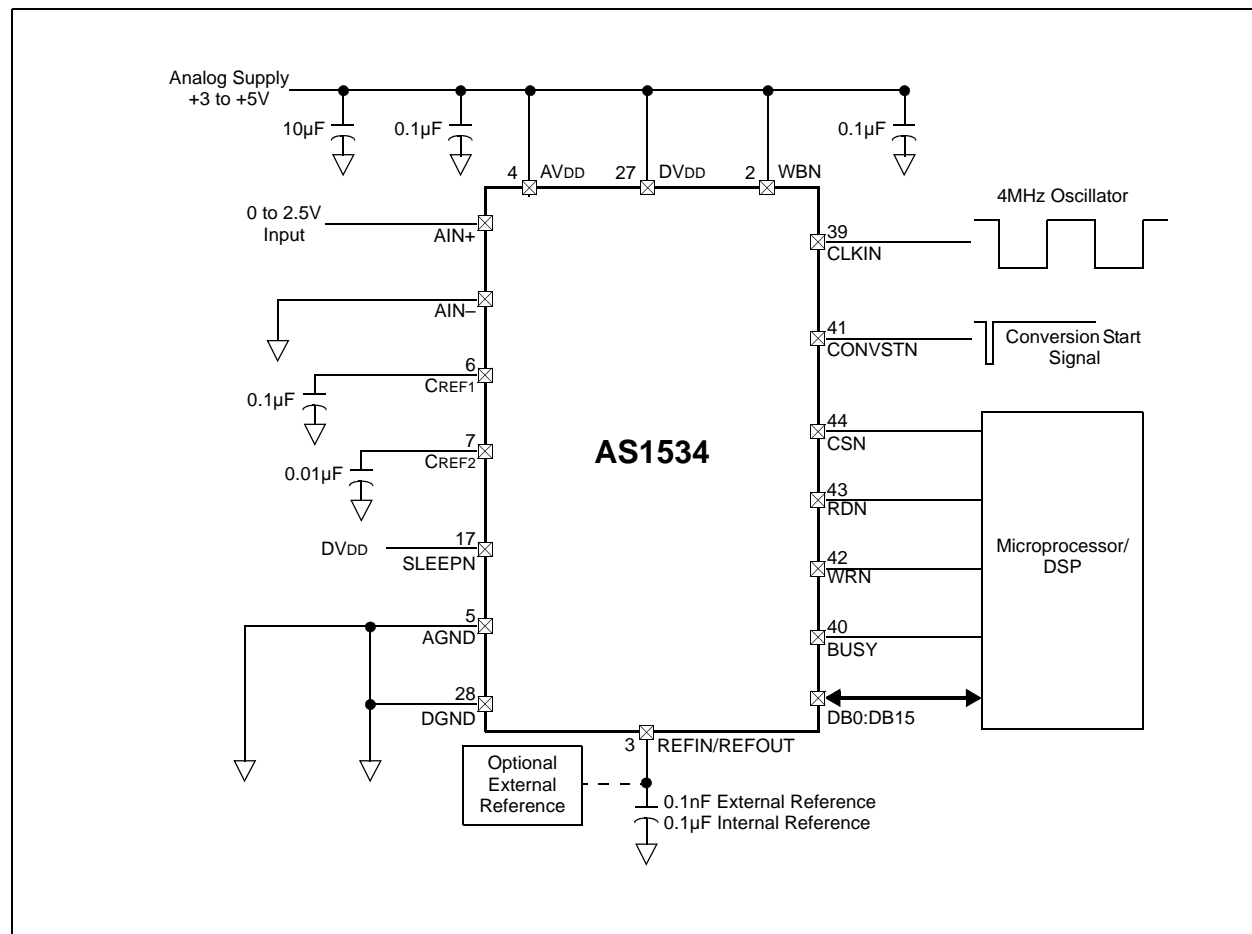
Analog Input

In the equivalent analog input circuit shown in Figure 12, AIN+ is the channel connected to the positive input of the track/hold circuitry and AIN– is connected to the negative input. See Table 11 on page 17 and Table 12 on page 17 for details on channel selection.

Figure 12. Equivalent Input Circuit
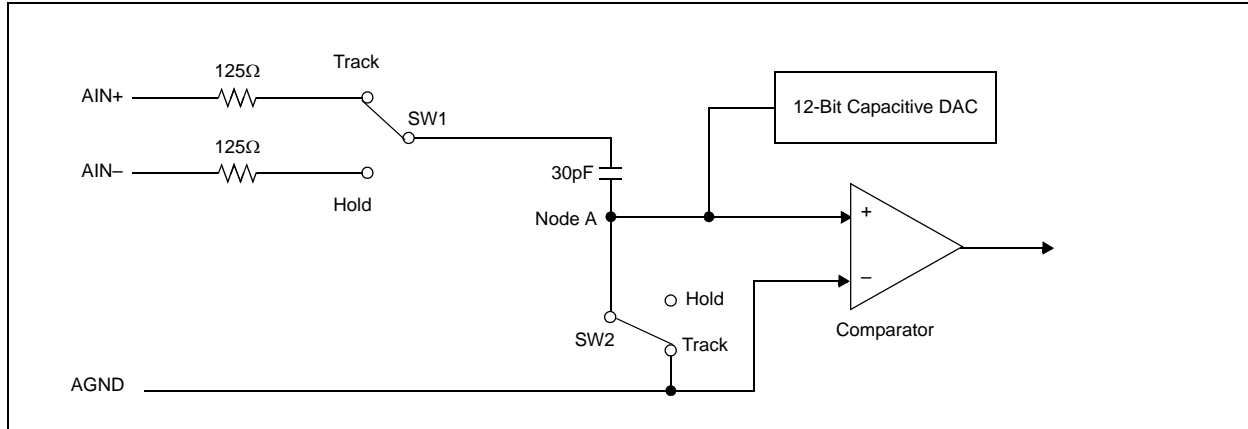
Acquisition Time

During data acquisition time (tACQ), SW1 and SW2 (Figure 12) are in the track position and AIN+ charges the 30pF capacitor through the 125Ω resistor. At the rising edge of the CONVSTN signal, SW1 and SW2 go into the hold position and retains charge on the 30pF capacitor as a sample of the signal on AIN+. In the hold position, pin AIN– is connected to the 30pF capacitor, unbalancing the voltage at Node A at the input of the comparator.

The capacitive DAC adjusts during the remainder of the conversion cycle to restore the voltage at Node A to the correct value. This action transfers a charge, representing the analog input signal, to the capacitive DAC which in turn forms a digital representation of the analog input signal.

The voltage on pin AIN– directly influences the charge transferred to the capacitive DAC at the hold instant, therefore, if this voltage changes during the conversion period, the DAC representation of the analog input voltage will be altered.

Note: The AIN– pin should always be connected to AGND or to a fixed DC voltage since the voltage on pin AIN– remains constant during the conversion period.

Track/Hold

The track-and-hold amplifier enters its tracking mode on the falling edge of the BUSY signal. The time required for the track-and-hold amplifier to acquire an input signal (tACQ) will depend on how fast the 30pF input capacitance is charged. The minimum acquisition time of 400ns includes the time required to change channels.

For large source impedances (>2kΩ) the acquisition time is calculated using the formula:

$$t_{ACQ} = 9(R_{IN} + 125\Omega)30pF \qquad\qquad (EQ\ 1)$$

Where:

R_{IN} is the source impedance of the input signal.

125Ω, 30pF are the input R/C component values.

Input Ranges

The analog input range for the AS1534 is 0V to VREF in unipolar range, and the output coding in unipolar range is straight binary (see Table 10 on page 16 and Figure 14 on page 13).

In bipolar range, the input range is ±VREF/2 biased about VREF/2, and the output coding is two's complement (see Table 10 and Figure 15 on page 13).

Table 6. Analog Input Connections

Analog Input Range	AIN+	AIN–	Diagram	Notes
0V to V_{REF}	V_{IN}	AGND	Figure 14	Output code format is straight binary.
$\pm V_{REF}/2$	V_{IN}	$V_{REF}/2$	Figure 15	Range is $\pm V_{REF}/2$ biased about $V_{REF}/2$. Output code format is two's complement.

Figure 13. Analog Input Buffering
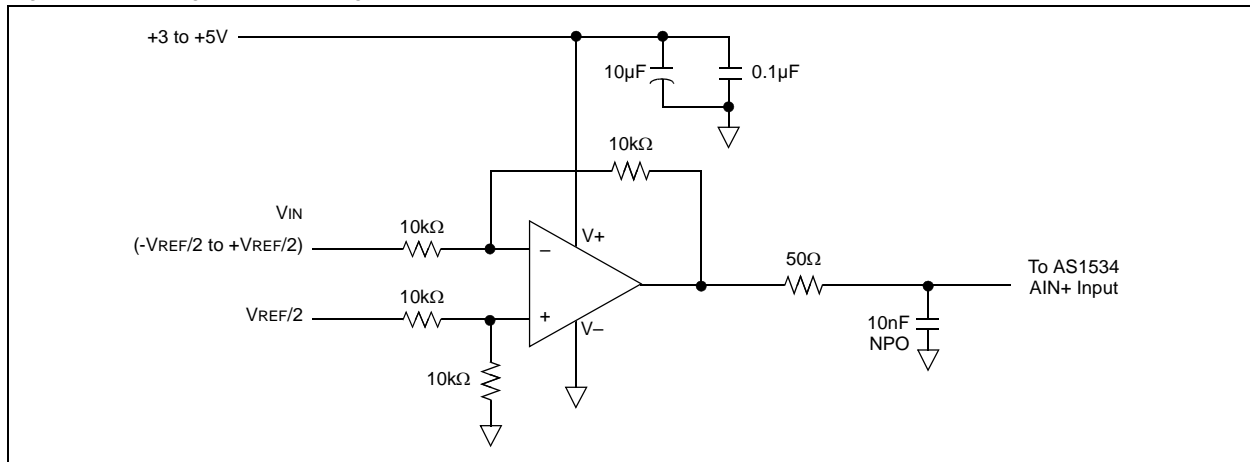
The AIN– channel on the AS1534 can be biased up above AGND in the unipolar mode, or above $V_{REF}/2$ in bipolar mode if required. The advantage of biasing the lower end of the analog input range away from AGND is that the analog input does not have to swing all the way down to AGND. Thus, in single-supply applications the input amplifier will not have to swing all the way down to AGND. The upper end of the analog input range is shifted up by the same amount.

Note: Ensure that the bias applied does not shift the upper end of the analog input above the AV_{DD} supply. In cases where the reference is the AV_{DD} supply, the AIN– input should be tied to AGND in unipolar mode or to $AV_{DD}/2$ in bipolar mode.

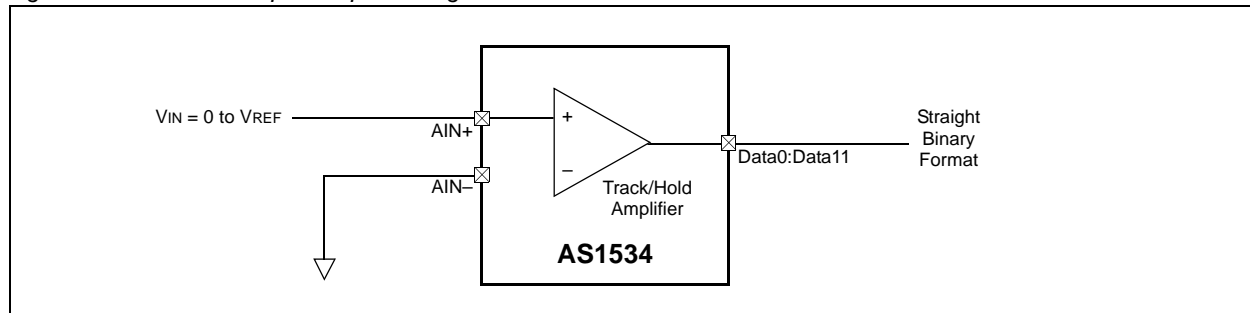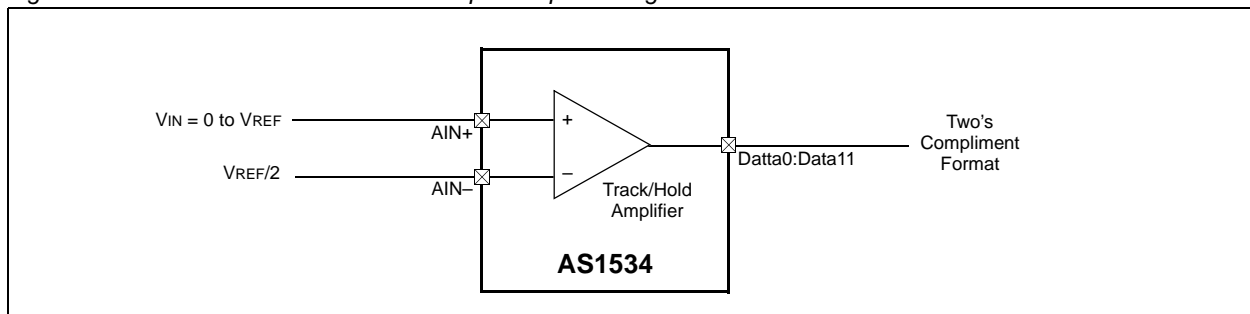*Figure 14. 0 to V_{REF} Unipolar Input Configuration*

Figure 15. $\pm V_{REF}/2$ Biased about $V_{REF}/2$ Bipolar Input Configuration

Analog-to-Digital Conversion

Analog-to-digital (A/D) conversions can be initiated by software (see Control Register on page 16) or by hardware (pin CONVSTN). An external clock for the AS1534 must be applied to pin CLKIN.

Hardware conversions are initiated by pulsing the CONVSTN input. On the rising edge of CONVSTN the AS1534 internal track/hold circuit goes from track- to hold-mode.The falling edge of the CLKIN signal which follows the rising edge of CONVSTN initiates the conversion, as long as the rising edge of CONVSTN occurs at least 10ns (typ) before this CLKIN edge.

Software conversion is started by writing to the Control Register and setting bit CONVST (page 16) to 1. At the end of this Control Register write operation, the AS1534 internal track/hold circuit goes from track- to hold-mode. The falling edge of the CLKIN signal initiates the conversion, as long as the rising edge of WRN occurs at least 10ns (typ) before this CLKIN edge.

A conversion takes 16.5 CLKIN periods from the falling edge of CLKIN. If the 10ns setup time is not exhausted, the conversion will take 17.5 CLKIN periods. The time required by the AS1534 to acquire a signal (t_{ACQ} – see Acquisition Time on page 12) is determined by the source resistor connected to the AIN+ input.

When a conversion is completed, the BUSY output goes low, and the result of the conversion can be read by accessing the ADC Output Data Register through the data bus. For optimal performance, read or write operations should not occur during a conversion, or less than 200ns prior to the next CONVSTN rising edge, since reading/writing during conversion typically degrades the SNR+distortion by less than 0.5 dBs.

The AS1534 operates at throughput rates of over 200ksps using a 4MHz clock. When using the software-initiated conversion for maximum throughput, Control Register write operations (see page 15) should extend beyond the falling edge of BUSY. The falling edge of BUSY resets bit CONVST (page 16) to 0 at which time this bit can be re-set to 1 to start another conversion.

Figure 11 shows the typical application connections for the AS1534. The AGND and the DGND pins are connected together for optimal noise suppression.

Note: Once power is applied to AV$_{DD}$ and DV$_{DD}$, and the CONVSTN signal is applied, the AS1534 requires a certain time (70ms + 1/sample rate) for the internal reference to stabilize.

For applications where minimal power consumption is critical, the AS1534 power-down options (see page 29) can be enabled by software (see Control Register on page 16) or by using pin SLEEPN (see Power-Down Between Conversions Using SLEEPN on page 22).

Internal Registers

The key features of the AS1534 such as power-down modes, hardware/software conversion initiation, and input chan-nel-type and -selection, as well as AS1534 status information, are accessed by internal registers:

- Control Register – See Control Register on page 16.

- Status Register – See Status Register on page 18.

- ADC Output Data Register – Contains the conversion results data.

Note: The AS1534 powers up with default register settings which enable full functionality of the device with minimal changes to internal register settings. Initially, the only register-write operation that is required for full operation of the AS1534 is for channel configuration (see bits CHSLT0:CHSTL2 on page 16).

Register Write Operations

Write operations to the AS1534 internal registers require the transfer of a 16-bits of data in two modes: word-mode (16-bit data word) or byte-mode (two 8-bit bytes), depending on the logic level at pin WBN.

In word-mode (WBN is logic high), the 16 bits are written to the AS1534 on pins DB0:DB15, where DB0 is the LSB and DB15 is the MSB of the write.

In byte-mode (WBN is logic low), pin DB8/HBEN assumes its high-byte enable functionality and data is transferred in two 8-bit bytes on pins DB0:DB7. In byte-mode pin DB0 is the LSB of each transfer and pin DB7 is the MSB. When writing to the AS1534 in byte-mode, the low byte must be written first, followed by the high byte. Each of the MSBs (bits ADDR1 and ADDR0 (see Table 7) of the complete 16-bit word are decoded to determine which register is being addressed, and the 14 LSBs contain the data to be written to the addressed register.

Table 7. Control Register Write Select Bits

Bit 15	Bit 14	Bit 13:Bit 0
ADDR0	ADDR1	Control Register Data Bits (see Table 9 on page 16)

Table 8. Register Write Select Bit Descriptions

Bit	Name	Description
0:13	Data Bits	Control Register Data Bits (see Table 10 on page 16).
14:15	ADDR1:ADDR0	**Write Address Select Bits.** These two bits select an internal register for write operations. 0 0 = This setting does not address any register. 1 1 = This setting addresses the Control Register for write operations. **Note:** These bits are only used to address the internal registers and the Control Register does not store these bit values.

Register Read Operations

Reading from the AS1534 internal registers requires a write to bits RDSLT0:RDSLT1 (page 16). These bits are decoded to determine the register being addressed during a read operation.

The power-up default setting of bits RDSLT0/RDSLT1 is 00 so that the default read will be from the ADC Output Data Register. As with writing to the AS1534 internal registers, 16-bit word or byte-format can be used. See DC and AC Application Notes on page 29 for more information on the two word formats.

After bits RDSLT0/RDSLT1 are set, all subsequent read operations are from the selected register until these bits are changed.

Control Register

The Control Register is a write-only register and contains 14 bits of data (see Table 9). The Control Register is selected by bits ADDR0 and ADDR1 (see Table 7 on page 15). The power-up default setting for of all bits is 0.

Table 9. Control Register Format

		Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		SGL/DIFF	CHSLT2	CHSLT1	CHSLT0	PMGT1	PMGT0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDSLT1	RDSLT0	AMODE	CONVST	N/A	N/A	N/A	N/A (LSB)

Table 10. Control Register Bit Descriptions

Bit	Name	Description
0:3	N/A	
4	CONVST	**Conversion Start Bit.** 0 = Indicates the end of a conversion. 1 = Starts a single conversion; this bit is automatically reset to 0 after a conversion.
5	AMODE	**Analog Mode Bit**. This bit has two functions controlled by bit SGL/DIFF. When SGL/DIFF = 0, AMODE selects between unipolar and bipolar analog input ranges: 0 = Enable unipolar range, 0 to V_{REF} (AIN+ − AIN− = 0 to V_{REF}). 1 = Enable bipolar range −V_{REF}/2 to +VRV_{REF}EF/2 (AIN+ − AIN−) = −V_{REF}/2 to +V_{REF}/2). In this case, AIN− needs to be tied to at least +V_{REF}/2 to allow AIN+ to have a full input swing from 0 V to +V_{REF}. When SGL/DIFF = 1, AMODE selects the source for the track/hold AIN− channel. 0 = AGND is selected. 1 = AIN8 is selected (see Table 11 and Table 12).
6:7	RDSLT0:RDSLT1	**Read Select Bits**. Theses two bits determine which register is addressed for read operations. The default power up setting is 00. 0 0 = All successive read operations are from the ADC Output Data Register. There are always four leading zeros when reading from the ADC Output Data Register. 1 1 = All successive read operations are from the Status Register.
8:9	PMGT0:PMGT1	**Power Management Bits.** These two bits are used with pin SLEEPN for putting the AS1534 into various power-down modes (see DC and AC Application Notes on page 29). PMGT0 PMGT1 SLEEPN Function 0 0 0 Full power-down between conversions 0 0 1 Full power-up 1 0 x Full power-down between conversions 0 1 x Full power-down 1 1 x Partial power-down between conversions
10:12	CHSLT0:CHSTL2	**Channel Select Bits.** These three bits are used to select the analog input on which the conversion is performed. The analog inputs can be configured as eight single-ended channels or four differential channels (see Table 11 and Table 12). The default selection is AIN1 for the positive input and AIN2 for the negative input.
13	SGL/DIFF	**Input Mode Select Bit.** (see Table 11 and Table 12). 0 = Sets the input channels for differential (AMODE = 0) or fully-differential mode (AMODE = 1). 1 = Sets the input channels in single ended mode.

Table 11. Channel Selection for Differential Input Mode

AMODE	CHSLT			AIN+	AIN–	Mode
	2	**1**	**0**			
0	0	0	0	AIN1	AIN2	Unipolar
0	0	0	1	AIN3	AIN4	Unipolar
0	0	1	0	AIN5	AIN6	Unipolar
0	0	1	1	AIN7	AIN8	Unipolar
0	1	x	x	x	x	Not Used
1	0	0	0	AIN1	AIN2	Bipolar
1	0	0	1	AIN3	AIN4	Bipolar
1	0	1	0	AIN5	AIN6	Bipolar
1	0	1	1	AIN7	AIN8	Bipolar
1	1	x	x	x	x	Not Used

Table 12. Channel Selection for Single-Ended Input Mode

AMODE	CHSLT			AIN+	AIN–	Mode
	2	**1**	**0**			
0	0	0	0	AIN1	AGND	Unipolar
0	0	0	1	AIN3	AGND	Unipolar
0	0	1	0	AIN5	AGND	Unipolar
0	0	1	1	AIN7	AGND	Unipolar
0	1	0	0	AIN2	AGND	Unipolar
0	1	0	1	AIN4	AGND	Unipolar
0	1	1	0	AIN6	AGND	Unipolar
0	1	1	1	AIN8	AGND	Unipolar
1	0	0	0	AIN1	AIN8	Unipolar
1	0	0	1	AIN3	AIN8	Unipolar
1	0	1	0	AIN5	AIN8	Unipolar
1	0	1	1	AIN7	AIN8	Unipolar
1	1	0	0	AIN2	AIN8	Unipolar
1	1	0	1	AIN4	AIN8	Unipolar
1	1	1	0	AIN6	AIN8	Unipolar
1	1	1	1	AIN8	AIN8	Unipolar

Status Register

The Status Register is a read-only register and contains 16 bits of data (see Table 13). This register is selected by the setting bits RDSLT0:RDSLT1 (page 16). The power-up default settings of all Status Register bits is 0.

Table 13. Status Register Format

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (MSB)	0	SGL/DIFF	CHSLT2	CHSLT1	CHSLT0	PMGT1	PMGT0
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	AMODE	BUSY	N/A	N/A	N/A	N/A (LSB)

Table 14. Status Register Bit Descriptions

Bit	Name	Description
0:3	N/A	
4	BUSY	**Conversion Busy Bit.** This bit indicates the conversion status. 0 = No conversion in progress. 1 = Conversion in progress.
5	AMODE	**Analog Mode Bit.** This bit is used along with SGL/DIFF and CHSLT2 – CHSLT0 to indicate the track/hold AIN+ and AIN– inputs and the conversion mode (unipolar or bipolar) (see Table 11 on page 17 and Table 12 on page 17).
6:7	N/A	
8:9	PMGT0:PMGT1	**Power Management Bits.** These bits along with pin SLEEPN indicate if the AS1534 is in one of the power-down modes.
10:12	CHSLT0:CHSLT2	**Channel Selection Bits.** These bits, in conjunction with the SGL/DIFF bit, indicate which channel has been selected for conversion (see Table 11 on page 17 and Table 12 on page 17).
13	SGL/DIFF	**Single/Differential Bit.** 0 = Indicates the AS1534 is set for differential input mode. 1 = Indicates the AS1534 is set for single-ended input mode.
14:15	N/A	

Figure 16. Flowchart for Reading the Status Register
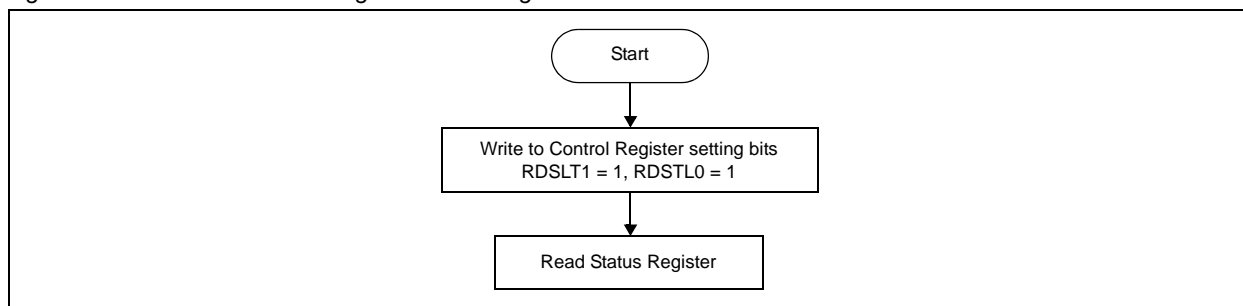
Parallel Interface

The AS1534 provides a flexible, high-speed, parallel interface, capable of transferring 16-bit data words in word-mode (pin WBN tied high) or byte-mode (WBN tied low).

Read Operations

Figure 17 shows the read cycle timing diagram for 16-bit data word transfers for the AS1534.

In word-mode (pin WBN at a logic high) read operations, a single read operation from the AS1534 accesses the 16-bit word on pins DB0:DB15 (the 12 data bits appear on pins DB0:DB11). DB0 is the LSB of the word.

In word-mode, pin DB8/HBEN assumes its DB8 functionality, since the high-byte enable function is not required.

In byte-mode (pin WBN at a logic low), two read cycles (shown in Figure 18) are required to access the full 16-bit data word from the AS1534. In Figure 18, the first read operation places the lower 8 bits of the full data word onto pins DB0:DB7; the second read operation places the upper 8 bits of the data word on pins DB0:DB7.

In byte-mode, pin DB8/HBEN assumes its high-byte enable function, and determines whether the read operation accesses the high-byte or low-byte of the 16-bit word. To read a low-byte, DB0 is the LSB of the 16-bit word; for a high-byte read, DB0 is data bit 8 of the 16-bit word and DB7 is the MSB of the 16-bit word.

Figure 17. Read and Write Cycle Timing for Word-Mode Transfers – WBN is Logic Low
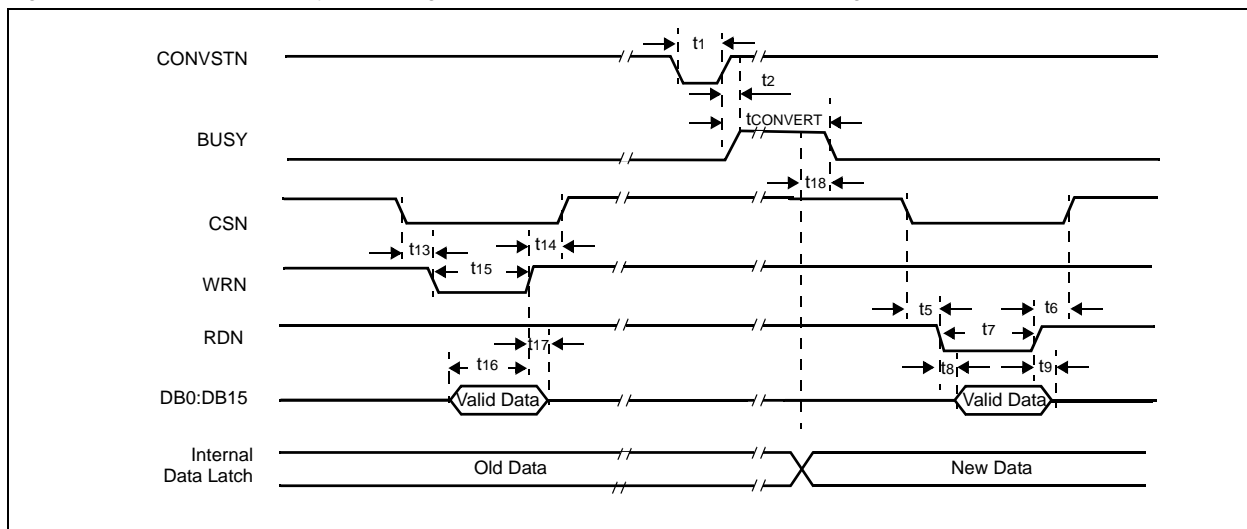
Figure 18. Read Cycle Timing for Byte-Mode Transfers – WBN is Logic Low
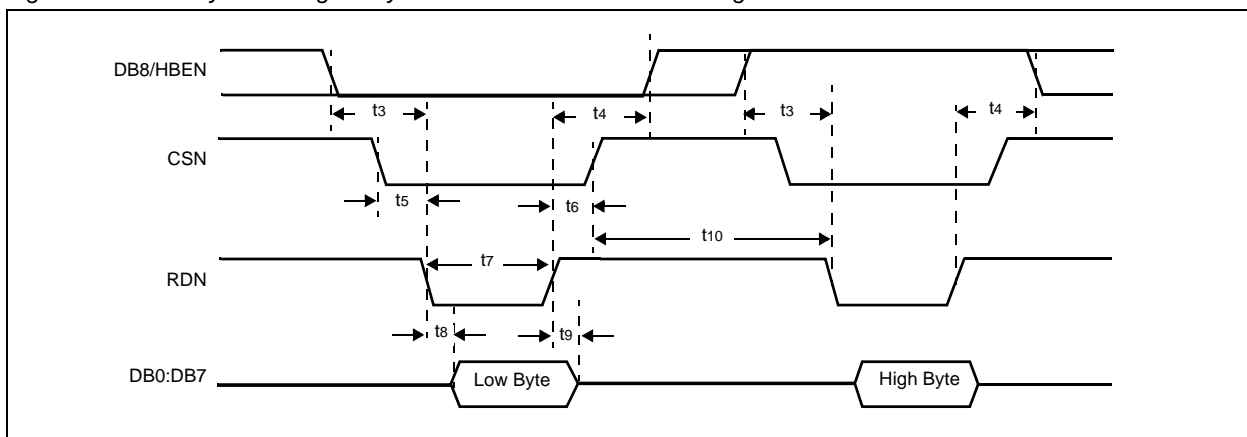
Signals CSN and RDN are gated internally and level-triggered active low. In word- or byte-mode, CSN and RDN may be tied together (since the timing specification for t_5 and t_6 is 0ns (min)). The data is output a time, t_8, after both CSN and RDN go low. RDN rising edge should be used to latch data. After time t_9, the data lines will become tri-stated.

Write Operations

In word-mode (pin WBN at a logic high), a single write operation transfers a full 16-bit word to the AS1534. Data to be written to the AS1534 must be put on the DB0:DB15 inputs with DB0 the LSB of the data word. In word-mode write operations, pin DB8/HBEN assumes its DB8 function.

Figure 17 on page 19 shows the word-mode write cycle timing diagram for the AS1534.

In word-mode, pin DB8/HBEN assumes its DB8 functionality, since the high-byte enable function is not required.

In byte-mode (WBN at a logic low), the AS1534 requires two write operations shown in Figure 19 to transfer a full 16-bit word to the AS1534. Data to be written to the AS1534 should be provided on inputs DB0:DB7.

In byte-mode write operations, pin DB8/HBEN determines whether the byte to be written is the high-byte or the low-byte data. The low-byte should be written first with DB0 the LSB of the 16-bit data word. For the high-byte write, DB8/HBEN must be high; data on the DB0 input should be data bit 8 of the 16-bit data word. DB7 is the MSB of the 16-bit data word.

Figure 19. Write Cycle Timing for Byte-Mode Transfers – WBN is Logic Low
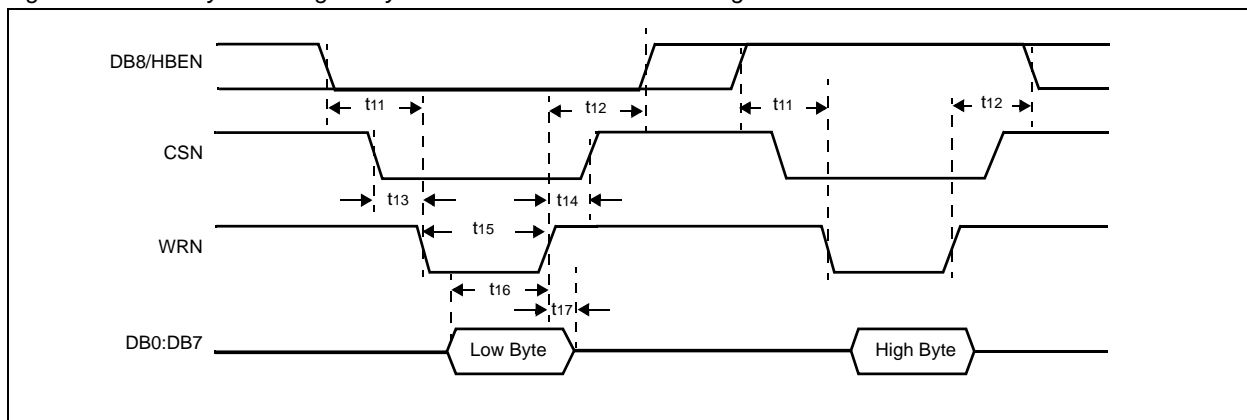
Signals CSN and WRN are gated internally, and may be tied together (since the timing specification for t_{13} and t_{14} is 0ns (min)). Data is latched on the rising edge of WRN. The data needs to be set up a time, t_{16}, before the WRN rising edge and held for a time, t_{17}, after the WRN rising edge.

Power-Down Options

The AS1534 can be fully- or partially-powered down to allow the device to achieve the best power performance for a given throughput rate. Power-down options are selected (see Table 15) by the use of pin SLEEPN and/or by programming bits PMGT0 and PMGT1.

Figure 20. Typical Low-Power Circuit
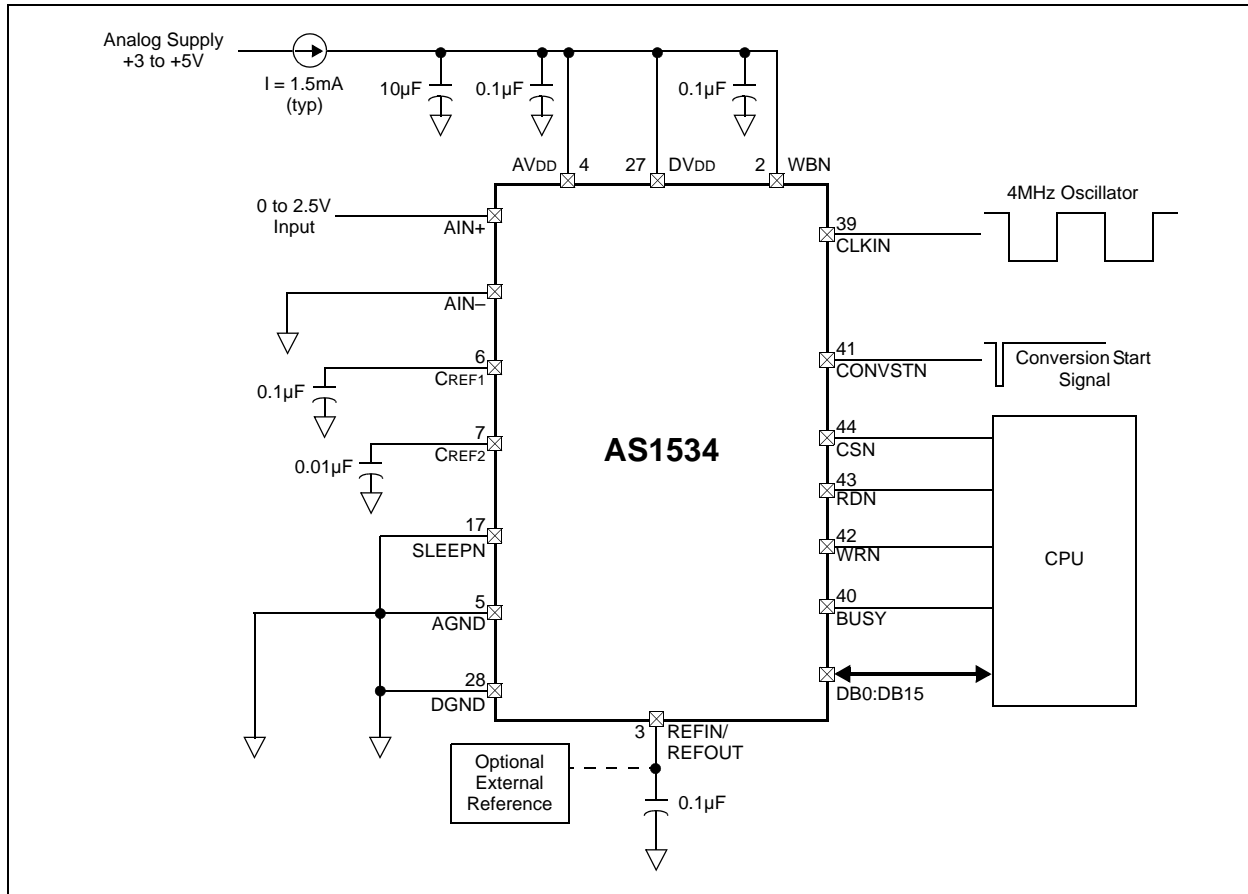
Table 15. Power-Down Settings

PMGT0	PMGT1	SLEEPN	Function
0	0	0	Full power-down between conversions
0	0	1	Full power-up
1	0	x	Full power-down between conversions
0	1	x	Full power-down
1	1	x	Partial power-down between conversions

Full Power-Up Mode

In this mode (see Table 15), the AS1534 will not power down at anytime. This mode is used in cases of high throughput rates when a power down is not possible.

Full Power-Down Mode

In this mode (see Table 15), the AS1534 will stay powered down until bits PMGT0:PMGT1 (page 16) are rewritten for another mode.

Full Power-Down Between Conversions Mode

In this mode (see Table 15), the AS1534 is only powered up for the duration of the conversion, otherwise all internal circuitry is powered down and I$_{DD}$ is 10μA (typ). A full power-down after a conversion significantly reduces the power consumption of the AS1534 at lower throughput rates.

The AS1534 has a conversion time of 4.5μs using a 4MHz external clock, thus consuming 2.5mA (typ) for 9μs in every conversion cycle if it is fully powered down at the end of each conversion. See Typical Operating Characteristics on page 7 for the details of power consumption for V$_{DD}$ = 3 V as a function of throughput.

Partial Power-Down Between Conversions Mode

In this mode (see Table 15), all internal circuitry except the internal reference is powered down between conversions, and I$_{DD}$ = 500μA (typ). The selection of partial-power down does not provide any significant improvement in throughput versus full power-down. However, a partial power-down does allow for the use of an external reference. Partial-power down also allows the AS1534 to be powered-up faster after a long power-down period when using an external reference (see Using an External Reference on page 22).

Power-Down Between Conversions Using SLEEPN

Pulling pin SLEEPN (see Table 15) low puts the AS1534 in full power-down mode between conversions. As long as pin SLEEPN is set to a logic high, the AS1534 is set for normal operation. This may be necessary if the AS1534 is being used at high-throughput rates and it is not possible or practical to power down between conversions.

Notes:

1. If the power-down mode will only be controlled using pin SLEEPN; bits PMGT0:PMGT1 (page 16) must be set to 00.
2. If the power-down mode will only be controlled by software, pin SLEEPN should be tied logic high.
3. A combination of hardware and software power-down mode selection can also be used (see Table 15).
4. For optimal power down between conversions at lower throughput rates (e.g., <100 ksps) pin SLEEPN should be tied logic low.

Power-Up

Using an External Reference

The AS1534 is powered up from one of two conditions: when the power supplies are initially powered up or when powered up from a hardware or software power-down (see DC and AC Application Notes on page 29). The power-up time is the longer of two conditions: the time required (300μs typ) for the AS1534 to power-up when power is first applied or the time it takes the external reference to stabilize at the 12-bit level.

When AV$_{DD}$ and DV$_{DD}$ are powered up, the AS1534 enters a mode whereby the CONVSTN signal initiates a timeout.

Notes:

1. At power-up, the functionality of pin SLEEPN is disabled.
2. The AS1534 powers up from a full hardware or software power-down in 5μs (typ). This limits the throughput which the AS1534 is capable of to 100 kSPS when powering down between conversions.

Figure 21 shows power-down between conversions implemented using pin CONVSTN. The power-down between conversions option is selected by using pin SLEEPN and bits PMGT0:PMGT1 on page 16. In this mode the AS1534 automatically enters a full power-down at the end of each conversion (i.e., when the BUSY signal goes low). The falling edge of the next CONVSTN pulse causes the AS1534 to power up.

Assuming the external reference is left powered up, the AS1534 should be ready for normal operation 5μs after this falling edge of CONVSTN. The rising edge of CONVSTN initiates a conversion, thus the CONVSTN pulse should be at least 5μs wide.

The AS1534 automatically powers down upon completion of a conversion.

Note: In software-initiated conversions, the AS1534 may be powered up via software before initiating a conversion.

Figure 21. Timing Waveforms for Pin CONVSTN to Power Up the AS1534 and Start a Conversion
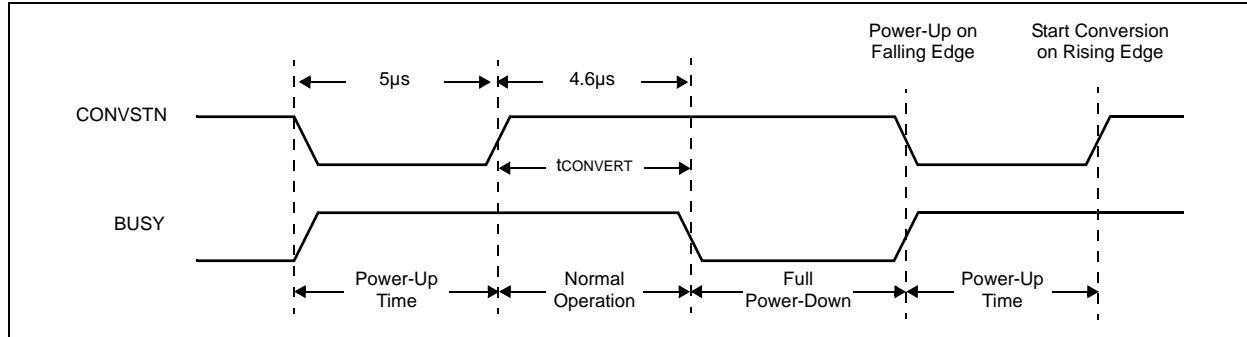
Using the Internal Reference

When using the internal reference, the power-up time is effectively the time it takes to charge up the external capacitor on the REFIN/REFOUT pin. This time is given by the equation:

$$t_{UP} = 9RC \hspace{4cm} \text{(EQ 2)}$$

Where:

R = 150KΩ
C = External reference capacitor. The recommended value of the external capacitor is 100nF; this gives a power-up time of approximately 135ms before normal AS1534 operation should begin.

When the reference capacitor is fully charged, the power-up time from a hardware or software power-down reduces to 5µs. This is because an internal switch opens to provide a high impedance discharge path for the reference capacitor during power-down (see Figure 22).

Figure 22. Internal Reference During Power-Down
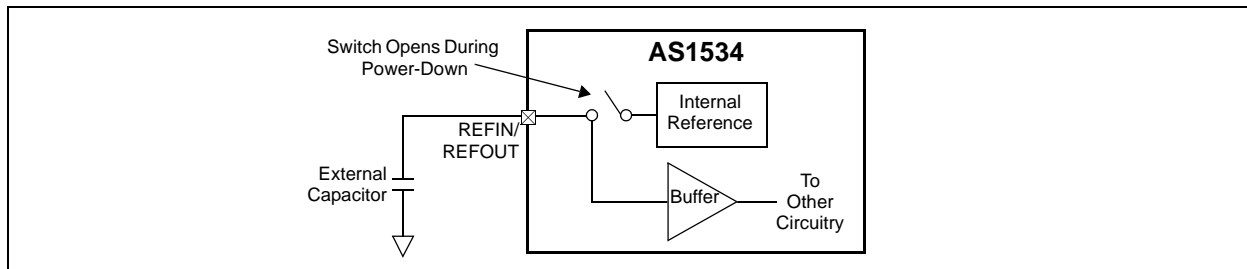
An advantage of the low-charge leakage from during power-down is that even though the reference is being powered down between conversions, the reference capacitor holds the reference voltage to within 0.5 LSBs with throughput rates ≥ 100 samples/s, with a full power-down between conversions. A high-input impedance op amp should be used to buffer this external reference capacitor.

Note: If the AS1534 is left in its powered-down state for more than 100ms, the charge on the reference capacitor will start to leak away and the power-up time will increase. In this case, a partial power-down for the last conversion should be used to keep the reference powered up.

9 Application Information

Internal/External Reference

When the AS1534 internal reference is used, pin REFIN/REFOUT should be decoupled with a 100nF capacitor to AGND very close to the REFIN/REFOUT pin. These connections are shown in Figure 22 on page 23.

If the internal reference is required for use external to the AS1534, it should be buffered at the REFIN/REFOUT pin and a 100nF capacitor should be connected from this pin to AGND. The typical noise performance for the internal reference with 5V supplies is 150nV/√Hz @ 1kHz, and DC noise is 100mVp-p.

Figure 23. Internal Reference Connections
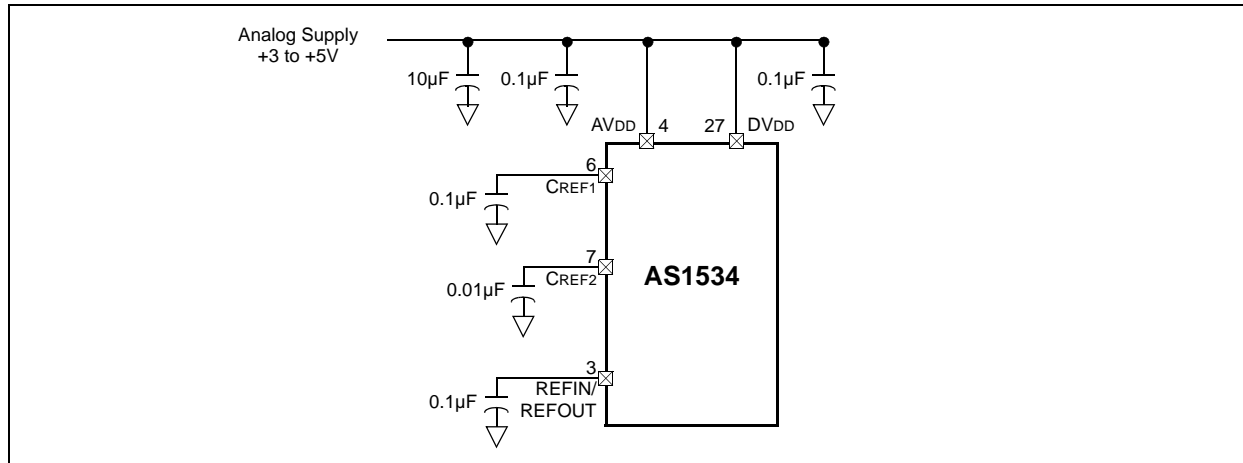
Pin REFIN/REFOUT may be over-driven by connecting it to an external reference as shown in Figure 24. This is possible due to the series resistance from the REFIN/REFOUT pin to the internal reference. The external reference can be in the range 2.3V to AV$_{DD}$.

When using AV$_{DD}$ as the reference source, the 10nF capacitor from pin REFIN/REFOUT to AGND should be as close as possible to pin REFIN/REFOUT, and also the C$_{REF1}$ pin should be connected to AV$_{DD}$ to keep this pin at the same voltage as the reference. When using AV$_{DD}$ it may be necessary to add a resistor in series with the AV$_{DD}$ supply. This has the effect of filtering the noise associated with the AV$_{DD}$ supply.

Note: When using an external reference, the voltage present at the REFIN/REFOUT pin is determined by the external reference source- and series-resistance of 150kΩ from pin REFIN/REFOUT to the internal 2.5V reference. Therefore, a low source-impedance external reference is recommended.

Figure 24. Connections with AV$_{DD}$ as the Reference
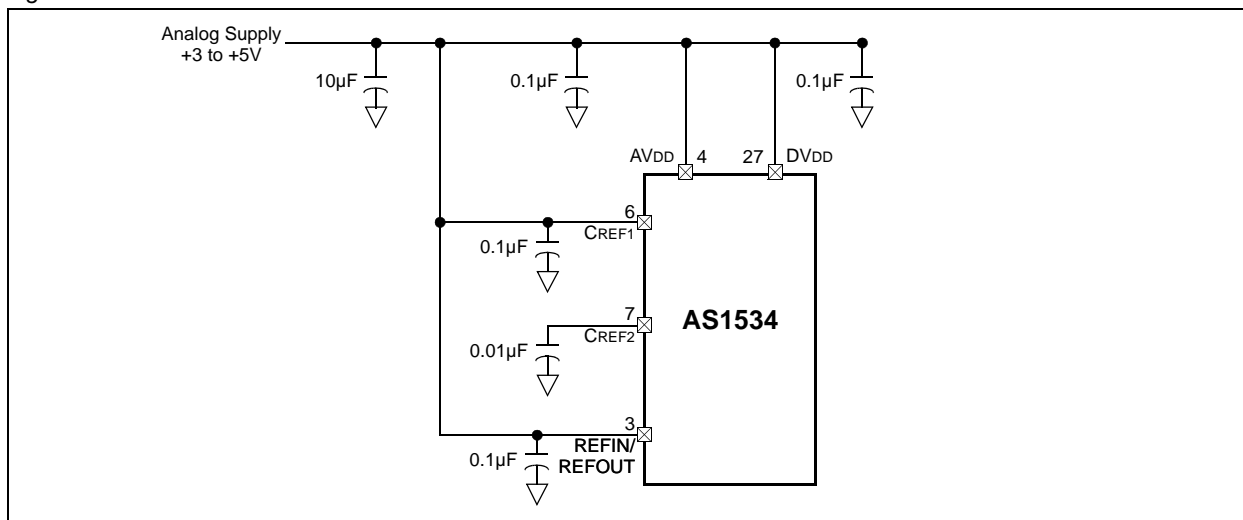
Microprocessor and DSP Interfacing

The AS1534 parallel interface provides connections a wide range of microprocessors or DSPs as a memory-mapped or I/O-mapped device. Inputs CSN and RDN are common to all memory peripheral interfaces.

Note: In all microprocessor interfaces, an external timer controls the CONVSTN input of the AS1534; the BUSY output interrupts the host DSP and the WBN input is logic high.

TMS32020, TMS320C25, and TMS320C5x Interface

The interface between the AS1534 and the TMS32020, TMS320C25 and TMS320C5x family of DSPs is shown in Figure 25. The memory mapped address selected for the AS1534 should be chosen to fall within the I/O memory space of the DSP.

Figure 25. TMS32020/C25/C5x Interface
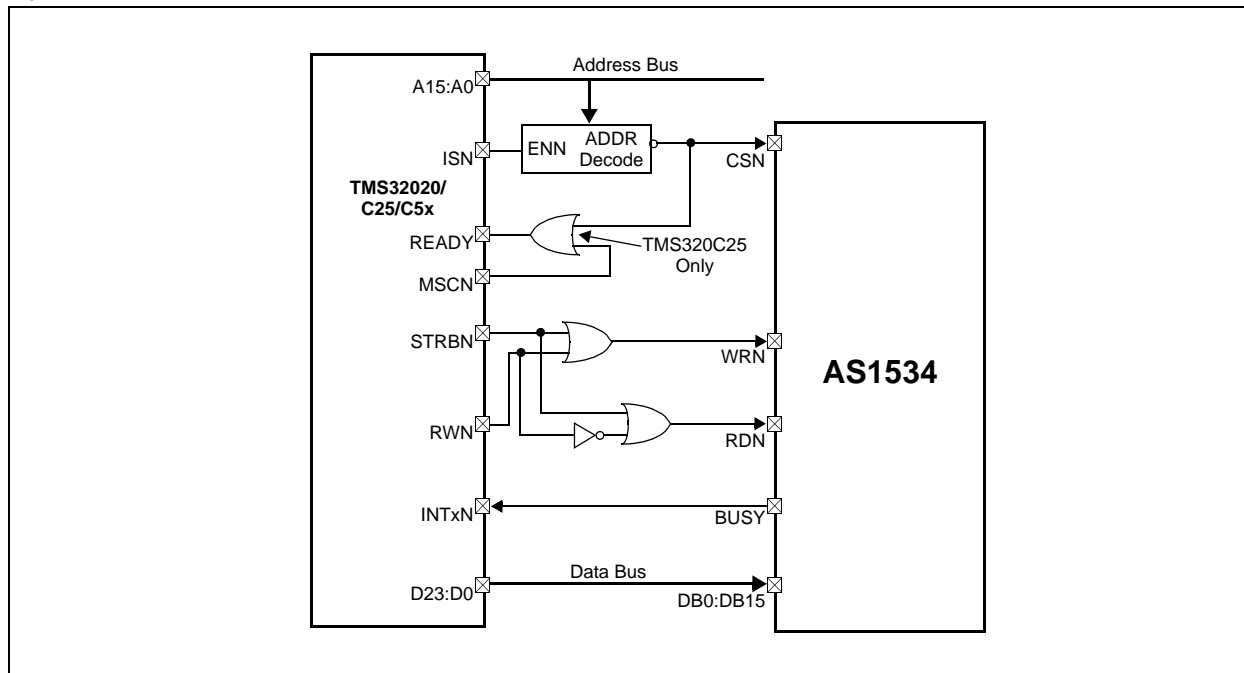
Wait state requirements for these DSPs is as follows:

- TMS32020 – The parallel interface on the AS1534 is fast enough so no extra wait states are required.

- TMS320C25 – If high speed glue logic devices are used to drive the WRN and RDN lines when interfacing to the TMS320C25, no extra wait states are required. If slower logic is used, the insertion of one wait state may be required since data accesses may be slowed sufficiently when reading from and writing to the AS1534. This wait state can be generated using the single OR gate to combine the CSN and MSC signals to drive the READY line of the TMS320C25, as shown in Figure 25.

- TMS320C5x – Extra wait states will be necessary with this DSP at its fastest clock speeds. Wait states can be programmed via the TMS320C5x IOWSR and CWSR registers (see the *TMS320C5x User Guide* for details).

Data can be read from the AS1534 using the instruction:

<div align="center">IN D,ADC</div>

Where:

D is the memory location where the data is to be stored.
ADC is the I/O address of the AS1534.

TMS320C30 Interface

The parallel interface between the AS1534 and the TMS320C3x family of DSPs is shown in Figure 26. The AS1534 is interfaced to the expansion bus of the TMS320C3x. A single wait state is required in this interface. This can be programmed using the WTCNT bits of the Expansion Bus Control Register (see the *TMS320C3x Users Guide* for details).
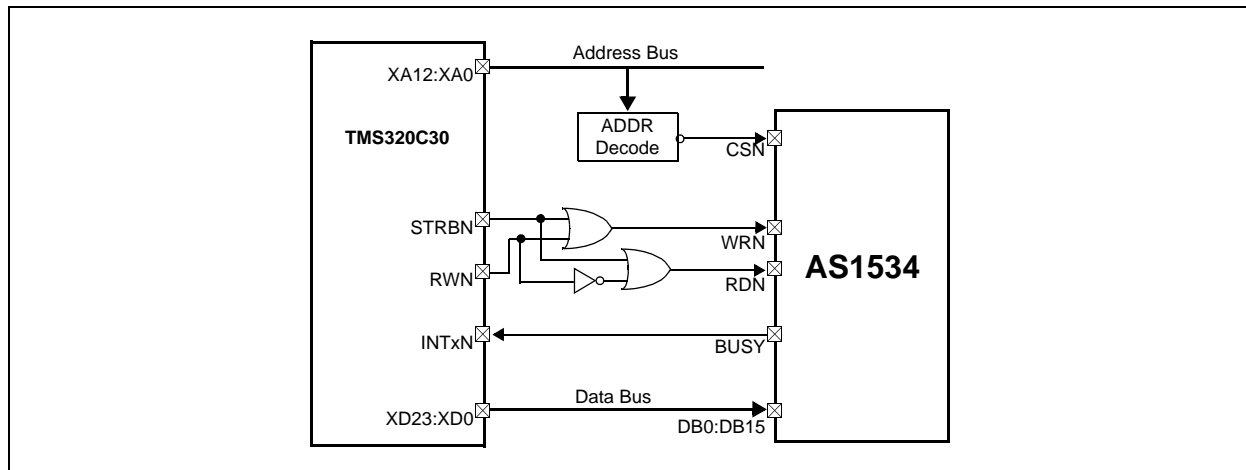
Data can be read from the AS1534 using the instruction:

LDI *ARn,Rx

Where:

ARn is an auxiliary register containing the lower 16 bits of the AS1534 address in the TMS320C3x memory space. *Rx* is the register into which the ADC data is loaded.

Figure 26. TMS320C30 Interface

DSP5600x Interface

The parallel interface between the AS1534 and the DSP5600x series of DSPs is shown in Figure 27. The AS1534 should be mapped into the top 64 locations of Y data memory. If extra wait states are needed in this interface, they can be programmed using the Port A Bus Control Register (see the *DSP5600x Users Manual* for details).

Data can be read from the AS1534 using the instruction:

MOVEO Y:ADC,X0

Where:

ADC is the address in the DSP5600x address space to which the AS1534 has been mapped.

Figure 27. DSP5600x Interface
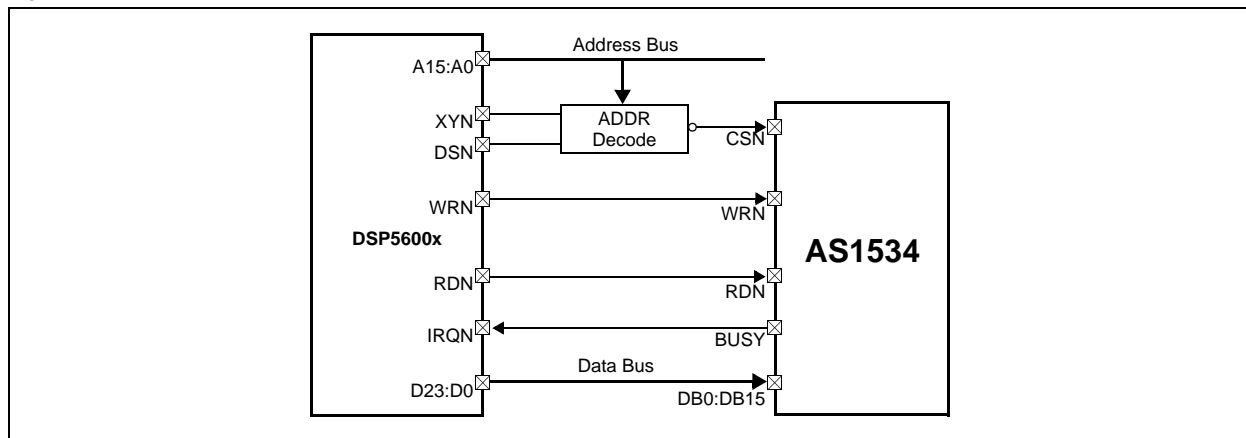
ADSP-21xx Interface

The parallel interface between the AS1534 and the ADSP-21xx series of DSPs is shown in Figure 28. The AS1534 should be configured as a memory mapped device. A single wait state may be necessary to interface the AS1534 to the ADSP-21xx depending on the clock speed of the DSP. This wait state can be programmed via the ADSP-21xx Data Memory Waitstate Control Register (see the *ADSP-2100 Family Users Manual* for details).

Data can be read from the AS1534 using the instruction:

$$MR = DM(ADC)$$

Where:

ADC is the address of the AS1534.

Figure 28. ADSP-21xx Interface
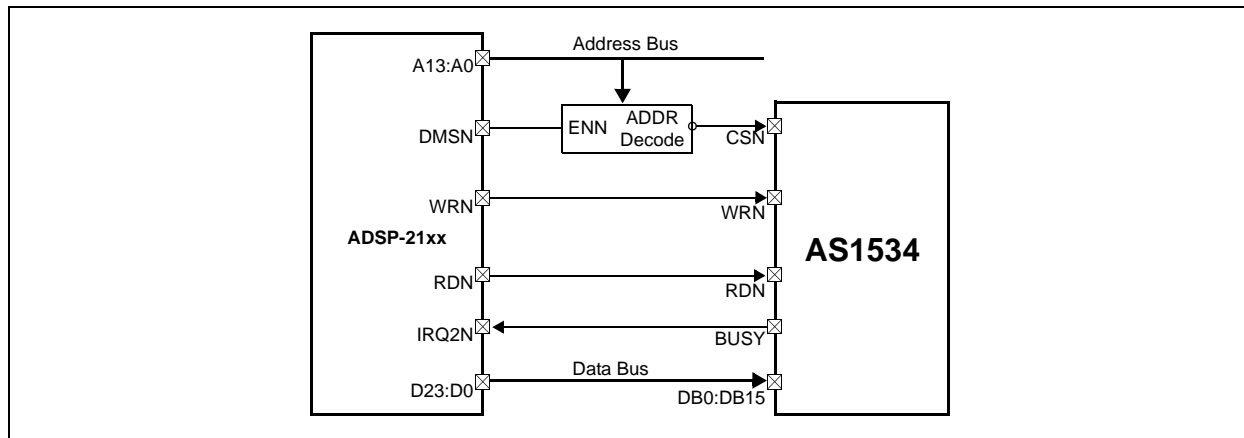
8051 Interface

The parallel interface between the AS1534 and the 8051 microcontroller is shown in Figure 29. This interface can be used to connect the AS1534 directly to microprocessors with an 8-bit data bus.

The AS1534 is put into byte-mode by placing a logic low signal on pin WBN. In Figure 29, pin WBN is tied logic low and pin DB8/HBEN is connected to line 1 of Port 2. Port 0 serves as a multiplexed address/data bus to the AS1534. Alternatively if the 8051 is not using external memory or other memory mapped peripheral devices, line 2 of Port 2 (or any other line) could be used as the CSN signal.

Figure 29. 8051 Interface
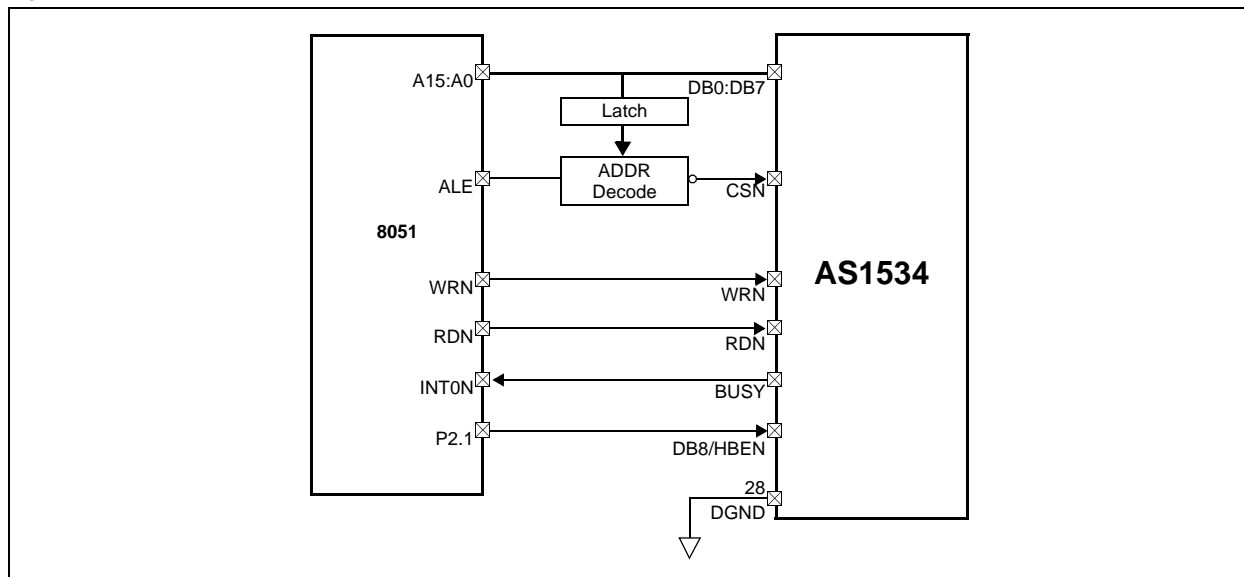
Transfer Functions

For the unipolar range, the designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS –3/2 LSBs). The output coding is straight binary for the unipolar range with 1 LSB = FS/4096 = 3.3 V/4096 = 0.8 mV when V_{REF} = 3.3 V. Figure 14 on page 13 shows the unipolar analog input configuration; the ideal input/output transfer characteristic for the unipolar range is shown in Figure 30.
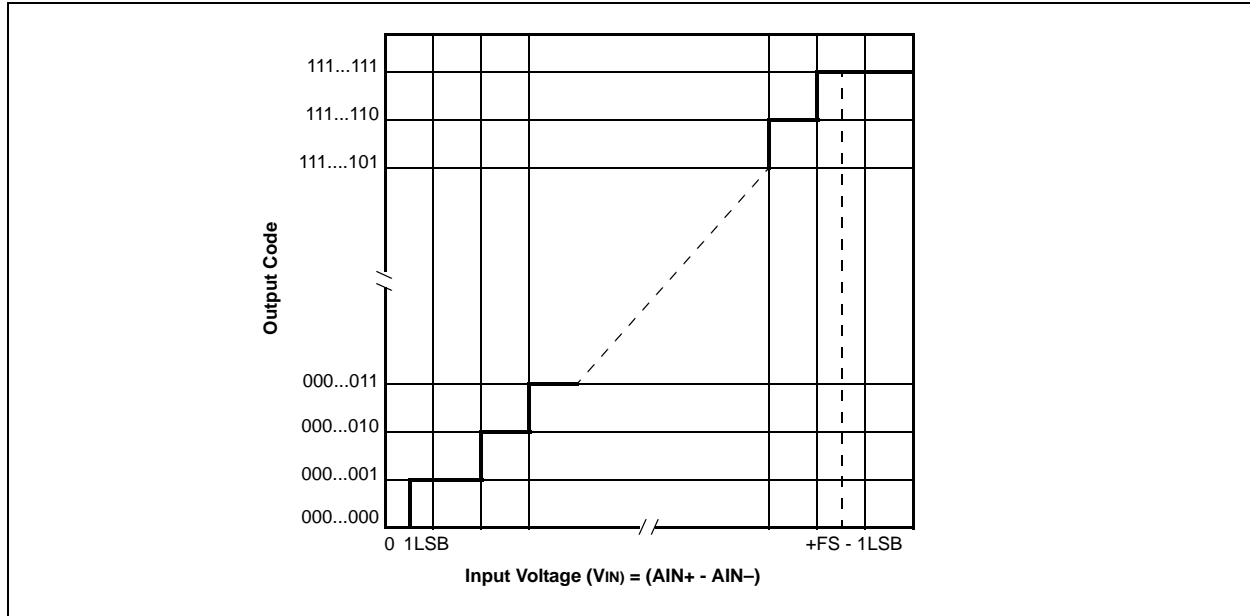
Figure 30. Unipolar Transfer Function

Figure 15 on page 13 shows the AS1534 ±V_{REF}/2 bipolar analog input configuration. AIN+ cannot go below 0V so for the full bipolar range, AIN– should be biased to at least +V_{REF}/2. The designed code transitions occur midway between successive integer LSB values. The output coding is two's complement with 1 LSB = 4096 = 3.3 V/4096 = 0.8 mV. The ideal input/output transfer characteristic is shown in Figure 31.

Figure 31. Bipolar Transfer Function
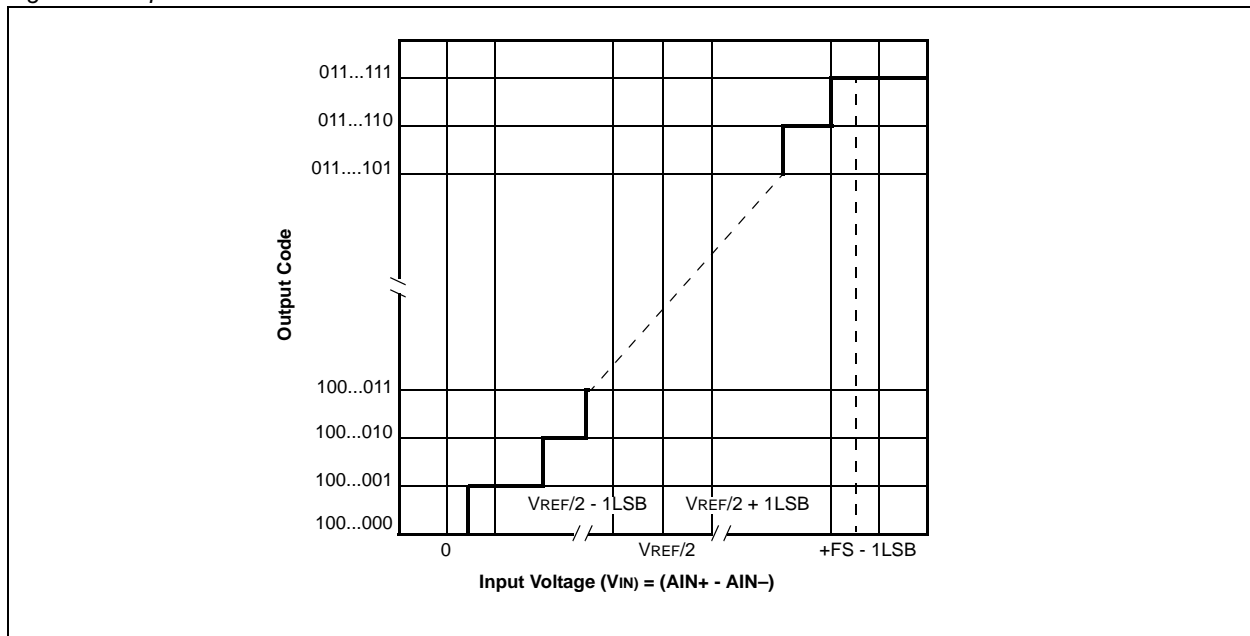
DC and AC Application Notes

For DC applications, high source-impedances are acceptable provided the acquisition time (t_{ACQ}) between conversions is long enough for the 20pF capacitor to fully charge. For example with R_{IN} = 5kΩ, the required t_{ACQ} is 922ns. For AC applications, high-frequency components greater than the Nyquist frequency should be removed from the analog input signal by using a low-pass filter on the AIN+ pin as shown in .

In applications where THD and SNR ratio are critical, the analog input should be driven from a low-impedance source. Large source impedances significantly affect the AC performance of the ADC circuit, and the use of an input buffer amplifier may be required.

Note: Input buffer amplifier selection is a function of the specific application for which the AS1534 is intended.

The maximum source impedance depends on the acceptable amount of THD. THD increases as the source impedance increases. With the configuration shown in , the THD is at the -90 dB level. With a source impedance of 1kΩ and no capacitor on the AIN+ pin, THD increases with frequency.

In a single-supply application (3 or 5V), the V+ and V– of the op amp can be taken directly from the supplies to the AS1534 which eliminates the need for extra external power supplies. When operating with Rail-to-Rail inputs and outputs at frequencies greater than 10kHz, selection of the op amp should be specific to the application. In particular, for single-supply applications the input amplifiers should be connected in a gain of –1 arrangement to get the optimum performance. Figure 13 shows the arrangement for a single supply application with a 50Ω/10nF low-pass filter (cutoff frequency 320kHz) on the AIN+ pin.

Note: Use a 10nF capacitor with good linearity to ensure excellent AC performance.

Layout Considerations

The AS1534 requires proper layout and design techniques for optimum performance.

- The analog and digital supplies of the AS1534 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The AS1534 has excellent immunity to noise on the power supplies as can be seen by the PSRR versus Frequency graph . Nonetheless, care should still be taken with regard to grounding and layout.

- Mount the AS1534 on the PCB such that the analog and digital sections are separated and confined to independent areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum-etch technique is generally best for ground planes as it gives the best overall shielding.

- Digital and analog ground planes should be joined in only one place. If the AS1534 is the only device requiring an AGND-to-DGND connection, the ground planes should be connected at the AGND and DGND pins of the AS1534. If multiple devices require AGND-to-DGND connections, the connection should still be made at a star ground point which should be established as close to the AS1534 as is practical.

- Avoid running digital lines under the AS1534 as these couple noise onto the die.

- The analog ground plane should be allowed to run under the AS1534 to avoid noise coupling.

- The power supply lines to the AS1534 should use as traces as large as is practical to provide low-impedance paths and to reduce the effects of transient signals on the power supply line.

- Fast switching signals (e.g., clocks and data inputs) should be shielded with digital ground to avoid radiating noise to other sections of the PCB.

- Clock signals should not be run near the analog inputs.

- Avoid crossover of digital and analog signals. Traces on opposite sides of the PCB should run at right angles to each other. This reduces the effects of feed-through of the board. A micro-strip technique is the best because the component side of the board is dedicated to ground planes while signals are placed on the solder side, although it is not always possible with a double-sided board.

- All analog supplies should be decoupled with a 10µF tantalum capacitor in parallel with 0.1µF disc-ceramic capacitor to AGND. All digital supplies should have a 0.1µF disc-ceramic capacitor to DGND. To achieve the best performance from these decoupling components, place them as close to the device as is practical, ideally directly adjacent to the device.

- In systems where a common supply voltage is used to drive both the AVDD and DVDD of the AS1534, the system AVDD supply should be used. In this case an optional 10Ω resistor between pin AVDD and pin DVDD can help to filter noise from digital circuitry. This supply should have the recommended analog supply decoupling capacitors between pins AVDD of the AS1534 and AGND and the recommended digital supply decoupling capacitor between pins DVDD of the AS1534 and DGND.

10 Package Drawings and Markings

The AS1534 is available in a 44-pin PQFP package.

Figure 32. 44-pin PQFP Package

DETAIL 'A'
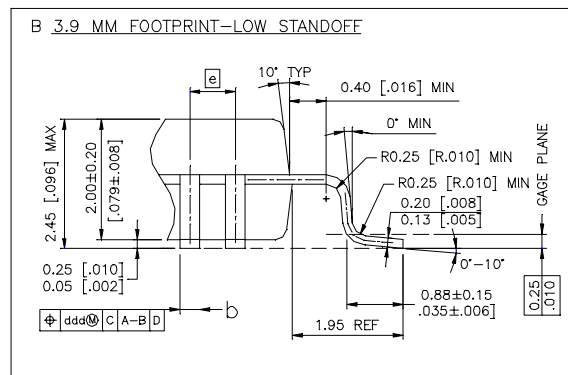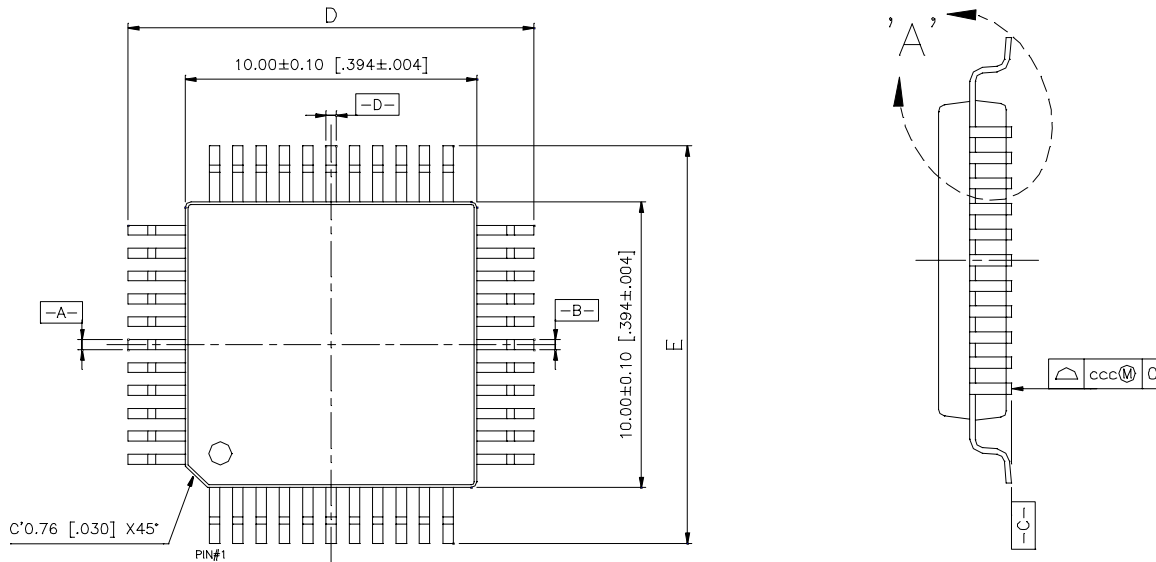
Variations					
e	**b**			**ccc**	**ddd**
	Min	**Typ**	**Max**		
0.80	0.30	0.37	0.45	0.10	0.20
.031	.012	.015	.018	.004	.008

D and E Variations with Respect to Footprint			
Symbol	**3.9 FP-LS**		
	Min	**Typ**	**Max**
D	13.65	13.90	14.15
	.537	.547	.557
E	13.65	13.90	14.15
	.537	.547	.557

Notes:

1. Controlling dimension is millimeters.

11 Ordering Information

The device is available as the following standard products.

Model	Description	Delivery Form	Package
AS1534	Single-Supply, Low-Power, 200ksps A/D Converter	Tray	PQFP 44-pin
AS1534-T	Single-Supply, Low-Power, 200ksps A/D Converter	Tape and Reel	PQFP 44-pin

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