AS3668

4 Channel Breathlight Controller

1 General Description

The AS3668 is a 4-channel LED driver designed to produce lighting effects for portable devices. A highly efficient charge pump enables LED driving over full Li-Ion battery voltage range. The device is equipped with an internal program memory, which allows control of LED patterns even without processor control. This helps the whole system to save power and extend for example battery life time in every mobile application. The AS3668 maintains excellent efficiency over a wide operating range by automatically selecting the best charge pump gain based on the LED forward voltage requirements and the device input voltage.

Furthermore the chip supports an automatic power-save mode which gets active when LED outputs are not active. The special power-save mode has a extremely low current consumption below 10µA (typ.).the AS3668 has an I2C-compatible control interface which supports two slave address without having a dedicated address selection pin. For fancy lighting effects synchronized with an audio signal the device supports special digital filter modes in order to make music literally visible on the 4 independent configurable current sources.

The AS3668 is available in a very tiny 12-pin WL-CSP (1.255x1.680mm) 0.4mm pitch package.

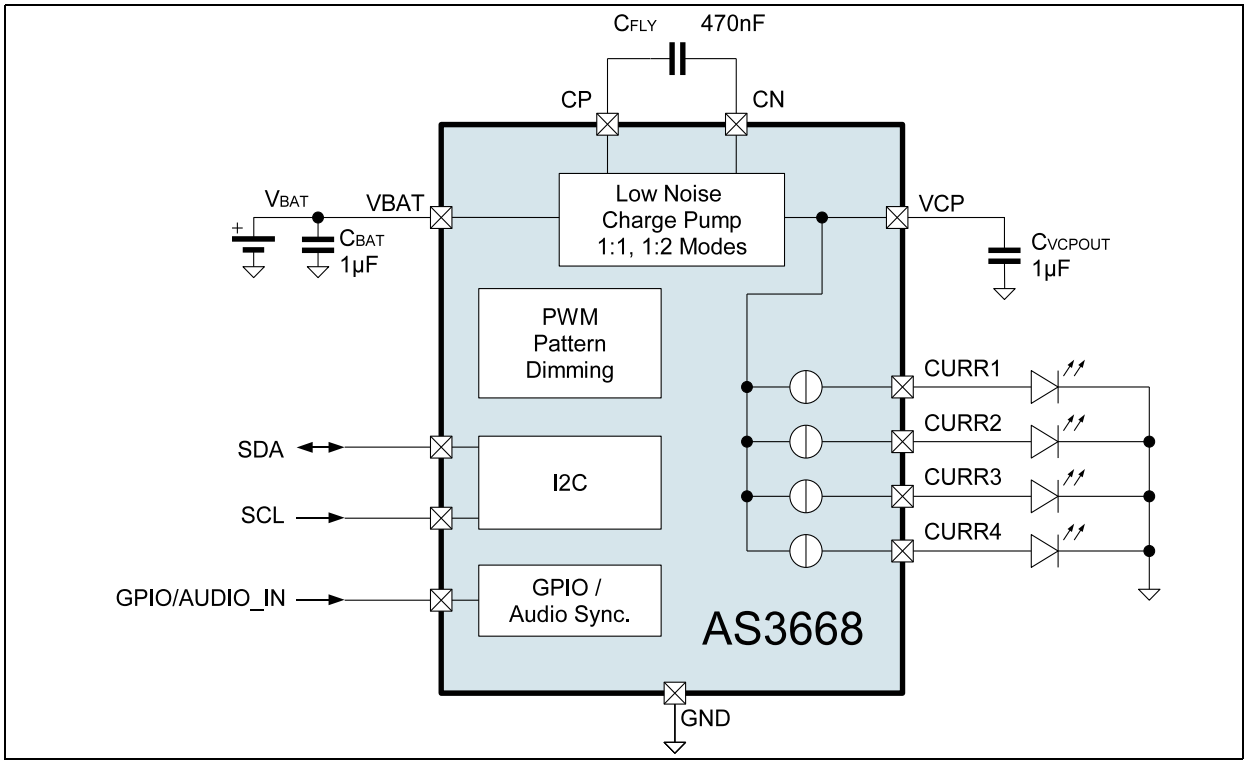
2 Key Features

- High efficiency capacitive 60mA charge pump with 1:1 and 1:2 mode
- Automatic mode switching for charge pump
- Automatic Pattern Mode without digital control
- Highly accurate 4 Channel High Side 25.5mA current sources
- Audio Controlled Lighting with internal digital filters
- Charge Pump with soft start and overcurrent/short circuit protection
- Integrated “easy to use” pattern generator for breathlight LED function with logarithmic dimming
- Small application circuit
- Minimum number of external components
- Available in 12-pin WL-CSP (1.255x1.680mm) with 0.4mm pitch

3 Applications

The product is perfect for Mobilephones, MP3 Player, Portable Navigation Devices, Digital Cameras, USB Dongles/Modems, Game Controllers and can be used for fun and indicator lights, backlighting and as programmable current sources.

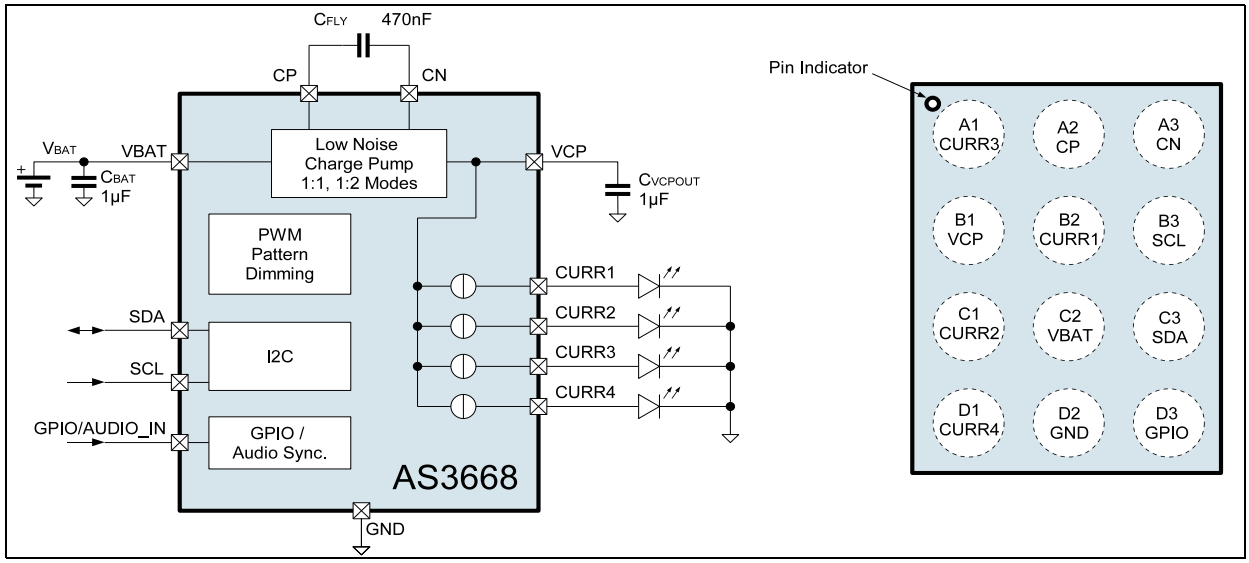
Figure 1. AS3668 Block Diagram



Contents

4 Pin Assignments

Figure 2. Pin Assignments 12-pin WL-CSP (1.255x1.680mm)(Top View)



4.1 Pin Description

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
V_{BAT}	C2	**Positive Power Supply Input** for AS3668.
GND	D2	**Signal and Power Ground**. Provide a short, direct PCB path between this pin and the negative side of the output capacitor of the charge pump capacitor C_{VCPOUT}.
SCL	B3	**Serial Clock Input** for the two wire I2C interface.
SDA	C3	**Serial-Data I/O** for I2C interface. This pin is a open drain digital I/O which requires a pull up resistor for data transfer.
GPIO/AUDIO_IN	D3	**General Purpose Input/Output or Audio Input.** Depending on AS3668 configuration this pin provided three different features. It can either be configured as general purpose input/output[1] or as analogue audio input for music playback synchronization of AS3668 with an audio source. Furthermore it is possible to use it as power up pin starting up with a default PWM pattern sequence for LED1. If the pin is not used it is mandatory to connect it to ground.
CURR1	B2	**CURR1 Output**. This pin is a current source output which can be used to operate a LED. The current source is internally connected to V_{CP}. If the AS3668 is powered up with GPIO/AUDIO_IN pin this current source is active with a default PWM pattern.
CURR2	C1	**CURR2 Output**. This pin is a current source output which can be used to operate a LED. The current source is internally connected to V_{CP}.
CURR3	A1	**CURR3 Output**. This pin is a current source output which can be used to operate a LED. The current source is internally connected to V_{CP}.
CURR4	D1	**CURR4 Output**. This pin is a current source output which can be used to operate a LED. The current source is internally connected to V_{CP}.
V_{CP}	B1	**Charge Pump Output.** This pin requires an external blocking capacitor. The capacitor must be placed as close as possible to V_{CP} terminal.
CP	A2	**Charge Pump Flying Capacitor.** This is the positive terminal for the charge pump flying capacitor. The capacitor should be placed as close as possible to AS3668. In addition it is mandatory to keep the signal trace between the capacitor and CP terminal as short as possible.
CN	A3	**Charge Pump Flying Capacitor.** This is the negative terminal for the charge pump flying capacitor. The capacitor should be placed as close as possible to AS3668. In addition it is mandatory to keep the signal trace between the capacitor and CN terminal as short as possible.

1. The output is an open-drain output only. Therefore an external Pull-Up resistors is required for output operation.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V_{BAT}, V_{CP}, CN, CP to GND	-0.3	7	V	
V_{CP} to GND	-0.3	7	V	Protection diode between V_{CP} and GND
LED1, LED2, CURR3, CURR4 to GND	-0.3	7	V	
SCL, SDA, GPIO/AUDIO_IN to GND	-0.3	7	V	
Input Pin Current without causing latch up	-100	+100	mA	At 25ºC, Norm: EIA/JESD78
Electrostatic Discharge				
ESD HBM (CURR1 to CURR4)	2		kV	JEDEC JESD22-A114
ESD HBM (all other pins)	2		kV	
ESD MM	100		V	JEDEC JESD22-A115
ESD CDM	500		V	JEDEC JESD22-C101
Storage Temperature Range	-55	+125	ºC	
Temperature Ranges and Storage Conditions				
Continuous Power Dissipation		0.83	W	Internally limited (over temperature protection)[1]
Storage Temperature Range	-55	+125	ºC	
Junction to Ambient Thermal Resistance (θ_{JA})[2]		60	°C/W	
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	1			Represents a max. floor life time of unlimited.
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/ JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".*

1. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 140°C (typ.) and disengages at T_J = 135°C (typ.).
2. Junction to ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

6 Electrical Characteristics

V_{BAT} = 3.6V, C_{BAT} = C_{VCPOUT} = 1µF, C_{FLY} = 470nF, T_{AMB} = -30ºC to +85ºC, typical values @ T_{AMB} = +25ºC (unless otherwise specified) .

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
General Operating Conditions						
V_{BAT}	Supply Voltage		2.7		5.5	V
I_{VBAT}	Standby supply current	SCL = 0V and GPIO = 0V		0.2	3	µA
	Normal Mode supply current	SCL = V_{BAT} and SDA = V_{BAT}, no I2C communication and no internal block enabled		10		µA
		Charge pump in 1x mode, no load, current source outputs disabled		70		µA
		Charge pump in 2x mode, no load, current source outputs disabled		2.5		mA
f_{OSC}	Internal Oscillator Frequency Accuracy		-10		+10	%
T_{AMB}	Operating Temperature[1]		-30	25	85	°C
Charge Pump						
R_{OUT}	Charge Pump Output Resistance	Operating Mode 1:1		2		Ω
		Operating Mode 1:2; V_{BAT} = 3.0V		20		
f_{SW}	Switching Frequency			1		MHz
t_{ON}	V_{CP} Turn-On Time[2]	no load, current sources CURR1 - CURR4 deactivated		30		µs
		I_{OUT} = 50mA, current sources CURR1 - CURR4 deactivated		40		µs
Current Sources						
I_{LEAK}	Leakage Current (LED1 to CURR4)	PWM = 0%		0.1	1	µA
I_{MAX}	Maximum Source Current	Outputs CURR1 to CURR4		25.5		mA
I_{OUT}	Output Current Accuracy	Output Current set to 25.5 mA	-15		+15	%
I_{MATCH}	Matching Accuracy	Output Current set to 25.5 mA	-10		+10	%
f_{LED}	Switching Frequency	PWM mode with internal oscillator		122		Hz
Logic Interface						
Logic Input SCL, SDA and GPIO/AUDIO_IN						
V_{IL}	Input Low Level				0.52	V
V_{IH}	Input High Level		1.38		V_{BAT}	V
I_{IN}	Input Current		-1.0		1.0	µA
V_{OLGPIO}	Low Level Output voltage	Pin GPIO/AUDIO_IN at 4mA		0.2		V
V_{HYS}	Hysteresis			0.1		V
f_{EXT}	External PWM input	Only possible with GPIO/AUDIO_IN			1	MHz
Analogue Input						
Analogue Audio Input GPI/AUDIO_IN						
V_{AUDIO}	Input Signal Level				2.5	V_{PEAK}
R_{AUDIO_IN}	Audio Input Resistance	Audio Preamplifier Gain = -6dB		400		kΩ
		Audio Preamplifier Gain = +20dB		60		kΩ

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{AUDIO_IN}	Input Capacitance			10		pF
A_{Audio}	Programmable Amplifier Gain		-6		25	dB

1. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 140°C (typ.) and disengages at T_J = 135°C (typ.).
2. Turn-on time is measured from the moment the charge pump is activated until the V_{CP} crosses 90% of its target value

6.1 Timing Characteristics

VBAT = 3.6V, CBAT = CVCPOUT = 1µF, CFLY = 470nF, TAMB = -30ºC to +85ºC, typical values @ TAMB = +25ºC (unless otherwise specified) .

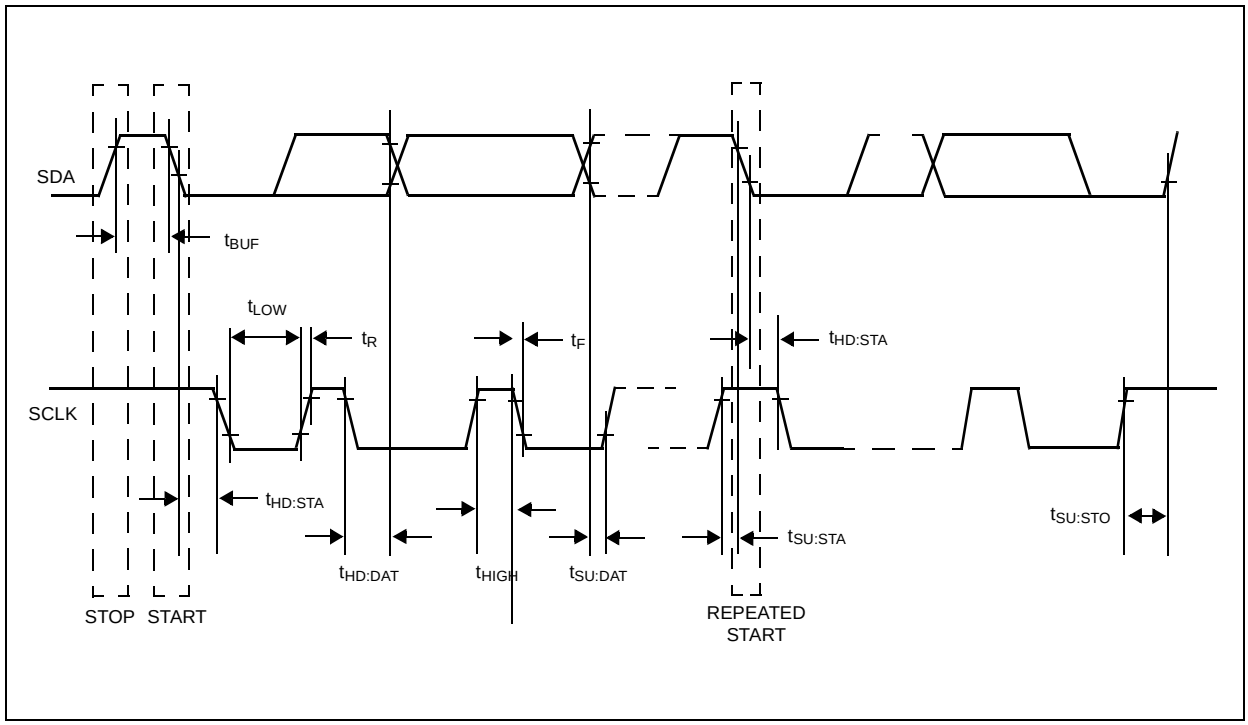
Table 4. Electrical Characteristics I²C[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I2C mode timings - see						
fSCLK	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START Condition		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) START Condition[2]		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time[3]		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time[4]		100			ns
t_R	Rise Time of Both SDA and SCL Signals		20 + 0.1C_B		300	ns
t_F	Fall Time of Both SDA and SCL Signals		20 + 0.1C_B		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	C_B — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

1. Specification is guaranteed by design and is not tested in production. V_{EN} = 1.65V to VBAT.
2. After this period the first clock pulse is generated.
3. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.
4. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCLK line is released.

6.2 Timing Diagrams

Figure 3. I2C Mode Timing Diagram



7 Typical Operating Characteristics

V_{BAT} = 3.6V, C_{BAT} = C_{VCPOUT} = 1µF, C_{FLY} = 470nF, T_{AMB} = -30ºC to +85ºC, typical values @ T_{AMB} = +25ºC (unless otherwise specified).

Figure 4. Off Mode Current vs. VBAT

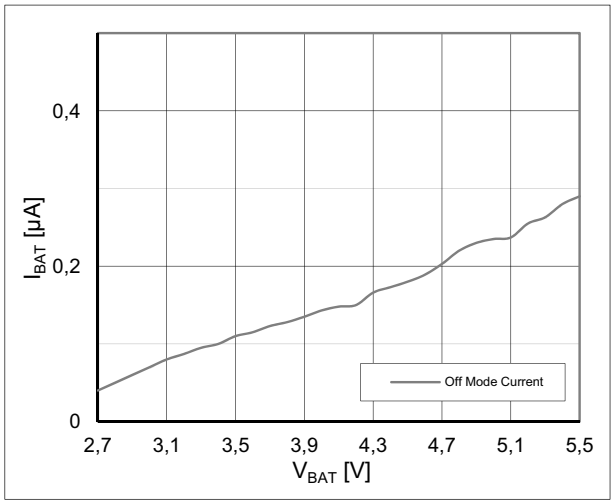


Figure 5. CURRx linearity (0mA - 25.5mA) vs. Code

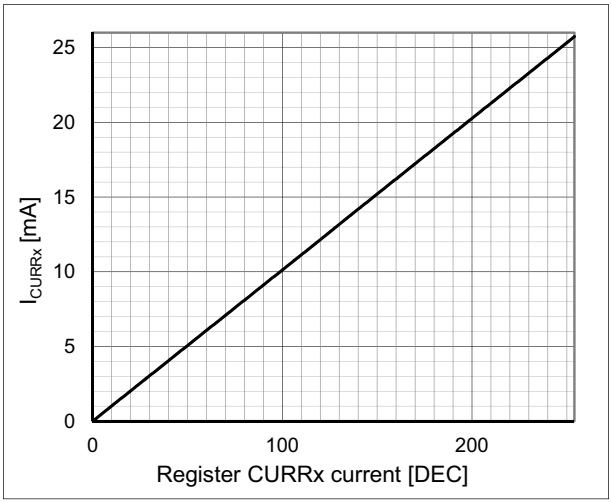


Figure 6. Output Voltage vs. load current (1:1, 4.2V,3,6V, 3,3V) L

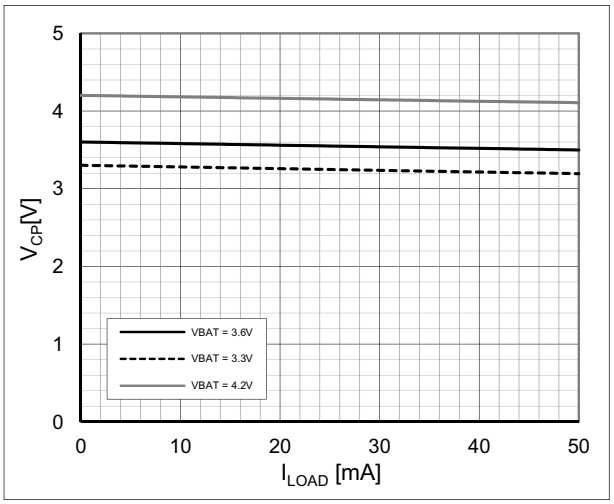


Figure 7. Output voltage. vs. load current (1:2, 4.2V,3,6V, 3,3V)

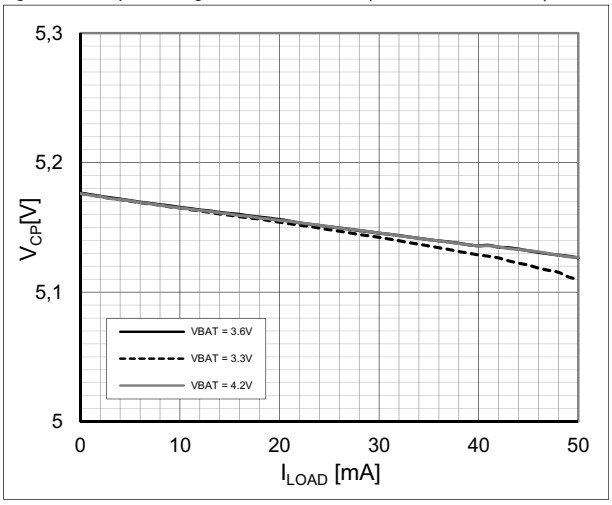


Figure 8. CP Efficiency vs.VBAT in 1:2 MODE(10mA,30mA,60mA)

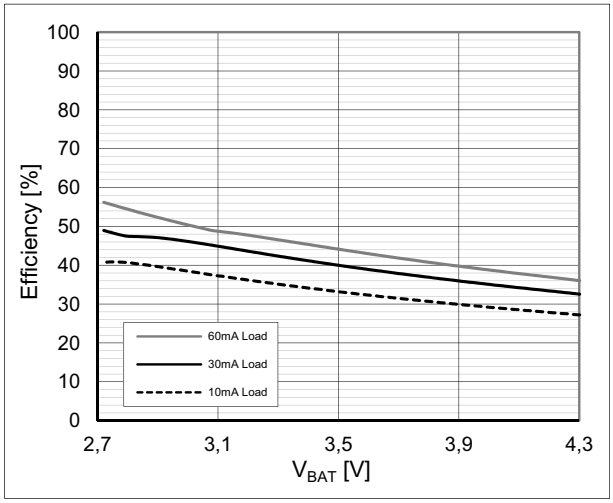


Figure 9. CP Efficiency vs. VBAT in 1:1 Mode(10mA,30mA,60mA)

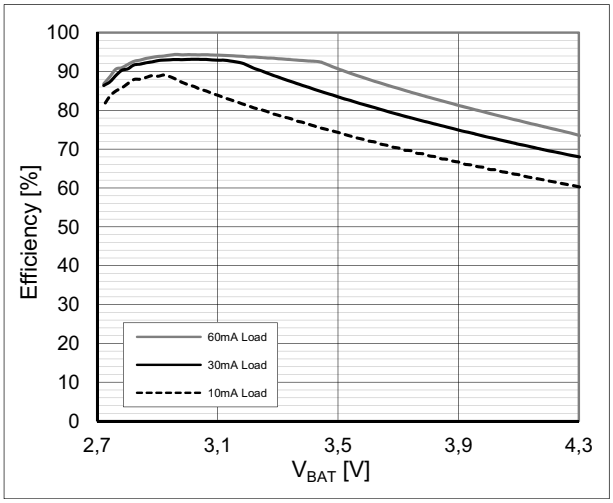


Figure 10. CURRx logarithmic PWM Ramp

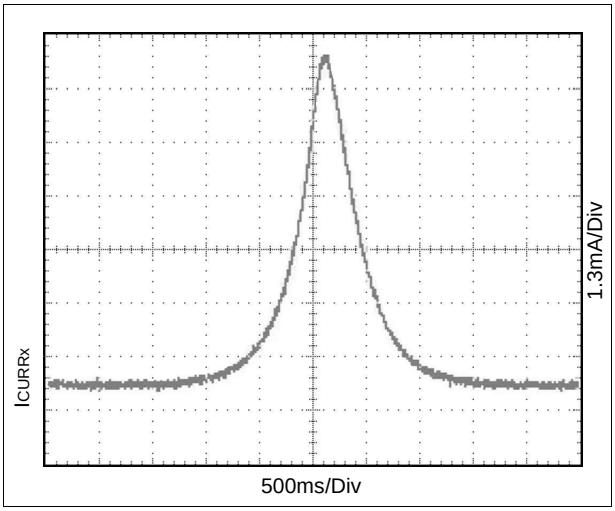


Figure 11. VCP and VBAT in 1:2 Mode and 50mA load current

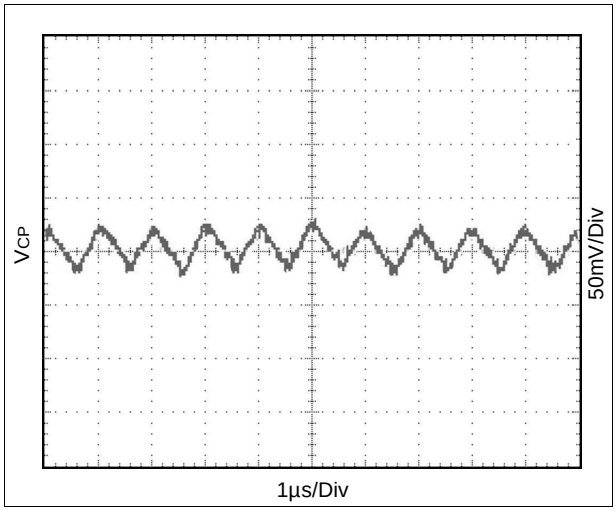


Figure 12. VCP with charge pump in 1:2 mode and 10mA load current

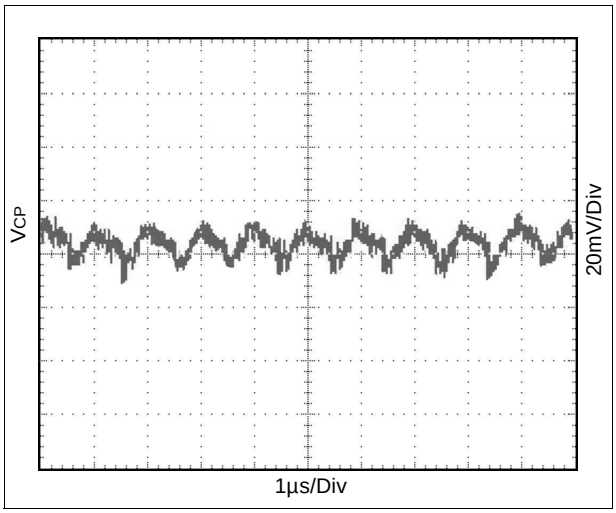


Figure 13. Line Regulation autom. gain change to 1:2 mode with 1mA load current

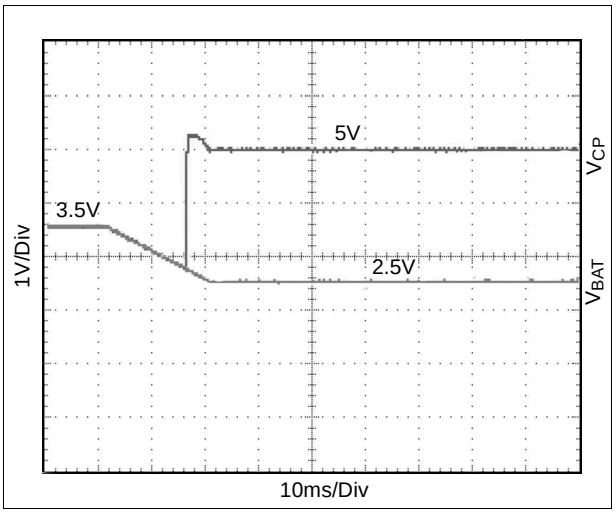


Figure 14. Line Regulation autom. gain change to 1:2 mode with 10mA load current

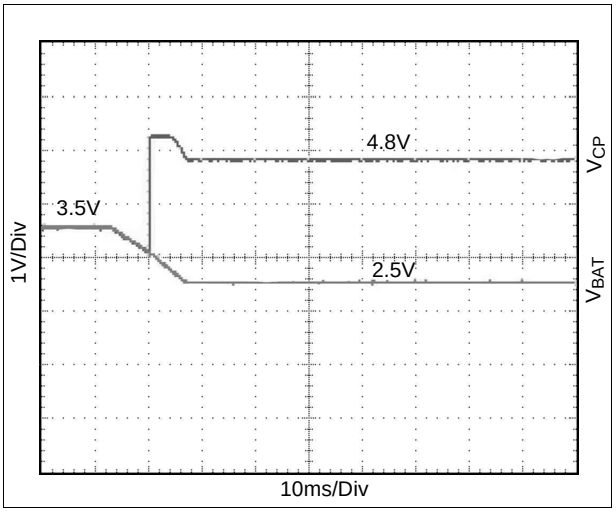


Figure 15. Line Regulation autom. gain change to 1:2 mode with 25.5mA load current

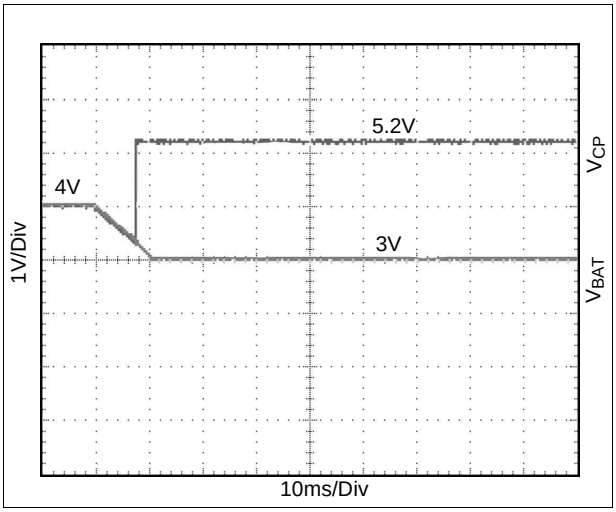


Figure 16. Output current of CURRx vs. U(CURRx) with 25,5mA CURRx output current

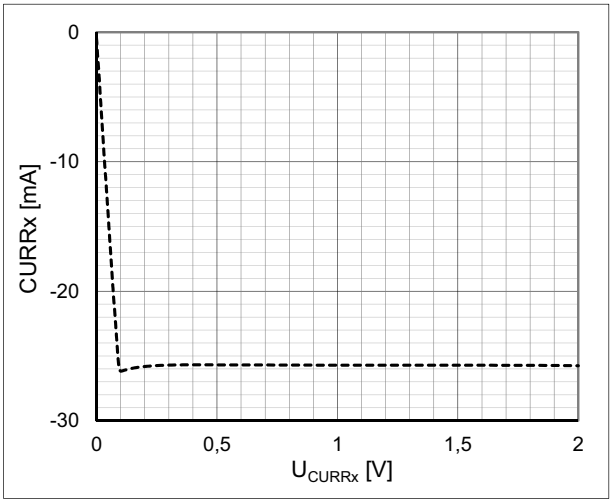


Figure 17. Output current of CURRx vs. U(CURRx) with 10mA CURRx output current

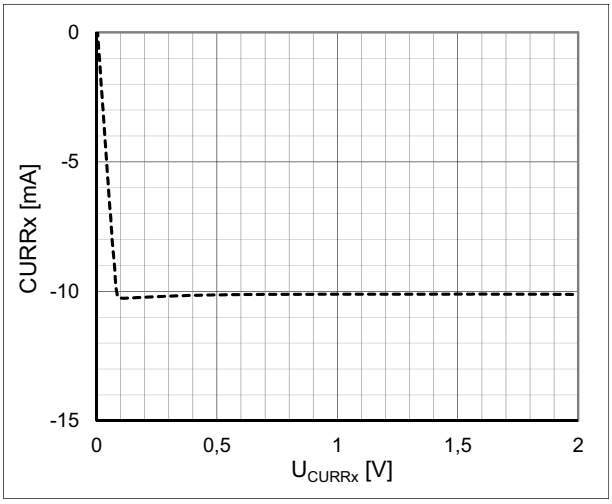


Figure 18. Output current of CURRx vs. U(CURRx) with 1mA CURRx output current)

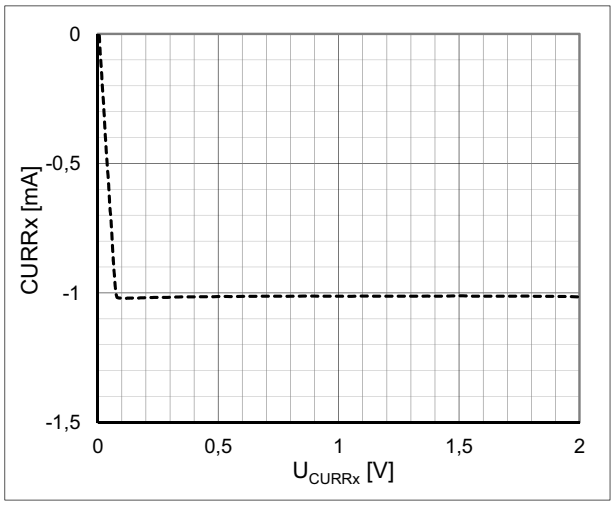


Figure 19. Battery Current vs. VBAT with CP in 1:2 Mode (10mA, 30mA, 60mA

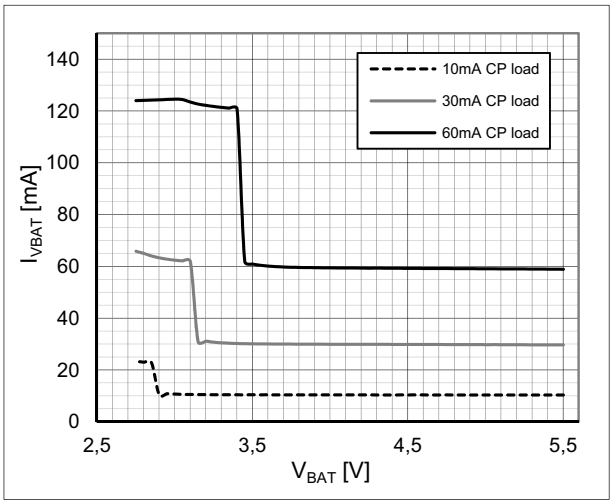


Figure 20. CP efficiency vs. VBAT with automatic CP mode switching

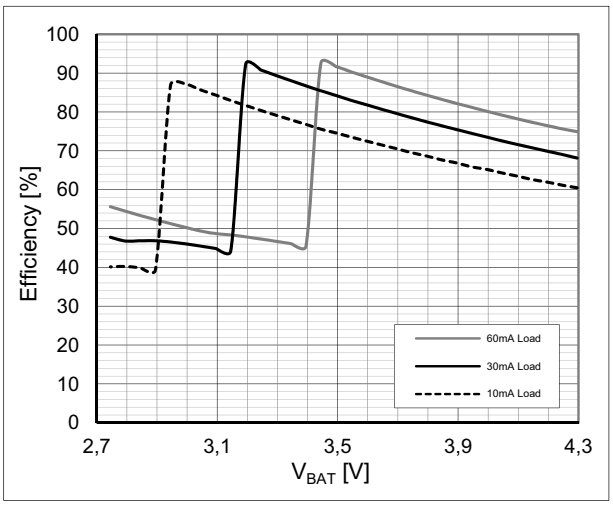
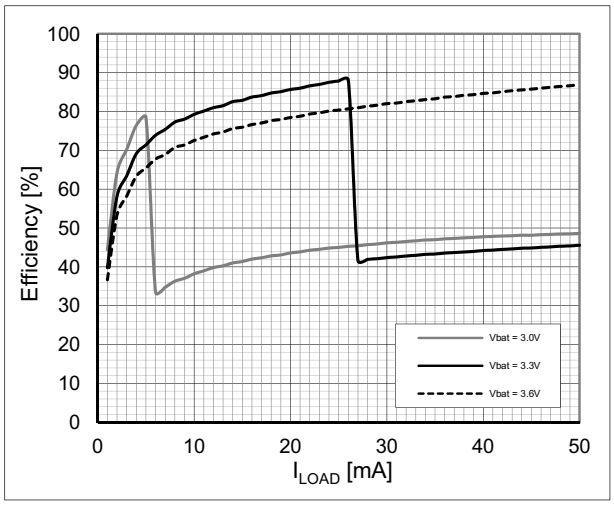


Figure 21. CP efficiency vs. ILOAD with automatic CP mode switching



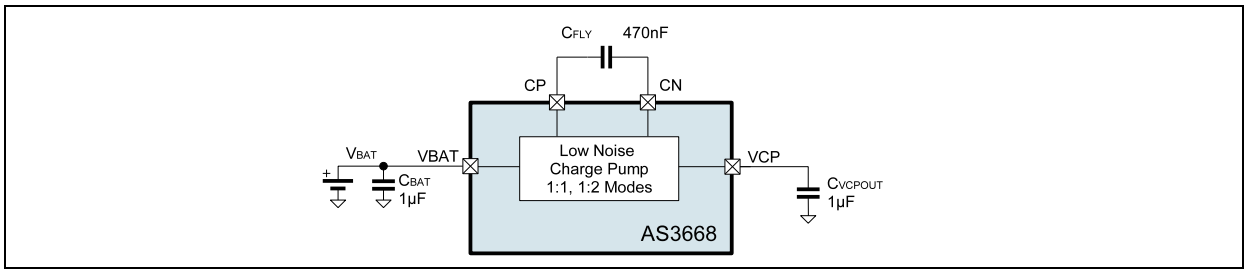
8 Detailed Description

8.1 Charge Pump

The Charge Pump uses the external flying capacitor CFLY to generate output voltages higher than the battery voltage. There are two different operating modes of the charge pump itself:

- 1:1 Bypass Mode
  - Battery input and output are connected by a low-impedance switch
  - battery current = output current.
- 1:2 Mode
  - The output voltage is up to 2 times the battery voltage (without load), but is limited to VCPOUTmax all the time
  - battery current = 2 times output current

Figure 22. Charge Pump Block Diagram .



As the battery voltage decreases, the Charge Pump must be switched from 1:1 mode to 1:2 mode in order to provide enough supply for the current sinks. Depending on the actual current the mode with best overall efficiency can be automatically or manually selected:

The charge pump mode switching can be done manually or automatically with the following possible software settings:

- Automatic
  - Start with 1:1 mode
  - Switch up automatically to 1:2 mode
- Manual
  - Set modes 1:1 and 1:2 by software

The Charge Pump requires the external components listed in the following table:

Table 5. Charge Pump External Components

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CFLY	External Flying Capacitor	Ceramic low-ESR capacitor between pins CP and CN		470		nF
CVCPOUT	External Storage Capacitor	Ceramic low-ESR capacitor between pins VCP and VSS		1.0		µF

Note: The connections of the external capacitors CVCPOUT and CFLY should be kept as short as possible.

.

Table 6. Charge Pump Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICPOUT	Output Current Continuous	Depending on PCB layout	0.0		60	mA
VCPOUTmax	Output Voltage	Internally limited, Including output ripple			5.6	V
η	Efficiency	Including current sink loss; ICPOUT = 60mA.		88		%
ICP1_2	Power Consumption without Load, fclk = 1 MHz	1:2 Mode		2.5		mA

Table 6. Charge Pump Characteristics

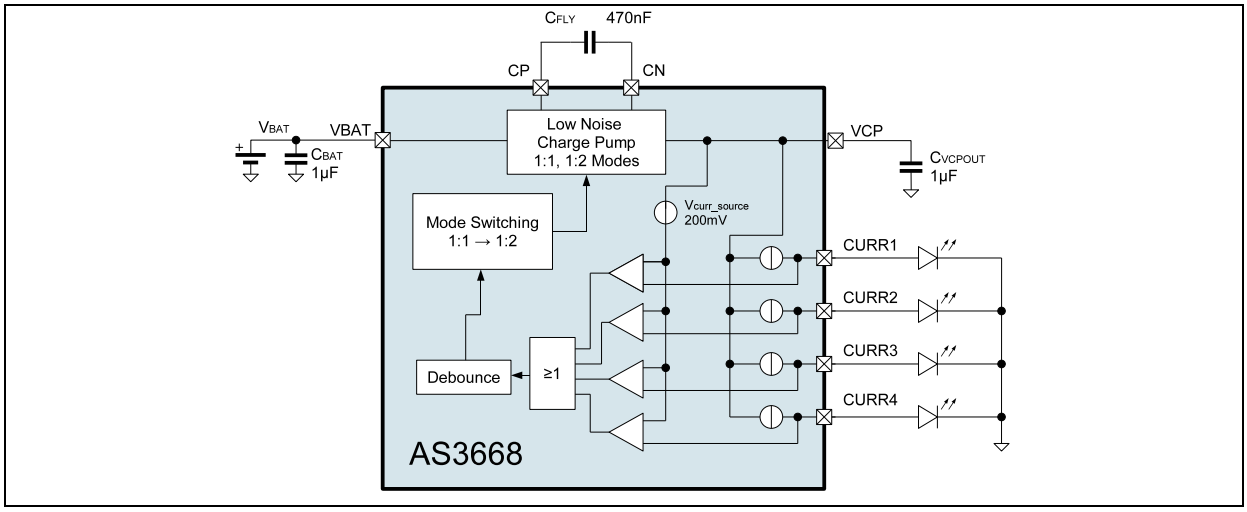
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Rcp1_1	Effective Charge Pump Output Resistance (Open Loop, fclk = 1MHz)	1:1 Mode; V_{BAT} = 3.6V		2.5		Ω
Rcp1_2		1:2 Mode; V_{BAT} = 3V		20		
fclk Accuracy	Accuracy of Clock Frequency		-10		10	%
V_{curr_source}	LED1 - CURR4 current source dropout voltage	If the voltage drops below this threshold, the charge pump will use the next available mode (1:1 -> 1:2)			0.2	V
I_{soft_start}	Current limit for soft start feature			400		mA
t_{deb}	CP automatic up-switching debounce time	cp_start_debounce=0		32		ms
		cp_start_debounce=1		200		µs

8.1.1 Charge Pump Mode Switching

If automatic mode switching is enabled the charge pump monitors the current sources, which are directly connected to the output of the charge pump V_{CP}. In order to identify the enabled current sources, the related registers should be setup before starting the charge pump. If any of the voltage on these current sources drops below the threshold (V_{curr_source}), the higher mode is selected after the debounce time (t_{deb}).

The charge pump mode switching supports only a mode change to a higher charge pump mode (e.g.: mode 1:1 to mode 1:2). In case V_{BAT} increases again during operation the automatic mode switching will not change the operation mode from 1:2 down to 1:1. In order to change the mode all current sources must be switched off to reset the charge pump mode switching mechanism. After enabling the current sources again the mode switching mechanism chooses the appropriate mode for the optimized operation of the charge pump either in 1:1 mode or 1:2 mode. In case an automatic pattern is used the current sources get a reset after each pattern cycle because the current sources are automatically switched off when executing a pattern after each cycle.

Figure 23. Charge Pump Mode Switching .



8.1.2 Soft Start

An implemented soft start mechanism reduces the inrush current. Battery current is smoothed when switching the charge pump on and also at each switching condition. This precaution reduces electromagnetic radiation significantly.

8.1.3 Unused Charge Pump

If the charge pump is not used, capacitors C_{FLY} and C_{VCPOUT} can be removed. The pins CP, CN and V_{CP} should be left open and keep register cp_on and cp_auto_on at 0 (default value).

8.1.4 Charge Pump Control Register .

Table 7. Reg Control Register

0x00 Reg Control register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	cp_on	0	R/W	This bit enables the charge pump for operation if at lease one current source is enabled and the current source has a low voltage condition. Once the charge pump is running it will be keep on even if all current sources are switched off. **0: Chargepump off** 1: Charge Pump on

Table 8. CP Control Register

0x23 Current Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6	cp_auto_on	1	R/W	This bit enables the charge pump for operation. Once at last one current source is enabled and minimum one current source has a low voltage condition the charge pump is switched on. If all current sources are switched off again the charge will also switch of automatically. 0: Chargepump off **1: Chargepump on in automatic mode**
5	cp_start_debounce	0	R/W	Selects the startup debounce time of the charge pump **0: 32ms debounce time.** 1: 240µs debounce time
4	cp_mode_switching	0	R/W	Allows the user to select between automatic mode switching or manual mode switching of the charge pump. If the bit is set, the user can change register cp_mode in order to select 1:1 mode or 1:2 mode of the charge pump. **0: Automatic CP Mode Switching** 1: Manual CP Mode Switching using register cp_mode
2	cp_mode	0	R/W	Selects the charge pump operating mode if register cp_mode_switching is set to 1. Reading the register return the mode in which the charge pump is operating, either 1:1 or 1:2 mode. **0: 1:1 mode** 1: 1:2 mode
0	cp_clk	0	R/W	Selects the charge pump clock frequency. **0: 1Mhz** 1: 500kHz

8.2 Current Sources

The AS3668 features four general purpose current sources. All current sources and be controlled independently from each other and share internally the same power supply VCP.

Table 9. Current Sink Function Overview

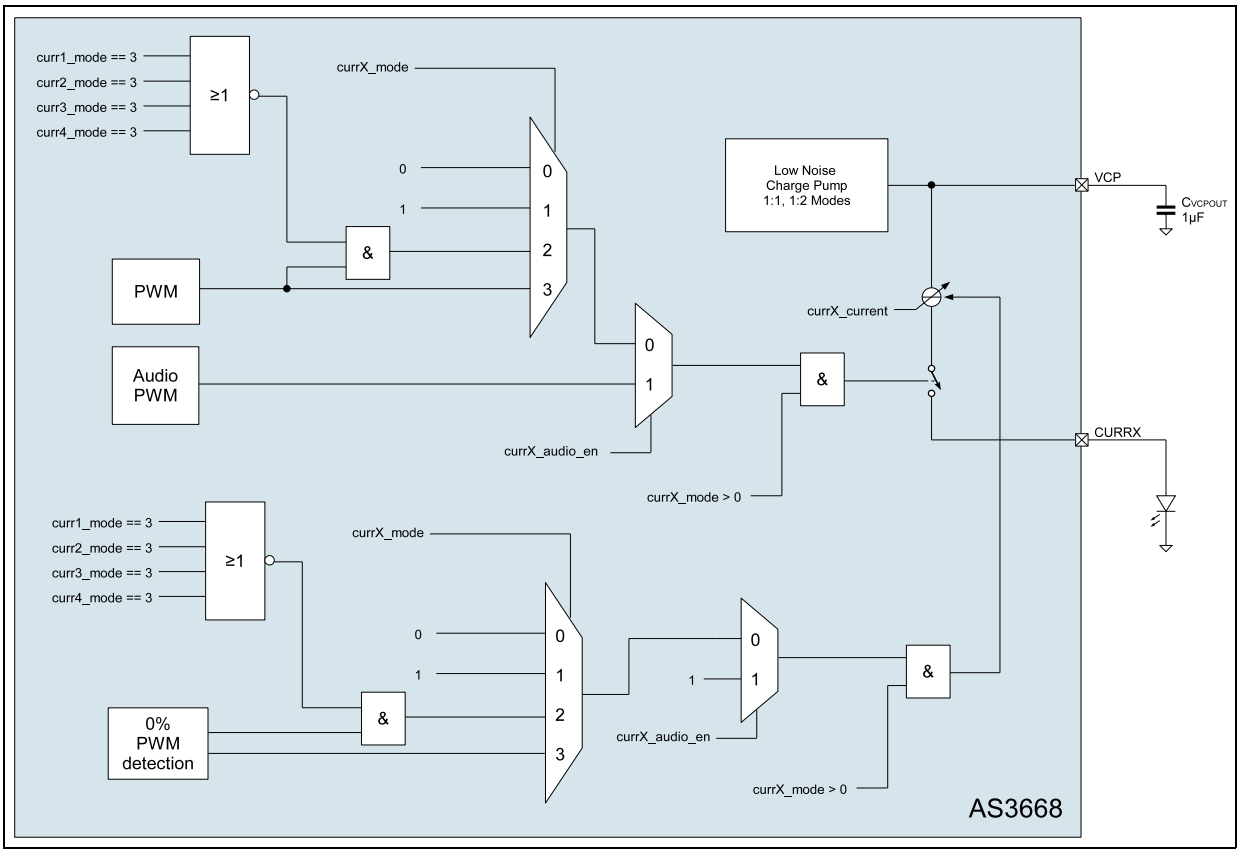
Current Sink	Max. Voltage (V)	Max. Current (mA)	Resolution		Software Current Control	Hardware On/Off Control
			(Bits)	(mA)		
CURR1	5.5	25.5	8	0.1	Separate for each current source	Internal PWM; external PWM at GPIO/AUDIO_IN, Pattern generator
CURR2						
CURR3						
CURR4						

.

Table 10. Current Sources Characteristiks

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{BIT7}	Current sink if Bit7 = 1	CURR1, CURR2, CURR3, CURR4 > 0.2V		12.8		mA
I_{BIT6}	Current sink if Bit6 = 1			6.4		
I_{BIT5}	Current sink if Bit5 = 1			3.2		
I_{BIT4}	Current sink if Bit4 = 1			1.6		
I_{BIT3}	Current sink if Bit3 = 1			0.8		
I_{BIT2}	Current sink if Bit2 = 1			0.4		
I_{BIT1}	Current sink if Bit1 = 1			0.2		
I_{BIT0}	Current sink if Bit0 = 1			0.1		
I_{MATCH}	Matching Accuracy	CURR1, CURR2, CURR3 and CURR4	-10		+10	%
I_{OUT}	Absolute Accuracy		-15		+15	%
V_{CUR1-4}	Voltage Compliance		0		V_{CP}-0.2	V

Figure 24. Internal processing of current sources



8.2.1 Unused Current Sources

Unused current sources can be left open. There are no external connections or components necessary if they are not used.

8.2.2 Current Source Registers .

Table 11. Current Control Register

0x01 Current Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	curr4_mode	0	R/W	**00: Current Source CURR4 is in off mode** 01: Current Source CURR4 is in on mode 10: Current source CURR4 is in PWM control mode 11: Current source CURR4 is in LED pattern generation mode
5:4	curr3_mode	0	R/W	**00: Current Source CURR3 is in off mode** 01: Current Source CURR3 is in on mode 10: Current source CURR3 is in PWM control mode 11: Current source CURR3 is in LED pattern generation mode
3:2	curr2_mode	0	R/W	**00: Current Source CURR2 is in off mode** 01: Current Source CURR2 is in on mode 10: Current source CURR2 is in PWM control mode 11: Current source CURR2 is in LED pattern generation mode
1:0	curr1_mode	3	R/W	00: Current Source CURR1 is in off mode 01: Current Source CURR1 is in on mode 10: Current source CURR1 is in PWM control mode **11: Current source CURR1 is in LED pattern generation mode**

Table 12. Current Source Register LED1

0x02 Current Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr1_current	0x40	R/W	**0000 0000: 0mA current output from source CURR1** 0000 0001: 0.1mA current output from source CURR1 0000 0010: 0.2mA current output from source CURR1 0000 0011: 0.3mA current output from source CURR1 ... 1111 1111: 25.5mA current output from source CURR1

Table 13. Current Control Register LED2

0x03 Current Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr2_current	0	R/W	**0000 0000: 0mA current output from source CURR2** 0000 0001: 0.1mA current output from source CURR2 0000 0010: 0.2mA current output from source CURR2 0000 0011: 0.3mA current output from source CURR2 ... 1111 1111: 25.5mA current output from source CURR2

Table 14. Current Control Register CURR3

0x04 Current Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr3_current	0	R/W	**0000 0000: 0mA current output from source CURR3** 0000 0001: 0.1mA current output from source CURR3 0000 0010: 0.2mA current output from source CURR3 0000 0011: 0.3mA current output from source CURR3 ... 1111 1111: 25.5mA current output from source CURR3

Table 15. Current Control Register CURR4

0x05 Current Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr4_current	0	R/W	**0000 0000: 0mA current output from source CURR4** 0000 0001: 0.1mA current output from source CURR4 0000 0010: 0.2mA current output from source CURR4 0000 0011: 0.3mA current output from source CURR4 ... 1111 1111: 25.5mA current output from source CURR4

Table 16. CURRx Low Voltage Status Register

0x2b Current Source Low Voltage Status Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	curr4_low_v	0	R	This is a read only register and returns 0 if the voltage on current source CURR4 is ok. If the voltage drops below 200mV across the current source the bit is set to 1. **0: CURR4 voltage is OK** 1: CURR4 voltage is too low
2	curr3_low_v	0	R	This is a read only register and returns 0 if the voltage on current source CURR3 is ok. If the voltage drops below 200mV across the current source the bit is set to 1. **0: CURR3 voltage is OK** 1: CURR3 voltage is too low
1	curr2_low_v	0	R	This is a read only register and returns 0 if the voltage on current source CURR2 is ok. If the voltage drops below 200mV across the current source the bit is set to 1. **0: CURR2 voltage is OK** 1: CURR2 voltage is too low
0	curr1_low_v	0	R	This is a read only register and returns 0 if the voltage on current source CURR1 is ok. If the voltage drops below 200mV across the current source the bit is set to 1. **0: CURR1 voltage is OK** 1: CURR1 voltage is too low

8.3 Power - On Reset

The AS3668 provides an power - on reset feature that is controlled by two different sources:

- VBAT supply voltage
- Serial interface state (SCL only)

If the internal VBAT supply voltage reset is forced, when the supply voltage VBAT of AS3668 drops below a predefined voltage, the device enters shutdown mode. This predefined voltage is 2V (typ.) and is defined as VPOR_VBAT. Besides this hard wired voltage level where an internal reset is forced to shut down the device, AS3668 supports an additional VBAT monitoring feature. This means that the designer can select according to its application requirements a reset level which is appropriate for mobile Li-Ion battery powered applications. The use case for this second VBAT monitoring is to make sure that if a mobile device switches off suddenly, at a dedicated voltage, to make sure that also AS3668 enters power down mode. Otherwise unwanted LED effects could occur even if the digital system is not running any more. AS3668 allows the designer now to set the VBAT monitoring level to the same voltage level the whole system is powering down. There's no need any more for the CPU to reset or power down AS3668 in a low battery case any more. The device can handle this use case automatically.

In addition to the VBAT voltage monitoring the device supports also a shut down function forced by the serial interface. If the voltage on the serial interface pin SCL is below 1V (typ.) and GPIO/AUDIO_IN pin is low, the device forces a reset. To prevent the system against wrong resets caused by electromagnetically influences there is also a debounce timer integrated with a typical debounce time of 100ms. This debounce time is used for VBAT monitoring as well. If the serial interface monitoring is not supposed to be used in an application it is also possible to disable the feature using the corresponding register bit.

Figure 25. Reset Circuit Block Diagram

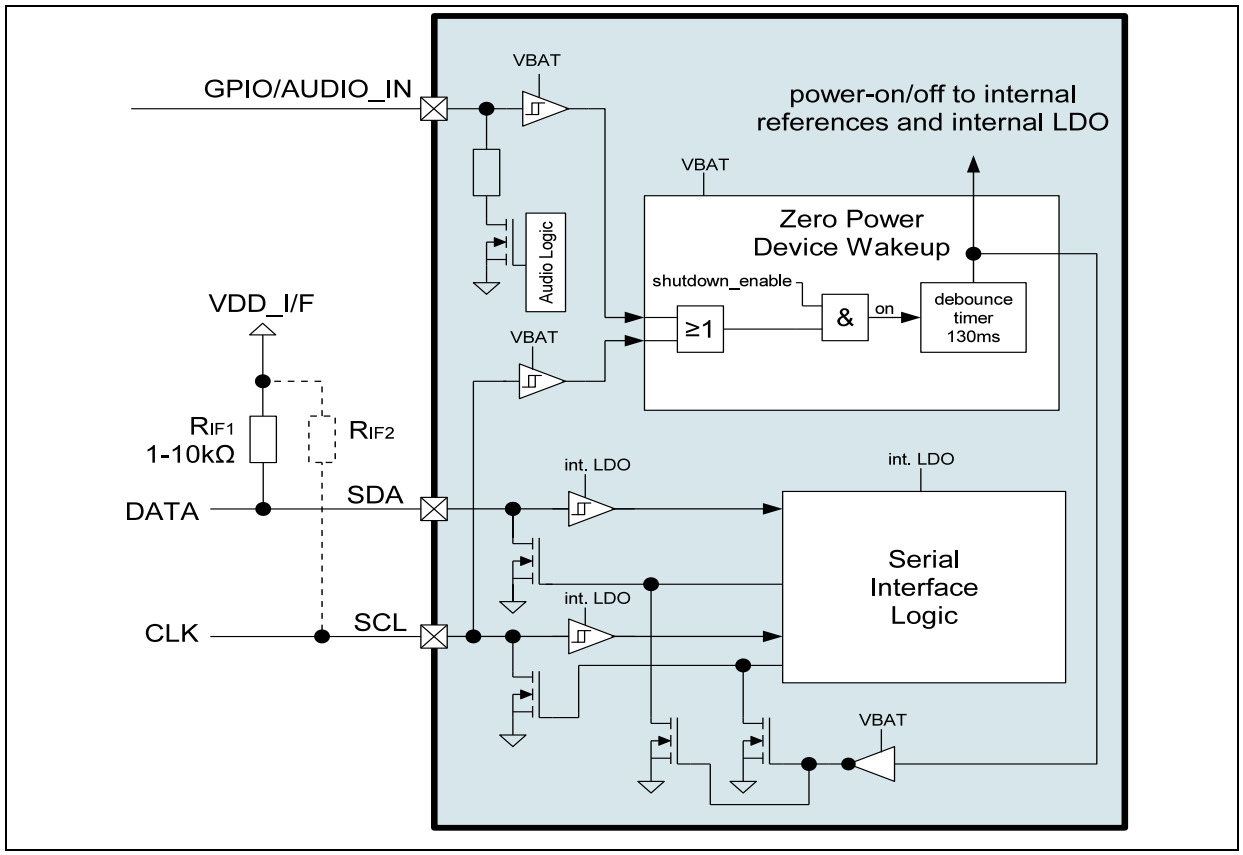


Table 17. Power On Reset Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VPOR_VBAT	Overall Power-On Reset	Monitor voltage on VBAT; power-on reset for all internal functions.		2.0		V
VMON_VBAT	Register defined stand by mode voltage	depending on register setting the voltage can be configured	3.0V		3.3V	
VPOR_PERI	Reset Level for pins SCL	Monitor voltage on pin SCL		1.0		V
tPOR_DEB	Reset debounce time for pins SCL		110	130	150	ms
tstart	Interface Startup Time			3		ms

8.4 VBAT Monitor

The *VBAT* monitor is a supervisory circuit. The monitor is per default disabled when the AS3668 is powered up. The function can be used in order to send the device automatically into standby mode if the supply voltage of AS3668 drops below the defined values in register vmon_vbat. All together the user can select between three different voltage thresholds for this function with 3.375V, 3.3V and 3.0V. If the function is disabled the device switches of if the battery voltage drops below 2.0V. The monitor function has also a debouncer with 100ms implemented in order to filter the 217Hz GSM noise pulses from the battery supply voltage. Without the debouncer the chip would be susceptible to this noise and maybe enter into standby mode due to a misinterpretation of the supply voltage.

Figure 26. VBAT Monitor Block Diagram

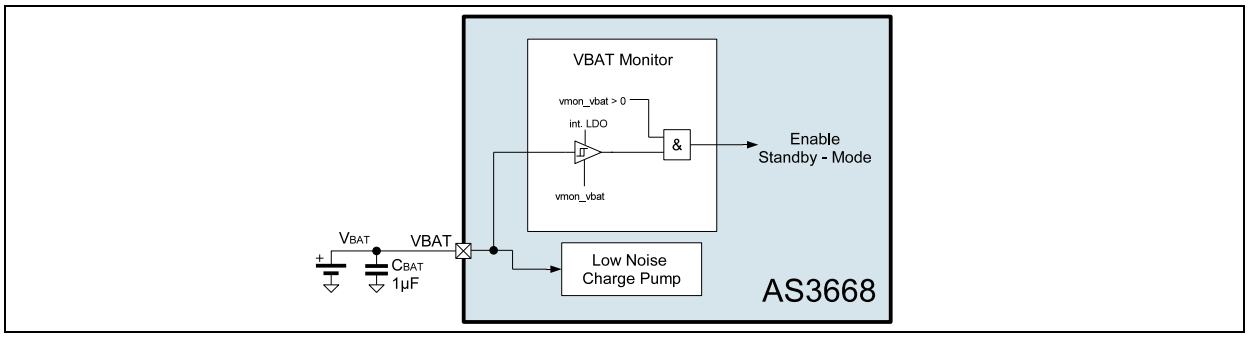


Table 18. VBAT Monitor Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VMON_VBAT	Register defined stand by mode voltage	depending on register setting the voltage can be configured	3.0V		3.3V	

8.4.1 VBAT Monitor Registers .

Table 19. Overtemperature Control / VBAT Monitor Register

0x29 Overtemperature Control / VBAT Monitor Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:5	vmon_vbat	0	R/W	**0: Device enters shutdown mode if VBAT voltage drops below ~2.0V** 1: Device enters standby mode if VBAT voltage drops below 3.0V 2: Device enters standby mode if VBAT voltage drops below 3.15V 3:Device enters standby mode if VBAT voltage drops below 3.3V
4	shutdown_enable	1	R/W	This bit allows the user to disable the I2C shutdown feature. If the bit is set to '0' both I2C signal lines can be low without shutting down AS3668. 0: disables the automatic shutdown of AS3668 **1: enables the automatic shutdown of AS3668**
2	rst_ov_temp	0	W	This register is a self clearing register. Write a '1' to this register to clear ov_temp.
1	ov_temp	0	R	This is a read only register and provides feedback about the junction temperature of the chip. The bit is usually set if the junction temperature reaches about 140°C. **0: Junction temperature OK** 1: Junction Overtemperature
0	ov_temp_on	1	R/W	This bit allows the user the enable/disable the junction temperature monitoring for AS3668. 0: Temperature supervision OFF **1: Temperature supervision ON**

8.5 Temperature Supervision

An integrated temperature sensor provides over-temperature protection for the AS3668. This sensor generates a flag if the device temperature reaches the over temperature threshold of 140°. The threshold has a hysteresis to prevent oscillation effects.

If the device temperature exceeds the T140 threshold all current sources and the charge pump get disabled and the ov_temp flag is set. After decreasing the temperature by THYST operation is resumed. Although the device resumes ordinary operation after a overtemperature event, the register ov_temp keeps set to 1. Even a read operation from the register doesn't reset the register. Therefore it's necessary to use the register rst_ov_temp to reset the overtemperature register ov_temp.

The ov_temp flag can only be reset by first writing a 1 to the register bit rst_ov_temp. If bit ov_temp_on = 1 activates temperature supervision Table 20. It is recommend to leave this bit set (default state).

Table 20. Overtemperature Detection

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{140}	ov_temp Rising Threshold			140		°C
T_{HYST}	ov_temp Hysteresis			5		°C

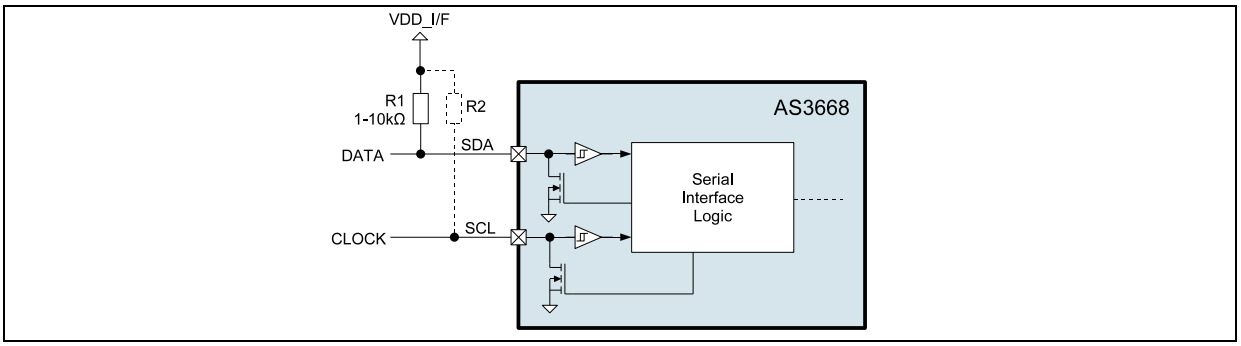
Table 21. Overtemperature Control / V_{BAT} Monitor Register

0x29 Overtemerature Control / V_{BAT} Monitor Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	rst_ov_temp	0	W	Write a 1 to this register to reset ov_temp
1	ov_temp	0	R	**0: Junction temperature is ok and below T_{140}** 1: Junction temperature is too high and above T_{140}
0	ov_temp_on	1	R/W	0: Disables the overtemperature supervision (not recommended) **1: Enabled the overtemperature supervision**

8.6 I²C Serial Interface Bus

The AS3668 supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. The AS3668 operates as a slave on the I²C bus. Due to the reason that the device is also power up/down with the I²C interface there is a debouncer (130ms) on the signal lines integrated to avoid a system shut down while having I²C traffic on the bus.

Figure 27. Serial Interface Block Diagram



The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The clock line SCL is never held low by AS3668 because clock stretching of the bus is not supported.

Figure 28. AS3668 Interface Initialization

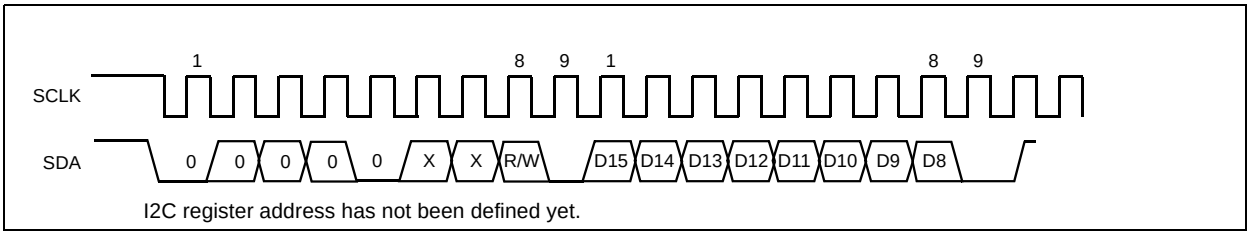
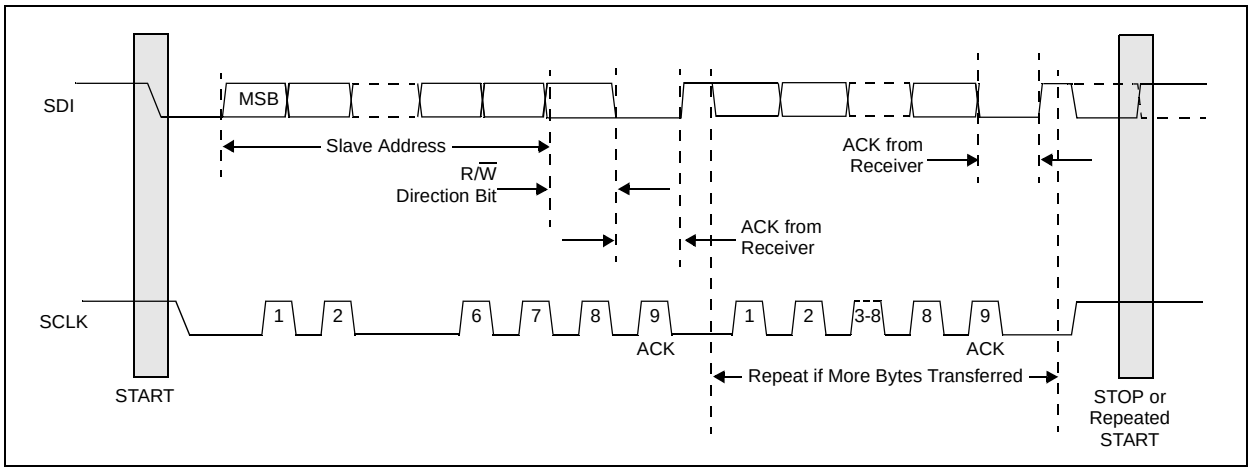


Figure 29. Bus Protocol



The bus protocol (as shown in Figure 29) is defined as:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The bus conditions are defined as:

- **Bus Not Busy**. Data and clock lines remain HIGH.
- **Start Data Transfer**. A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
- **Stop Data Transfe**r. A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.
- **Data Valid**. The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.
  Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.
  Within the I²C bus specifications a high-speed mode (3.4MHz clock rate) is defined.
- **Acknowledge**: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.
- Figure 29 on page 23 details how data transfer is accomplished on the I²C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:
- **Master Transmitter to Slave Receiver**. The first byte transmitted by the master is the slave address, followed by a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- **Slave Transmitter to Master Receiver**. The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

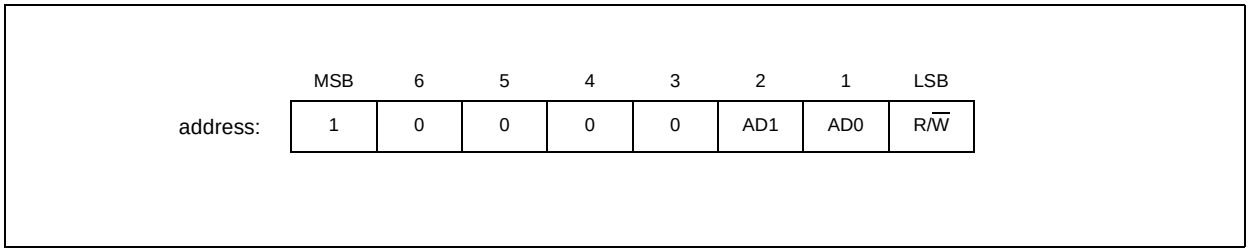
The AS3668 can operate in the following slave modes:

- **Slave Receiver Mode**. Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode**. The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the AS3668 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

8.6.1 I²C Device Address Byte

The address byte (see Figure 30) is the first byte received following the START condition from the master device. The 7 bit device address is 0x42.

Figure 30. I²C Device Address Byte



- Bit 1 and bit 2 of the address byte are defined by the external bus connection of the slave to the master shown in chapter 8.6.3. A maximum of two devices can be connected in parallel on the same bus at one time.
- The last bit of the address byte (R/$\overline{W}$) define the operation to be performed. When set to a 1 a read operation is selected; when set to a 0 a write operation is selected.

Following the START condition, the AS3668 monitors the I²C bus, checking the device type identifier being transmitted. Upon receiving the address code, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

8.6.2 Command Byte

The AS3668 operation, (see Table 29 on page 23) is determined by a command byte (see Table 31).

Figure 31. Command Byte

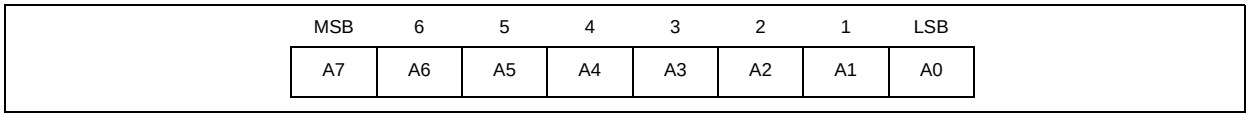


Figure 32. Command and Single Data Byte received by AS3668

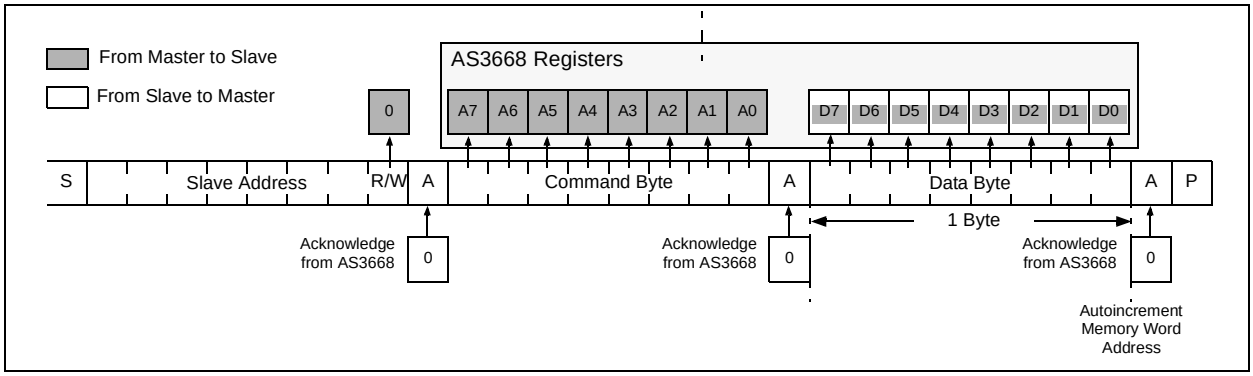


Figure 33. Setting the Pointer to a Address Register to select a Data Register for a Read Operation

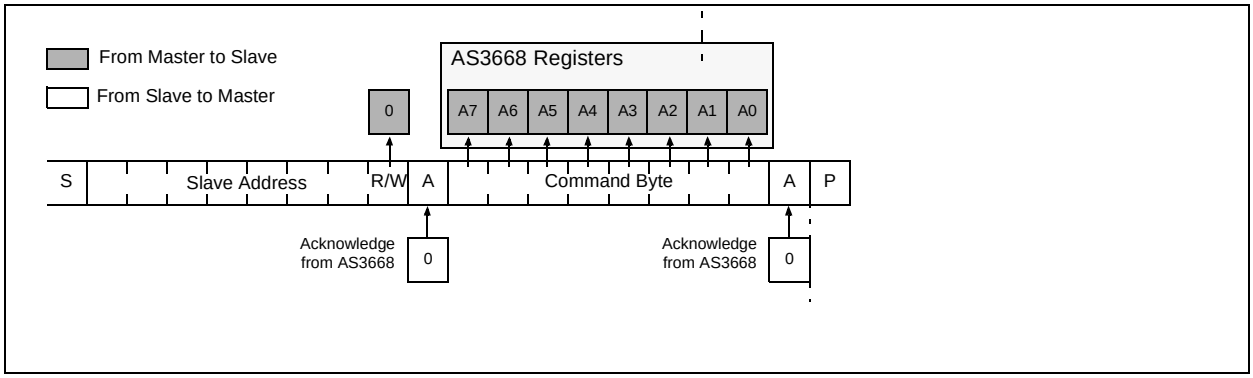
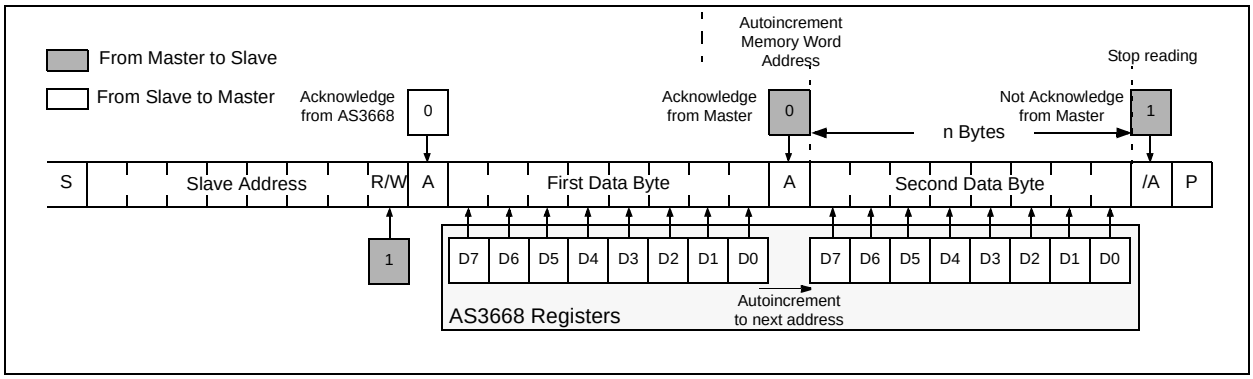


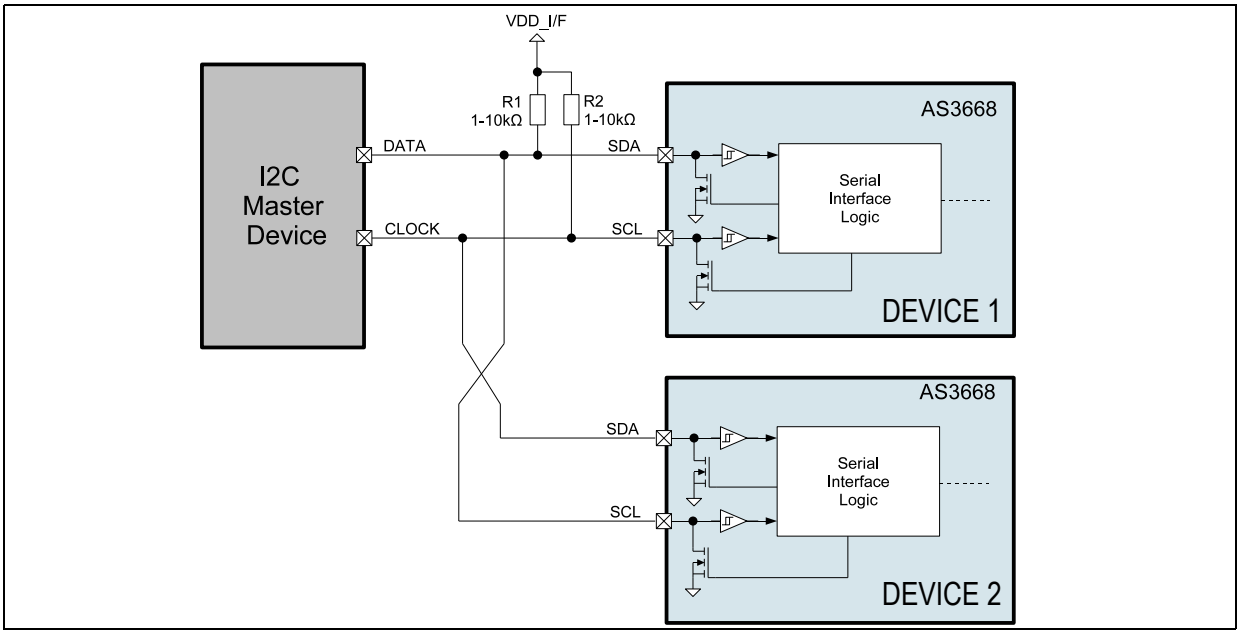
Figure 34. Reading n Bytes from AS3668



8.6.3 I²C Device Address Selection

The AS3668 features two I²C slave addresses without having a dedicated address selection pin. The selection of the I²C address is done with the interconnection of AS3668 to the bus lines shown in Figure 35 below. The serial interface logic inside AS3668 is able to distinguish between a direct I2C connection to the master or a second option where data and clock line are crossed. Therefore it is only possible to address a maximum of two AS3668 slaves on one I²C bus.

Figure 35. I²C Address Selection Application Diagram



The I²C addresses for the devices in the different connection modes can be found in Table 22.

Table 22. I²C Addresses for AS3668

DEVICE Number	7 bit I²C address	8 Bit read address	8 Bit write address
1(default)	0x42	0x85	0x84
2	0x43	0x87	0x86

8.7 Operating Modes

Due to the reason that AS3668 has no dedicated enable or power - on pin the device is basically controlled with the I²C signal lines SDA and SCL. If the voltages on these pins are less than V_{POR_PERI} for > t_{POR_DEB} and GPIO/AUDIO_IN input is low, the AS3668 is in shut down mode with a minimized current consumption of I_{VBAT} = 1µA (typ.). All blocks inside AS3668 are basically switched off except the power up reset circuit is always active.

If the voltage on the I²C signal lines is bigger than V_{POR_PERI} for a time frame longer than t_{POR_DEB}, the device changes it's operation mode from power off to standby mode. In this use state only the power on reset and the I²C block of the device is active with an average current consumption of 10µA(typ.). The device changes its operating mode from standby to active mode automatically if one of the following blocks inside AS3668 are activated:

- Charge Pump
- Current Source
- Pattern Mode activated
- External PWM mode via GPIO/AUDIO_IN

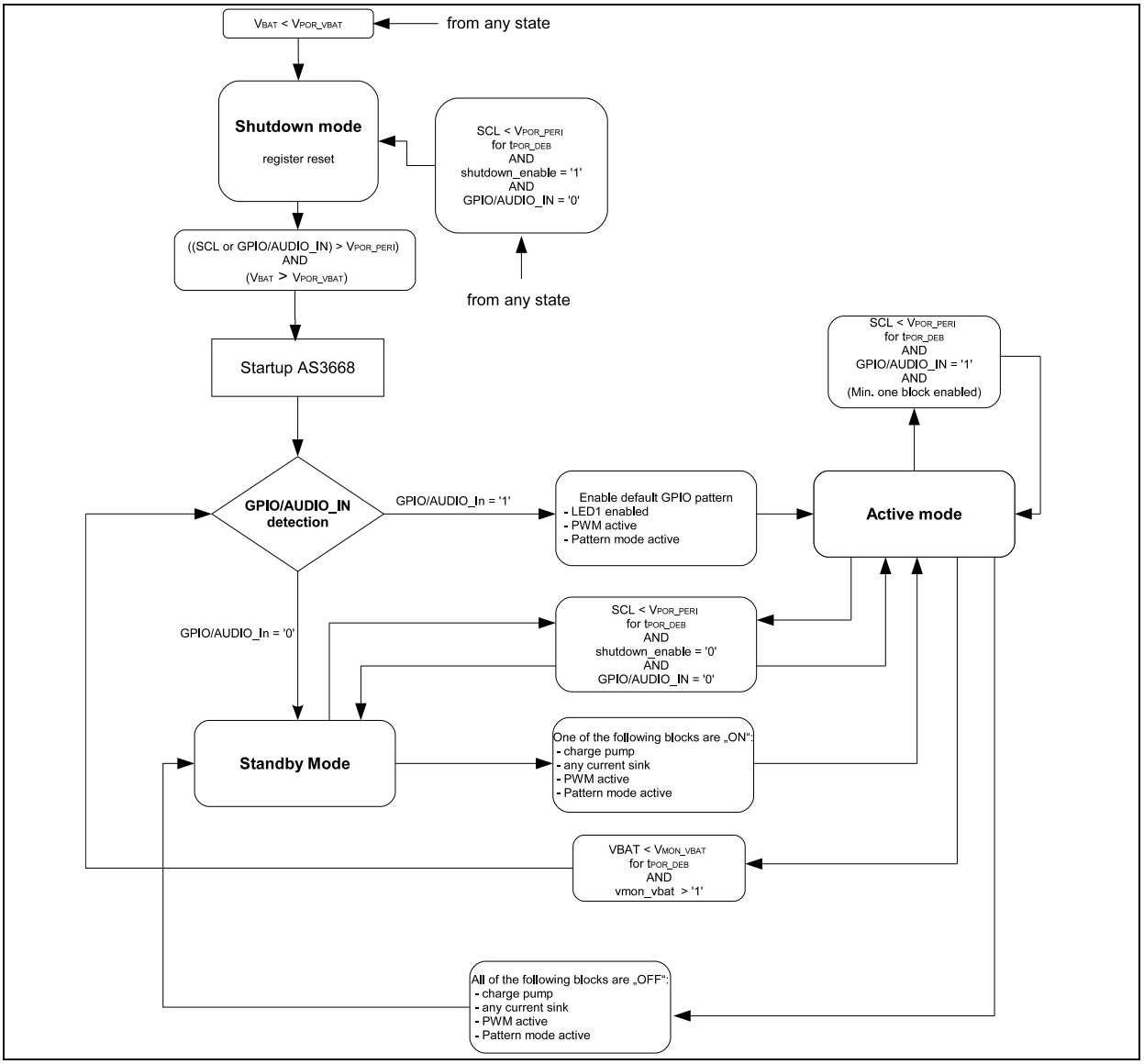
In addition to the I²C monitoring for startup of the device it is possible to power up AS3668 with GPIO/AUDIO_IN pin while the I²C signal lines are low. this is a special use case which starts a predefined pattern on current source CURR1. For a detailed description please refer to chapter 8.7.1.

Besides the monitoring of the I²C signal lines there is also an additional feature which monitors the battery supply voltage V_{BAT}. Basically there are two voltage levels where this voltage monitoring becomes active. The first voltage V_{POR_VBAT} can be seen as a shut down and minimum supply voltage of the device voltage which is fixed at 2V (typ.). The same voltage level is used for the power on reset circuit. If the battery voltage drops below V_{POR_VBAT} the device automatically changes from active mode or standby mode to off mode. Besides the V_{POR_VBAT} level there is a second V_{BAT} monitoring voltage which can be activated in a register. This voltage V_{MON_VBAT} is typically set to 3.4V (default register setting) but can be reconfigured using the I²C interface down to 2.4V according to the requirements of an application. It is also possible to disable the V_{BAT} monitoring. The V_{POR_VBAT} monitoring can not be disabled.

Table 23. Truth Table for AS3668 operating modes

AS3668 Blocks	Off Mode	Standby Mode	Active Mode
Power On/Off Reset	enabled	enabled	enabled
I²C	disabled	enabled	enabled
Charge Pump	disabled	disabled	enabled/disabled depending on register setting
Current Sources	disabled	disabled	enabled/disabled depending on register setting
Pattern Mode	disabled	disabled	enabled/disabled depending on register setting
External PWM	disabled	disabled	enabled/disabled depending on register setting

Figure 36. Startup and operating mode selection



8.7.1 GPIO/AUDIO_IN Automatic Pattern Start-up Mode

As described in the previous chapter it is basically possible to start up the device using the I²C clock line. In some cases it is not possible to configure AS3668 in an application because the application processor is not running that time. Therefore AS3668 supports a special startup mode shown in Figure 36 and Figure 37 to start up the device without pulling the I²C clock line high. If an external device is connected to the GPIO/AUDIO_IN pin of AS3668 and the pin is pulled high the device starts up with an default pattern running on CURR1 although the I²C clock line is low shown in Figure 37. If for example AS3668 starts up with I²C and the GPIO/AUDIO_IN pin is low that time the device starts up in standby mode and can be configured using the two wire interface. If the I2C signal lines become low whereas the GPIO/AUDIO_IN pin is high at the same time the chip keeps activated and running as long as GPIO/AUDIO_IN pin is high. Once the GPIO/AUDIO_IN pin goes low the device enters shut down mode. This use case enables the user to keep on charging the battery for example and indicate this with a special PWM pattern while the CPU is powered down for example. A typical application is shown in Figure 38.

Figure 37. Timing Diagram Startup Modes

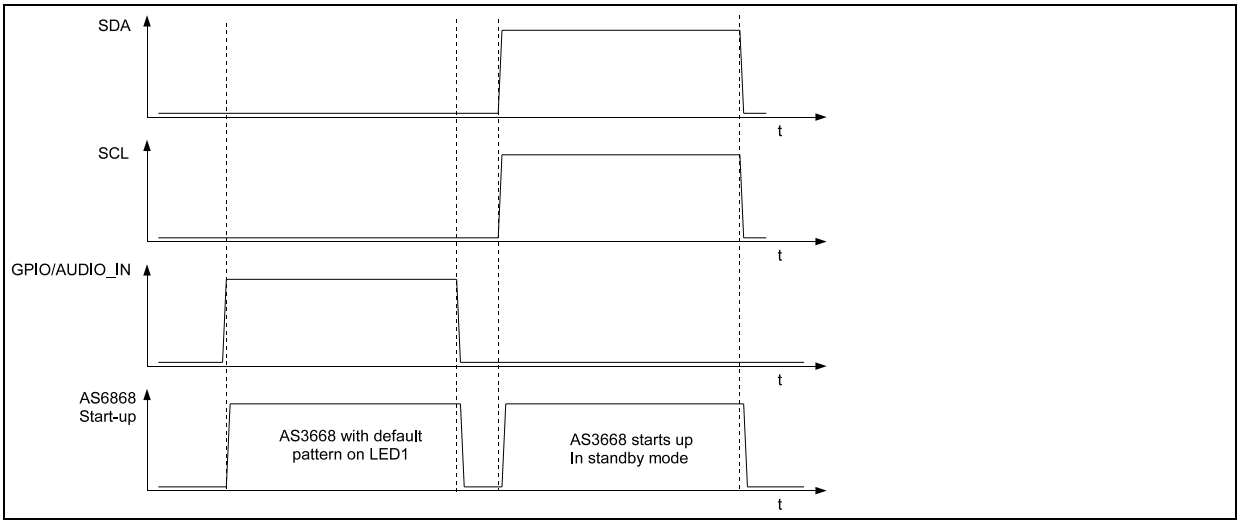
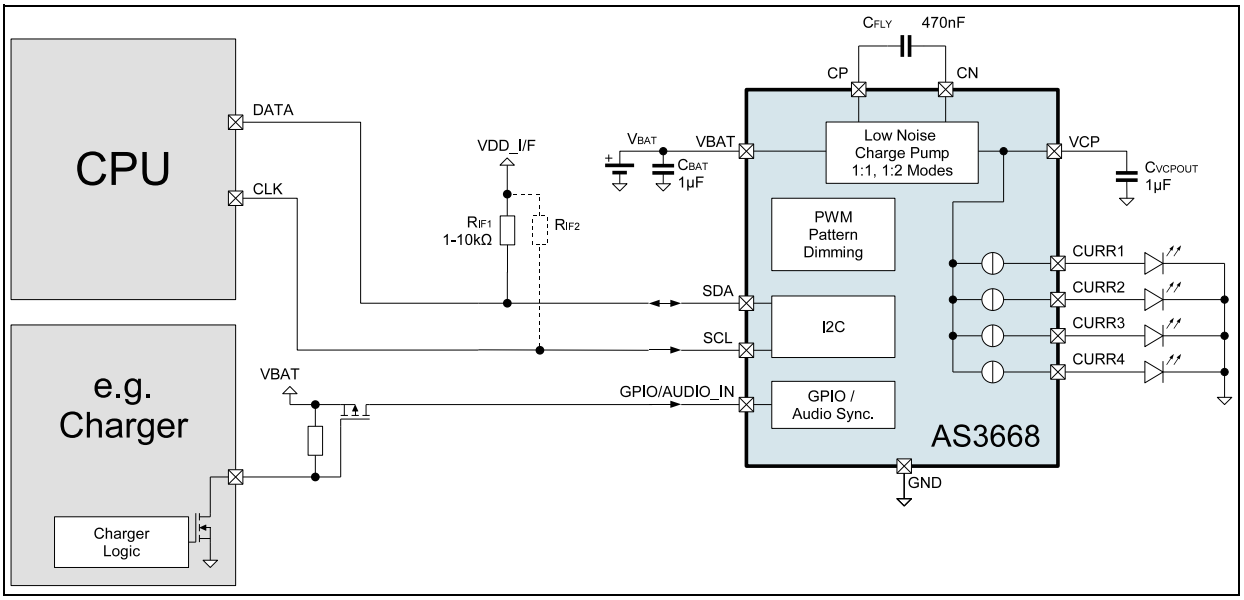


Figure 38. Typical Application Automatic Pattern Startup



The application in Figure 38 shows the AS3668 connected to a CPU and a typical charger. Most of the stand alone chargers do have a open drain output for charger indication with a LED. This output pin can be used to control AS3668. If the charger is active the GPIO/AUDIO_IN input pin of AS3668 is pulled high. The chip starts up with a default pattern on CURR1output. With this special mode it is possible to indicate charging using for example the RGB LED connected to AS3668 although the CPU is not running. This use case can happen if the battery of a device is almost fully discharged and the CPU can not start up because the battery voltage is too low in trickle charge mode. The automatic pattern start-up mode allows the operate the LED on AS3668 without I²C interaction with the CPU. AS3668 starts up in automatic pattern start-up mode with the default pattern shown in Figure 39. Please mind that the pattern is only active for current source CURR1.

Figure 39. Timing for Automatic Pattern Startup

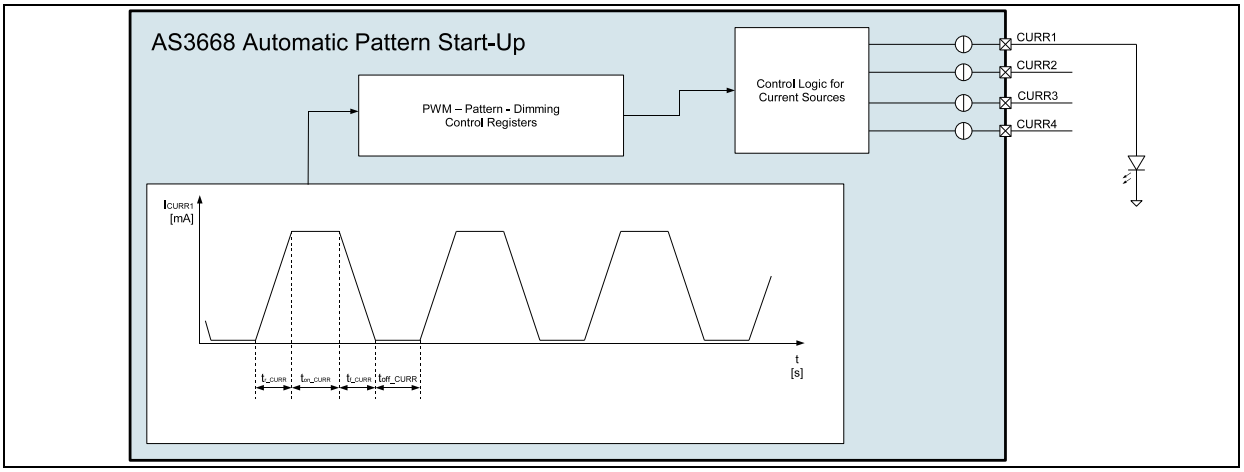


Table 24. Automatic Pattern Start-Up Parameters

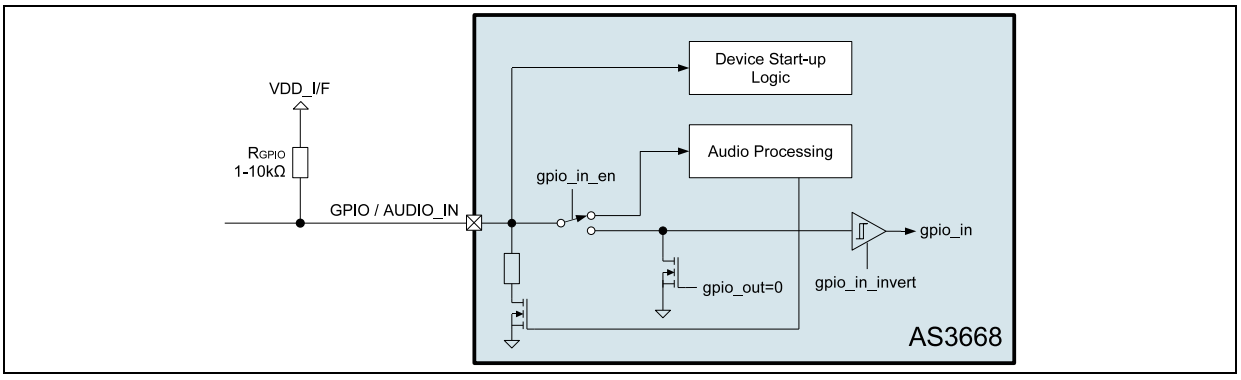
Symbol	Parameter	Condition	Min	Typ	Max	Unit
tr_CURR	Rise time for dimming up CURR1			2.62		s
tf_CURR	Fall time for dimming down CURR1			2.62		s
ton_CURR	On time for CURR1			49		ms
toff_CURR	Off time for CURR1			0.54		s
ICURR1	Output Current for CURR1			6.4		mA

8.8 General Purpose Input / Output

The pin GPIO/AUDIO_IN is a general purpose input / output which is shared as a audio input for music synchronization. The pin can support the following features:

- Digital Schmitt Trigger Input
- Digital output with open drain functionality
- Analogue Audio input for audio controlled LEDs
- PWM input for CURR1, CURR2, CURR3 and CURR4 (max. 1MHz)
- Device Start-up in Automatic Pattern Generation mode

Figure 40. General Purpose Input / Output Block diagram



Although the GPIO/AUDIO_IN pin supports digital output as well for simple control exercises an external pull up resistor is mandatory. The pin is not able to actively drive the signal line because there is no push/pull stage integrated. The internal pull down resistor is disabled in audio synchronization mode.

For a detailed description of music playback synchronization please refer to chapter 8.9.

8.8.1 Unused General Purpose Input / Output

If the pin is not used it is recommended to connect it to ground.

8.8.2 GPIO Control Register . .

Table 25. GPIO Control Register

0x06 GPIO Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	gpio_in_invert	0	R/W	This bit allows the user to invert input signal of GPIO/AUDIO_IN if the pin is configured as digital input. **0: Non-inverted digital input GPIO/AUDIO_IN** 1: Inverted digital input GPIO/AUDIO_IN
1	gpio_in_en	1	R/W	0: GPIO/AUDIO_IN pin is configured as analog input (audio mode) **1: GPIO/AUDIO_IN pin is configured as digital input (general purpose)**
0	gpio_mode	0	R/W	**0: GPIO/AUDIO_IN pin is configured as input** 1: GPIO/AUDIO_IN pin is configured as output in open drain configuration The pin requires an external pull up resistor

Table 26. GPIO Signal Register

0x08 GPIO Signal Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	gpio_in	0	R	The register is a read only register. The register is set to 1, if the pin GPIO/AUDIO_IN is externally pulled high. The register is set to 0, if the pin is connected to ground.

Table 27. GPIO Output Register

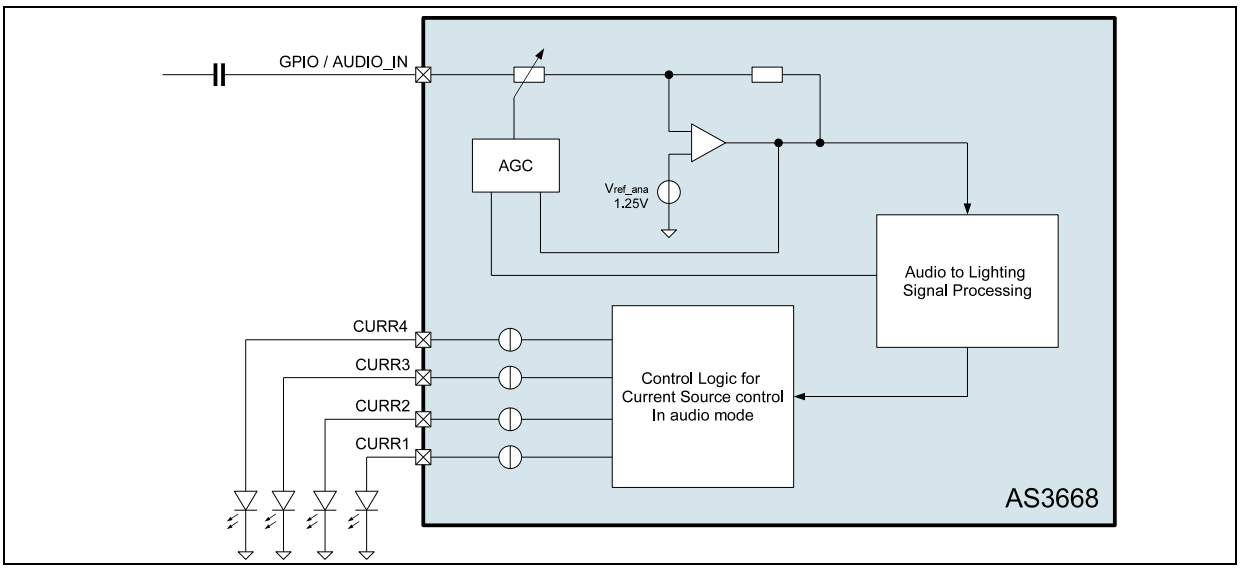
0x07 GPIO Output Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	gpio_out	0	R/W	This register is the output register if the pin GPIO/AUDIO_IN is configured as output. Writing to the register changes the output state of the pin. **0: GPIO/AUDIO_IN pin low** 1: GPIO/AUDIO_IN pin high (external pull-up resistor required)

8.9 Audio Input

The audio input pin GPIO/AUDIO_IN is shared with a general purpose input/output. It is possible to switch the operating mode of the pin from a GPIO to an analogue audio input. This multiplexed audio input pin allows the AS3668 to do lighting effects depending on the audio content connected to GPIO/AUDIO_IN.

The block diagram for the signal processing path is shown in Figure 41. The analogue audio signal is coupled into the pin GPIO/AUDIO_IN with an external DC blocking capacitor. The integrated audio pre-amplifier with automatic gain control attenuates or amplifies the input signal to avoid clipping inside the signal processing path and furthermore increase the dynamic range of the signal in case a very small signal is applied to AS3668. The AGC of the preamplifier uses the audio gain defined in register audio_gain as start value and changes the gain in a range of +/- 3dB. The pre-amplified audio signal is then feed into an special analogue signal processing unit to create special lighting effects. Various settings inside the signal processing unit allow the user to define different types fancy lighting effects. This processing unit it directly linked together with the control logic for the four current sources of the device. Thus, besides the ordinary lighting pattern control of the current sources with register settings, the outputs are directly controlled in audio mode from the audio signal processing unit.

Figure 41. Audio Input block diagram



8.9.1 Audio Control Register . .

Table 28. Audio AGC Register

0x40 Audio AGC Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6	agc_up_level	0	R/W	This bit allows the change of the AGC up switching threshold. **0: Default AGC up switching threshold** 1: Increased AGC up switching threshold
5	agc_down_level	0	R/W	This bit allows the change of the AGC down switching threshold. **0: Default AGC down switching threshold** 1: Increased AGC down switching threshold
4:3	decay_agc_down	0	R/W	Defines the decay time for the automatic gain control of the audio input amplifier for decreasing the gain. **00: 0.131s** 01: 0.262s 10: 0.393s 11: 0.524s
2:1	decay_agc_up	0	R/W	Defines the decay time for the automatic gain control of the audio input amplifier for increasing the gain. **00: 0.262s** 01: 0.524s 10: 0.786s 11: 1.049s
0	agc_on	0	R/W	This bit allows the user the enable / disable the automatic gain control of the audio input amplifier. **0: Automatic Gain Control off** 1: Automatic Gain Control on

Table 29. Audio Input Buffer Register

0x41 Audio Input Buffer Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	audio_dis_start	0	R/W	Enables the audio input capacitor precharging. This function is only active if register audio_man_start is set to manual precharging. After precharging register audio_dis_start must be cleared again. **0: Input capacitor precharging enabled** 1: Input capacitor precharging disabled
6	audio_man_start	0	R/W	Configures the input capacitor precharging mechanism for auto precharging or manual precharging. **0: Automatic Precharging** 1: Manual Precharging
5:1	audio_gain	0	R/W	Configures the gain of the audio preamplifier. The gain can be configured in the range of -6dB up to +25dB according to the register setting in 1dB steps. **0 0000: -6dB** 0 0001: -5dB 0 0010: -4dB 0 0011: -3dB ... 1 1111: 25dB
0	aud_buf_on	0	R/W	This bit switches the internal audio buffer amplifier on and off according to the register setting **0: Audio Buffer off** 1: Audio Buffer on

Table 30. Audio Control Register

0x42 Audio Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	audio_input_pin	0	R/W	This bit enables pin GPIO/AUDIO_IN or CURR4 pin to be configured as audio input pin for audio playback synchronization of the current sources. **0: GPIO/AUDIO_IN selected for audio synchronization** 1: CURR4 pin selected for audio synchronization
6	pld_off	0	R/W	This bit defines if the internal pull down resistor of GPIO/AUDIO_IN pin is enabled or disabled. If the audio mode is enabled the internal pull down is automatically disabled **0: Pull down resistor enabled if register aud_buf_on is set to '0'** 1: Pull down resistor disabled
5	adc_characteristic	0	R/W	Defines the ADC characteristic of the ADC for general purpose ADC measurements depending on the selected ADC characteristics in register adc_mode. **00: x*250mV (adc_mode = 0)** 01: x*50mV (adc_mode = 0) 00: 75mV*2^x(adc_mode = 0 or adc_mode = 1)
4:3	audio_decay	0	R/W	Defines the audio decay time. **00: 10ms** 01: 20ms 10: 40ms 11: 80ms
2:0	audiosync_mode	0	R/W	In this register it is possible to select between different audio synchronization modes of the current sources in order to create different lighting effects. **000: 4 LED bar code** 001: 4 LED bar code with dimming 010: Running LED bar code 011: Running LED bar code with dimming 100: RGB 101: RGB with dimming 110: 4 LED parallel with dimming 111: Do not use

Table 31. Audio Output Register

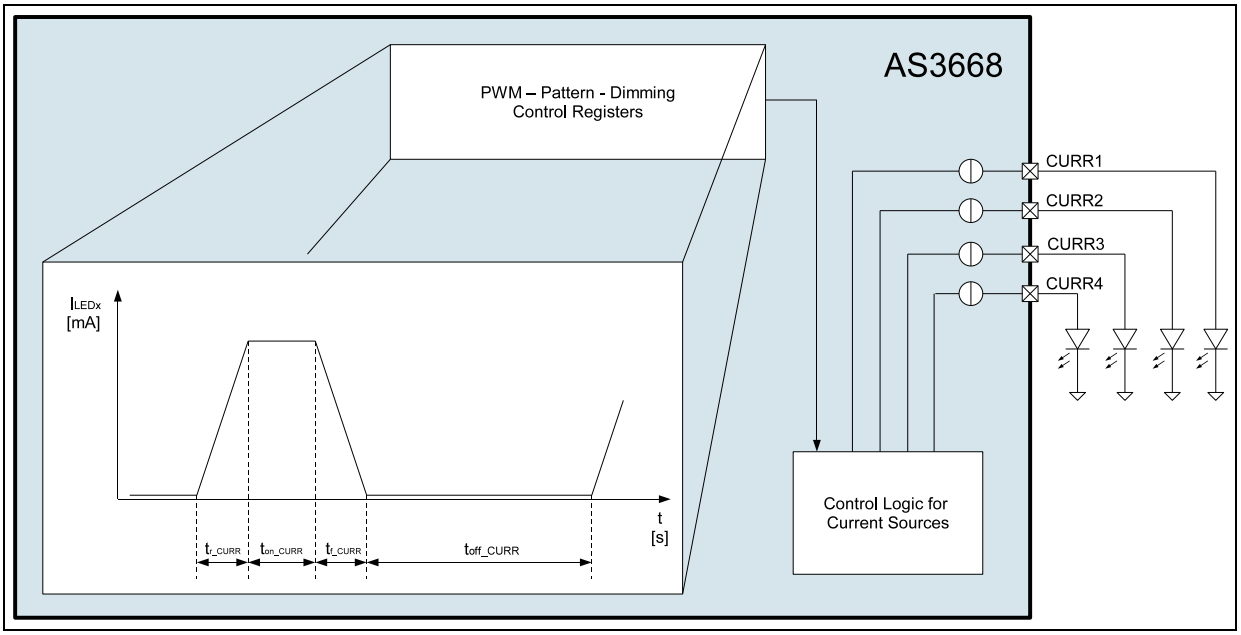
0x43 Audio Output Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	curr4_aud_en	0	R/W	This register allows the user to select between normal control (e.g. PWM pattern control) and audio synchronization mode of current source CURR4 . **0: CURR4 normal function** 1: CURR4 audio synchronization mode
2	curr3_aud_en	0	R/W	This register allows the user to select between normal control (e.g. PWM pattern control) and audio synchronization mode of current source CURR3 . **0: CURR3 normal function** 1: CURR3 audio synchronization mode
1	curr2_aud_en	0	R/W	This register allows the user to select between normal control (e.g. PWM pattern control) and audio synchronization mode of current source CURR2 . **0: CURR2 normal function** 1: CURR2 audio synchronization mode
0	curr1_aud_en	0	R/W	This register allows the user to select between normal control (e.g. PWM pattern control) and audio synchronization mode of current source CURR1 . **0: CURR1 normal function** 1: CURR1 audio synchronization mode

8.10 LED Pattern Configuration

8.10.1 Single Pulse Mode

The AS3668 supports basically three basic LED pattern modes to create fancy lighting effect for the LEDs which can be connected to the current sources CURR1, CURR2, CURR3 and CURR4. The first and basic mode is the “Single Pulse Mode”. This mode is basically defined out of five parameters shown in Figure 42 below.

Figure 42. LED Pattern - Single Pulse Mode



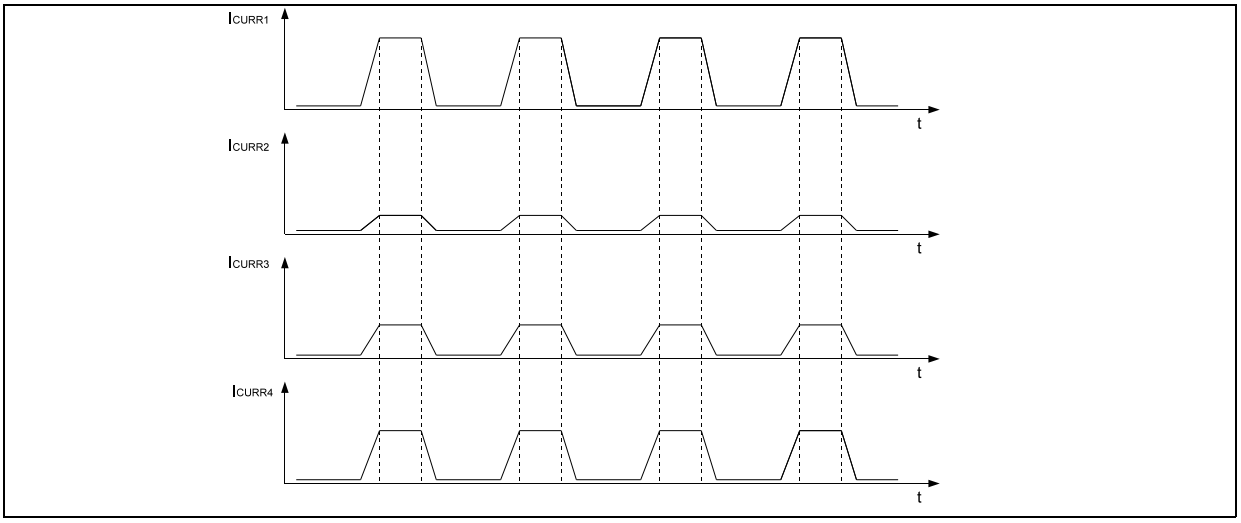
The first parameter which can be configured in register pwm_dim_speed_up is t_{r_CURR}. This time defines how long it takes to ramp up the current to the defined value in registers curr1_current, curr2_current, curr3_current and curr4_current for each current source. The dimming of the current source is of course logarithmic for a better visual effect but can be reconfigured to linear mode in register pwm_dim_shape. The second parameter t_{f_CURR}, which can be controlled in register pwm_dim_speed_down, defines the fall time for dimming down the LEDs. The third parameter is t_{on_CURR} and can be configured in register pattern_ton. It defines how long a current source keeps switched on with the current configured in register curr1_current, curr2_current, curr3_current and curr4_current for each current source. Also this down dimming is done with a logarithmic scale for a better visual effect. The last parameter t_{off_CURR} defines how long the current sources or LEDs are switched off until the whole pattern cycle starts from the beginning and can be configured in register pattern_toff.

Table 32. Singe Pulse Mode Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{r_CURR}	Rise time for dimming up CURRx		0		8.39	s
t_{f_CURR}	Fall time for dimming down CURRx		0		8.39	s
t_{on_CURR}	On time for CURRx		0.05		4.2	s
t_{off_CURR}	Off time for CURRx		0.08		8.4	s

Please mind that the settings for t_{f_CURR}, t_{r_CURR}, t_{on_CURR} and t_{off_CURR} are valid for all four current sinks at the same time. It is not possible to define individual time values for each current source differently to each other. The only parameter which can differ from on current source to another is the current which can be configured in registers curr1_current, curr2_current, curr3_current and curr4_current for each current source individually. An example how the mode looks like for all four current sources in parallel can be seen in Figure 43. All current sources work synchronously to each other with a fixed and parallel start point.

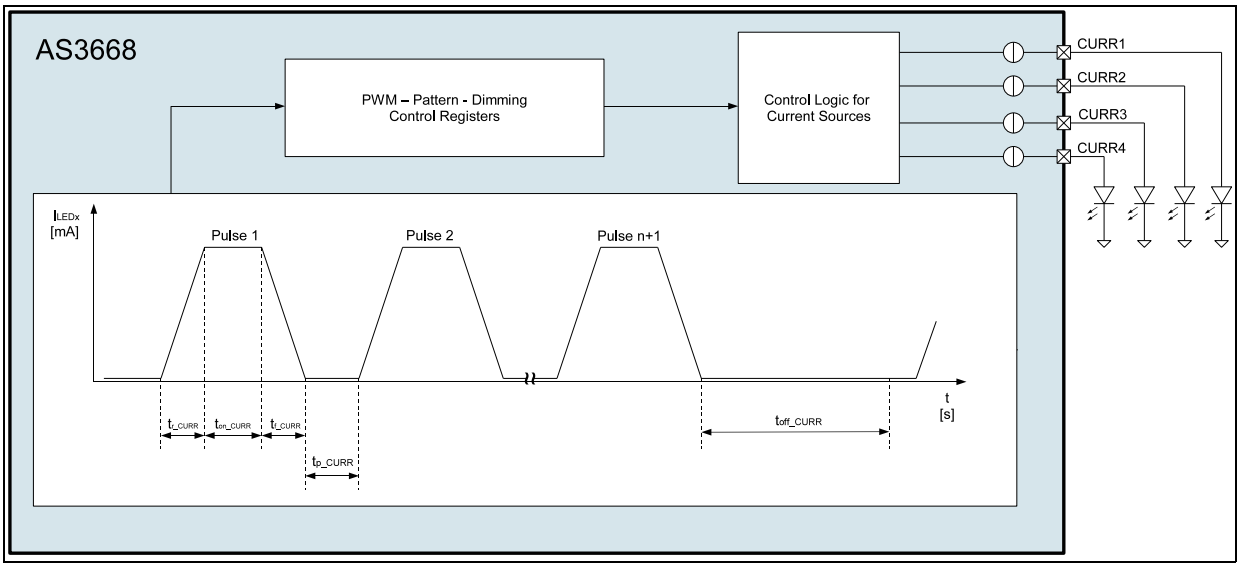
Figure 43. Single Pulse Mode - Example



8.10.2 Multiple Pulse Mode

In addition to the Single Pulse Pattern Mode described in Section 8.10.1 there is a second mode which is basically based on the Single Pulse Mode. The Multiple Pulse Mode still uses the parameters t_{r_CURR}, t_{f_CURR}, t_{on_CURR} and t_{off_CURR} of the Single Pulse Mode but has two more parameters. The first parameter is t_{p_CURR} and can be configured in register tp_led. This register defines the pause time between two pulses. The second new parameter is a parameter that defines the number of multiple pulses. This can be configured in register multiple_pulse

Table 33. Timing Multiple Pulse Mode



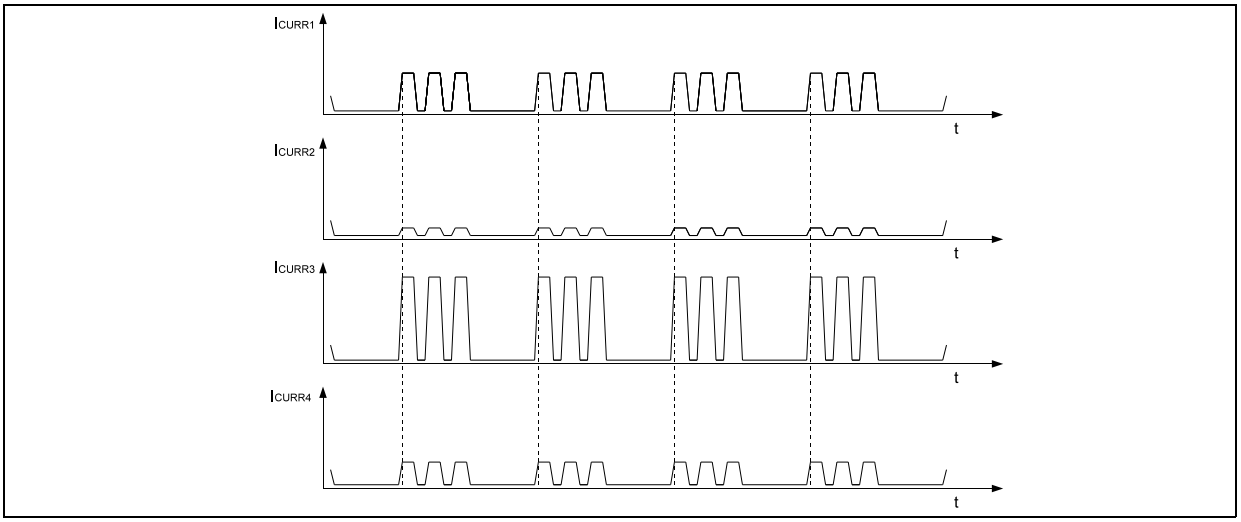
The new parameter can be found in Table 34. All other parameters keep the same and are shared with the Single Pulse Mode. These parameters can be found in Table 32. /

Table 34. Singe Pulse Mode Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tp_CURR	Pause time between multiple pulses		0		540	ms

Please mind that the settings for t_{r_CURR}, t_{f_CURR}, t_{on_CURR}, t_{off_CURR} and t_{p_CURR} and the pulse count number in register multiple_pulse are valid for all four current sinks at the same time. It is not possible to define individual time values for each current source differently to each other. The only parameter which can differ from on current source to another is the current which can be configured in registers curr1_current, curr2_current, curr3_current and curr4_current for each current source independently.

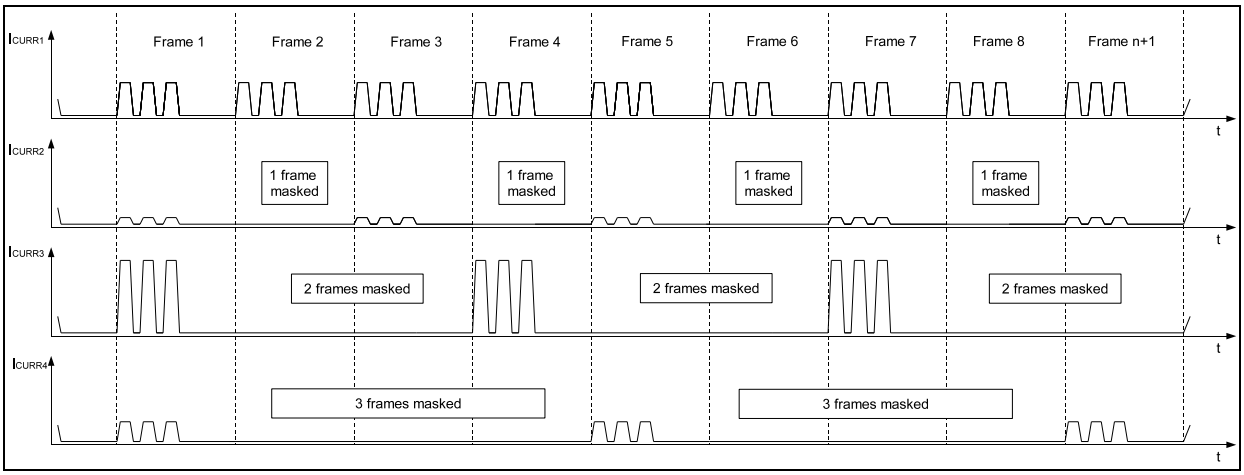
Figure 44. Multiple Pulse Mode - Example



8.10.3 Frame Mask Mode

An additional feature for creating unique LED lighting effects is the Frame Mask Mode. In order to use this mode there is no additional timing parameter necessary. All the timing parameters described in Section 8.10.1 and Section 8.10.2 are also valid for this third mode and can be combined together. There are no restrictions when using this mode together with Single- or Multiple Pulse Mode. For a better understanding how this special mode works a timing diagram example can be found in Figure 45 below.

Figure 45. Multiple Pulse Mode - Example

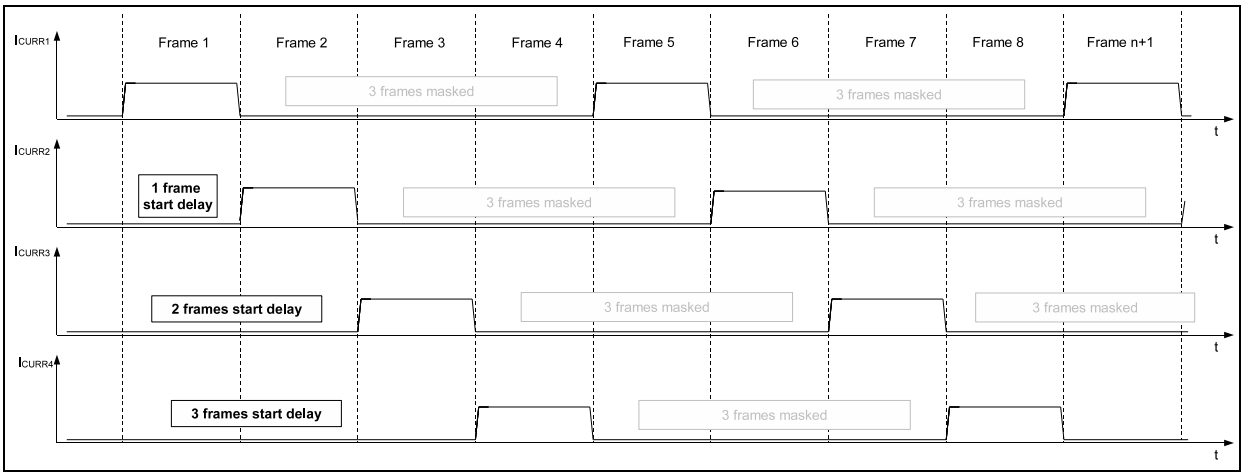


As the example shows, each defined pattern, no matter if it is a single pulse or multiple pulse pattern, can be divided into frames which are basically running in parallel mode. The pattern which has be defined with the different parameters like t_{r_CURR}, t_{on_CURR}, t_{off_CURR} and t_{p_CURR} is repeated in an endless loop. In order to enhance the functionality of the pattern generation it is possible to mask or skip frames in between the endless pattern loop. Each current source comes with a dedicated register to support masking of one frame up to four frames. This means the Frame Mask Mode allows the user to individually skip frames in each current source. The example above shows that the Frame Mask Register fmask_curr2 of CURR2 has been set to 1, which means every second frame will be masked out when playing the pattern. The Frame Mask Register fmask_curr3 of CURR3 has been set to 2, therefore two frames are masked out in the example. The register fmask_curr4 of CURR4 has been set to 3, thus three frames are masked out in the example. The frame mask order in the example is not fixed and can be easily exchanged depending on the Frame Mask Register setting for each current source.

8.10.4 Frame Start Delay Mode

The frame delay mode allows the user to add a start-delay for each current source separately in pattern generation mode. This feature allows an user to create again more complex lighting patterns like a running LED shown in the example in Figure 46.

Figure 46. Frame Start Delay Mode

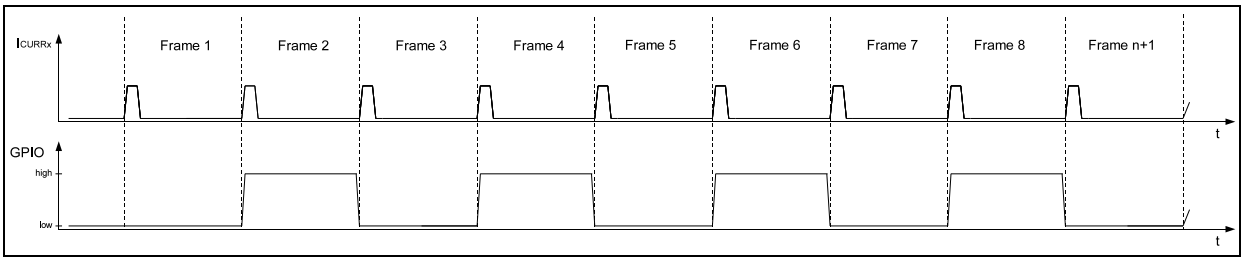


Each current source has a dedicated delay register(frame_delay1, frame_delay2, frame_delay3 and frame_delay4) which allow adding different start delays to each current source. This feature can of course be combined with the frame mask mode described in 8.10.3. In the example above the frame_delay2 register has been set to 1 to add one frame delay to CURR2. The frame_delay3 register has been set to 2 adding two frames startup delay to CURR3. CURR4 needs a startup delay of 3 frames which means theframe_delay4 registers must be set to 3. It is worth mentioning that there are also no restrictions when using this mode together with Single- or Multiple Pulse mode described in chapter 8.10.1 and 8.10.2.

8.10.5 GPIO Toggle Mode

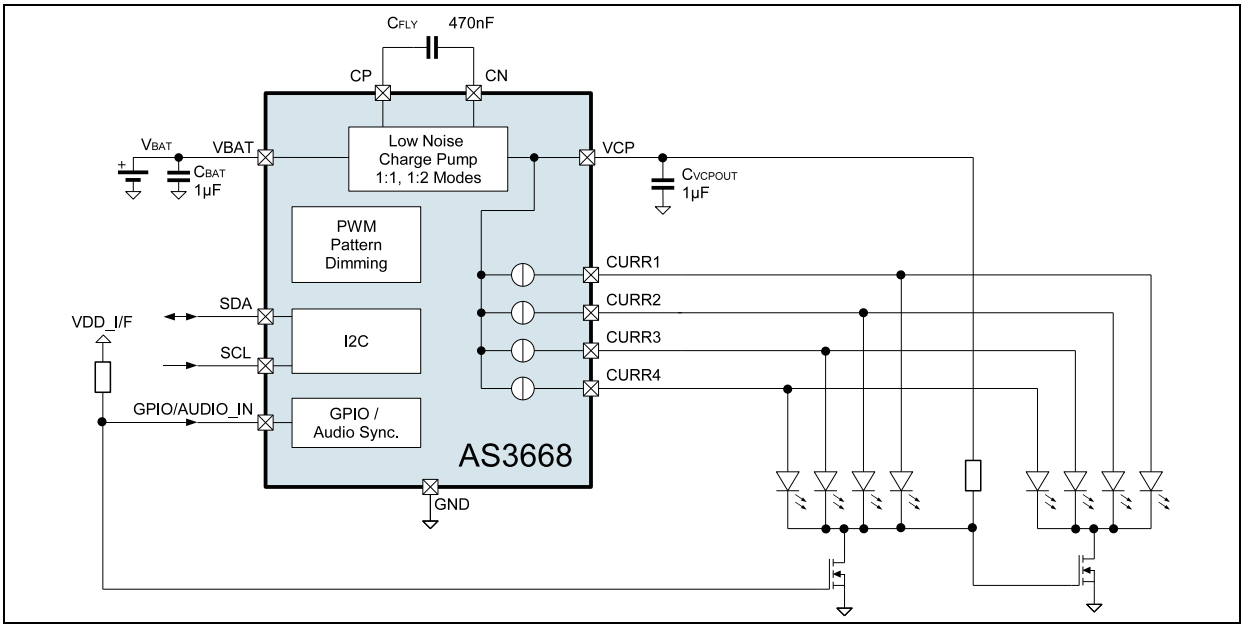
An add on feature which enables the user to use up to eight LEDs in pattern generation mode in a sequential order is the GPIO Toggle mode.

Figure 47. GPIO Toggle Mode 1 Frame



The mode can be enabled with the register gpio_toggle_en. Once the mode has been enabled register gpio_toggle_framenr gets activated and allows the user to select after how many frames the GPIO/AUDIO_IN pin toggles. An example is shown in Figure 47 above. The gpio_toggle_en register has been set to 1. The gpio_toggle_framenr register has also been set to 1. The GPIO/AUDIO_IN pin toggles after each frame. The pin can be used to control an external switch to enable some more LEDs. An example of such an application is shown in Figure 48. Please mind that it is not possible to operate all eight LEDs in parallel. It is only possible to enable either one or the other block. This mechanism is handled automatically with the external control transistors.

Figure 48. Application Proposal GPIO Toggle Mode



8.10.6 LED Pattern Control Registers

Table 35. PWM Control Register

0x15 PWM Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1	pwm_dim_shape	0	R/W	This bit defines if the current sources do logarithmic or linear up/down dimming. **0: logarithmic dimming** 1: linear dimming
0	pwm_src	0	R/W	Defines the PWM source. It can either be selected the internal PWM generator to dim the current sources or us the pin GPIO/AUDIO_IN as PWM input. **0: internal PWM generator** 1: external PWM input selected (GPIO/AUDIO_IN)

Table 36. PWM Control Register

0x16 PWM Timing Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	pwm_dim_speed_up	0x08	R/W	These bits define the value of t_{r_CURR} which is the dim speed when dimming up and down the current sources. The dim speed is valid for all current sources at the same time. 0000: immediate 0001: 0.12s 0010: 0.25s 0011: 0.38s 0100: 0.51s 0101: 0.77s 0110: 1.0s 0111: 1.6s **1000: 2.1s** 1001: 2.6s 1010: 3.1s 1011: 4.2s 1100: 5.2s 1101: 6.2s 1110: 7.3s 1111: 8.3s
3:0	pwm_dim_speed_down	0x08	R/W	These bits define the value of t_{r_CURR} which is the dim speed when dimming up and down the current sources. The dim speed is valid for all current sources at the same time. 0000: immediate 0001: 0.12s 0010: 0.25s 0011: 0.38s 0100: 0.51s 0101: 0.77s 0110: 1.0s 0111: 1.6s **1000: 2.1s** 1001: 2.6s 1010: 3.1s 1011: 4.2s 1100: 5.2s 1101: 6.2s 1110: 7.3s 1111: 8.3s

Table 37. PWM Trigger Register

0x17 PWM Trigger Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	start_dim	0	R/W	This bit defines in PWM mode of the current sources if the outputs are switched on/off directly or dimmed up/down using the timing of register pwm_dim_speed_up. **0: direct on/off of current sources** 1: logarithmic/linear - up/down dimming of current sources
3	dim_curr4	0	R	A register read of this register reflects the status of current source CURR4. If the register returns 0, the current source is switched off. If the register returns 1, the current source is switch on with the current defined in register curr4_current. **0: Current Source CURR4 is switched off** 1: Current Source CURR4 is switched on
			W	A write to this register defines the target value for CURR4. If 0 is written to this register CURR4 is switched off or dimmed down depending on register start_dim. If 1 is written to this register CURR4 is switched on or dimmed up depending on register start_dim. Mind that this setting is only effective if CURR4 is configured to PWM mode in register curr4_mode. 0: Target value of CURR4 for dimming down or direct control 1: Target value of CURR4 for dimming up or direct control
2	dim_curr3	0	R	A register read of this register reflects the status of current source CURR3. If the register returns 0, the current source is switched off. If the register returns 1, the current source is switch on with the current defined in register curr3_current. **0: Current Source CURR3 is switched off** 1: Current Source CURR3 is switched on
			W	A write to this register defines the target value for CURR3. If 0 is written to this register CURR3 is switched off or dimmed down depending on register start_dim. If 1 is written to this register CURR3 is switched on or dimmed up depending on register start_dim. Mind that this setting is only effective if CURR3 is configured to PWM mode in register curr3_mode. 0: Target value of CURR3 for dimming down or direct control 1: Target value of CURR3 for dimming up or direct control
1	dim_curr2	0	R	A register read of this register reflects the status of current source CURR2. If the register returns 0, the current source is switched off. If the register returns 1, the current source is switch on with the current defined in register curr2_current. **0: Current Source CURR2 is switched off** 1: Current Source CURR2 is switched on
			W	A write to this register defines the target value for CURR2. If 0 is written to this register CURR2 is switched off or dimmed down depending on register start_dim. If 1 is written to this register CURR2 is switched on or dimmed up depending on register start_dim. Mind that this setting is only effective if CURR2 is configured to PWM mode in register curr2_mode. 0: Target value of CURR2 for dimming down or direct control 1: Target value of CURR2 for dimming up or direct control

Table 37. PWM Trigger Register

0x17 PWM Trigger Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	dim_curr1	0	R	A register read of this register reflects the status of current source CURR1. If the register returns 0, the current source is switched off. If the register returns 1, the current source is switch on with the current defined in register curr1_current. **0: Current Source CURR1 is switched off** 1: Current Source CURR1 is switched on
			W	A write to this register defines the target value for CURR1. If 0 is written to this register CURR1 is switched off or dimmed down depending on register start_dim. If 1 is written to this register CURR1 is switched on or dimmed up depending on register start_dim. Mind that this setting is only effective if CURR1 is configured to PWM mode in register curr1_mode. 0: Target value of CURR1 for dimming down or direct control 1: Target value of CURR1 for dimming up or direct control

Table 38. Pattern Timing Register

0x18 Pattern Timing Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5:3	pattern_toff	0x03	R/W	These bits define the value of the parameter t_{off_CURR}. It defines the off time of CURR1, CURR2, CURR3 and CURR4 in pattern generation mode. The same value is used for all four current sources in parallel. 000: 0.08s 001: 0.15s 010: 0.28s **011: 0.54s** 100: 1.1s 101: 2.1s 110: 4.2s 111: 8.4s
2:0	pattern_ton	0	R/W	These bits define the value of the parameter t_{on_CURR}. It defines the on time of CURR1, CURR2, CURR3 and CURR4 in pattern generation mode. The same value is used for all four current sources in parallel. **000: 0.04s** 001: 0.07s 010: 0.14s 011: 0.27s 100: 0.53s 101: 1.1s 110: 2.1s 111: 4.2s

Table 39. Pattern Multiple Pulse Register

0x19 Pattern Multiple Pulse Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	multiple_pulse	0	R/W	Defines the number of multiple pulses applied to all current sources at the same time. **00: 1 pulse** 01: 2 pulses 10: 3 pulses 11: 4 pulses
1:0	tp_led	0	R/W	These bits define the value of parameter t_{P_CURR}. It defines the pause time for multiple pulse mode in pattern generation mode. **00: 0ms** 01: 150ms 10: 280ms 11: 540ms

Table 40. Pattern Frame Mask Register

0x1a Pattern Frame Mask Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	fmask_curr4	0	R/W	Defines the frames to be masked out in pattern generation mode for current source CURR4. **00: No frame mask for CURR4** 01: Mask 1 frame for CURR4 10: Mask 2 frames for CURR4 11: Mask 3 frames for CURR4
5:4	fmask_curr3	0	R/W	Defines the frames to be masked out in pattern generation mode for current source CURR3. **00: No frame mask for CURR3** 01: Mask 1 frame for CURR3 10: Mask 2 frames for CURR3 11: Mask 3 frames for CURR3
3:2	fmask_curr2	0	R/W	Defines the frames to be masked out in pattern generation mode for current source CURR2. **00: No frame mask for CURR2** 01: Mask 1 frame for CURR2 10: Mask 2 frames for CURR2 11: Mask 3 frames for CURR2
1:0	fmask_curr1	0	R/W	Defines the frames to be masked out in pattern generation mode for current source CURR2. **00: No frame mask for CURR1** 01: Mask 1 frame for CURR1 10: Mask 2 frames for CURR1 11: Mask 3 frames for CURR1

Table 41. Pattern Start Control Register

0x1b Pattern Start Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	pattern_phase_out	0	R/W	The bit defines the way how a pattern is being stopped when the pattern_enable register is cleared. If the bit is set to 0 and the pattern_enable register is cleared the running pattern stops immediately. If the bit is set to 1 and the pattern_enable is cleared the pattern finishes the running frame and stops afterwards. **0: Stop pattern immediately** 1: Phase-out pattern
1	pattern_enable	0	W	Starts the pattern generation on current sources. 0: Pattern generation off 1: Start of pattern generation
0	pattern_start_src	1	R/W	Selects the input source to trigger the pattern generation start. 0: Pattern enable by software bit **1: pattern enable by GPIO/AUDIO_IN**

Table 42. Pattern Frame Start Delay Register

0x1c Pattern Frame Start Delay Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	frame_delay4	0	R/W	Defines the start delay of CURR4 in pattern generation mode. Note that changes in this register are only getting active after a restart of the pattern generation unit by toggling the pattern_enable bit. **00: No start delay for CURR4** 01: 1 frame start delay for CURR4 10: 2 frames start delay for CURR4 11: 3 frames start delay for CURR4
5:4	frame_delay3	0	R/W	Defines the start delay of CURR3 in pattern generation mode. Note that changes in this register are only getting active after a restart of the pattern generation unit by toggling the pattern_enable bit. **00: No start delay for** CURR3 01: 1 frame start delay for CURR3 10: 2 frames start delay for CURR3 11: 3 frames start delay for CURR3
3:2	frame_delay2	0	R/W	Defines the start delay of CURR2 in pattern generation mode. Note that changes in this register are only getting active after a restart of the pattern generation unit by toggling the pattern_enable bit. **00: No start delay for** CURR2 01: 1 frame start delay for CURR2 10: 2 frames start delay for CURR2 11: 3 frames start delay for CURR2
1:0	frame_delay1	0	R/W	Defines the start delay of CURR1 in pattern generation mode. Note that changes in this register are only getting active after a restart of the pattern generation unit by toggling the pattern_enable bit. **00: No start delay for** CURR1 01: 1 frame start delay for CURR1 10: 2 frames start delay for CURR1 11: 3 frames start delay for CURR1

Table 43. GPIO Toggle Control Register

0x1d GPIO Toggle Control Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	gpio_toggle_en	0	W	This bit enables the GPIO/AUDIO_IN pin to toggle after a defined number of frames. The number of frames where the pin toggles is defined in register gpio_toggle_framenr. **0: GPIO toggle disabled** 1: GPIO toggle enabled
1:0	gpio_toggle_framenr	0	R/W	This register defines the number of frames where the GPIO/AUDIO_IN toggles. The register setting is only active if gpio_toggle_en bit is enabled. **00: GPIO toggles after 1 frame** 01: GPIO toggles after 2 frames 10: GPIO toggles after 3 frames 11: GPIO toggles after 4 frames

9 Register Map

Table 44. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
Chip ID									
3Eh	CHIP ID1	chip_id1<7:0> Constant value 'b10100101'							
3Fh	CHIP ID2	chip_id2<7:4>				revision<3:0>			
LED Control									
01h	CurrX control	curr4_mode<7:6> 0: current source 4 off; 1:current source 4 on; 2: current source 4 PWM; 3: Current source 4 Patt.		curr3_mode<5:4> 0: current source 3 off; 1:current source 3 on; 2: current source 3 PWM; 3: Current source 3 Patt.		curr2_mode<3:2> 0: current source 2 off; 1:current source 2 on; 2: current source 2 PWM; 3: Current source 2 Patt.		curr1_mode<1:0> 0: current source 1 off; 1:current source 1 on; 2: current source 1 PWM; 3: Current source 1 Patt.	
02h	CURR1 current	curr1_current<7:0> Output current for current source CURR1 = 0mA ... 25.5mA; 256 steps of 0.1mA.							
03h	CURR2 current	curr2_current<7:0> Output current for current source CURR2 = 0mA ... 25.5mA; 256 steps of 0.1mA.							
04h	CURR3 current	curr3_current<7:0> Output current for current source CURR3 = 0mA ... 25.5mA; 256 steps of 0.1mA.							
05h	CURR4 current	curr4_current<7:0> Output current for current source CURR4 = 0mA ... 25.5mA; 256 steps of 0.1mA.							
2Bh	CurrX low voltage status					curr4_low_v 0: CURR4 voltage ok 1: CURR4 low voltage	curr3_low_v 0: CURR3 voltage ok 1: CURR3 low voltage	curr2_low_v 0: CURR2 voltage ok 1: CURR2 low voltage	curr1_low_v 0: CURR1 voltage ok 1: CURR1 low voltage
GPIO Control									
06h	GPIO Control						gpio_in_invert 0: non-inverted dig. input 1: inverted digital input	gpio_in_en 0: analog input 1: digital input	gpio_mode 0: Input only 1: Output (open drain)

Table 44. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
07h	GPIO Output								gpio_out 0: GPIO pin low 1: GPIO pin high
08h	GPIO Signal								gpio_in 0: GPIO pin low 1: GPIO pin high
PWM control									
15h	PWM Control							pwm_dim_shape 0: logarithmic ramp 1: linear ramp	pwm_src 0: internal PWM 1: external PWM
16h	PWM Timing	pwm_dim_speed_up<7:4> 0: immediate 1: 0.12s 2: 0.25s 3: 0.38s 4: 0.51s 5: 0.77s 6: 1.0s 7: 1.6s 8: 2.1s 9: 2.6s 10: 3.1s 11: 4.2s 12: 5.2s 13: 6.2s 14: 7.3s 15: 8.3s				pwm_dim_speed_down 0: immediate 1: 0.12s 2: 0.25s 3: 0.38s 4: 0.51s 5: 0.77s 6: 1.0s 7: 1.6s 8: 2.1s 9: 2.6s 10: 3.1s 11: 4.2s 12: 5.2s 13: 6.2s 14: 7.3s 15: 8.3s			
17h	PWM Trigger				start_dim 0: no dimming 1: start log dimming	dim_curr4 0: CURR4 off 1: CURR4 on	dim_curr3 0: CURR3 off 1: CURR3 on	dim_curr2 0: CURR2 off 1: CURR2 on	dim_curr1 0: CURR1 off 1: CURR1 on
Pattern Control									
18h	Pattern Timing			pattern_toff<5:3> 000: 0.08s 001: 0.15s 010: 0.28s 011: 0.54s 100: 1.1s 101: 2.1s 110: 4.2s 111: 8.4s			pattern_ton<2:0> 000: 0.04s 001: 0.07s 010: 0.14s 011: 0.27s 100: 0.53s 101: 1.1s 110: 2.1s 111: 4.2s		
19h	Multiple Pulse	multiple_pulse<7:6> 00: 1 pulse 01: 2 pulses 10: 3 pulses 11: 4 pulses						tp_led<1:0> 00: 0ms 01: 150ms 10: 280ms 11: 540ms	
1Ah	Frame Mask	fmask_curr4<7:6> 00: No frame mask for CURR4 01: Mask 1 frame for CURR4 10: Mask 2 frame for CURR4 11: Mask 3 frame for CURR4		fmask_curr3<5:4> 00: No frame mask for CURR3 01: Mask 1 frame for CURR3 10: Mask 2 frame for CURR3 11: Mask 3 frame for CURR3		fmask_curr2<3:2> 00: No frame mask for CURR2 01: Mask 1 frame for CURR2 10: Mask 2 frame for CURR2 11: Mask 3 frame for CURR2		fmask_curr1<1:0> 00: No frame mask for CURR1 01: Mask 1 frame for CURR1 10: Mask 2 frame for CURR1 11: Mask 3 frame for CURR1	
1Bh	Start Control						pattern_phase_out 0: turn off immediately 1: phase out pattern	pattern_enable 0: pattern off 1: start pattern	pattern_start_src 0: Softw. pattern enable 1: GPIO pattern enable
1Ch	Pattern Frame Start Delay	frame_delay4 0: no delay 1: CURR4 1 frame delay 2: CURR4 2 frames delay 3:CURR4 3 frames delay		frame_delay3 0: no delay 1: CURR3 1 frame delay 2: CURR3 2 frames delay 3:CURR3 3 frames delay		frame_delay2 0: no delay 1: CURR2 1 frame delay 2: CURR2 2 frames delay 3:CURR2 3 frames delay		frame_delay1 0: no delay 1: CURR1 1 frame delay 2: CURR1 2 frames delay 3:CURR1 3 frames delay	
1Dh	GPIO toggle control						gpio_toggle_en 0: disabled 1: enabled	gpio_toggle_framenr 0: 1 frame 1: 2 frames 2: 3 frames 3: 4 frames	
ADC Result									
26h							adc_select 0: Audip Preamplifier 1: GPIO direct	adc_mode 0: linear ADC 1: logarithmic ADC	adc_on 0: ADC off 1: ADC on
27h	ADC Result					adc_result<3:0>			

Table 44. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
Charge Pump									
00h	Reg Control						cp_on 0: Charge Pump off 1: Charge Pump on		
23h	CP Control		cp_auto_on 0: Manual CP Mode 1: automatic CP Mode	cp_start_debounce 0: 32ms debounce time 1: 240µs debounce time	cp_mode_switching 0: Automatic Mode 1: Manual Mode		cp_mode 0: 1:1 mode 1: 1:2 mode		cp_clk 0: 1MHz 1: 500kHz
Overtemperature Control									
29h	Overtemp Control		vmon_vbat<6:5> 0: ~2V - Shutdown Mode 01: 3.0V - Standby Mode 10: 3.15V - Standby Mode 11: 3.3V - Standby Mode		shutdown_enable 0: disable shutdown 1: enable shutdown		rst_ov_temp	ov_temp	ov_temp_on 0: temp supervision off 1: temp supervision on
Audio Control									
40h	Audio AGC		agc_up_level 0: Normal AGC up switching level threshold 1: AGC up switching threshold increased	agc_down_level 0: Normal AGC down switching level threshold 1: AGC down switching threshold increased	decay_agc_down<4:3> 00: 0.131s 01: 0.262s 10: 0.393s 11: 0.524s		decay_agc_up<2:1> 00: 0.262s 01: 0.524s 10: 0.786s 11: 1.049s		agc_on 0: AGC switched off 1: AGC switched on
41h	Audio Input Buffer	audio_dis_start 0: input cap precharge 1: no precharging	audio_man_start 0: auto precharge 1: manual precharge	audio_gain<5:1> Controls the audio input gain from -6dB ... +25dB in 1dB steps					aud_buf_on 0: Audio Buffer off 1: Audio Buffer on
42h	Audio Control	audio_input_pin 0: GPIO 1: CURR4	pld_off 0: Pull down enabled 1: Pull down disabled	adc_characteristic 0: x*250mV (linear) 1: x*50mV (linear) 0: $75mV*2^{x}$ (log) 1: $75mV*2^{x}$ (log)	audio_decay<4:3> 00: 10ms 01: 20ms 10: 40ms 11: 80ms		audiosync_mode<2:0> 000: 4 LED bar code 001: 4 LED bar code with dimming 010: running LED bar code 011: running LED bar code with dimming 100: RGB 101: RGB with dimming 110: 4 LED parallel with dimming 111: -		
43h	Audio Output					curr4_aud_en 0: CURR4 normal mode 1: CURR4 audio sync	curr3_aud_en 0: CURR3 normal mode 1: CURR3 audio sync	curr2_aud_en 0: CURR2 normal mode 1: CURR2 audio sync	curr1_aud_en 0: CURR1 normal mode 1: CURR1 audio sync

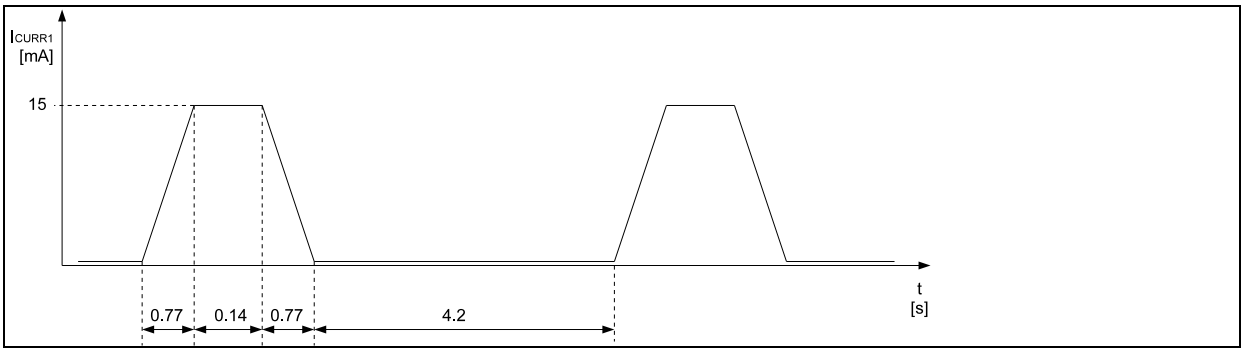
10 Application Information

10.1 LED Software Implementation Examples

10.1.1 Simple Breathlight Pattern with one LED

In this example we'd like to use CURR1 in pattern generation mode to create a simple breathlight pattern without continuous I2C traffic. This helps to unload the calculation power from the CPU.

Figure 49. Simple Breathlight Pattern Example



The timing example shown in Figure 49 above, can be easily implemented with just a couple of I2C commands.

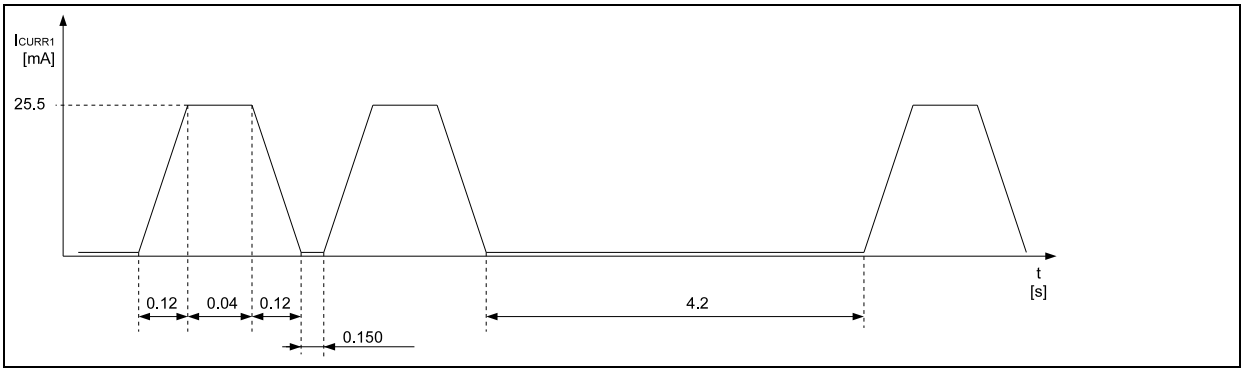
Table 45. Code Example Simple Breathlight Pattern

Register Name	Address	Write Value	Comments
CurrX Control	0x01	0x03	Enable CURR1 for pattern generation mode. Other current sources are off
CURR1 Current	0x02	0x96	Set the output current of CURR1 to 15mA.
PWM Timing	0x16	0x55	Define Rise/Fall time with 0,77s
Pattern Timing	0x18	0x32	Define 0,15s on time and 4,21s off time
Start Control	0x1B	0x02	Start breathlight pattern

10.1.2 Dual Pulse Pattern with one LED

In this example we would like to use CURR1 in pattern generation mode to create a simple dual pulse pattern without continuous I2C traffic. This helps again to unload the CPU.

Figure 50. Dual Pulse Pattern Example



The timing example shown in Figure 50 above, can be easily implemented with just a couple of I2C commands.

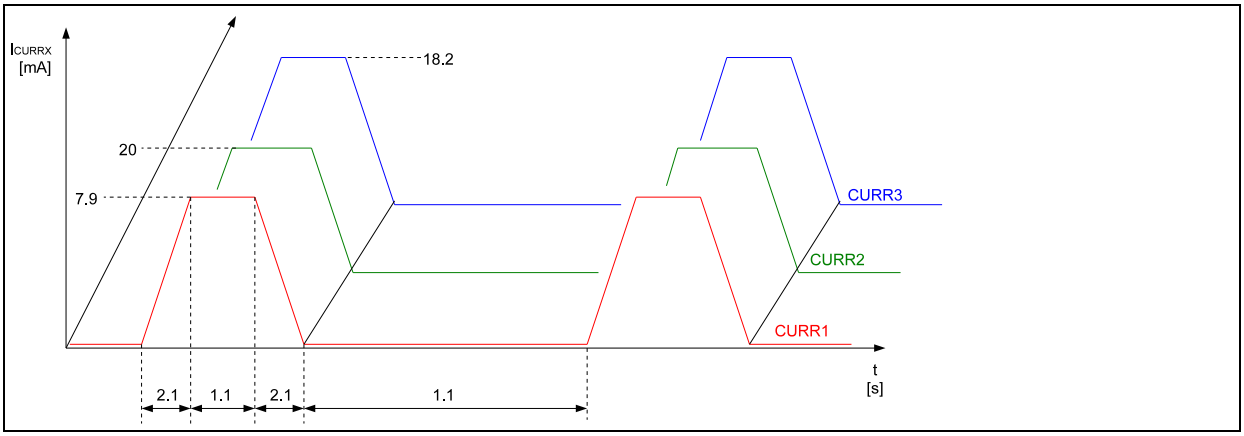
Table 46. Code Example Dual Pulse Pattern Example

Register Name	Address	Write Value	Comments
CurrX Control	0x01	0x03	Enable CURR1 for pattern generation mode. Other current sources are off
CURR1 Current	0x02	0xFF	Set the output current of CURR1 to 25,5mA.
PWM Timing	0x16	0x11	Define Rise/Fall time with 0,12s
Pattern Timing	0x18	0x30	Define 0,04s on time and 4,2s off time
Multiple Pulse	0x19	0x41	Define 2 pulses and 150ms pause time
Start Control	0x1B	0x02	Start breathlight pattern

10.1.3 RGB LED Pattern

In this example we would like to demonstrate how to use an RGB LED which is connected to CURR1, CURR2 and CURR3.

Figure 51. RGB Pulse Pattern Example



With the timing example above you get a mixture of red, green and blue color. Table 43 below shows how to configure the device to get the pattern shown in Figure 51.

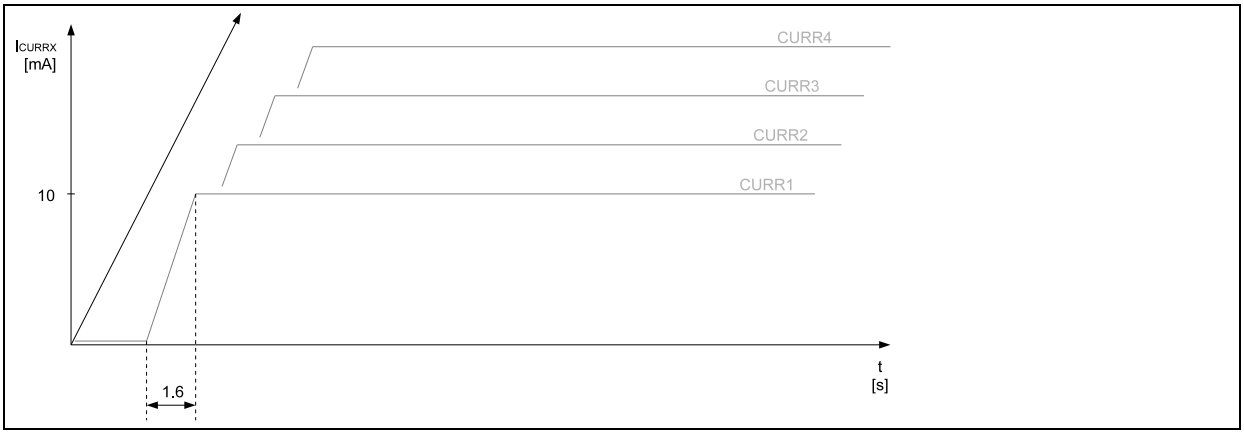
Table 47. Code Example RGB Pulse Pattern

Register Name	Address	Write Value	Comments
CurrX Control	0x01	0x3F	Enable CURR1, CURR2 and CURR3 for pattern generation mode. CURR4 is in off mode.
CURR1 Current	0x02	0x4F	Set the output current of CURR1 to 7,9mA.
CURR2 Current	0x03	0xC8	Set the output current of CURR2 to 20mA.
CURR3 Current	0x04	0xB6	Set the output current of CURR3 to 18,2mA.
PWM Timing	0x16	0x88	Define Rise/Fall time with 2.1s
Pattern Timing	0x18	0x25	Define 1,1s on time and 1,1s off time
Multiple Pulse	0x19	0x00	Define single pulse mode
Start Control	0x1B	0x02	Start breathlight pattern

10.1.4 Parallel Up - Dimming

In this example we would like to demonstrate how to do simple PWM up-dimming of all four LEDs in parrallel.

Figure 52. PWM Up-Dimming Example



If the output current of all four current sources is configured according to the requirements of the application it is possible to dimm the LEDs up with a single I2C command.

Table 48. Code Example Up-Dimming

Register Name	Address	Write Value	Comments
CurrX Control	0x01	0xAA	Enable CURR1, CURR2, CURR3 and CURR4 for PWM mode.
CURR1 Current	0x02	0x64	Set the output current of CURR1 to 10mA.
CURR2 Current	0x03	0x64	Set the output current of CURR2 to 10mA.
CURR3 Current	0x04	0x64	Set the output current of CURR3 to 10mA.
CURR4 Current	0x05	0x64	Set the output current of CURR4 to 10mA.
PWM Timing	0x16	0x77	Define dimming time with 1.6s
PWM Trigger	0x17	0x1F	Start up-dimming of all current sources with 1.7s dimming time.

10.1.5 Parallel Down- Dimming

In this example we would like to demonstrate how to do simple PWM down-dimming of all four LEDs in parallel.

Figure 53. PWM Down-Dimming Example

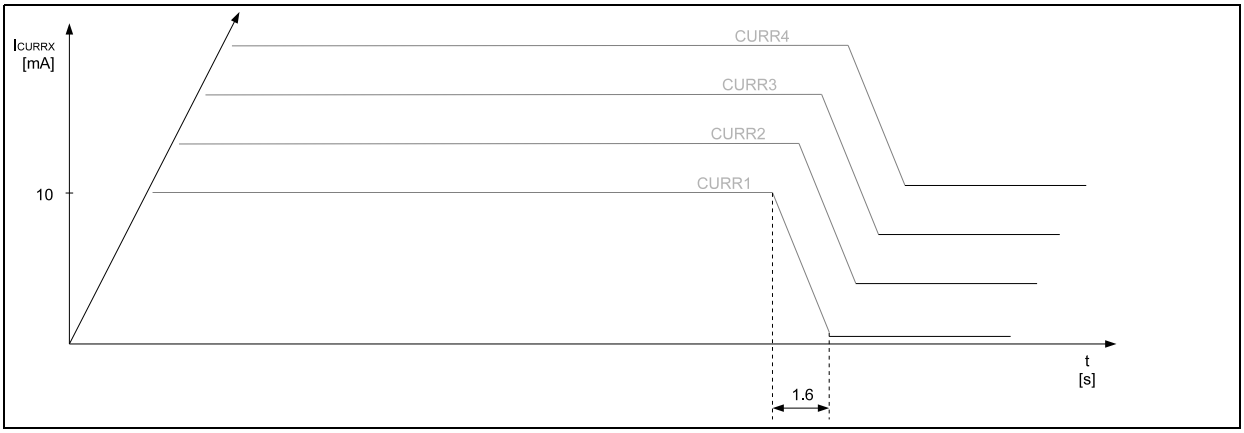


Table 49. Code Example Down-Dimming

Register Name	Address	Write Value	Comments
CurrX Control	0x01	0xAA	Enable CURR1, CURR2, CURR3 and CURR4 for On mode.
CURR1 Current	0x02	0x64	Set the output current of CURR1 to 10mA.
CURR2 Current	0x03	0x64	Set the output current of CURR2 to 10mA.
CURR3 Current	0x04	0x64	Set the output current of CURR3 to 10mA.
CURR4 Current	0x05	0x64	Set the output current of CURR4 to 10mA.
PWM Trigger	0x17	0x0F	Enable CURR1, CURR2, CURR3 and CURR4 for PWM mode. All four current sources keep switched on when we change from On Mode to PWM Mode.
PWM Timing	0x16	0x77	Define dimming time with 1.6s
PWM Trigger	0x17	0x10	Start down-dimming of all current sources with 1.7s dimming time.

10.2 Hardware Examples

Figure 54. AS3668 Standard 4 Channel LED Application Example

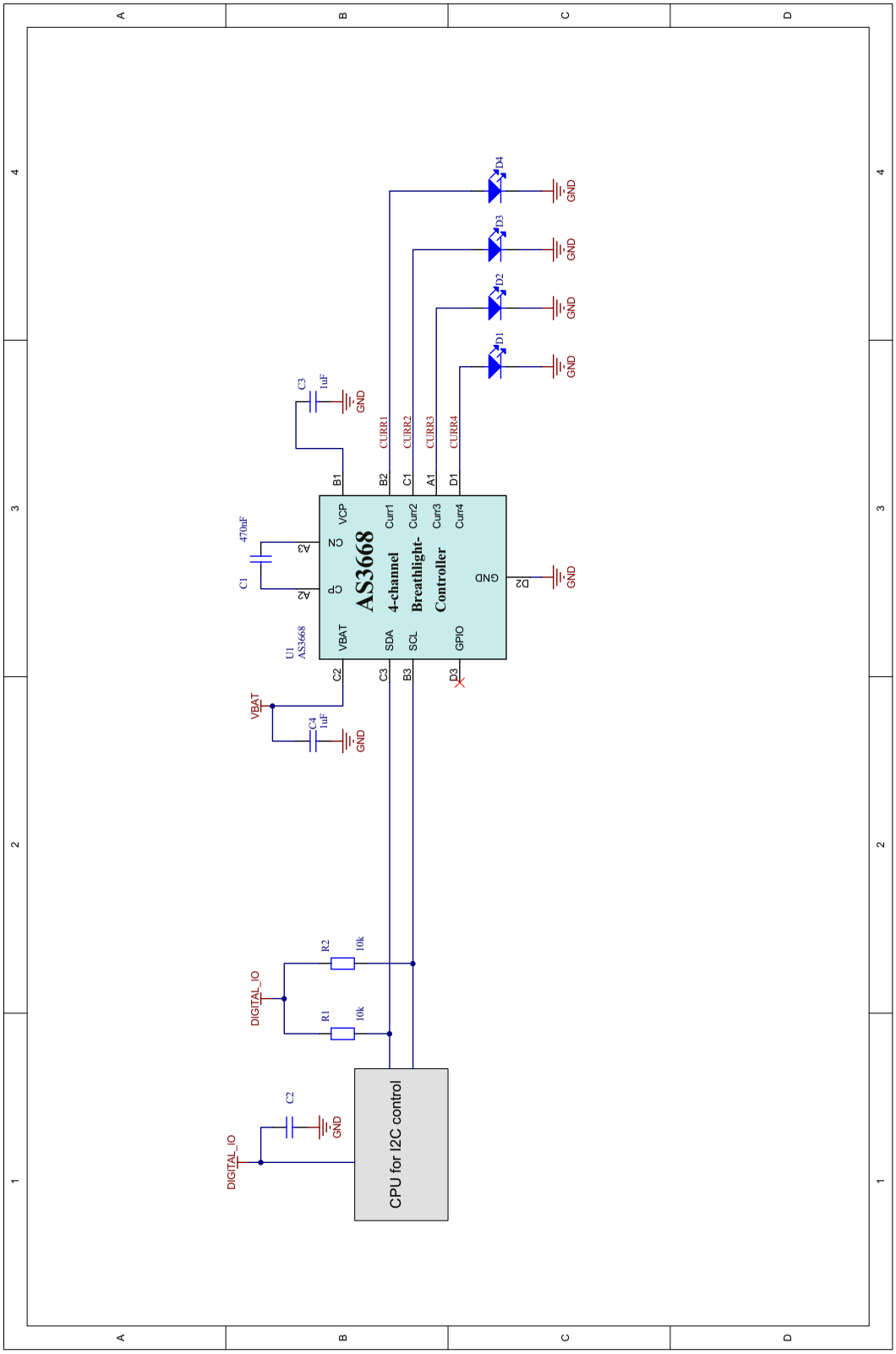


Figure 55. AS3668 Standard RGB LED Operation with GPIO Control Application Example

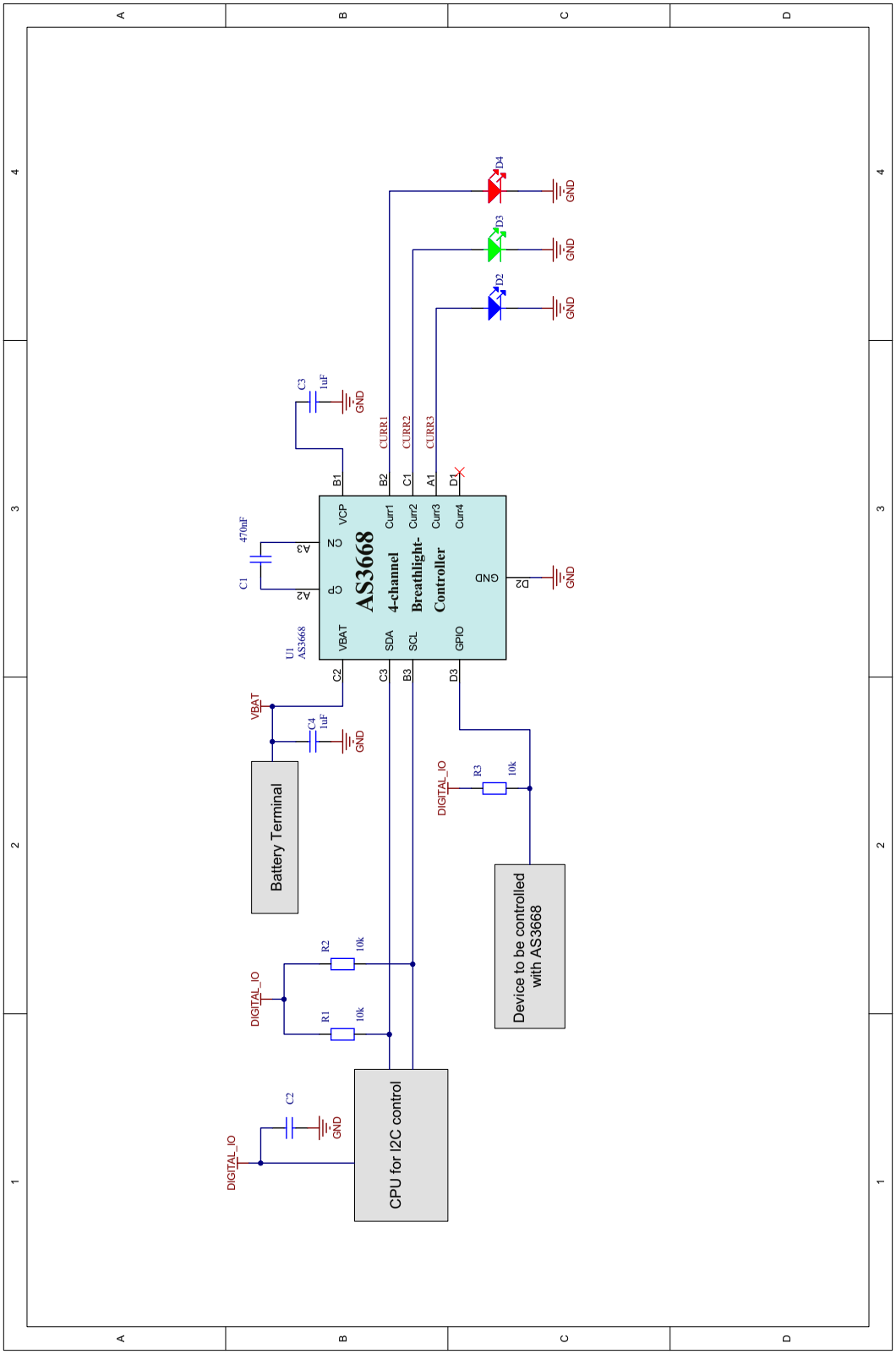


Figure 56. AS3668 Audio Synchronization Application Example

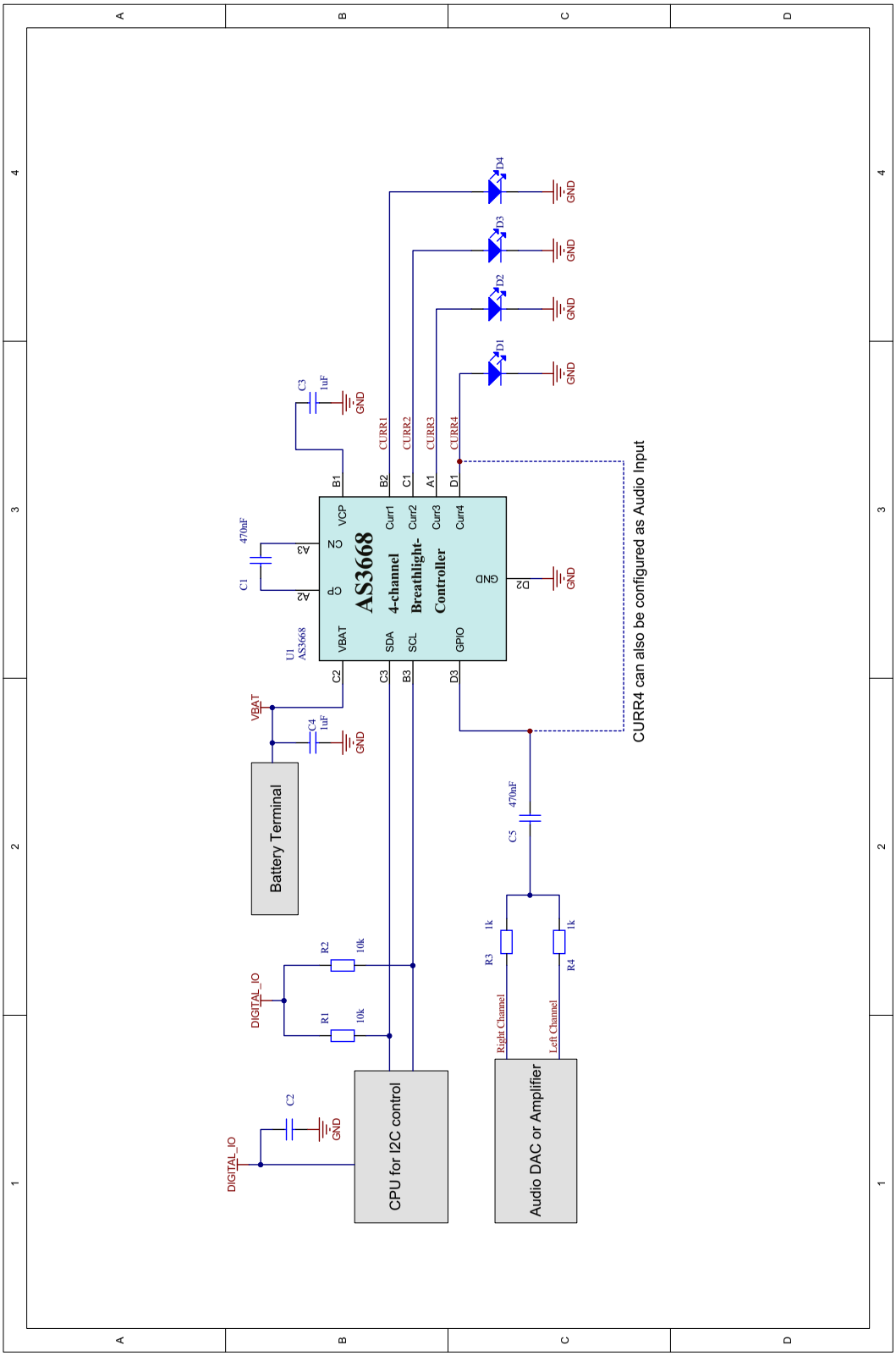


Figure 57. AS3668 Charger Application Example with Audio Synchronization

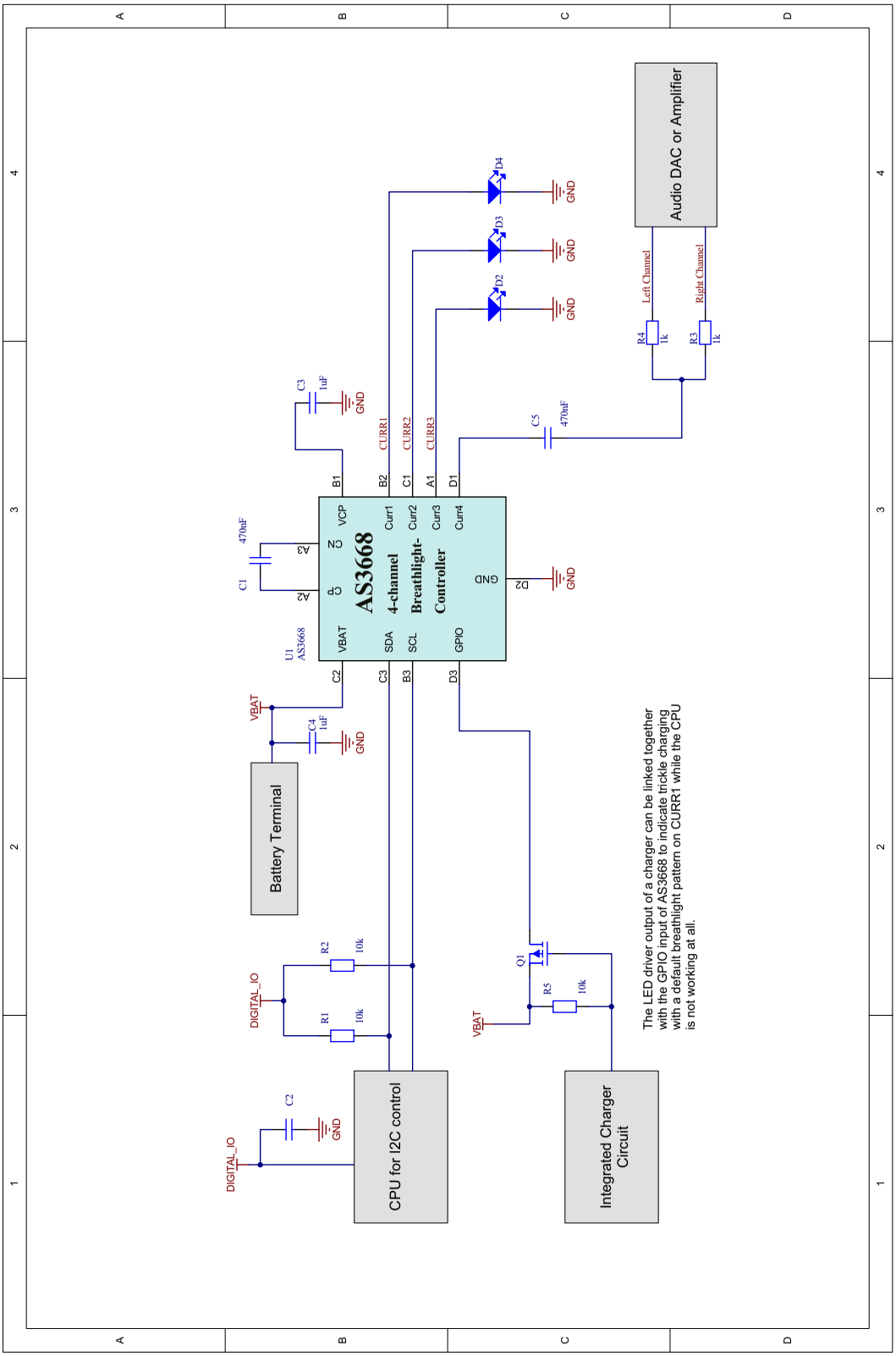
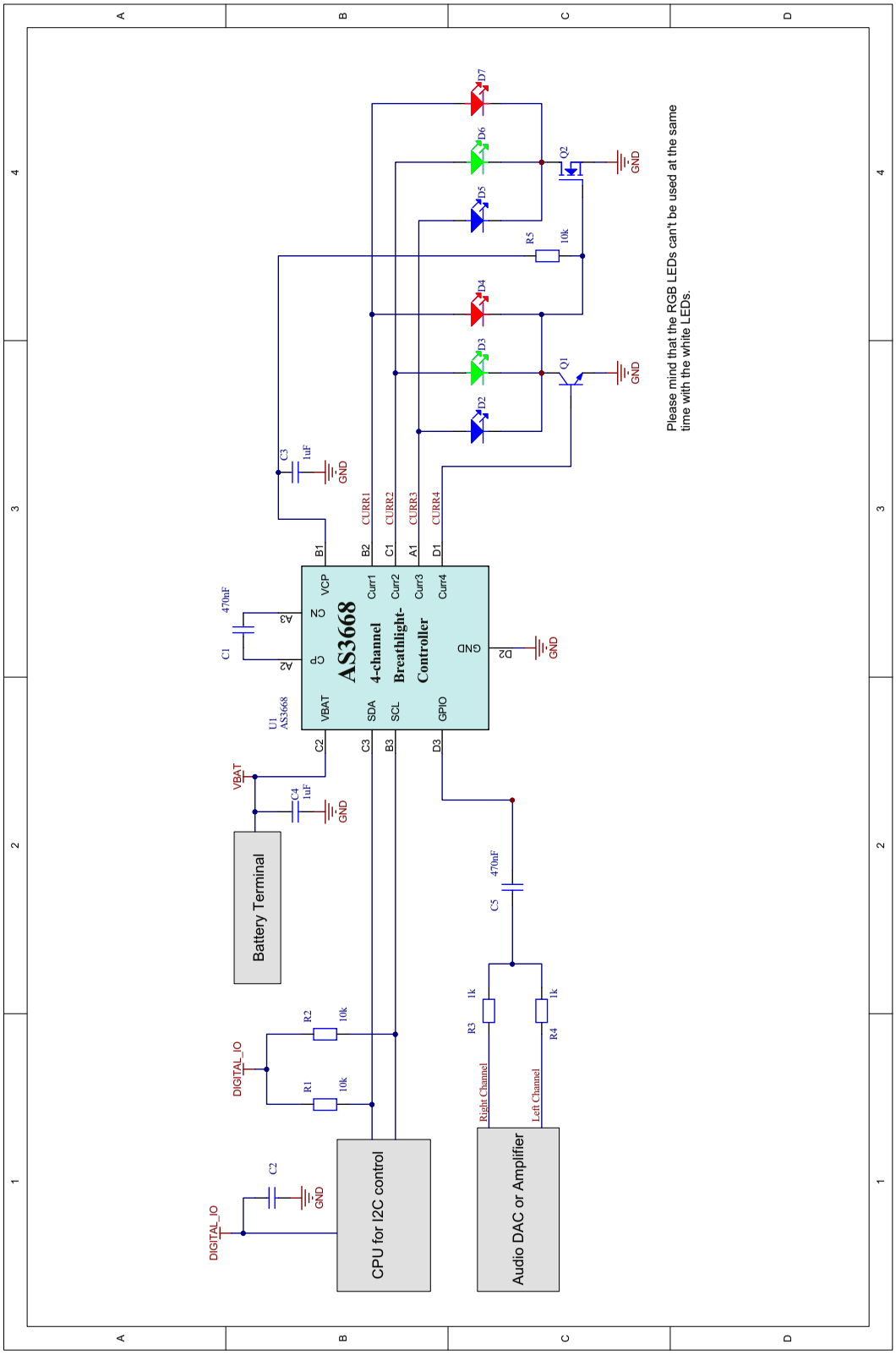


Figure 58. AS3668 Dual RGB LED Application Example



11 Package Drawings and Markings

The device is available in a *12-pin WL-CSP (1.255x1.680mm)* package.

Figure 59. 12-pin WL-CSP (1.255x1.680mm) Marking

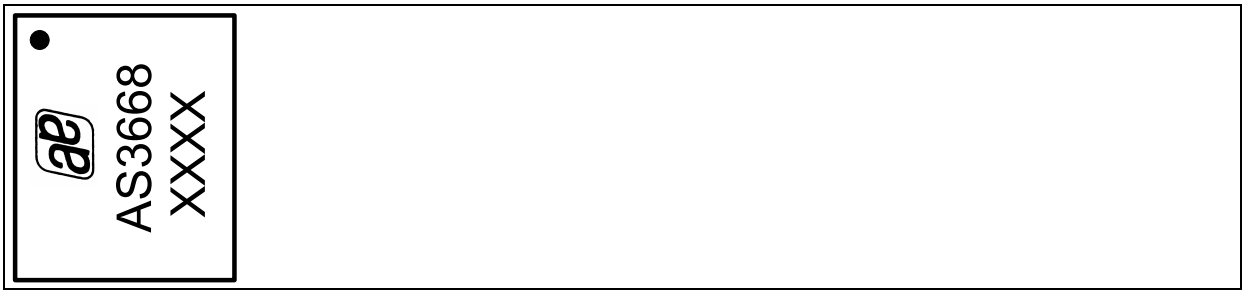
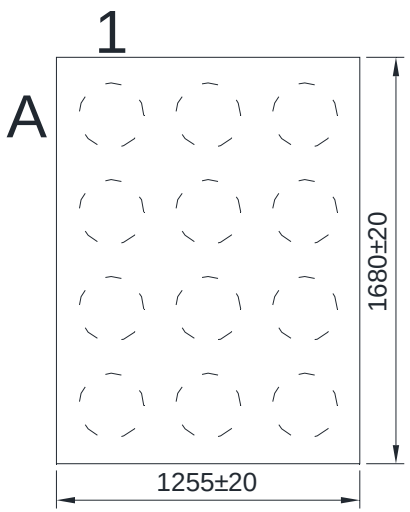


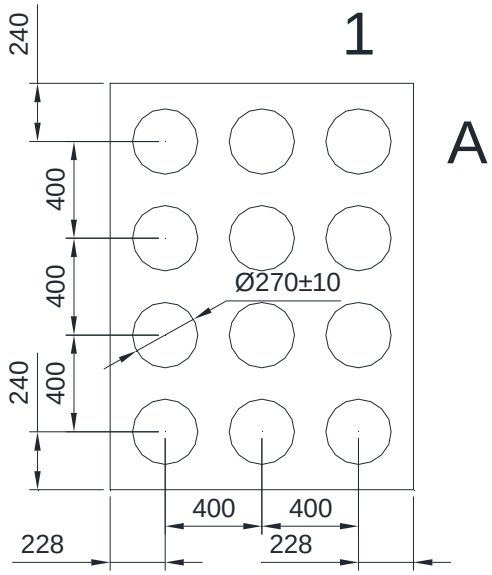
Table 50. Packaging Code XXXX

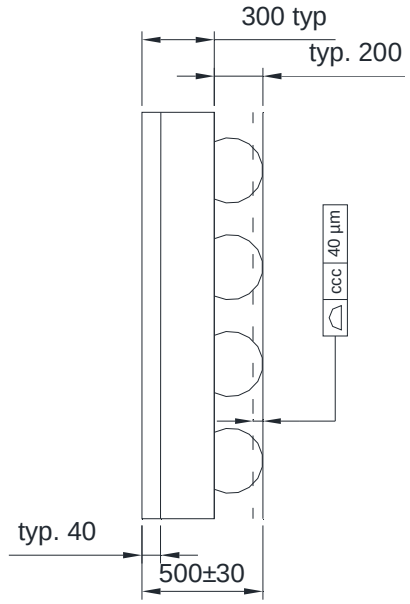
XXXX
encoded Datecode

top through view



bottom view (ball side)





Notes:
ccc Coplanarity
All dimensions in µm

Figure 60. 12-pin WL-CSP (1.255x1.680mm) Package Drawing

Revision History

Revision	Date	Owner	Description
1.0	11/02/11	hgt	first release
1.1	12/15/11	hgt	updated electrical characteristics; updated Figure 25 and Figure 36

Note: Typos may not be explicitly mentioned under revision history.

12 Ordering Information

The devices are available as the standard products shown in Table 51.

Table 51. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS3668-BQFT	AS3668	4-channel smart LED driver	Tape & Reel	12-pin WL-CSP (1.255x1.680mm)

Note: All products are RoHS compliant and austriamicrosystems green.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

Copyrights

Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

austriamicrosystems

Contact Information

Headquarters

austriamicrosystems AG
Tobelbaderstrasse 30
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact