AS1367

150mA, Adaptive Low Dropout Linear Regulator

1 General Description

The AS1367 is a precise, low noise, high speed, low dropout regulator with adaptive operation. AS1367 adapts the bias current of the control loop to the load current. As the load current increases, the bias current tracks the increase in order to improve the regulator transient performance. As a result, improved efficiency is obtained at low load currents.

Additional features provided by the AS1367 are low dropout operation, high ripple rejection, and excellent noise performance. Normal preset output voltage operation is provided by connecting the SET pin to ground. If non-standard output voltages are required, the SET pin provides access to the feedback point of the error loop when the SET pin is <100mV. The reference voltage is 1V in this condition.

The EN pin turns on the regulator. When the enable pin is low, the regulator is turned off, and a 740Ω (typ) discharge path is enabled between the output pin and ground. This ensures a consistent discharge of the load capacitance at the regulator output pin.

A Power OK comparator monitors the voltage on the SET pin and if the voltage goes out of regulation (e.g. during dropout, current limit, or thermal shutdown), the POK pin goes low. If the pin SET is connected to GND, an internal resistive-divider is activated and connected to the output. Therefore, the Power-OK functionality is available for pre-set and adjustable voltage applications.

Low noise operation is ensured by connecting a 10nF capacitor between the BYP pin and OUT pin. Transient performance is assisted by the path through the BYP capacitor to the error amplifier.

Comprehensive protection is built-in. Apart from short circuit and over-current protection, thermal protection shuts down the device when the die temperature reaches 160°C.

The device is available in a 8-pin TDFN 2x2 package.

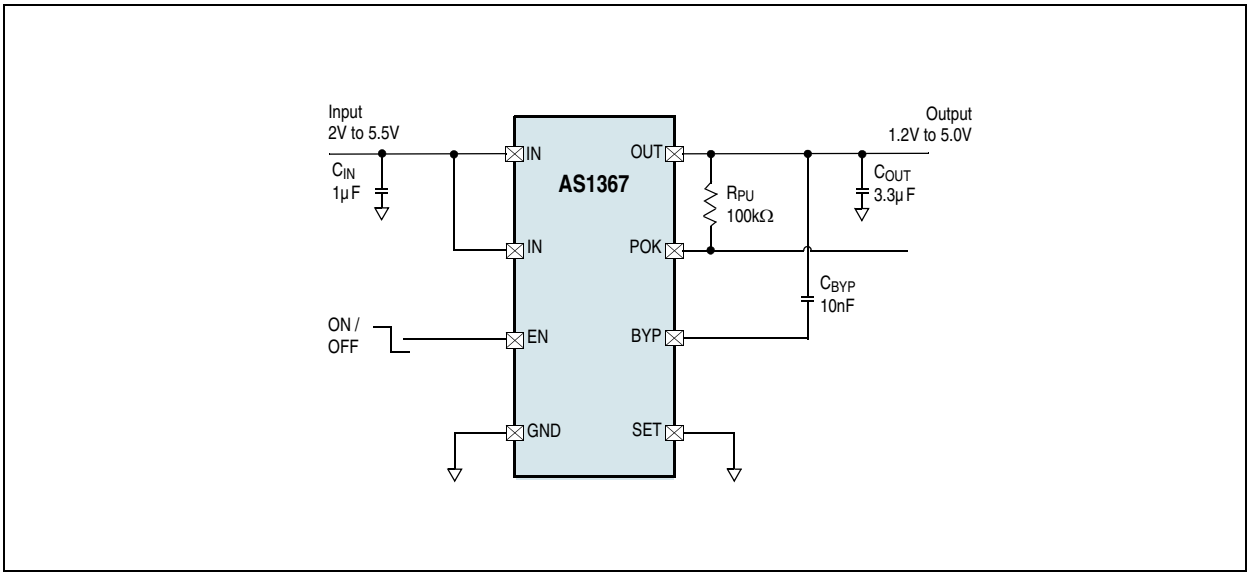
2 Key Features

- Low Dropout Voltage: 110mV @ 150mA load
- Operating Input Voltage Range: 2.0V to 5.5V
- Output Voltage Range: 1.2V to 5.0V (50mV steps)
- Maximum Output Current: 150mA
- Low Shutdown Current: 100nA
- High PSRR: 60dB @ 10kHz
- Integrated Over-temperature / Over-current Protection
- Under-Voltage Lockout Feature
- Chip Enable Input
- Power-OK
- Low Quiescent Current: 10µA
- Low Output Noise: 15µV @ 100kHz Bandwidth
- Operating Temperature Range: -40°C to +85°C
- 8-pin TDFN 2x2 Package

3 Applications

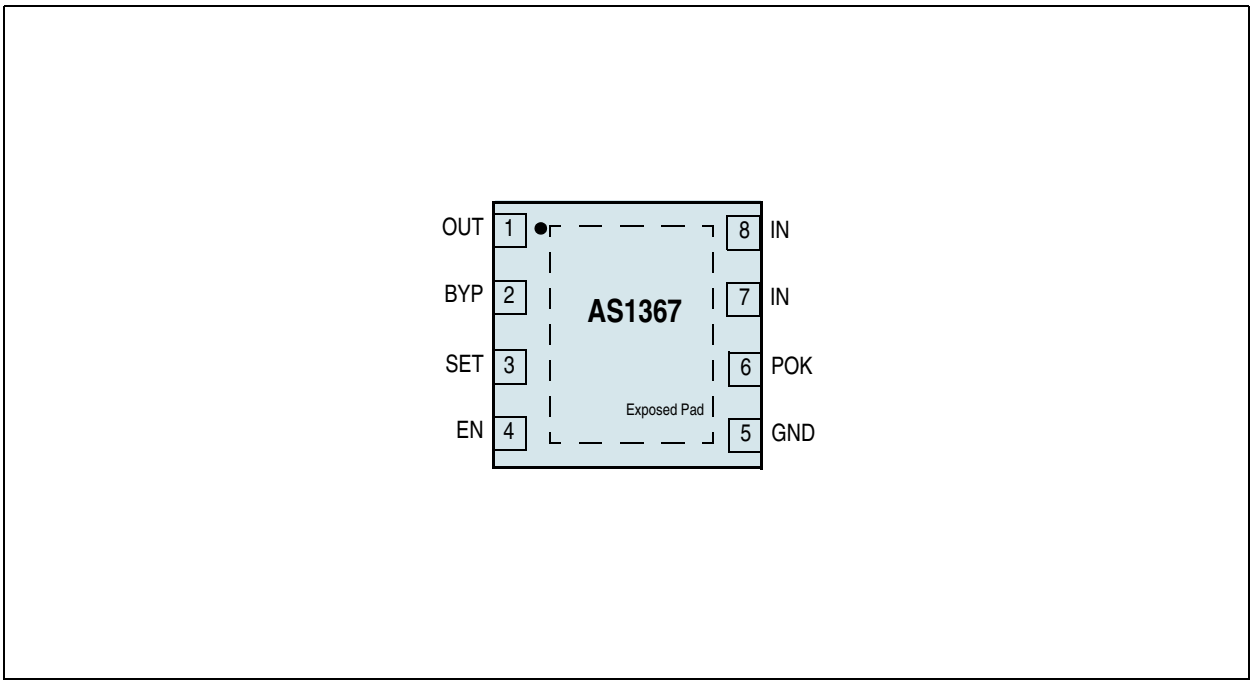
The AS1367 is ideal for cellular phones, cordless phones, wireless communication equipment, portable games, cameras, video recorders, portable audio-video equipment and personal digital assistants.

Figure 1. AS1367 - Typical Application Diagram



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin descriptions

Pin Name	Pin Number	Description
OUT	1	**Regulated Output Voltage**. The current flowing out of this pin is equivalent to a DC load current. Fixed 1.2V, 1.5V, 1.8V, 3.0V, 3.3V and 4.5V output, as well as versions from 1.2V up to 5.0V can be ordered. Bypass this pin with 3.3µF to GND.
BYP	2	**Bypass.** This pin should be connected via a 10nF capacitor to pin OUT.
SET	3	**Set Input.** Connect to GND for preset output. Connect to a resistive voltage-divider between OUT and GND to set the output voltage between 1.2V and 5.0V. Changeover threshold is 100mV on SET pin. Above this value, the SET pin becomes the feedback connection point for the external voltage setting resistor network. Feedback reference is 1V.
EN	4	**Active-High Enable Input.** A logic low reduces the supply current to <1µA. Connect this pin to pin IN for normal operation.
GND	5	**Ground.** This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.
POK	6	**Power-OK Output.** Active-low, open-drain output indicates an out-of-regulation condition. Connect a 100kΩ pull-up resistor to pin OUT for logic levels. Leave this pin unconnected if the Power-OK feature is not used.
IN	7, 8	**Input Voltage**. These pins should be connected to the positive terminal of the input capacitor. Bypass this pin with 1µF to **GND**. Input voltage can range from 2.0V to 5.5V.
GND	Exposed Pad	**Exposed Pad.** This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation. Internally it is connected GND.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Typ	Units	Comments
Electrical Parameters					
IN, POK to GND	-0.3	+7		V	
OUT to GND	-0.3	V_{IN} + 0.3		V	
BYP to GND	-0.3	V_{OUT} + 0.3		V	
Output Short-Circuit Duration	Indefinite			V	
Continuous Power Dissipation					
Continuous Power Dissipation		300		mW	Derate 7.1mW/ºC above +70ºC
Temperature Ranges and Storage Conditions					
Operating Temperature Range	-40	+85		ºC	
Junction Temperature T_J		+125		ºC	Internally limited
Thermal Resistance Θ_{JA}		+140		ºC/W	Junction-to-ambient thermal resistance is very dependent on application and board-layout. In situations where high maximum power dissipation exists, special attention must be paid to thermal dissipation during board design.
Storage Temperature Range	-65	+150		ºC	
Package Body Temperature		+260		ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"*

6 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

V_{IN} = $V_{OUT(NOM)}$ + 0.5V or V_{IN} = 2V (whichever is greater), EN = IN, C_{IN} = 1µF, C_{OUT} = 3.3µF, C_{BYP} = 10nF, T_{AMB} = -40°C to +85ºC (unless otherwise specified). Typical values are at T_{AMB} = +25ºC.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage		2.0		5.5	V
V_{OUT}	Output Voltage	Trimmable in 50mV steps	1.2		5.0	V
ΔV_{OUT}	Output Voltage Accuracy	T_{AMB} = +25ºC, I_{OUT} = 1mA, V_{OUT} > 2V	-1		1	%
		I_{OUT} = 100µA to 150mA, V_{OUT} > 2V	-2.5		2.5	
		T_{AMB} = +25ºC, I_{OUT} = 1mA, V_{OUT} ≤ 2V	-20		20	mV
		I_{OUT} = 100µA to 150mA, V_{OUT} ≤ 2V	-50		50	
I_{OUT}	Maximum Output Current		150			mA
I_{LIM}	Current Limit	V_{OUT} forced to GND		180		mA
I_Q	Quiescent Current	I_{OUT} = 0mA		10	16	µA
		I_{OUT} = 100µA		10	20	
		I_{OUT} = 150mA		15	30	
V_{IN} -V_{OUT}	Dropout Voltage [1]	3.0V < V_{OUT}, I_{OUT} = 150mA		110	200	mV
ΔV_{LNR}	Line Regulation	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 5.5V, I_{OUT} = 1mA		0.02	0.06 [2]	% / V
ΔV_{LDR}	Load Regulation	I_{OUT} = 100µA to 150mA		0.001	0.01	% / mA
	Dynamic Line Transient	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 5.5V within 10µs, I_{OUT} = 1mA		17		mV
	Dynamic Load Transient	I_{OUT} = 1mA to 150mA within 10µs		12	50	mV
	Output Noise Voltage	I_{OUT} = 10mA, f = 100Hz to 100kHz		15		µV_{RMS}
PSRR	Output Voltage Power-Supply Rejection Ratio	I_{OUT} = 10mA, f = 1kHz		75		dB
		I_{OUT} = 10mA, f = 10kHz		60		
		I_{OUT} = 10mA, f = 100kHz		52		
Shutdown [3]						
t_{ON}	EN Exit Delay [4]	I_{OUT} = 0mA			500	µs
I_{OFF}	Shutdown Supply Current	EN = 0V		0.1	1	µA
V_{IH}	Enable Input Threshold		1.4			V
V_{IL}					0.4	
R_{SHDN}	Auto-discharge Resistance	EN = 0V, I_{OUT} = 0mA		740		Ω
Power-OK Output						
V_{POK}	Power-OK Voltage Threshold	I_{OUT} = 0mA, $V_{OUTRISING}$	90	94	97.5	% V_{OUT}
		I_{OUT} = 0mA, $V_{OUTFALLING}$		3		
V_{OL}	POK Output Low Voltage	POK sinking 1mA, EN = 0V			0.3	V
I_{POK}	POK Leakage Current	V_{OUT} in regulation		1	100	nA
SET						
V_{SET}	SET Threshold Voltage	V_{OUT} to V_{IN}	50	100	150	mV
I_{SET}	Set Input Bias Current	SET = 0V	-100		100	nA
V_{REF}	Feedback Reference Point	V_{SET} > 150mV	0.08	1	1.02	V
Output Capacitor						
C_{OUT}	Output Capacitor	Load Capacitor Range	3.3	10		µF
		Load Capacitor ESR			200	mΩ

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Thermal Protection						
T_{SHDN}	Thermal Shutdown Temperature			160		ºC
ΔT_{SHDN}	Thermal Shutdown Hysteresis			20		ºC

1. Dropout voltage = V_{IN} - V_{OUT} when V_{OUT} is 100mV < V_{OUT} for V_{IN} = $V_{OUT(NOM)}$ + 0.5V (applies only to nominal output voltages ≥ 2.5V).
2. Guaranteed by design.
3. The rise and fall time of the shutdown signal must not exceed 1ms.
4. The delay time is defined as time required to set V_{OUT} to 95% of its final nominal value.

7 Typical Operating Characteristics

V_{OUT} = 3.3V, I_{OUT} = 10mA, T_{AMB} = +25°C (unless otherwise specified)

Figure 3. Output Voltage vs. Output Current

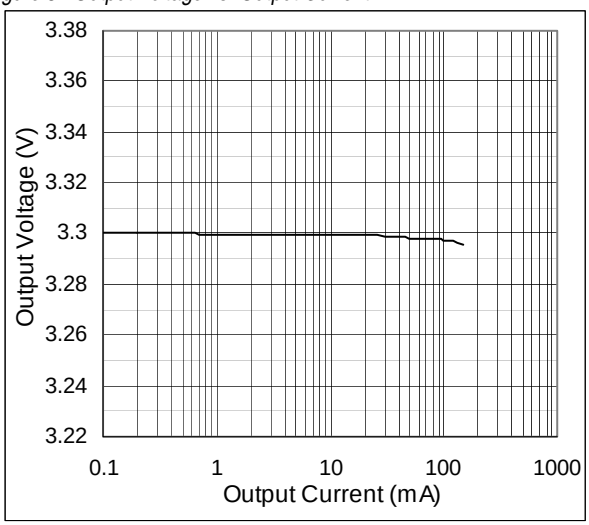


Figure 4. Output Voltage vs. Input Voltage

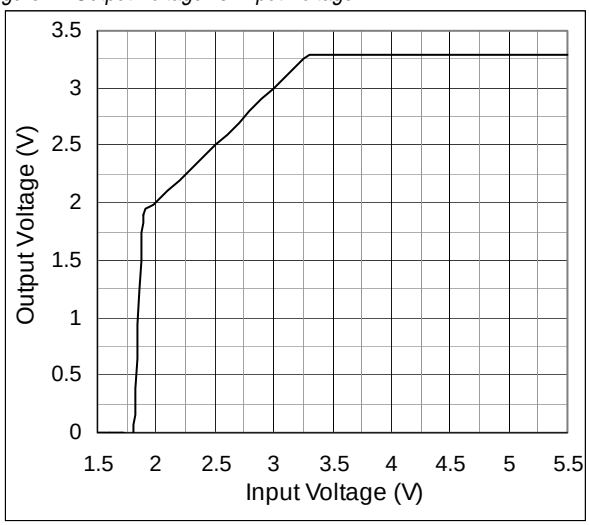


Figure 5. Output Voltage vs. Temperature

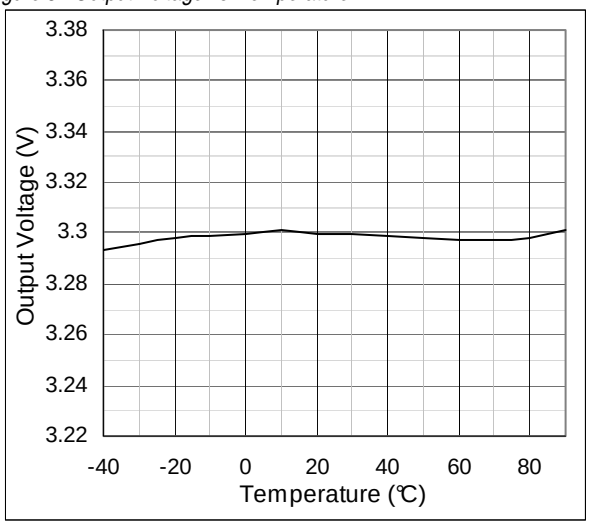


Figure 6. No Load Battery Current vs. Input Voltage

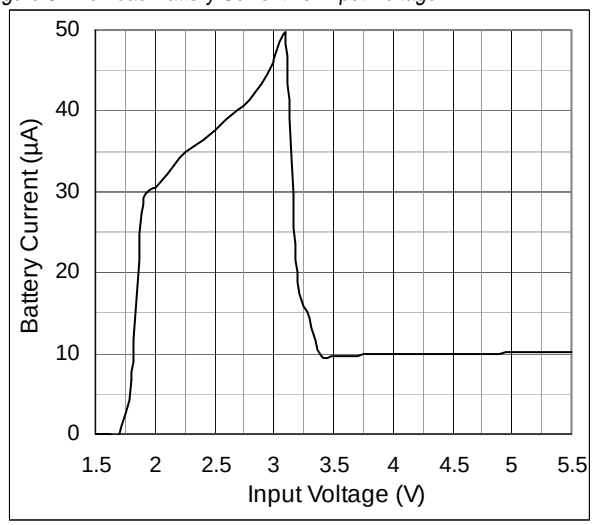


Figure 7. Quiescent Current vs. Output Current

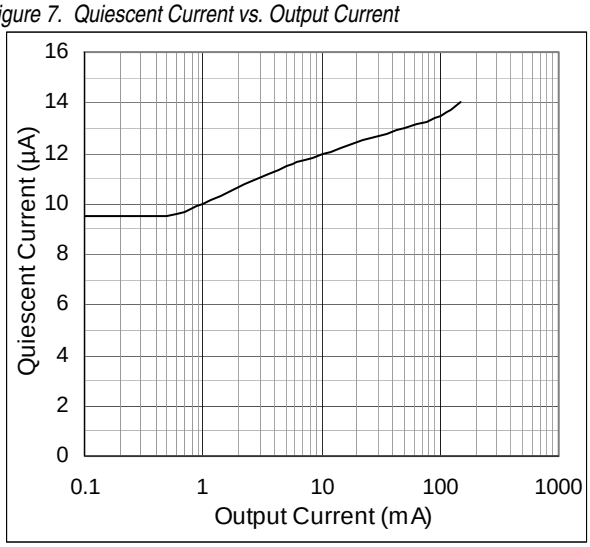


Figure 8. Quiescent Current vs. Input Voltage

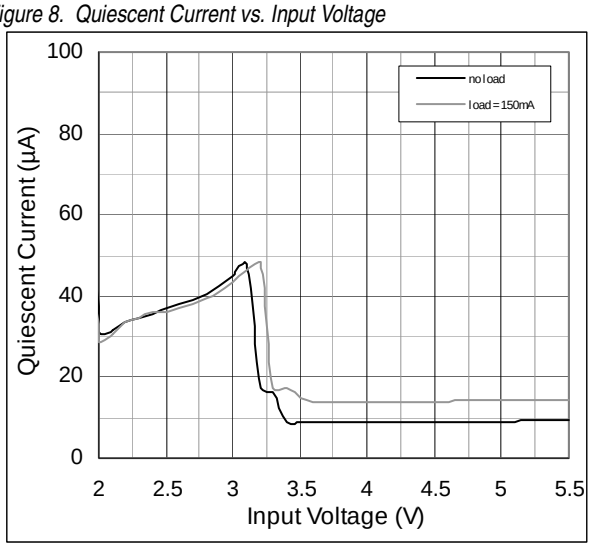


Figure 9. PSRR vs. Frequency

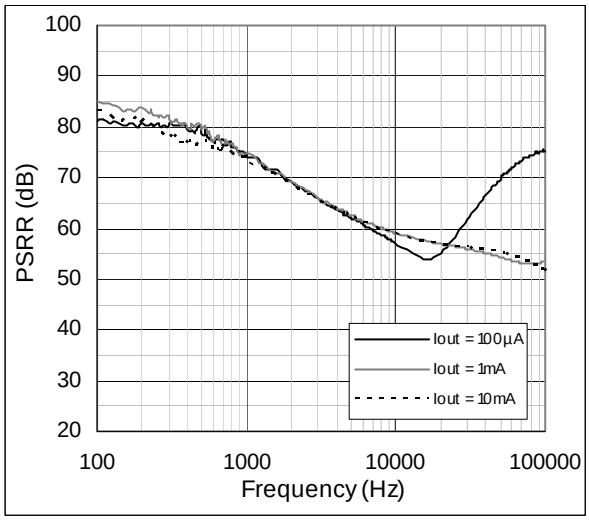


Figure 10. Startup; VIN = 3.8V, IOUT = 100mA

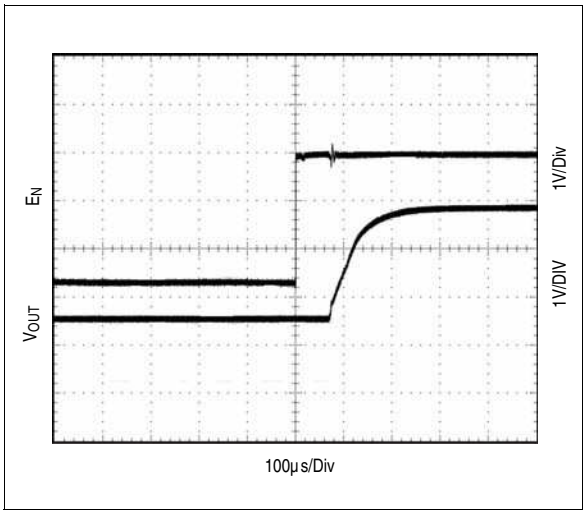


Figure 11. Startup; VIN = 3.8V, IOUT = 100mA

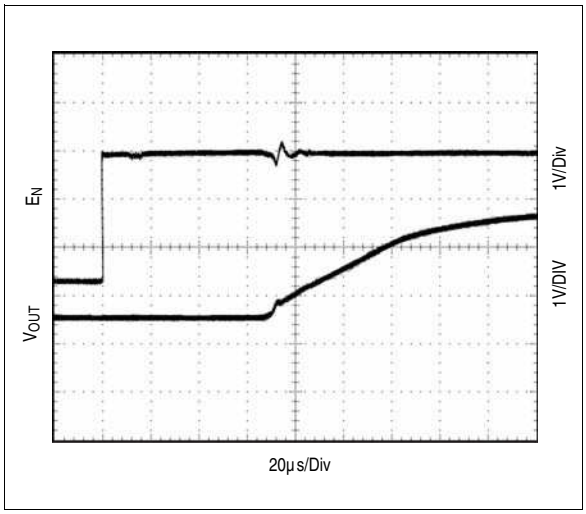


Figure 12. Line Transient Response; VIN = 3.8V to 4.1V, IOUT = 100mA

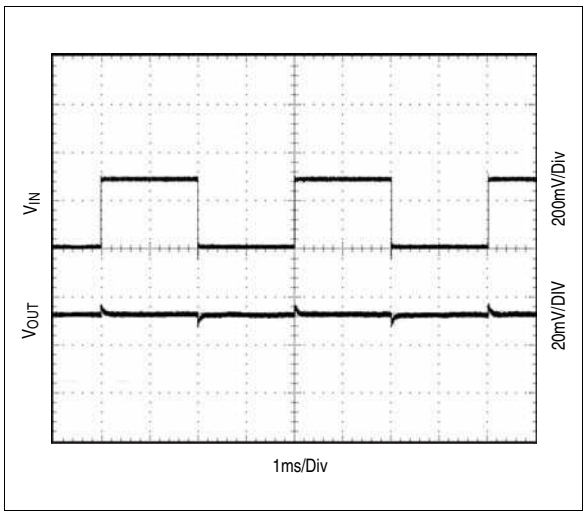


Figure 13. Line Transient Response; VIN = 3.8V to 4.1V, IOUT = 100mA

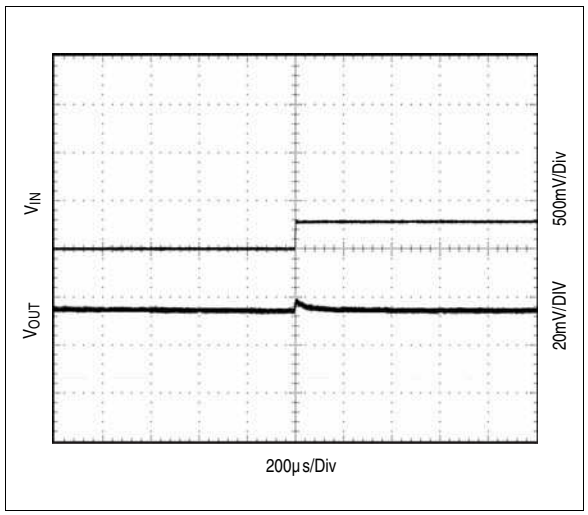


Figure 14. Load Transient Response; VIN = 3.8V, IOUT = 1mA to 100mA

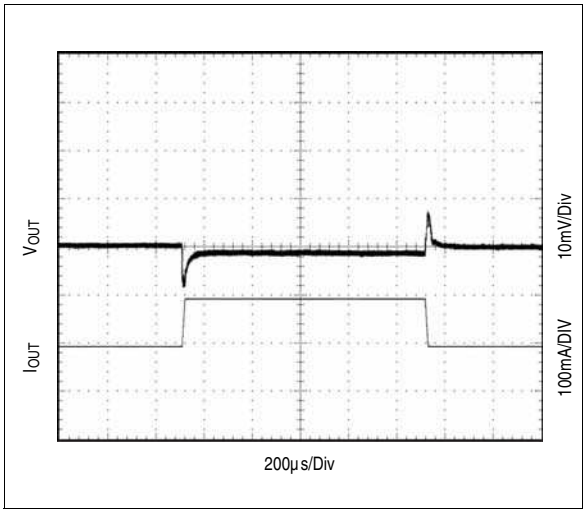
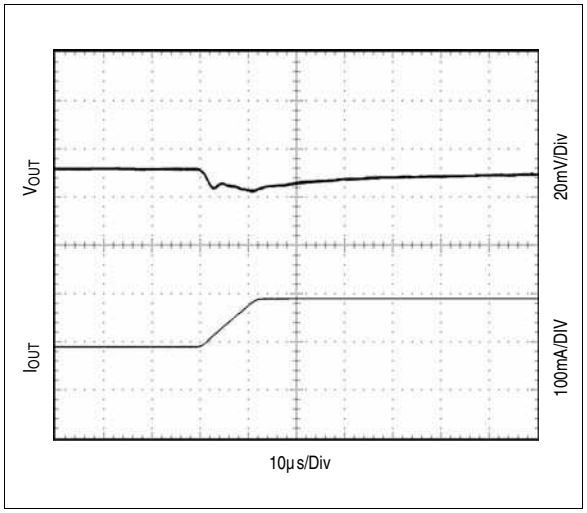


Figure 15. Load Transient Response; VIN = 3.8V, IOUT = 1mA to 100mA



8 Detailed Description

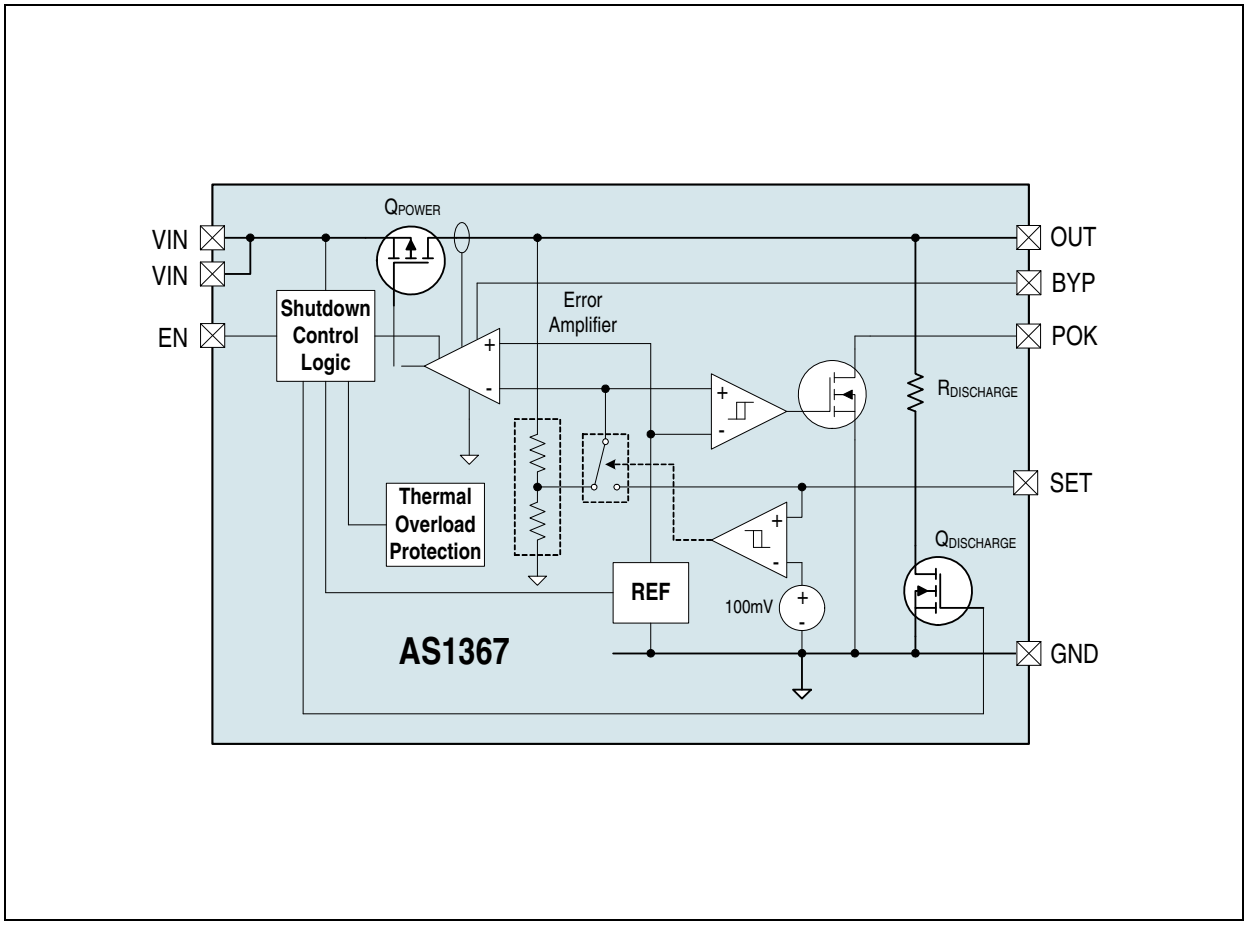
Figure 16 shows the block diagram of the AS1367. It identifies the basics of a series linear regulator employing a P-Channel MOSFET as the control element. A stable voltage reference (REF in Figure 16) is compared with an attenuated sample of the output voltage. Any difference between the two voltages (reference and sample) creates an output from the error amplifier that drives the series control element to reduce the difference to a minimum. The error amplifier incorporates additional buffering to drive the relatively large gate capacitance of the series pass P-channel MOSFET, when additional drive current is required under transient conditions. Input supply variations are absorbed by the series element, and output voltage variations with loading are absorbed by the low output impedance of the regulator.

The AS1367 is low-dropout, low-quiescent-current linear regulator intended for LDO regulator applications where output current load requirements range from no load to 150mA. All devices come standard with adjustable output voltages of 1.2V to 5.0V and fixed output voltages.

An additional feature of the AS1367 adapts the bias current of the control loop to the load current. At low load currents the control loop bias current is small. As the load current increases, the bias current tracks the increase in order to improve the regulator transient performance. Efficiency is improved at low load currents because of this feature.

All devices are able to override the internally trimmed output voltage by using the SET pin. Connecting an external voltage divider to this pin converts the part from fixed to an adjustable version. The SET voltage threshold above which the changeover occurs is 100mV. For fixed output variants, see Ordering Information on page 18.

Figure 16. AS1367 Block Diagram



8.1 Output Voltages

Standard products are factory-set with output voltages from 1.2V to 5.0V. A two-digit suffix of the part number identifies the nominal output (see Ordering Information on page 18). Non-standard devices are available.

For more information contact: http://www.austriamicrosystems.com/contact

9 Application Information

9.1 Dropout Voltage

Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different currents and, in particular at the regulator maximum one. From this is obtained the MOSFET maximum series resistance over temperature etc. More generally:

$$V_{DROPOUT} = I_{LOAD} \times R_{SERIES} \quad \text{(EQ 1)}$$

Dropout is probably the most important specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful “end of life” of the battery before replacement or re-charge is required.

Figure 17. Graphical Representation of Dropout Voltage

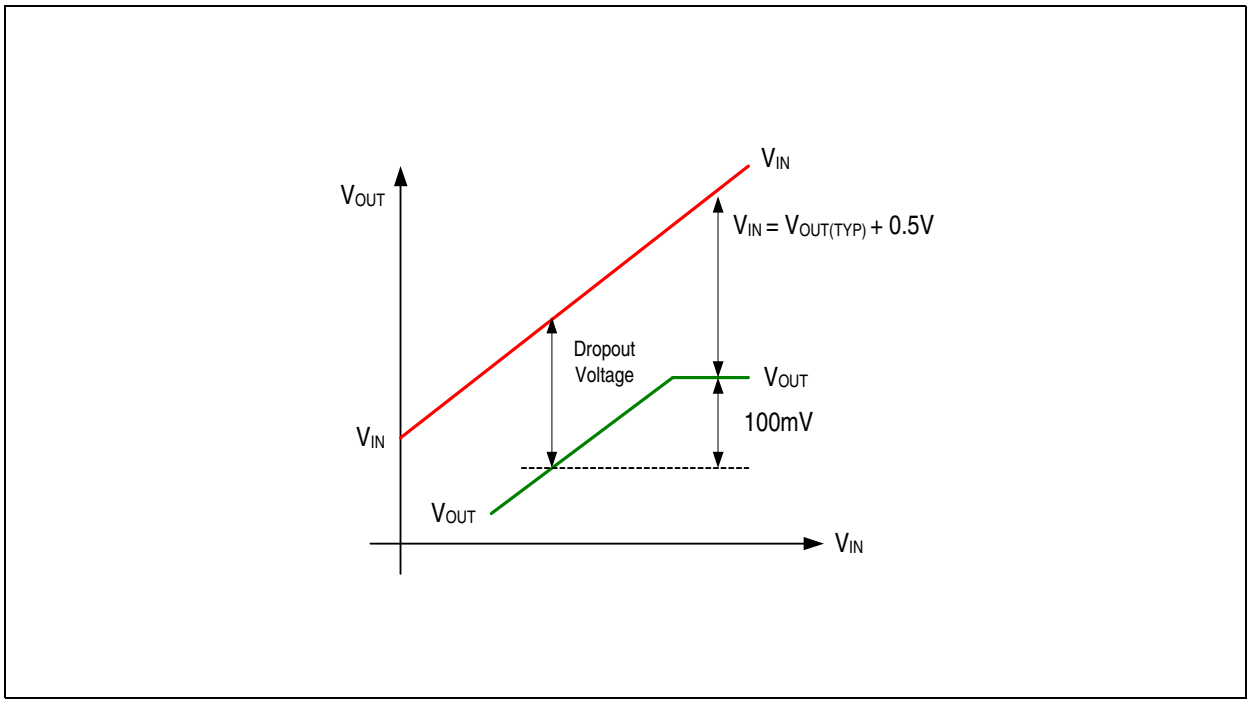


Figure 17 shows the variation of VOUT as VIN is varied for a certain load current. The practical value of dropout is the differential voltage (VOUT-VIN) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.

9.2 Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage. Efficiency is given by:

$$\textit{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{V_{IN}(I_Q + I_{LOAD})} \times 100\ \% \quad \text{(EQ 2)}$$

Where:
I_Q = Quiescent current of LDO

9.3 Power Dissipation

Maximum power dissipation (PD) of the LDO is the sum of the power dissipated by the internal series MOSFET and the quiescent current required to bias the internal voltage reference and the internal error amplifier, and is calculated as:

$$PD_{(MAX)}(Seriespass) = I_{LOAD(MAX)}(V_{IN(MAX)} - V_{OUT(MIN)}) \ \ Watts \qquad (EQ\ 3)$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$PD_{(MAX)}(Bias) = V_{IN(MAX)}I_Q \ \ Watts \qquad (EQ\ 4)$$

Total LDO power dissipation is calculated as:

$$PD_{(MAX)}(Total) = PD_{(MAX)}(Seriespass) + PD_{(MAX)}(Bias) \ \ Watts \qquad (EQ\ 5)$$

9.4 Junction Temperature

Under all operating conditions, the maximum junction temperature should not be allowed to exceed 125ºC (unless the data sheet specifically allows). Limiting the maximum junction temperature requires knowledge of the heat path from junction to case (θ_{JC}ºC/W fixed by the IC manufacturer), and adjustment of the case to ambient heat path (θ_{CA}ºC/W) by manipulation of the PCB copper area adjacent to the IC position.

Figure 18. Package Physical Arrangements

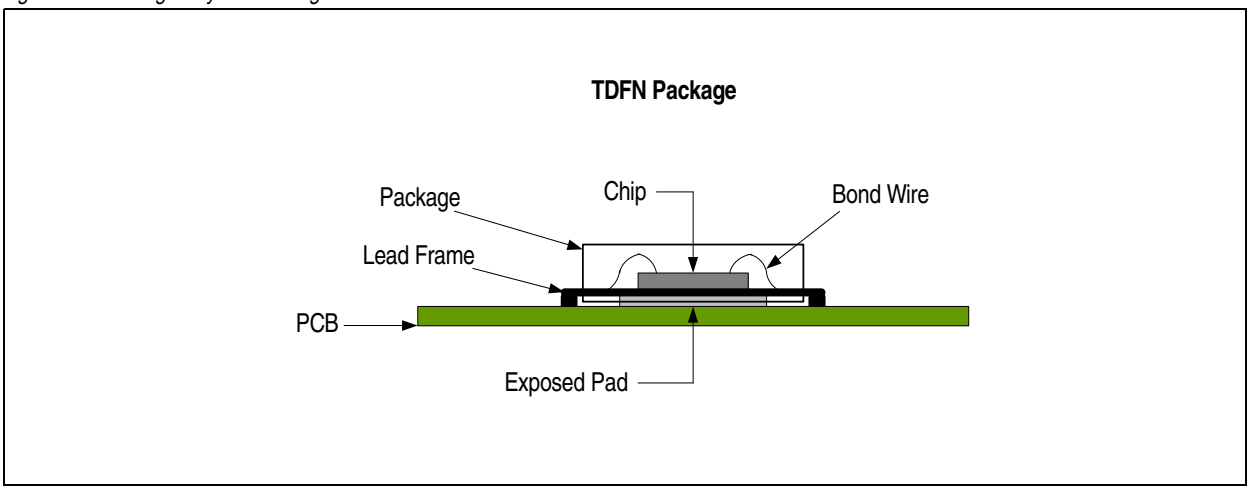
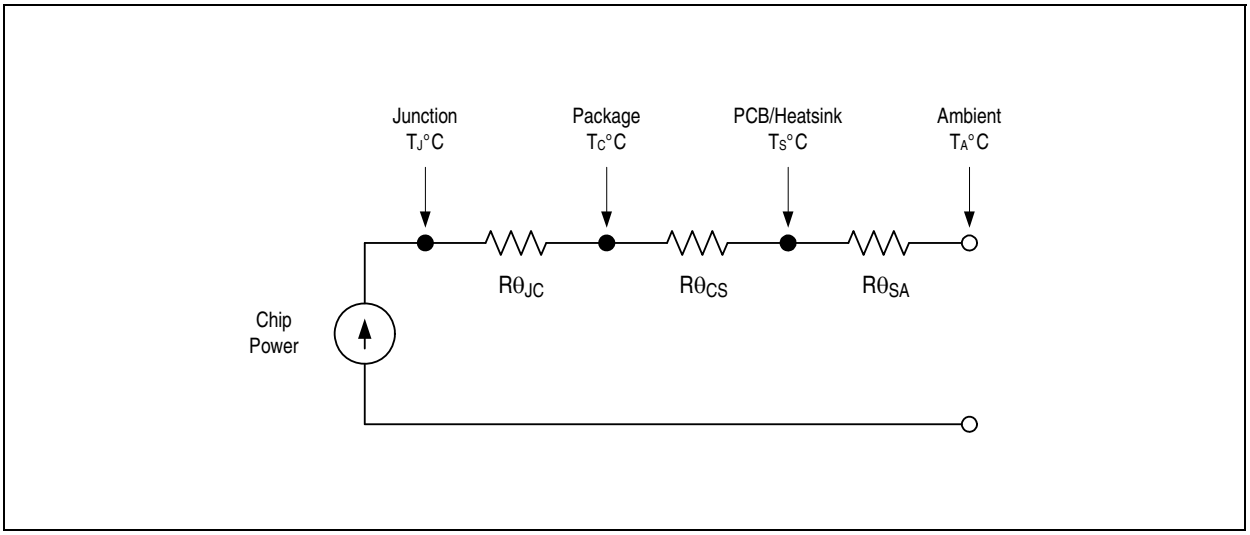


Figure 19. Steady State Heat Flow Equivalent Circuit



Total Thermal Path Resistance:

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CS} + R\theta_{SA} \quad \textit{(EQ 6)}$$

Junction Temperature (T_JºC) is determined by:

$$T_J = (PD_{(MAX)} \times R\theta_{JA}) + T_{AMB} \ ºC \quad \textit{(EQ 7)}$$

9.5 Explanation of Steady State Specifications

9.5.1 Line Regulation

Line regulation is defined as the change in output voltage when the input (or line) voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. Line regulation is a measure of the DC open loop gain of the error amplifier. More generally:

Line Regulation = $\frac{\Delta V_{OUT}}{\Delta V_{IN}}$ and is a pure number

In practise, line regulation is referred to the regulator output voltage in terms of % / VOUT. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\textit{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}} \ \textit{\% / V} \quad \textit{(EQ 8)}$$

9.5.2 Load Regulation

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator. More generally:

$$\textit{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \ \textit{and is units of ohms (}\Omega\textit{)} \quad \textit{(EQ 9)}$$

In practise, load regulation is referred to the regulator output voltage in terms of % / mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\textit{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \times \frac{100}{\Delta V_{OUT}} \ \textit{\% / mA} \quad \textit{(EQ 10)}$$

9.5.3 Setting Accuracy

Accuracy of the final output voltage is determined by the accuracy of the ratio of R1 and R2, the reference accuracy and the input offset voltage of the error amplifier. When the regulator is supplied pre-trimmed, the output voltage accuracy is fully defined in the output voltage specification.

When the regulator has a SET terminal, the output voltage may be adjusted externally. In this case, the tolerance of the external resistor network must be incorporated into the final accuracy calculation. Generally:

$$V_{OUT} = (V_{SET} \pm \Delta V_{SET})\left(1 + \frac{R1 \pm \Delta R1}{R2 \pm \Delta R2}\right) \quad \textit{(EQ 11)}$$

The reference tolerance is given both at 25ºC and over the full operating temperature range.
For AS1367, the reference point for VSET is 1V ±2%.

9.5.4 Total Accuracy

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation. Generally:

Total % Accuracy = Setting % Accuracy + Load Regulation % + Line Regulation % *(EQ 12)*

9.6 Explanation of Dynamic Specifications

9.6.1 Power Supply Rejection Ratio (PSRR)

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR is a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low quiescent current conditions. Generally:

$$PSSR = 20Log\frac{\delta V_{OUT}}{\delta V_{IN}}\ dB \text{ using lower case } \delta \text{ to indicate AC values} \qquad (EQ\ 13)$$

Power supply rejection ratio is fixed by the internal design of the regulator. Additional rejection must be provided externally.

9.6.2 Output Capacitor ESR

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a limit statement in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations with temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below T_{AMB} = -10ºC. With X7R or X5R capacitors, a 4.7µF capacitor should be sufficient at all operating temperatures.

Larger output capacitor values (10µF max) help to reduce noise and improve load transient-response, stability and power-supply rejection.

9.6.3 Input Capacitor

An input capacitor at V_{IN} is required for stability. It is recommended that a 4.7µF capacitor be connected between the AS1364 power supply input pin V_{IN} and ground (capacitance value may be increased without limit subject to ESR limits). This capacitor must be located at a distance of not more than 1cm from the V_{IN} pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

9.6.4 Noise

The regulator output is a DC voltage with noise superimposed on the output. The noise comes from three sources; the reference, the error amplifier input stage, and the output voltage setting resistors. Noise is a random fluctuation and if not minimized in some applications, will produce system problems. Additional noise reduction is possible with the AS1367 by connecting a 10nF capacitor between the BYP and the OUT pins.

9.6.5 Transient Response

The series regulator is a negative feedback system, and therefore any change at the output will take a finite time to be corrected by the error loop. This “propagation time” is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance, and during this time, ESR is the dominant mechanism causing voltage transients at the output. More generally:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times R_{ESR} \quad \text{Units are Volts, Amps, Ohms.} \qquad (EQ\ 14)$$

Thus an initial +50mA change of output current will produce a -12mV transient when the ESR=240mΩ. Remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage droop during the time that the LDO feedback loop takes to respond to the output change. This drift is approx. linear in time and sums with the ESR contribution to make a total transient variation at the output of:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times \left(R_{ESR} + \frac{T}{C_{LOAD}}\right) \quad \text{Units are Volts, Seconds, Farads, Ohms.} \qquad (EQ\ 15)$$

Where:
C_{LOAD} is output capacitor
T = Propagation delay of the LDO

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for t < “propagation time”, so that a faster LDO needs a smaller cap at the load to achieve a similar transient response. For instance 50mA load current step produces 50mV output drop if the LDO response is 1µsec and the load cap is 1µF.

There is also a steady state error caused by the finite output impedance of the regulator. This is derived from the load regulation specification discussed above.

9.6.6 Turn On Time

This specification defines the time taken for the LDO to awake from shutdown. The time is measured from the release of the enable pin to the time that the output voltage is within 5% of the final value. It assumes that the voltage at VIN is stable and within the regulator Min and Max limits. Shutdown reduces the quiescent current to very low, mostly leakage values (<1µA).

9.6.7 Thermal Protection

To prevent operation under extreme fault conditions, such as a permanent short circuit at the output, thermal protection is built into the device. Die temperature is measured, and when a 160ºC (AS1367) threshold is reached, the device enters shutdown. When the die cools sufficiently, the device will restart (assuming input voltage exists and the device is enabled). Hysteresis of 20ºC prevents low frequency oscillation between start-up and shutdown around the temperature threshold.

9.6.8 Auto-Discharge

When the AS1367 is placed in shutdown, a 740Ω path to ground is connected at the output. This path speeds up the discharge of the capacitor(s) connected to the regulator output. Assuming that VIN remains constant and always >VOUT, output discharge time is calculated from the following relationship:

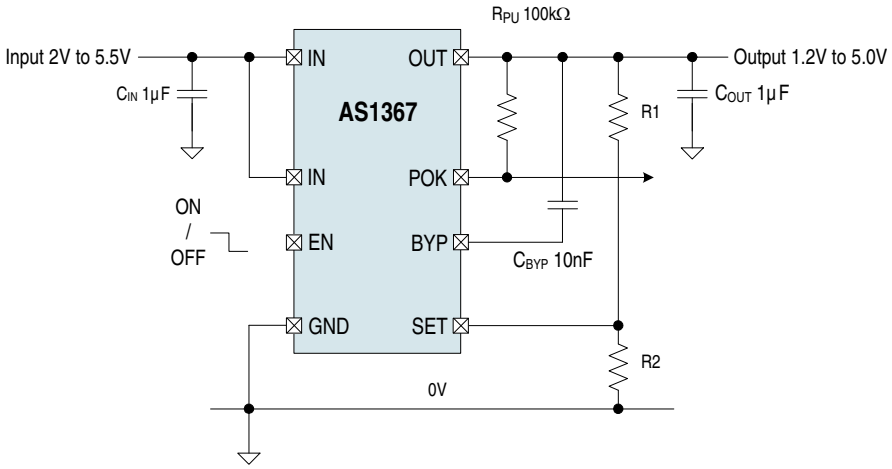
$$V(t) = V_{REG} e^{-\frac{t}{RC}} \quad \textit{(EQ 16)}$$

Where:
t = specified time after regulator shutdown (sec)
VREG = Regulated output voltage (initial condition)
R = 740Ω (typ) discharge resistance
C = Output capacitance (Farad)

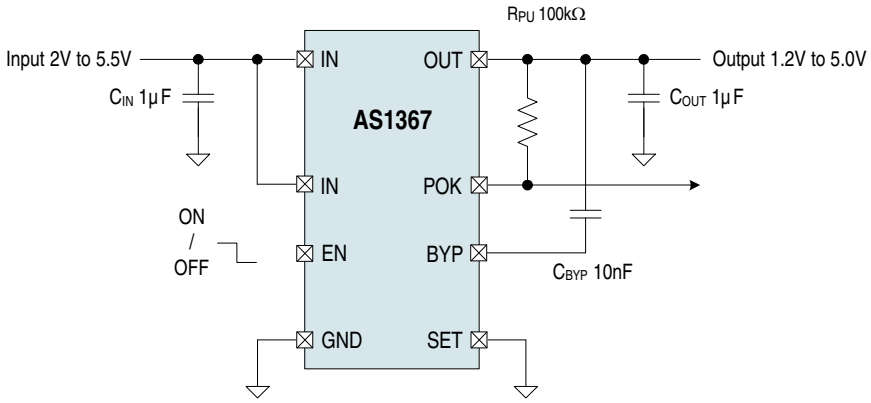
In other words, the output discharge will reach 90% below the regulated output voltage in 2.2RC seconds; R and C defined as above.

Figure 20. Applications Diagram

External Voltage Level Detection (Input Monitoring)



Internal Voltage Level Detection (Output Monitoring)



10 Package Drawings and Markings

The device is available in a 8-pin TDFN package.

Figure 21. 8-pin TDFN 2x2 Package Diagram

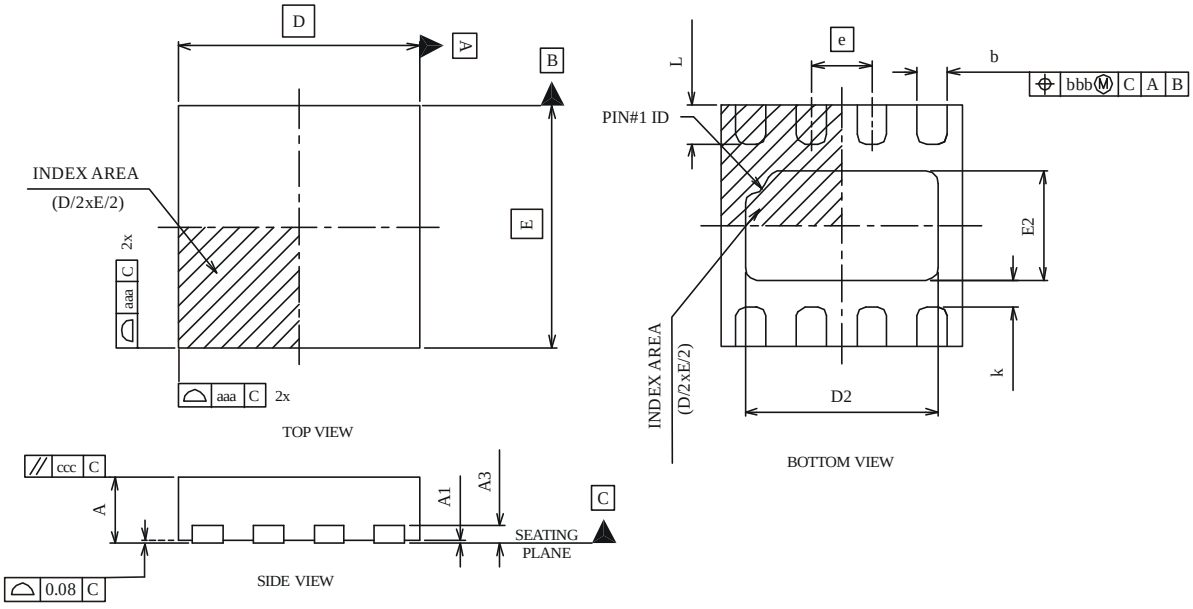


Table 4. 8-pin TDFN 2x2 package Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.51	0.55	0.60	D BSC		2.00	
A1	0.00	0.02	0.05	E BSC		2.00	
A3		0.15 REF		D2	1.45	1.60	1.70
b	0.18	0.25	0.30	E2	0.75	0.90	1.00
e		0.50		L	0.225	0.325	0.425
aaa		0.15		k	0.20		
bbb		0.10		ND		4	
ccc		0.10		N		8	

Note:

1. Figure 21 is shown for illustration only.
2. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
3. All dimensions are in millimeters, angle is in degrees (°).
4. N is the total number of terminals.
5. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
6. ND and NE refer to the number of terminals on each D and E side respectively.
7. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension B should not be measured in that radius area.
8. Coplanarity applies to the terminals and all other bottom surface metallization.

Revision History

Revision	Date	Owner	Description
1.2		afe	Initial revision
1.3	30 Nov, 2011		Changes made across document for version 1.3
1.4	12 Dec, 2011		Updated equations in Power Dissipation section

Note: Typos may not be explicitly mentioned under revision history.

11 Ordering Information

The device is available as the standard products listed in Table 5.

Table 5. Ordering Information

Ordering Code	Marking	Output	Description	Delivery Form	Package
AS1367-BTDT-12	AB	1.2V	150mA, Adaptive LDO	Tape and Reel	8-pin TDFN 2x2
AS1367-BTDT-18	AC	1.8V	150mA, Adaptive LDO	Tape and Reel	8-pin TDFN 2x2
AS1367-BTDT-30	AD	3.0V	150mA, Adaptive LDO	Tape and Reel	8-pin TDFN 2x2
AS1367-BTDT-33	AE	3.3V	150mA, Adaptive LDO	Tape and Reel	8-pin TDFN 2x2
AS1367-BTDT-45	AF	4.5V	150mA, Adaptive LDO	Tape and Reel	8-pin TDFN 2x2

Non-standard devices from 1.2V to 5.0V are available in 50mV steps.
For more information and inquiries contact http://www.austriamicrosystems.com/contact

Note: All products are RoHS compliant.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

Technical Support is available at http://www.austriamicrosystems.com/Technical-Support

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