AS13986

Dual Low-Noise, Low-Dropout Voltage Regulator

1 General Description

The AS13986 dual low-dropout regulator provides up to 150mA at each output using a 2.5 to 5.5V input voltage. The ultra-low drop-out voltage, low quiescent current, and low noise make the AS13986 perfect for low-power, battery-operated applications.

Regulator ground current increases only slightly in drop-out, extending the battery life in low-power applications.

The device features excellent power supply rejection (55dB @ 1kHz and 50dB at 10kHz). The high power supply rejection is maintained down to low input voltage levels used in battery operated devices.

Integrated shutdown logic control function is available for each output. In cases where the device is used as a local regulator it is possible to switch some of the circuitry into standby mode, thus decreasing total power consumption.

The AS13986 was specifically designed to work with low-ESR ceramic capacitors.

The AS13986 is available in a 8-pin WLP package.

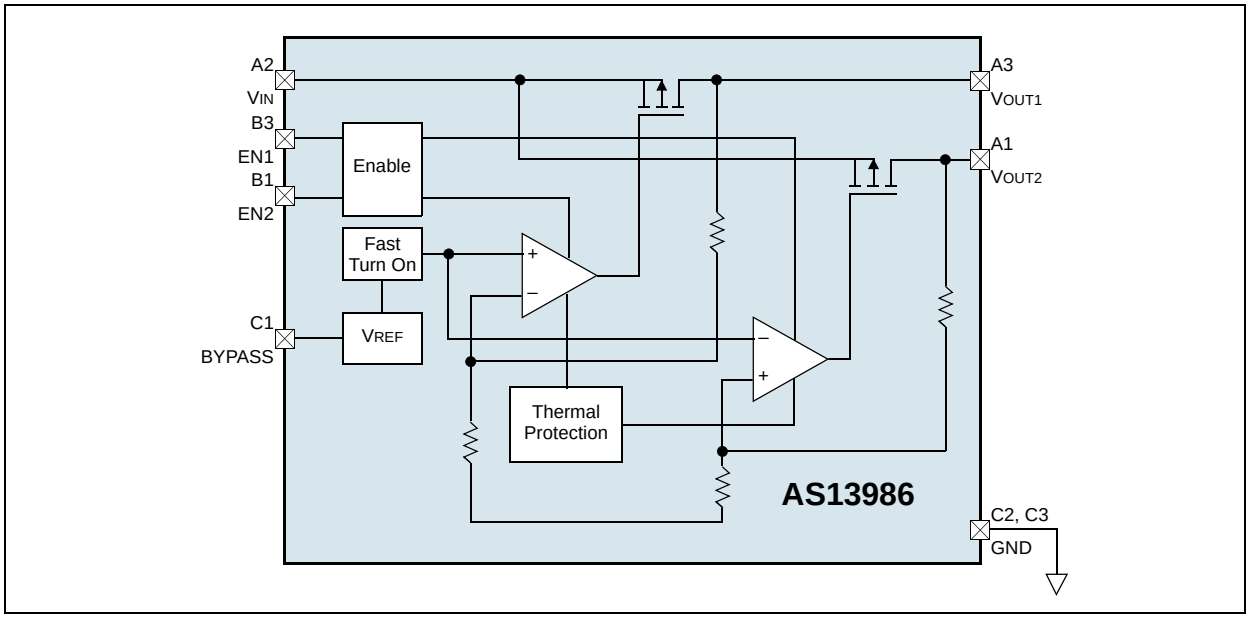
2 Key Features

- Input Voltage: 2.5 to 5.5V
- Dual Output Voltages: 1.2 to 5.0V (in 50mV Steps)
- Ultra-Low Dropout Voltage: 45mV @ 150mA Load, 0.3mV @ 1mA Load
- Very Low Quiescent Current: 135µA @ No Load, 255µA @ 150mA Load, 2µA In Off Mode
- Guaranteed Output Current up to 150mA
- Fast Turn-On Time: 160µs (C_{OUT} = 1µF, C_{BYPASS} = 10nF, I_{OUT} = 1mA)
- Logic-Controlled Shutdown
- Up to 1.5% Output Voltage Accuracy
- Integrated Current-Limit and Thermal Overload Protection
- Output Low-Noise Voltage: 30µV_{RMS} (10Hz to 100kHz)
- Supply Voltage Rejection.: 55dB @ 1kHz, 50dB @ 10kHz
- Stable With Low-ESR Ceramic Capacitors
- Temperature Range: -40 to 125ºC
- 8-pin WLP Package

3 Applications

The device is ideal for powering cordless and mobile phones, MP3 players, CD and DVD players, PDAs, handheld computers, digital cameras and any other hand-held battery-powered device.

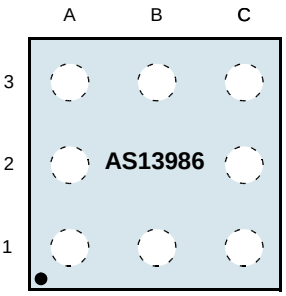
Figure 1. AS13986 - Block Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
A1	V_{OUT2}	**Regulated Output Voltage 2**
B1	EN2	**Output Voltage 2 Enable/Disable** $V_{EN} \leq 0.4V$: V_{OUT2} is disabled. $V_{EN} \geq 1.2V$: V_{OUT2} is enabled. **Note:** This pin must not float as it is not internally pulled-up or pulled-down.
C1	BYPASS	**Bypass Pin**. This pin should be connected to an external capacitor (10nF typ) to minimize noise.
C2	GND	**Common Ground**
C3	GND	**Common Ground**
B3	EN1	**Output Voltage 1 Enable/Disable** $V_{EN} \leq 0.4V$: V_{OUT1} is disabled. $V_{EN} \geq 1.2V$: V_{OUT1} is enabled.
A3	V_{OUT1}	**Regulated Output Voltage 1**
A2	V_{IN}	**Input Voltage**

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
DC Input Voltage	-0.3	7	V	
DC Output Voltage	-0.3	V_{IN} + 0.3	V	
ENABLE Input Voltage	-0.3	V_{IN} + 0.3	V	
Output Current	Internally limited			
Power Dissipation	Internally limited			
Storage Temperature Range	-65	+150	ºC	
Operating Junction Temperature Range	-40	+125	ºC	
Thermal Resistance Junction Ambient Temperature		+120	ºC/W	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

T_{AMB} = 25ºC, V_{IN} = $V_{OUT(NOM)}$ +0.5V, C_{OUT} = C_{IN} = 1µF, C_{BYPASS} = 10nF, I_{OUT} = 1mA, V_{EN} = 1.2V (unless otherwise specified)

Note: Exposing the WLP package to direct light could cause device malfunction.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage		2.5		5.5	V
ΔV_{OUT}	Output Voltage Tolerance $V_{OUT} \geq 3V$	I_{OUT} = 1mA	-1.5		1.5	% of $V_{OUT(NOM)}$
		T_{AMB} = -40 to 125ºC	-2.5		2.5	
	Output Voltage Tolerance $V_{OUT} < 3V$	I_{OUT} = 1mA	-75		75	mV
		T_{AMB} = -40 to 125ºC	-100		100	
	Line Regulation [1]	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 4.5V, $V_{OUT} < 3V$	-0.2		0.2	%/V
		V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 5.5V, $V_{OUT} < 3V$	-0.35		0.35	
	Load Regulation [1]	I_{OUT} = 1 to 150mA		0.003	0.008	%/mA
	Output AC Line Regulation (Figure 3)	V_{IN} = $V_{OUT(NOM)}$ + 1V, I_{OUT} = 150mA, t_R = t_F = 30µs		1		mVpp
IQ	Quiescent Current	Both Outputs Enabled, V_{EN} = 1.4V, I_{OUT} = 0mA		135		µA
		Both Outputs Enabled, V_{EN} = 1.4V, I_{OUT} = 0mA,T_{AMB} = -40 to 125ºC			200	
		Both Outputs Enabled, V_{EN} = 1.4V, I_{OUT} = 0 to 150mA		255		
		Both Outputs Enabled, V_{EN} = 1.4V, I_{OUT} = 0mA to 150mA, T_{AMB} = -40 to 125ºC			370 [2]	
		Both Outputs Disabled, V_{EN} = 0.4V		0.001 [2]		
		Both Outputs Disabled, V_{EN} = 0.4V, T_{AMB} = -40 to 125ºC			4	
		One Output Enabled, I_{OUT} = 0mA		90		
		One Output Enabled, V_{EN} = 1.4V, I_{OUT} = 0mA, T_{AMB} = -40 to 125ºC			130	
		One Output Enabled, V_{EN} = 1.4V, I_{OUT} = 0 to 150mA		100		
		One Output Enabled, V_{EN} = 1.4V, I_{OUT} = 0 to 150mA, T_{AMB} = -40 to 125ºC			220 [2]	
V_{LOAD}	Dropout Voltage [3]	I_{OUT} = 1mA		0.3		mV
		I_{OUT} = 1mA, T_{AMB} = -40 to 125ºC			2 [2]	
		I_{OUT} = 150mA		45		
		I_{OUT} = 150mA, T_{AMB} = -40 to 125ºC			100	
SVR	Supply Voltage Rejection (Figure 4)	V_{IN} = $V_{OUT(NOM)}$ + 0.25V, V_{RIPPLE} = 0.1V, I_{OUT} = 50mA, f = 1kHz		55		dB
		V_{IN} = $V_{OUT(NOM)}$ + 0.25V, V_{RIPPLE} = 0.1V, I_{OUT} = 50mA, f = 10kHz		50		
I_{SC}	Short Circuit Current	R_{LOAD} = 0Ω		500		mA
$I_{OUT(PK)}$	Peak Output Current	$V_{OUT} \geq V_{OUT(NOM)}$ - 5%	300	480		mA

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{EN}	Enable Input Logic Low	V_{IN} = 2.5V to 5.5V, T_{AMB} = -40 to 125ºC [4]			0.4	V
	Enable Input Logic High		1.2			
I_{EN}	Enable Input Current	V_{EN} = 0.4V, V_{IN} = 5.5V		±10 [2]		nA
eN	Output Noise Voltage	BW = 10Hz to 100kHz, C_{OUT} = 1µF, I_{OUT} = 0mA		30		μV_{RMS}
t_{ON}	Turn On Time [5]	C_{BYPASS} = 10nF		160	250	µs
T_{SHDN}	Thermal Shutdown [4, 6]			160		ºC
Recommended Output Capacitor						
C_{OUT}	Output Capacitor	Capacitance	1		22 [2]	µF
		ESR	0.005		5	Ω

1. Temperature variations are included within the output voltage accuracy. The line and load regulation tests will be indirectly tested and covered by the total accuracy test.
2. Guaranteed by Design.
3. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value (does not apply to input voltages below 2.5V).
4. EN*x* must be driven with a $t_R = t_F$ < 10ms.
5. Turn on time is time measured between the enable input just exceeding the V_{INH} high value and the output voltage just reaching 95% of its nominal value. Maximum limit guaranteed by design.
6. Typical thermal protection hysteresis is 20ºC.

Note: All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 3. AC Line Regulation Input Voltage Test Signal

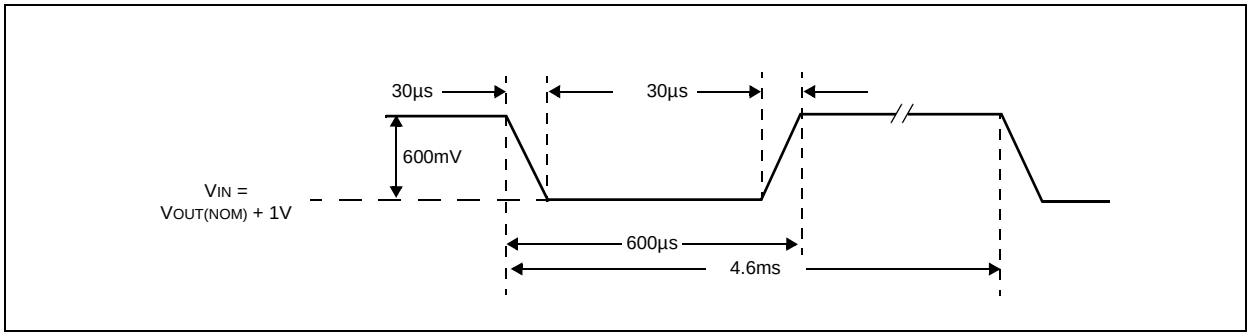
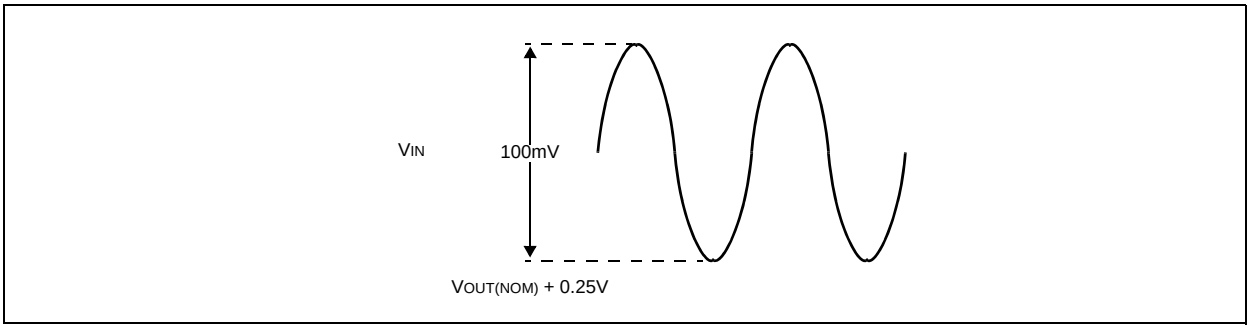


Figure 4. SVR Input Voltage Test Signal



7 Typical Operating Characteristics

TAMB = +25ºC (unless otherwise specified)

Figure 5. Output Voltage vs. Temperature; VIN = 3.3V, VSHDN = 1.4V, IOUT = 0mA

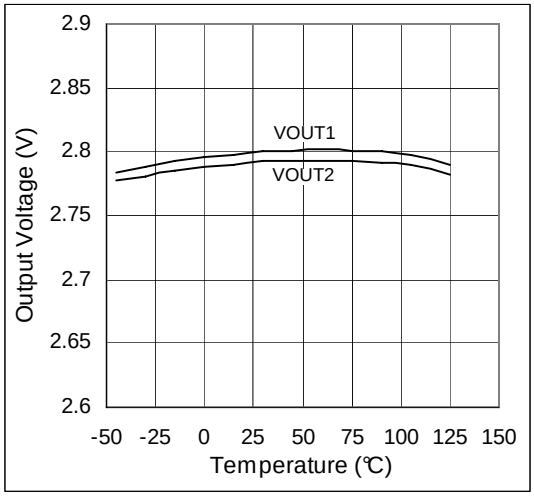


Figure 6. Output Voltage vs. Temperature; VIN = 3.3V, VSHDN = 1.4V, IOUT = 150mA

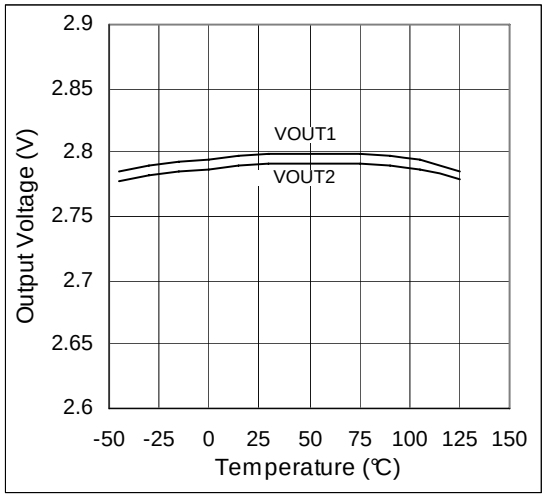


Figure 7. Load Regulation vs. Temperature; VIN = 3.3V, VSHDN = 1.4V, IOUT = 1 to 150mA

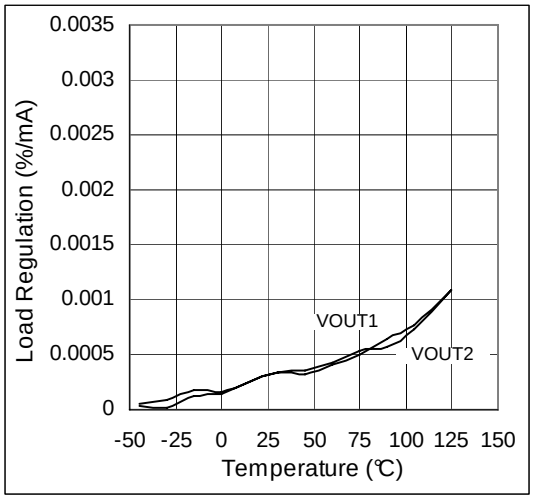


Figure 8. Line Regulation vs. Temperature; VIN = 3.3 to 4.5V, VSHDN =1.4V, IOUT =1mA

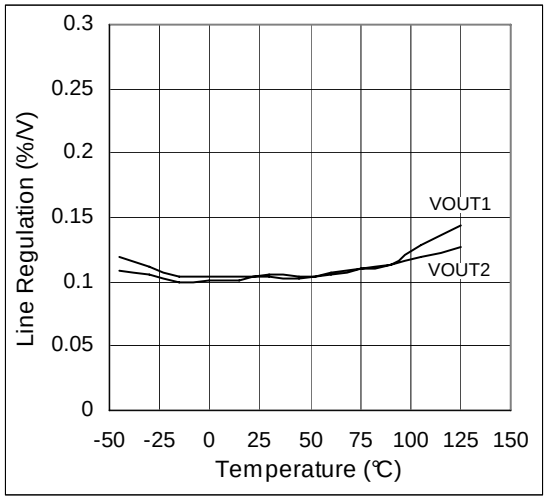


Figure 9. Quiescent Current vs. Temperature; VOUT = 2.8V, VIN = 3.3V, IOUT = 150mA, VSHDN = 1.4V

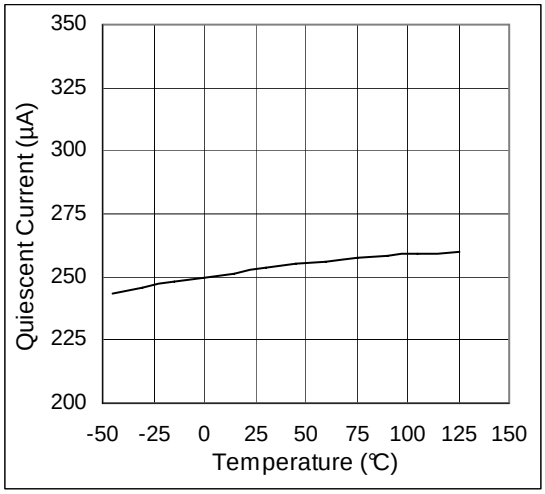


Figure 10. Quiescent Current vs. Temperature; VOUT = 2.8V, VIN = 3.3V, IOUT = 0mA, VSHDN = 1.4V

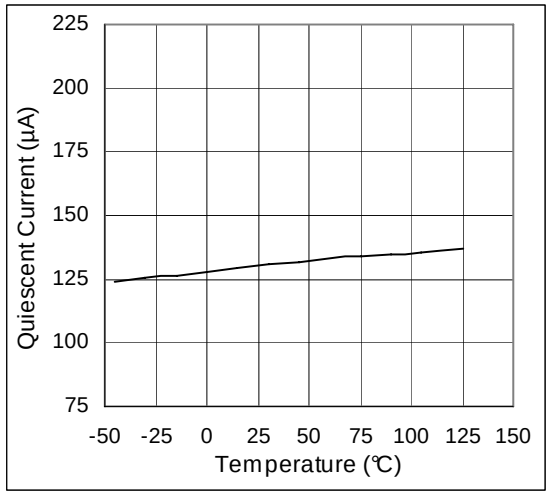


Figure 11. Line Transient Response; V_{IN} = 3.8 to 4.4V, I_{OUT} = 150mA, C_{IN} = C_{OUT} = 1µF, V_{OUT} = 2.8V C_{BYPASS} = 10nF, Rise Time/Fall Time = 1µs

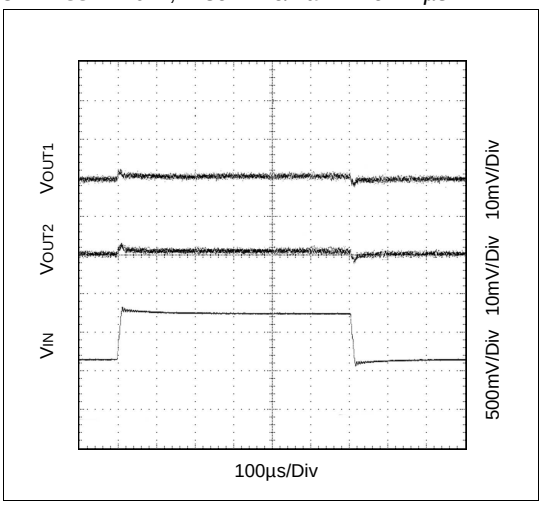


Figure 12. Load Transient Responds; V_{IN} = 3.3V, C_{BYPASS} = 10nF, C_{IN} = C_{OUT} = 1µF (Ceramic), t_R = 20ns, I_{OUT} = 1mA, V_{OUT} = 2.8V

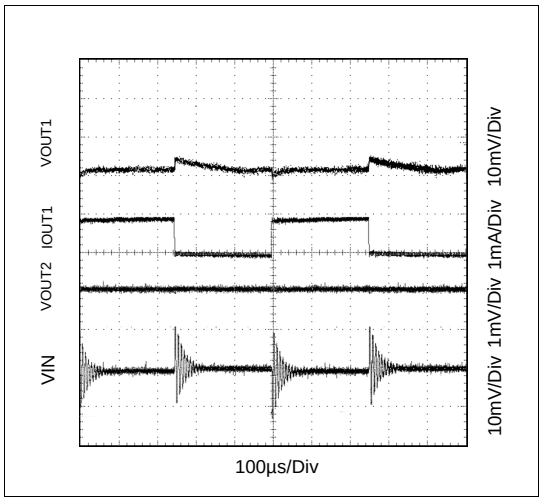


Figure 13. Turn On Time; V_{IN} = 3.3V, I_{OUT1} = I_{OUT2} =150mA, C_{IN} = C_{OUT} = 1µF, V_{OUT} = 2.8V C_{BYPASS} = 10nF, Rise Time/Fall Time = 1µs

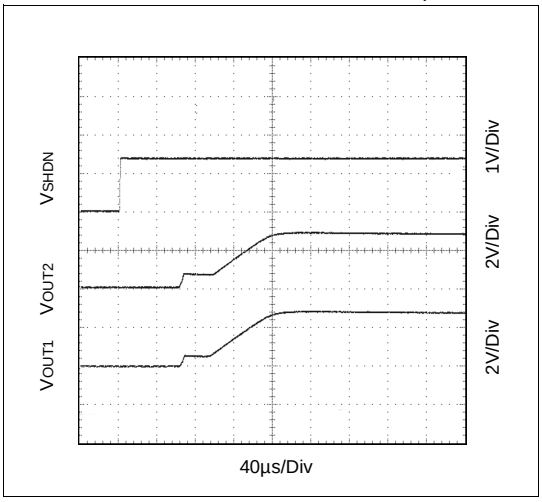
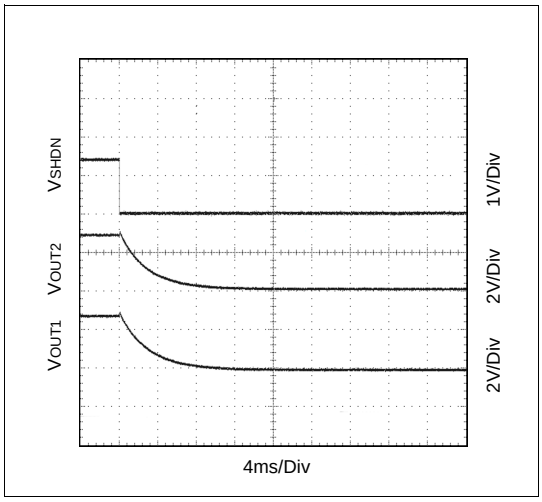


Figure 14. Turn Off Time; V_{IN} = 3.3V, C_{BYPASS} = 10nF, C_{IN} = C_{OUT} = 1µF (Ceramic), t_R = 20ns, I_{OUT} = 1mA, V_{OUT} = 2.8V



8 Detailed Description

Regulator On/Off Operation

The AS13986 outputs (V_{OUT1} and V_{OUT2}) are enabled by pulling the corresponding EN*x* pin high (1.4V) and disabled by pulling the EN*x* pin low (0V). For reliable operation, the signal source used to drive the EN*x* input must be capable of swinging above and below the specified turn-on/off voltage thresholds listed in Table 3 on page 4 (Enable Input Logic Low and Enable Input Logic High parameters).

Note: Reliable enable/disable operation of V_{OUT1} and V_{OUT2} is guaranteed by driving the EN*x* pins with t_R and t_F = 10ms.

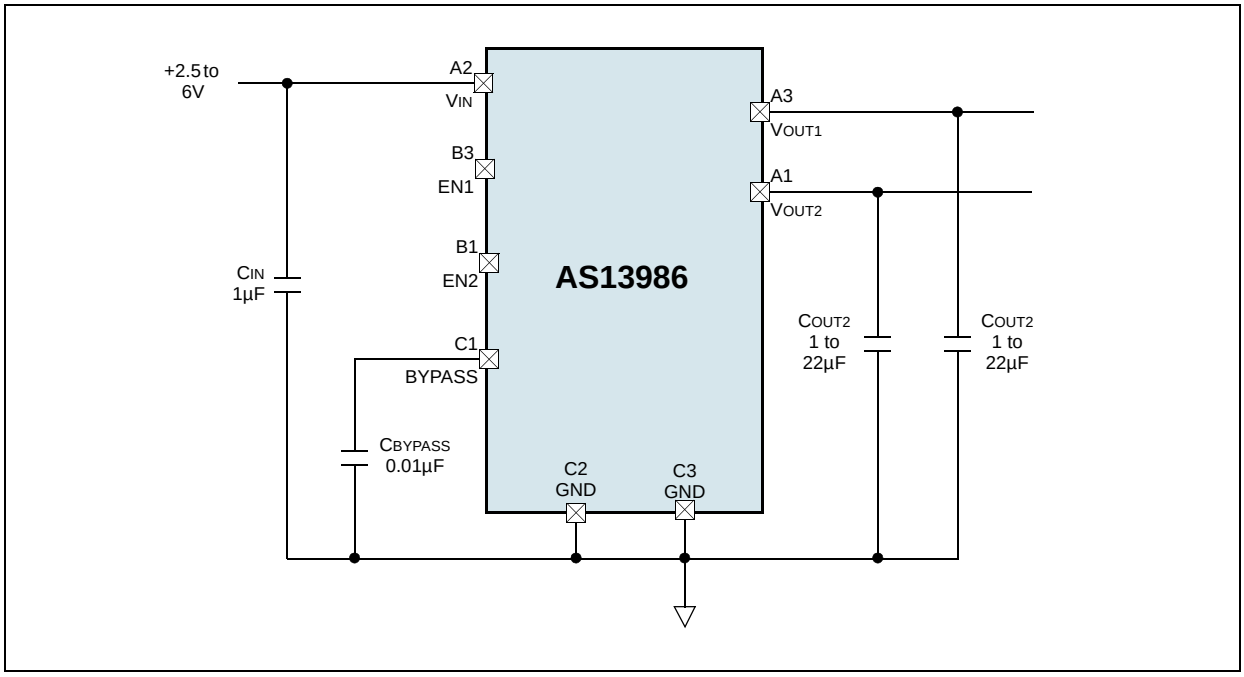
Fast Turn-On Time

In normal operation, the AS13986 outputs are turned on when V_{REF} reaches its regulated value (1.23V nominal). Turn-on time is decreased by charging the capacitor at pin BYPASS with the internal 70µA current source. The current source is turned off when the bandgap voltage reaches approximately 95% of its regulated value.

Turn-on time is determined by the time constant of the bypass capacitor; smaller capacitor values decrease turn-on time, although noise reduction decreases as well. Therefore, turn-on time and noise reduction must be taken into consideration when choosing the value of the bypass capacitor.

9 Application Information

Figure 15. Typical Application Diagram



Current Limit

The AS13986 features integrated short-circuit protection and a current limiting circuitry which controls the pass transistor gate voltage, limiting output current to approximately 500mA.

Thermal Overload Protection

On-chip thermal overload protection limits total power dissipation in the AS13986. When the junction temperature (T_J) exceeds +160ºC, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistors and allowing the device to cool down. The pass transistors will turn on again when the junction temperature cools by 20ºC (typ), resulting in a pulsed output during continuous thermal overload conditions.

Power Dissipation

Maximum power dissipation of the AS13986 depends on the thermal resistance of the case and PCB, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipated by the AS13986 is calculated as:

$$PD = IO\ (V_{IN} - V_{OUT}) \quad \textit{(EQ 1)}$$

The maximum power dissipation is:

$$PMAX = (T_{J(MAX)} - T_{AMB})/R_{TH} \quad \textit{(EQ 2)}$$

Where:

$T_{J(MAX)}$ = +125ºC
T_{AMB} is the ambient temperature.
R_{TH} is the thermal resistance.

External Component Selection

Input Capacitor

A ceramic, tantalum, or film capacitor of 1µF (typ) should be used between pin VIN and GND (the value of the capacitor may be increased without limit). This capacitor must be located a distance of not more than 1cm from VIN, and returned to a clean analog ground (see Figure 15).

Note: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be approximately 1µF over the entire operating temperature range.

Output Capacitor

The AS13986 was specifically designed to use very small ceramic output capacitors (temperature characteristics X7R, X5R, Z5U or Y5V) in 1 to 22µF range (ESR of 0.005 to 5Ω). Tantalum or film capacitors can be used at the output, however these types of capacitors require more PCB space and are more expensive than ceramic capacitors.

Note: The output capacitor must meet the minimum capacitance requirement and also have an ESR value which is within a stable range.

Bypass Capacitor

Noise on both regulator outputs (VOUT1 and VOUT2) can be significantly reduced by connecting a 0.01µF capacitor between pin BYPASS and GND (see Figure 15), with virtually no effect on the transient response of the AS13986. Using a bypass capacitor will also prevent output overshoot during start up. This capacitor should be connected directly to a high-impedance node in the band gap reference circuit. See also Fast Turn-On Time on page 8.

Note: Any significant loading on the high-impedance node will effect the regulated output voltage. For this reason, DC leakage current through pin BYPASS must be kept as low as possible for best output voltage accuracy.

High-quality ceramic capacitors with NPO or COG dielectric are ideal as bypass capacitors as they typically exhibit very low leakage current. Polypropylene and polycarbonate film capacitors are also a good choice as these capacitors typically have extremely low leakage current and are available in small surface-mount packages.

Layout and Grounding Considerations

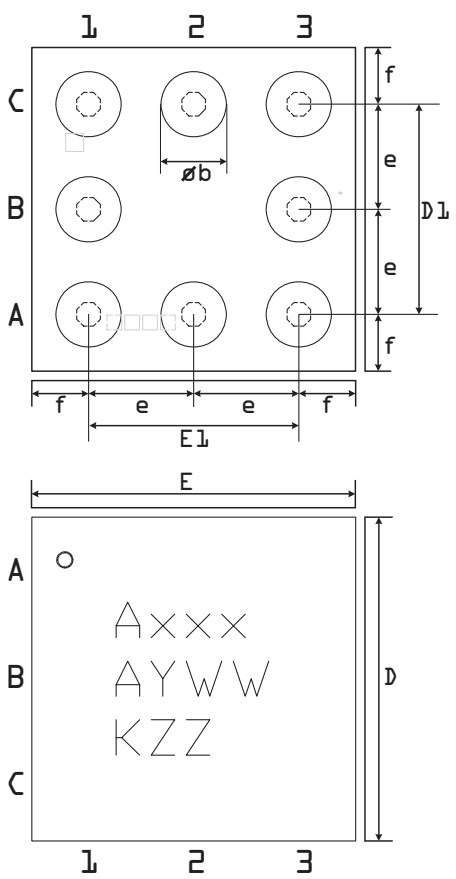
Well designed PC board layout is essential for optimizing device performance. In addition to providing electrical connections, the AS13986 pins also channel heat away from the die.

- Wide circuit-board traces and large, solid copper polygons should be used to improve power dissipation.
- Multiple vias to buried ground planes should be used to further enhance thermal conductivity.

10 Package Drawings and Markings

The device is available in an 8-pin WLP package.

Figure 16. 8-pin WLP Package



Symbol	Min	Typ	Max
A	0.570	0.600	0.630
A1	0.230	0.250	0.270
A2	0.340	0.350	0.360
b	0.301	0.311	0.321
D		1.550	
D1		1	
E		1.550	
E1		1	
e		0.5	
f		0.275	

11 Ordering Information

The device is available as the standard products shown in Table 4.

Table 4. Ordering Information

Ordering Code	Markings	Description	Delivery Form	Package
AS13986-2828-T	ASKP	Dual LDO 2.8V and 2.8V, 150mA	Tape and Reel	8-pin WLP
AS13986-1833-T	ASRL	Dual LDO 1.8V and 3.3V, 150mA	Tape and Reel	8-pin WLP
AS13986-xxyy-T[1]		Dual LDO, 150mA	Tape and Reel	8-pin WLP

1. *xx* is a placeholder for V_{OUT1}, 1.2V to 5.0V (in 50mV Steps).
yy is a placeholder for V_{OUT2}, 1.2V to 5.0V (in 50mV Steps).
Available upon request. For more information and inquiries contact http://www.austriamicrosystems.com/contact

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

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