1 General Description

The AS3654 is a highly integrated solution for power supply generation and monitoring, battery management including charging. It is controlled via a serial control interface and integrates all necessary system specific functions such as clock, reset and interrupt generation, voltage and temperature monitoring.

2 Key Features

System Control
- Serial Control Interface
- On/Off Control Module
- Reset Generation for system controller
- Programmable Interrupt Controller
- Low power off mode (9µA; 2.5V LDO on)

Supply Voltage Generation
- 1 RF Programmable Low Noise LDOs (400mA)
- 1 RF Programmable Low Noise LDOs (150mA)
- 2 Programmable Digital Low Power LDOs (200mA)
- 2 General Purpose PWM DC/DC step up converter with two programmable current sinks (e.g. for white led)
- 3 General Purpose high efficiency DC/DC step down converter
- 1 Low noise charge pump with 5V output voltage
- 1 Ultra Low Power 2.5V LDO (always on)

Current sinks
- 4 programmable(6-bit) from 0.625 to 40mA optional useable as GPIOs
- 3 programmable high voltage (15V) (6-bit) from 0.625 to 40mA

10-bit Successive Approximation ADC
- 40µs conversation time

Battery Management
- Full featured chemistry independent step down charger with included Gas Gauge and Current limitation.
- 0.15 Ω Battery switch for start-up during trickle charging
- Integrated USB charger up to 400mA

Power Management Features
- Wide Battery Supply Range 3.0...5.5V
- On-Chip Bandgap Tuning for High Accuracy (±1%)
- Current protection
- Thermal Protection with internal temperature sensor
- 0.35µm CMOS Solution

Audio
- Two Digital Audio Inputs (I2S interface)
- 18 Bit Audio DAC
- 2.9V low Noise LDO for Audio DAC
- Headphone Amplifier Output with GND separation
- GND Buffer for Headphone Amplifier
- Line/ Headphone output with GND separation

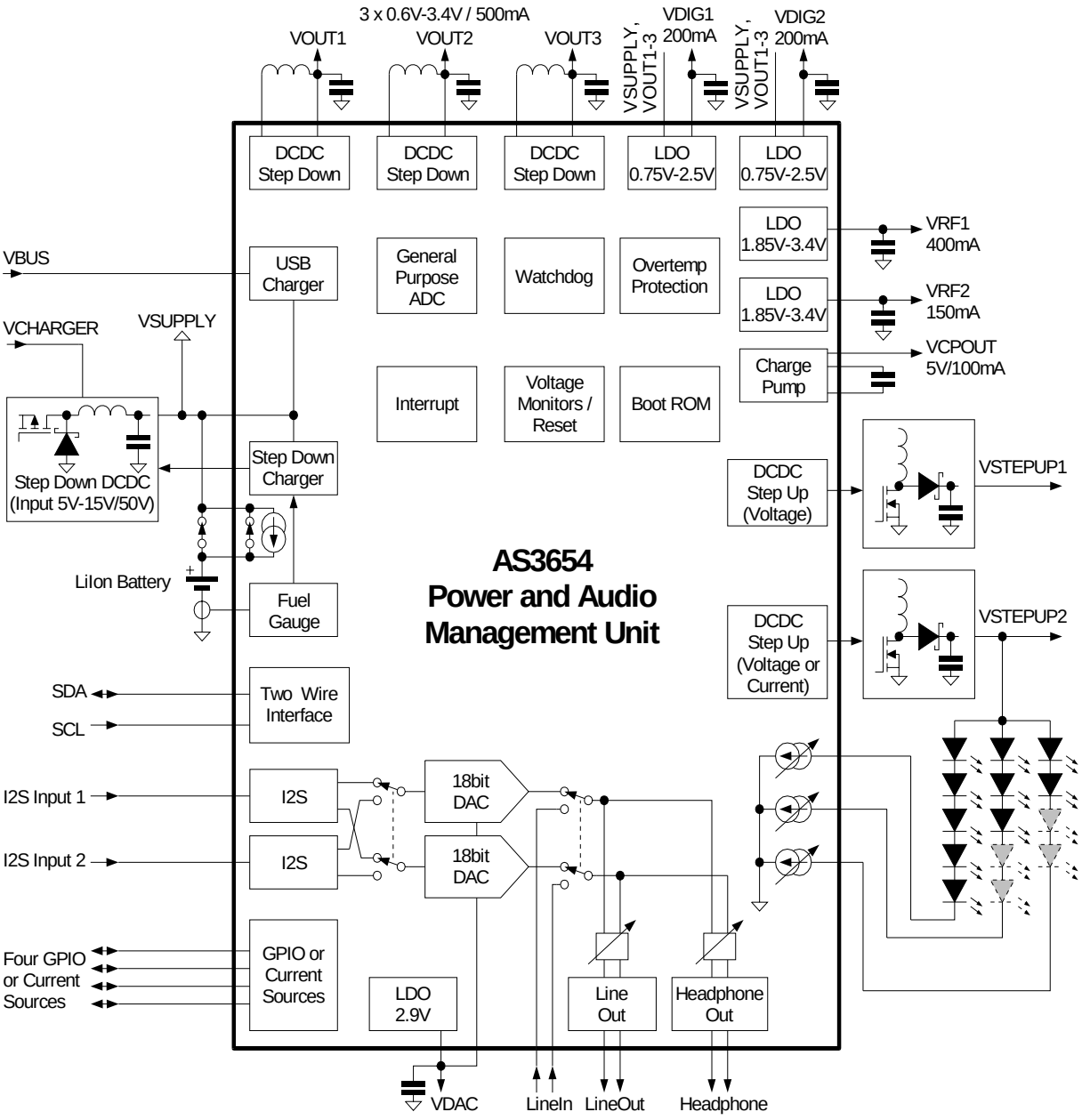
Programmable System clock
- 1.6 MHz to 2.3 MHz with 100 kHz steps

3 Applications

- Power and Audio Management Unit
- 1 Cell Li+ or 3 Cell NiMH powered devices
- Car Battery powered systems with and without internal battery

4 Block Diagram

Figure 1 – AS3654 Application Diagram



Document Revision History

Chapter	REV	Description of Change	Date	Author
all	0V19	- Additional descriptions and updates - Removed duplicated hp_det bit (register 58, b3)	21.3.2006	TJE/PTR
all	0V20	Typical XON pull up current updated = 5uA, Charger external components Qpu=BSS84 Added applicationdiagramm, reformatted headings	24.11.2006	TJE/PTR
all	0V21	- Changed V_{DETECT} minimum value to 2mV (dcdc stepup1 load detection) - Updated soldering conditions	12.1.2007	TJE/PTR
all	0V22	- Updated pwm_high_time and pwm_low_time settings - Updated package thickness tolerance from +/-0.1mm to +0.1/-0.15	17.12.2007	TJE/PTR

Index

List of Tables

List of Figures

5 Characteristics

5.1 Absolute Maximum ratings (non operating)

Stressed beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or beyond those under 'Operating conditions' is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 1 – Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{IN_HV}	High voltage pins	-0.3	17.0	V	Applicable for high voltage pins (1)
V_{IN_MV}	5V pins	-0.3	7.0	V	Applicable for pins 5V-pins (2)
V_{IN_LV}	3.3V pins	-0.3	5.0	V	Applicable for 3.3V-Pins (3)
I_{IN}	Input pin current	-25	+25	mA	At 25 °C, Norm: Jedec 78
T_{strg}	Storage Temperature Range	-55	125	°C	
	Humidity	5	85	%	Noncondens.
V_{ESD05}	Electrostatic discharge 0.5kV	-500	500	V	Norm: MIL 883 E Method 3015 Applicable for pins: LX1, LX2, LX3, VSUPPLY_1…VSUPPLY_6
V_{ESD1}	Electrostatic discharge 1kV	-1000	1000	V	Norm: MIL 883 E Method 3015 Applicable for pins: all, except the pins listed at V_{ESD05} Setup: Note(4)
P_t	Total Power Dissipation		1 0.72	W W	T_A = 70 degrees T_A = 85 degrees
Soldering Conditions					
TBODY	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
TPEAK	Solder Profile(5)	235	245	°C	
Dwell		30	45	s	above 217 °C

Notes

(1) HV pins are VCHARGER, VGATE, VOFF_B, DCDC_CURR1,DCDC_CURR2

(2) 5V pins are V_USB, CH_SENSE_N, CH_SENSE_P, VSUP_SW1, VSUP_SW2, VBAT_SW1, VBAT_SW2, V_BAT, SCL, SDA, XRESET, XINT, VSUPPLY_3, CURR1..6, DCDC_GATE1, DCDC_GATE2, DCDC_SENSE_P1, DCDCSENSE_P2, DCDC_SENSE_N1, DCDC_SENSE_N2, DCDC_FB1, DCDC_FB2, VCL, VCP_OUT, VCP_N, VCP_P, VCP_IN, VCP_IN, VRF1, VREF1_IN, VRF2, VRF2_IN, VDIG1, VDIG1_IN, VDIG2, VDIG2_IN, VSUPPLY_1, VSUPPLY_2, LX1, LX2, GND_SW, VSUPPLY_4, LINE_CM, HP_CM_PWR, HP_CM, LOUT_R, LOUT_L, ALVDD, AVDD, LSP_R, BVSS, LSP_L, AVDD, VSUPPLY_4

(3) 3.3V pins are ISENSEP, ISENSEN, ADC_IN, RPROGRAM, V2_5, CREF, ON, VI2S, SDI, SCLK, MCLK, LRCLK,AGND, VREF, LINL,LINR, VDAC

(4) ESD setup Following pins connected:
VSUPPLY_1...VSUPPLY_6, VCP_IN, VRF1_IN, VRF2_IN, VCURR connected together
VDIG1_IN,VDIG2_IN connected together
AVDD, ALVDD connected together

VBAT_SW1 and VBAT_SW2 connected together
VSUP_SW1 and VSUP_SW2 connected together
All VSS connected together

(5) Soldering austriamicrosystems strongly recommends to use underfill

5.2 Operating Conditions

Table 2 – Operating conditions

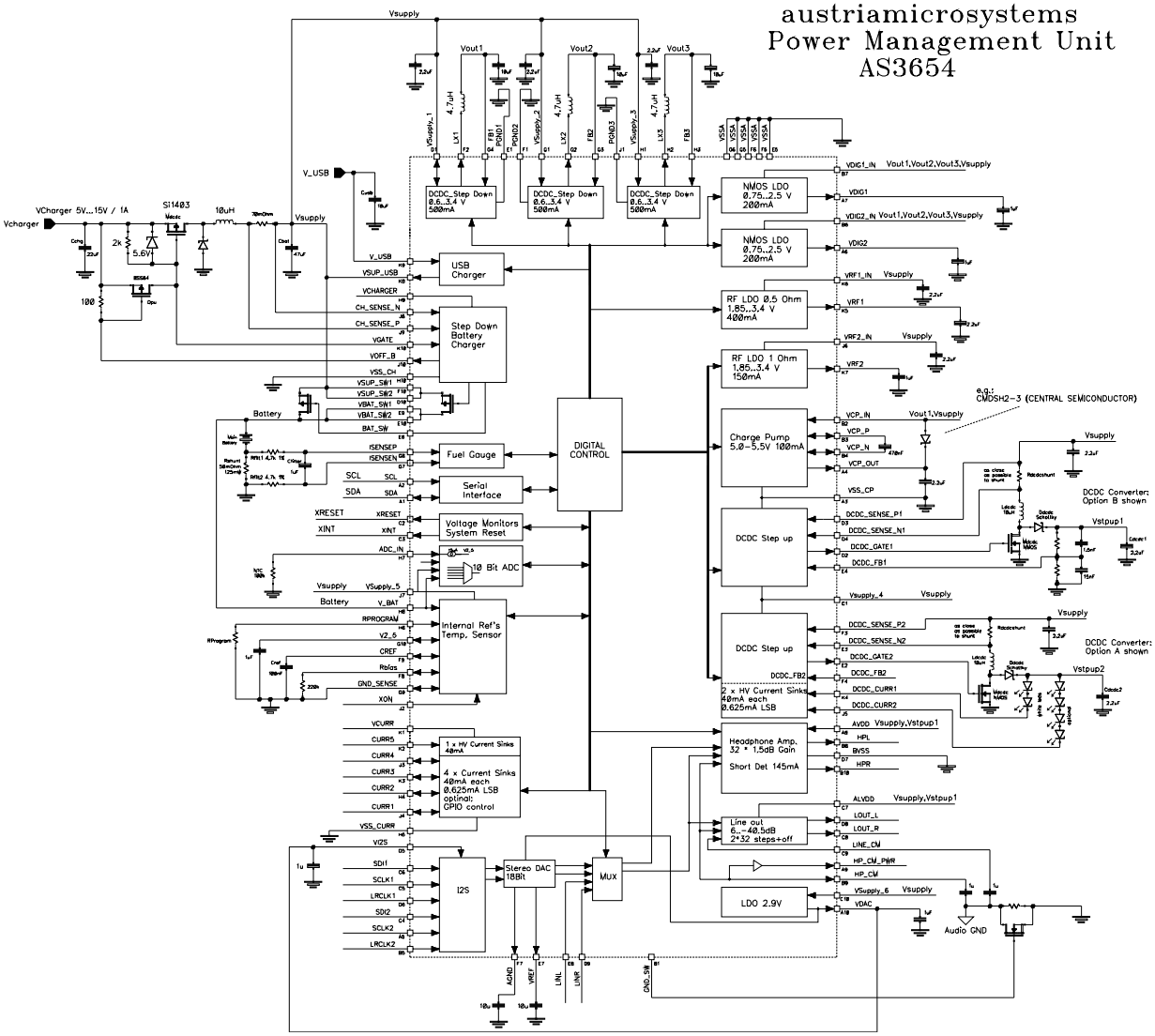
Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{HV}	High Voltage	0.0		15.0	V	VCHARGER, VGATE, DCDC_CURR1,DCDC_CURR2
V_{BAT}, V_{SUPPLY}	Battery, Supply Voltage	3.0	3.6	5.5	V	For pins V_BAT, VSUPPLY1-6 (always connect all VSUPPLY1-6 pins together), VSUP_SW1-2, VBAT_SW1-2, VRF1_IN, VRF2_IN, VCP_IN, AVDD, ALVDD, VCURR (1)
V2_5	Voltage on Pin V2_5	2.4	2.5	2.6	V	Internally generated
VCP_OUT	Output Voltage charge pump	4.9	5.2	5.6	V	Voltage generated by charge pump
T_{AMB}	Ambient Temperature	-30	25	85	deg.	
$I_{LOWPOWER}$	Low power mode current consumption		7 200		mA µA	Current consumption in low power mode with step down charger on(2) With step down charger off(3)
$I_{PowerOff}$	Power Off mode current consumption		16		µA	Current consumption in power off mode (4)

Notes

(1) During startup from the AC/DC adapter, the battery voltage can be below 3.0V
(2) with register bit **low_power_on** = 1, only Rf1=3.3V,Vout2=1.2V,Battery 3.6V,Vcharger=6.0V, no additional external loads
(3) with register bit **low_power_on** = 0, All regulators switched off, no additional external loads
(4) after setting register bit **xon_enable**=1 and **power_off**=1; only V2_5 is active in Power Off mode

6 General Description

Figure *2 – Blockdiagram AS3654*



7 Detailed Functional Descriptions

7.1 Step Up DC/DC Converter

Figure *3 – DC/DC step-up Converter 1*

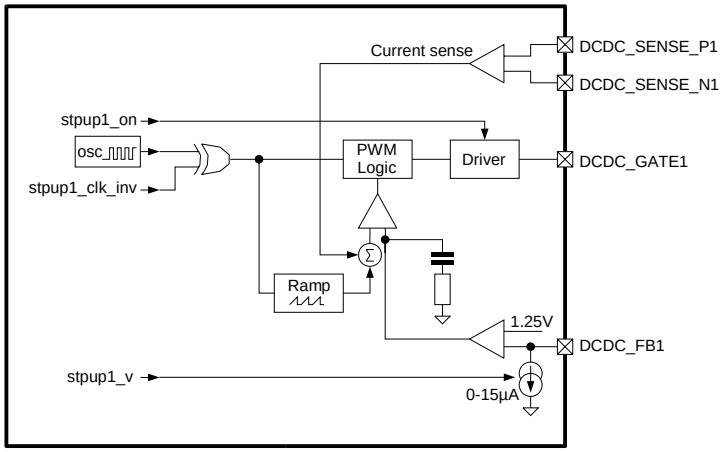


Figure *4 – DC/DC step-up Converter 2*

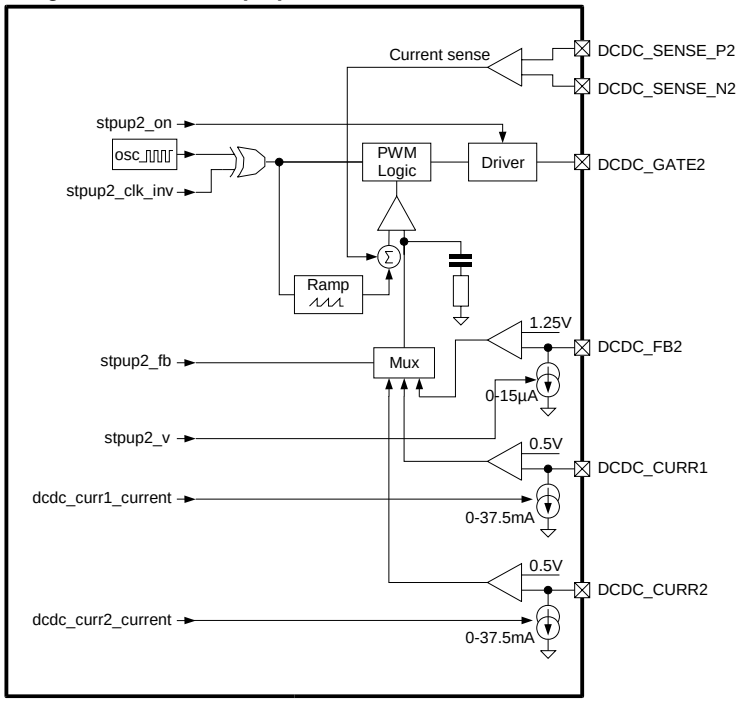


Table 3 – DC/DC Converter parameters

Symbol	Parameter	Min	TYP	Max	Unit	Note
I_{VDD}	Quiescent Current		140		µA	Pulse skipping mode
V_{FB1}	Feedback voltage for external resistor divider:	1.20	1.25	1.30	V	for constant voltage control
V_{FB2}	Feedback voltage for current sink regulation		0.5		V	DCDC_CURR1 or DCDC_CURR2
I_{DCDC_FB}	Additional tuning current at DCDC_FB	0		15	µA	adjustable by software in 1µA steps
	Accuracy of feedback current	-4		4	%	@ full scale
V_{rsense_max}	Current limit voltage at Rsense		100		mV	(e.g.: 0.65A for 0.15Ω sense resistor
R_{SW}	switch resistance			1	Ω	ON-resistance of external switching transistor
I_{load}	Load current	0		50	mA	at 15V output voltage
f_{IN}	Switching frequency		$f_{clk\_int}/2$		MHz	internal CLK frequency/2 Programmable: 0.8 to 1.15 MHz
C_{out}	Output capacitor		2.2		µF	ceramic, ±20%
L	Inductor		10		µH	Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency
t_{MIN_ON}	Minimum on time		130		ns	
MDC	Maximum duty cycle		91		%	

DC/DC Step Up converter is a high efficiency current mode PWM regulator, which provides an output voltage up to 20V and a load current up to 50mA . A constant switching frequency results in a low noise on supply and output voltage.

Feedback selection

For step up DCDC 1, the feedback is always DCDC_FB1.

For step up DCDC 2 following feedback selections are possible:
Stpup2_fb selects the type of feedback for the DCDC_step_up2 converter:
DCDC_CURR1, DCDC_CURR2 or DCDC_FB2 feedback (see Fig.3)

Setting stpup2_fb to 00b enables the feedback on DCDC_FB2, stpup2_fb to 01b enables feedback at pin DCDC_CURR1 , setting step_up_fb to 10b enables feedback at pin DCDC_CURR2. The Step-up converter is regulated such that the required current at the feedback path can be supported.
Always choose the path with the higher voltage drop as feedback to guarantee adequate supply for the other, unregulated path.
To protect the DCDC output voltage against overvoltage, if a LED string is broken, set stpup2_prot=1. In this mode the output voltage will be limited by limiting the DCDC_FB voltage to 1.25V (select the external resistor network to adjust this limitation voltage).

Figure *5 – DC/DC step up 2 converter with regulation of LED string on pin DCDC_CURR1 or DCDC_CURR2*

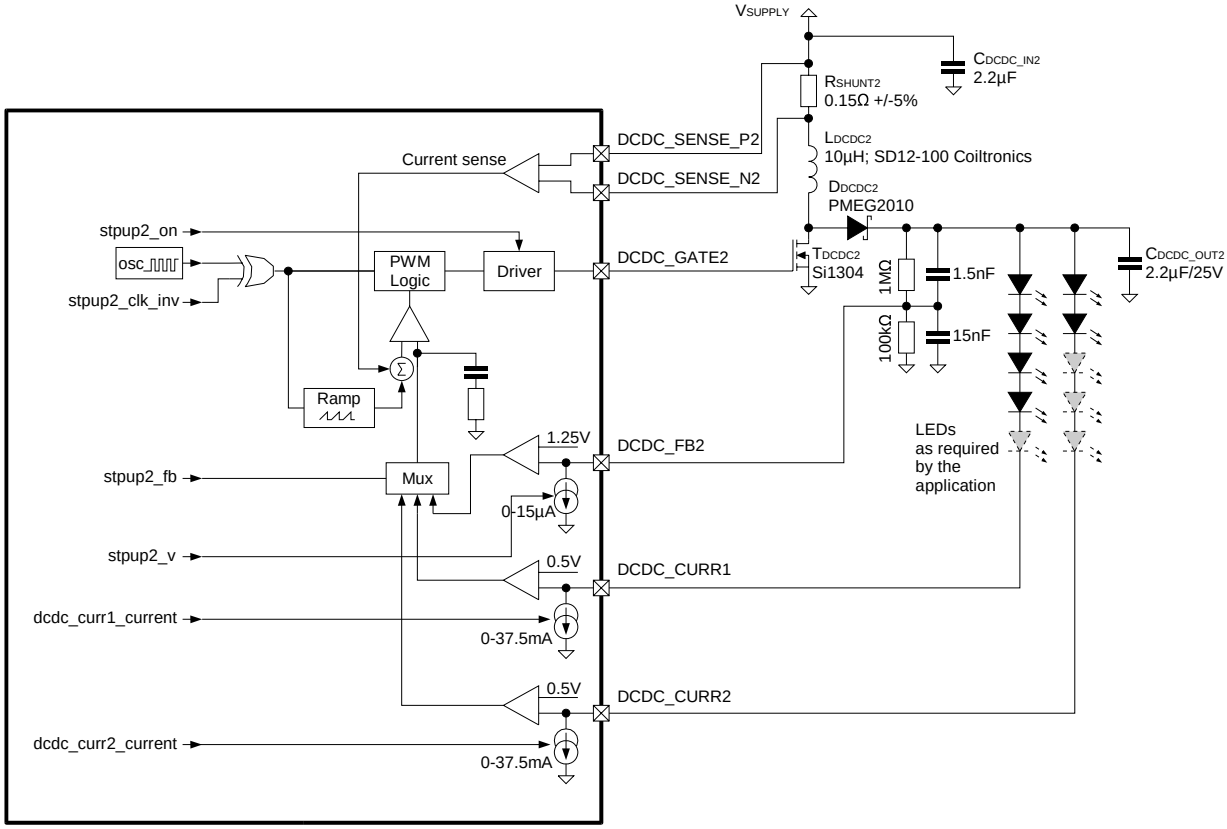
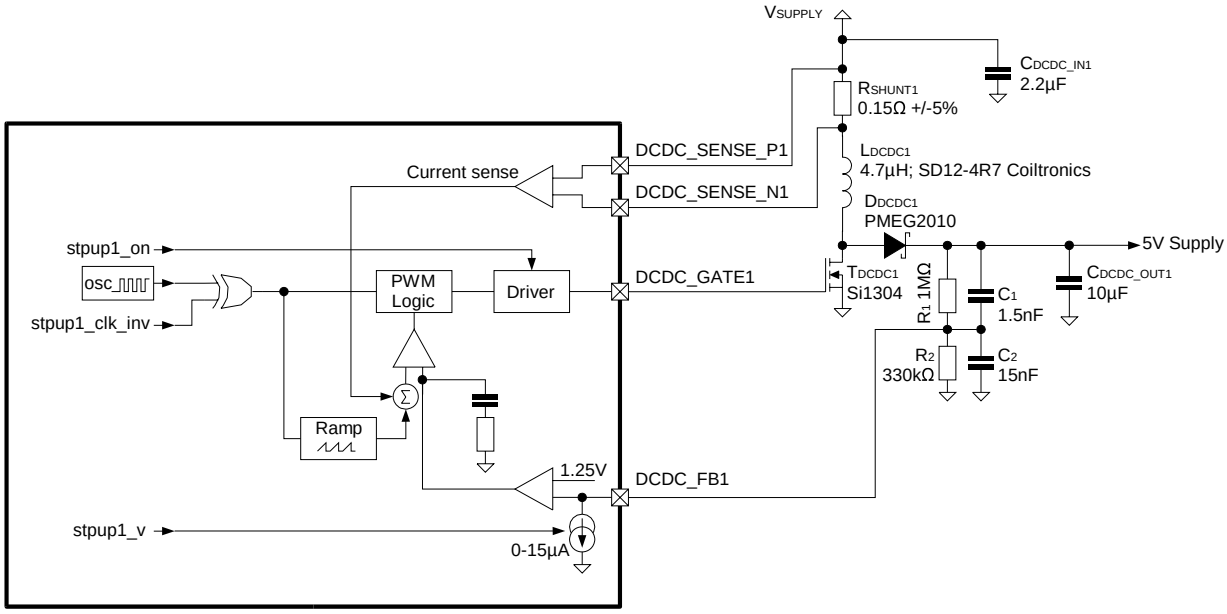


Figure *6 – DC/DC step up 1 converter with regulated output voltage of 5V. Feedback is at pin DCDC_FB1*



Voltage Feedback : (see Fig.5)

For Step UP DCDC 1 voltage feedback is always selected on pin DCDC_FB1. For Steup UP DCDC 2 set step2_fb to 00 to enable voltage feedbback at pin DCDC_FB2.
Bit stepX_res (X = 1 or 2) should be set to 1 in voltage feedback mode using two resistors.

The output voltage is regulated to a constant value, given by:

$$V_{stepup\_out} = \frac{R_1 + R_2}{R_2} 1.25 + I_{I_{DCDC\_FB}} \bullet R_1$$

If R2 is not used, the output voltage is:

$$V_{stepup\_out} = 1.25 + I_{I_{DCDC\_FB}} \bullet R_1$$

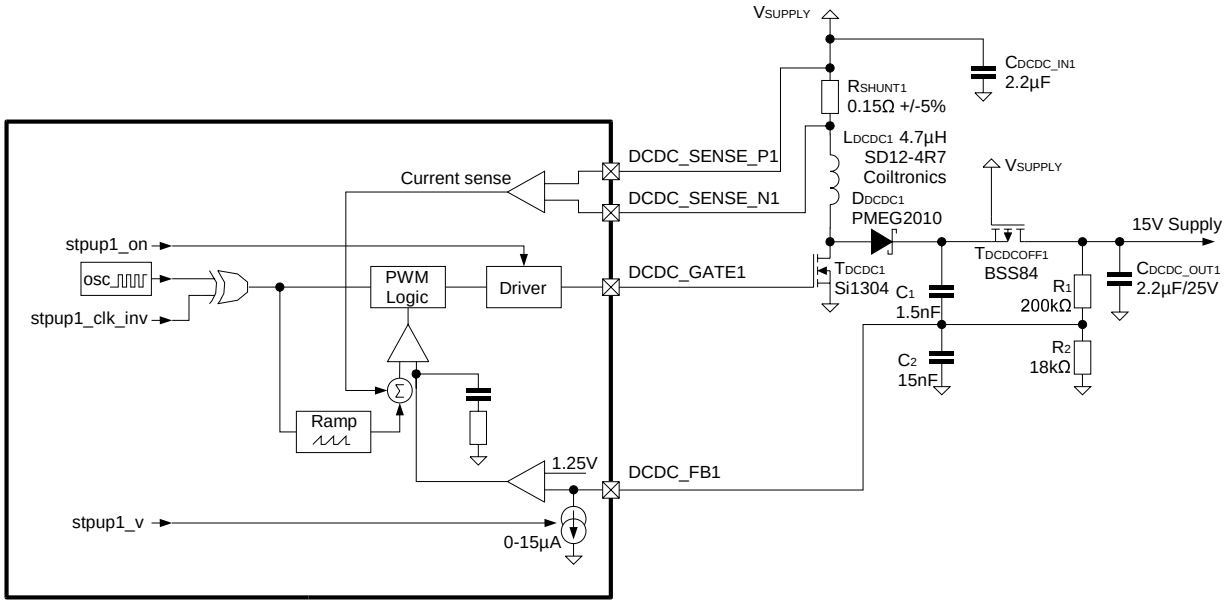
V_{stepup_out}	Step up regulator output voltage
R_1	Feedback resistor R1
R_2	Feedback resistor R2
$I_{Vtuning}$	Tuning current on DCDC_FB pin: stpupX_v (0µA to 15µA (1µA steps)) (X= 1 or 2)

Examples:

$I_{vtuning}$	V_{stepup_out}	V_{stepup_out}
µA	R1=1MΩ,R2 not used	R1=500kΩ,R2=64kΩ
0	-	11
1	-	11.5
2	-	12
3	-	12.5
4	-	13
5	6.25	13.5
6	7.25	14
7	8.25	14.5
8	9.25	15
9	10.25	15.5
10	11.25	16
11	12.25	16.5
12	13.25	17
13	14.25	17.5
14	15.25	18
15	16.25	18.5

Note: The voltage on pin DCDC_CURR1 and DCDC_CURR2 must never exceed 15V

Figure *7 – DC/DC step up converter 1 with regulated output voltage (15V), and switch off function of output voltage, to reduce shutdown current*



As the output voltage is always on, an additional output transistor can be added to reduce shutdown current through R1, R2 and the connected output circuit.
Note: A similar circuit can be used for step up converter 2.

Table 4 – Step Up DC/DC Bit definitions

Name	Default	Access	Description
stpupX_on	ROM	R/W	On/Off control of the step up dc/dc converter; (X=1 or 2)
stpupX_clkinv	ROM	R/W	Invert input clock of step up converter; (X=1 or 2) 0 Use positive edge of internal clk 1 Use negative edge of internal clk
stpup2_fb	ROM	R/W	Controls the feedback source 00 DCDC_FB enabled (external resistor divider) 01 DCDC_CURR1 feedback enabled (feedback through white LEDs) 10 DCDC_CURR2 feedback enabled (feedback through white LEDs) 11 reserved (don't use)
stpupX_freq	ROM	R/W	Defines the clock frequency of the step up dc/dc converter; (X=1 or 2) 0 $f_{clk\_int}/2$ (0.8 to 1.15 MHz) 1 $f_{clk\_int}/4$ (0.4 to 0.575 MHz)
stpupX_v	ROM	R/W	Defines the tuning current at DCDC_fb pin; (X=1 or 2) 0000 0 µA 0001 1 µA . 1111 15 µA
stpupX_res	ROM	R/W	Gain selection for DCDC step_up: (X=1 or 2) 0 Select 0 if DCDC is used with current feedback (DCDC_CURR1,DCDC_CURR2) or if DCDC_FB is used with current feedback only (Only R1,C1 connected; see Fig.6) 1 Select 1 if DCDC_FB1 or DCDC_FB2 is used with external resistor divider (2 resistors)
stpupX_fastskip	ROM	RW	DCDC converter output voltage at low loads, when pulse skipping is active: ; X=1 or 2 0: accurate output voltage, higher ripple (normal operation) 1: elevated output voltage, less ripple
stpup2_prot	ROM	RW	DCDC converter 2 overvoltage protection to prevent damage of external NFET, if DCDC_CURR1 or DCDC_CURR2 feedback selected, and no LED string connected: 0: Overvoltage protection disabled. 1: Switch off DCDC step up 2 if the voltage on DCDC_FB2 exceeds 1.25V
stpup1_shortprot	ROM	RW	Enables Protection and Detection circuit for DCDC step up1 – see next section 0: No protection and load detection 1: Short protection and load detection enabled
stpup1_oc_timeout	ROM	RW	Controls GPIOx switch off, after overcurrent timeout (5ms) for DCDC step up 1 0: disabled 1: enabled

Table 5 – Step Up Registermap

Register Definition	Addr.[1]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Step Up DC/DC Control	15	ROM (00h)	stpup2_res	stpup2_fastskip	stpup2_freq		stpup1_res	stpup1_fastskip	stpup1_freq	
Step Up1 DC/DC Control	16	ROM (00h)		stpup1_oc_timeout	stpup1_shortprot	stpup1_clkinv	stpup1_v			
Step Up2 DC/DC Control	17	ROM (00h)	stpup2_prot	stpup2_clkinv	stpup2_fb		stpup2_v			
Reg Power2 Ctrl	31	ROM					stpup2_on	stpup1_on	rf2_sw	rf1_sw

7.2 Stepup1 load detection and overcurrent protection circuit

This circuit protects the DCDC step up1 converter during short circuit and startup, by regulation of the output current.
An additional feature is the detection of a minimum output load of the StepUp converter. It is also possible to use this circuit without the DCDC step up converter, by using the sense resistor only:

- Detection circuit
  If the voltage on R_{sense} exceeds V_{DETECT} for more than 1msecond, or the DCDC Step up converter is not in Pulseskip for more than 1 msecond, the stepup1_det bit will be set.
- Overcurrent protection
  If the Overcurrent voltage $V_{OVCURRENT}$ has been exceeded by more than 5 msec the Bit stpup1_oc will be set and can only reset, by switching off and on the Protection circuit by writing Stpup1_shortprot 0 – 1.
  If stepup1_oc is set the load will be disconnected, if Stpup1_oc_timeout=1

Table 6 – StepUp1 protection/detection circuit parameters

Symbol	Parameter	Min	TYP	Max	Unit	Note
V_{DETECT}	Detection Threshold	2	12.5	20	mV	For Rsense=0.150Ohm => 83mA typ.
$V_{OVCURRENT}$	Overcurrent Threshold rising	150	180	215	mV	For Rsense=0.150Ohm => 1.2A typ.
$V_{OVhysteresis}$	Overcurrent Hysteresis		50		mV	
$t_{OV\_timeout}$	Overcurrent timeout		5		ms	Interrupt and/or external PMOS switching off after timeout f_{clk_int} = 2.2MHz
t_{detect}	Detection denounce time		1		ms	f_{clk_int} = 2.2MHz

[1] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

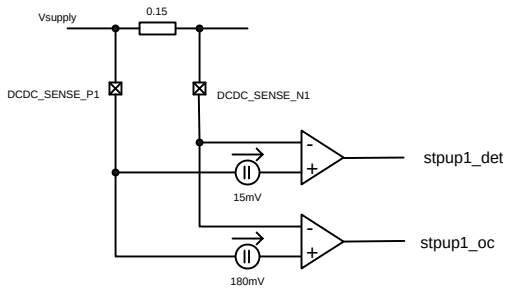


Table 7 – Low voltage status Bit definitions (stpup1_det and stpup1_oc)

Name	Default	Access	Description
stpup1_det	NA	R	Step up detection status register 0 V_{Rsense} < V_{DETECT} for more than 1msecond, and DCDC Step up converter is in Pulseskip for more than 1 msecond 1 V_{Rsense} > V_{DETECT} for more than 1msecond, or the DCDC Step up converter is not in Pulseskip for more than 1 msecond
stpup1_oc	NA	R	Step up overcurrent status bit 0 V_{Rsense} < $V_{OVCURRENT}$ 1 V_{Rsense} > $V_{OVCURRENT}$ for more than 5 msec (latched state)

Table 8 – Step Up protection Registermap

Register Definition	Addr.[2]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Low voltage Status	47	40h	stpup1_det	stpup1_oc	hpdet	dig2_lv	dig1_lv	sd3_lv	sd2_lv	sd1_lv

[2] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

7.3 Current Sinks

These are general-purpose current sinks intended to control the backlight(s), buzzer and vibrator. The low voltage current sink has an integrated protection against over voltage and can therefore also drive inductive loads ($V_{PROTECT}$).

DCDC_CURR1 and DCDC_CURR2, CURR5 are high voltage (15V) current sinks, e.g. for series of white LEDs
CURR1,CURR2, CURR3, CURR4 are four 5V, 40mA current sinks, e.g. for buzzer, vibrator, LEDs

CURR1, CURR2, CURR3, CURR4 can be used as general propose Input/Output (GPIO) functions optional

7.3.1 High voltage Current Sinks 40mA (CURR5, DCDC_CURR1 and DCDC_CURR2):

Current sinks CURR5 DCDC_CURR1 and DCDC_CURR2 can be controlled individually. The step-up DCDC converter may supply them with voltages up to15V.

Table 9 – Current Sinks Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
$I_{DCDC\_Curr1,2,5}$	DCDC_CURR1,2 and CURR5 current, 00h-3Fh	0		40	mA	For V(CURRx) > 0.45V resolution = 0.625mA
$I_{DCDC\_protect}$	Current sink protection Current		2		µA	Protection Current if stpup2_on=1 and dcdc_currx_current=00h
Δ	absolute Accuracy	-20%		+20%		All Current sinks
V_{DCDC_Curr1}, V_{DCDC_Curr2}	Voltage compliance	0.45		15	V	during normal operation

Table *10 – Current Sink Bit definitions*

Name	Default	Access	Description
dcdc_currX_current, curr5_current	(00)h	R/W	Defines the current into DCDC_CURRX (X = 1…4) 00h power down (default state) 01h 0.625mA … 3Fh 39.375mA
dcdc_currX_low_bias, curr5_low_bias	0b	R/W	Reduces bias current by 2 0 Normal current (LSB=0.625mA, max current= 39.375mA) 1 Current reduction by 2 (LSB=0.3125mA, max current= 19.687mA)
dcdc_currX_ctrl, curr5_ctrl	00b	R/W	On/Off control of the pad DCDC_CURR1,2 and CURR5 00 Pad is turned off 01 Pad is active 1X don't use

7.3.2 Low voltage Current Sink 40mA (CURR1, CURR2, CURR3, CURR4):

Curr1, Curr2, Curr3, Curr4 can be controlled individually. Each one can sink up to 40mA.

Table *11 – Current Sinks Characteristics*

Symbol	Parameter	Min	Typ	Max	Unit	Note
$I_{CURR1,2,3,4}$	Curr1,2,3,4 current, 00h-1Fh	0		40	mA	For V(CURRx) > 0.2V resolution = 0.625mA, each current sink
Δ	absolute Accuracy	-20%		+20%		All Current sinks
$V_{Curr1,2,3,4}$	Voltage compliance	0.2		Vcurr.	V	during normal operation, New pin will be added

Table *12 – Current Sink Bit definitions*

Name	Default	Access	Description
currX_current	(00)h	R/W	Defines the current into CURRX (X = 1…4), if Register *GPIOXmode=011b or 100b* 00h power down (default state) 01h 0.625mA … 3Fh 39.375mA
currX_low_bias	0b	R/W	Reduces bias current by 2 for CURRX (X = 1…4) 0 Normal current (LSB=0.625mA, max current= 39.375mA) 1 Current reduction by 2 (LSB=0.3125mA, max current= 19.687mA)

Table 13 – Currentsink registermap

Register Definition	Addr.[3]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
DCDC_CURR1 value	35	00h		dcdc_curr1_low_bias	dcdc_curr1_current					
DCDC_CURR2 value	36	00h		dcdc_curr2_low_bias	dcdc_curr2_current					
CURR1 value	37	00h		curr1_low_bias	curr1_current					
CURR2 value	38	00h		curr2_low_bias	curr2_current					
CURR3 value	39	00h		curr3_low_bias	curr3_current					
CURR4 value	40	00h		curr4_low_bias	curr4_current					

[3] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

Register Definition	Addr.[3]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
CURR5 value	41	00h		curr5_low_bias	curr5_current					
CURR control	51	00h			curr5_ctrl		dcdc_curr2_ctrl		dcdc_curr1_ctrl	

7.4 General Purpose Input / Output (GPIO) Pins

7.4.1 High Current GPIO Pins (Same pins as Current sinks CURR1…4)

The device contains 4 high current GPIO pins, which using the same pins CURR1...4, that are capable of sinking 100mA from any supply or VSUPPLY voltage. Each of the pins can be configured as open drain NMOS or push-pull output with VCURR high levels, as high impedance output or as digital input. When configured as output the output source can be a register bit, or the PWM generator, furthermore the output signal can be inverted. Integrated active clamp circuits can be enabled for the open drain NMOS output mode by setting *GPIOxPulls*=11b, thus allowing to use the high current GPIO pins for driving inductive loads. A pull-up resistor to VCURR can be enabled for the open drain NMOS output mode by setting *GPIOxPulls*=10b. When configured as digital input the logic level (*GPIOxInvert*='0') or the inverted logic level (*GPIOxInvert*='1') of the pin is reflected by bit *GPIOxBit* in the *GPIO Bit* register. Moreover, a special function can be selected for each digital input pin and a pull-up resistor to VCURR or a pull-down resistor can be enabled.

Table 14 – High Current GPIO Pin Characteristics (GPIO1…4)

$V_{VSUPPLY}$=3.0…5.5V; T_{amb}=–20…+70°C; unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{GPIOMAX}$	Maximum voltage on GPIO1…4 pins			$V_{Vcurr.}$+0.3	V	
V_{OLH}	Low level output voltage switch mode	–0.3		+0.35	V	I_{OL}=+100mA; digital output (GPIOxMode=100b and currentx=3Fh)
V_{OL}	Low level output voltage	–0.3		+0.4	V	I_{OL}=+1mA; digital output (GPIOxMode=000b ... 010b)
V_{OH}	High level output voltage	0.8·$V_{Vcurr.}$		$V_{Vcurr.}$	V	I_{OH}=–1mA; digital push-pull output
V_{IL}	Low level input voltage	–0.3		0.4	V	digital input
V_{IH}	High level input voltage	1.3		$V_{Vcurr.}$	V	digital input
$I_{LEAKAGE}$	Leakage current			10	µA	high impedance
$R_{pull-up}$	Pull-up resistance		78		kΩ	*GPIOxMode*=x0b; *GPIOxPulls*=10b; VCURR=3.6V
$R_{pull-down}$	Pull-down resistance		161		kΩ	digital input; *GPIOxPulls*=01b; VCURR=3.6V

Table 15 – GPIO 1…4 Register

R/W access;

Bit	Symbol	Default	Description
2…0	*GPIOxMode*	ROM	000b digital open drain NMOS output 001b digital push-pull output 010b digital input 011b digital open drain current sink operation Current defined by CURRx_current 100b digital open drain switch operation On resistance defined by CURRx_current101b to 111b .high impedance (

Bit	Symbol	Default	Description
4…3	*GPIOxIOSF*		00b input / output signal is written to or set by *GPIOxBit* in the *GPIO Bit* register 01b PWM (O) / WDOG (I) if used for PWM, pwm_h_time and pwm_l_time define the high and low time of this output 10b Protection of DCDC stepUp1 GPIO X (O) 11b NA
5	*GPIOxInvert*		0 normal polarity of input / output signal 1 inverted polarity of input / output signal
7…6	*GPIOxPulls*		00b no pull-up or pull-down resistor is enabled in all modes 01b pull-down resistor is enabled in digital input mode (clamp disabled) 10b pull-up resistor is enabled for *GPIOxMode*=000b,010b,011b,100b (clamp disabled) 11b enable active clamp circuit for *GPIOxMode*=000b,010b,011b,100b (pull-up/down disabled)

Table 17 – GPIO Bit Register

Address 58; R/W access; register is reset at power-on-reset only and at each reset cycle.

Bit	Symbol	Default	Description
0	*GPIO1*	0	This bit determines the output signal of the GPIO1 pin when selected as output source
1	*GPIO2*	0	This bit determines the output signal of the GPIO2 pin when selected as output source
2	*GPIO3*	0	This bit determines the output signal of the GPIO3 pin when selected as output source
3	*GPIO4*	0	This bit determines the output signal of the GPIO4 pin when selected as output source
4	*GPIO1_in*	NA	This bit reflects the logic level of the GPIO1 pin when configured as digital input pin
5	*GPIO2_in*	NA	This bit reflects the logic level of the GPIO2 pin when configured as digital input pin
6	*GPIO3_in*	NA	This bit reflects the logic level of the GPIO3 pin when configured as digital input pin
7	*GPIO4_in*	NA	This bit reflects the logic level of the GPIO4 pin when configured as digital input pin

Table 18 – PWM Frequency Control High Time Registers

Address 49; R/W access; register is reset at power-on-reset only and at each reset cycle.

Bit	Symbol	Default	Description
7-0	*pwm_h_time*	00h	This bit defines the high time of the pwm generator in $2/f_{clk\_int}$ units 0 = $2/ f_{clk\_int}$ 1 = $3/ f_{clk\_int}$ 2 = $4/ f_{clk\_int}$ … FFh = $257/ f_{clk\_int}$

Table 19 – PWM Frequency Control Low Time Registers

Address 49; R/W access; register is reset at power-on-reset only and at each reset cycle.

Bit	Symbol	Default	Description
7-0	*pwm_l_time*	00h	This bit defines the low time of the pwm generator in $2/f_{clk\_int}$ units 0 = $2/ f_{clk\_int}$ 1 = $3/ f_{clk\_int}$ 2 = $4/ f_{clk\_int}$ … FFh = $257/ f_{clk\_int}$

The following settings are not allowed: **pwm_h_time - pwm_l_time = 1** or **pwm_h_time - pwm_l_time = -1**

Table 20 – GPIOs Registermap

Register Definition	Addr.[4]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
GPIO 1	18	ROM (07h)	gpio1_pulls		gpio1_invert	gpio1_iosf		gpio1_mode		
GPIO 2	19	ROM (07h)	gpio2_pulls		gpio2_invert	gpio2_iosf		gpio2_mode		
GPIO 3	20	ROM (07h)	gpio3_pulls		gpio3_invert	gpio3_iosf		gpio3_mode		
GPIO 4	21	ROM (07h)	gpio4_pulls		gpio4_invert	gpio4_iosf		gpio4_mode		
GPIO Signal	48	NA	gpio4_in	gpio3_in	gpio2_in	gpio1_in	gpio4	gpio3	gpio2	gpio1
PWM Frequency Control High Time	49	00h	pwm_h_time							
PWM Frequency Control Low Time	50	00h	pwm_l_time							

7.5 ADC

Table *21 –ADC Characteristics*

Parameter	Symbol	Min	Typ	Max	Unit	Note
Resolution		10			Bit	
Input Voltage Range	Vin	0		1.8	V	
Differential Nonlinearity	DNL		± 0.25		LSB	1LSB ≈ 1.76mV
Integral Nonlinearity	INL		± 0.5		LSB	
Input Offset Voltage	Vos		2		LSB	
Input Impedance	Rin	100			Mohms	
Input Capacitance	Cin			9	pF	
Power Supply Current	Idd		500		µA	During conversion only
Power Down Current	Idd		100		NA	
Transient Parameters (25°C)						
Conversion Time	Tc		40		µs	
Clock Frequency	fc		$f_{clk\_int}/8$		kHz	internal CLK frequency/8 Programmable: 0.2 to 0.2875 MHz
Settling time of S&H	ts	1			µs	
ADC_IN pull up current		14.25	15	15.75	µA	Pull up current, if adc_idc=1111b

[4] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

Table *22 - ADC Bit definitions*

Name	Default	Access	Description
start_conversion	0b	W	Writing a 1 into this bit starts one ADC conversion.
adc_on	0b	R/W	Writing a 1 into this bit activates the ADC and the input multiplexer. The ADC and the MUX are also activated for a conversion period when start_conversion is set to '1'
adc_select	000b	R/W	Selects an ADC channel 000 ADC_IN (LSB = 1.76mV) 001 not used 010 VBAT (Battery voltage divided by 3) (LSB=5.27mV) 011 Vcharger (Charger voltage divided by 10) (LSB=17. 6mV) clamping at 10V! 100 USB Voltage (USB voltage divided by 3) (LSB=5.27mV) 101 not used 110 vtemp (temperature sensor output voltage) (LSB=1.76mV) 111 ADC test channel
adc_idac	000b	R/W	Current source at ADC_IN input 0000 0µA 0001 1µA ... 1111 15 µA
adc_test	0b	R/W	always 0, don't change
adc_slow	0b	R/W	select ADC sampling frequency 0 275kHz (conversion time: 60us) 1 70kHz (conversion time: 240us)
result_not_ready	NA	R	Indicates end of conversion 0 result is ready 1 conversion is running
D0 - D9	NA	R	ADC result register

Figure *8 – ADC Timing-diagram*

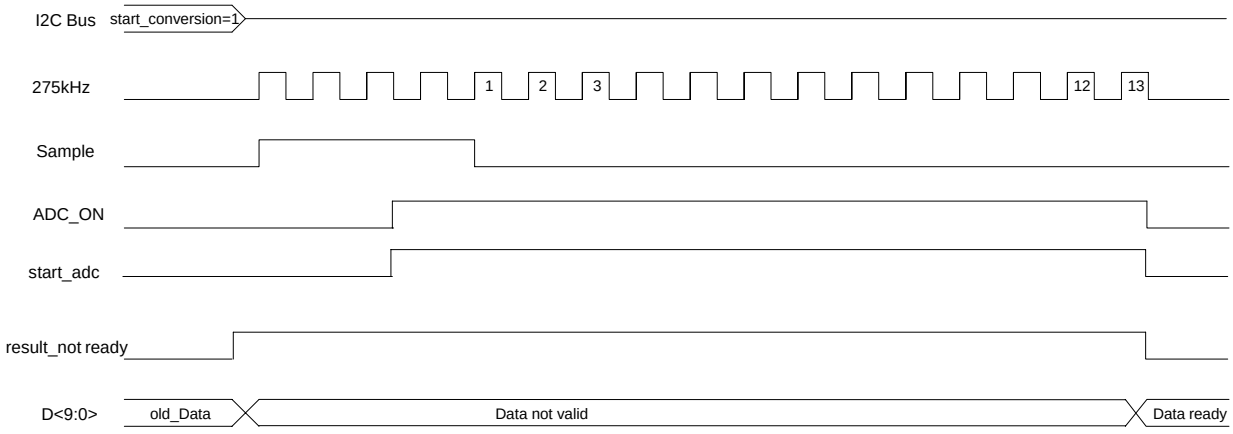


Table *23 – ADC register map*

Register Definition	Addr.[5]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
ADC_control	63	00h	start_conversion	adc_on		adc_slow	adc_test	adc_select		
ADC_MSB result	64	NA	result_not_ready	D9	D8	D7	D6	D5	D4	D3
ADC_LSB result	65	NA						D2	D1	D0
ADC Idac	42	00h					adc_idac			

7.6 Internal Battery switch (Vsupply , Battery)

The internal Battery switch enables normal operation of the System during trickle charging of a deeply discharged battery.
The Switch provides the following functions:

- Trickle charging, if Vbattery is smaller than ResVolt. The current is defined in TrickleCurrent[1:0]
  PMOS is switched on if Vbattery is greater then ResVolt.
- Current limitation during tricklecharge, to avoid inrush current : $I_{trickle\_Ilimit}$
- Undervoltage protection of Vsupply during trickle charge. The trickle current is switched of , if Vsupply drops below $V_{trickleoff}$
- Ideal diode operation in Isolate Battery mode and disable charging mode, if charger is unplugged. This operation is for the internal battery switch only. External battery switch is open in that mode. Regulation will start, if the VSUPPLY voltage drops by more then V_{Diode} below the VBattery voltage

Table *24 – Battery switch parameters*

Symbol	Parameter	Min	TYP	Max	Unit	Note
V_{Supply}	Input voltage	3.0		5.5	V	PIN VSUP_SW1,VSUP_SW2
$I_{trickle\_limit}$	Trickle current limit		400		mA	
V_{Diode}	Ideal Diode start voltage		50		mV	
$V_{trickleoff}$	Vsupply threshold for trickle enable	-6%	3.9	3%	V	Trickle current will be switched of, if vsupply drops below this level
R_{SW}	P-Switch ON resistance		0.15		Ω	VSUP_SW=3.6V

Table *25 – Battery switch status Bit definitions*

Name	Default	Access	Description
batsw_mode		R	0 Trickle charging, if batsw_on=1. External PMOS switch disabled 1 Switch on Battery switch, if batsw_on=1. External PMOS switch enabled.
batsw_on		R	0 Battery switch off 1 Battery switch on (Mode defined by batsw_mode)

[5] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

Table 26 – Battery switch Registermap

Register Definition	Addr.[6]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
ChargerStatus_usb	67	NA					batsw_on	batsw_mode	USB_ChAct	USB_ChDet

7.7 Step Down Charger

The battery charge controller controls the Step Down charger.
During Trickle charge of the deeply discharged battery the step down converter regulates the Vsupply to $V_{chlimit}$.
If the Vbattery voltage exceeds ResVoltRise, the internal battery switch is switched on, the Vsupply voltage drops down to Vbattery immediately, and the step down converter operates as controlled current source to Vsupply. The battery current is regulated to the value defined in ConstantCurrent register.
In EOC operation (see section Battery Charge Controller), the operation of the step down charger depends on the bit isolate_battery:
If isolate_battery = 1 and EOC the output is regulated to $V_{chlimit}$.
If isolate_battery = 0 and EOC the output is not allowed to drop below V_{EOC} (3.6V).

Table *27 – Step down charger parameters*

Symbol	Parameter	Min	TYP	Max	Unit	Note
$V_{chlimit}$	Voltage limit of Step down (if not in current limitation mode)	-3%	ch_voltage	3%	V	Vsupply voltage
V_{rsense_max}	Current limit voltage at Rsense	70	100	130	mV	(e.g.: 1.4A for 0.07Ω sense resistor typ.)
C_{out}	Output capacitor	20		60	µF	X7R ceramic
L	Inductor		10/22		µH	See table 32 – Charger External Components
$I_{trickle\_limit}$	Trickle current limit		400		mA	

Table 28 – Step Down Charger control

Address; R/W access; register is reset at power-on-reset only. Default value after reset: 00h.

Bit	Symbol	Default	Description
0	*sdc_frequ*	0	0 fclk_int/4 (use as default, if Vcharger>6V) 1 fclk_int/8 (use as default, if Vcharger<6V)

Table 29 – Step down charger Registermap

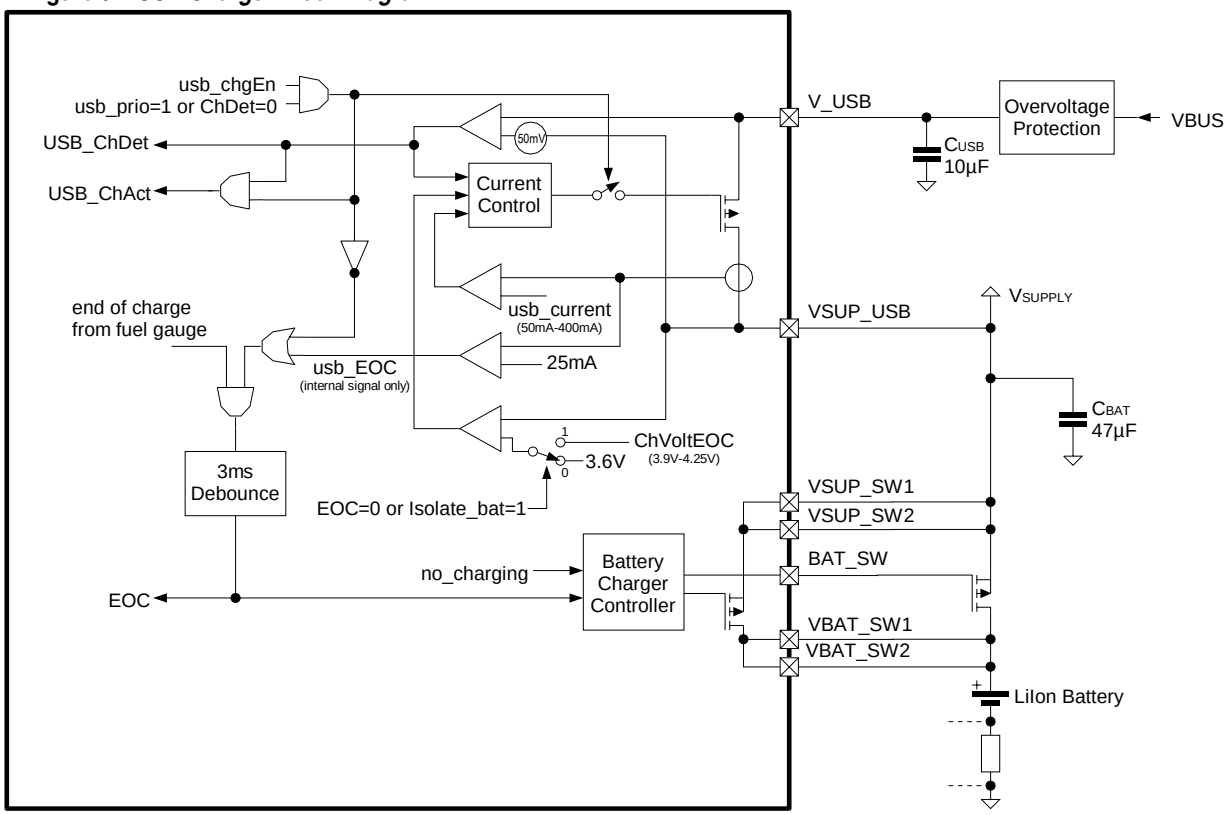
Register Definition	Addr.[7]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0

[6] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence
[7] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

Register Definition	Addr.[7]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Step down charger control	34	00h		sd3_dis_curmin	sd2_dis_curmin	sd1_dis_curmin				sdc_freq u

7.8 USB Charger

Figure *9 – USB Charger Block Diagram*



The AS3654 serves an integrated USB charger for Li+ batteres. The USB Charger is a current and voltage limited charger, which can be used to charge Li+ batteries directly from the USB supply. The voltage limit is set by the register ChVoltEOC (3.9V – 4.25V in 50mV steps; identical for USB charger and step down charger) and the current limit is set by the register usb_current (50mA to 400mA in 50mA steps).
For USB charging, it is recommended to start with a current limit of 100mA and after negotiates via the USB bus (this has to be done by e.g. the uProcessor directly) a different current setting can be set to speed up charging (e.g. 400mA).
If Bit usb_chgEn=1 in the Boot ROM is set, VSUPPLY can start up with USB supply allowing startup from the USB supply.

If ChEn=1 and chdet=1 and usb_prio=0 the usb_charger will be deactivated automatically. (The Battery charger overrides the USB charger). If usb_prio=1, both chargers (usb charger and step down charger) can operate in parallel (the voltage on VSUPPLY is always defined by the higher voltage of the two chargers).

End of charge of the USB charger is reached, if the current through the USB charger falls below 25mA. Please note that this current includes the added current to the battery and the system. If the current to the system is too high, the end of charge condition should be detected by measuring the current through the battery with the fuel gauge. After this detection, the no_charging bit should be set. Then the voltage on the battery should be monitored by the ADC to restart the charger if the voltage on VBAT drops and a new charging cycle should be triggered.

Table *30 – USB-Charger Bit definitions*

Name	Default	Access	Description
no_charging	ROM (1b)		0 Normal battery charger operation (usb charger and/or step down charger) 1 USB and Step down charger is supplying VSUPPLY, but battery switch is open USB charger regulates to ChVoltEOC voltage. Step down charger regulates to ch_voltage
usb_ChargerCurrent			
usb_Current	ROM (001b)	R/W	Sets the USB current. (000)b 50mA (001)b 100mA (default) (010)b 150mA (011)b 200mA (100)b 250mA (101)b 300mA (110)b 350mA (111)b 400mA
usb_prio	ROM (0b)	R/W	Sets the USB charger priority 0 USB charging possible if Chdet=0 only (battery step down charger is off) default 1 USB charging possible with both charger on
usb_chgEn	ROM (1b)	R/W	ON/OFF control of USB charger
USB_Chact		R	set to 1 if charger is active
USB_Chdet		R	Set to 1 if charger is detected

Table 31 – Step down charger Registermap

Register Definition	Addr.[8]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
USB ChargerControl	07	ROM (52h)	ext_batsw_en	No_charging	usb_prio	usb_chgEn	usb_Current			
ChargerStatus_usb	67	NA					batsw_on	batsw_mode	USB_ChAct	USB_ChDet

Charger Detection:
The Charger will be detected by comparison of the V_USB voltage with the Vsupply voltage.
If V_USB is 50mV higher than VSupply voltage, the USB_ChDet is set to 1.

[8] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

7.9 Battery Charge Controller

The AS3654 device serves as a standalone battery charge controller supporting rechargeable lithium ion (Li+) and nickel metal hydride (NiMH) batteries. Requiring only a few external components, a full-featured battery charger with a high degree of flexibility can easily be realised. The main features of the controller are:

- Charge adapter detection
- Charging of deeply discharged batteries
- Low current (trickle) charging with 60min timeout
- Real constant current charging by regulation of the battery current instead of the charge current
- Fast charging
- 2 different top-off charging modes: Pulse charging and constant voltage charging
- Fuel gauge enables highly accurate remaining capacity estimation of the battery
- Overvoltage protection for charge adapter input and main battery
- Battery presence indication
- Operation without battery
- Reverse polarity and short protection

Figure 10 – Charger Block Diagram with optional reverse polarity and short protection

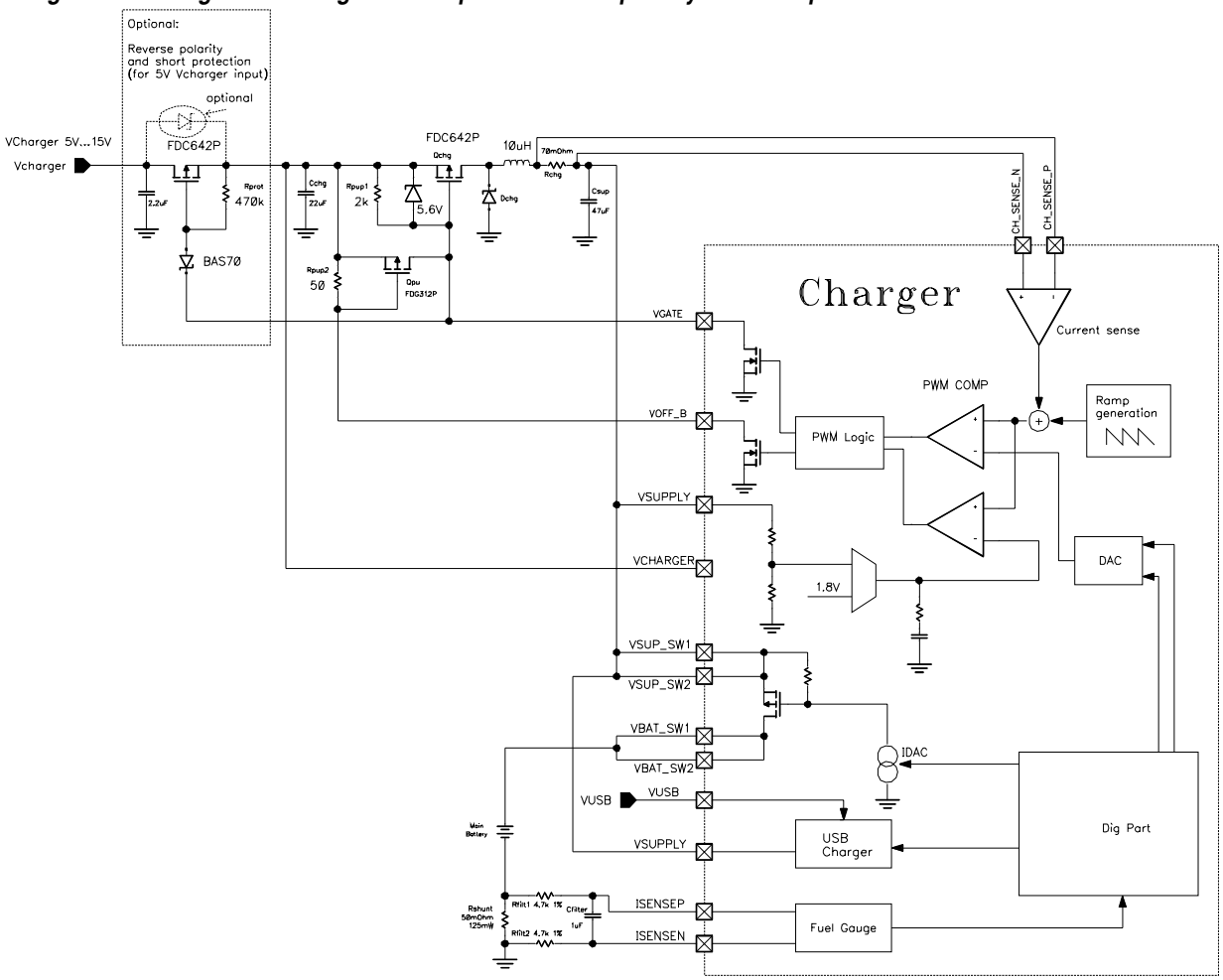


Figure 11 – Charger Block Diagram for voltages >15V (Protection up to 50V; minimum Vcharger voltage 8V)

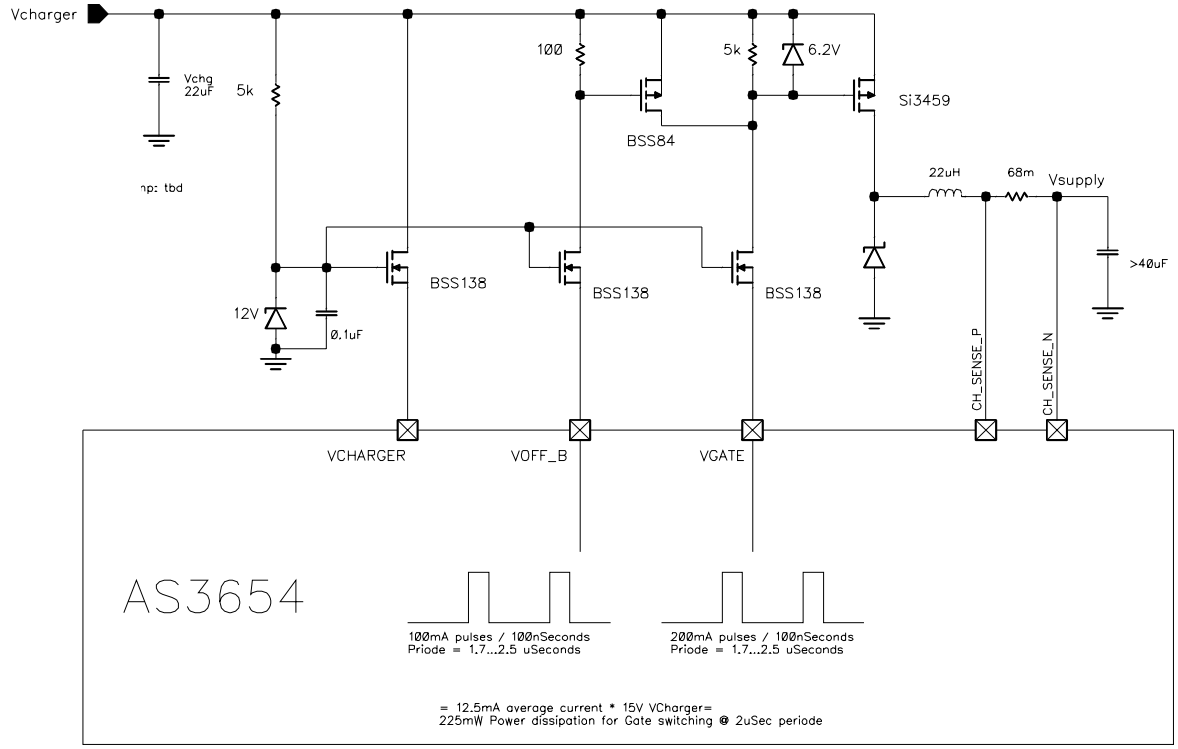
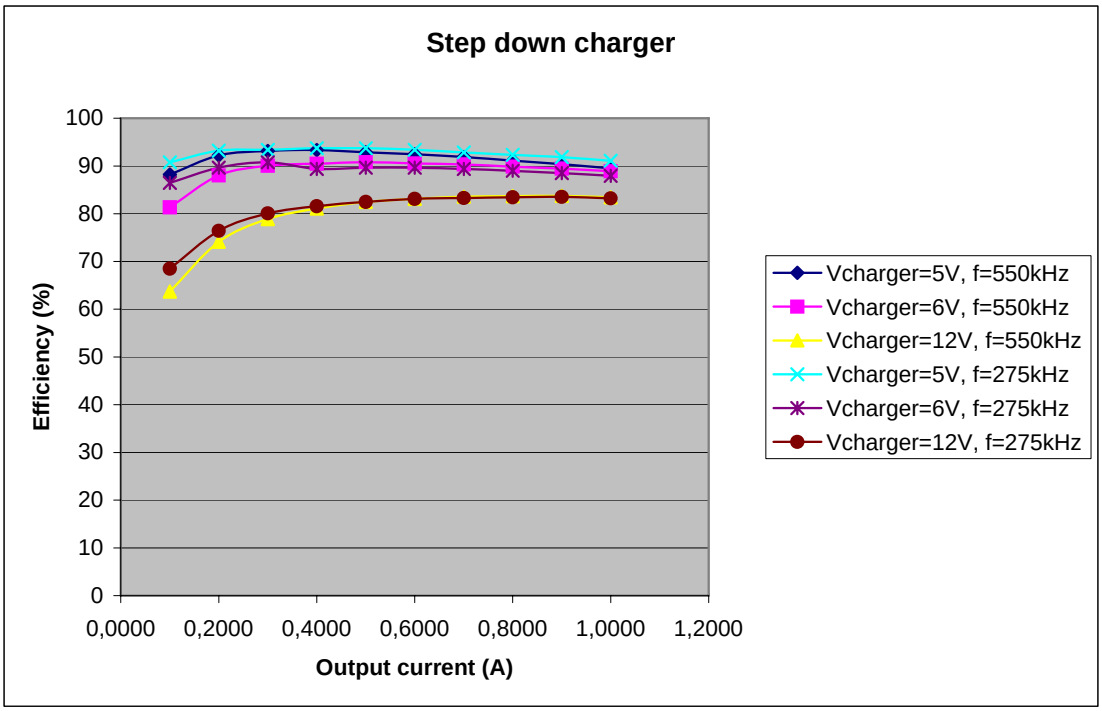


Table 32 – Charger External Components

Symbol	Component	Value	Note
Q_{chg}	P-channel MOSFET	Si1403 or FDC642P or similar	
Q_{pu}	P-channel MOSFET	BSS84 or FDG312P or similar	
R_{pup1}	Pull-up resistor1	2kΩ ± 5%	
R_{pup2}	Pull-up resistor2	100Ω ± 5%	for Qpu=BSS138
		50Ω ± 5%	for Qpu=FDG312P
L_{chg}	Inductor for charging	10µH	5V or 6V Vcharger input
		22uH	12V Vcharger input
D_{chg}	Diode	Tbd	
R_{chg}	Current sense resistor charger	70mΩ ± 5%, 125mW	e.g. Vishay Dale WSL0805 series
R_{sense}	Current sense resistor	50mΩ ± 1%, 125mW for $I_{VBAT,DC}$<1.5A	e.g. Vishay Dale WSL0805 series
$R_{filt1,2}$	Filter resistor	4.7kΩ ± 1%	Can be omitted if fuel gauge and charger functionality is not used
C_{filt}	Filter capacitor	1µF ± 20%, X5R or X7R dielectric	
C_{chrg}	Bypass capacitor on charger pin	1µF ± 20%, X5R or X7R dielectric + 22uF ± 20%, Tantal dielectric	
C_{bat}	Minimum total capacitance parallel to Vsupply	22µF± 20%, X5R or X7R dielectric	10 µH inductor
		47µF± 20%, X5R or X7R dielectric	22 µH inductor

Figure *12 – Step down charger Efficiency (Measured)*

VSupply=4.4V



7.9.1 Charge Controller Operating Modes and Building Blocks

Charge adapter detection

The charge controller uses an integrated detection circuit to determine if an external charge adapter has been applied to the VCHARGER or V_USB pin. If the adapter voltage exceeds the supply voltage at pin V_SUPPLY5 by V_{CHDET} the *ChDet or USB_CHDet* bit in the *Charger Status* register will be set. The detection circuit will reset the charge controller (*ChDet* or USB_CHDet is cleared) as soon as the voltage at the VCHARGER or USB_CHDet pin drops to only V_{CHMIN} above the battery voltage. In case the AS3654 device is reset the charge controller will also be reset, even if a charge adapter is applied to the VCHARGER or V_USB pin.

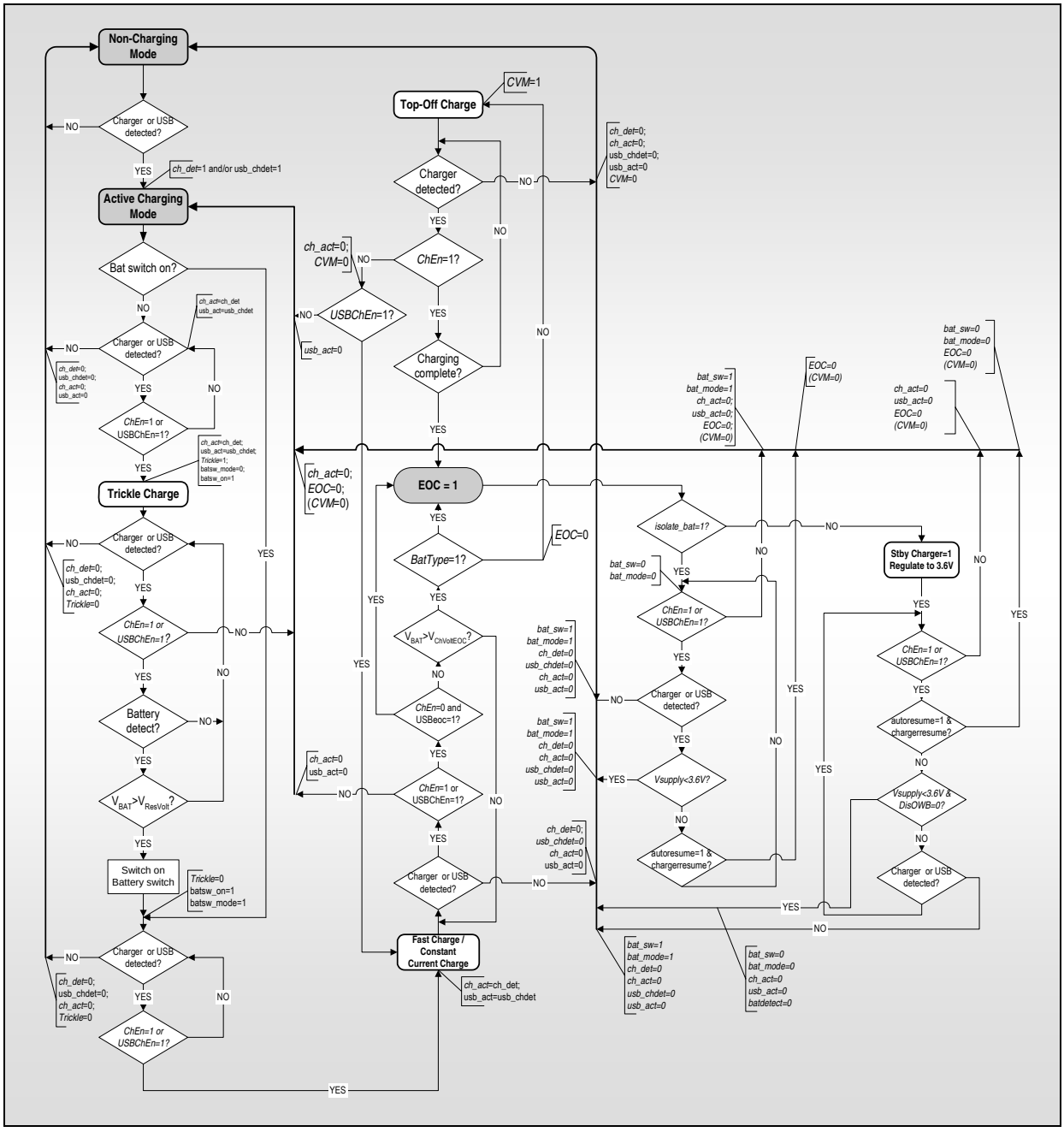
Charging deeply discharged batteries

To be able to charge even completely discharged batteries the AS3654 device contains an internal voltage regulator that uses the voltage of the external charge adapter at pin VCHARGER or V_USB to generate a bootstrap voltage V_{2_5V} to supply the internal circuitry necessary for charging. As soon as the battery voltage exceeds 2.5V, the bootstrap regulator is disabled and the battery voltage will be used to generate the internal supply voltage to supply the charger circuitry.

Low current (trickle) charging

Trickle charge mode is started when an external charge adapter has been detected and ChEn or usb_chgEn is set, and the battery voltage at pin V_BAT is below the ResVoltRise threshold $V_{RESRISE.}$; The Battery switch is open in that case (batsw_on=1 batsw_mode=0). Bits *ChAct* and/or USBChAct and *Trickle* will be set in the *Charger Status* registers. In this mode the charge current into the battery will be limited to *TrickleCurrent* (set in the *Charger Current* register) by the battery switch to prevent undue stress on either the battery or any of the charger components in case of deeply discharged batteries. if Vsupply drops below $V_{trickleoff}$ threshold the trickle current is regulated down, to keep the Vsupply voltage up, even with an current limited charger (e.g.:USB charger). Once $V_{RESRISE}$ has been exceeded, the battery switch will be closed and the charge controller will proceed to constant current charge mode. The Vsupply voltage of the step down charger will be set to Vcurr_preset to prevent undervoltage on vsupply during the transition between Trickle and constant current charging. (*Trickle* is cleared). In case the battery voltage does not exceed $V_{RESRISE}$ within $t_{TRICKLE,MAX}$ after charging has been started, trickle_tmax interrupt will be generated and trickle charging will be stopped. Trickle charging can be started again by writing trickle_tmax=0 in the charger_control1 register.

Figure 13 – Charger Flow Chart



Constant current charging

Constant current charging is initiated by setting bit *ChEn and/or USBChEn* in the *Charger Control* register, and resetting the No_charging bit. Note that *ChEn* and/or USBChEn should be set by default to enable operation of the device without a battery connected to the system. The *ChAct and/or USBChAct* bit is set when the charger has started, and the charge current into the battery will be limited to *ConstantCurrent* (set in the *Charger Current* register) by the battery charge controller. When the battery approaches full charge, its instantaneous voltage will exceed the charge termination threshold V_{CHOFF}. V_{CHOFF} depends on the battery chemistry selected by bit *BatType* and on the *ChVoltEOC* value in case a Li+ battery has been selected (*BatType*='0'). Depending on the battery type, the charging action will either be terminated (*BatType*='1'; bit *EOC* will be set) or a top-off charge mode will be started (*BatType*='0'; bit *CVM* will be set). By default the charge controller will be configured for charging lithium based batteries (*BatType*='0'), battery type determination must be performed by the system host.

Pulse charging

Pulse charge mode is initiated and the *CVM* bit will be set when the V_{CHOFF} threshold has been exceeded for the first time and bit *Pulse* is set. If the battery voltage at pin V_BAT is below the V_{CHOFF} threshold the battery switch will be switched on for a minimum on-time set by *TPON* in the *Charger Timing* register. If the battery voltage is below V_{CHOFF} at the end of the minimum on-time the battery switch will remain switched on until the battery voltage exceeds V_{CHOFF}. At this moment the battery switch is switched off for at least the minimum off-time set by *TPOFF*, and the battery switch will only be switched on again when the battery voltage falls below V_{CHOFF}. Note that unless the *Fast* bit is set the charge controller will limit the charge current to the value set by *ConstantCurrent* in the *Charger Current* register during on-pulses; if *Fast* is set, the charge current will not be limited during on-pulses.

At the beginning of the pulse charging procedure the battery switch will be operated at a duty cycle close to 100%. Towards the end of the charging cycle the charger will be switched off for long periods of time between short on-pulses. Eventually, the off-time will become longer than *TPOFFMAX*, and the charging cycle is terminated (*EOC* is set). In the following the charge controller starts the EOC operation.

Constant voltage charging

Constant voltage charge mode is initiated and the *CVM* bit will be set when the V_{CHOFF} threshold has been exceeded for the first time and bit *Pulse* is not set. In the following the charge controller will act to regulate the battery voltage to a value set by *ChVoltEOC* in the *Charger Config* register.

The charge current is monitored during constant voltage charging. It will be decreasing from its initial value during constant current charging and eventually drop below the value set by *TrickleCurrent* in the *Charger Current* register. If the measured charge current is less than or equal to *TrickleCurrent* and the battery voltage is larger than V_{CHRES}, the charging cycle is terminated and *EOC* is set . Then the charge controller starts the EOC operation.

For the USB charger, the EOC is set if the voltage through the USB charger drops below 25mA.

If both chargers are operating, both chargers have to reach EOC (End of charge) to continue with EOC operation.

EOC operation

There are two possibilities:

1. if **isolate_bat=1** the battery switch will be switch off and the battery charger regulates to its highest voltage $V_{chlimit.}$ The USB_charger regulates to its maximum voltage, which is defined by V_{CHOFF}. The advantage of this mode is a longer lifetime of the Li+ battery, because there is no discharging after the EOC condition. If autoresume=1 and the battery voltage drops below V_{CHRES} the battery charger continues charging, by checking in trickle charge mode, if there is a battery connected, and then starting with constant voltage or fast charging.
2. If **isolate_bat=0** the battery switch remains closed and the power to the system is supplied by the battery. The battery charger and the USB charger regulates to V_{EOC}, in case the battery is removed. If autoresume=1 and the battery voltage drops below V_{CHRES} the battery charger continues charging, by checking in trickle charge mode, if there is a battery connected, and then starting with constant voltage or fast charging.

Battery Detection and Restart of Charging:

If the battery voltage drops below V_{CHRES} and the bit AutoResume is set, the battery detection is started. The battery switch will be switched into current source mode and V_{SUPPLY} will be regulated to $V_{chlimit}$ (Step Down Charger) and V_{CHOFF} (USB charger) (regulation is performed to the higher of the two voltage settings and depends on the availability of the USB and VCHARGER supply). The AS3654 measured the battery current with the fuel gauge in this mode. If there is no current, the AS3654 is kept in this state and the bit NoBat is set. Otherwise the bit NoBat is cleared and the charger and the AS3654 continues with 'Constant Current Charging' mode.

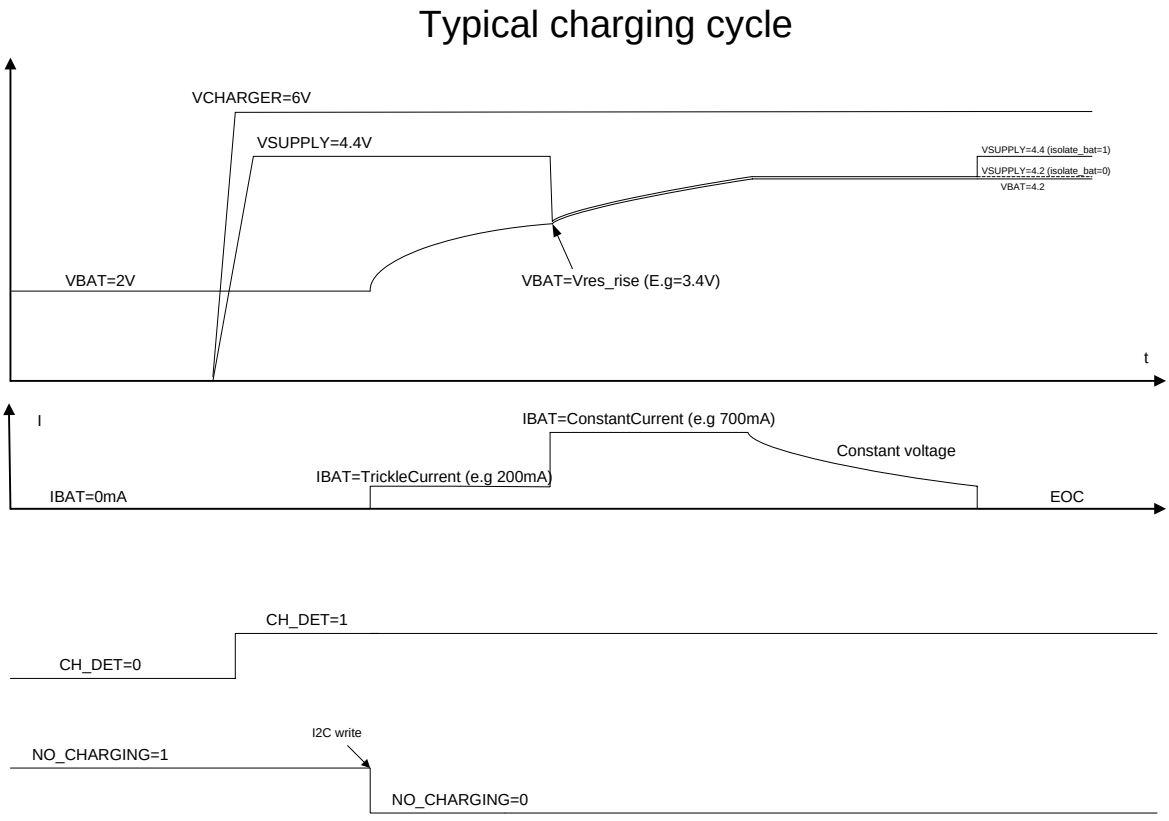


Table 33 – Charger Characteristics

V_{VBAT}=3.0…5.5V; T_{amb}=–20…+85°C; unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{CHARGER}$	VCHARGER operating range	5.0		15.0	V	For input voltage higher than 15V see above protection circuit; for chargers with input voltages down to 4.5V see: 'Application Note for DC/DC Step down Charger for Chargers Supplying 4.5V to 5.5V'
V_{CHDET}	Charge adapter detection threshold	50	75	105	mV	Hysteresis is > 40mV; for USB and step down charger
V_{CHMIN}		0	20	35		
$I_{STARTmax}$	Maximum load current during startup on Vsupply		5		mA	
V_{UVLO}	Undervoltage lockout threshold	–3%	2.7…3.4	+3%	V	Value is set by *ResVoltRise* in the *Battery Voltage Monitor* register
V_{CHOFF}	Charge termination threshold	–0.06	3.90…4.25	+0.06	V	Li+ battery (*BatType*='0'); value is set by *ChVoltEOC* in the *Charger Config* register
			4.7			NiMH battery (*BatType*='1')
V_{CHRES}	Charger resume voltage		3.85…4.20		V	Value is set by *ChVoltResume* in the *Charger Config* register. **Do not set V_{CHRES} higher than V_{CHOFF}!**
V_{curr_preset}	Charger constant current pre-set voltage		$V_{RESRISE}$ +100mV		V	
V_{EOC}	Charger EOC voltage		3.60		V	If isolate_bat=0; to prevent a system reset if the battery is removed in EOC operation
$t_{TRICKLE,MAX}$	Trickle charge timeout		60		min	

Table 34 – Charger Register Overview

Register Definition	Addr.[9]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
USB ChargerControl	07	ROM (52h)	ext_batsw_en	No_charging	usb_prio	usb_chgEn	usb_Current			
ChargerControl1	08	ROM (41h)	Isolate_bat	Boost	trickle_tmax	Pulse	Auto Resume	~~Fast~~	BatType	ChEn
Charger Config	10	ROM (26h)	ChVoltResume			DisOWB	DisBDet	ChVoltEOC		
ChargerTiming	11	ROM (4bh)	TPOFFMAX		TPOFF			TPON		
ChargerStatus	66	NA		NoBat	EOC	CVM	Trickle	Resume	ChAct	ChDet
ChargerStatus_usb	67	NA					batsw_on	batsw_mode	USB_ChAct	USB_ChDet

Table 35 – Charger Status Register

Address 5; Read only access; register is reset at power-on-reset only.

Bit	Symbol	Default	Description
0	*ChDet*	NA	Bit is set when external charge adapter has been detected on pin VCHARGER
1	*ChAct*	NA	Bit is set when step down charger is operating (independent of Reg. bit no_charging)
2	*Resume*	NA	Bit is set when battery voltage has dropped below resume level
3	*Trickle*	NA	Bit is set when charger is in trickle charge mode
4	*CVM*	NA	Bit is set when charger is in top-off charge mode (constant voltage mode)
5	*EOC*	NA	Bit is set when charging has been terminated. Bit is cleared automatically when *ChEn* is cleared, no_charging ist set or charging is resumed.
6	*NoBat*	NA	Bit is set when battery detection circuit indicates that no battery is connected to the system. Detection is started after EOC and if bit autoresume=1 only. Bit is cleared automatically when a battery is connected, when *DisBDet* is set and/or when *ChEn* is cleared.

Table 36 – Charger Control1 Register

Address 8; R/W access; register is reset at power-on-reset only. Default value after reset: C1h.

Bit	Symbol	Default	Description
0	*ChEn*	ROM(1b)	0 Disable step down charger (Independent of bit no_charging) 1 Enable step down charger (default) (Independent of bit no_charging)
1	*BatType*	ROM(0b)	0 Li+ battery 1 NiMH battery
2	*nc*	ROM(0b)	
3	*AutoResume*	ROM(0b)	0 Charging does not restart automatically in EOC when bit *Resume* is set. 1 Charging will restart automatically in EOC when bit *Resume* is set.
4	*Pulse*	ROM(0b)	0 Select constant voltage charging mode (default recommended) 1 Select pulse charging mode
5	*trickle_tmax*	ROM(1b)	0 Read: no timeout reached Write: reset trickle_tmax state 1 $t_{TRICKLE,MAX}$ timeout reached and trickle charging stopped
6	*Boost*	ROM(**1b**)	**0 Don't use** **1 Normal operation of Trickle charger use**

[9] Register address codes 00 – 31 are identical to Boot-ROM address codes

ROM-adr. 25-30…Power1 Control states at startup sequence

Bit	Symbol	Default	Description
7			

Table 37 – Battery Voltage Monitor Register

Address 9; R/W access; register is reset at power-on-reset only. Default value after reset: ROM.

Bit	Symbol	Default	Description
2…0	*ResVoltRise*	ROM (101b)	This value determines the reset level $V_{RESRISE}$ for rising V_{VBAT}. It is recommended to set this value at least 200mV higher than $V_{RESFALL}$. 000b $V_{RESRISE}$=2.7V 100b $V_{RESRISE}$=3.1V 001b $V_{RESRISE}$=2.8V 101b $V_{RESRISE}$=3.2V 010b $V_{RESRISE}$=2.9V 110b $V_{RESRISE}$=3.3V 011b $V_{RESRISE}$=3.0V 111b $V_{RESRISE}$=3.4V
5…3	*ResVoltFall*	ROM (011b)	This value determines the reset level $V_{RESFALL}$ for falling V_{VBAT}. It is recommended to set this value at least 200mV lower than $V_{RESRISE}$. 000b $V_{RESFALL}$=2.7V 100b $V_{RESFALL}$=3.1V 001b $V_{RESFALL}$=2.8V 101b $V_{RESFALL}$=3.2V 010b $V_{RESFALL}$=2.9V 110b $V_{RESFALL}$=3.3V 011b $V_{RESFALL}$=3.0V 111b $V_{RESFALL}$=3.4V
6	SupResEn	ROM (0b)	0 A hard reset is generated if Vsupply falls below 2.7V. (If V_{VBAT} falls below $V_{RESFALL}$ only an interrupt is generated (if enabled) and the uProcessor can shut down the system) 1 Vsupply Voltage below $V_{RESFALL}$ generates a reset
7			

Table 38 – Charger Timing Register

Address 11; R/W access; register is reset at power-on-reset only. Recommended value after reset: ROM 4Bh.

Bit	Symbol	Default	Description
2…0	*TPON*	ROM	Sets the minimum on-time in pulse charge mode from 137.3ms…1098ms in steps of 137.3ms. Default is 011b = 549.2ms.
5…3	*TPOFF*	ROM	Sets the minimum off-time in pulse charge mode from 68.65ms…549.2ms in steps of 68.65ms. Default is 001b = 137.3ms.
7…6	*TPOFFMAX*	ROM	Sets the maximum off-time in pulse charge mode before charging is terminated. 00b 4 x *TPON* (yields 1/5 of the charging current in constant current mode) 01b 9 x *TPON* (yields 1/10 of the charging current in constant current mode) 10b 19 x *TPON* (yields 1/20 of the charging current in constant current mode) 11b no termination (not recommended)

Table 39 – Charger Config Register

Address 10; R/W access; register is reset at power-on-reset only. Recommended value after reset: ROM ,26h.

Bit	Symbol	Default	Description
2…0	*ChVoltEOC*	ROM	Sets the end-of-charge voltage level V_{CHOFF}. 000b 3.90V 100b 4.10V 001b 3.95V 101b 4.15V 010b 4.00V **110b 4.20V (default)** 011b 4.05V 111b 4.25V
3	*DisBDet*	ROM	0 Enable battery presence indication(default) 1 Disable battery presence indication. **Don't use**
4	*DisOWB*	ROM	0 Enable "operation without battery" feature(default) 1 Disable "operation without battery" feature. **Don't use**
7…5	*ChVoltResume*	ROM	Sets the resume voltage level V_{CHRES}. 000b 3.85V 100b 4.05V 001b 3.90V(default) 101b 4.10V

Bit	Symbol	Default	Description
			010b 3.95V 110b 4.15V 011b 4.00V 111b 4.20V

7.9.2 Fuel Gauge

The fuel gauge circuit enables remaining capacity estimation of the battery by tracking the net current flow into and out of the battery using a voltage-to-frequency converter.

Voltage-to-Frequency Converter

The voltage-to-frequency (VFC) converter constantly monitors the voltage drop across an external current sense resistor R_{sense} connected in series between the negative battery terminal and ground. The use of an additional external RC lowpass filter is highly recommended. Using two 4.7kΩ resistors ($R_{filt1,2}$) and a 1µF ceramic capacitor (C_{filt}), the filter cut-off is approximately 16.9 Hz. This filter will capture the effect of most spikes, and will thus allow the current accumulators to accurately reflect the total charge that has gone into or out of the battery.

The key building block of the VFC is an integrator. It will integrate the voltage V_{SNS} across input pins ISENSP and ISENSN. If V_{SNS} is positive (battery is charged), the output voltage of the integrator increases; a negative input voltage (battery is discharged) will cause the integrator output voltage to decrease.

Table 40 – Fuel Gauge parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{CLK}	Internal reference clock		$f_{clk\_int}/2$		MHz	internal CLK frequency/2 Programmable: 0.8 to 1.15 MHz
f_{VFC}	Sample frequency		$f_{CLK}/59$		Hz	
V_{ISENSP} V_{ISENSN}	Input voltage	-0.1		0.1	V	
Z_{ISENSP} Z_{ISENSN}	Input impedance	4.67			MΩ	
A_{VFC}	(Dis)Charge gain		91.0		Hz / V	f_{CLK} = 1.1MHz
FR_{VFC}	Fundamental rate		3.05		µVh	
	Supply voltage gain coefficient		tbd		% / V	
	Temperature gain coefficient		tbd		% / °C	
V_{OFF}	Uncompensated offset voltage	-500		500	µV	
$V_{OFF,COMP}$	Compensated offset voltage	-50	±10	50		Offset compensation with CalMod=1 only. Don't use CalMod=0

Charge Current Accumulator

The output signals of the charge count dividers are used as inputs for the charge current accumulator that is realised as a 15-bit up-down counter with separate inputs for incrementing and decrementing the counter. An additional sign bit indicates the polarity of the counter value that is maintained in two's complement format. The current accumulator is updated at a rate equivalent to one count per 3.05µVh, which is equivalent to one count per 61.03µAh when using a 50mΩ current sense resistor. It will roll over beyond (7FFF)h when incremented and (0000)h when decremented, and the value given by the counter will be ambiguous in that case. It is the responsibility of the host to read the counter before rollover occurs.

The content of the charge current accumulator will be transferred into the *DeltaCharge* register when the *UpdReq* bit in the *FuelGauge* register has been set. The update of the register has to be synchronised to the sample clock f_{VFC} and can take up to 1.5 clock cycles (max. 2.5µs). After the registers have been updated successfully, the *UpdReq* bit is cleared automatically and the charge current accumulator together with the sign bit will be reset.

Elapsed Time Counter

The sample clock f_{VFC} of the fuel gauge circuit is fed to a 14-bit clock count divider. Its output signal is used as a clocking signal for the 16-bit elapsed time counter, resulting in an equivalent rate of 1.1379 counts per second (4096.60 counts = 1 hour). The elapsed time counter will rollover beyond (FFFF)h, and the value given by the counter will be ambiguous in that case. It is the responsibility of the host to read the counter before rollover occurs.

The content of the elapsed time counter will be transferred into the *ElapsedTime* register when the *UpdReq* bit in the *FuelGauge* register has been set. The update of the register has to be synchronised to the sample clock f_{VFC} and can take up to 1.5 clock cycles (max. 2.5µs). After the registers have been updated successfully, the *UpdReq* bit is cleared automatically and the elapsed time counter will be reset.

Offset Calibration Mode

Although the VFC compensates for the offset of the integrator the fuel gauge features an additional offset calibration mode to enhance the measurement accuracy even further. By setting the *CalReq* bit in the *FuelGauge* register the integrator is reset and the offset calibration mode is activated. The charge count dividers are bypassed during offset calibration to allow a faster calibration procedure with adequate resolution. The offset is accumulated during 16 clocks of the elapsed time counter, the resulting offset calibration value *FGOffCal* has a resolution of 3.05µV and is transferred to the *DeltaCharge* register. The *CalReq* bit is cleared automatically after the calibration has completed successfully and *FGOffCal* has been written to the register.

Please note that offset calibration is not possible while the charger is active. If the *CalReq* bit is set while the charger is active the calibration will start automatically after the charger has been disabled by clearing the *ChEn* bit or if the external charge adapter has been removed. If during an offset calibration procedure the charger is enabled the offset calibration mode is terminated, the *CalReq* bit is cleared, the current value of the elapsed time counter is transferred to the *ElapsedTime* register and the *DeltaCharge* register is loaded with (FFFF)h.

Calculation of Battery Status

The host system can calculate all the parameters necessary for estimating the remaining battery capacity by evaluating *ElapsedTime*, *DeltaCharge* and *FGOffCal*.

Calculating Elapsed Time

The host system can evaluate the change in time Δt by setting the *UpdReq* bit in the *FuelGauge* register and reading *ElapsedTime* after *UpdReq* has been automatically cleared. The change in time in seconds is given by:

$$\Delta t = ElapsedTime \times 3600 / 4096.60 \text{ [s]} \quad (1)$$

Note that the absolute accuracy of Δt is directly related to the absolute accuracy of the internal reference oscillator. To cancel the error associated with the accuracy of the oscillator, a correction factor CV can be introduced. CV can be evaluated by comparing the change in time calculated by (1) with some reference value Δt_{REF} obtained from a RTC or measured during system calibration. CV is given by:

$$CV = \Delta t_{REF} / \Delta t \quad (2)$$

By multiplying Δt and CV the correct value for the change in time can be calculated:

$$\Delta t_{CORR} = CV \times \Delta t \text{ [s]} \quad (3)$$

Calculating Average Current

The host system can calculate the average current during the last time period by setting the *UpdReq* bit in the *FuelGauge* register and reading *DeltaCharge* and *ElapsedTime* after *UpdReq* has been automatically cleared. Together with *FGOffCal* determined during offset calibration mode the average current is given by:

$$I_{AVG} = DeltaCharge / (\Delta t \times A_{VFC} \times R_{sense}) - FGOffCal \times 3.05\mu V / R_{sense} \text{ [A]} \quad (4)$$

Δt is the change in time in seconds calculated by (1), A_{VFC} is the gain of the VFC in Hz/V, R_{sense} is the value of the sense resistor in Ω and *FGOffCal* is the offset calibration value. As *DeltaCharge* and Δt both are proportional to the oscillator frequency, no correction factor needs to be introduced in the formula.

Calculating Accumulated Current

Accumulated current is used to calculate the absolute remaining capacity of the battery. It is given by:

$$I_{ACC} = I_{AVG} \times \Delta t_{CORR} \text{ [As]} \quad (5)$$

Calculating the Remaining Capacity

Remaining capacity is the entire goal of fuel gauging. It is given by:

$$RC = RC + I_{ACC} \text{ [As]} \quad (6)$$

Calculating the Time to Empty

The time to empty is calculated from the average current I_{AVG} given by (4). The longer the time period for which I_{AVG} is calculated, the more accurate the value for I_{AVG} and therefore the estimated time to empty will be. It is given by:

$$TTE = RC / I_{AVG} \text{ [s]} \quad (7)$$

Table *41 – Fuel Gauge Register definitions*

Register Definition		Content							
Name	**Addr.**	b7	b6	b5	b4	b3	b2	b1	b0
FuelGauge	12					CalMod	CalReq	UpdReq	FGEn
$DeltaCharge_{MSB}$	68	sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
$DeltaCharge_{LSB}$	69	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
$ElapsedTime_{MSB}$	70	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
$ElapsedTime_{LSB}$	71	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Table *42 – Fuel Gauge Bit definitions*

Name	Default	Access	Description
FuelGauge – ROM default (01)h			
FGEn	ROM	R/W	0 Disable Fuel Gauge 1 Enable Fuel Gauge (default)
UpdReq	0b	R/W	This bit controls the update of the *DeltaCharge* and *ElapsedTime* registers. When set, the bit is cleared automatically after the registers have been updated successfully. Bit should not be set to "0" by the host! 0 Update of registers complete (default) 1 Request update of registers
CalReq	0b	R/W	This bit controls the offset calibration. When set, the bit is cleared automatically after the calibration has completed successfully. 0 Calibration complete OR terminate offset calibration (default) 1 Request offset calibration
CalMod	0b	R/W	Sets the mode for offset calibration 0 Connect inputs to ground internally (default) 1 Use ISENSP and ISENSN (for testing purposes only)
DeltaCharge – read only			
DeltaCharge	(0000)h	R	The register is maintained in two's complement format with a resolution of 3.05μVh and a full-scale value of ±99.98mVh. When using a 50mΩ current sense resistor this is equivalent to a resolution of 61.03μAh and a full-scale value of 1.999Ah. Sign is set for negative values. Register will be updated after setting bit *UpdReq* to "1".
ElapsedTime – read only			
ElapsedTime	(0000)h	R	The elapsed time count is stored in the register with a resolution of 0.8788s and a full-scale value of 15.997 hours. Register will be updated after setting bit *UpdReq* to "1".

Table 43 – FG Registermap

Register Definition	Addr.[10]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
FuelGauge	12	ROM (01h)					CalMod	CalReq	UpdReq	FGEn
USB ChargerControl	07	ROM (52h)	ext_batsw_en	No_charging	usb_prio	usb_chgEn	usb_Current			
ChargerStatus_usb	67	NA					batsw_on	batsw_mode	USB_ChAct	USB_ChDet
$DeltaCharge_{MSB}$	68	NA	sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
$DeltaCharge_{LSB}$	69	NA	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
$ElapsedTime_{MSB}$	70	NA	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
$ElapsedTime_{LSB}$	71	NA	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

7.9.3 Charger Operation

The charger controls the battery current through the internal transistor between VSUP_SW1,2 and VBAT_SW1,2, the step down charger and the battery switch between VSUPPLY and VBAT. With this control the charger obtain all different operating modes.

Charge Current Regulator

The regulator is programmed by setting *TrickleCurrent* and *ConstantCurrent* in the *ChargerCurrent* register and yields a resolution of 0.625mV or 12.5mA when using a sense resistor of 50mΩ.

Table 44 – *Charge Current Regulator parameters*

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_{MEAS}	Measurement period		68.65		ms	f_{clk_int} = 2.2MHz
$I_{MEAS,LSB}$	Resolution of *InstCurCnt*		0.625		mV	

Table *45 – Charger Register map*

Register Definition	Addr.[11]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
ChargerCurrent	13	ROM (2Eh)	ch_voltage			ConstantCurrent			TrickleCurrent	

Table *46 – Charger Bit definitions*

Name	Default	Access	Description
ChargerCurrent – ROM			
TrickleCurrent	ROM	R/W	Sets the trickle current. Default is (01)b = 2.5mV x R_{sense}^{-1}. (00)b 1.25mV x R_{sense}^{-1} (01)b 2.50mV x R_{sense}^{-1} (10)b 5.00mV x R_{sense}^{-1} (default) (11)b 10.0mV x R_{sense}^{-1}

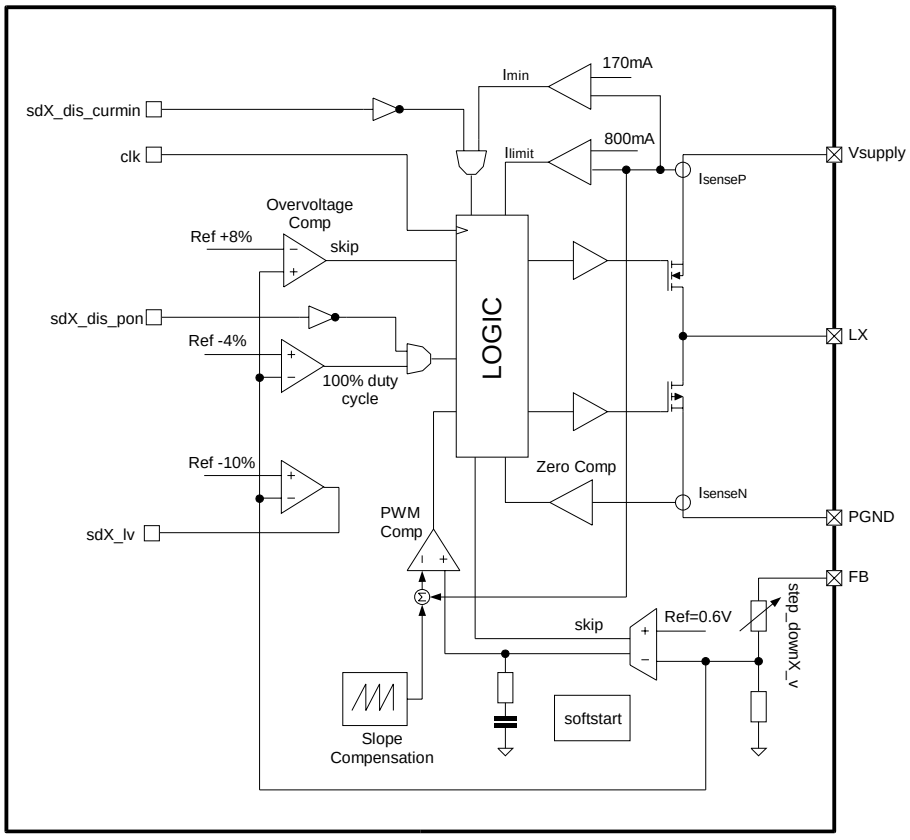
[10] Register address codes 00 – 31 are identical to Boot-ROM address codes ROM-adr. 25-30…Power1 Control states at startup sequence

[11] Register address codes 00 – 31 are identical to Boot-ROM address codes ROM-adr. 25-30…Power1 Control states at startup sequence

Name	Default	Access	Description
ConstantCurrent	ROM	R/W	Sets the charging current in constant current mode from (0mV…35mV) x R_{sense}^{-1} in steps of 5mV x R_{sense}^{-1}. Default is (011)b = 15mV x R_{sense}^{-1}.
Ch_voltage – ROM			
ch_voltage	ROM	R/W	Charger voltage after EOC and isolate_battery=1 (000)b 4.3V **(001)b 4.4V (default)** (010)b 4.5V (011)b 4.6V (100)b 4.7V (101)b 4.8V (110)b 4.9V (111)b 5.0V

7.10 Step Down DC/DC Converter

Figure *14 – Step Down DC/DC Converter Blockdiagram*



Functional Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the

whole output voltage range, up to an output current of 500mA, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

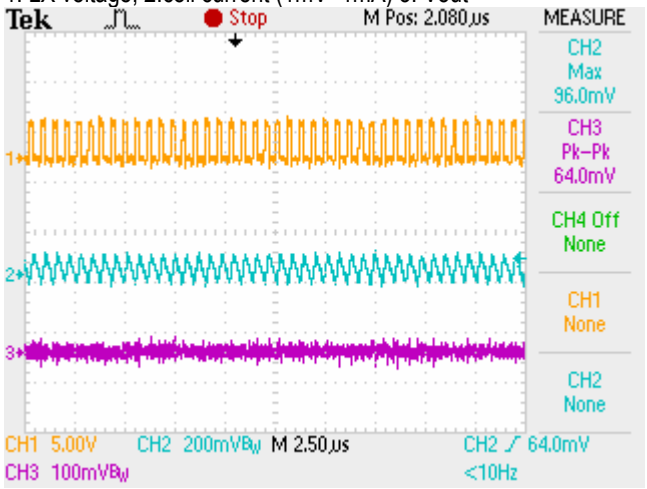
To allow optimised performance in different applications, there are bit settings possible, to get the best compromise between high efficiency and low input, output ripple:

Low ripple, low noise operation:

Bit settings:
sdX_dis_curmin=1
In this mode there is no minimum coil current necessary before switching off the PMOS. As result, the ON time of the PMOS will be reduced down to tmin_on at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences. Because of the inverted coil current in that case the regulator will not operate in pulse skip mode.

Figure *15 –sdX_dis_curmin=1 operation*

1: LX voltage, 2:coil current (1mV=1mA) 3: Vout

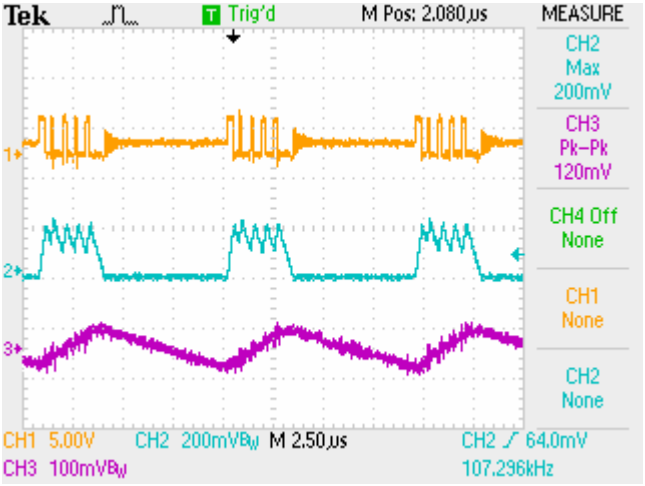


High efficiency operation (default setting):

Bit settings:
sdX_dis_curmin=0
In this mode there is a minimum coil current necessary before switching off the PMOS. As result there are less pulses at low output load necessary, and therefore the efficiency at low output load is increased. This results in higher ripple, and noisy pulse skip operation up to a higher output current.

Figure *16 –sdX_dis_curmin=0 operation*

1: LX voltage, 2:coil current (1mV=1mA) 3: Vout



It's also possible to switch between these two modes during operation:
E.g.:
sdX_dis_curmin=0: System is in idle state. No audio, RF signal. Decreased supply current preferred. Increase ripple doesn't effect system performance.

sdX_dis_curmin=1: System is operating. Audio signal on and/or RF signal used. Decreased ripple and noise preferred. Increased power supply current can be tolerated.

100% PMOS ON mode for low dropout regulation:

For low input to output voltage difference the sdX_dis_pon bit can be set, to allow 100% duty cycle of the PMOS transistor, if the output voltage drops by more than 4%.

Low power mode:

The sdX_lpo mode bit can be set all the time. This mode allows internal power down, of not used blocks during pulseskip mode, which results in a better efficiency at light output loads.

Inductor setting:

The step down regulator is optimised for 2.2µH at 2.2MHz and 4.7µH at 1.1MHz
Use the following settings for optimised operation:
sdX_4u7=1 for 4.7µH at 1.1MHz
sdX_4u7=0 for 2.2µH at 2.2MHz

Table *47 – Step Down DC/DC Converter parameters*

Symbol	Parameter	Min	TYP	Max	Unit	Note
V_{IN}	Input voltage	3.0		5.5	V	PIN VSUPPLY_1,VSUPPLY_2, VSUPPLY_3
V_{OUT}	Regulated output voltage	0.6		3.3	V	
V_{OUT_tol}	Output voltage tolerance	-50		+50	mV	output voltage <2.0V
		-100		+100	mV	output voltage >2.0V
I_{LIMIT}	Current limit		800		mA	

Symbol	Parameter	Min	TYP	Max	Unit	Note
R_{PSW}	P-Switch ON resistance			0.5	Ω	V_SUPPLYx=3.0V
R_{NSW}	N-Switch ON resistance			0.5	Ω	V_SUPPLYx=3.0V
I_{load}	Load current	0		500	mA	
f_{SW}	Switching frequency		2.2		MHz	sdX_frequ=0, f_{clk_int} =2.2MHz
			1.1		MHz	sdX_frequ=1, f_{clk_int} =2.2MHz
C_{out}	Output capacitor		10		µF	Ceramic
Lx	Inductor	2.2		4.7	µH	+/- 10% tolerance
η_{eff}	Efficiency		90		%	Iout=100mA, Vout=2.3V, Vsup.=3V
I_{VDD}	Current consumption		250 100 0.1		µA	Operating current without load Low power mode current Shutdown current
t_{MIN_ON}	Minimum on time		80		ns	
t_{MIN_OFF}	Minimum off time		40		ns	
$V_{LineReg}$	Line regulation		tbd		mV	Static
			tbd			Transient;Slope: t_r=10µs
$V_{LoadReg}$	Load regulation		tbd		mV	Static
			tbd			Transient;Slope: t_r=10µs

Table *48 – Step Up DC/DC Bit definitions*

Name	Default	Access	Description
sdX_dis_curmin	0	R/W	Step down curmin feature control 0: curmin feature enabled: Inductor current regulated to min 170mA. Higher efficency in low dropout and low output current operation. Higher output ripple and noise. 1: curmin feature disabled: Decreased efficiency in low dropout mode and at low output current. Small output ripple and noise.
sdX_dis_pon	0	R/W	Step down pon feature control 0: PON feature enabled: 100% duty cycle (pmos always on) if output voltage drops more than 4%. Increased output ripple in that operation. 1: PON feature disabled: Maximum dutycycle=1-(tmin_off*fsw)
sdX_lpo	0	R/W	Set always to 0 Step down low power mode: 0: Increased current consumption in pulseskip mode 1: Decreased current consumption in pulseskip mode
sdX_on	00h	R/W	Switch on/off the step down dc/dc converter
sdX_clkinvert	00h	R/W	Inverts the input clock of the step down converter
sdX_psw_on		R/W	Only if *buck_on* = 0, switch on PSW (0.5Ω PMOS)
sdX_dis_n		R/W	If '1' the synchron rectifier is disabled (NSW is always off)
sdX_4u7		R/W	If '1' optimise operation for 4.7µH inductor
sdX_nsw_on		R/W	Only if *buck_on* = 0, switch on NSW (0.5Ω NMOS)

Name	Default	Access	Description
sdX_v		R/W	Control the voltage selection for the step down DC/DC converter 000000 0.6 V … (LSB=50mV) 111000 – 11111 3.4 V
sdX_frequ		R/W	Select the step down frequency 0 f_{clk_int} (1.6MHz to 2.3 MHz) 1 $f_{clk\_int}/2$ (0.8MHz to 1.15 MHz)

7.10.1 Typical Performance Characteristics

Figure *17 – DC/DC step-down Efficiency (sdX_dis_curmin=0, sdX_lpo=0)*

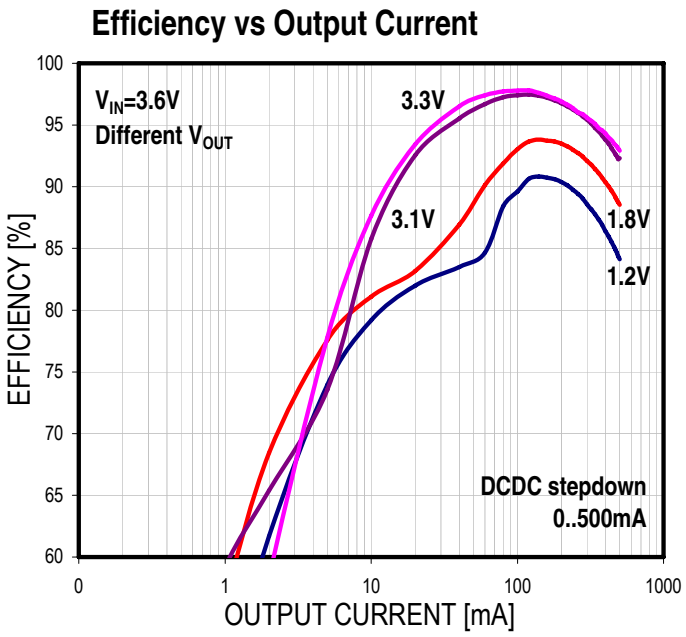


Figure *18 –PCB Layout recommendation*

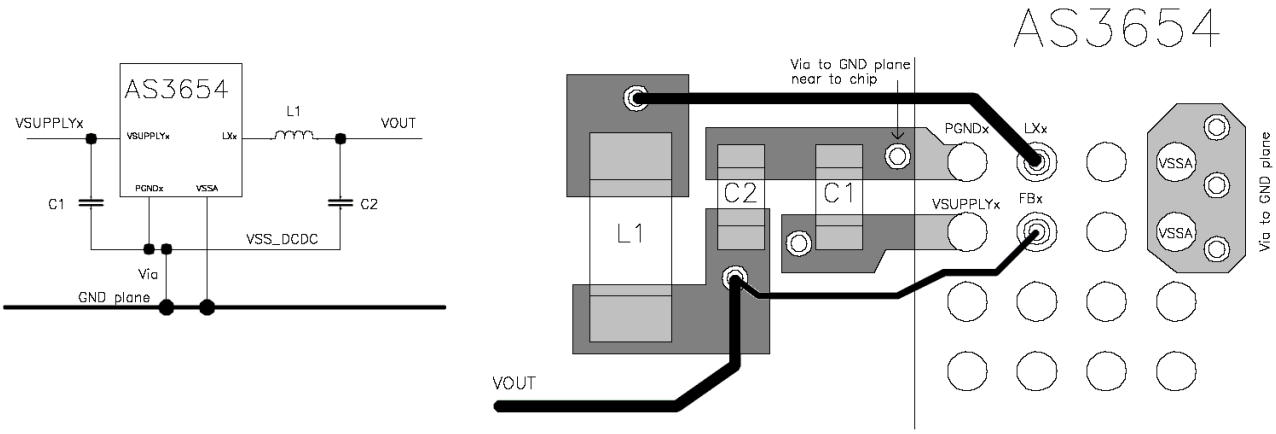


Table *49 – Step down Register map*

Register Definition	Addr.[12]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Reg Power1 Ctrl	23	ROM	cp_on	sd3_on	sd2_on	sd1_on	ldo_dig2_on	ldo_dig1_on	ldo_rf2_on	ldo_rf1_on
Step Down Control1	32	00h	sd2_nsw_on	sd2_4u7	sd2_dis_n	sd2_psw_on	sd1_nsw_on	sd1_4u7	sd1_dis_n	sd1_psw_on
Step Down Control2	33	00h	sd3_dis_pon	sd2_dis_pon	sd1_dis_pon	sdX_lpo	sd3_nsw_on	sd3_4u7	sd3_dis_n	sd3_psw_on
Step down charger control	34	00h		sd2_dis_curmin	sd2_dis_curmin	sd1_dis_curmin				sdc_frequ

7.11 Low Dropout Regulators (LDO)

The low dropout regulators are linear high performance regulators with programmable output voltage.

They are controlled by the following registers:

Table *50 – LDO's Bit definitions*

Name	Default	Acces	Description
ldo_rfX_on	Boot-ROM	R/W	Switch on control of RFX LDO (X = 1,2); **Important: Set rfX_sw=0 before setting ldo_rfX_on=1**
ldo_rfX_v		R/W	Control the voltage selection for LDO's VRF_1 – VRF_2 00000 1.85V … (LSB=50mV) 11111 3.40V
ldo_digX_v		R/W	Control the voltage selection for LDO's VDIG_1 and VDIG_2 (see *Table* 54 – Digital LDO (VDIG_1, VDIG_2) Programming voltage table)

[12] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

Name	Default	Acces	Description
rfX_sw	ROM	R/W	If '1' RFx-LDO is operating as High side switch (Ron=1Ω) , valid if *ldo_rfX_on*=0
rf1_swprot_en	ROM	R/W	If '1' current limitation is enabled, if RFx-LDO is operating as High side switch
rf1_lcurr_en	ROM	R/W	If '1' current limitation Ilimit=Ilimit/2 If '0' current limitation = Ilimit

7.11.1 RF LDO's (VRF_1 - VRF_2)

These LDO's are designed to supply sensitive analogue circuits like LNA's, Transceivers, VCO's and other critical RF components of cellular radios. Another application is the supply of audio devices or as a reference for AD and DA converters. The design is optimised to deliver the best compromise between quiescent current and regulator performance for battery powered devices.
Stability is guaranteed with ceramic output capacitors of 1µF +/-20% (X5R) or 2.2µF +100/-50% (Z5U) for RF2 and 2.2µF +/-20% (X5R) or 4.7µF +100/-50% (Z5U) for RF1. The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress the PA-ripple on the battery in TDMA systems at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

Figure *19 – Analog LDO Blockdiagram*

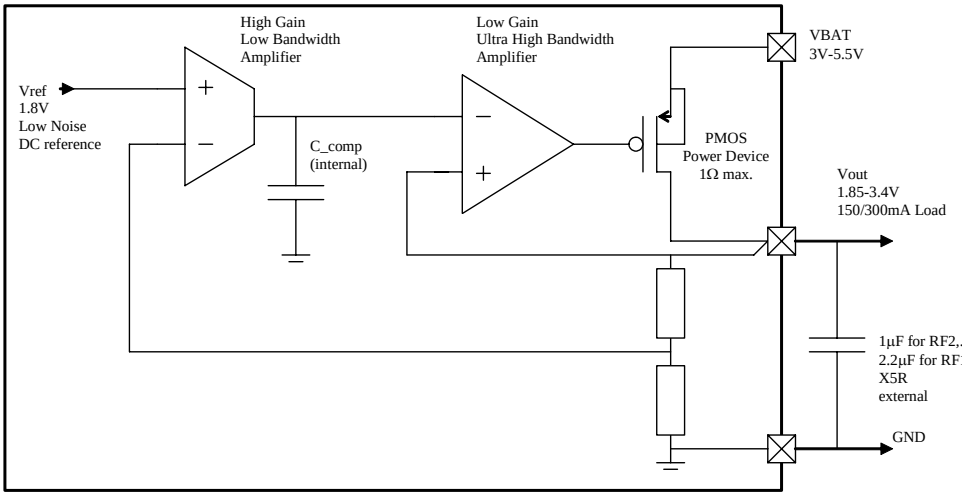


Table *51 – Analog LDO (VRF_1, VRF_2) Characteristics*

Vx_IN=4V; I_{LOAD}=150mA; T_{amb}=25ºC; C_{LOAD} =2.2µF (Ceramic); unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Note
Vx_IN	Supply voltage rage	3		5.5	V	
R_{ON}	On resistance			0.5	Ω	VRF_1
R_{ON}	On resistance			1	Ω	VRF_2
PSRR	Power supply rejection ratio	70			dB	f=1kHz
		40				f=100kHz
I_{OFF}	Shut down current			100	nA	
I_{VDD}	Supply current			50	µA	without load
Noise	Output noise			50	μV_{rms}	10Hz < f < 100kHz

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_{start}	Startup time			200	µs	
V_{out}	Output voltage	1.85		2.85	V	VRFX_IN>3.0V, VRF1 @ Iout=300mA, VRF2 @ Iout=150mA (X=1,2)
		1.85		3.4	V	VRFX_IN>3.55V, VRF1 @ Iout=300mA, VRF2 @ Iout=150mA (X=1,2)
V_{out_tol}	Output voltage tolerance	-50		50	mV	
$V_{LineReg}$	Line regulation	-1		1	mV	Static
		-10		10		Transient;Slope: t_r=10µs
$V_{LoadReg}$	Load regulation	-1		1	mV	Static
		-10		10		Transient;Slope: t_r=10µs
$I_{LIMIT\_VRF1\_HCURR}$	Current limitation		800		mA	VRF_1, rf1_lcurr_en=0
$I_{LIMIT\_VRF1\_LCURR}$	Current limitation		400		mA	VRF_1, rf1_lcurr_en=1 and during startup
I_{LIMIT_VRF2}	Current limitation		400		mA	VRF_2
C_{LOAD_RF1}	Load capacitor	2		5	µF	ceramic only
C_{LOAD_RF2}	Load capacitor	1		5	µF	ceramic only

Table *52 – LDO_RF Register map*

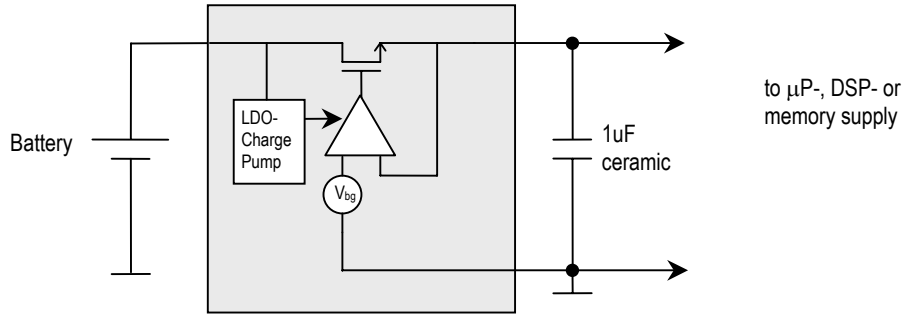
Register Definition	Addr.[13]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
LDO_RF1 Voltage	03	ROM		rf1_swprot_en	rf1_lcurr_en	ldo_rf1_v				
LDO_RF2 Voltage	04	ROM				ldo_rf2_v				
Reg Power1 Ctrl	23	ROM	cp_on	sd3_on	sd2_on	sd1_on	ldo_dig2_on	ldo_dig1_on	ldo_rf2_on	ldo_rf1_on

7.11.2 Digital LDO's (VDIG_1, VDIG_2)

The Digital LDO's can be used in any medium power system or subsystem where quiescent power consumption of the regulator itself has to be minimised without sacrificing its performance. For its stability a cheap 1uF ceramic capacitor is required. **The 5V charge pump will be switch on automatically**, if one of the digital LDO's are switched on

[13] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

Figure *20 – Digital LDO Blockdiagram*



.

Table *53 – Digital LDO (VDIG_1, VDIG_2) Characteristics*

VSUPPLY=4V; I_{LOAD}=200mA; T_{amb}=25ºC; C_{LOAD} =1uF (Ceramic); unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Note
VDIGX_IN	Supply voltage range	1		5.5	V	
R_{ON}	On resistance			4	Ω	
PSRR	Power supply rejection ratio	60			dB	f=1kHz
		30				f=100kHz
I_{OFF}	Shut down current			100	nA	
I_{VDD}	Supply current			20	µA	without load
t_{start}	Startup time			200	µs	
V_{out}	Output voltage	0.75		2.20	V	Vsup.>3.0V, V5_6=5.2V, Iout<200mA
				2.5	V	Vsup.>3.0V, V5_6=5.2V, Iout<100mA
V_{out_tol}	Output voltage tolerance	-50		50	mV	
$V_{LineReg}$	Line regulation	-10		10	mV	Static
		-50		50		Transient;Slope: t_r=10µs
$V_{LoadReg}$	Load regulation	-20		20	mV	Static
		-50		50		Transient;Slope: t_r=10µs
I_{LIMIT}	Current limitation		400		mA	

Table *54 – Digital LDO (VDIG_1, VDIG_2) Programming voltage table*

Code (d)	Code (b)	Vout [V]		Code (d)	Code (b)	Vout [V]
0	000000	0.75		22	010110	1.80
1	000001	0.80		23	010111	1.80
2	000010	0.85		24	011000	1.80
3	000011	0.90		25	011001	1.80
4	000100	0.95		26	011010	1.80
5	000101	1.00		27	011011	1.80
6	000110	1.05		28	011100	1.80
7	000111	1.10		29	011101	1.80
8	001000	1.15		30	011110	1.80
9	001001	1.20		31	011111	1.80
10	001010	1.25		32	100000	1.50
11	001011	1.30		33	100001	1.60
12	001100	1.35		34	100010	1.70
13	001101	1.40		35	100011	1.80
14	001110	1.45		36	100100	1.90
15	001111	1.50		37	100101	2.00

Code (d)	Code (b)	Vout [V]		Code (d)	Code (b)	Vout [V]
16	010000	1.55		38	100110	2.10
17	010001	1.60		39	100111	2.20
18	010010	1.65		40	101000	2.30
19	010011	1.70		41	101001	2.40
20	010100	1.75		42	101010	2.50
21	010101	1.80				

Note: full performance for Vout≤2.20V
max. 100mA output current for Vout≤2.50V
don't use values Vout>2.50V

Table *55 – LDO_DIG Register map*

Register Definition	Addr.[14]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
LDO_DIG1 Voltage	05	ROM			ldo_dig1_v					
LDO_DIG2 Voltage	06	ROM			ldo_dig2_v					
Reg Power1 Ctrl	23	ROM	cp_on	sd3_on	sd2_on	sd1_on	ldo_dig2_on	ldo_dig1_on	ldo_rf2_on	ldo_rf1_on

7.11.3 Low power LDO (V2_5)

The Low power LDO V2_5 is needed to supply the chip core (analog and digital) of the device. It is designed to get the lowest possible power consumption, and still offering reasonable regulation characteristics. The regulator has three supply inputs selecting automatically the higher one. This gives the possibility to supply the chip core either with the battery or with the charger depending on the conditions. Bulk switch comparators are used to avoid any parasitic current flow. To ensure high PSRR and stability, a low-ESR ceramic capacitor of min. 1µF must be connected to the output.
Note: Levelshifters in both directions (input- and output) are placed between digital pins and the digital core of the device.

Table *56 – Low power LDO (V2_5) Characteristics*

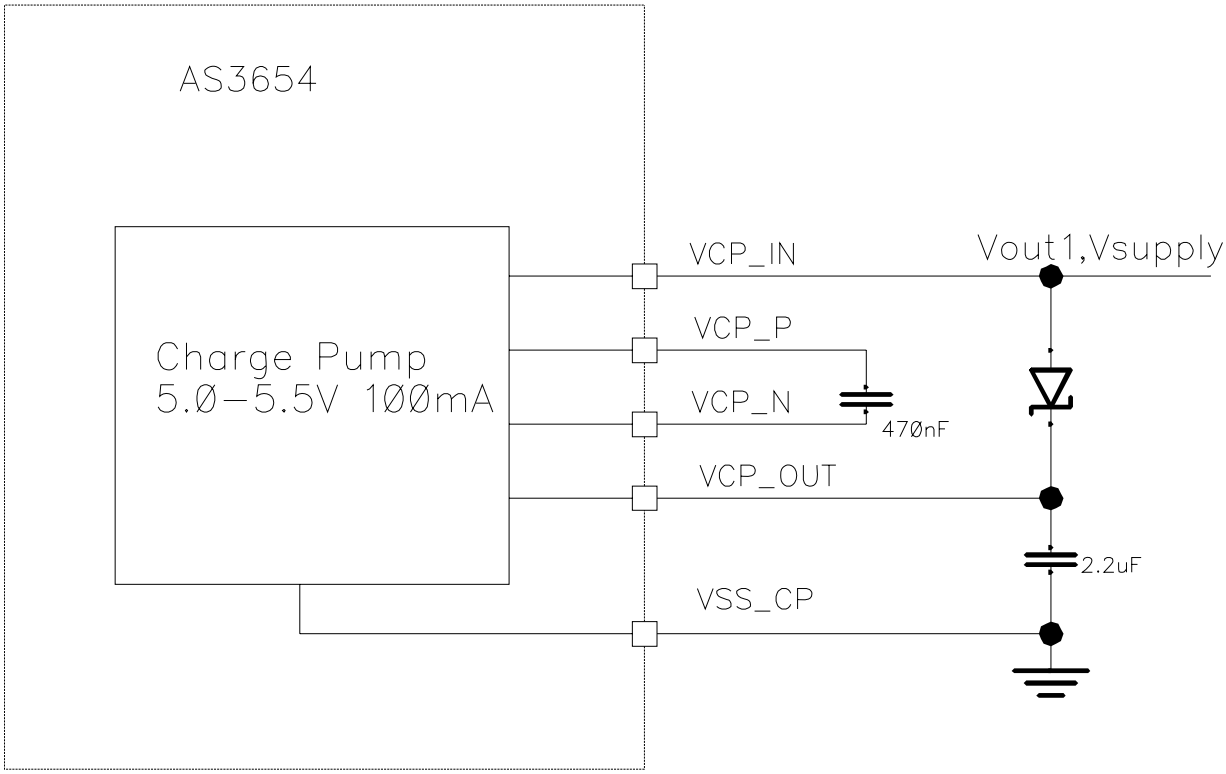
VBAT=4V; I_{LOAD_ext}=0; T_{amb}=25ºC; C_{LOAD} =2.2µF (Ceramic); unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Note
VBAT	Supply voltage rage	2.8		5.5	V	
$V_{CHARGER}$		4		15		
R_{ON}	On resistance			50	Ω	Guaranteed per design
PSRR	Power supply rejection ratio	60			dB	f=1kHz
		40				f=100kHz
I_{OFF}	Shut down current			100	nA	
I_{VDD}	Supply current			3	µA	Guaranteed per design, consider chip internal load for meas.
t_{start}	Startup time			200	µs	
V_{out}	Output voltage	2.4	2.5	2.6	V	
V_{out_tol}	Output voltage tolerance	-50		50	mV	
$V_{LineReg}$	Line regulation	-10		10	mV	Static
		-50		50		Transient;Slope: t_r=10µs
$V_{LoadReg}$	Load regulation	-10		10	mV	Static
		-50		50		Transient;Slope: t_r=10µs

[14] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

7.12 5V Charge Pump

Figure *21 – Digital LDO Blockdiagram*



The charge pump uses the pad VCP_IN as input, regulates and doubles its voltage with the help of the flying capacitor between CAPP and CAPN to its output VCP_OUT. If the bit cp_pulseskip is set, the charge pump operates in pulse skip mode, and only starts cycles if its output voltage is below this level. In this mode the supply current is reduced.

The charge pump requires the following external components:

Table *57 – Charge Pump External Components*

Symbol	Parameter	Min	Typ	Max	Unit	Note
C_{FLY}	External flying capacitor	370	470	850	nF	Ceramic X5R or X7R low-ESR capacitor between CAPP and CAPN
C_{STORE}	External storage capacitor	1.76	2.2	2.64	µF	Ceramic low-ESR capacitor between VCP_OUT and VSS
Dout	Schottky Diode for startup between VCP_IN and VCP_OUT	1			A	Peak current

Make the connections of the two external capacitors as short as possible.

Table *58 – Charge Pump Characteristics*

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CPIN}	Charge Pump input voltage	3.0		5.5	V	

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{IN}	Switching frequency		1.1		MHz	cp_freq=0, f_{clk_int}=2.2MHz
			0.55		MHz	cp_freq=1, f_{clk_int}=2.2MHz
I_{CPOUT}	Output Current	0.0		100	mA	VCP_IN = 3.2V, Clock = f_{clk_int}/2; cp_pulseskip=0; f_{in}=1.1MHz
V_{CPOUT}	Output Voltage	4.9	5.2	5.6	V	
V_{CPSKIP}	Output Voltage during pulseskip		4.92		V	Use with cp_frequ=1 only
I_{CP_noload}	Supply current without load		2		mA	1.1MHz switching frequency
$I_{CP\_pulseskip}$	Charge pump supply current without load in pulseskip mode		20		µA	cp_pulseskip=1 and cp_frequ=1

Table *59 – Charge Pump Bit definitions*

Name	Default	Access	Description
cp_on	ROM	R/W	Switch on of the charge pump block, charge pump is automatically activated when any of the following blocks are active: VDIG1, VDIG2
cp_pulseskip		R/W	Switches on the pulseskip mode of the charge pump 0 Normal fixed frequency mode 1 Pulse skip, low power mode (Set cp_frequ=1 in this mode)
cp_freq		R/W	Defines the clock frequency of the step up dc/dc converter 0 f_{clk_int}/2 (0.8 to 1.15 MHz) 1 f_{clk_int}/4 (0.4 to 0.575 MHz)

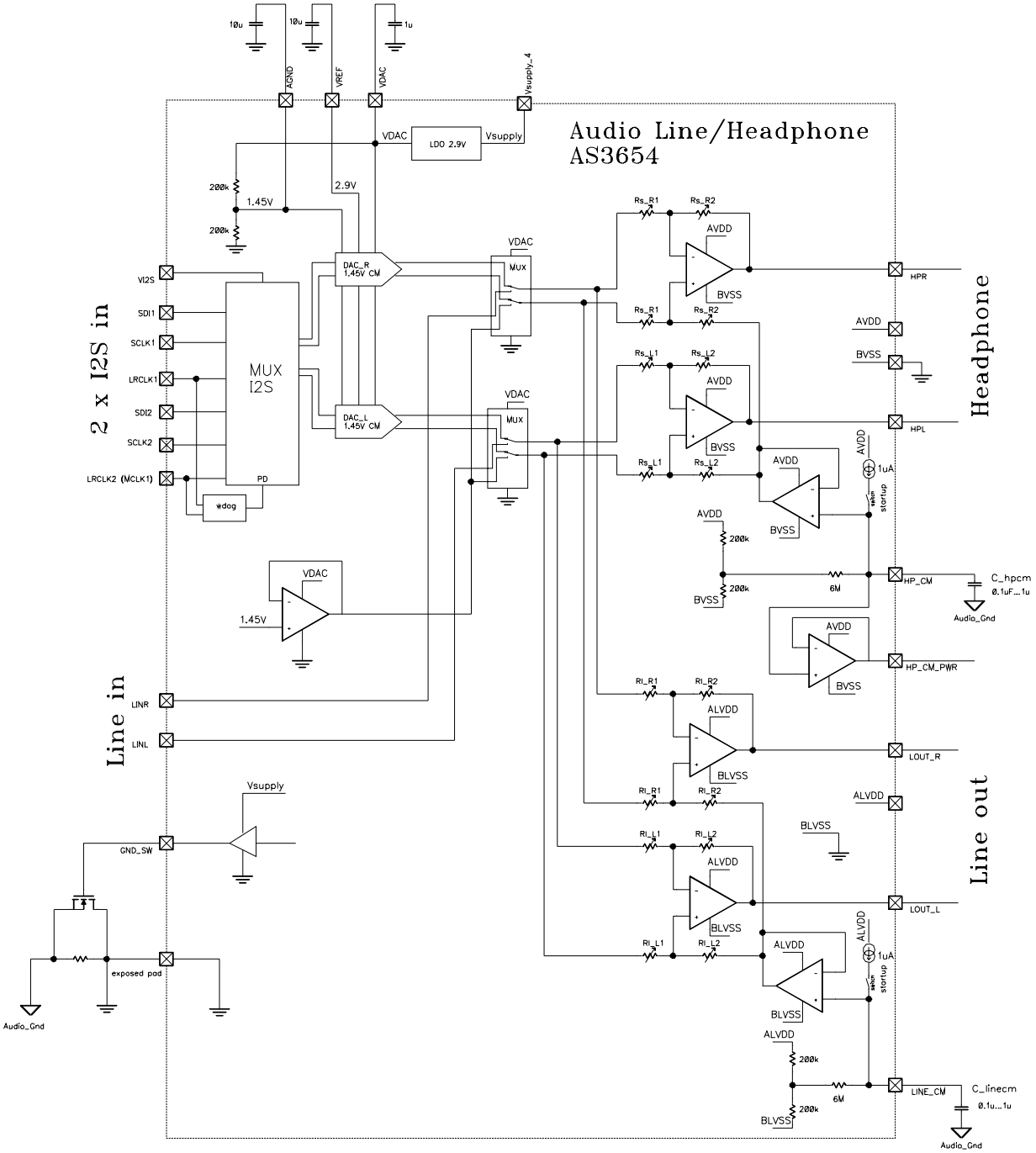
Table *60 – Charge pump Register map*

Register Definition	Addr.[15]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Charge Pump Control	14	ROM (00h)						cp_clkinv	cp_freq	cp_pulseskip

[15] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

7.13 Audio

Figure *22 – Audio Blockdiagram*



7.14 Common mode voltage generation of HP_CM, LINE_CM

The common mode voltage of the Headphone and Lineout is stored in the C_hpcm and C_linecm capacitor. These capacitor are also responsible for the popless startup, PSRR of the amplifiers and sense path of the GND cancellation circuit. Startup and PSRR is defined by the value of the external capacitors. The RC limits the maximum achievable PSRR: R=6MOhm typ, C=0.1...1uF :

Table 61 – common mode voltage, Audio start-up and PSRR

Capacitor value for C_hpcm and C_linecm	Startup time (typ)	Maximum achievable PSRR	
		@ 1kHz (typ)	@ 100Hz (typ)
uF	msec	dB	dB
0.1	150	76	56
1	1500	90	76

7.15 First AudioSet Register

Audio LDO has to be switched on first, and enables all other functions.
The register is R/W; default value is 00h

Table 62 - AudioSet1 Register

Bit	Symbol	Default	Description
7		00h	
6			
5	mclk_invert		MCLK invert selection 0: Change of LRCLK at falling edge of MCLK 1: Change of LRCLK at rising edge of MCLK
4	aud_ldo_on		Audio LDO ON control 0: Audio LDO off 1: Audio LDO on
3	gnd_sw_on		0: GND switch off 0V at pin GND_SW 1: GND switch on Vsupply at pin GND_SW
2	mux_sel		0: DAC input selected 1:Line input selected
1	dac_on		Switch on control of AUDIO DAC 1: DAC enabled (Switch on , if I2S signal valid only) 0: DAC disabled
0	lin_on		1: Line input enabled 0: Line input disabled

Second AudioSet Register

The register is R/W; default value is 00h

Table 63 - AudioSet2 Register

Bit	Symbol	Default	Description
7	I2S_mclk_en	0h	0: Generation of the master clock by the internal PLL 1: Use Pin LRCLK_2 as MCLK_1 input; (the bit I2S_select is used to switch between MCLK *128 = LRCLK and MCLK *256 = LRCLK)

6	I2S_select	0h	0:Select I2S_1 input 1:Select I2S_2 input
5,4	ibr_hph<1:0>		Bias current reduction settings for headphone output: 00: 0% 01: 17% 10: 34% 11: 50%
3	NA		Don't use
2	dith_on		1: add dither to the audio stream 0: no dither added
1,0	ibr_dac<1:0>		Bias current reduction settings for DAC: 00: 0% 01: 25% 10: 40% 11: 50%

Table 64 – Low voltage status Register

Bit	Symbol	Default	Description
5	hpdet	NA	Headphone detect status register

7.16 Digital Audio Input

7.16.1 General

Digital audio data can be fed into the AS3654 via the I2S interface These input data are then used by the 18-bit DAC to generate the analog audio signal.
The stage is set to mute by default; If the DAC input is not enabled.

7.16.2 Signal Description

The digital audio interface uses the standard I2S format:
- left justified
- MSB first
- one additional leading bit

MCLK has to have a fixed ratio of 128 or 256 to LRCK. With a LRCK equal to 32, 44.1 or 48kHz, the MCLK can be generated by the on-chip PLL (do not use the internal PLL if there is jitter on the LRCLK1 or 2). For lower sample rates the MCLK has to generated external.
The high going edge of MCLK has to have timing separation from LRCK edges. If the clock generation is so that LRCK edges are at the same time as MCLK high going edges, the MCLK can be inverted to guarantee a proper DAC function.
This audio input interfaces uses an I2S synchroniser to be able to handle audio sample length of 24bits or less.

Figure *23 – I2S Timing Diagram*

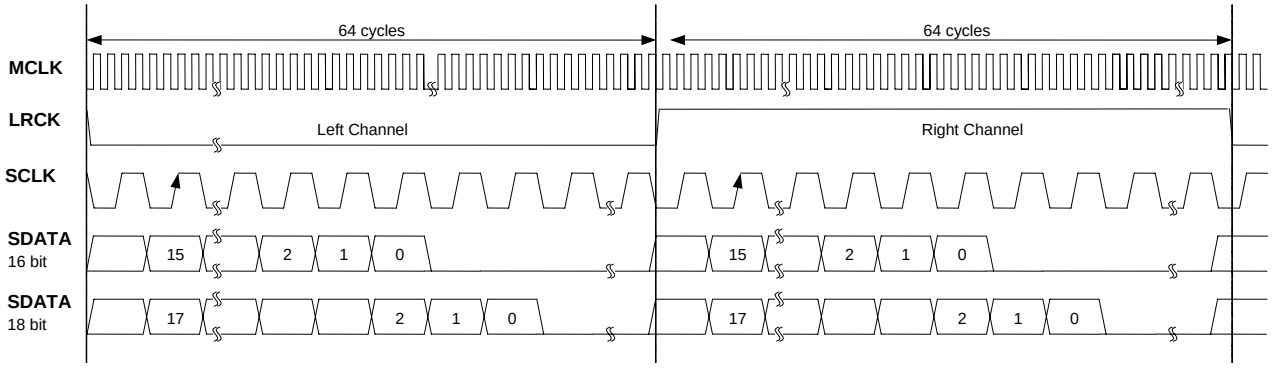


Table 65 – PLL,MCLK Settings

I2S_mclk_en	I2S_select	mclk_invert	Description
0	0	0	I2S_1 selected (PLL used) Internal MCLK synchronised to external LRCLK
0	0	1	I2S_1 selected (PLL used) Internal LRCLK used, synchronised to external SDI
0	1	0	I2S_2 selected (PLL used) Internal MCLK synchronised to external LRCLK
0	1	1	I2S_2 selected (PLL used) Internal LRCLK used, synchronised to external SDI
1	0	0	I2S_1 selected, external MCLK *128 = LRCLK
1	0	1	I2S_1 selected, external MCLK *128 = LRCLK MCLK input inverted
1	1	0	I2S_1 selected, external MCLK *256 = LRCLK
1	1	1	I2S_1 selected, external MCLK *256 = LRCLK MCLK input inverted

7.16.3 Power Save Options

The bias current of the DAC block can be reduced in three steps down to 50% to reduce the power consumption with the register ibr_dac<1:0>.

7.16.4 Parameter

Table 66 - AudioDAC Parameter

PARAMETER	MIN	TYP	MAX	UNIT
ANALOG PERFORMANCE				
THD+Noise at FS		-85	-75	dB
Dynamic Range (20Hz-20kHz, -60dBFS) A-weighted	90	93		dB
Interchannel Mismatch			0.25	dB

Table 67 - I2S Parameter

I2S Inputs and Outputs VI2S=2.9V		MIN	TYP	MAX
VIL	SCLKx, LRCKx, SDIx (30%VI2S/2)	-	-	0.42V
VIH	SCLKx, LRCKx, SDIx (70%VI2S/2)	1.02V	-	VI2S

Table *68 – Audio Register map*

Register Definition	Addr.[16]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Audio Set1	57	00h			mclk_invert	aud_ldo_on	gnd_sw_on	mux_sel	dac_on	lin_on
Audio Set2	58	00h	I2S_mclk_en	I2S_select	ibr_hph			dith_on	ibr_dac	

Table *69 – Low voltage Status register bit*

Register Definition	Addr.[17]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Low voltage Status	47	40h	stpup1_det	stpup1_oc	hpdet	dig2_lv	dig1_lv	sd3_lv	sd2_lv	sd1_lv

7.17 Line Input

7.17.1 General

AS3654 includes one stereo single ended inputs.

Table 70 - Line Inputs Parameter

PARAMETER	MIN	TYP	MAX	UNIT
ANALOG PERFORMANCE				
Rin		50		kOhm

7.18 Headphone Output

The headphone output is designed to provide the audio signal with 2x40mW @ 16Ω or 2x20mW @32Ω, which are typical values for headphones.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB.

7.18.1 Phantom Ground

HP_CM_PWR pin is the buffered HP_CM output. It can be used to drive the loads without external de-coupling capacitors between HPL / HPR and HPCM. If the load is between HPR / HPR and BVSS, 100uF of de-coupling capacitors are

[16] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence
[17] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

needed. The phantom ground can be switched off to save power if not needed.

7.18.2 No-Pop Function

To avoiding click and pop noise during power-up and shutdown, the output is automatically set to mute when the output stage is disabled. Also the volume settings are set to their default values, and can't be changed, as long the output stage is not enabled.

HP_CM pin, which needs a 100nF to 1uF capacitor outside, gets charged on power-up with 1uA to AVDD/2. After start-up the DC level of the following pins are the same: HPR=HPL=HP_CM=HP_CM_PWR=AVDD/2. The Start-up time before releasing mute is about 150ms. To avoid pop-noise 150ms discharging time of HP_CM after a shutdown, have to be waited before starting up again.

7.18.3 Over-current Protection

This output stage has an over-current protection, which disables the output for 256ms or 512ms. This value can be set in the headphone registers. The over-current protection limit of HPR and HPL pin is about 260mA while HP_CM_PWR pin has a 370mA limit.

7.18.4 Headphone Detection

With a control bit the headphone detection can be enabled. The detection is only working as long the headphone stage is in power down mode and the load is applied between HPR / HPL and HP_CM_PWR.

7.18.5 Power Save Options

To save power, especially when driving 32 Ohm loads, a reduction of the bias current can be selected.

Bias current reduction settings for headphone output:

00: 0%

01: 17%

10: 34%

11: 50%

Parameter

Table 71 - Power Amplifier Parameter

PARAMETER		MIN	TYP	MAX	UNIT
ANALOG PERFORMANCE					
R_Load at AOUTR and AOUTL single ended		16			Ohm
Vout				1.13	Vp
Gain Step Precision (RLmin-max,20Hz-20kHz)			±0.5		dB
SINAD no load, LineIn-> HPH, A-weighted			-97		dB
THD @ 1kHz, no load			-88		dB
THD @ 1kHz, 32Ohm, 10mW			-80		dB
THD @ 1kHz, 32Ohm, 20mW			-74	-66	dB
THD @ 1kHz, 16Ohm, 40mW			-68	-60	dB
Channel Separation (32Ohm, dc-coupled)			60		dB
PSRR (200Hz-20kHz)		60	90		dB
Shorted Protection Level			260		mA
Shorted Protection Level of common mode buffer			370		mA
IOUT_powerdown		-20		20	µA
Tpower_up (HP_CM=0.1µF)			150		ms
GND cancellation GND - AUDIO_GND to HP_R, HP_L no load	100Hz		50		dB
	1kHz		50		
	10kHz		40		

7.18.6 Register Description

To get an interrupt on an over-current event, the corresponding bit in the Interrupt enable register has to be set. Changing the bias current or the output driver strength is done via AudioSet2 register. All other headphone driver settings are controlled by the following two registers.

Right Headphone Register

The register is R/W; default value is 00h

Table 72 - HPH_OUT_R Register

Bit	Symbol	Default	Description
7..6	hp_ovc_to	00h	headphone over current time out: speaker over current time out: 11: 0 ms 10: 512 ms 01: 128 ms 00: 256 ms
5	hpcm_off		headphone phantom ground disable 0: normal operation 1: disable common mode buffer
4..0	hpr_vol		volume settings for right headphone output, adjustable in 32 steps @ 1.5dB 00000: -40.5 dB gain 00001: -39 dB gain .. 11110: 4.5 dB gain 11111: 6 dB gain

Left Headphone Register

The register is R/W; default value is 00h

Table 73 - HPH_OUT_L Register

Bit	Symbol	Default	Description
7	hp_mute	00h	0: normal operation 1: headphone output set to mute (mute is on during power-up)
6	hp_on		0: headphone stage not powered 1: power up headphone stage
5	hpdeton		0: no headphone detection 1: enable headphone detection
4..0	hpl_vol		volume settings for left headphone output, adjustable in 32 steps @ 1.5dB 00000: -40.5 dB gain 00001: -39 dB gain .. 11110: 4.5 dB gain 11111: 6 dB gain

Table *74 – Headphone Register map*

Register Definition	Add [18]	Default	Content

[18] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

Name			b7	b6	b5	b4	b3	b2	b1	b0
HPH out R	59	00h	hp_ovc_to		hpcm_off	hpr_vol				
HPH out L	60	00h	hp_mute	hp_on	hpdeton	hpl_vol				

7.19 Line Output

7.19.1 General

The line output is designed to provide the audio signal on 600 Ω min.
This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB..

7.19.2 No-Pop Function

To avoiding click and pop noise during power-up and shutdown, the output is automatically set to mute when the output stage is disabled. Also the volume settings are set to their default values, and can't be changed, as long the output stage is not enabled.
LINE_CM pin, which needs a 0.1µF... 1µF capacitor outside gets charged on power-up with 1uA to ALVDD/2. After start-up the DC level of the following pins are the same: LOUT_L=LOUT_R=LINE_CM= ALVDD/2. The Start-up time before releasing mute is about 150ms with 0.1µF. To avoid pop-noise 150ms discharging time of LINE_CM after a shutdown, have to be waited before starting up again.

7.19.3 Power Save Options

To save power, a reduction of the bias current can be selected.

Table 75 - Line Power-Save Options

IBR_LINE	IDD_LINE (typ.)
0	2.2mA
1	1.5mA

7.19.4 Parameter

Table 76 - Line out Block Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
ANALOG PERFORMANCE					
R_Load at LOUT_L and LOUT_R single ended		600			Ohm
Gain Step Precision (RLmin-max,20Hz-20kHz)			±0.5		dB
SINAD no load, LineIn-> Line out, A-weighted			-97		dB
THD @ 1kHz, no load			-88		dB
THD @ 1kHz, 600Ohm			-80		dB
PSRR (200Hz-20kHz)		60	90		dB
IOUT_powerdown		-20		20	µA
Tpower_up (C_LINECM=100nF)			150		ms
GND cancellation GND - AUDIO_GND to LOUT_R, LOUT_L no load	100Hz		50		dB
	1kHz		50		
	10k		40		

7.19.5 Register Description

To get an interrupt on an over-current event, the corresponding bit in the Interrupt enable register has to be set. All other Line/headphone driver settings are controlled by the following two registers.

Right Line Register

The register is R/W; default value is 00h

Table 77 - LINE_OUT_R Register

Bit	Name	Default	Description
7,6	ibr_line<1:0>	00h	Bias current reduction settings for line output: 00: 0% 01: 17% 10: 34% 11: 50%
5	-		reserved
4..0	liner_vol		volume settings for right Line output, adjustable in 32 steps @ 1.5dB 00000: -40.5 dB gain 00001: -39 dB gain .. 11110: 4.5 dB gain 11111: 6 dB gain

Left Line Register

The register is R/W; default value is 00h

Table 78 - LINE_OUT_L Register

Bit	Symbol	Default	Description
7	line_mute		0: normal operation 1: Line output set to mute (mute is on during power-up)
6	line_on		0: Line stage not powered 1: power up Line stage
5	-		reserved

4..0	linel_vol		volume settings for left Line output, adjustable in 32 steps @ 1.5dB 00000: -40.5 dB gain 00001: -39 dB gain .. 11110: 4.5 dB gain 11111: 6 dB gain

Table *79 – Lineout Register map*

Register Definition	Addr.[19]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Line out R	61	00h	ibr_line			liner_vol				
Line out L	62	00h	line_mute	line_on		linel_vol				

7.20 I²C Serial Interface

Table *80 – I2C SDA,SCL Characteristics*

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{IL}	SCL,SDA Low Level input voltage	-0.3		0.4	V	
V_{IH}	SCL,SDA High Level input voltage	1.3		VSUPPLY	V	

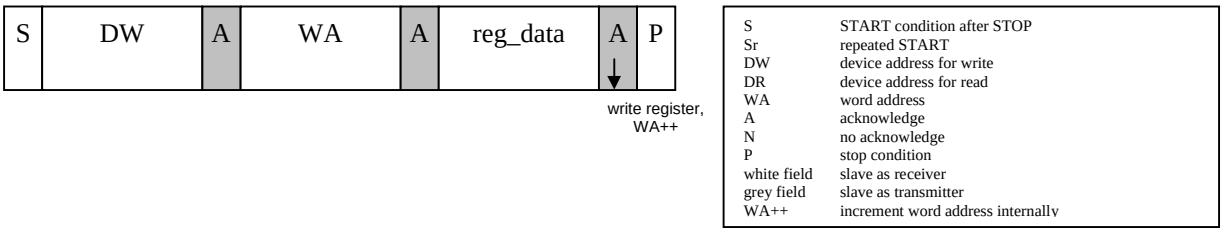
Feature List

- Fast-mode capability (max. SCL-frequency is 400 kHz)
- 7+1-bit addressing mode
- 60h x 8-bit data registers (word address 0x00 - 0x60)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

[19] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

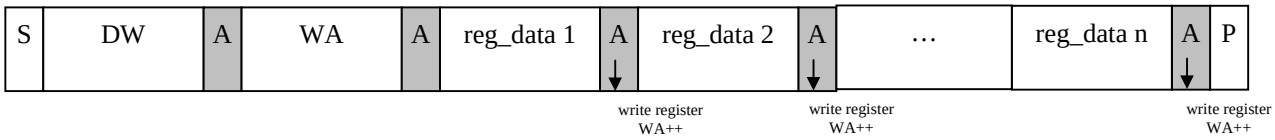
Transfer Formats

Figure *24 – I²C Byte-Write:*



AS3654 device address write (DW):80h = 10000000b
AS3654 device address read (DR): 81h = 10000001b

Figure *25 – I²C Page-Write:*

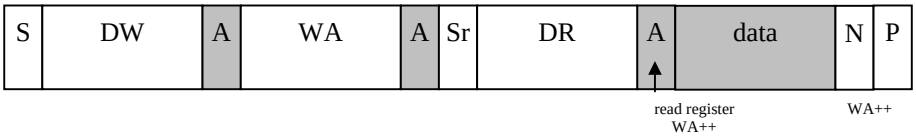


Byte-Write and Page-Write are used to write data to the slave.
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be send to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read-Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

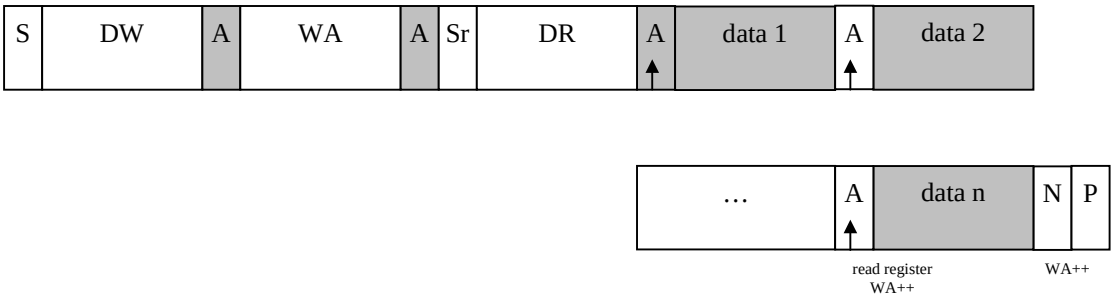
The diagrams below show various read formats available:

Figure *26 – I²C Random-Read:*



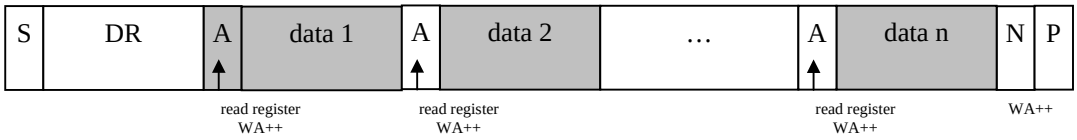
Random-Read and Sequential-Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.
The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure *27 – I²C Sequential-Read:*



Sequential-Read is the extended form of Random-Read, as more than one register-data bytes are transferred subsequently. In difference to the Random-Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure *28 – I²C Current-Address-Read:*



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random-Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential-Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

7.21 Reset

XRESET is a low active bi-directional pin. An external pull-up to the periphery supply has to be added.

During each reset cycle the following states are controlled by the AS3654:
- Pin XRESET is forced to GND
- Programmable Power-off function
- Programmable Power-on sequence and regulator voltages
- Programmable reset timer
- All registers are set to their default values after power-on, except the reset control- and status-registers.

Note:
Programming is controlled by the internal Mask-PROM and the external resistor RPROGRAM

Table *81 – XRESET,XON Characteristics*

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{XRESET_IL}	XRESET Low Level input voltage	-0.3		0.4	V	TBD
V_{XRESET_IH}	XRESET High Level input voltage	1.3		VSUPPLY	V	TBD

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{XON_IL}	XON Low Level input voltage	-0.3		0.3*V2_5		
V_{XON_IH}	XON High Level input	0.7*V2_5		V2_5		
I_{XON_PUP}	XON Pull up current		5		µA	

Reset Conditions

Reset can be activated from 7 different sources:
- Power on (battery or charger insertion)
- Low Battery
- Software forced reset
- Power off mode
- External triggered through the pin RESET
- Overtemperature
- Watchdog

Voltage detection:

There are two types of voltage dependent resets: V_{POR} and V_{XRESET}. V_{POR} monitors the voltage on V2_5 and V_{XRESET} monitors the voltage on VSUPPLY. The linear regulator for V2_5 is always on and uses the voltage VCHARGER, VBAT or V_USB as its source.

The pin RESET is only released if V2_5 is above V_{POR} and VSUPPLY is above $VXRESET_{RISE}$.

Table *82 – Reset Levels*

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{POR}	Overall power on reset	1.5	2.0	2.3	V	Monitor voltage on V2_5; power on reset for all internal functions
$VXRESET_{RISE}$	Reset level for Vsupply rising		ResVoltrise		V	Monitor voltage on Vsupply; rising level
$VXRESET_{FALLING}$	Reset level for Vsupply falling		2.7		V	Monitor voltage on VSupply; falling level
			ResVotfall		V	if SupResEn=1 only
$VRESET_{MASK}$	Mask time for $VXRESET_{FALLING}$	2.0	2.5	3.0	ms	Duration for VBAT<$VXRESET_{FALLING}$ until a reset cycle is started[20]

$VRESET_{FALLING}$ is only accepted if the reset condition is longer than $VRESET_{MASK}$. This guard time is used to avoid a complete reset of the system in case of short drops of VBAT.

Power off:

To put the chip into ultra low power mode, write '1' into xon_enable and '1' into *power_off*. The chip waits until the external pin XON is pulled low, the charger is inserted or the level V_{POR} is reached to start a complete reset cycle. The bit *power_off* is automatically cleared by this reset cycle. During *power_off* state all circuits are shut-off except the Low Power LDO (V2_5). Thus the current consumption of AS3654 is reduced to less than 15µA. The digital part is supplied by V2_5, all other circuits are turned off in this mode, including references and oscillator. Except the reset control registers all other registers are set to their default value after power-on.

[20] VRESET signal is debounced with the specified mask time for rising- and falling slope of VBAT.

Software forced reset

Writing '1' into the register bit force_reset immediately starts a reset cycle. The bit *force_reset* is automatically cleared by this reset.

External triggered reset:

If the pin XRESET is pulled from high to low by an external source (e.g. microprocessor or button) a reset cycle is started as well.

Overtemperature reset:

The reset cycle can be started by overtemperature conditions. See section 'Protection Functions'.

Watchdog reset:

If the watchdog is armed (register bit *wtdg_on* = 1 and *wtdg_res_on* = 1) and the timer expires it causes a reset. See section 'Watchdog'.

Reset Control Bits

Table *83 – Reset Register map*

Register Definition	Addr.[21]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Reset Timer	22	ROM (0Fh)					xon_enable	res_timer		
Reset Control	72	00h			reset_reason			xon_input	power_off	force_reset

Table *84 – Reset Bit definitions*

Name	Default	Access	Description
force_reset	0b	R/W	Setting to '1' starts a complete reset cycle
power_off	0b	R/W	Setting to '1' starts a reset cycle, but waits after the Reg_off state for a falling edge on the pin XON or until the charger is detected
xon_input	NA	R	This flag represents the state of the XON pad directly
xon_enable	ROM	R/W	This flag enables the XON pad and sets the power on state of the ASIC 0 XON pad disabled. Startup of chip; if VBAT>$VRESET_{RISING}$ 1 XON pad enabled. Startup of chip; if VBAT>$VRESET_{RISING}$ and XON=0

[21] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

Name	Default	Access	Description
reset_reason	NA	R	Flags to indicate to the software the reason for the last reset 000 V_{POR} has been reached (battery or charger insertion from scratch) 001 $VRESET_{FALLING}$ was reached (battery voltage drop below 2.75V) 010 software forced by *force_reset* 011 software forced by *power_off* and XON was pulled low 100 software forced by *power_off* and charger was detected 101 external triggered through the pin RESET 110 reset caused by overtemperature T_{140} 111 reset caused by watchdog
res_timer	Boot-ROM	R/W	Set RES_{TIME} 000 RES_{TIME}=10ms 001 RES_{TIME}=20ms 010 RES_{TIME}=35ms 011 RES_{TIME}=50ms 100 RES_{TIME}=65ms 101 RES_{TIME}=80ms 110 RES_{TIME}=95ms 111 RES_{TIME}=110ms

Reset Cycle

During a reset cycle the pin XRESET is forced to low for at least RES_{TIME} and all registers are set to their default values (except the bit *ov_temp_140* and the Boot-Ctrl register). During the reset time a normal startup happens (see section 'Startup'), the reset is active until the reset timer (set by register bits *res_timer<2:0>*) expires. Then the voltage on the pin XRESET is pulled high by the external resistor and the whole system is leaving the reset state.

res_con: Reset Control

Reset is internally generated from a power supply supervisor and provided to internal logic as well as externally through the open-drain pad XRESET. At this point, it could be also forced externally from an external power supply supervisor. Additionally Reset can be forced by software.

7.22 Interrupt Controller

The interrupt controller generates an interrupt request for the host controller as soon as one or more of the bits in the *Interrupt 1…2* register is set by pulling low pin XINT. All the interrupt sources can be enabled in the *Interrupt Mask 1…2* register. The *Interrupt 1…2* registers are cleared automatically after the host controller has read them. To prevent the AS3654 device from loosing an interrupt event, the register that is read is captured before it is transmitted to the host controller via the serial interface. As soon as the transmission of the captured value is complete a logical AND operation with the bitwise inverted captured value is applied to the register to clear all interrupt bits that have already been transmitted. Clearing the read interrupt bits takes 2 clock cycles, a read access to the same register before the clearing process has completed will yield a value of '0'. Note that an interrupt that has been present at the previous read access will be cleared as well in case it occurs again before the clearing process has completed.

During a read access to one of the interrupt registers the XINT pin will be released. As soon as the transferred bits of the interrupt register have been cleared the XINT pin will be pulled low in case a new interrupt has occurred in the meantime. By doing so the interrupt controller will work correctly with host controllers that are edge- and level-sensitive on their interrupt request input. Multiple byte read access is recommended to avoid reading the *Interrupt 1* register over and over again in response to a new interrupt that has occurred in the same register (and thus pulling low pin XINT) before the *Interrupt 2* register has been read.

Table 85 – Interrupt 1 Register

Address 1; Read only access; register is reset at power-on-reset and after each read access. Default value after reset: 00h.

Bit	Symbol	Default	Description
0	*chstate_i*	NA	Bit is set when the following status bits are set or reset: Trickle, CVM, NoBat
1	*cheoc_i*	NA	Bit is set when the EOC status bits are set or reset:
2	*trickle_tmax_i*	NA	Bit is set when trickle charge timeout has been expired
3	*usb_chdet_i*	NA	Bit is set when the USB_ChDet Bit is set or reset.
4	*chdet_i*	NA	Bit is set when the ChDet Bit is set or reset.
5	*Onkey_i*	NA	Bit is set when status XON bit is set or reset.
6	*ovtmp_i*	NA	Bit is set when the lower temperature threshold $Temp_{110}$ of the temperature sensor is exceeded for longer than $t_{RESMASK}$.
7	*Lowsup*	0	Bit is set when the main supply voltage VSUPPLY has dropped below $V_{RESFALL}$ for longer than $t_{RESMASK}$.

Table 86 – Interrupt 2 Register

Address 2; Read only access; register is reset at power-on-reset and after each read access. Default value after reset: 00h.

Bit	Symbol	Default	Description
0	*sd1_lv_i*	0	Bit is set when voltage of step down1 drops below low voltage threshold (1msec debounce time default)
1	*sd2_lv_i*	0	Bit is set when voltage of step down2 drops below low voltage threshold (1msec debounce time default)
2	*sd3_lv_i*	0	Bit is set when voltage of step down3 drops below low voltage threshold (1msec debounce time default)
3	*dig1_lv_i*	0	Bit is set when voltage of LdoDig1 drops below low voltage threshold (1msec debounce time default)
4	*dig2_lv_i*	0	Bit is set when voltage of LdoDig2 drops below low voltage threshold (1msec debounce time default)
5	*hphcurr_i*	0	Bit is set when output stage of headphone amplifier exceeds overcurrent limit.
6	*hpdet_i*	O	Bit is set when hp_det status bit is set or reset (1msec debounce time default)
7	*stpup1_i*	O	Bit is set when stpup1_oc or stpup1_det is set.

Table 87 – Interrupt mask 1 Register

Address 29; R/W access; register is reset at power-on-reset only. Default value after reset: FFh.

Bit	Symbol	Default	Description			
0	chstate_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
1	cheoc_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
2	trickle_tmax_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
3	usb_chdet_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
4	chdet_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
5	onkey_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
6	ovtmp_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
7	LowSup_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled

Table 88 – Interrupt mask 2 Register

Address 30; R/W access; register is reset at power-on-reset only. Default value after reset: FFh.

Bit	Symbol	Default	Description			
0	sd1_lv_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
1	sd2_lv_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
2	sd3_lv_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled

Bit	Symbol	Default	Description			
3	dig1_lv_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
4	dig2_lv_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
5	hphcurr_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
6	hpdet_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled
7	stpup1_int_mask	1b	0	Interrupt is enabled	1	Interrupt is disabled

Table 89 – Low voltage status Register

Bit	Symbol	Default	Description
0	sd1_lv	0b	Step down1 low voltage status bit (-10% voltage drop)
1	sd2_lv	0b	Step down2 low voltage status bit (-10% voltage drop)
2	sd3_lv	0b	Step down3 low voltage status bit (-10% voltage drop)
3	dig1_lv	0b	Ldo Dig1 low voltage status bit (-50mV voltage drop)
4	dig2_lv	0b	Ldo Dig2 low voltage status bit (-50mV voltage drop)
5	hpdet	0b	Headphone detect status bit
6	stpup1_oc	0b	Bit is set by analog part, if overcurrent of DCDC StepUp1 occurs for more than 4msec(tbd)
7	stpup1_det	0b	Current Detection signal of step up 1

deb_time of low voltage and headphone detect and stpup1_oc and stpup1_det signal = 911µSec

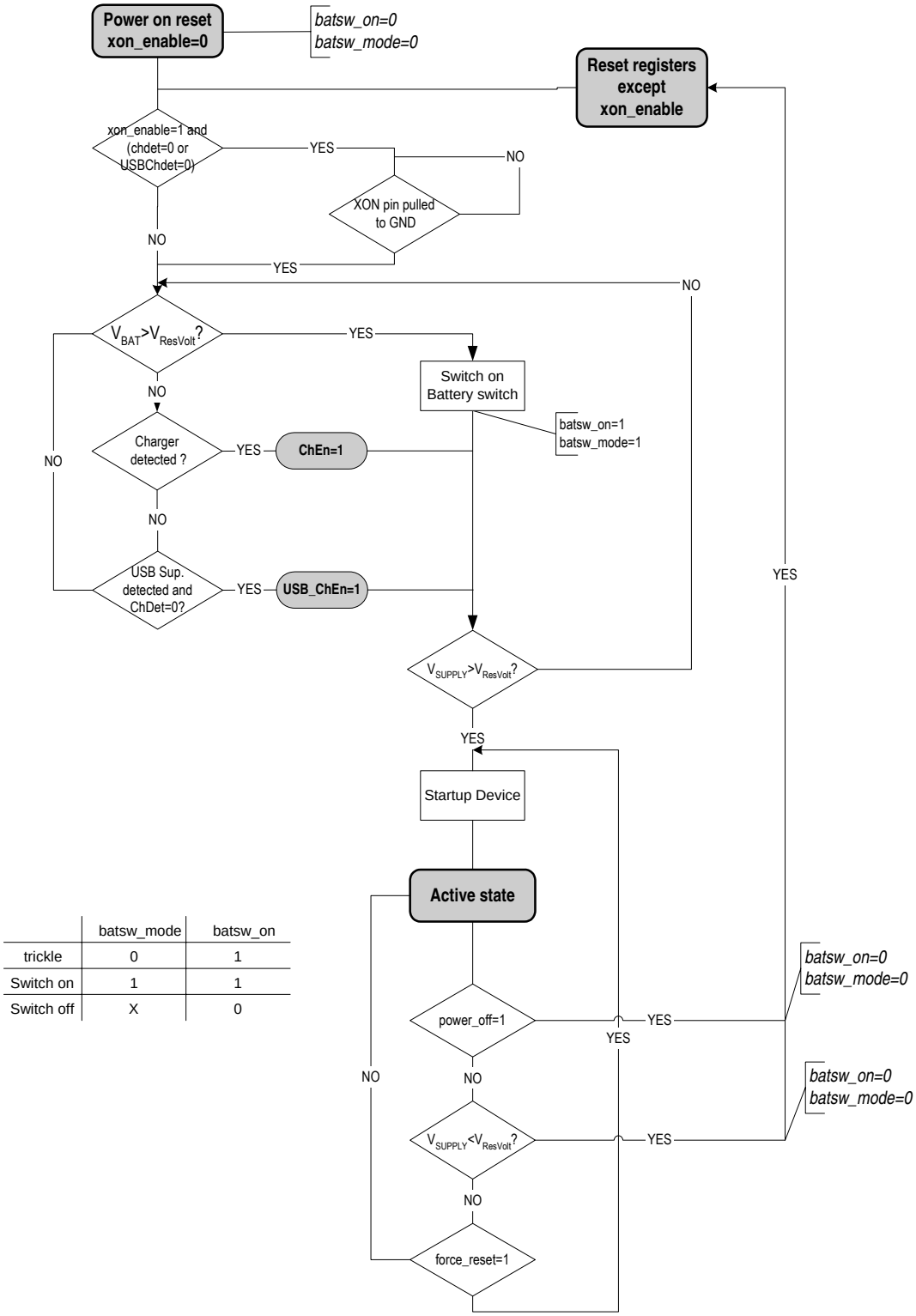
Table *90 – Interrupt Register map*

Register Definition	Addr.[22]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Interrupt Mask1	43	FFh	LowBat_int_m	ovtmp_int_m	onkey_int_m	chdet_int_m	usb_chdet_int_m	trickle_tmax_int_m	cheoc_int_m	chstate_int_m
Interrupt Mask2	44	FFh	stpup1_int_m	hpdet_int_m	hphcurr_int_m	dig2_lv_int_m	dig1_lv_int_m	sd3_lv_int_m	sd2_lv_int_m	sd1_lv_int_m
Interrupt Status1	45	NA	LowBat_i	ovtmp_i	onkey_i	chdet_i	usb_chdet_i	trickle_tmax_i	cheoc_i	chstate_i
Interrupt Status2	46	NA	stpup1_i	hpdet_i	hphcurr_i	dig2_lv_i	dig1_lv_i	sd3_lv_i	sd2_lv_i	sd1_lv_i
Low voltage Status	47	40h	stpup1_det	stpup1_oc	hpdet	dig2_lv	dig1_lv	sd3_lv	sd2_lv	sd1_lv

[22] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

7.23 Startup

Figure *29 – Startup flow chart*



	batsw_mode	batsw_on
trickle	0	1
Switch on	1	1
Switch off	X	0

Normal Startup

During a normal reset cycle (see section Reset), but after V2_5 is above V_{POR} and Vsupply is above $VRESET_{RISE}$ a normal startup happens:

- The external capacitor on CREF is charged to 1.8V (internal signal precharge_n, low active)
- The 3bit A/D conversion is performed (configuration: ratio of R_{BOOT}/R_{BIAS}, result→*boot_ctrl<2:0>*)
- Startup Statemachine reads out the internal Boot-ROM (address defined by *boot_ctrl*), Startsequence of Step-Down Converter and LDO's controlled by the Boot-ROM
- Reset-Timer is set by the Boot-ROM
- The reset is released when the Reset Timer expires (external pin XRESET)

7.23.1 Programmable Startup Sequences

see *austriamicrosystems AG* document
BootGen3654_2v0_050415.xls

Startup from Charger

If the voltage on pin VCHARGER is within $VSTART_{CHARGER}$, the charger is started in any case (even with VBAT = 0V). This allows the battery to be charged (even from deep discharge) and finally a normal startup to happen.

Table *91 – Charger Startup Conditions*

Symbol	Parameter	Min	Typ	Max	Unit	Note
$VSTART_{CHARGER}$	Voltage on VCHARGER for system to start	4.0	5.0	15	V	on Pin VCHARGER

7.23.2 Protection Functions

All LDO's, the DCDC step up and DCDC step down have an integrated overcurrent protection. An overtemperature protection of the chip is also integrated which can be switched on with the serial interface signal **temp_pmc_on**. The chip has two signals for the serial interface: **ov_temp_110** and **ov_temp_140**. The flag **ov_temp_110** is automatically reset if the overtemperature condition is removed, whereas **ov_temp_140** has to be reset by the serial interface with the signal **rst_ov_temp_140**.
If the flag **ov_temp_140** is set, an automatic reset of the complete chip is initiated. The flag **ov_temp_140** is not affected by this reset cycle allowing the software to detect the reason for this unexpected shutdown.

Table *92 – Overtemperature Detection*

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{110}	ov_temp_110 rising threshold	95	110	125	Degrees	
T_{140}	ov_temp_140 rising threshold	125	140	155	Degrees	
T_{hyst}	ov_temp_110 and ov_temp_140 hystersis		5		Degrees	

Table *93 – Overtemperature detection Regsiter definitions*

Register Definition	Addr.[23]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0

[23] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

Register Definition	Addr.[23]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Overtemperature Control	73	00h	tco_140_a	tco_110_a	temp_test1	temp_test0	rst_ov_temp_140	ov_temp_140	ov_temp_110	temp_pmc_on

Table *94 – Overtermperature detection Bit definitions*

Name	Default	Access	Description
temp_pmc_on	0	R/W	Switch on / off of temperature supervision; default: off – all other bits are only valid if set to '1'
ov_temp_110	NA	R	Flag that the overtemperature threshold 1 (T_{110}) has been reached
ov_temp_140	NA	R	Flag that the overtemperature threshold 2 (T_{140}) has been reached – this flag is not reset by a overtemperature caused reset and has to be reset by **rst_ov_temp_140**
rst_ov_temp_140	0	W	If the overtemperature threshold 2 has been reached, the flag **ov_temp_140** is set and a reset cycle is started. **ov_temp_140** should be reset by writing 1 and afterward 0 to **rst_ov_temp_140**
temp_test0	0	R/W	Only used for production test; always leave at '0'
temp_test1	0	R/W	Only used for production test; always leave at '0'
tco_110_a	NA	R	Only used for production test – direct output of T110 comparator
tco_140_a	NA	R	Only used for production test – direct output of T140 comparator

TMP_SV: Temperature Supervision

Comment: If one of the bits **temp_test0** or **temp_test1** is set, the output of the analog block **tco_110_a** and **tco_140_a** must be ignored.

A temperature sensor is implemented to provide over-temperature protection of the chip. It generates two flags linked to the two temperature thresholds (110 degrees, 140 degrees). Both thresholds have an hysteresis to prevent oscillation effects.
First threshold (110 degrees) ***tco_110_a*** sets the flag ***ov_temp_110,*** signalling the serial interface part and software the 110 degrees overtemperature condition. Thus software can react and shuts down power consuming functions to decrease temperature.
Second threshold (140 degrees) ***tco_140_a*** activates ***reset_140_n***, which activates **XRESET** within rescon: this sets all regulators into power-down mode and stops charging, and performs the reset cycle of the AS3654.
An additional function also implemented within tmp_sv is the generation of a rst_ov_temp_140 flag indicating, that a 140 degrees overtemperature condition caused the last reset of the digital part.
The signal *temp_pmc_on*=HIGH activates the temperature supervision.

rstovtemp_140 flag

In case of an activated reset (*resetpb_n* active), the system loses any information about the error which activated the reset state. Therefore, a flag is implemented, which indicates that the reset was caused by a reset_140_n activation. For the digital part, this flag is only resetable via the input signal rst_ovtemp_140:

- reset via signal rst_ovtemp_140
- set in case that reset_140_n goes active

7.23.3 Watchdog

The purpose of the watchdog is to detect a deadlock of the software. If the watchdog is active, it must become continuously a trigger signal within a programmable time window. If there is no signal anymore for a certain time period from a defined pad or

special serial interface bit, it starts either a complete reset cycle or changes the state of an output pin, which can be used e.g. as an interrupt to the processor.

The watchdog is highly configurable by the following register bits:
The complete block can be switched on by *wtdg_on* = 1 and off by by *wtdg_on* = 0.
The watchdog time window is defined by the register *wtdg_min_timer* and *wtdg_max_timer*.
The trigger signal can be configured by register *wtdg_trigger* and *wtdg_gpio_input*. (Pin CURR1-CURR4 (GPIO1-GPIO4) or register bit)
If the watchdog expires, the system can start automatically a reset cycle if *wtdg_reset_on* = 1
Any of the general purpose input / outputs can be configured to output the watchdog signal (see section "General Purpose Input and Outputs"). The Watchdog delivers a signal "wtdg_alarm", which is normal '0' and goes to '1' in the case of a timer-overflow. This signal can be used as e.g. a reset or interrupt for a processor.

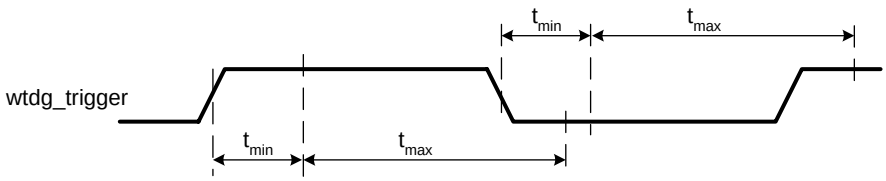
Table *95 – Watchdog Regsiter definitions*

Register Definition	Addr.[24]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Watchdog Control	53	02h						wtdg_trigger	wtdg_res_on	wtdg_on
Watchdog_min Timer	54	00h	wtdg_min_timer							
Watchdog_max Timer	55	FFh	wtdg_max_timer							
Watchdog Software Signal	56	00h								wtdg_sw_sig

Table *96 – Watchdog Bit definitions*

Name	Default	Access	Description
wtdg_on	0b	R/W	Switches on the complete watchdog
wtdg_res_on	1b	R/W	If the watchdog expires and *wtdg_res_on* = 1 a reset cycle will be started – see section 'Reset'
wtdg_trigger	0b	R/W	0 Use the register bit *wtdg_sw_signal* as trigger signal for the watchdog 1 Use the pin defined by *wtdg_gpio_input* as trigger signal for the watchdog
Wtdg_min_timer	(00)h	R/W	Defines the minimum watchdog trigger time (LSB=7.5ms, range: 0 – 1.9s)
Wtdg_max_timer	(FF)h	R/W	Defines the maximum watchdog trigger time (LSB=7.5ms, range: 7.5ms – 1.9s), do not set to (00)h
wtdg_sw_sig	0b	R/W	Trigger input by the serial interface if *wtdg_trigger* = 0

Figure *30 – Watchdog timing diagram*



[24] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

7.23.4 Internal References (V, I, f_{clk})

The internal reference circuits needs the following external components:

Table *97 – Rrefernce External Components*

Symbol	Parameter	Min	Typ	Max	Unit	Note
C_{EXT}	External filter capacitor	-10%	100	+10%	nF	Ceramic low-ESR capacitor between CREF and VSS

Table *98 – Refererences*

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CEXT}	Reference Voltage	-1%	1.8	+1%	V	Low noise trimmed voltage reference – connected to Pad CREF; **do not load**
Δf_{CLK}	Accuracy of Internal reference clock	-10		+10	%	Trimable by serial interface

To reduce the current consumption of the chip, the circuit can be set into a special low power mode with the serial interface bit '**low_power_on**'. All specification parameters except the noise parameters are still valid for this mode.

Table 99 – Internal References Regsiter definitions

Register Definition	Addr.[25]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
References Control	52	0ch					clk_int			low_power_on

Table *100 – Internal references Bit definitions*

Name	Default	Access	Description
clk_int	0b	R/W	Sets the internal CLK frequency used for fuel gauge, DCDCs, PWM, charge pump (000b) – 1.6 MHz (001b) – 1.7 MHz (010b) – 1.8 MHz (011b) – 1.9 MHz (100b) – 2.0 MHz (101b) – 2.1 MHz (110b) – 2.2 MHz (default) (111b) – 2.3 MHz All timings and delays are based on 2.2MHz clk_int
low_power_on	0b	R/W	0 Standard mode 1 Low power mode – all specification except noise parameters are still valid

[25] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

Additional Voltage ref (unfiltered, high impedance, not low noise): 10mV resolution from 0 – 1.8V with an accuracy of +/-1% (invalid if prechage_n = 0),
Current references: 1uA +/- 3% generated by a pmos from V2_5 (one for each analog block)

Low Power Mode

Use bit ***low_power_on*** (reg. References Control) to activate the Low Power Mode. In this mode the on-chip voltage reference and the temperature supervision comparators are operating in pulsed mode. This reduces the quiescent current of the AS3654 by 45µA (typ.). Because of the pulsed function some specifications are not fulfilled in this mode (e.g. increased noise), but still the full functionality is available.
Note: Low power mode can be controlled by the serial interface.

7.24 ON-Detect

The startup- and reset sequences of the device are highly configurable. The configuration of these sequences is defined by the ratio of the internal trimmed bias resistors and RPROGRAM. At the beginning of each reset cycle a 3 bit AD-conversion is performed. The result of this conversion is used to select 1 of 8 possible address-ranges of an internal mask-programmable ROM. The information that is stored in this ROM defines the following parameters:

- power-on sequence and voltage levels of 8 voltage regulators
- duration of the reset cycle (8 possible timer values)

The following values of $R_{PROGRAM}$ are required to select the 8 possible address ranges:

000 open
001 320kΩ
010 160kΩ
011 80kΩ
100 40kΩ
101 20kΩ
110 10kΩ
111 0Ω

Table *101 – ON-Detect Register definitions*

Register Definition	Addr.[26]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Boot_status	74	NA					rom_ valid	rom_adr		

Table *102 – ON-Detect Bits definitions*

Name	Default	Access	Description
rom_adr	(000)b	R	Boot-ROM address
rom_valid	0	R	If '1' Boot-ROM address is valid

[26] Register address codes 00 – 31 are identical to Boot-ROM address codes ROM-adr. 25-30…Power1 Control states at startup sequence

[27] Register address codes 00 – 31 are identical to Boot-ROM address codes ROM-adr. 25-30…Power1 Control states at startup sequence

8.2 Packaging and Pinout

8.2.1 Pin Description

Table *113 – Pinlist CTBGA100,9x9mm (AS3654)*

Pin	Name	Type	Supply	Description
	Charger			
K9	V_USB	P		USB voltage supply input
K8	VSUP_USB	P		Supply output of USB charger (connect to Vsupply)
H9	VCHARGER	P		High voltage input coming from the charger; if the charger is used connect a ceramic capacitor of 1µF
K10	VGATE	A		Switch ON control pin for the external PMOS Fet transistor of the charger step down converter
J10	VOFF_B	A		Switch OFF control pin for the external PMOS Fet transistor of the charger step down Buck converter
H10	VSS_CH	P		Ground pad of Step down Charger
E9	VBAT_SW1	P	VBAT	Battery switch input1 (battery side)
E10	VBAT_SW2	P	VBAT	Battery switch input2 (battery side)
F10	VSUP_SW1	P	Vsupply	Battery switch input1 (supply side)
D10	VSUP_SW2	P	Vsupply	Battery switch input2 (supply side)
E6	BAT_SW	A		Battery switch output for external PMOS
J8	CH_SENSE_N	A	Vsupply	Charger step down converter, external shunt resistor negative connection
J9	CH_SENSE_P	A	Vsupply	Charger step down converter, external shunt resistor positive connection
G8	ISENSP	A	V2_5	Positive sensing input voltage for the external charging current shunt resistor
G7	ISENSN	A	V2_5	Negative sensing input voltage for the external charging current shunt resistor
	Serial interface			
A2	SCL	DI	(Vsupply)	SCL input in I²C mode
A1	SDA	DIO	(Vsupply)	SDA input / output in I²C mode
	Control interfaces			
C2	XRESET	OD	Vsupply	Bidirectional Reset Pin – add an external pullup resistor to the digital supply
C3	XINT	OD	Vsupply	Interrupt Pin - add an external pullup resistor to the digital supply
J2	XON	IPU	V2_5	Input pin to startup the system (power on), internal pullup, apply zenerzap-programming voltage here
	Internal Refs			
J7	VSUPPLY_5	P		Supply for voltage Measurement, **always** connect to VSUPPLY
H8	V_BAT	P	VBAT	Battery supply for Reference blocks.
H6	RPROGRAM	A	V2_5	Select register setup at startup.
G10	V2_5	P		Internal regulator analogue output
F9	CREF	A	V2_5	Reference voltage bypass capacitor connection
F8	RBIAS	A	V2_5	Internal Bias Reference Resistor (connect 220kΩ resistor)
G9	GND_SENSE	P	VSSA	GND reference for analog blocks (connect to GND plane separate)
H7	ADC_IN	A	V2_5	Analog input for ADC10
	Current Sinks			
J4	CURR1	A	VCURR	Current sink 1, or GPIO1
H4	CURR2	A	VCURR	Current sink 2, or GPIO2
K3	CURR3	A	VCURR	Current sink 3, or GPIO3
J3	CURR4	A	VCURR	Current sink 4, or GPIO4
K2	CURR5	A	VCURR	Current sink 5
K1	VCURR	A		Supply voltage of GPIOs and current sinks
H5	VSS_CURR	A	VCURR	Ground pad of Current sink
	General Purpose DC/DC Converter1 and 2			

Pin	Name	Type	Supply	Description
C1	VSUPPLY_4	P		Supply for DCDC step up and control interface, **always** connect to VSUPPLY
E4	DCDC_FB1	A	Vsupply	Step up DC/DC converter1 feedback input
D2	DCDC_GATE1	A	Vsupply	Step up DC/DC converter1 control for external mosfet
D3	DCDC_SENSE_P1	A	Vsupply	Step up DC/DC converter1 external shunt resistor positive connection
F3	DCDC_SENSE_P2	A	Vsupply	Step up DC/DC converter2 external shunt resistor positive connection
D4	DCDC_SENSE_N1	A	Vsupply	Step up DC/DC converter1 external shunt resistor negative connection
E3	DCDC_SENSE_N2	A	Vsupply	Step up DC/DC converter2 external shunt resistor negative connection
E2	DCDC_GATE2	A	Vsupply	Step up DC/DC converter2 control for external mosfet
F4	DCDC_FB2	A	Vsupply	Step up DC/DC converter2 feedback input
K4	DCDC_CURR1	A	Vsupply	Step up DC/DC converter2 current source 1
J5	DCDC_CURR2	A	Vsupply	Step up DC/DC converter2 current source 2
	Linear Regulators			
K6	VRF1_IN	P	Vsupply	Supply Pad for RF1 LDO (RF_1), **always** connect to Supply>3.0V
K5	VRF_1	A	VRF_IN	Output voltage of one of the RF LDO's; can be used as High-Side Switch, if used as LDO connect a ceramic capacitor of 1µF (+/-20%) or 2.2µF (+100%/-50%)
J6	VRF2_IN	P	Vsupply	Supply Pad for RF2 LDO (RF_1), **always** connect to Supply>3.0V
K7	VRF_2	A	VRF_IN	Output voltage of one of the RF LDO's; can be used as High-Side Switch, if used as LDO connect a ceramic capacitor of 1µF (+/-20%) or 2.2µF (+100%/-50%)
B7	VDIG1_IN	P	Vsupply	Supply Pad for DIG1 LDO (VDIG_1)
A7	VDIG_1	A	VDIG_IN	Output voltage of one of the DIG LDO's. Connect a ceramic capacitor of 1µF (+/-20%) or 2.2µF (+100%/-50%)
B6	VDIG2_IN	P	Vsupply	Supply Pad for DIG2 LDO (VDIG_2)
A6	VDIG_2	A	VDIG_IN	Output voltage of one of the DIG LDO's. Connect a ceramic capacitor of 1µF (+/-20%) or 2.2µF (+100%/-50%)
	Charge Pump			
B2	VCP_IN	P	Vsupply	Supply Pad for Charge Pump, **always** connect to Supply>3.0V
B4	VCP_N	A	Vsupply	HVS charge pump flying capacitor positive side
B3	VCP_P	A		HVS charge pump flying capacitor negative side
A4	VCP_OUT	A		Charge pump output, connect a ceramic capacitor of 2.2µF (+100%/-50%)
A3	VSS_CP	A	Vsupply	Ground pad of charge pump
	DCDC Step Down			
D1	VSUPPLY_1	P		Supply Pad for DCDC_Step down converter1, **always** connect to VSUPPLY
F2	LX1	A	Vsupply	DC/DC step down converter1 output
G4	FB1	A	Vsupply	DC/DC step down converter1 feedback
E1	PGND1	A	Vsupply	Power Ground of DCDC step down converter1
G1	VSUPPLY_2	P		Supply Pad for DCDC_Step down converter2, **always** connect to VSUPPLY
G2	LX2	A	Vsupply	DC/DC step down converter2 output
G3	FB2	A	Vsupply	DC/DC step down converter2 feedback
F1	PGND2	A	Vsupply	Power Ground of DCDC step down converter2
H1	VSUPPLY_3	P		Supply Pad for DCDC_Step down converter3, **always** connect to VSUPPLY
H2	LX3	A	Vsupply	DC/DC step down converter3 output
H3	FB3	A	Vsupply	DC/DC step down converter3 feedback
J1	PGND3	A	Vsupply	Power Ground of DCDC step down converter3
	Audio			
C10	VSUPPLY_6	P		Supply for VI2S Regulator
D5	VI2S	P		Supply Pad for I2S Interface, Connect to VDAC Supply
C6	SDI1	IPD	VI2S	I2S_1 Data input to DAC

Pin	Name	Type	Supply	Description
C5	SCLK1	IPD	VI2S	I2S_1 Shift clock
D6	LRCLK1	IPD	VI2S	I2S_1 Left/Right clock
C4	SDI2	IPD	VI2S	I2S_2 Data input to DAC
A5	SCLK2	IPD	VI2S	I2S_2 Shift clock
B5	LRCLK2	IPD	VI2S	I2S_2 Left/Right clock (or Master clock input for I2S1: DAC (128*Fsdac))
F7	AGND	A	VDAC	CM voltage bypass capacitor connection (1.45V)
E7	VREF	A	VDAC	VDAC voltage bypass capacitor connection (2.9V)
E8	LINL	A	VDAC	Line input left channel.
D9	LINR	A	VDAC	Line input right channel
B1	GND_SW	O	Vsupply	Digital output for controlling the external NMOS
A10	VDAC	A	VDAC	2.9V Output voltage of one of DAC LDO; Connect a ceramic capacitor of 1µF (+/-20%) or 2.2µF (+100%/-50%)
B9	HP_CM	A	AVDD	Bypass capacitor connection of common mode voltage of Audio headphone amplifier (AVDD/2)
A9	HP_CM_PWR	A	AVDD	Buffered voltage of HP_CM
C9	LINE_CM	A	ALVDD	Bypass capacitor connection of common mode voltage of Audio line out amplifier (ALVDD/2)
D8	LOUT_L	A	ALVDD	Line out output Left channel
C8	LOUT_R	A	ALVDD	Line out output Right channel
C7	ALVDD	P		Supply pad of Line out amplifier
A8	AVDD	P		Supply pad of headphone amplifier
B8	HPL	A	AVDD	Headphone output left channel
B10	HPR	A	AVDD	Headphone output right channel
D7	BVSS	P	AVDD	Power ground of headphone amplifier
E5,F5, F6,G5 ,G6	VSSA	VSS		Analog Ground Pads

Pin Types:

- I Digital Input Pin
- IPD Digital Input Pin with internal pull-down resistor
- IPU Digital Input Pin with internal pull-up resistor
- IODPU Digital Input / Open Drain Output Pin with internal pull-up resistor
- O Digital Output Pin
- OD Digital Open Drain Output Pin; requires external pull-up resistor
- IO Digital Input / Output Pin
- A Analogue Pin
- P Power Pin

8.3 Registermap

Table *114 – Registermap*

Register Definition	Addr.[28]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Step Down Voltage1	00	ROM	sd1_clkinv	sd1_frequ	step_down1_v					
Step Down Voltage2	01	ROM	sd2_clkinv	sd2_frequ	step_down2_v					
Step Down Voltage3	02	ROM	sd3_clkinv	sd3_frequ	step_down3_v					
LDO_RF1 Voltage	03	ROM		rf1_swprot_en	rf1_lcurr_en	ldo_rf1_v				
LDO_RF2 Voltage	04	ROM				ldo_rf2_v				
LDO_DIG1 Voltage	05	ROM			ldo_dig1_v					
LDO_DIG2 Voltage	06	ROM			ldo_dig2_v					
USB ChargerControl	07	ROM (52h)	ext_batsw_en	No_charging	usb_prio	usb_chgEn	usb_Current			
ChargerControl1	08	ROM (41h)	Isolate_bat	Boost	trickle_tmax	Pulse	Auto Resume	~~Fast~~	BatType	ChEn
Battery voltage monitor	09	ROM (1dh)		SupResEn	ResVoltFall			ResVoltRise		
Charger Config	10	ROM (26h)	ChVoltResume			DisOWB	DisBDet	ChVoltEOC		
ChargerTiming	11	ROM (4bh)	TPOFFMAX		TPOFF			TPON		
FuelGauge	12	ROM (01h)					CalMod	CalReq	UpdReq	FGEn
ChargerCurrent	13	ROM (2Eh)	ch_voltage			ConstantCurrent			TrickleCurrent	
Charge Pump Control	14	ROM (00h)						cp_clkinv	cp_freq	cp_pulseskip
Step Up DC/DC Control	15	ROM (00h)	stpup2_res	stpup2_fastskip	stpup2_freq		stpup1_res	stpup1_fastskip	stpup1_freq	
Step Up1 DC/DC Control	16	ROM (00h)		stpup1_oc_timeout	stpup1_shortprot	stpup1_clkinv	stpup1_v			
Step Up2 DC/DC Control	17	ROM (00h)	stpup2_prot	stpup2_clkinv	stpup2_fb		stpup2_v			
GPIO 1	18	ROM (07h)	gpio1_pulls		gpio1_invert	gpio1_iosf		gpio1_mode		
GPIO 2	19	ROM (07h)	gpio2_pulls		gpio2_invert	gpio2_iosf		gpio2_mode		
GPIO 3	20	ROM (07h)	gpio3_pulls		gpio3_invert	gpio3_iosf		gpio3_mode		
GPIO 4	21	ROM (07h)	gpio4_pulls		gpio4_invert	gpio4_iosf		gpio4_mode		
Reset Timer	22	ROM (0Fh)					xon_enable	res_timer		
Reg Power1 Ctrl	23	ROM	cp_on	sd3_on	sd2_on	sd1_on	ldo_dig2_on	ldo_dig1_on	ldo_rf2_on	ldo_rf1_on

[28] Register address codes 00 – 31 are identical to Boot-ROM address codes

ROM-adr. 25-30...Power1 Control states at startup sequence

Register Definition	Addr.[28]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Reg Power1 Ctrl Startup 1..6msec	24-30	ROM								
Reg Power2 Ctrl	31	ROM					stpup2_on	stpup1_on	rf2_sw	rf1_sw
Step Down Control1	32	00h	sd2_nsw_on	sd2_4u7	sd2_dis_n	sd2_psw_on	sd1_nsw_on	sd1_4u7	sd1_dis_n	sd1_psw_on
Step Down Control2	33	00h	sd3_dis_pon	sd2_dis_pon	sd1_dis_pon	sdX_lpo	sd3_nsw_on	sd3_4u7	sd3_dis_n	sd3_psw_on
Step down charger control	34	00h		sd3_dis_curmin	sd2_dis_curmin	sd1_dis_curmin				sdc_frequ
DCDC_CURR1 value	35	00h		dcdc_curr1_low_bias	dcdc_curr1_current					
DCDC_CURR2 value	36	00h		dcdc_curr2_low_bias	dcdc_curr2_current					
CURR1 value	37	00h		curr1_low_bias	curr1_current					
CURR2 value	38	00h		curr2_low_bias	curr2_current					
CURR3 value	39	00h		curr3_low_bias	curr3_current					
CURR4 value	40	00h		curr4_low_bias	curr4_current					
CURR5 value	41	00h		curr5_low_bias	curr5_current					
ADC idac	42	00h					adc_idac			
Interrupt Mask1	43	FFh	LowBat_int_m	ovtmp_int_m	onkey_int_m	chdet_int_m	usb_chdet_int_m	trickle_tmax_int_m	cheoc_int_m	chstate_int_m
Interrupt Mask2	44	FFh	stpup1_int_m	hpdet_int_m	hphcurr_int_m	dig2_lv_int_m	dig1_lv_int_m	sd3_lv_int_m	sd2_lv_int_m	sd1_lv_int_m
Interrupt Status1	45	NA	LowBat_i	ovtmp_i	onkey_i	chdet_i	usb_chdet_i	trickle_tmax_i	cheoc_i	chstate_i
Interrupt Status2	46	NA	stpup1_i	hpdet_i	hphcurr_i	dig2_lv_i	dig1_lv_i	sd3_lv_i	sd2_lv_i	sd1_lv_i
Low voltage Status	47	40h	stpup1_det	stpup1_oc	hpdet	dig2_lv	dig1_lv	sd3_lv	sd2_lv	sd1_lv
GPIO Signal	48	NA	gpio4_in	gpio3_in	gpio2_in	gpio1_in	gpio4	gpio3	gpio2	gpio1
PWM Frequency Control High Time	49	00h	pwm_h_time							
PWM Frequency Control Low Time	50	00h	pwm_l_time							
CURR control	51	00h			curr5_ctrl		dcdc_curr2_ctrl		dcdc_curr1_ctrl	
References Control	52	0ch					clk_int			low_power_on
Watchdog Control	53	02h						wtdg_trigger	wtdg_res_on	wtdg_on
Watchdog_min Timer	54	00h	wtdg_min_timer							
Watchdog_max Timer	55	FFh	wtdg_max_timer							

Register Definition	Addr.[28]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Watchdog Software Signal	56	00h								wtdg_sw_sig
Audio Set1	57	00h			mclk_invert	aud_ldo_on	gnd_sw_on	mux_sel	dac_on	lin_on
Audio Set2	58	00h	I2S_mclk_en	I2S_select	ibr_hph			dith_on	ibr_dac	
HPH out R	59	00h	hp_ovc_to		hpcm_off	hpr_vol				
HPH out L	60	00h	hp_mute	hp_on	hpdeton	hpl_vol				
Line out R	61	00h	ibr_line			liner_vol				
Line out L	62	00h	line_mute	line_on		linel_vol				
ADC_control	63	00h	start_conversion	adc_on		adc_slow	adc_test	adc_select		
ADC_MSB result	64	NA	result_not_ready	D9	D8	D7	D6	D5	D4	D3
ADC_LSB result	65	NA						D2	D1	D0
ChargerStatus	66	NA		NoBat	EOC	CVM	Trickle	Resume	ChAct	ChDet
ChargerStatus_usb	67	NA					batsw_on	batsw_mode	USB_ChAct	USB_ChDet
$DeltaCharge_{MSB}$	68	NA	sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
$DeltaCharge_{LSB}$	69	NA	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
$ElapsedTime_{MSB}$	70	NA	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
$ElapsedTime_{LSB}$	71	NA	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
Reset Control	72	00h			reset_reason			xon_input	power_off	force_reset
Overtemperature Control	73	00h	tco_140_a	tco_110_a	temp_test1	temp_test0	rst_ov_temp_140	ov_temp_140	ov_temp_110	temp_pmc_on
Boot_status	74	NA					rom_valid	rom_adr		
Test_enable	75	00h	test_en_code							
Testmux Control N	76	00h				mux_ctrl_n				
Testmux Control P	77	00h				mux_ctrl_p				
Digital Testmux	78	00h						DigTestMux		
Testmode control1	79	00h	serial_tm	NoReset	zzap_force_readout	zzap_testmode	quasitrimen	digmuxEn	anamuxEn	atpg_mode
Testmode control2	80	00h	rom_test	cp_tm	sdX_tm2	sdX_tm1	sdX_del50	stpup_tm2	stpup_tm1	ext_clk
Testmode control3	81	00h	aud_rtm	adc3_tm	batsw_tm	ch_sdtm	aud_17db_test	charger_dishyst	charger_tm	aud_ltm
Testmode idac	82	00h	idac<7:0>							
Testmode vsupply_l	83	00h	vsupply<7:0>							
Testmode vsupply_h	84	00h						preset_en	vsupply<9:8>	
ASIC ID 1	85	NA	1	1	0	0	1	1	0	1
ASIC ID 2	86	NA	0	1	0	1	rev			
Zener Zap lsb	87	NA	RefOsc1Mhz1		Vref_Trim					
Zener Zap msb	88	NA	smc_ihold	smc_ioff		smc_ion		VrefLpTrim		

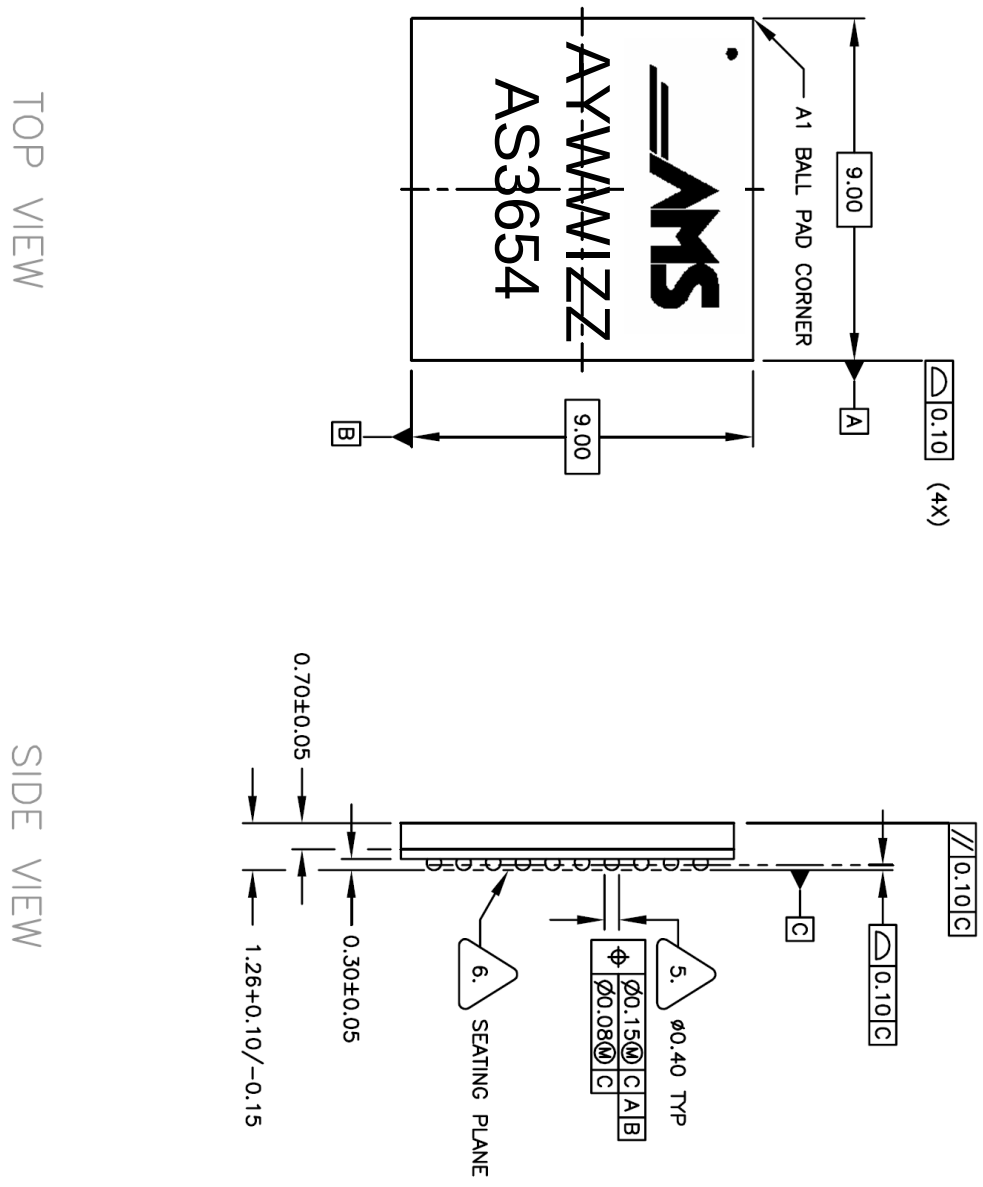
Register Definition	Addr.[28]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
							Read Only			

8.4 Pinout Drawing (Top view) CTBGA100 9x9mm:

	1	2	3	4	5	6	7	8	9	10
A	SDA	SCL	VSS_CP	VCP_OUT	SCLK2	VDIG2	VDIG1	AVDD	HP_CM_PWR	VDAC
B	GND_SW	VCP_IN	VCP_P	VCP_N	LRCLK2	VDIG2_IN	VDIG1_IN	HPL	HP_CM	HPR
C	VSUPPLY_4	XRESET	XINT	SDI2	SCLK1	SDI1	ALVDD	LOUT_R	LINE_CM	VSUPPLY_6
D	VSUPPLY_1	DCDC_GATE1	DCDC_SENSE_P1	DCDC_SENSE_N1	VI2S	LRCLK1	BVSS	LOUT_L	LINR	VSUP_SW2
E	PGND1	DCDC_GATE2	DCDC_SENSE_N2	DCDC_FB1	VSSA	BAT_SW	VREF	LINL	VBAT_SW1	VBAT_SW2
F	PGND2	LX1	DCDC_SENSE_P2	DCDC_FB2	VSSA	VSSA	AGND	RBIAS	CREF	VSUP_SW1
G	VSUPPLY_2	LX2	FB2	FB1	VSSA	VSSA	ISENSEN	SENSEP	GND_SENSE	V2_5
H	VSUPPLY_3	LX3	FB3	CURR2	VSS_CURR	RPROGRAM	ADC_IN	V_BAT	VCHARGER	VSS_CH
J	PGND3	XON	CURR4	CURR1	DCDC_CURR2	VRF2_IN	VSUPPLY_5	CH_SENSE_N	CH_SENSE_P	VOFF_B
K	VCURR	CURR5	CURR3	DCDC_CURR1	VRF1	VRF1_IN	VRF2	VSUP_USB	V_USB	VGATE

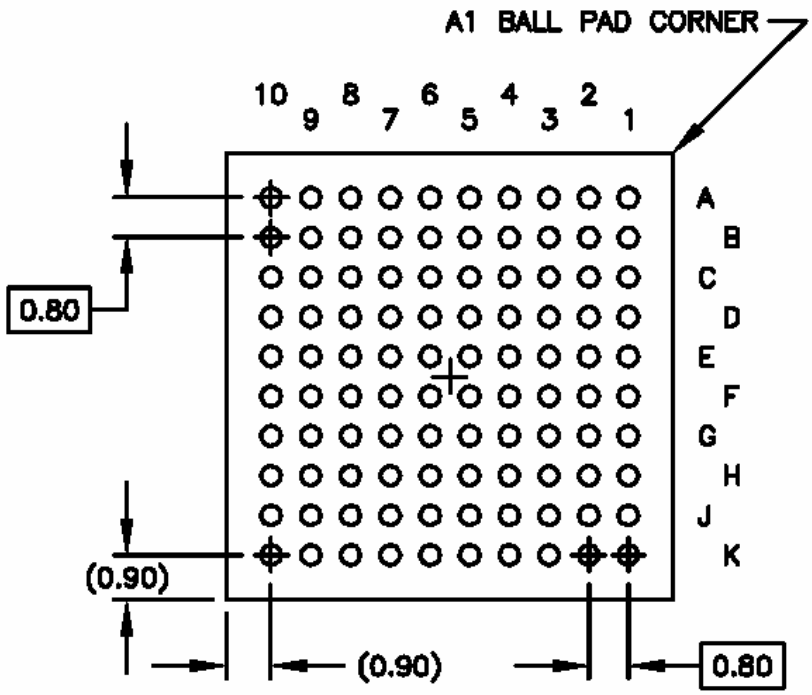
8.6 Package and Marking

8.6.1 CABGA100_9x9mm 0.8mm pitch(AS 3654)



Marking: **A Y W W I Z Z**

A	.....	Pb free
Y	.....	year
WW	.....	week
I	.....	plant identifier
ZZ	.....	letters of free choice



BOTTOM VIEW

100 SOLDER BALLS