CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX7011
Digital Voice Processor

D/7011_FI1.x/1 Apr 2012

DATASHEET

Advance Information

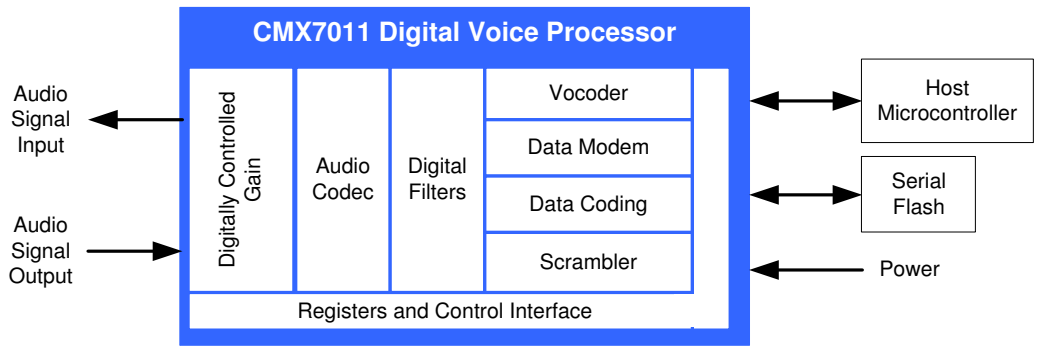
7011FI-1.x: Digital Voice Scrambler for Analogue Radio Systems

Features

- Simple integration directly into the radio audio path via the audio input/output connections
- Improved performance offers better quality than traditional analogue scrambling
- Ultimate in high-level analogue radio security
- Embedded internal scrambling algorithm
- External scrambling option via external microcontroller
- Progammable instant voice capture
- Flexible 256 address programming
- Integrated RALCWI vocoder
- RALCWI licence included (royalty free)
- Embedded data modem with robust and proven modulation scheme
- Small 48-pin LQFP/VQFN package options

Applications

- Implementation of digital voice within analogue PMR
- Secure scrambling add on to existing radios
- Wireless door access systems
- Wireless gate entry systems



1 Brief Description

The CMX7011 is a flexible, half duplex, digital voice processor specifically designed for digital voice scrambling applications that transmits and receives secure voice via an embedded robust data modem for use within an analogue PMR. The device allows simple implementation and configuration within existing designs and is intended to be added to a radio via an accessory module or “feature socket”. The device is simple to control via a small, low-power microcontroller. The CMX7011 offers better quality speech than that of traditional analogue radios and, using the internal digital scrambling algorithm, significantly higher

levels of security are achieved. The voice scrambling function is provided by an internal digital voice scrambler algorithm. Alternatively, external scrambling is possible via the host microcontroller.

Built in to the CMX7011 is CML's proven and reliable RALCWI (Robust Advanced Low Complexity Waveform Interpolation) vocoder providing near toll quality speech at low bit rates. One of the most significant features in the CMX7011's design is the programmable push-to-talk (PTT) buffer which offers instant voice capture in transmit mode. The PTT buffer temporarily stores the initial part of the speech and can therefore eliminate clipping that can be caused by the time taken to decode sub audio signals like CTCSS and system delays caused by repeaters. Within the CMX7011's header frame is a user-programmable 8-bit address field which allows up to 256 individual user addresses to be defined.

Function Image™. The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™ data file that is uploaded during device initialisation and defines the device's function and feature set. New features and enhancements to existing functions may be provided from time to time, expanding the capabilities of the device. These will also be provided as Function Images™ which can be downloaded from the CML Technical Portal, a secure area of the CML web site. Details of currently available Function Images™ can be found in the CMX7011 product page on the CML website.

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

This Data Sheet is the first part of a two-part document.

CONTENTS

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
1	First release, Advance Information	Apr 2012

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document. Information in this advance document should not be relied upon for final product design.

2 Block Diagram

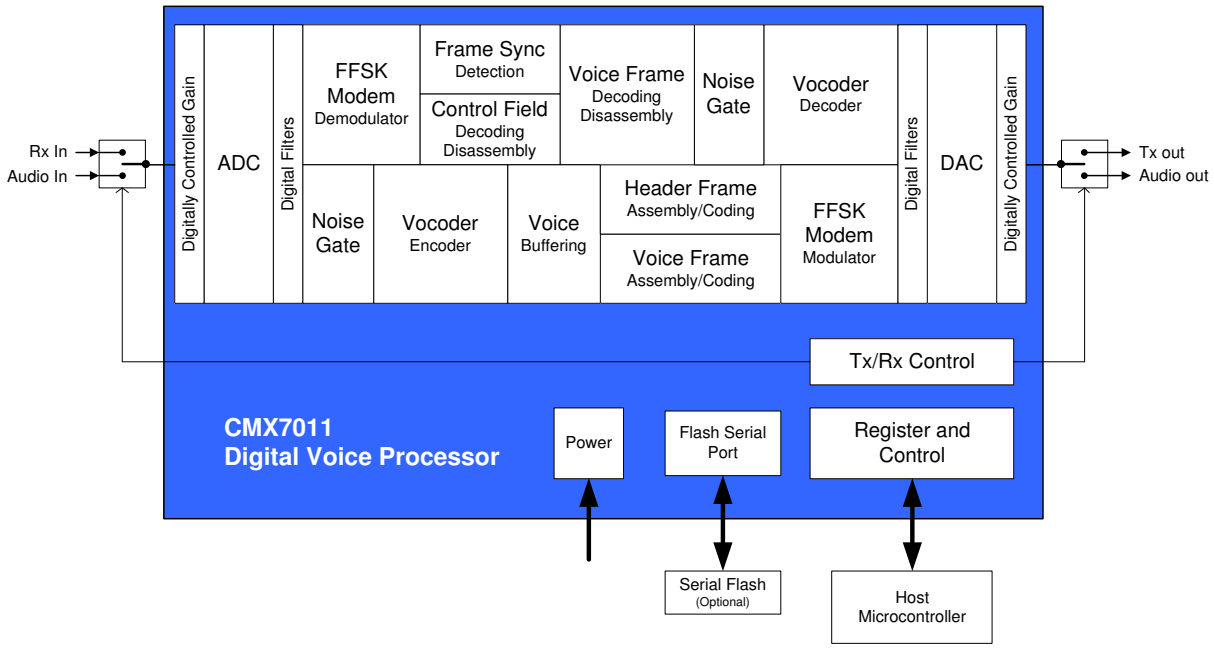


Figure 1 Block Diagram

3 Pin and Signal List

CMX7011 L4/Q3	Pin		Signal Description	
Pin No.	**Name**	**Type**		
1	AVDD	Power	Analogue Positive Power Supply 3.3V	
2	AVSS	Power	Analogue Negative Power Supply 0V	
3	VBIAS	Analogue Output	Analogue Bias (approximately 1.65 Volts)	
4	VSSREF	Power	Analogue Negative Reference	
5	INPUTP	Analogue Input	Audio CODEC Positive Input (self biased)	
6	INPUTN	Analogue Input	Audio CODEC Negative Input (self biased)	
7	AVDD	Power	Analogue Positive Power Supply 3.3V	
8	AVSS	Power	Analogue Negative Power Supply 0V	
9	VSSPA	Power	Output Amplifier Negative Power Supply 0V	
10	OUTP	Analogue Output	Audio CODEC – Amplifier Positive Output	
11	OUTN	Analogue Output	Audio CODEC – Amplifier Negative Output	
12	VDDPA	Power	Output Amplifier Positive Power Supply 3.3V	
13	DVDD	Power	Digital Positive Power Supply 1.8V	
14	GPIO3	Digital Input/Output	General Purpose Input/Output	
15	SDI	Digital Input	SSP port serial data input	FLASH PORT
16	SDO	Digital Output	SSP port serial data output	
17	SCLK	Digital Input	SSP port serial clock input	
18	~	NC	Reserved for future use. Do not connect to this pin.	
19	GPIO1	Digital Input/Output	General Purpose Input/Output	
20	GPIO2	Digital Input/Output	General Purpose Input/Output	
21	SSOUT	Digital Output	SSP Slave Select	
22	DVSS	Power	Negative Power Supply 0V	
23	~	NC	Reserved for future use. Do not connect to this pin.	
24	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
25	~	NC	Reserved for future use. Do not connect to this pin.	

CMX7011 L4/Q3	Pin		Signal Description	
Pin No.	**Name**	**Type**		
26	DVSS	Power	Negative Power Supply 0V	
27	XTAL/CLK	Input	Crystal Input	
28	XTALN	Output	Crystal Output	
29	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
30	RESETN	Digital Input	General Reset (active low)	
31	XTALSEL1	Digital Input	These bits select the crystal/clock frequency, according to Table 3.	
32	XTALSEL2	Digital Input		
33	XTALSEL3	Digital Input		
34	ENABXTAL	Digital Input	Enable Crystal Oscillator/External Clock Input	
35	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
36	~	NC	Reserved for future use. Do not connect to this pin.	
37	~	NC	Reserved for future use. Do not connect to this pin.	
38	~	NC	Reserved for future use. Do not connect to this pin.	
39	~	NC	Reserved for future use. Do not connect to this pin.	
40	~	NC	Reserved for future use. Do not connect to this pin.	
41	VSS	Power	Negative Power Supply 0V	
42	CLK	Digital Input	C-BUS Serial Clock	C-BUS
43	CDATA	Digital Input	C-BUS Command Data	
44	RDATA	Tri-state output	C-BUS Reply Data	
45	CSN	Digital Input	C-BUS Chip Select (bar)	
46	IRQN	Open Drain Digital Output	C-BUS Interrupt Request (bar)	
47	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
48	VDD	Power	Digital Positive Power Supply 1.8V	
EXPOSED METAL PAD	SUB	NC	On the Q3 package only, the central metal pad may be connected to Analogue Ground (Avss) or left unconnected. **No other electrical connection is permitted.**	

Table 1 Pin List and Functions

4 External Components

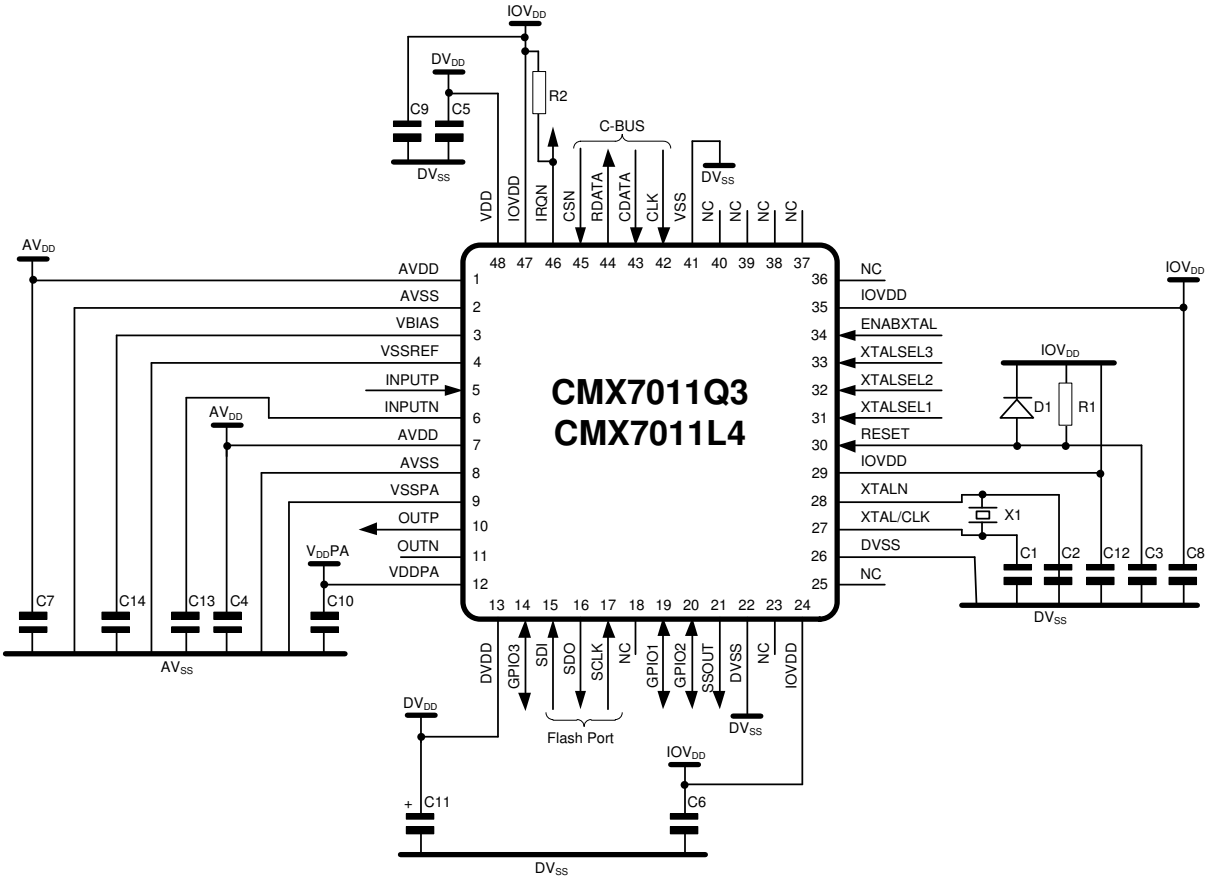


Figure 2 Recommended External Components

C1	22pF	C7	100nF	C13	100nF
C2	22pF	C8	100nF	C14	100nF
C3	1.0µF	C9	100nF		
C4	100nF	C10	100nF	R1	470kΩ
C5	1.0µF	C11	1.0µF	R2	100kΩ
C6	100nF	C12	100nF	D1	small signal diode

Table 2 Recommended Component Values

Notes: 1. On the CMX7011, the crystal selection pins (XTALSEL1, XTALSEL2 and XTALSEL3) must be permanently tied to either IOVDD or VSS and not driven from a logic level output of the host µController (see Table 3 for a list of crystal frequencies). For 9.6MHz and 12.0MHz operation, either a crystal or a clock can be used. For all other frequencies, a clock must be injected into the XTALIN pin and the XTALOUT pin must be left unconnected.

2. To use the CMX7011, tie the ENABXTAL pin to IOV_{DD}. If the ENABXTAL pin is connected to VSS it will force the device into a deep powersave mode, where the C-BUS interface and clock input (XTALIN) are disabled and the crystal oscillator is powered down.

3. A single 10µF electrolytic capacitor may be fitted in place of C5 and C11, providing the two V_{DD} pins are connected together on the pcb with an adequate width power supply trace.

Crystal Select Input Pins:			Clock/Crystal Frequency	Clock/Crystal Choice
XTALSEL3	XTALSEL2	XTALSEL1		
0	0	1	9.6MHz	crystal or clock
0	1	0	12.0MHz	crystal or clock
0	1	1	14.4MHz	external clock only
1	0	0	16.8MHz	external clock only
1	0	1	19.2MHz	external clock only
1	1	0	21.6MHz	external clock only
1	1	1	24.0MHz	external clock only

Table 3 Clock/Crystal Selection

5 PCB Layout Guidelines and Power Supply Decoupling

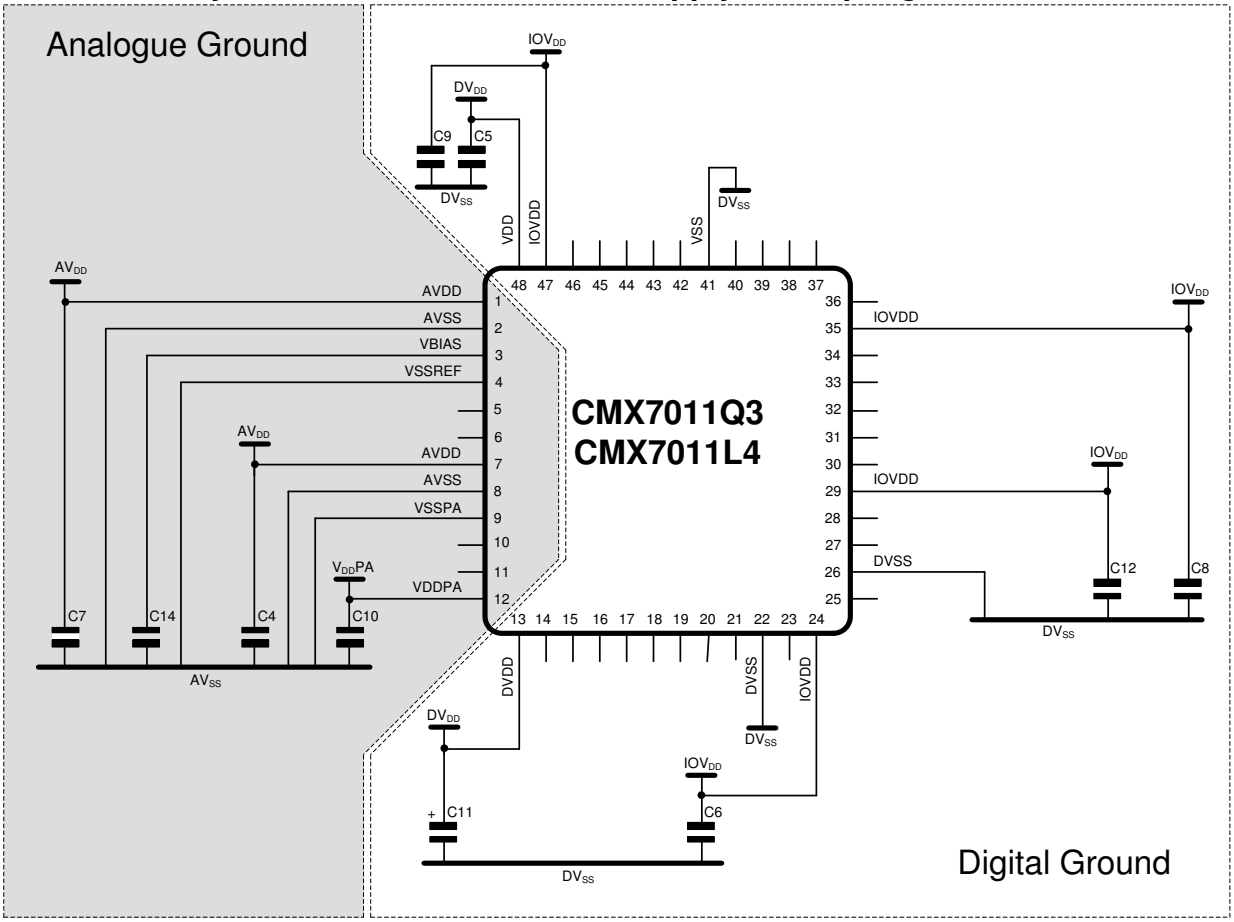


Figure 3 CMX7011 Power Supply and De-coupling

Component values as per Figure 3.

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7011 and the power supply and bias de-coupling capacitors. The de-coupling capacitors C4, C6, C7, C8, C9, C10, C12, C13 and C14 should be as close as possible to the CMX7011. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and (digital) V_{SS} supplies in the area of the CMX7011, with provision to make links between them close to the CMX7011. The use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers. The layout of a CMX7011printed circuit board should make use of a single ground plane covering the whole chip area shown above.

On the CMX7011, V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set an external mid-point reference, it must be buffered with a high input impedance buffer.

6 General Description

The CMX7011, when loaded with FI-1.x, is a half duplex, secure digital voice processor for use within an analogue PMR. The device uses an FFSK transmit/receive modem, a secure internal scrambling algorithm (with an option to use external scrambling via the host microcontroller), a press-to-talk (PTT) speech buffer with programmable instant voice capture to avoid traditional PTT clipping, and CML's proprietary RALCWI vocoder which offers near-toll quality encoding/decoding using a very low bit rate algorithm. The CMX7011 has four basic modes of operation:

- Digital Voice transmit mode using internal scrambling
- Digital Voice transmit mode using external scrambling
- Digital Voice receive mode using internal scrambling
- Digital Voice receive mode using external scrambling

Control of the CMX7011 is via a C-BUS serial port from the host microcontroller. Each of the functional block descriptions below will reference the relevant C-BUS register used to control that function. The individual register name is then described in more detail within the C-BUS registers section later in this document.

7 Detailed Descriptions

7.1 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7011 and the host microcontroller; this interface is compatible with Microwire/SPI. Interrupt signals notify the host microcontroller when a change in status has occurred and the microcontroller should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set.

To minimise activity on the C-BUS interface, optimise response times and ensure reliable data transfers, it is advised that the IRQ facility be used (using the IRQ enable register, $1F). It is permissible for the host to poll the IRQ pin if the host does not support a fully interrupt-driven architecture. This removes the need to continually poll the C-BUS status register ($40) for status changes.

7.1.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the internal registers of the CMX7011 and the host µC, by using the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the µC, which may be followed by a data word sent from the µC (written into one of the Write-Only Registers), or a data word sent to the µC (read out from one of the Read-Only Registers). All C-BUS data words are a multiple of 8 bits wide, the width depending on the source or destination register. Note that certain C-BUS transactions require only an address byte to be sent from the µC, no data transfer being required. The operation of the C-BUS is illustrated in Figure 4.

Data sent from the microcontroller on the CDATA (command data) line is clocked into the CMX7011 on the rising edge of the CLK input. Data sent from the CMX7011 to the µC on the RDATA (reply data) line is valid when CLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Figure 4 and Figure 5 give detailed C-BUS timing requirements.

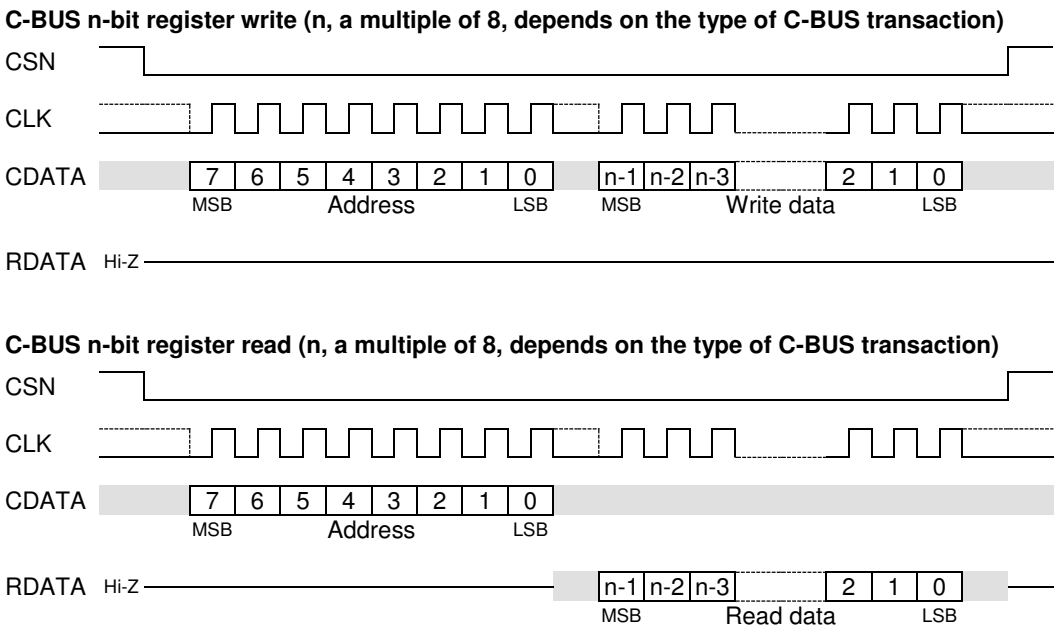


Figure 4 Basic C-BUS Transactions

To increase the data bandwidth between the µC and the CMX7011, certain of the C-BUS read and write registers are capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words via a FIFO, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 5.

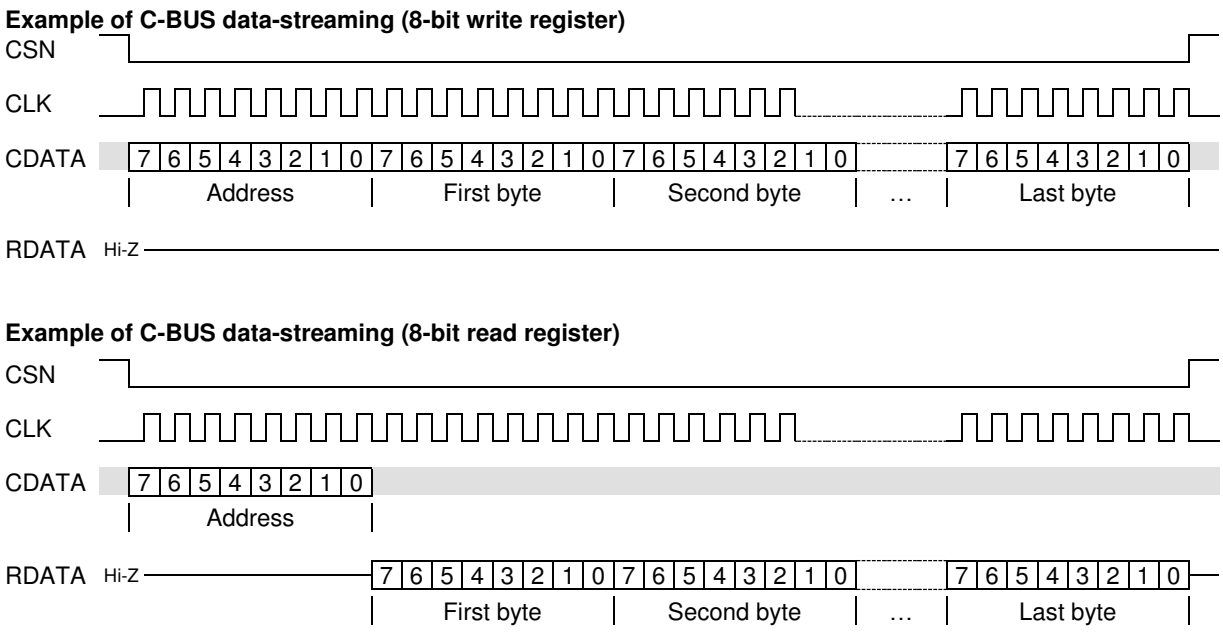


Figure 5 C-BUS Data-Streaming Operation

Filling a FIFO to a pre-determined level (e.g. 128 bytes) can be done in one of two ways:

1) Stream an entire C-BUS message consisting of 1 address byte followed by 128 data bytes to the FIFO.

2) Stream multiple C-BUS messages consisting of any number of address bytes from 1 - 128 and any number of data bytes from 1 - 128, as long as 128 data bytes eventually get across into the FIFO.

i.e. i) 128 x single C-BUS writes is a valid transfer (128 address bytes + 128 data bytes)
ii) 64 x C-BUS writes is a valid transfer (64 address bytes + 64*2 data bytes)

It is not a requirement that data MUST be streamed into the FIFOs in one single transaction. If it is more convenient, the data streaming facility need not be used at all.

7.2 Input Stage

Voice is fed in to the CMX7011 via the audio inputs at pins 5 and 6 via a variable analogue input gain stage. This input stage includes up to 22.5dB of switchable gain in 1.5dB steps. The input gain blocks are provided to allow for inputs from different audio sources. Depending on the type of audio source used, users may wish to consider an external low-noise preamplifier prior to the input stage. The gain is controlled by the register $05 - AIG (analogue input gain). In addition to the variable gain there is also an additional 20dB of gain available (microphone amplifier gain) in a single step (also controlled by the analogue input gain register). If the user requires an input gain in the order of 20dB or above, the use of this single gain stage is advised to provide the bulk of the gain. Any additional smaller increments can then be added using the variable gain. Using this approach means that the best noise performance will be achieved.

7.3 Peak Level Function

The 20ms voice frames may be passed through a peak level measurement function which may be used to determine when the input signal is approaching the threshold at which clipping occurs. The peak level function monitors each 20ms block of speech (160 discrete samples) and will select the sample with the highest value and write the value to the PLEVEL register. This information is useful for setting the value of the input gain stage to obtain the best possible performance of the CMX7011. The function is switched on and off via the PLV register and is controlled by the one of the bits in the CTRL register.

7.4 Noise gate

The programmable noise gate stage that follows peak level detection removes the background noise between speech pauses and can be used to remove noise generated in front-end analogue circuitry or the effects of ambient noise.

Three parameters control the noise gate. An upper threshold level value controls the point at which the gate opens and allows audio to pass. A lower threshold value controls the point at which the gate closes thereby preventing audio to pass. These two parameters together control the hysteresis and prevent 'chattering'. A third parameter controls how many consecutive frames of audio must be below the lower threshold before the gate closes. This 'gate shut delay' prevents the tail end of words (like a trailing 's') from being clipped.

Once the gate shut delay has expired, the gate does not shut abruptly, but closes over a period of 16 frames. Each frame has progressively more attenuation applied, until the frames are silent. This happens in approximately 6dB steps. The diagram below illustrates the difference between a gated and non-gated signal and clearly shows the improvement in background noise level which is a benefit that this stage brings.

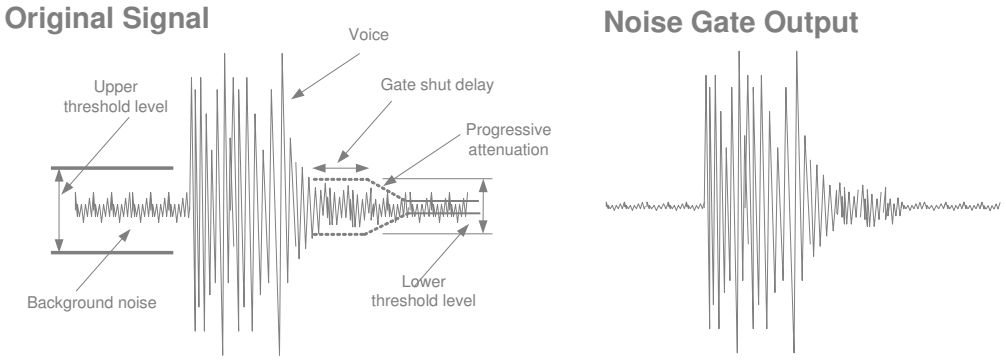


Figure 6 Noise Gate Behaviour

The various parameters of the noise gate such as upper threshold, lower threshold, mute, and gate shut delay are controlled by dedicated C-BUS registers described later.

7.5 Vocoder

The voice encoding/decoding is performed by a low data rate vocoder algorithm which is based on Robust Advanced Low Complexity Waveform Interpolation (RALCWI) technology.

RALCWI technology uses unique proprietary signal decomposition and parameter encoding methods, ensuring high voice quality at high compression ratios. The voice quality of RALCWI-class Vocoders, as estimated by independent listeners, is similar to that provided by standard Vocoders running at bit rates above 4000 bps. The Mean Opinion Score (MOS) of voice quality for this Vocoder is about 3.5-3.6. This value was determined by a paired comparison method, performing listening tests of developed and standard voice Vocoders.

Both input and output stages include a high-order digital channel filter, to constrain the input and output signals to an audio bandwidth of 4kHz. This avoids the necessity of adding external third (or higher) order filters, thus saving external components.

7.6 Internal Scrambling

Internal scrambling is implemented with a 16-bit pseudo-random sequence which operates on all data bits after the header frame. The scrambler uses start codes ('seeding') which means that the sequence will be seeded to start from any value other than zero. System security is improved because only receivers with the same seed can descramble and decode the transmitted data.

There are 16 possible scramble seeds and these values are held in an internal table - two of the values are not modifiable (scramble "whitening" or scramble disabled). It is also possible to program new scramble seed values into the table. This is covered in more detail in the C-BUS register descriptions.

7.7 External Scrambling

If external scrambling is used the vocoder output must be redirected to the host microcontroller. This is controlled by setting one of the bits in the SCRAMBLE register to external scrambling. Each 6-byte frame of encoded speech will be fed to the first of two FIFOs. The FIFO can accommodate a maximum of 20 frames of data which will be read by the host microcontroller. In practical terms however, this is likely to be 1, 2 or 3 frames. These frames of data are passed out of the CMX7011 to the host and back again under the control of the C-BUS ODATA and IDATA which are the streaming data output and input registers respectively. Whilst this is happening, other internal processing can continue. However, if the frames of data sent to the host are not received due to an external delay, this will create a FIFO underrun condition. Similarly, if the PTT buffer is fed with too many frames of data, this will create a FIFO overrun condition. For either of these conditions a host interrupt will be generated and reads an appropriate bit into the vocoder frame flow status register (FSTAT).

7.8 Instant Voice Capture

The CMX7011 features an instant voice capture feature which adds a delay between the time when the device starts to encode voice for transmission to the time when it actually transmits the encoded voice. This is useful because in an analogue PMR radio network there are various inherent system delays which can all contribute to an overall time lag before a receiving device starts to respond to a transmission. Examples of such delays are: time taken to decode a CTCSS sub-audio signal, and system delays introduced by repeaters. The PTT buffer allows a user to programme delay times between 0 and 600ms. The delay times are specified in frames, and the function is controlled by the PTTDELAY register described in the C-BUS register section.

The following diagram illustrates how the PTT delay buffer is implemented.

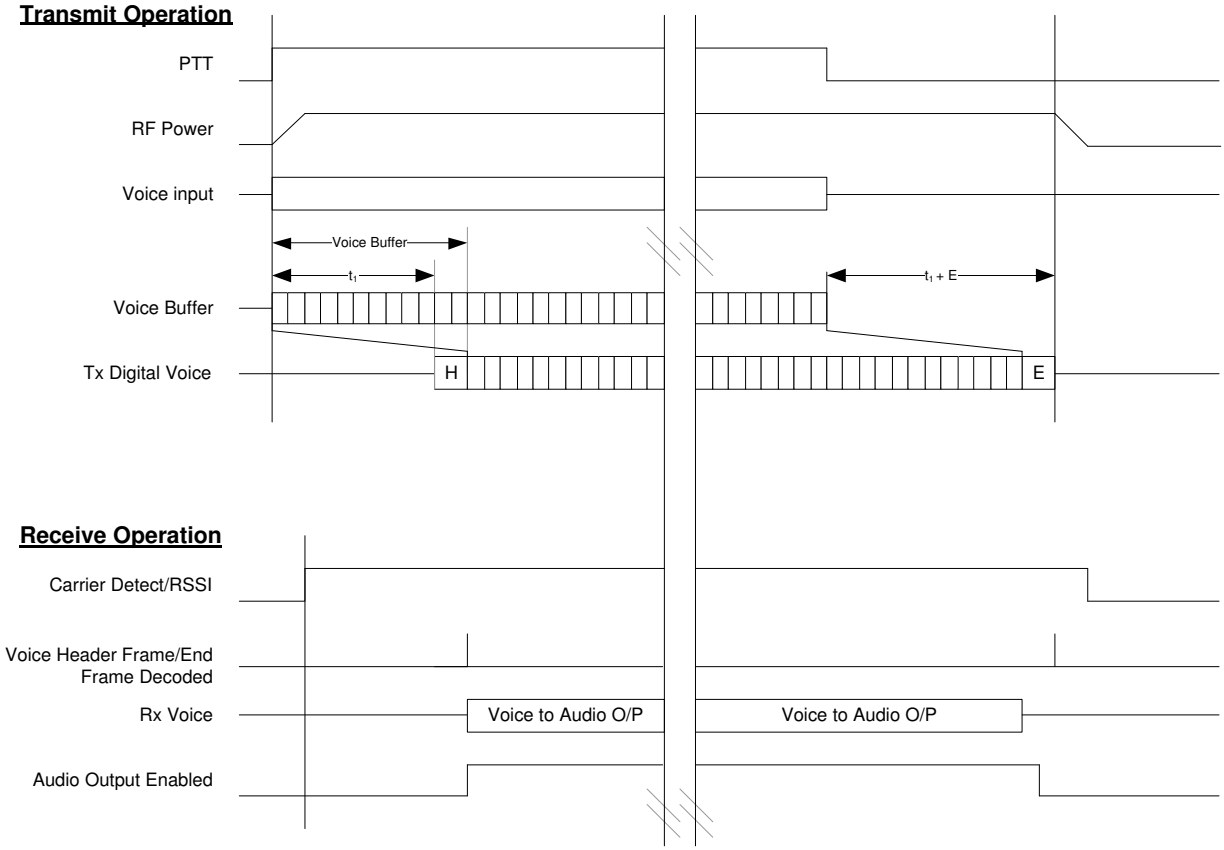


Figure 7 Typical Timing for PTT Delay

In Figure 7 it can be seen that from the time that the PTT button is engaged, there will be a small finite time taken for the RF power to ramp up from zero to full operating power. However, voice input will be captured immediately and vocoded voice data will be buffered in RAM on a frame-by-frame basis. In the example, 12 frames are buffered and this includes the header frame time. Therefore the actual transmission of digital voice is delayed by a period equal to t_1 plus the header frame time. At the end of the transmit operation, following the last frame of buffered voice frames, the actual transmission will continue for a period equal to t_1 plus the end-of-voice (EOV) frames time. The host will then be notified when digital voice transmission has finished.

In receive mode, carrier detect/RSSI may be present, but the audio output will not be enabled until the header frame has been correctly detected. Audio output will continue and will be only be disabled once the final end-of-voice frame has been detected.

7.9 Initialisation

On first applying power, three actions have to be performed: the crystal oscillator has to start up (if used), the bias chain has to be powered up, so that the decoupling capacitor (C14) has charged to AV_{DD} / 2, and on-chip digital circuits have to be reset into a known state. The crystal oscillator typically takes much less than 20ms to start up, but the actual time will depend on the ESR of the crystal used. With the components shown in Figure 3, the BIAS pin will take 100ms typically to reach its steady-state value of AV_{DD} / 2. There are two sources of reset:

- pulling the RESETN signal (pin 30) to '0' for at least 200ns, then returning it to '1' (the pin does not have an internal pullup resistor). Note that the device does not have an automatic power-up reset.
- writing to the C-BUS RESET register ($01). This is a 1-byte command which has no data.

A hard reset (taking RESETN low) will also force the ENABXTAL signal low, which disables the clock and powersaves the crystal oscillator. On first applying power, the RESETN pin should be held low until all the power supplies have stabilised, to ensure correct operation of the device. When coming out of a hard reset, the device needs the crystal oscillator to be working, then counts 65,536 clock cycles (= 5.4ms delay with a 12.0MHz clock), then automatically performs a soft reset by writing to the C-BUS RESET register.

A soft reset (writing to the RESET register) will clear all registers to '0', unless noted otherwise – in which case the default settings are restored. The device will be ready to accept C-BUS commands approximately 1.5ms after completion of the soft reset action and will indicate that it is ready by setting bit 15 of the STATUS register ($40) to '1' and also by indicating a C-BUS interrupt request by pulling the IRQN pin low. Note that on reset, the IRQENAB register ($1F) bit 15 will automatically be set to '1', thus enabling the RDY interrupt to activate the IRQN pin.

Connecting the ENABXTAL pin to V_{SS} when the device is operational will force the device into a power-save mode where the C-BUS interface and clock input (XTALIN) are disabled and the crystal oscillator is powered down. However, the BIAS pin and C-BUS registers are not disturbed, so normal operation can be resumed by re-connecting the ENABXTAL pin to IOV_{DD} and waiting for the crystal oscillator to re-start.

The device is now ready to accept the loading of the Function Image™. Please refer to the Application Note in Section 10.1.

7.10 C-BUS register Summary

C-BUS Register Name	C-BUS Address	CMX7011 R/W/CMD	CMX7011 Size (bits)
RESET	$01	CMD	-
SCRAMBLE	$04	W	8
AIG	$05	W	8
AOG	$06	W	8
RADDR	$07	W	8
LADDR	$08	W	8
POWERSAVE	$09	W	8
PTTDELAY	$0A	W	8
EOVCOUNT	$0B	W	8
IDD	$0C	W	8
SVSREQ	$0E	W	8
IOCTRL	$0F	W	8
IDATA	$10	W	8
CTRL	$11	W	16
LSEED	$12	W	16
FSYNC	$13	W	16
IRQENAB	$1F	W	16
FHEADV	$23	R	8
DESCRAMBLE	$24	R	8
ADDRESS	$25	R	8
SVCACK	$2E	R	8
IORD	$2F	R	8
ODATA	$30	R	8
PLEVEL	$31	R	16
STATUS	$40	R	16

Table 4 C-BUS Registers

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

8.1 Performance Specification

8.2 Electrical Performance

8.2.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Power Supplies			
IOV_{DD} - V_{SS}	-0.3	4.0	V
V_{DD} - V_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
V_{DD}PA - V_{SS}PA	-0.3	4.0	V
Voltage on any pin to V_{SS}	-0.3	IOV_{DD} + 0.3	V
Current into or out of any pin, except power supply pins, OUTP and OUTN.	-20	+20	mA
Current into or out of power supply pins, OUTP and OUTN.	-120	+120	mA

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16.0	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

8.2.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
IOV_{DD} - V_{ss}	3.0	3.3	3.6	V
V_{DD} - V_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
V_{DD}PA - V_{SS}PA	3.0	3.3	3.6	V
Operating Temperature	-40	–	+85	°C
Xtal Frequency	9.6	–	12	MHz
External Clock Frequency (injected into XTALin pin)	9.6	–	24	MHz

8.2.3 Operating Characteristics

Using the recommended components in Figure 2 and for the following conditions unless otherwise specified:

Xtal Freq. = 12.0MHz ±100ppm, $V_{DD}PA = AV_{DD} = IOV_{DD}$ = 3.0V to 3.6V; V_{DD} = 1.7V to 1.9V; T_{AMB} = 25°C; all gain settings are 0dB. Figures apply to CMX7011, unless otherwise stated.
Note: Parametric measurements in this section are subject to further characterisation.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} Total powersaved (ENABXTAL pin connected to VSS)	1	–	50	–	µA
I_{DD} Digital (after Reset, Xtal enabled)	1, 8, 18	–	14.0	–	mA
I_{DD} IODigital (after Reset, Xtal enabled)	1, 9, 18	–	0.5	–	mA
I_{DD} Digital	1, 8, 19	–	17.5	–	mA
Operational Modes					
I_{DD} IODigital	1, 9, 20	–	0.6	–	mA
I_{DD} Analogue PA	1, 9, 20	–	0.7	–	mA
I_{DD} Analogue Vocoder encoding	1, 9, 20	–	6.5	–	mA
I_{DD} Analogue Vocoder decoding	1, 9, 20	–	2.8	–	mA
I_{DD} Digital Vocoder encoding	1, 8	–	33	–	mA
I_{DD} Digital Vocoder decoding	1, 8	–	20.0	–	mA
I_{DD} Analogue	1, 9, 20	–	10	–	mA
Logic Inputs and Outputs					
Input logic '1' level		80%	–	–	IOV_{DD}
Input logic '0' level		–	–	20%	IOV_{DD}
Input leakage current (Vin = 0 to IOV_{DD})	1	–	–	±5.0	µA
Input capacitance		–	3	–	pF
Output logic '1' level (I_{OH} = 2mA)		90%	–	–	IOV_{DD}
Output logic '0' level (I_{OL} = -5mA)		–	–	10%	IOV_{DD}
"Off" state leakage current (IRQN or RDATA)	1	–	–	±5	µA
Analogue Outputs					
Differential output dc offset (OUT P – OUT N)	3	–	–	±40	mV
XTALin					
Input logic '1' level		70%	–	–	IOV_{DD}
Input logic '0' level		–	–	30%	IOV_{DD}
Input current (Vin = 0 to IOV_{DD})		–	–	±40	µA
XTALout					
Output logic '1' level (I_{OH} = 0.5mA)		90%	–	–	IOV_{DD}
Output logic '0' level (I_{OL} = -1.2mA)		–	–	10%	IOV_{DD}

	Notes	Min.	Typ.	Max.	Units
AC Parameters					
XTALin					
'High' pulse width	4	15	–	–	ns
'Low' pulse width	4	15	–	–	ns
Input impedance (at 12.0MHz)					
Powered-up Resistance		–	150	–	kΩ
Capacitance		–	20	–	pF
Powered-down Resistance		–	300	–	kΩ
Capacitance		–	20	–	pF
Xtal start up time (from powersave)		–	20	–	ms
BIAS					
Start up time (from powersave)		–	100	–	ms
CODEC					
Input Impedance (INPUT P or INPUT N)		–	10	–	kΩ
Input Voltage Range (INPUT P or INPUT N)	10, 17	–	–	20 to 80	%AV_{DD}
Differential Input Voltage (pk to pk)	11, 12, 17	–	–	100	%AV_{DD}
Output Load Impedance (OUT P or OUT N)	6	32	–	–	Ω
Output Voltage Range (OUT P or OUT N)	3, 13, 17	–	–	10 to 90	% V_{DD}PA
Differential Output Voltage (pk to pk)	3, 11, 17	–	–	160	% V_{DD}PA
Differential Output Power	3	–	120	–	mW
Input Gain Setting Accuracy		–	±0.5	–	dB
Output Gain Setting Accuracy		–	±0.5	–	dB
ADC SINAD	5, 14	–	86	–	dB
DAC SINAD	7, 15	–	80	–	dB
Vocoder Performance					
Sample Rate		–	8	–	ks/s
Data Rate		–	2400	–	bps
Lower Frequency Limit (internally bandlimited)		60	–	–	Hz
Upper Frequency Limit (internally bandlimited)		–	–	3900	Hz
Encoder Algorithmic Delay	16	–	–	20	ms
Decoder Algorithmic Delay	16	–	–	12	ms

		Notes	Min.	Typ.	Max.	Units
C-BUS Timings		2				
t_{CSE}	CSN-Enable to Clock-High time		100	–	–	ns
t_{CSH}	Last Clock-High to CSN-High time		100	–	–	ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0	–	–	ns
t_{HIZ}	CSN-High to Reply Output 3-state time		–	–	1.0	µs
t_{CSOFF}	CSN-High time between transactions		1.0	–	–	µs
t_{NXT}	Inter-Byte time		200	–	–	ns
t_{CK}	Clock-Cycle time		200	–	–	ns
t_{CH}	Serial Clock-High time		100	–	–	ns
t_{CL}	Serial Clock-Low time		100	–	–	ns
t_{CDS}	Command Data Set-Up time		75	–	–	ns
t_{CDH}	Command Data Hold time		25	–	–	ns
t_{RDS}	Reply Data Set-Up time		50	–	–	ns
t_{RDH}	Reply Data Hold time		0	–	–	ns

Notes:
1. T_{AMB} = 25°C, not including any current drawn from the device pins by external circuitry.
2. Maximum 30pF load on each C-BUS or CODEC (SSP) interface line.
3. Measured whilst driving a 32Ω resistive load between OUT P and OUT N pins.
4. Timing for an external input to the XTALin pin.
5. Differential measurement, 10Hz to 4kHz bandwidth.
6. Care should be taken to avoid shorting the OUTP and OUTN pins together, or to V_{DD} or V_{SS}.
7. Differential measurement, 300Hz to 4kHz bandwidth, no load.
8. 1.8V nominal supply.
9. 3.3V nominal supply.
10. This is the maximum signal range on each pin of the differential input. The common mode voltage can be any voltage within this range but, for optimum dynamic range, it should be set to about AV_{DD} /2. If the inputs are ac coupled, on-chip resistors will set the dc bias of each input to this voltage automatically.
11. This is the maximum differential peak to peak signal amplitude, which corresponds to a signal on each input of (AV_{DD} /2 ± 25% AV_{DD}). Exceeding this can result in increased distortion products.
12. Because the amplitude of speech fluctuates, it is important to set the average speech level such that the level of distortion that results from the occasional overdriving of the inputs is at an acceptable level.
13. This is the maximum voltage on each pin of the differential output, such that the device does not start to introduce significant harmonic distortion.
14. The internal ADC is a sigma-delta type which samples at 2.4MHz. It is important that there is no significant energy close to this frequency or at any of its harmonics, thus avoiding the need for an external low-pass anti-alias filter.
15. The internal DAC is a sigma-delta type which samples at 2.4MHz. It will output energy at this frequency and its harmonics. Should this present a problem, it is suggested that some external filtering be used at the audio outputs.
16. Excludes the 20/40/60/80 ms sample collection period.
17. Internal gain settings are 0dB on input gain for the optimum vocoded level and +6dB on output gain for the optimum vocoded level, subject to further characterisation.
18. ADC or DAC disabled, Vocoder is disabled.
19. ADC or DAC enabled, Vocoder is disabled.
20. ADC or DAC enabled, Vocoder is enabled.

7.1.3 Operating Characteristics (continued)

Timing Diagrams

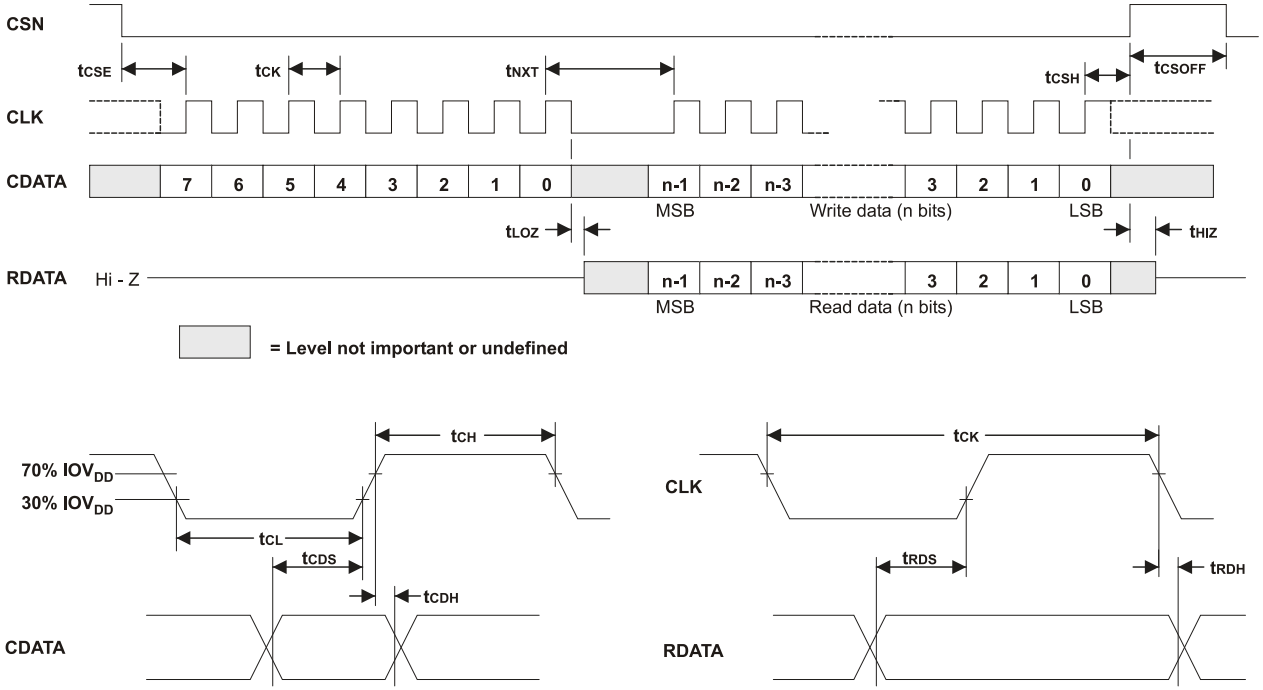


Figure 8 C-BUS Timing

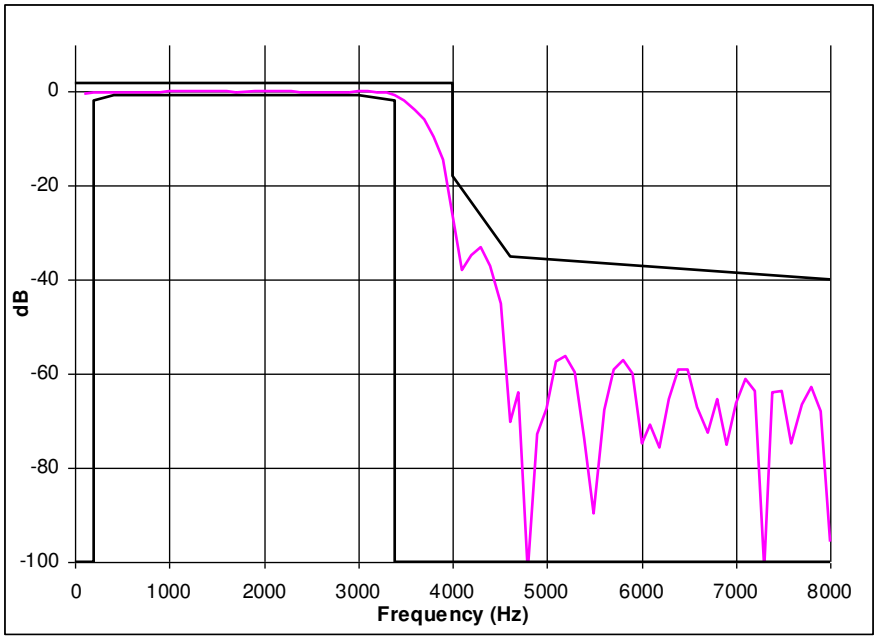
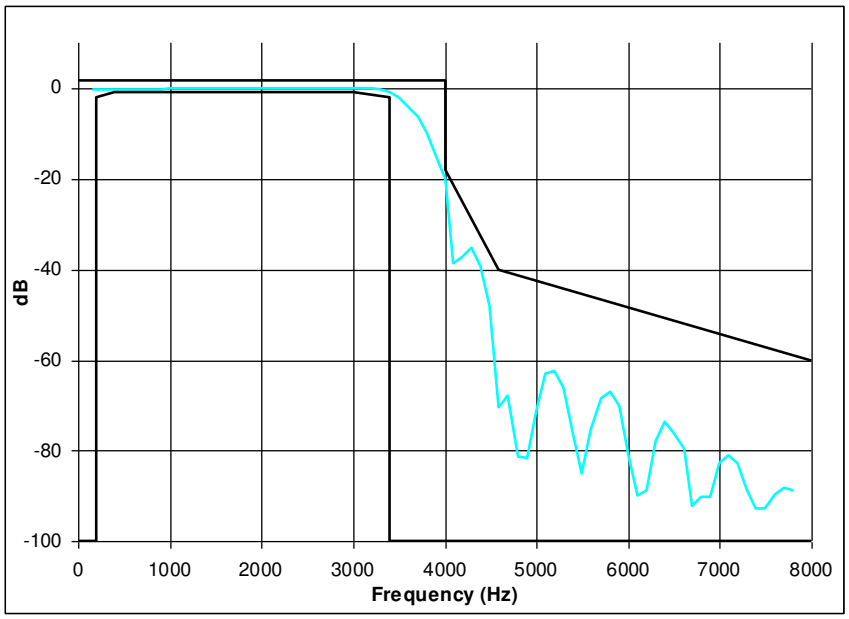


Figure 9 ADC Input Filter - Typical Response

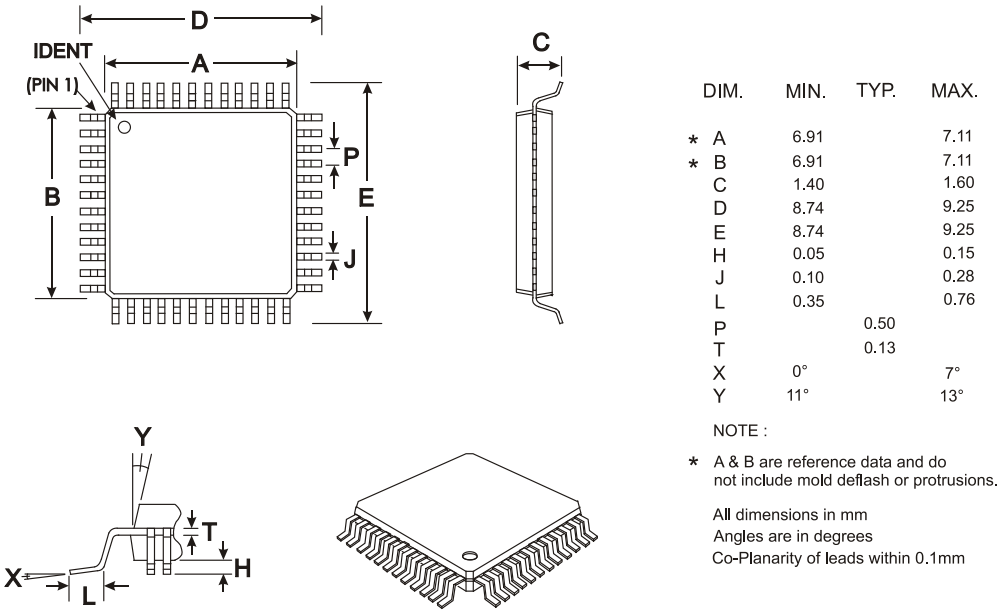


(ADC Input Frequency Vs Fundamental tone power for 750mVrms differential input, normalised to 1kHz)

Figure 10 DAC Output Filter - Typical Response

(DAC Output Frequency Vs Measured tone power for 32000 peak sample level differential output, normalised to 1kHz)

8.3 Packaging



DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

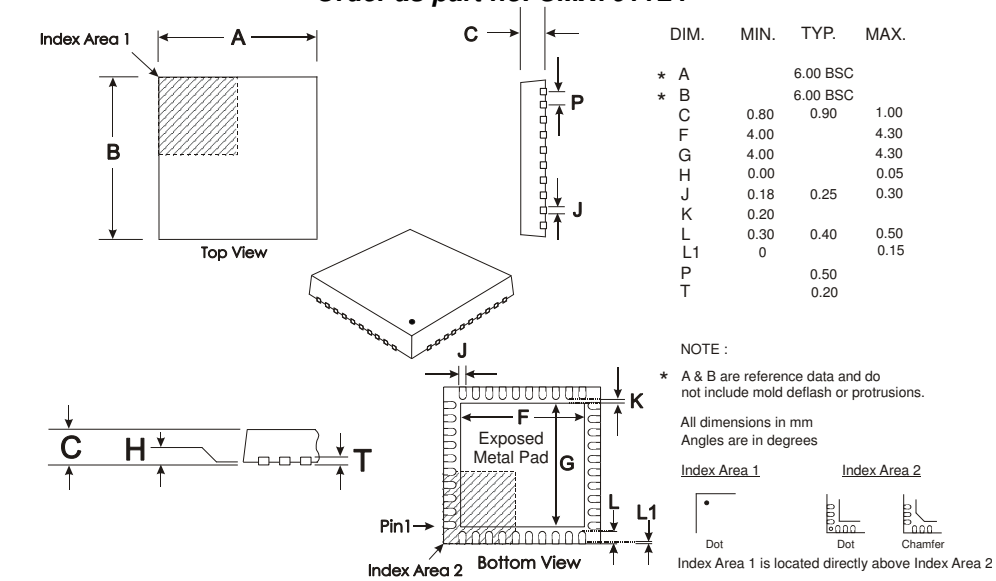
NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 11 48-pin LQFP Mechanical Outline (L4)

Order as part no. CMX7011L4



DIM.	MIN.	TYP.	MAX.
* A		6.00 BSC	
* B		6.00 BSC	
C	0.80	0.90	1.00
F	4.00		4.30
G	4.00		4.30
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Dot Dot Chamfer

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 12 48-pin VQFN Mechanical Outline (Q3)

Order as part no. CMX7011Q3

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [http://www.cmlmicro.com/].

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. . . Maximum Flexibility

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