CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX7045
AIS SART Processor

D/7045FI-1.x/1 October 2011 **DATASHEET** Advance Information

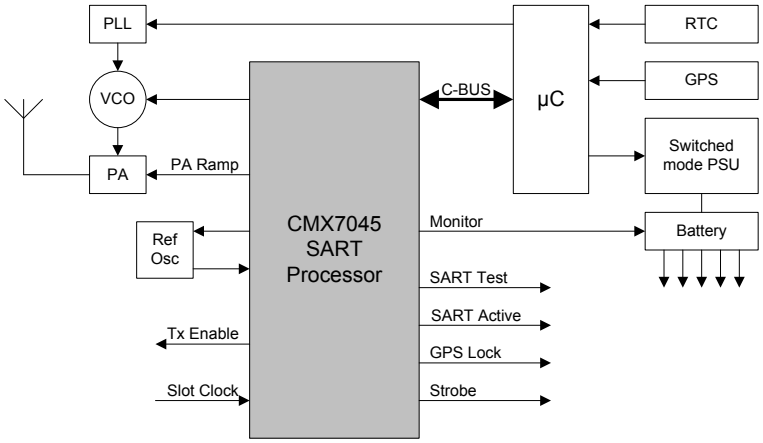
7045FI-1.x Marine AIS SART Processor

Features:

- Tx AIS GMSK Modem
- AIS SART Formatted Data
- Battery Monitor
- Flexible Tx Interface
- Configurable by Function Image™
- Two Auxiliary Clock Generators
- Two-Input Auxiliary (10-bit) ADC
- Four Auxiliary (10-bit) DACs
- Conforms to IEC 61097-14
- Integration Roadmap
- Low-Power (3.0V to 3.6V) Operation
- Low Profile 48-pin LQFP or VQFN

Applications:

- Automatic Identification System (AIS) Search And Rescue (SART) for Marine Safety



This document contains:

1 Brief Description

The CMX7045 is a dedicated processor for marine Automatic Identification System (AIS), Search and Rescue Transmitter (SART) operation, fully meeting the requirements of IEC 61097-14.

This highly integrated and flexible device includes a 9600 baud GMSK modem for transmission of formatted data. Additional auxiliary functions are also provided to further support the system host, these include: a two-input 10-bit ADC, four 10-bit DACs, two system clock outputs and four GPIOs.

The CMX7045 offers low power sleep modes to ensure maximum system battery life and is available in a in a small 48-pin LQFP or VQFN package.

This Datasheet is the first part of a two-part document comprising Datasheet and User Manual: the User Manual can be obtained by registering your interest in this product with your local CML representative.

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TABLES

FIGURES

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

1.1 History

Version	Changes	Date
1	Initial release	Oct 2011

2 Block Diagram

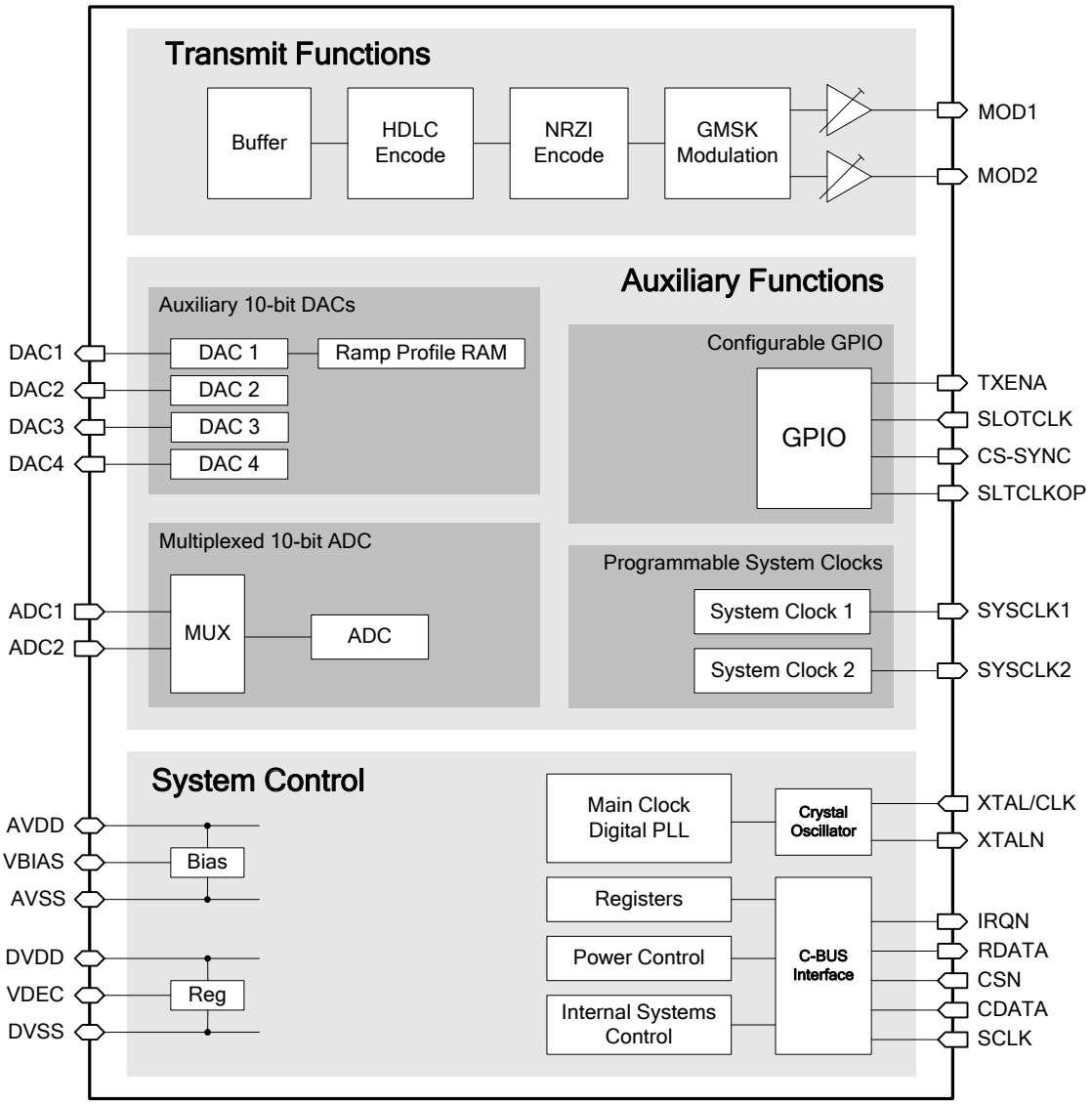


Figure 1 Block Diagram

3 Signal/Pin List

CMX7045 Q3 or L4	Pin Name	Type	Description
1	-	NC	*reserved* – do not connect.
2	-	NC	*reserved* – do not connect.
3	-	NC	*reserved* – do not connect.
4	-	NC	*reserved* – do not connect.
5	-	IP	Connect to $DV_{DD.}$
6	-	IP	Connect to $DV_{DD.}$
7	DVSS	PWR	Digital Ground.
8	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
9	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed.
10	SLOTCLK	IP	Slot clock from host (37.5Hz).
11	CS-SYNC	OP	Slot Sync.
12	SLTCLKOP	OP	Slot clock output.
13	SYSCLK1	OP	Synthesised Digital System Clock Output 1.
14	DVSS	PWR	Digital Ground.
15	TXENA	OP	Enable for external Tx hardware.
16	-	NC	*reserved* – do not connect.
17	-	NC	*reserved* – do not connect.
18	-	NC	*reserved* – do not connect.
19	-	NC	*reserved* – do not connect.
20	-	NC	*reserved* – do not connect.
21	-	NC	*reserved* – do not connect.
22	AVSS	PWR	Analogue Ground.
23	MOD1	OP	Modulator 1 output.
24	MOD2	OP	Modulator 2 output.
25	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.
26	-	NC	*reserved*– do not connect this pin.

CMX7045 Q3 or L4	Pin Name	Type	Description
27	-	NC	*reserved*– do not connect.
28	-	NC	*reserved* – do not connect.
29	ADC1	IP	ADC input 1.
30	ADC2	IP	ADC input 2.
31	AVDD	PWR	Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.
32	DAC1	OP	Aux DAC output 1/RAMDAC.
33	DAC2	OP	Aux DAC output 2.
34	AVSS	PWR	Analogue Ground.
35	DAC3	OP	Aux DAC output 3.
36	DAC4	OP	Aux DAC output 4.
37	DVSS	PWR	Digital Ground.
38	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins.
39	XTAL/CLK	IP	19.2MHz input from the external clock source or 9.6MHz Xtal.
40	XTALN	OP	The output of the on-chip 9.6MHz Xtal oscillator inverter. NC if 19.2MHz clock is used.
41	DVDD	PWR	Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.
42	CDATA	IP	C-BUS: Command Data. Serial data input from the µC.
43	RDATA	TS OP	C-BUS: Reply Data. A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
44	-	NC	*reserved* – do not connect this pin.
45	DVSS	PWR	Digital Ground.
46	SCLK	IP	C-BUS: The C-BUS serial clock input from the µC.
47	SYSCLK2	OP	Synthesised Digital System Clock Output 2.
48	CSN	IP	C-BUS: The C-BUS chip select input from the µC.
EXPOSED METAL PAD	SUB	~	The central metal pad may be connected to Analogue Ground (AV_{SS}) or left unconnected. **No other electrical connection is permitted.**

Notes:

IP	=	Input (+PU/PD = internal pullup/pulldown resistor)
OP	=	Output
TS OP	=	3-state Output
PWR	=	Power Supply Connection
NC	=	No Connection

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits.
DV_{DD}	DVDD	Power supply for digital circuits.
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator.
V_{BIAS}	VBIAS	Internal analogue reference level, derived from $AV_{DD.}$
AV_{SS}	AVSS	Ground for all analogue circuits.
DV_{SS}	DVSS	Ground for all digital circuits.

4 Recommended External Components

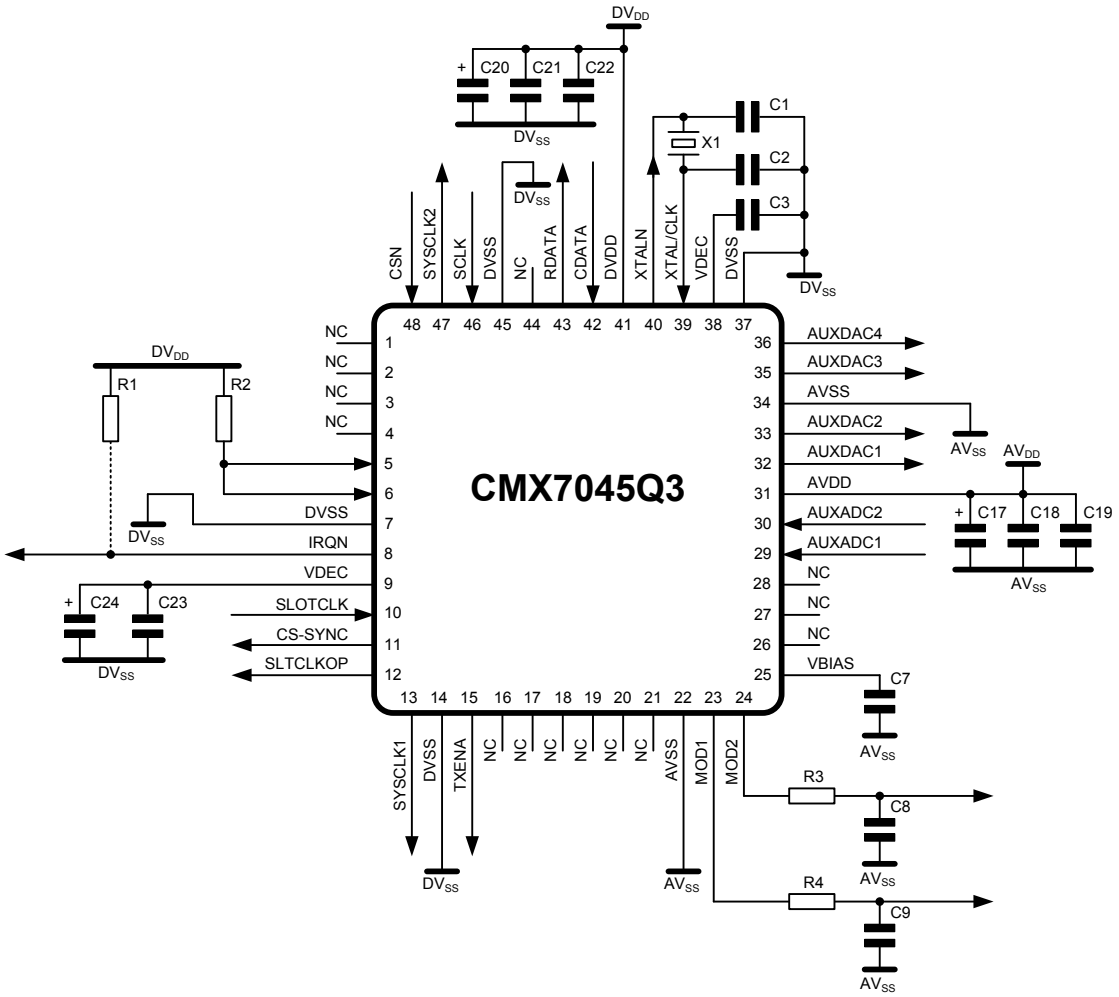


Figure 2 Recommended External Components

Table 2 Component Values

R1	100kΩ	C2	18pF	C17	10µF	C22	10nF
R2	220kΩ	C3	10nF	C18	10nF	C23	10nF
R3	100kΩ	C7	100nF	C19	10nF	C24	10µF
R4	100kΩ	C8	100pF	C20	10µF	X1	9.6MHz
C1	18pF	C9	100pF	C21	10nF		See note 1

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a 9.6MHz crystal or a 19.2MHz external clock generator. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance.

2. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

5 PCB Layout Guidelines and Power Supply Decoupling

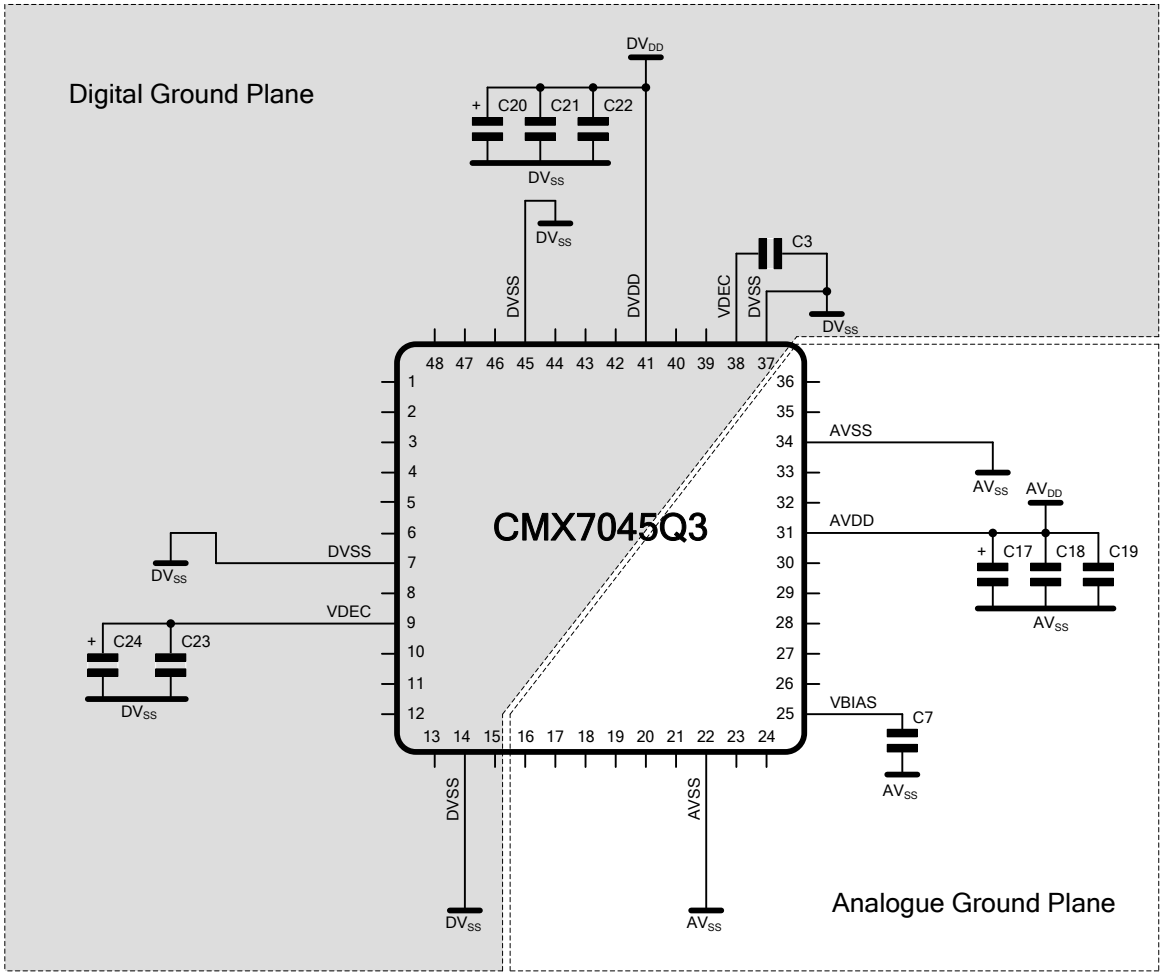


Figure 3 Power Supply Connections and De-coupling

Component values as per Table 2.

Notes:

1. The supply decoupling capacitors should be as close as possible to the CMX7045. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX7045, with provision to make links between them, close to the CMX7045. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.
2. The central metal pad on the 'Q3' package may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AV_{SS}). **No other electrical connection is permitted.**
3. V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled to ensure its integrity so, apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with an external high input impedance buffer.

6 General Description

6.1 Overview

Tx Modem Functions

- AIS 25kHz channel (GMSK, 9600bps, 2.4kHz deviation, BT = 0.4)
- AIS Burst mode with full AIS frame formatting (HDLC-type)
  - Bit stuffing
  - NRZI coding
  - Training sequence and start/stop flag insertion
  - CRC generation
- AIS Raw mode (for greater flexibility)
  - Supports arbitrary data streams for user-defined protocols
- 160-byte (equivalent to 5 AIS slots) Tx data buffer
- Flexible Tx Interface
  - Two-point modulation outputs, with independent gain and polarity controls

Analogue I/O Functions

- Auxiliary ADC system
  - A two-input 10-bit successive approximation ADC with integrated sample and hold
- Auxiliary DAC system
  - Four general purpose auxiliary 10-bit DACs
- Ramping auxiliary DAC (using DAC 1)
  - DAC steps through a user-configured sequence of DAC output values to develop a specific rising/falling DAC output signal. This is useful for ramping an RF PA, and can be configured to operate automatically at the start and end of a burst.

System Functions

- All internal subsystems are controlled via a single serial host interface to reduce host µC pin count and simplify external host driver complexity.
- Transaction oriented command/response logical host interface executes tasks supporting normal operation, device configuration, and functions to assist manufacturing calibration trimming of external circuits.
- Internal system clock derived from reference oscillator and eliminates the need for additional XTAL or baseband clock oscillator.
- Auxiliary clock synthesisers generate two clocks for external use to support peripheral devices.
- Function Image™ is loaded directly from the host µC via C-BUS.
- Integrated 2.5V regulator can develop 2.5V from required 3.3V supply.
- Powersave facilities minimise total system power.

6.2 AIS System Formats

The AIS system uses two basic channel access mechanisms: Self Organising Time Division Multiple Access (SOTDMA) and Carrier-Sensing Time Division Multiple Access (CSTDMA). The CMX7045 is compatible with both systems and offers additional features which simplify the implementation of an AIS SART device conforming to IEC 61097-14.

The relevant International standards are:

[0]	ITU-R M.1371-4
[1]	IEC 61993-2 Class A
[2]	IEC 62287-1 Class B CSTDMA
[3]	IEC 62287-2 Class B SOTDMA
[4]	IEC 62320-1 Base Station
[5]	IEC 62320-2 Aids to Navigation
[6]	IEC 61097-14 AIS-SART

7 Detailed Description

7.1 Clock Source

The CMX7045 can be used with either a 9.6MHz xtal or a 19.2MHz oscillator.

7.2 Host Interface

This section provides a general description of the C-BUS serial interface protocol used to transfer data, control and status information between the CMX7045 and its host.

C-BUS is a serial interface, similar to SPI, that uses a simple transaction-oriented command/response protocol with addressing to access specific registers within the CMX7045. Each C-BUS transaction consists of a single Register Address/Command byte (A/C byte) sent from the µC which may be followed by one or more data byte(s) sent from the µC to be written into one of the CMX7045's Write Only registers, or one or more data byte(s) read out from one of the CMX7045's Read Only registers, as illustrated in Figure 4.

Data sent from the µC on the CDATA line is clocked into the CMX7045 on the rising edge of the SCLK input. RDATA sent from the CMX7045 to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an A/C byte is dependent on the value of the A/C byte. The most significant bit of the address or data is sent first. For detailed timings see section 8.2.

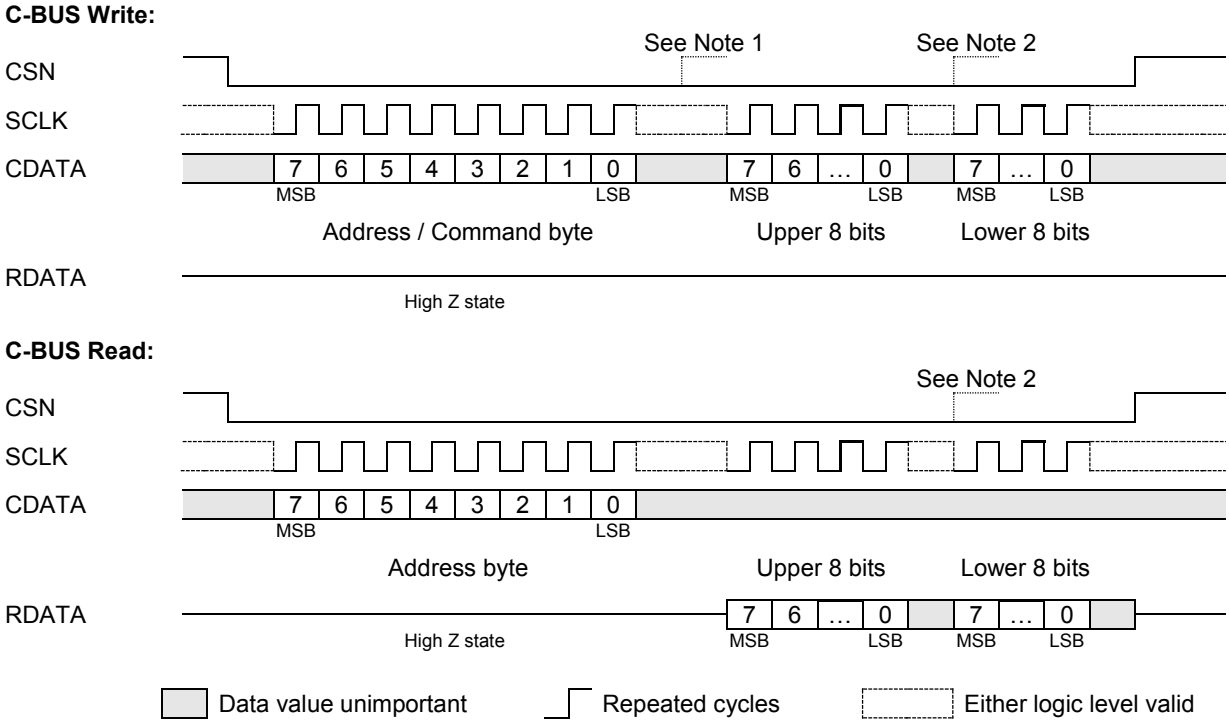


Figure 4 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred.
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.3 Function Image™ Load and Activation

The Function Image™ (FI) file, which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software. The Function Image™ data file is no more than 24kbytes.

Once the FI has been loaded, the CMX7045 performs these actions:

(1) the product identification code ($7045) is reported in C-BUS register $C5
(2) the FI version code is reported in C-BUS register $C9
(3) the two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
(4) the device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8
(5) once activated, the device initialises fully, enters Deep Sleep mode mode and becomes ready for use, and the Activation Register Ready (ACT) flag (bit 0 of the Status register) will be set
(6) Once the Deep Sleep bit (Status2 b:13) has been set, the host may then power down the Analogue sections of the device to minimise power consumption (typically while the host is waiting for the external GPS to output a valid position fix)
(7) When the host decides that the device should be returned to active mode in order to configure the device or transmit an AIS burst, it should first power-up the Analogue sections and then send the “exit Deep Sleep” command.

The checksums should be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and become unresponsive to all further host commands (including General Reset). A power-on reset is required to recover from this state.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Following a General Reset, reloading of the FI is required.

7.3.1 FI Loading from Host Controller

The FI needs to be included into the host controller software build and downloaded into the CMX7045 at power-up over the C-BUS interface. Wait for the ACT flag to be set (Status register $C6 bit 0), then the data can then be sent directly over the C-BUS to the CMX7045.

Each time the device is powered up or reset, its FI must first be loaded and then activated. These two steps assign internal device resources and determine all device features. The device does not operate until the FI is loaded and activated.

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

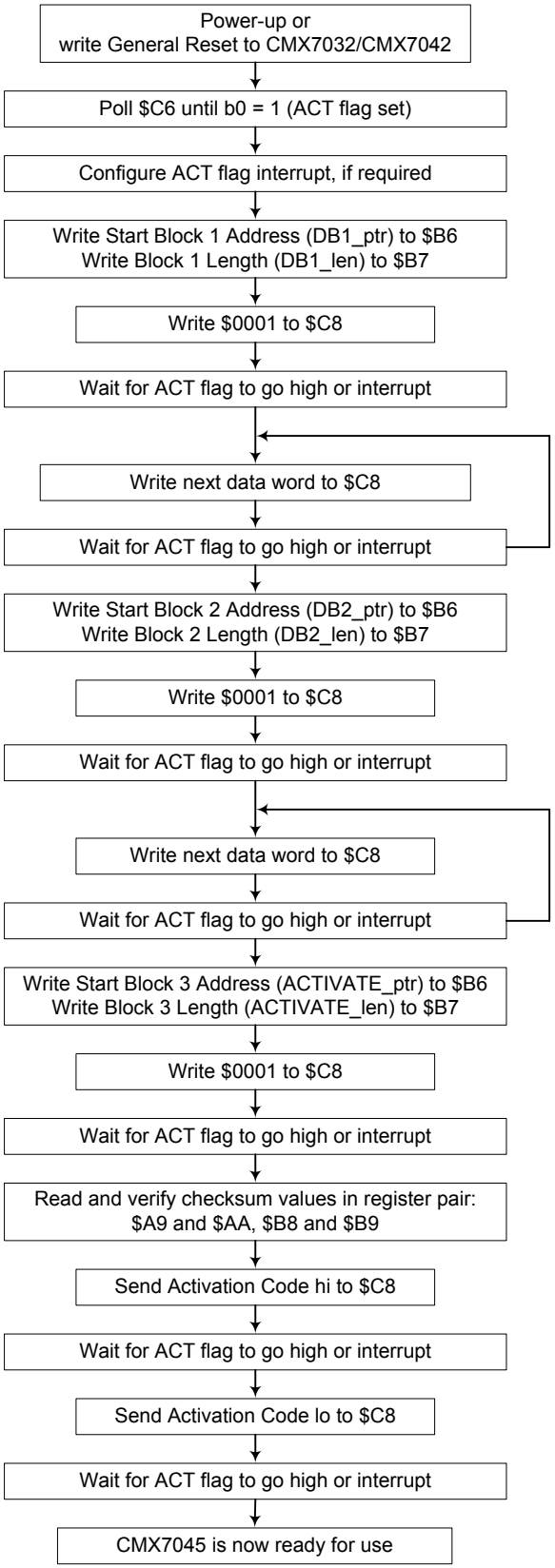


Figure 5 FI Loading from Host

7.4 System Description and Tasks

This section describes the operation of main sections of the CMX7045 and the task-oriented logical interface provided to the external host device.

7.4.1 Signal Routing

The Tx Modulation output signals may be configured to be suitable for two-point modulation circuits. Signal levels on both output pins, MOD1 and MOD2, can be set to within 0.2dB using a Configuration Mode task.

7.4.2 Operating Modes

The CMX7045 operates in either:

- Deep Sleep Mode
- Configuration mode
- Normal mode

Deep Sleep mode puts the device into a low-power standby mode to minimize power consumption. Whilst in this mode the host can switch off un-needed analogue functionality. Once the device has been activated, it will enter deep sleep mode automatically.

Configuration mode is used to set up various operating parameters of the CMX7045 subsystems, e.g. Transmit format, timing parameters etc. following a power-up or reset. The modem section is disabled when the device is in Configuration mode. Configuration mode uses dedicated tasks that are not valid whilst in Normal mode.

Normal mode is used when actively running the CMX7045 modem and other subsystems. Normal mode uses dedicated tasks that are not valid whilst in Configuration mode.

“Enter Config Mode” (ECM) is a Normal mode task that switches the device from Normal to Configuration mode. “Exit Config Mode” (EXIT_CONFIG) is a Configuration mode task that switches the device from Configuration to Normal mode.

7.4.3 Modem and Data Units

The CMX7045 is logically divided into two main units which can accept and perform tasks separately:

- Modem Unit
- Data Unit

The Modem Unit is primarily responsible for processing Tx data from the internal Tx data buffer, presenting it on the MOD1 and MOD2 pins.

The Data Unit is primarily responsible for transferring data between the internal data buffers or subsystems and the C-BUS registers, from where they can be accessed by the host µC.

When the device is in Normal mode, the Command register, $C8, is a 16 bit C-BUS write register that contains task fields for both Data and Modem units. A task is invoked by writing its code into the Data Task or Modem Task fields. A single C-BUS write transaction will change all Command register fields. Often, the host will only want to issue either a Data or Modem task, in which case it should ensure that the other task field is set to all zeroes, corresponding to a null/idle task. Sometimes it is useful to issue Data and Modem tasks simultaneously, in which case, the Data task will always be completed before the Modem task is started.

Certain internal subsystems can be directly accessed and controlled via C-BUS transactions, without issuing a specific task/command.

7.4.4 Timing and Synchronisation

The CMX7045 requires a Slot Clock (SLOTCLK) input from the host µC. This should be a pulse at least 50µs long, whose rising edge is aligned to the AIS Slot boundary. An edge is required at the start of every AIS slot or frame, hence the frequency of this signal is 37.5Hz or 0.5Hz[1].

The CMX7045 has several features to assist the host µC with timing, which are detailed below. All of these features are based on the SLOTCLK signal, provided by the host to the CMX7045's SLOTCLK pin. All timings are defined as a number of 24kHz "ticks" referenced to the rising edge of the SLOTCLK signal.

7.4.5 Tx Timing

The CMX7045 can be configured to perform a sequence of events when a TXB or TDBS task (transmit burst) is issued. The events are: start and end of modulation, ramping the RAMDAC up and down, asserting and releasing a digital output pin (intended as a Tx Enable) and CSTDMA sensing. Each of these can be configured to happen with specified delays from the rising edge of the SLOTCLK. The timings are set up with the Config Mode task Tx_Sequence. See User Manual section 9.12.3 for details.

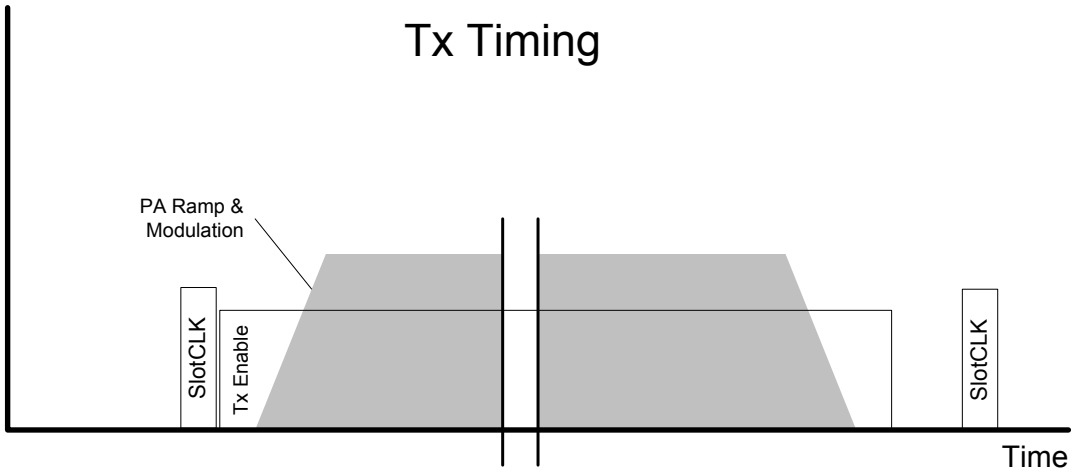


Figure 6 Tx Burst Timing

7.4.6 ADC

The ADC is available for user defined functions. The ADC runs continuously, the input is selected by the ADC Input Select bits in the C-BUS Mode register, $C1 and the results of the conversion are presented in ADC Data C-BUS register $C9. This register also includes a bit field to indicate which input was selected when this conversion was executed.

7.4.7 DACs

The four DACs can be updated in any combination using the DAC_Write data task. See User Manual 9.12. In addition, DAC1 can be configured as a RAMDAC to output a series of values as part of the transmit timing sequence. The values and the rate at which they change are set-up using a Config mode task.

7.4.8 Interrupt Operation

The CMX7045 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) are both set to 1. User Manual section 9.14 describes the situations which cause the IRQ bit to change from a 0 to a 1. The IRQN pin is an open collector output that requires an external pull-up resistor.

[1] If the host supplies a 0.5Hz signal, this should be aligned to the even UTC second and the selection of X1 should be chosen to maintain correct timing between SLOTCLK pulses.

7.4.9 Deep Sleep Mode

Deep Sleep mode (entered through Configuration mode or after the activation codes have been successfully loaded) puts the device into static state where all signal processing and clocks are stopped and only the C-BUS remains active. In this mode, the I_{DD} drops to the lowest level, as specified in section 8.1.3, and is thus suitable for use in AIS SART, where it is feasible for the host µC to switch off the CMX7045 at known times. See User Manual section 9.12.6.

7.5 Operation of Tasks

This section describes modem and data tasks. Understanding their operation requires knowledge of the internal buffering of the CMX7045.

Tx data is double buffered. Each Tx channel has a Data Buffer. The host µC accesses the C-BUS registers and the modulator/demodulator directly accesses the Data Buffers. Tasks transfer data between the buffers and the C-BUS registers.

7.5.1 Tx Task Operation

Typical stages of Tx task operation are depicted in Figure 7 and occur as follows:

1. The host writes up to 4 words of data for transmission into the Write Data C-BUS registers.
2. The host writes the Command register, specifying a data task. This results in transfer of the data from the Write Data registers into the Tx Data Buffer.
3. Steps 1 and 2 can be repeated to load the Tx Data Buffer with a large block of data.
4. A Modem task can then be used to instruct the Tx Modulator to transmit the data in the Data Buffer. This causes the content of the Tx Data Buffer to be coded and CRC'd (if in burst mode) and transmitted to the MOD1 and MOD2 output pins.
5. Once the system is up and running any modem task may potentially take some time to execute as it may have to wait for the previous task to complete.

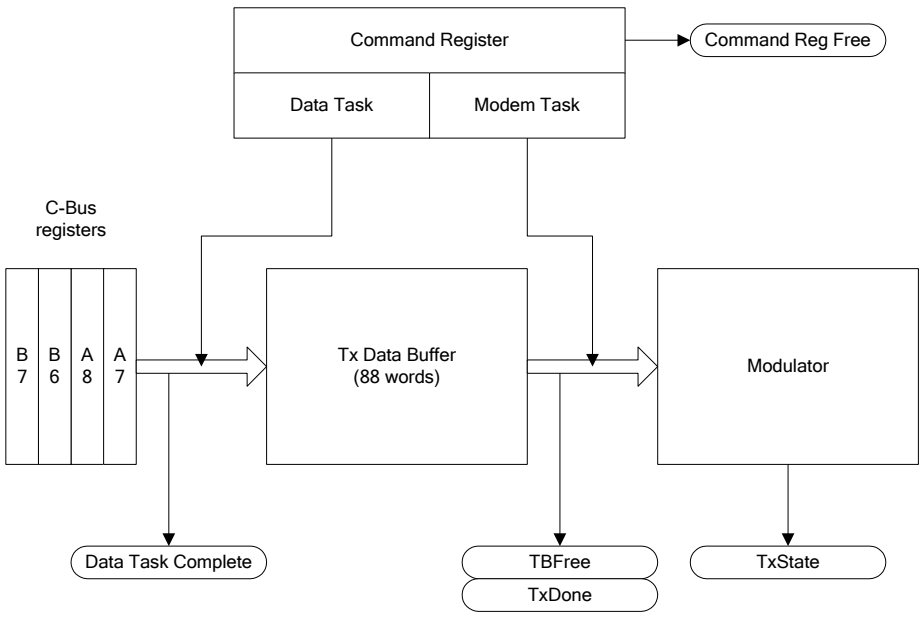


Figure 7 Tx Task Operation

7.5.2 Registers and Buffers for Tx Tasks

- **Command register**: contains Data and Modem task fields as described above.
- **Status register**: contains bits that indicate when tasks are complete, which can interrupt the host:
  - Command Reg Free
  - TBFREE
  - TxDONE
  - Config Task Complete
  - Data Task Complete.
- **Interrupt Mask**: Host write register to specify which status bit can cause an interrupt.
- **Write Data registers** 0-3: Contain data written from host µC to transmit via the Tx Modulator.
- **Tx Data Buffer**: The Tx Data is double buffered, which allows the host µC to write to the Tx Data Buffer while the modulator is simultaneously transmitting data it reads from the Tx Modem Buffer. Each buffer is capable of holding one full (5-slot) AIS message.

7.5.3 Write Data Registers

An array of four, 16 bit, C-BUS write registers form the Write Data C-BUS registers.

The device reads and acts upon the content of these data write registers as instructed by the Data Task bits of the Command register while in transmit mode. Generally, they may be written at any time by the host µC with no effect on internal device operation. When a "Data task" is issued the Data registers will be read by the device and so should not be modified by the host µC until the Data Task complete bit is set in the Status register.

Data tasks access the registers as a number of words (1 to 4) or as a number of bits (1 to 16 in $A7), however if a bit-format Data Task is used it must be the final data task issued in a multi-data transfer from the host. The next data task issued should be a DataWordResetN_Tx or DataBitResetN_Tx to re-initialise the internal data buffer pointers (a bit-format task is usually used as the last transfer of a data block that is not a complete number of words in length).

Word-format:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register $A7	Data write from host µC to device word 1(MSB sent first)															
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register $A8	Data write from host µC to device word 2(MSB sent first)															
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register $B6	Data write from host µC to device word 3(MSB sent first)															
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register $B7	Data write from host µC to device word 4(MSB sent first)															

Bit-format:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register $A7	Data write from host µC to device bits 0-15, (bit 15 transmitted first)															

7.5.4 Data Tasks

Data tasks are used to:

- Load data from the Write Data registers into Data Buffers while in normal or configuration modes
- Load data from the Data Buffers to the DACs
- Write or operate subsystems by passing data using the Write Data registers.

Table 3 Data Tasks

Name	Description
NULL	Null system task – takes no action.
DataWordResetN_Tx	• Reset Tx data buffer pointer. • Copy N words (1 to 4) from Write Data registers to Tx data buffer. • Increment the data buffer pointer.
DataBitReadN_Rx1	• Copy N bits (1 to 15) from Rx1 data buffer to Read Data register 0. • Increment the data buffer pointer.
DataBitReadN_Rx2	• Copy N bits (1 to 15) from Rx2 data buffer to Read Data register 0. • Increment data buffer pointer.
DataBitWriteN_Tx	• Copy N bits (1 to 15) from Write Data register 0 to Tx data buffer. • Increment data buffer pointer.
DataBitResetN_Tx	• Reset Tx data buffer pointer. • Copy N bits (1 to 15) from Write Data register 0 to Txdata buffer • Increment data buffer pointer.
DAC_Write	Interprets each of the first 1 to 4 words in the Write Data registers as a write command for the Auxiliary DACs.

7.5.5 Modem Tasks and Codes

Modem tasks transmit data on the MOD1 and MOD2 output pins. Modem tasks also coordinate data transfer between the Data Buffer and the modem.

Note that for receive tasks a 1 or 2 at the end of the task name refers to the Rx channel which is being addressed.

Table 4 Modem Tasks

Name	Description		
NULL	No command – takes no action		
AbortTx			
ECM	Enter Configuration mode		
Tx Tasks			
Tx Raw bit = 0		Tx Raw bit = 1	
TXB	Code and transmit AIS message using contents of data buffer. Start on next SLOTCLK	TDBS	Transmit contents of data buffer. Start on next SLOTCLK
		TDB	Transmit N data bits from the Tx mod buffer. Start as soon as modulator is free
		PRBS	Transmit pseudorandom bit sequence
		TRW	Repeatedly transmit one word
		HCT	Hardware Control

7.6 Transmission Format

The CMX7045 is capable of transmitting AIS data in either raw mode or burst mode.

In AIS raw mode, data is passed directly from the Tx Data Buffer to the GMSK modulator, so the µC will be responsible for sending any necessary training sequences and performing HDLC processing and NRZI coding.

In AIS burst mode, the CMX7045 uses an internal message buffer to assemble an entire message (up to 5 slots) to which it automatically adds the training sequence, start/stop flags, CRC, bit stuffing and NRZI coding prior to transmission.

After setting up the appropriate registers, transmission is initiated by issuing a Tx Burst or Tx Raw task.

7.6.1 Transmit Tasks

- **AbortTx:**
  This causes the current task on the Tx channel to abort. It also clears the Tx modem buffer.
- **TXB: Transmit AIS Burst**
  This task can only be executed if the Tx Raw bit (bit 5 in the command register) is cleared to 0. This causes the CMX7045 to take the contents of the Tx Data buffer, apply AIS data coding and transmit the resulting AIS message. The transmit sequence will start on the next SLOTCLK edge.

The following five transmit tasks can only be executed if the Tx Raw bit is set to 1:

- **TDBS: Transmit Data Buffer on SLOTCLK**
  This causes the CMX7045 to transmit the data buffer contents using AIS modulation. No data coding is applied, the Transmit Sequence will start on the next SLOTCLK edge, at which point the CS-SYNC output will become active.
- **TDB: Transmit Data Buffer**
  This causes the CMX7045 to transmit the data buffer contents using AIS modulation. No data coding is applied. The data will be transmitted as the modulator is available (Transmit Sequence is ignored).
- **PRBS: Transmit Pseudorandom Bit Sequence**
  This task causes the CMX7045 to transmit an internally generated pseudorandom bit sequence. The sequence is 511 bits in length, but will repeat indefinitely until aborted using the AbortTx task, (Transmit Sequence is ignored).
- **TRW: Transmit Repeated Word**
  This task causes the CMX7045 to repeatedly transmit the first word currently in the data buffer. Transmission will start immediately and will continue until an Abort Tx task is issued, (Transmit Sequence is ignored).
- **HCT: Hardware Control Task**
  Allows manual control of ancillary hardware functions.

7.6.2 AIS Burst Mode Transmit

In AIS burst mode, the CMX7045 responds to a TXB task by performing bit stuffing, NRZI encoding and the addition of training sequence, start/stop flags and CRC checksum as required by AIS. Note: in AIS burst mode, the data words are automatically transmitted *least significant bit first* as required by the AIS specification.

A number of error conditions are checked for during AIS burst mode transmit, each of which causes transmission to be aborted and a Tx Done interrupt to be generated. The associated Tx states are:

- **Tx Aborted, message too long:**
  This occurs if the internal message buffer is not big enough for the HDLC coded data (should not happen in normal operation, as the message buffer is big enough for a 5-slot message). This condition requires the µC to issue a AbortTx task.
- **Tx Aborted, buffer not ready:**
  This occurs in burst mode if the internal data coding has not completed before the timing_start value expires.

7.6.3 Transmit Example

The following detailed example describes the process of loading and transmitting an AIS message in Burst mode.

Table 5 AIS Burst Transmit Example

	Description	Cmd Reg Free	Data Task	TBFREE	TxDONE
1.	The host should ensure that the TBFREE, Data Task and CmdReg Free bits are set.	1	1	1	1
2.	The host loads the first N(typically 4) data words into the write data registers.	1	1	1	1
3.	The host issues a DataWordResetN_Tx Data Task.	0	1	1	1
4.	Device reads the Command register & notes task types.	1	0	1	1
5.	Device carries out the data task by copying the N data words as the first N data words of the data buffer.	1	1	1	1
6.	The steps above may be repeated (Using DataWordWriteN_Tx tasks) to load many words until the data buffer contains enough data to carry out the desired modem task.				
7.	The host writes a TXB task to the Command register to start the Tx process.	0	1	1	1
8.	Device reads the Command register.	1	1	0	1
9.	Device codes the data. Tx state changes from Idle to Tx Pending	1	1	1	0
10.	When the transmit point arrives (SLOTCLK), the Tx State changes to *Tx in progress* and the TxSequence is activated.				
11.	The Tx Modem Buffer will gradually empty as the Tx Modulator continues transmitting.	1	1	1	1
12.	When the transmission ends the TxDone bit in the Status register will be set, generating an interrupt if enabled. The host should then check the Tx state bits in the Status2 register to see if transmission was successful.	1	1	1	1

7.6.4 AIS Raw Mode Transmit

In AIS raw mode, transmit data is passed directly from the Tx Data Buffer to the GMSK modulator. The µC must calculate the entire transmitted message including the training sequence, HDLC processing (start/stop flags, bit stuffing, and CRC insertion) and NRZI coding. Note: In AIS raw mode, data words written to the CMX7045 are transmitted *most significant bit first*. The AIS message structure, however, requires each message byte to be output *least significant bit first*. The µC must therefore ensure that during the process of HDLC processing and NRZI coding that the resulting data bytes are correctly reversed.

7.6.5 Transmitter Timing Control

The CMX7045 can be configured to control the timing of transmission events whenever a Tx Burst Modem task is executed. This includes the enabling of external RF circuits (e.g. synthesisers and power amplifier), as well as the time at which internal data modulation begins. The flexibility of this timing control allows the CMX7045 to be simply adapted to the characteristics of the RF transmit circuits. The control of the external RF transmit circuits is performed using the TXENA pin and the DAC1 ramping function.

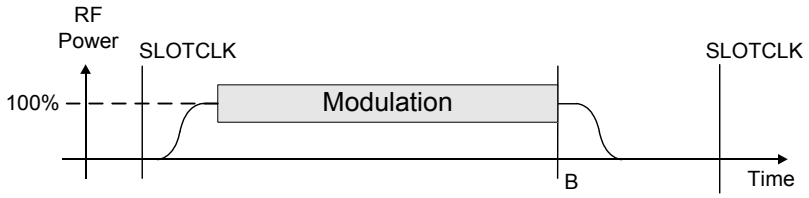


Figure 8 Typical AIS Transmission

A typical AIS transmission is shown in Figure 8. The CMX7045 starts timing relative to the rising edge of SLOTCLK. At the end of a transmission, a sequence of "power-down" actions is performed which are timed relative to the last message bit having been modulated, shown as point B in Figure 8. In this way differences in message length due to bit stuffing are automatically accommodated.

The relative timings of the transmit sequence events are configured as a table of values that are loaded into the CMX7045 using a Config Task operation (User Manual section 9.12.3) – this operation **must** be performed before any transmissions are attempted. Typically, this will only need to be done once as part of an initialization routine. All timings are measured in units of "ticks", each of which lasts for 1/24000Hz (≅ 41.666µs).

The transmit sequence consists of two initial setting values followed by a number of different event types. These are:

- Initial delay from the SLOTCLK edge
- Initial state of the TXENA pin
- Changes to the external hardware, via the TXENA pin (typically used to turn the Tx on/off) and the DAC1 ramp up/down
- Timing triggers for the start and end of the data modulation
- A dummy event in case any of the above are not required in the application.

The transmit event sequence is programmed using a Config task, see User Manual section 9.12.3.

Table 6 Tx Sequence events

b3	b2	b1	b0	Event id	Description
0	0	0	0	dummy	Do nothing
0	0	0	1	-	*reserved*
0	0	1	0	-	*reserved*
0	0	1	1	Tx_en_hi	Pin TXENA is set high
0	1	0	0	RAMDAC_UP	AuxDAC1 will start executing a Ramp up
0	1	0	1	MODULATE_START	Defines the start of data modulation
0	1	1	0	MODULATE_END	Delay from the end of modulation (based on the last data bit loaded into modem - includes a 20 tick delay for the internal filters)
0	1	1	1	RAMDAC_DOWN	AuxDAC1 will start executing a Ramp down
1	0	0	0	Tx_en_lo	Pin TXENA is set low
1	0	0	1	dummy	Do nothing

When calculating the MODULATE_START timing value, the delay through the CMX7045's internal transmit filters and any external components must be taken into account to ensure that data bits appear on-air at the correct time (the filter delays are specified in section 8.1.4. The MODULATE_END event has an in-built delay of 20 ticks to allow the last bit to make its way out of the transmit filter. Allowance must be made for this built-in delay, as well as for the delay through any external components, when calculating the timing of the transmit power down events.

A working example of how to set up a transmit event sequence is shown in Table 7 (the order of events and delay timings shown are for illustrative purposes only):

Table 7 Example Tx Event Sequence Setup

Parameter	Event ID	Delay	Total	Explanation
dummy	0	0	0	Do nothing
MODULATE_START	5	1	1	Start feeding data to the transmit modulator and filters (this allows for the 20 tick storage delay in the Tx filters so that modulated data appears at the end of the RAMDAC ramp_up period – tick 57).
dummy	0	0	0	Do nothing
Tx_en_hi	3	0	1	Set TXENA line high
RAMDAC_UP	4	3	4	Insert 3 tick delay then initiate the RAMDAC ramp-up (for AIS, the transmitted signal will be carrier only at this point)

At this point during a transmission the CMX7045 feeds the entire message to the transmit modulator bit-by-bit. All subsequent transmit events are timed relative to the end of the last message bit, indicated by the MODULATE_END event.

RAMDAC_DOWN	7	2	0	Initiate the RAMDAC ramp-down immediately
Tx_en_lo	8	7	9	Insert 7 tick delay (to allow RAMDAC to fully ramp down) then set the TXENA line low.
MODULATE_END	6	5	14	Allows for process delays

Notes:
1. MODULATE_START must appear in the first group of timed events (table entries 1–5), MODULATE_END must appear in the final group (table entries 6-8).
2. It is feasible to place the RAMDAC_DOWN task *before* the MODULATE_END task if it is desired to continue modulation during the Ramp down period.

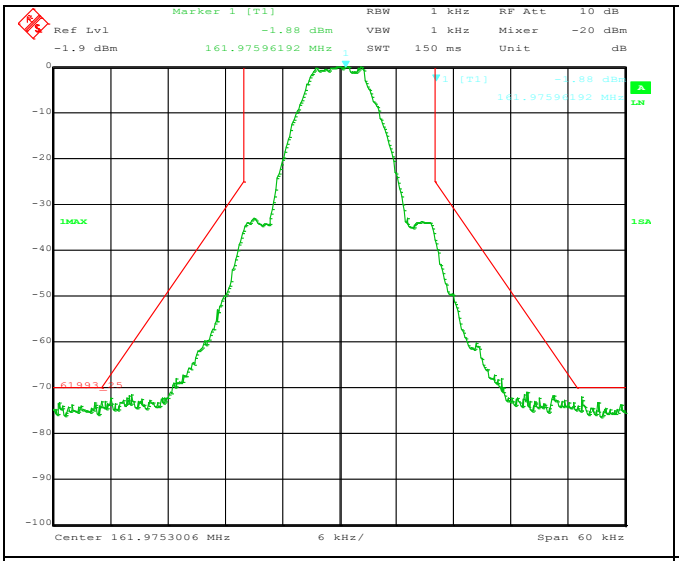
Assuming that the timing_start value has been set to 0 (see User Manual section 9.12.3) and the RAMDAC is set to its default values (312us), this sequence approximates to the SART timing with ideal hardware (RAMDAC starts 5bits / 12 ticks after SLOTCLK).

7.6.6 Modulation Formats

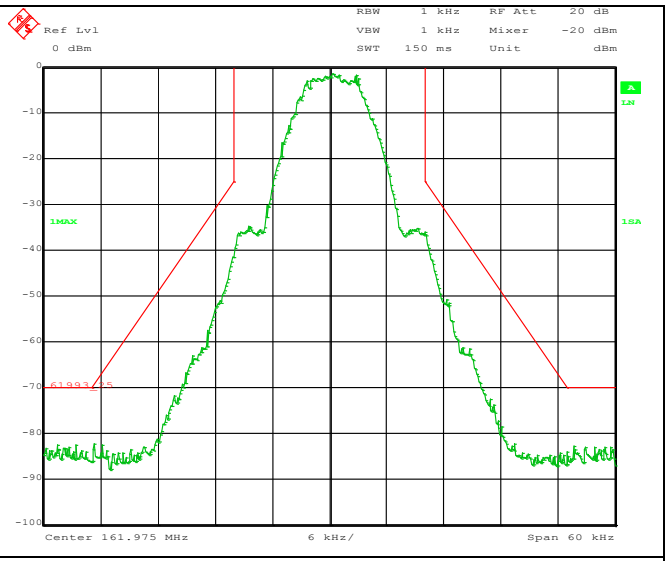
The CMX7045 can be configured to drive either a two-point VCO and Reference modulator.

Typical Tx spectrum plots for both modes are shown below (generated by modulating a signal generator with the outputs of MOD1 and MOD2 and then analysing the signal on a spectrum analyser). Note that these plots represent the steady-state transmission and so are shown with the Class A and Class B-SOTDMA spectrum mask (-70dBc). The Class B–CSTDMA standard specifies a slotted transmission with a mask at –60dBc.

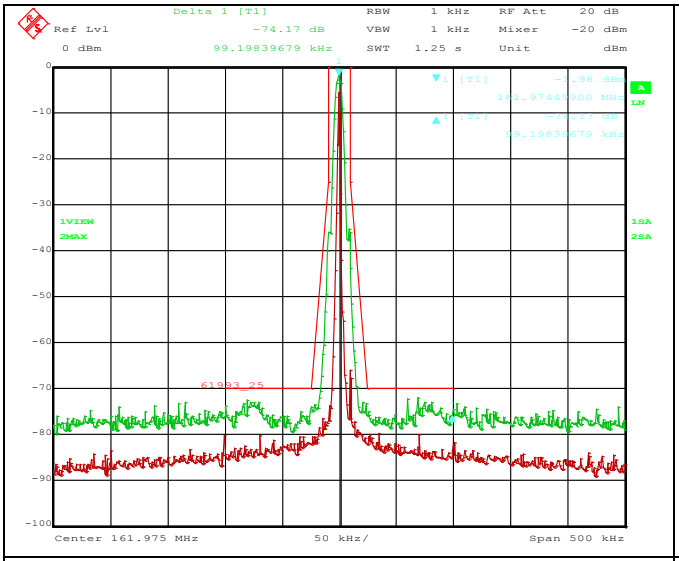
Table 8 Tx Spectrum Masks



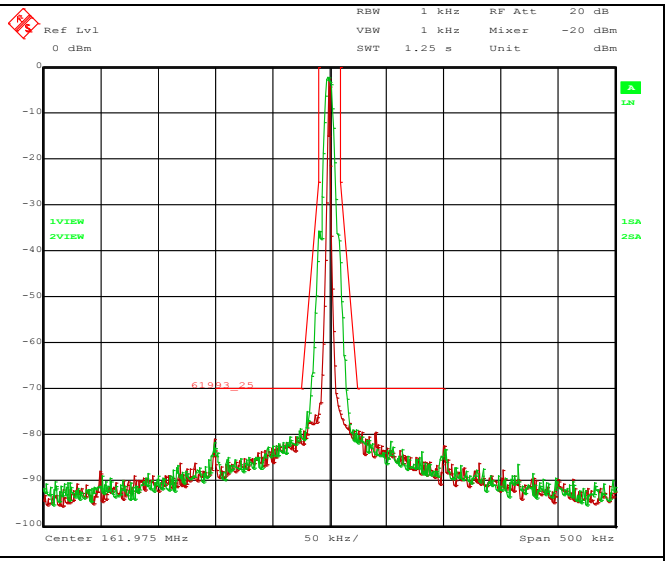
I/Q Tx spectrum mask



Two-point Tx spectrum mask



I/Q wideband spectrum



Two-point wideband spectrum

(Lower trace shows un-modulated signal generator)

7.7 Configuration Tasks and Codes

The device executes Configuration Tasks while in configuration mode. (See section 7.4.2 for a description of device operating modes and how to change between them, and User Manual section 9.12 for more details on a particular task). These tasks and their data are used to configure device subsystems.

Data required for the Configuration Task is loaded into the device using a Data Task, which can be executed at the same time as the Configuration Task if it requires less than four words.

Table 9 Configuration Tasks

Configuration Task	Words	Description	User Manual section
NULL	0	Do nothing	
EXIT_CONFIG	0	Return to Normal mode	
Tx I/Q or 2-point	1	Sets MOD1 and MOD2 output format (2-point or I/Q)	9.12.1
Tx MOD levels	1	Sets output levels on MOD1 and MOD2 signal pins	9.12.2
Tx_sequence	18	Loads Tx sequence commands	9.12.3
RAMDAC load	3 or 67	Configures RAMDAC and loads data table	9.12.4
Device Ident	2	Reads back the Device Ident and Version number	9.12.5
Enter Deep Sleep	0	Enter Deep Sleep mode	9.12.6
Leave Deep Sleep	0	Leave Deep Sleep mode	9.12.7
Reference clock	1	0 = 19.2MHz, 1 = 9.6MHz	9.12.8

7.8 System Clock Synthesisers

Two System Clock outputs, SYSCLK1and SYSCLK2, are available to drive additional circuits, as required. These are phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configuration registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configuration registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz.

The System Clock output divider stages are designed so that they have a 1:1 Mark-to-Space ratio when an even divide number is selected.

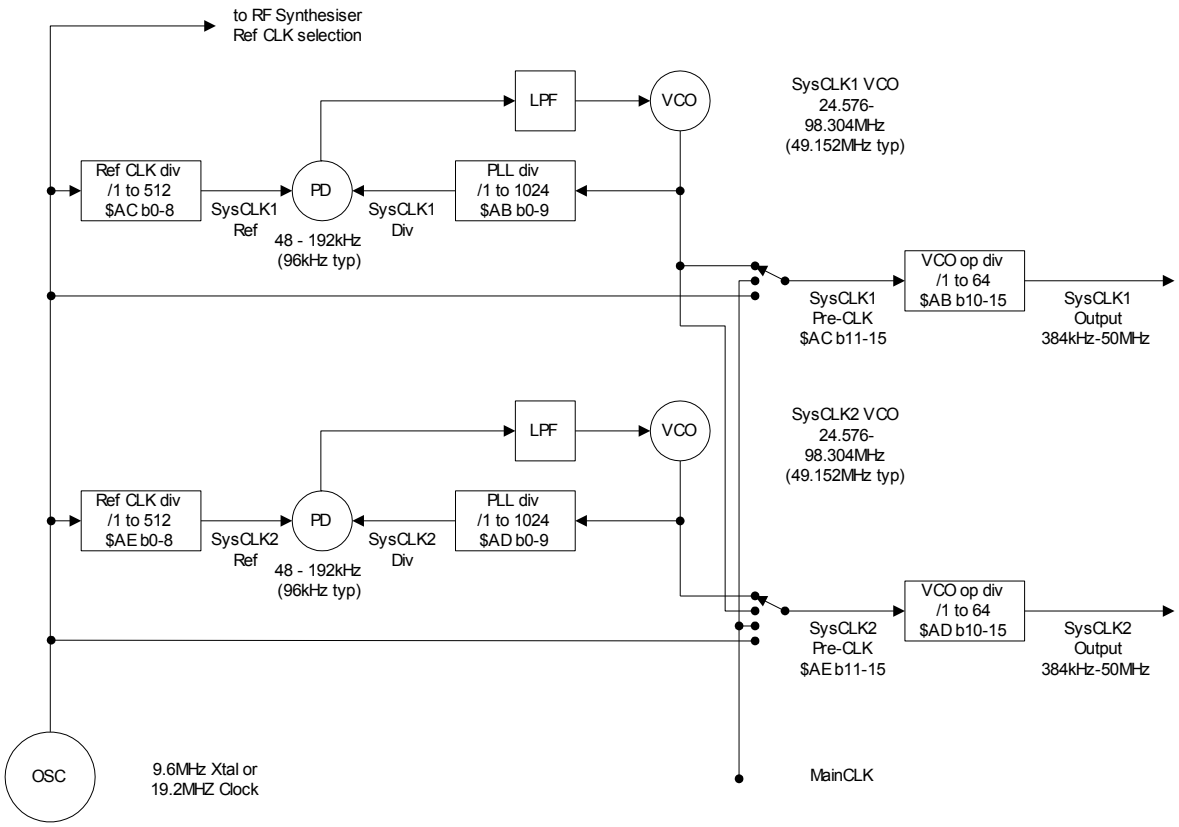


Figure 9 System Clock Generation

The CMX7045 includes a two-pin crystal oscillator circuit. This can either be configured as a 9.6MHz xtal oscillator, or the XTAL/CLK input can be driven by an externally generated 19.2MHz clock.

Note that, at power-on, the CMX7045 will inhibit both outputs are until they are enabled by a host command over the C-BUS.

7.9 Powersave

The CMX7045 implements a comprehensive powersaving scheme which will automatically enable the sections of the device that are required and return them to their powersaved state when no longer needed.

A Deep Sleep mode is also available through the Configuration mode which halts all signal processing activity and allows the analogue functions to be disabled so reducing power consumption to the lowest level – see section 7.4.9. This mode is entered automatically following successful activation of the device.

7.10 C-BUS Register Summary

Table 10 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	Data Write1	16
$A8	W	Data Write 2	16
$A9	R	Checksum 2 hi	16
$AA	R	Checksum 2 lo	16
$AB	W	System Clk 1 PLL Data	16
$AC	W	System Clk 1 Ref	16
$AD	W	System Clk 2 PLL Data	16
$AE	W	System Clk 2 Ref	16
$AF		*reserved*	
$B0		*reserved*	
$B1	W	Input/Output Gain and Routing	16
$B2		*reserved*	
$B3		*reserved*	
$B4		*reserved*	
$B5		*reserved*	
$B6	W	Data Write 3	16
$B7	W	Data Write 4	16
$B8	R	Checksum 1 hi	16
$B9	R	Checksum 1 lo	16
$BA		*reserved*	
$BB		*reserved*	
$BC		*reserved*	
$BD		*reserved*	
$BE		*reserved*	
$BF		*reserved*	
$C0	W	Power Down	16
$C1	W	Mode	16
$C2		*reserved*	
$C3		*reserved*	
$C4		*reserved*	
$C5	R	Status 2 / Product Identification Code	16
$C6	R	Status	16
$C7		*reserved*	
$C8	W	Command	16
$C9	R	ADC Data / FI Version Code	16
$CA		*reserved*	
$CB		*reserved*	
$CC		*reserved*	
$CD		*reserved*	
$CE	W	Interrupt Mask	16
$CF		*reserved*	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	−0.3	4.5	V
AV_{DD}- AV_{SS}	−0.3	4.5	V
Voltage on any pin to DV_{SS}	−0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	−0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding VBIAS) (i.e. VDEC, AVDD, AVSS, DVDD, DVSS)	−30	+30	mA
Current into or out of any other pin	−20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD} or CPV_{DD}	0	0.3	V
AV_{DD} and CPV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1600	mW
... Derating	–	16.0	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

Q3 Package (48-pad VQFN)	**Min.**	**Max.**	**Unit**
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C
Total Allowable Power Dissipation at Tamb = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
DV_{DD} – DV_{SS}		3.0	3.6	V
AV_{DD} – AV_{SS}		3.0	3.6	V
V_{DEC} – DV_{SS}	1	2.25	2.75	V
Operating Temperature		−40	+85	°C
Clock Frequency		9.6	19.2	MHz
Function Image™ size		24	46	kBytes

Notes: 1 The V_{DEC} supply is automatically created from DV_{DD} by the on-chip voltage regulator.

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Clock Frequency = 19.2MHz (±20ppm); Tamb = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V
Reference signal level = 300mV pk-pk with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	10				
All Powersaved (Deep Sleep mode)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	24	100	µA
AI_{DD} (AV_{DD} = 3.3V)		–	4	20	µA
Tx Mode	11				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	20	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	11	–	mA
Additional current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	250	–	µA
AI_{DD} (AV_{DD} = 3.3V)		–	300	–	µA
Additional current for the Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
AI_{DD} (AV_{DD} = 3.3V)		–	1	–	µA
Additional current for each Auxiliary DAC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	0	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA
CLK	11				
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input current (Vin = DV_{DD})		–	–	40	µA
Input current (Vin = DV_{SS})		−40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Leakage Current (Logic 1 or 0)		−1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1, (I_{OH} = 120µA)		90%	–	–	DV_{DD}
Output Logic 1, (I_{OH} = 1mA)		80%	–	–	DV_{DD}
Output Logic 0, (I_{OL} = 360µA)		–	–	10%	DV_{DD}
Output Logic 0, (I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
"Off" State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		−1.0	–	+1.0	µA
RDATA (output HiZ)		−1.0	–	+1.0	µA
V_{BIAS}	12				
Output voltage offset wrt AV_{DD}/2 (I_{OL} < 1µA)		−2%	–	+2%	AV_{DD}
Output impedance		–	22	–	kΩ

AC Parameters		Notes	Min.	Typ.	Max.	Unit
CLK Input						
'High' pulse width		20	19	–	–	ns
'Low' pulse width		20	19	–	–	ns
Input impedance (at 19.2MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Clock frequency			–	19.2	–	MHz
Clock stability/accuracy			–	–	±20	ppm
Clock start up (from powersave)			–	20	–	ms
V_{BIAS}						
Start up time (from powersave)			–	30	–	ms
Modulator Outputs (MOD 1, MOD 2)						
Power-up to output stable		21	–	50	100	µs
Modulator Attenuators						
Attenuation (at 0dB)		23	−1.0	0	+1.0	dB
Cumulative attenuation error (wrt attenuation at 0dB)			−0.6	0	+0.6	dB
Output impedance	Enabled	22	–	600	–	Ω
	Disabled	22	–	500	–	kΩ
Output current range (AV_{DD} = 3.3V)			−125	–	+125	µA
Output voltage range		24	0.5	–	AV_{DD} –0.5	V
Load resistance			20	–	–	kΩ
ADC 1 and 2 Inputs						
Source output impedance		25	–	–	24	kΩ
ADC						
Resolution			–	10	–	Bits
Input Range			–	–	10 to 90	%AV_{DD}
Conversion time			–	21	–	µs
Input impedance						
Resistance			–	> 10	–	MΩ
Capacitance			–	5	–	pF
Zero error (input offset to give ADC output = 0)			–	0	±10	mV
Integral non-linearity			–	–	±4	LSB
Differential non-linearity		27	–	–	±3	LSB
DACs						
Resolution			–	10	–	Bits
Settling time (to ±0.5 LSB)			–	10	–	µs
Output range		26	–	–	10 to 90	%AV_{DD}
Integral non-linearity			–	–	±4	LSB
Differential non-linearity		27	–	–	±1	LSB
Resistive load			5	–	–	kΩ
Noise output voltage in 30kHz bandwidth			–	5	–	µVrms

Notes:

10 Tamb = 25°C, not including any current drawn from the device pins by external circuitry.

11 Characteristics when driving the XTAL/CLK pin with an external clock source.

12 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 3.

20 Timing for an external input to the XTAL/CLK pin.

21 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable.

22 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

23 With respect to the signal at the feedback pin of the selected input port.

24 With the output driving a 20kΩ load to $AV_{DD}/2$.

25 Denotes output impedance of the driver of the auxiliary input signal, to ensure <1 bit additional error under nominal conditions.

26 With a load of 5kΩ to $AV_{DD}/2$

27 Guaranteed monotonic with no missing codes.

8.1.4 Parametric Performance

For the following conditions unless otherwise specified:
External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
CLK Frequency = 19.2MHz (±20ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V
Reference Signal Level = 300mV pk-pk with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.

Transmit Parameters	Notes	Min.	Typ.	Max.	Unit
AIS (GMSK 9600bps), 25kHz channel					
Bit rate accuracy		–	–	±50	ppm
BT		–	0.4	–	
Storage time (filter delay)	30	–	8	–	bits
Tx Buffer size		–	–	176	bytes
SLOT CLOCK					
Rise/Fall time		–	–	1.0	µs

Notes:
30. Through a GMSK/GFSK transmit filter.

8.2 C-BUS Timing

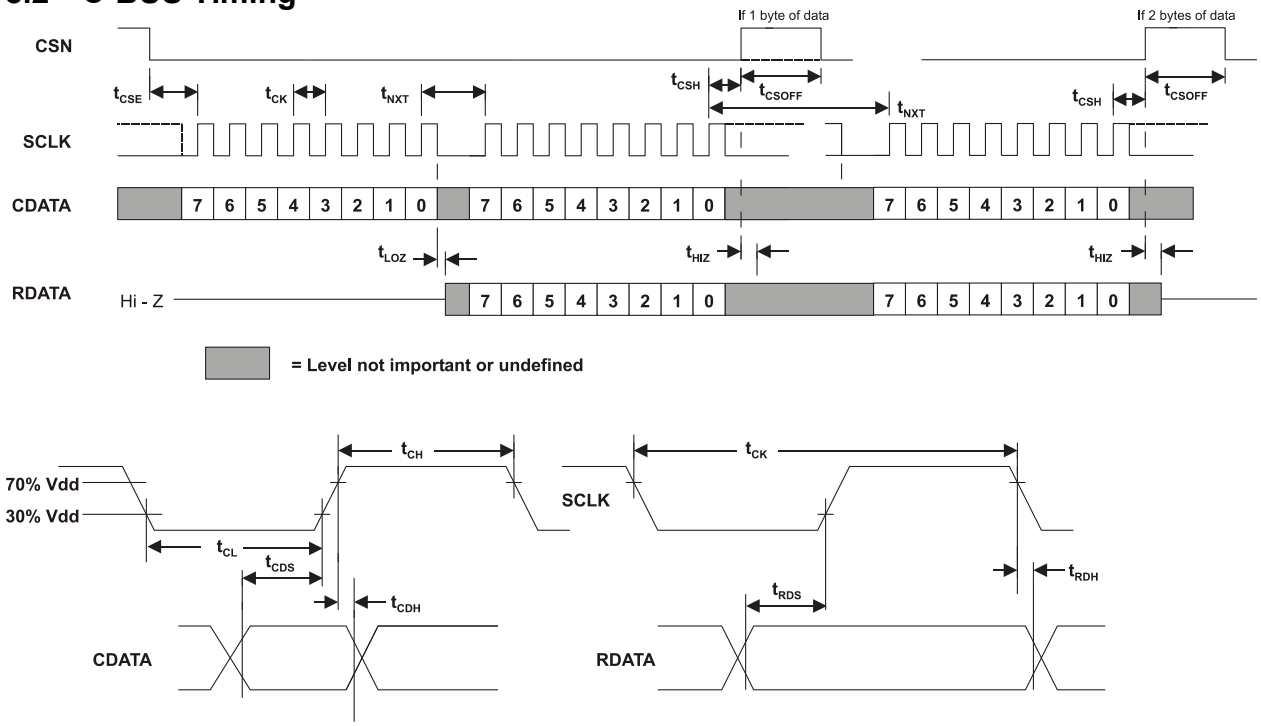


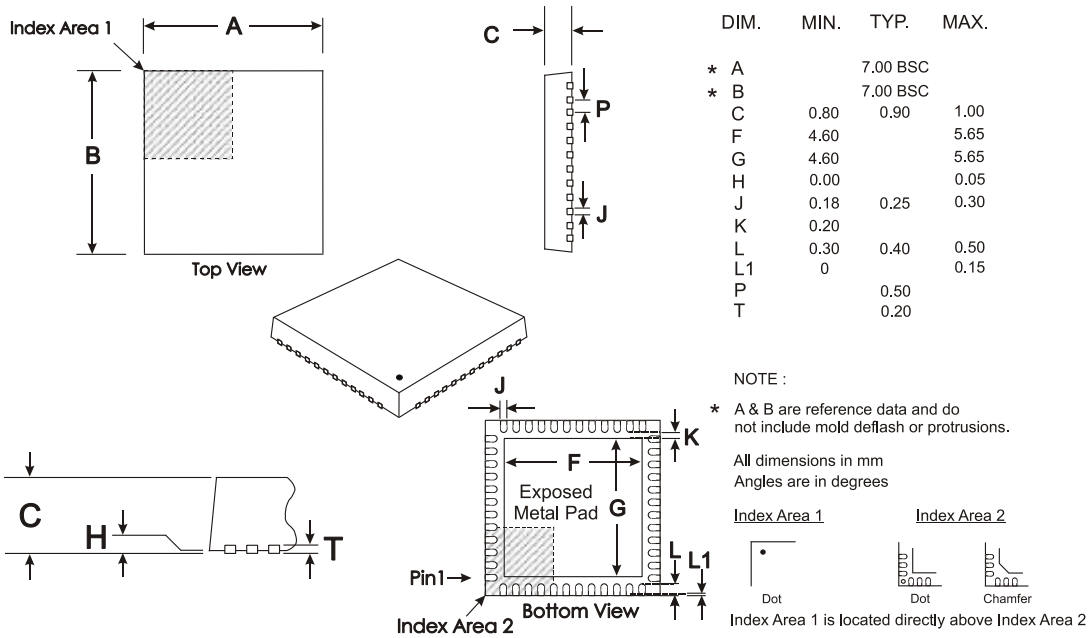
Figure 10 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA output enable time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7045 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

8.3 Packaging



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

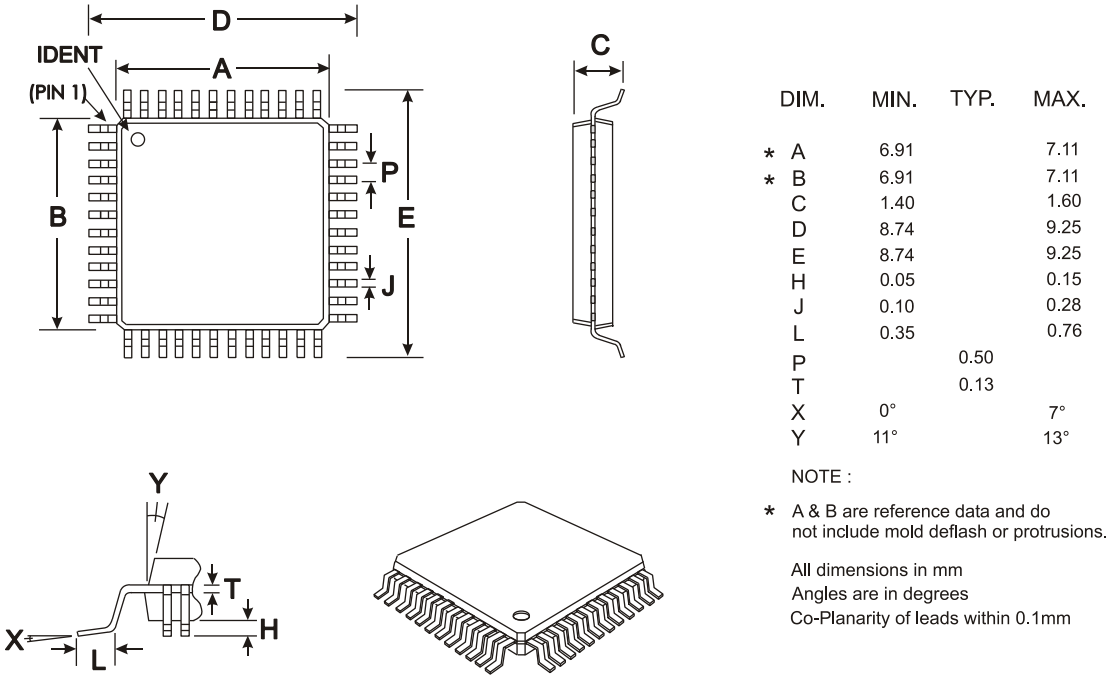
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 11 Mechanical Outline for 48-pad VQFN Package (Q3)

Order as CMX7045Q3



DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 12 Mechanical Outline for 48-pin LQFP Package (L4)

Order as CMX7045L4

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CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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