COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(on)}$	I_D T_A = 25℃
Q1	30V	60mΩ @ V_{GS} = 10V	3.4A
		100mΩ @ V_{GS} = 4.5V	2.7A
Q2	-30V	95mΩ @ V_{GS} = -10V	-2.8A
		140mΩ @ V_{GS} = -4.5V	-2.3A

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free Finish; RoHS compliant (Note 1)**
- **Halogen and Antimony Free. "Green" Device (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Description and Applications

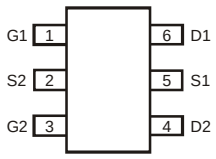
This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Backlighting
- DC-DC Converters
- Power management functions

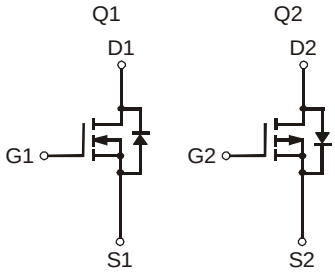
Mechanical Data

- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish – Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.013 grams (approximate)

TSOT26



Top View



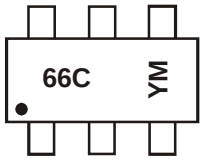
N-Channel P-Channel

Ordering Information (Note 3)

Part Number	Case	Packaging
DMG6602SVT-7	TSOT26	3000 / Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
3. For packaging details, go to our website at http://www.diodes.com.

Marking Information



66C = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: X = 2010)
M = Month (ex: 9 = September)

Date Code Key

Year	2010	2011	2012	2013	2014	2015	2016	2017
Code	X	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings – Q1 @TA = 25℃ unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = 10V	Steady State	T_A = 25℃ T_A = 70℃	I_D	3.4 2.7	A
Continuous Drain Current (Note 5) V_{GS} = 4.5V	Steady State	T_A = 25℃ T_A = 70℃	I_D	2.7 2.2	A
Maximum Continuous Body Diode Forward Current (Note 5)			I_S	1.5	A
Pulsed Drain Current (Note 5)			I_{DM}	25	A

Maximum Ratings – Q2 @TA = 25℃ unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = -10V	Steady State	T_A = 25℃ T_A = 70℃	I_D	-2.8 -2.4	A
Continuous Drain Current (Note 5) V_{GS} = -4.5V	Steady State	T_A = 25℃ T_A = 70℃	I_D	-2.3 -2.1	A
Maximum Continuous Body Diode Forward Current (Note 5)			I_S	-1.5	A
Pulsed Drain Current (Note 5)			I_D	-20	A

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 4)	T_A = 25℃	P_D	0.84	W
	T_A = 70℃		0.52	
Thermal Resistance, Junction to Ambient (Note 4)	Steady state	$R_{\theta JA}$	155	℃/W
	t<10s		109	
Total Power Dissipation (Note 5)	T_A = 25℃	P_D	1.27	W
	T_A = 70℃		0.8	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	102	℃/W
	t<10s		71	
Thermal Resistance, Junction to Case (Note 5)		$R_{\theta JC}$	34	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	℃

Notes: 4. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

Electrical Characteristics – Q1 NMOS @ T_A = 25°C unless otherwise stated

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	-	2.3	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	-	38 55	60 100	mΩ	V_{GS} = 10V, I_D = 3.1A V_{GS} = 4.5V, I_D = 2A
Forward Transfer Admittance	$\|Y_{fs}\|$	-	4	-	S	V_{DS} = 5V, I_D = 3.1A
Diode Forward Voltage	V_{SD}	-	0.8	1	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	-	290	400	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.2MHz
Output Capacitance	C_{oss}	-	40	80		
Reverse Transfer Capacitance	C_{rss}	-	40	80		
Gate Resistance	R_g	-	1.4	-	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	-	4	6	nC	V_{DS} = 15V, V_{GS} = 4.5V, I_D = 3.1A
Total Gate Charge (V_{GS} = 10V)	Q_g	-	9	13		V_{DS} = 15V, V_{GS} = 10V, I_D = 3A
Gate-Source Charge	Q_{gs}	-	1.2	-		
Gate-Drain Charge	Q_{gd}	-	1.5	-		
Turn-On Delay Time	$t_{D(on)}$	-	3	-	ns	V_{GS} = 10V, V_{DS} = 15V, R_G = 3Ω, R_L = 4.7Ω
Turn-On Rise Time	t_r	-	5	-		
Turn-Off Delay Time	$t_{D(off)}$	-	13	-		
Turn-Off Fall Time	t_f	-	3	-		

Notes: 6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to product testing.

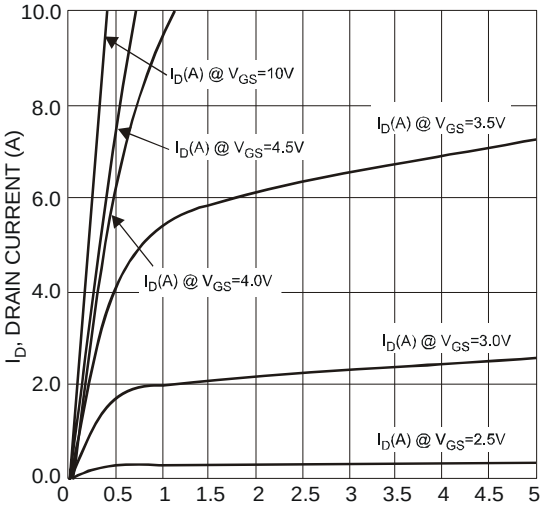


Fig. 1 Typical Output Characteristics

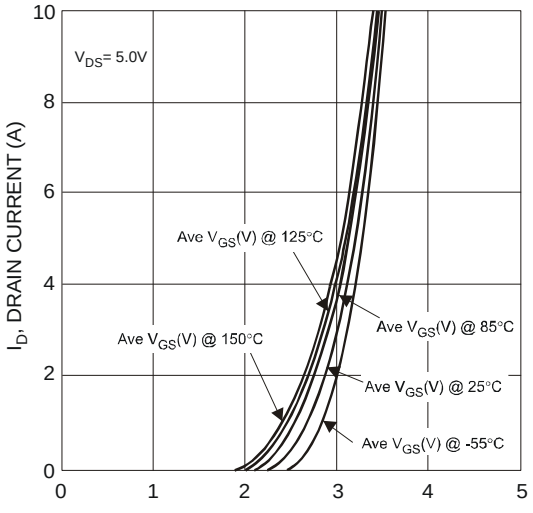


Fig. 2 Typical Transfer Characteristics

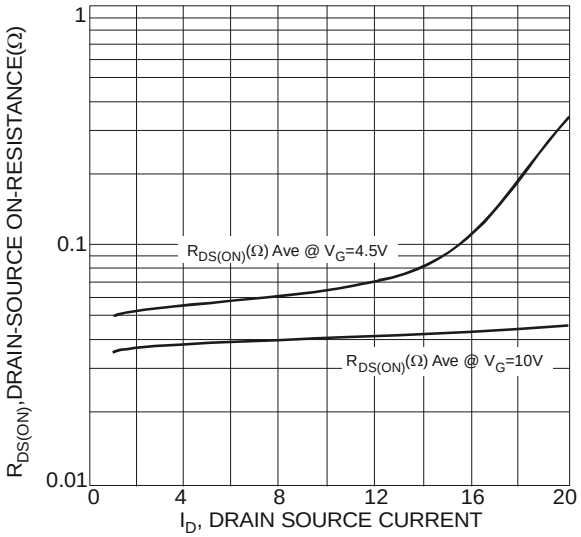


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

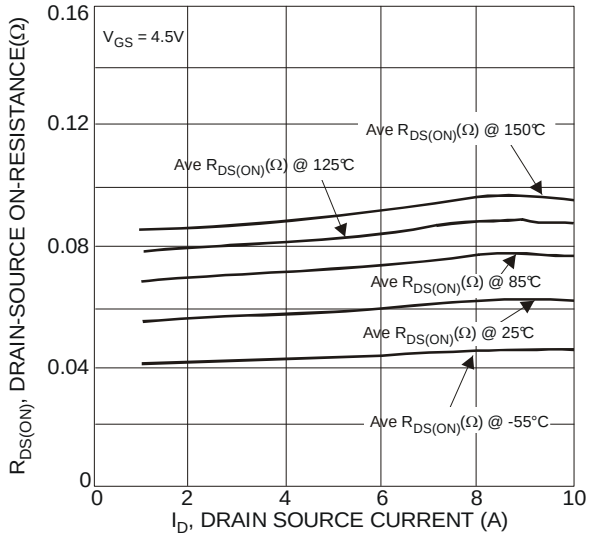


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

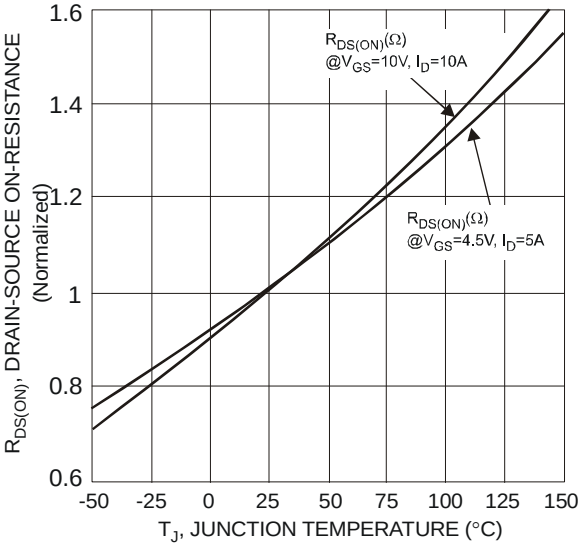


Fig. 5 On-Resistance Variation with Temperature

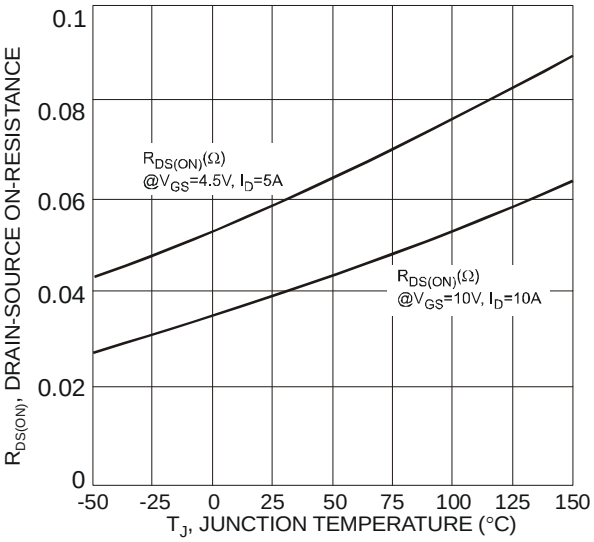


Fig. 6 On-Resistance Variation with Temperature

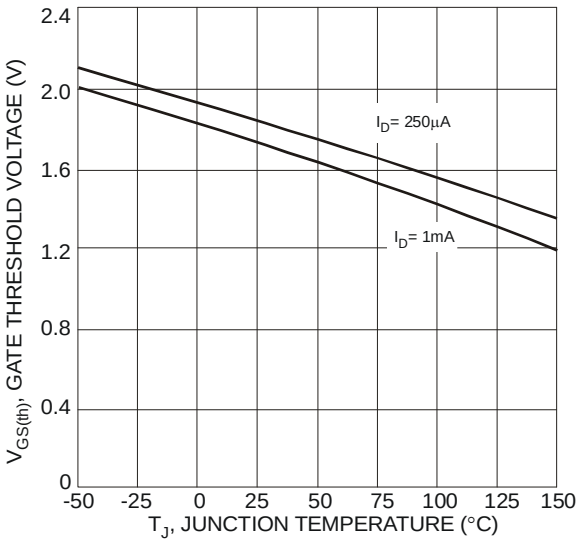


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

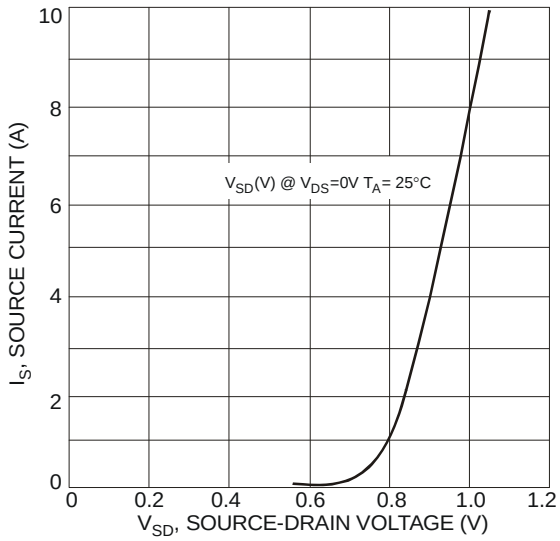


Fig. 8 Diode Forward Voltage vs. Current

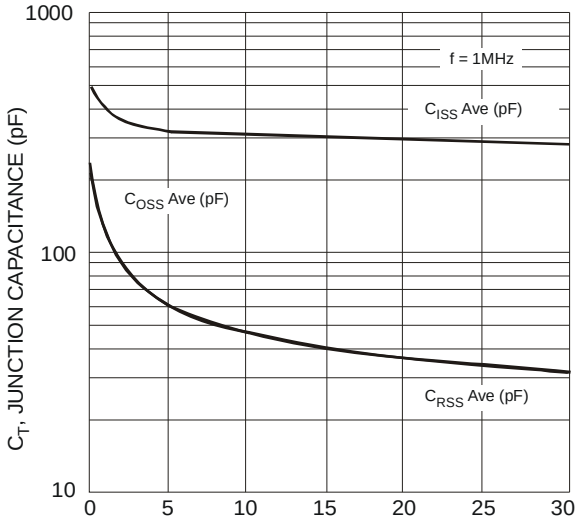


Fig. 9 Typical Junction Capacitance

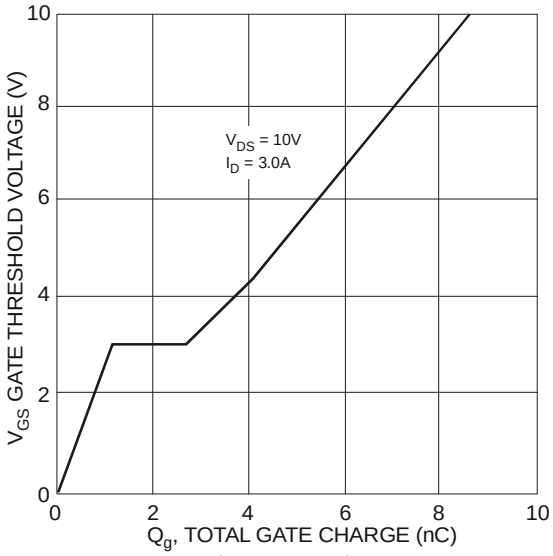


Fig. 10 Gate Charge

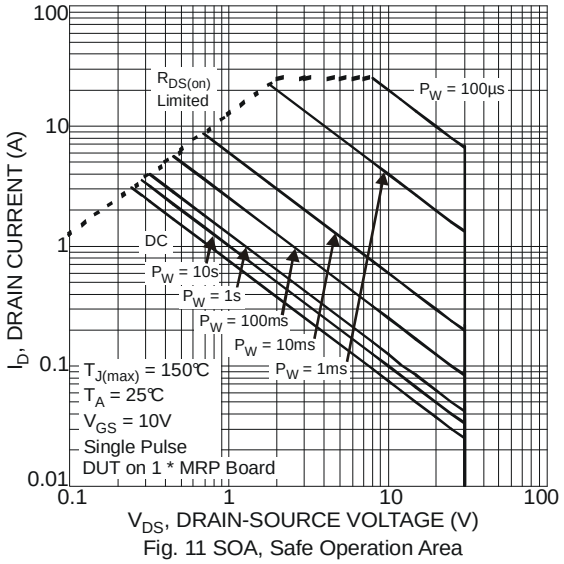


Fig. 11 SOA, Safe Operation Area

Electrical Characteristics – Q2 PMOS @ T_A = 25°C unless otherwise stated

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	-	-	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1.0	µA	V_{DS} = -24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	-	-2.3	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	-	73 99	95 140	mΩ	V_{GS} = -10V, I_D = -2.7A V_{GS} = -4.5V, I_D = -2A
Forward Transfer Admittance	$\|Y_{fs}\|$	-	6	-	S	V_{DS} = -5V, I_D = -2.7A
Diode Forward Voltage	V_{SD}	-	-0.8	-1.0	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	-	350	420	pF	V_{DS} = -15V, V_{GS} = 0V, f = 1.2MHz
Output Capacitance	C_{oss}	-	50	100		
Reverse Transfer Capacitance	C_{rss}	-	45	80		
Gate Resistance	R_g	-	17.1	-	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	-	4	6	nC	V_{DS} = -15V, V_{GS} = -4.5V, I_D = -3A
Total Gate Charge (V_{GS} = -10V)	Q_g	-	7	9		V_{DS} = -15V, V_{GS} = -10V, I_D = -3A
Gate-Source Charge	Q_{gs}	-	0.9	-		
Gate-Drain Charge	Q_{gd}	-	1.2	-		
Turn-On Delay Time	$t_{D(on)}$	-	4.8	-	ns	V_{GS} = -10V, V_{DS} = -15V, R_G = 6Ω, R_L = 15Ω
Turn-On Rise Time	t_r	-	7.3	-		
Turn-Off Delay Time	$t_{D(off)}$	-	20	-		
Turn-Off Fall Time	t_f	-	13	-		

Notes: 6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to production testing.

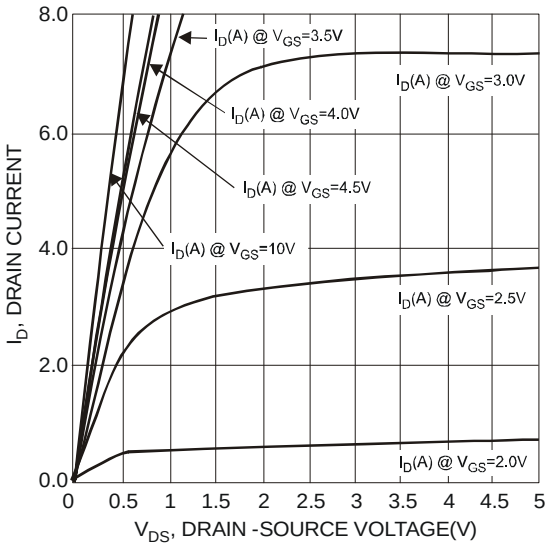


Fig. 12 Typical Output Characteristics

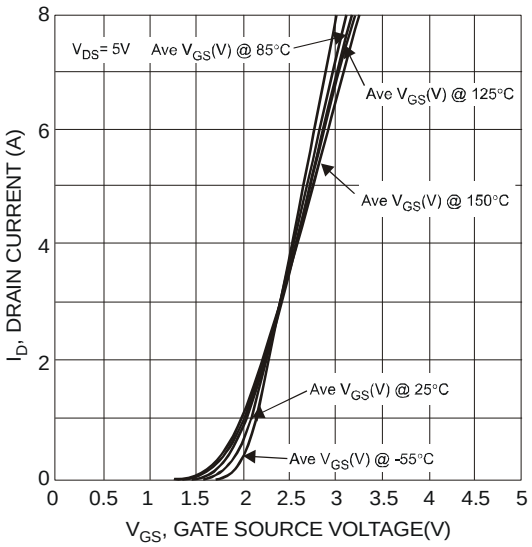


Fig. 13 Typical Transfer Characteristics

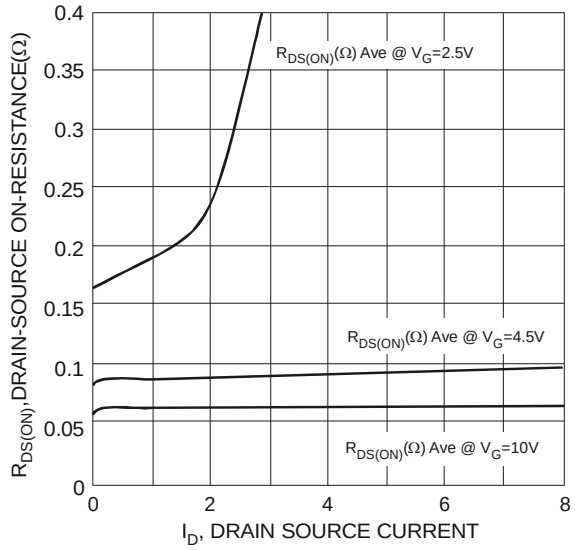


Fig. 14 Typical On-Resistance vs. Drain Current and Gate Voltage

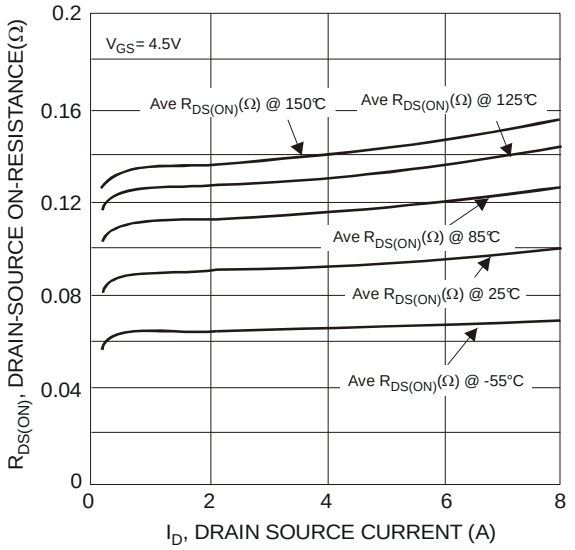


Fig. 15 Typical On-Resistance vs. Drain Current and Temperature

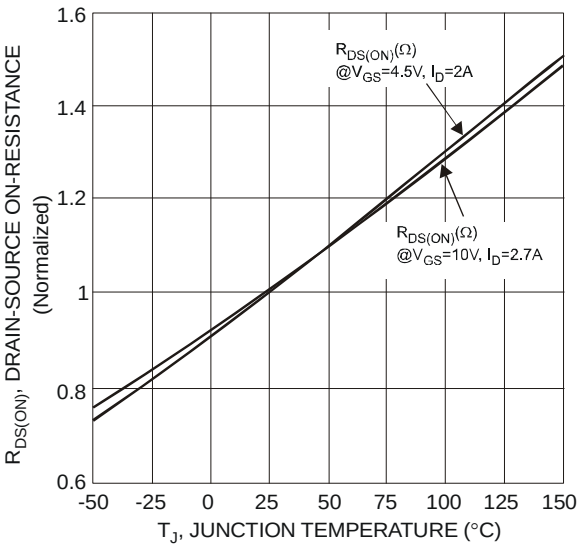


Fig. 16 On-Resistance Variation with Temperature

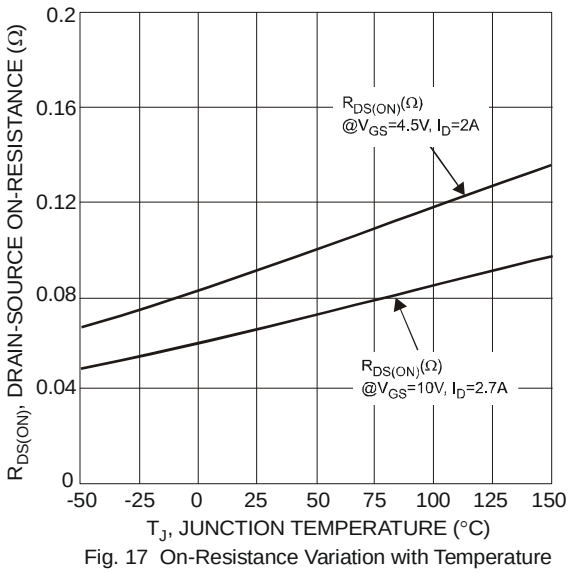


Fig. 17 On-Resistance Variation with Temperature

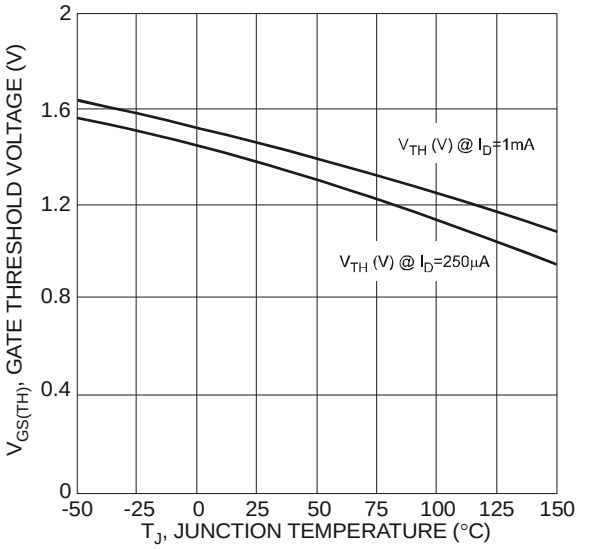


Fig. 18 Gate Threshold Variation vs. Ambient Temperature

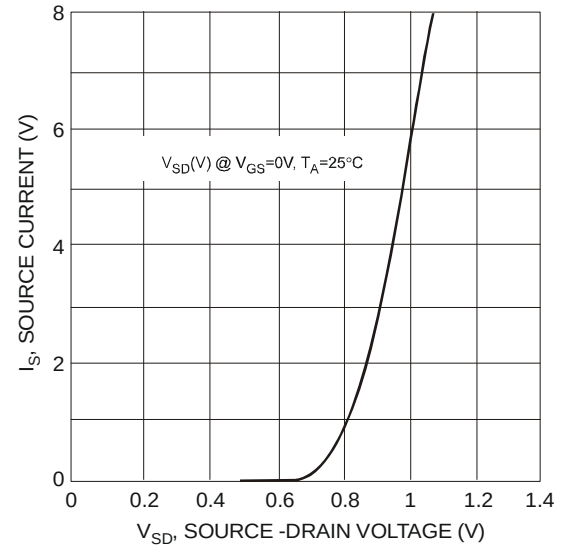


Fig. 19 Diode Forward Voltage vs. Current

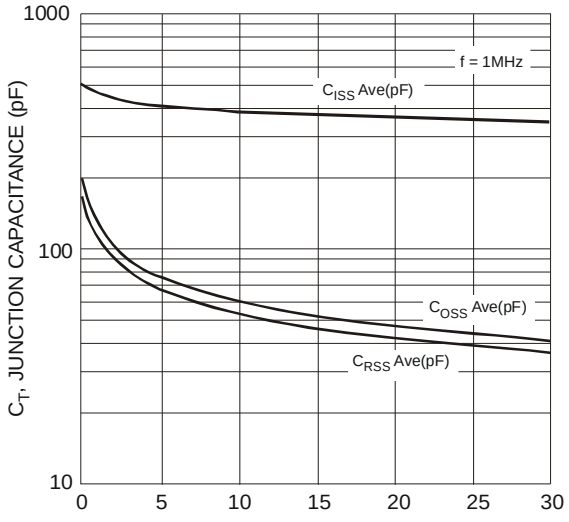


Fig. 20 Typical Junction Capacitance

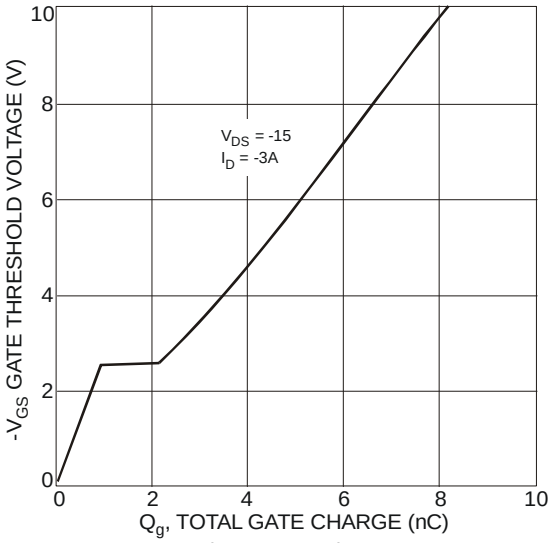


Fig. 21 Gate Charge

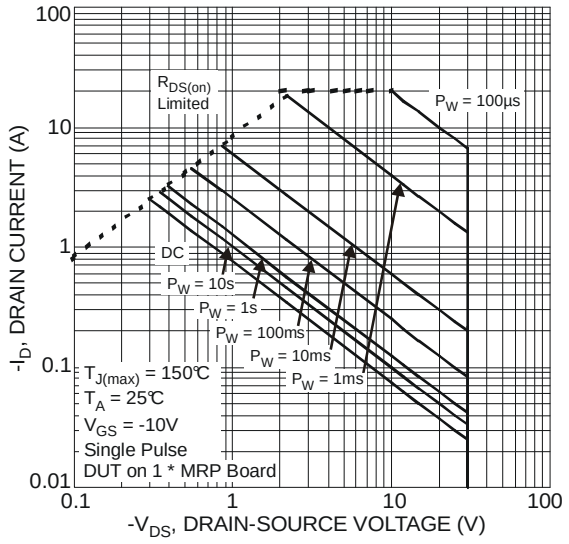


Fig. 22 SOA, Safe Operation Area

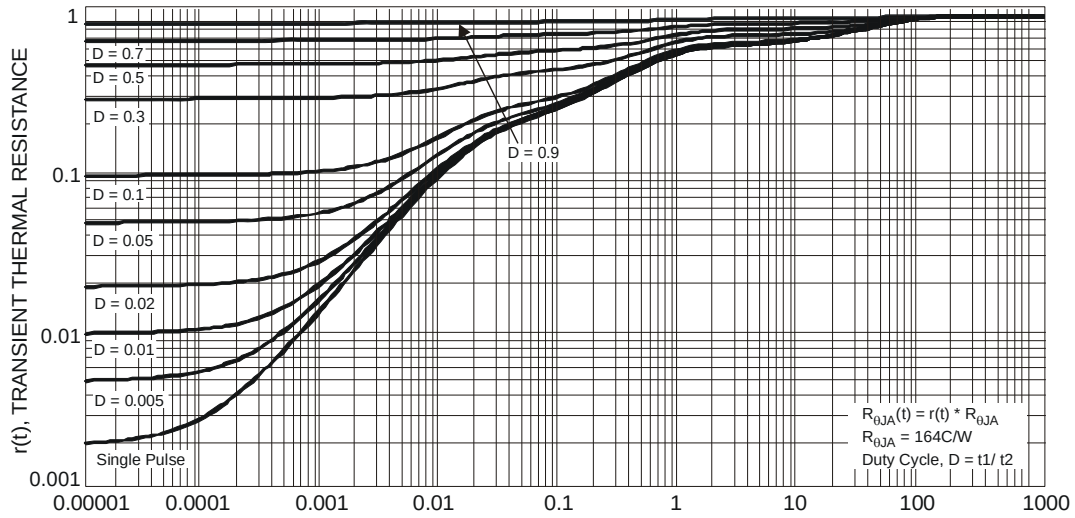
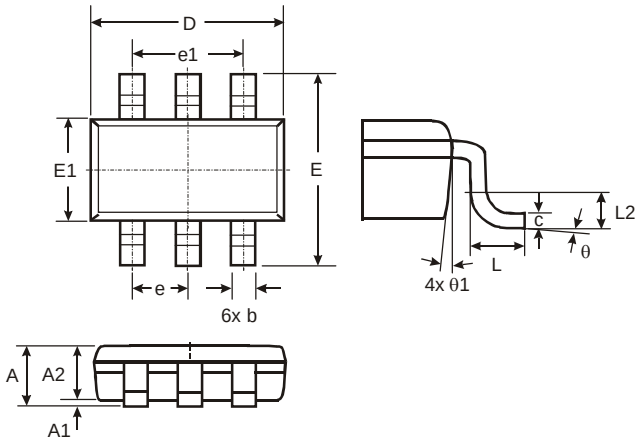


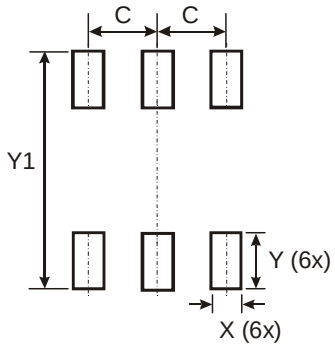
Fig. 23 Transient Thermal Resistance

Package Outline Dimensions



TSOT26			
Dim	**Min**	**Max**	**Typ**
A	–	1.00	–
A1	0.01	0.10	–
A2	0.84	0.90	–
D	–	–	2.90
E	–	–	2.80
E1	–	–	1.60
b	0.30	0.45	–
c	0.12	0.20	–
e	–	–	0.95
e1	–	–	1.90
L	0.30	0.50	
L2	–	–	0.25
θ	0°	8°	4°
θ1	4°	12°	–
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

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