WM8762

24-bit 192kHz Stereo DAC

DESCRIPTION

The WM8762 is a high performance stereo DAC designed for audio applications such as DVD, home theatre systems, and digital TV. The WM8762 supports data input word lengths from 16 to 24-bits and sampling rates up to 192kHz. The WM8762 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and stereo DAC in a very small 8-pin SOIC package.

The WM8762 supports a 16-24-bit left justified digital audio interface.

The WM8762 is an ideal device to interface to AC-3™, DTS™, and MPEG audio decoders for surround sound applications, or for use in DVD players, including supporting the implementation of 2 channels at 192kHz for high-end DVD-Audio applications.

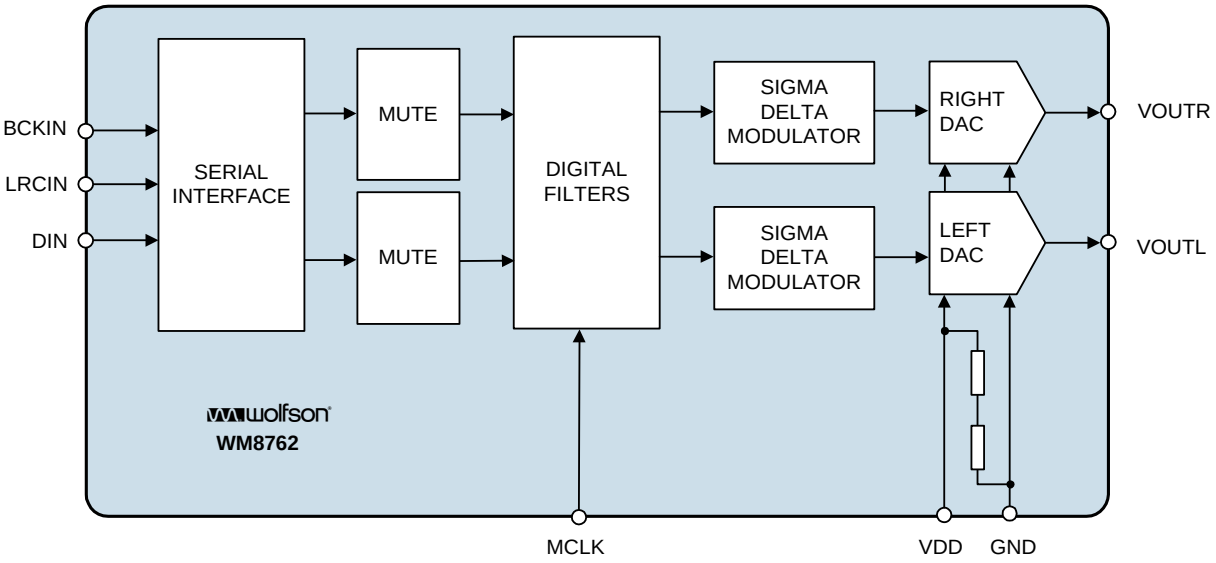
FEATURES

- Stereo DAC
- Audio Performance
  - 98dB SNR ('A' weighted @ 48kHz)
  - -84dB THD
- Sampling Frequency: 8kHz – 192kHz
- Audio Data Interface Format
  - 16-24-Bit Left Justified
- 2.7V – 5.5V Supply Operation
- 8-lead SOIC Package

APPLICATIONS

- DVD Players
- Digital TV
- Digital Set Top Box

BLOCK DIAGRAM



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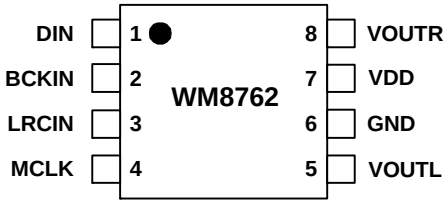
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8762CGED	-40 to +85°C	8-lead SOIC (Pb-free)	MSL1	260°C
WM8762CGED/R	-40 to +85°C	8-lead SOIC (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel Quantity = 3,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DIN	Digital input	Serial audio data input
2	BCKIN	Digital input	Bit clock input
3	LRCIN	Digital input	Sample rate clock input
4	MCLK	Digital input	System master clock input
5	VOUTL	Analogue output	Left channel DAC output
6	GND	Supply	Analogue ground supply
7	VDD	Supply	Positive supply
8	VOUTR	Analogue output	Right channel DAC output

Note:
Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltage	-0.3V	+7V
Voltage range digital inputs	GND -0.3V	VDD +0.3V
Master Clock Frequency		50MHz
Operating temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply range	VDD		2.7		5.5	V
Ground	GND			0		V
Supply current		VDD = 5V		26		mA
Supply current		VDD = 3.3V		20		mA
Power down current (note 3)		VDD=3.3V		0.5		mA

ELECTRICAL CHARACTERISTICS

Test Conditions

VDD = 5V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2			V
Output LOW	V_{OL}	I_{OL} = 2mA			0.10 x VDD	V
Output HIGH	V_{OH}	I_{OH} = 2mA	0.9 x VDD			V
DAC Output (Load = 10kΩ 50pF)						
0dBFS Full scale output voltage		At DAC outputs		1.2 x VDD/5		V_{rms}
SNR (Note 1,2)		A-weighted, @ fs = 48kHz		98		dB
SNR (Note 1,2)		A-weighted @ fs = 96kHz		95		dB
SNR (Note 1,2)		A-weighted @ fs = 192kHz		92		dB
SNR (Note 1,2)		A-weighted, @ fs = 48kHz VDD = 3.3V		95		dB
SNR (Note 1,2)		A-weighted @ fs = 96kHz VDD = 3.3V		95		dB
SNR (Note 1,2)		Non 'A' weighted @ fs = 48kHz		92		dB
THD		1kHz, 0dBFS		-84		dB
Dynamic range (Note 2)		1kHz, THD+N @ -60dBFs	90	98		dB
Analogue Output Levels						
Output level		Load = 10kΩ, 0dBFS		1.2		V_{RMS}
		Load = 10kΩ, 0dBFS, (VDD = 3.3V)		0.79		V_{RMS}
Gain mismatch channel-to-channel				±1		%FSR
Minimum resistance load		To midrail or a.c. coupled		1		kΩ
		To midrail or a.c. coupled (VDD = 3.3V)		1		kΩ
Maximum capacitance load		5V or 3.3V		100		pF
Output d.c. level				VDD/2		V
Power On Reset (POR)						
POR threshold				2.4		V

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. Power down occurs 1.5μs after MCLK stops.

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

POWER ON RESET (POR)

The WM8762 has an internal power-on-reset (POR) circuit which is used to reset the digital logic into a default state after power up. A block diagram of the reset circuit is shown in Figure 1.

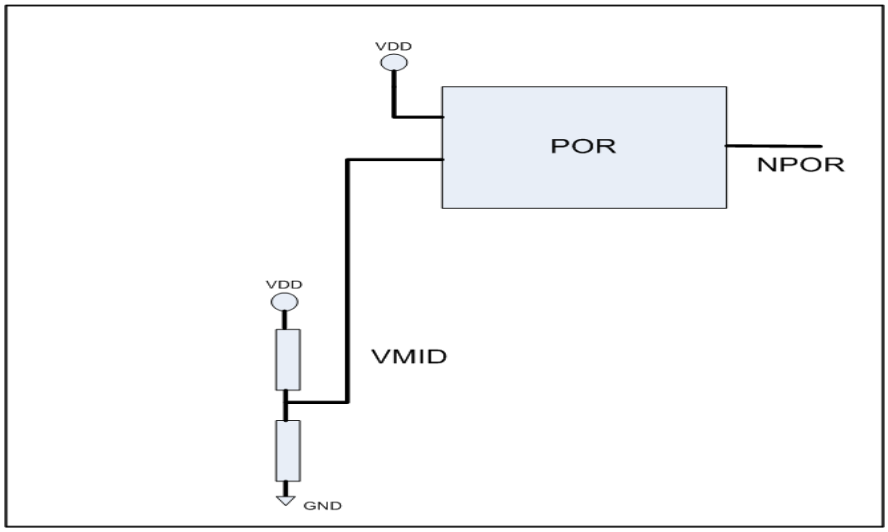


Figure 1 Block Diagram of Power-On-Reset

The active low reset signal NPOR will be asserted low until VDD=2.4V, which means VMID rises to 1.2V. When this threshold has been reached, then the NPOR is released and the digital interface has been reset. This is illustrated in the diagram shown in Figure 2.

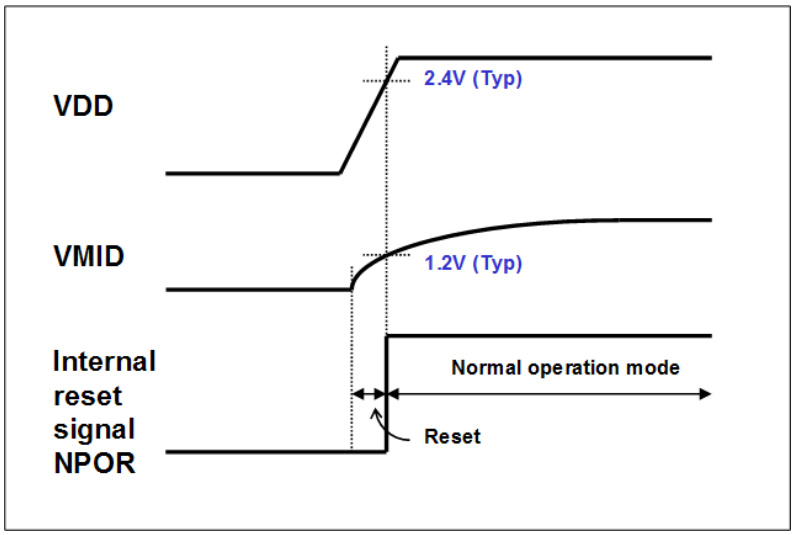


Figure 2 Generation of Internal NPOR at Power-On-Reset

Figure 3 illustrates the NPOR generation when the power is removed.

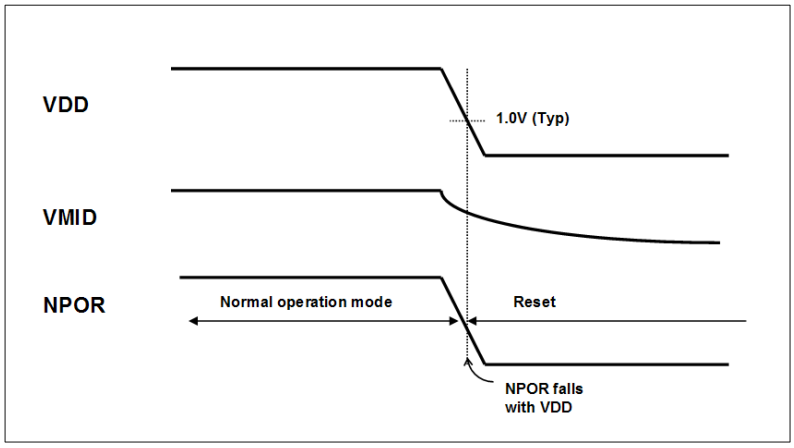


Figure 3 Generation of NPOR at Power-Off-Reset

MASTER CLOCK TIMING

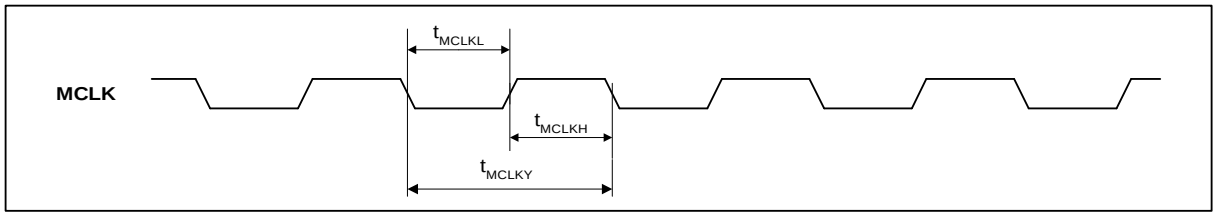


Figure 4 Master Clock Timing Requirements

Test Conditions

VDD = 5V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK Master clock pulse width high	t_{MCLKH}		8			ns
MCLK Master clock pulse width low	t_{MCLKL}		8			ns
MCLK Master clock cycle time	t_{MCLKY}		20			ns
MCLK Duty cycle			40:60		60:40	
Time from MCLK stopping to power down.			1.5		12	µs

DIGITAL AUDIO INTERFACE

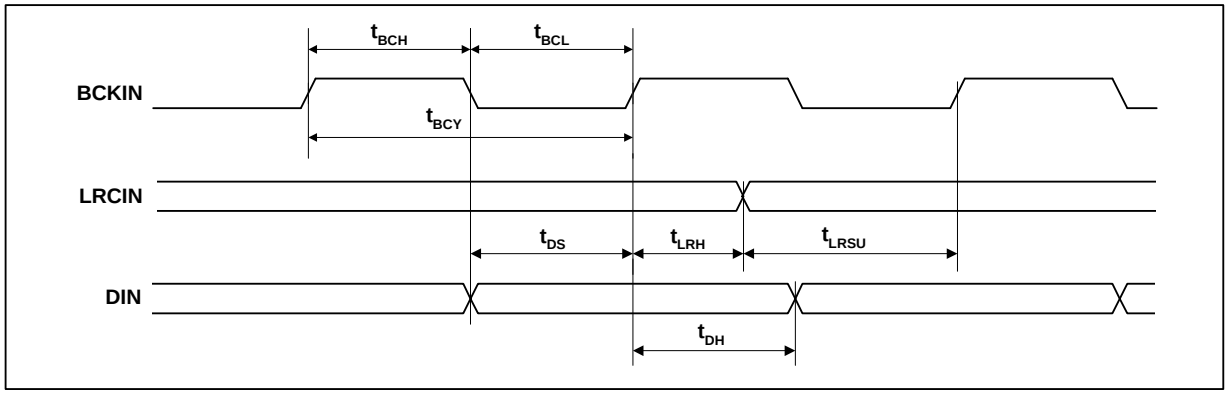


Figure 5 Digital Audio Data Timing

Test Conditions

VDD = 5V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCKIN cycle time	t_{BCY}		40			ns
BCKIN pulse width high	t_{BCH}		16			ns
BCKIN pulse width low	t_{BCL}		16			ns
LRCIN set-up time to BCKIN rising edge	t_{LRSU}		8			ns
LRCIN hold time from BCKIN rising edge	t_{LRH}		8			ns
DIN set-up time to BCKIN rising edge	t_{DS}		8			ns
DIN hold time from BCKIN rising edge	t_{DH}		8			ns

DEVICE DESCRIPTION

GENERAL INTRODUCTION

The WM8762 is a high performance DAC designed for digital consumer audio applications. The range of features make it ideally suited for use in DVD players, AV receivers and other consumer audio equipment.

The WM8762 is a complete 2-channel stereo audio digital-to-analogue converter, including digital interpolation filter, multi-bit sigma delta with dither, and switched capacitor multi-bit stereo DAC and output smoothing filters. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs. A novel multi bit sigma-delta DAC design is used, utilising a 128x oversampling rate to optimise signal to noise performance and offer increased clock jitter tolerance. (In 'high-rate' operation, the oversampling ratio is 64x for system clocks of 128fs or 192fs)

Operation using master clocks of 256fs, 384fs, 512fs or 768fs is provided, selection between clock rates being automatically controlled. Sample rates (fs) from less than 8kHz to 192KHz are allowed, provided the appropriate system clock is input.

The audio data interface supports a 16-24-bit left justified interface format. A single 2.7-5.5V supply may be used, the output amplitude scaling with absolute supply level. Low supply voltage operation and low current consumption combined with the low pin count small package make the WM8762 attractive for many consumer applications.

The device is packaged in a small 8-pin SOIC.

DAC CIRCUIT DESCRIPTION

The WM8762 DAC is designed to allow playback of 24-bit PCM audio or similar data with high resolution and low noise and distortion. Sample rates up to 192kHz may be used, with much lower sample rates acceptable provided that the ratio of sample rate (LRCIN) to system master clock (MCLK) is maintained at one of the required rates.

The two DACs on the WM8762 are implemented using sigma-delta oversampled conversion techniques. These require that the PCM samples are digitally filtered and interpolated to generate a set of samples at a much higher rate than the input rate. This sample stream is then digitally modulated to generate a digital pulse stream that is then converted to analogue signals in a switched capacitor DAC. The advantage of this technique is that the DAC is linearised using noise shaping techniques, allowing the 24-bit resolution to be met using non-critical analogue components. A further advantage is that the high sample rate at the DAC output means that smoothing filters on the output of the DAC need only have fairly crude characteristics in order to remove the characteristic steps, or images, on the output of the DAC. To ensure that generation of tones characteristic to sigma-delta converters is not a problem, dithering is used in the digital modulator and a higher order modulator is used. The multi-bit switched capacitor technique used in the DAC reduces sensitivity to clock jitter, and dramatically reduces out of band noise compared to switched current or single bit techniques used in other implementations.

The outputs of the 2 DACs are buffered out of the device by buffer amplifiers. These amplifiers will source load currents of several mA and sink current up to 1.5mA allowing significant loads to be driven. The output source is active and the sink is Class A, i.e. fixed value, so greater loads might be driven if an external 'pull-down' resistor is connected at the output.

Typically an external low pass filter circuit will be used to remove residual out of band noise characteristic of delta sigma converters. However, the advanced multi-bit DAC used in WM8762 produces far less out of band noise than single bit traditional sigma delta DACs, and so in many applications this filter may be removed, or replaced with a simple RC pole.

DAC OUTPUT PHASE

In the DAC to analogue output, the analogue output data VOUTL/R, is a phase inverted representation of the digital input signal.

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master clock can be applied directly through the MCLK input pin with no configuration necessary for sample rate selection.

Note that on the WM8762, MCLK is used to derive clocks for the DAC path. The DAC path consists of DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

The device can be powered down by stopping MCLK. In this state the power consumption is substantially reduced.

DIGITAL AUDIO INTERFACE

WM8762 supports the left justified audio interface format. The WM8762 supports word lengths of 16-24 bits (MSB first). The word length may be any value up to 24-bits. (If the word length shorter than 24-bits is used, the unused bits will be padded with zeros).

In left justified mode, the MSB of DIN is sampled by the WM8762 on the first rising edge of BCKIN following a LRCIN transition. LRCIN is high during the left samples and low during the right samples.

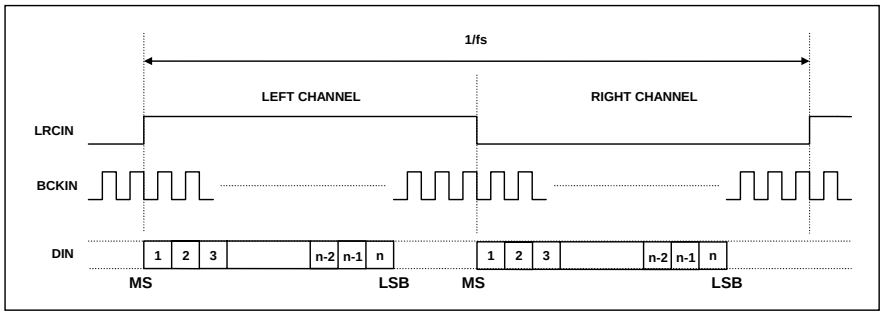


Figure 6 Left Justified Mode Timing Diagram

AUDIO DATA SAMPLING RATES

The master clock for WM8762 supports audio sampling rates from 128fs to 768fs, where fs is the audio sampling frequency (LRCIN) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

The WM8762 has a master clock detection circuit that automatically determines the relation between the master clock frequency and the sampling rate (to within +/- 8 master clocks). If there is a greater than 8 clocks error, the interface shuts down the DAC and mutes the output. The master clock should be synchronised with LRCIN, although the WM8762 is tolerant of phase differences or jitter on this clock.

SAMPLING RATE (LRCIN)	MASTER CLOCK FREQUENCY (MHZ) (MCLK)					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.114	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 1 Master Clock Frequencies Versus Sampling Rate

If operating in 192fs or 384fs modes, the following conditions must be met, otherwise the WM8762 may behave in an unspecified manner:

1) After reset, ensure that LRCLK and BCLK are provided within 768 MCLK periods of MCLK starting up

2) If switching to 192fs or 384fs modes at any time during operation, reset the WM8762 by recycling the power

DIGITAL FILTER CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband Edge		-3dB		0.487fs		
Passband Ripple		f < 0.444fs			±0.05	dB
Stopband Attenuation		f > 0.555fs	-60			dB

Table 2 Digital Filter Characteristics

DAC FILTER RESPONSES

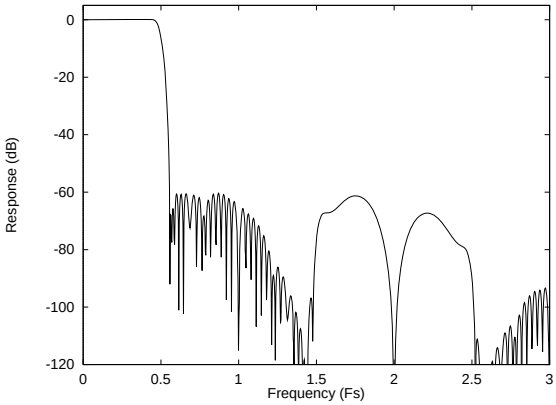


Figure 7 DAC Digital Filter Frequency Response -44.1, 48 and 96kHz

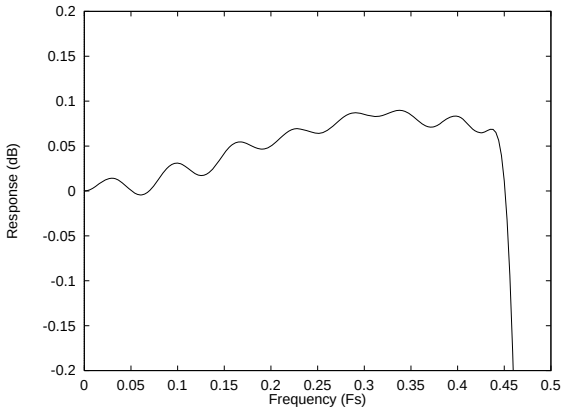


Figure 8 DAC Digital Filter Ripple -44.1, 48 and 96kHz

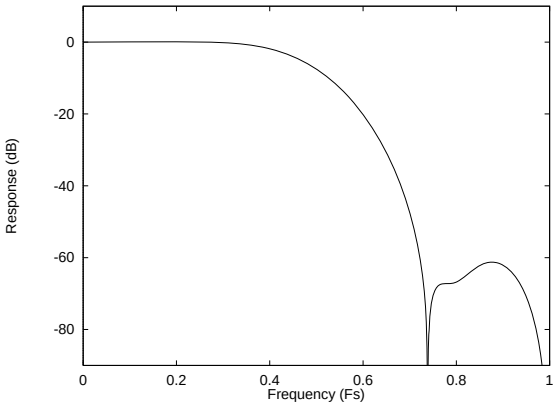


Figure 9 DAC Digital Filter Frequency Response – 192kHz

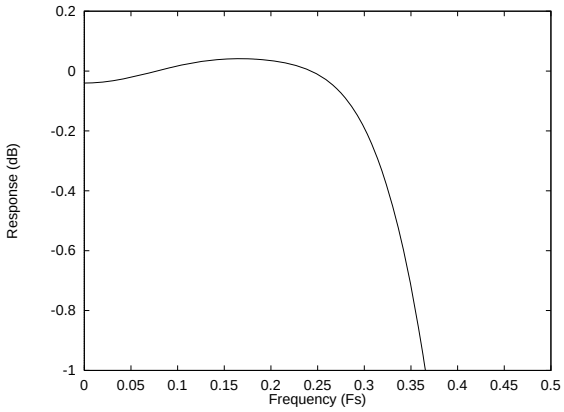


Figure 10 DAC Digital Filter Ripple –192kHz

TYPICAL PERFORMANCE

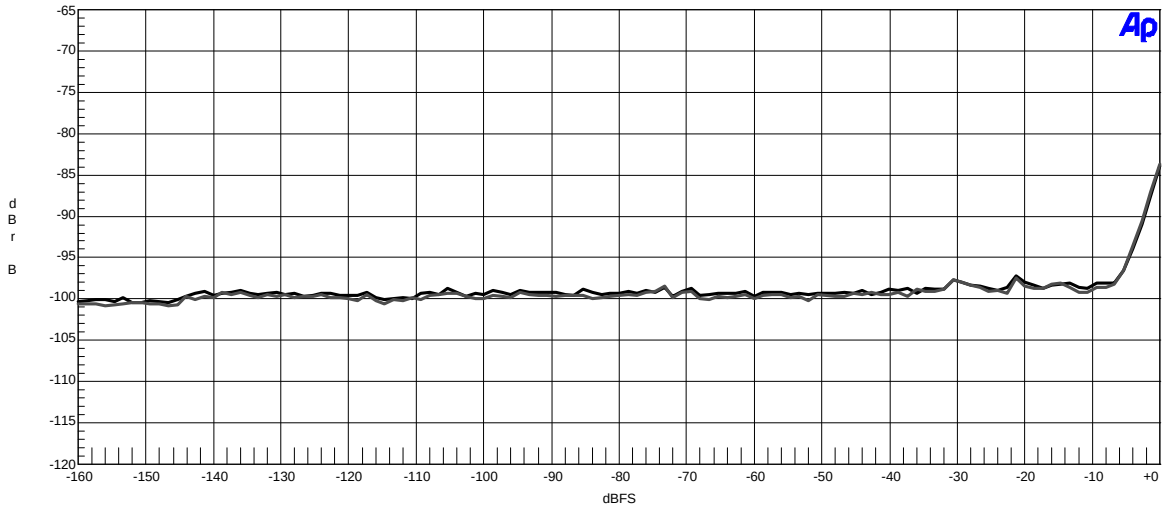


Figure 11 WM8762 Functionality THD+N VDD = 5V

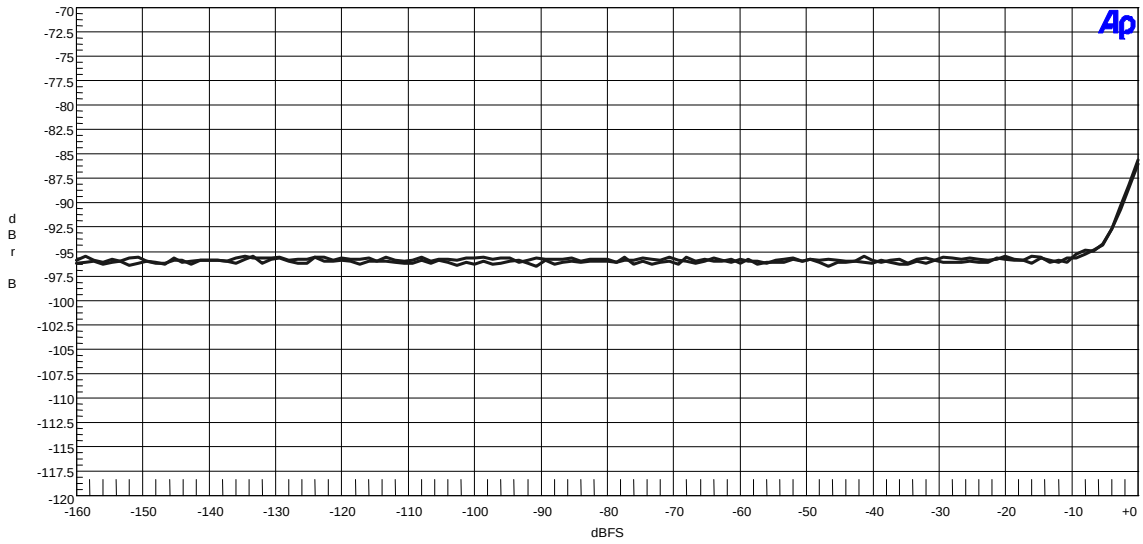
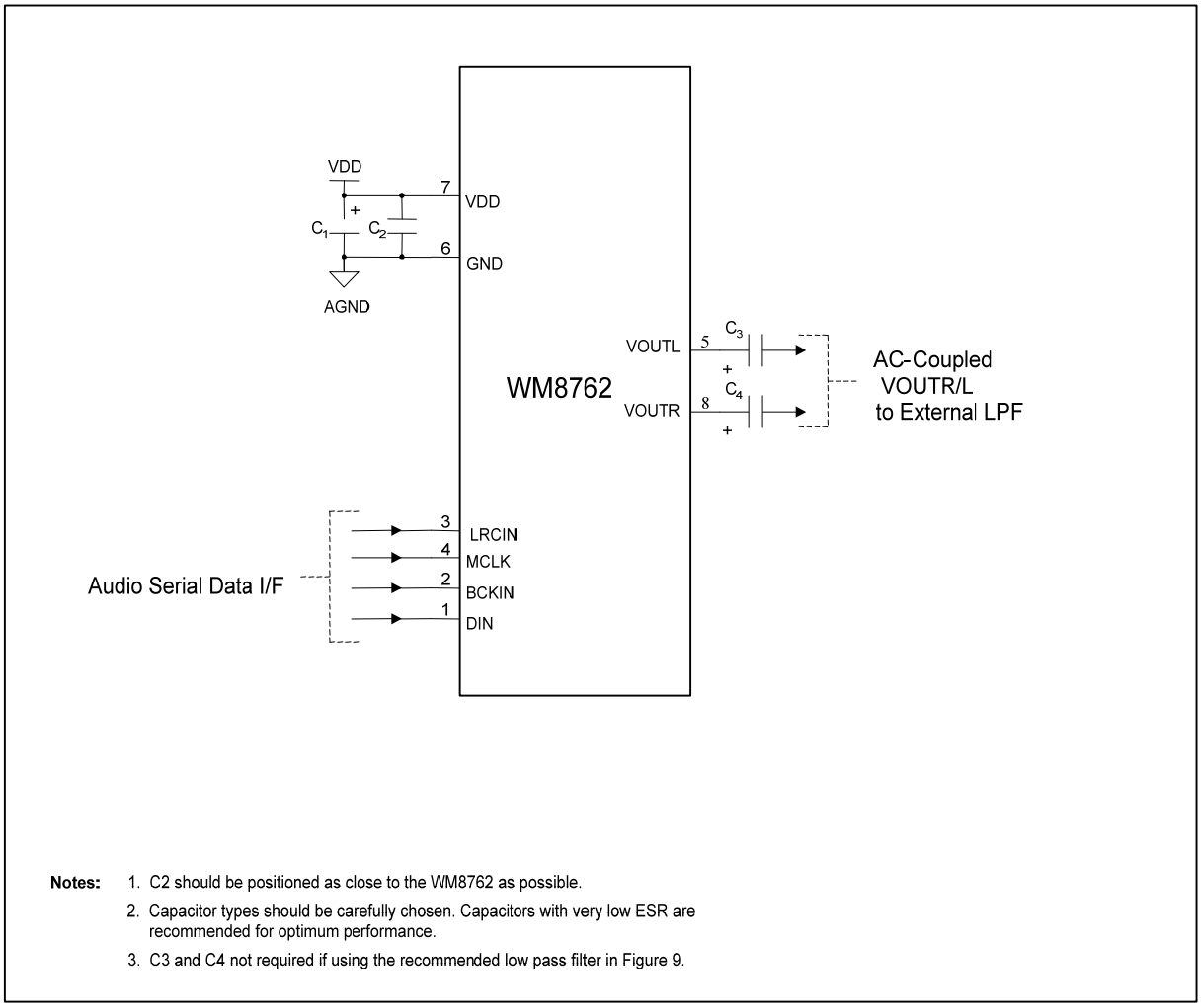


Figure 12 WM8762 Functionality THD+N VDD = 3V

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



Notes:
1. C2 should be positioned as close to the WM8762 as possible.
2. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.
3. C3 and C4 not required if using the recommended low pass filter in Figure 9.

Figure 13 External Component Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	10µF	De-coupling for VDD
C2	0.1µF	De-coupling for VDD
C3 and C4	10µF	Output AC coupling caps to remove midrail DC level from outputs

Table 3 External Components Description

RECOMMENDED ANALOGUE LOW PASS FILTER (OPTIONAL)

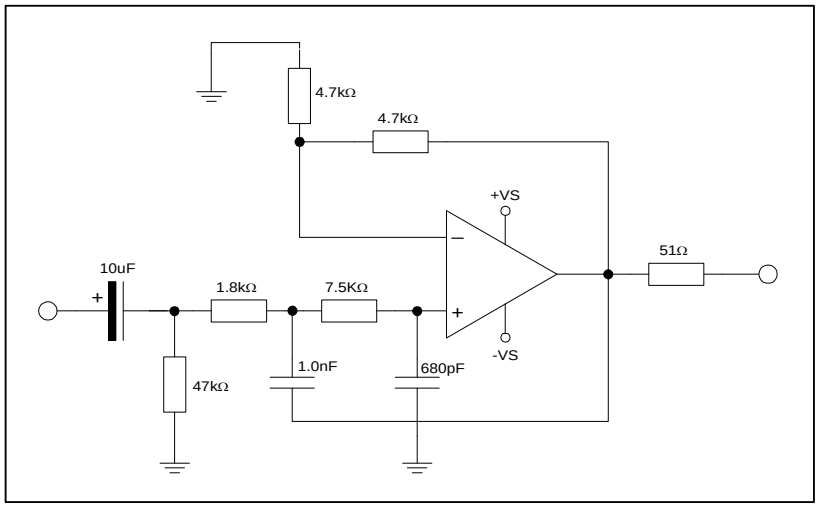


Figure 14 Recommended Low Pass Filter (Optional)

An external low pass filter is recommended (see Figure 20) if the device is driving a wideband amplifier. In some applications, a passive RC filter may be adequate.

PCB LAYOUT RECOMMENDATIONS

Care should be taken in the layout of the PCB that the WM8726 is to be mounted to. The following notes will help in this respect:

1. **The VDD supply to the device should be as noise free as possible.** This can be accomplished to a large degree with a 10uF bulk capacitor placed locally to the device and a 0.1uF high frequency decoupling capacitor placed as close to the VDD pin as possible. It is best to place the 0.1uF capacitor directly between the VDD and GND pins of the device on the same layer to minimize track inductance and thus improve device decoupling effectiveness.

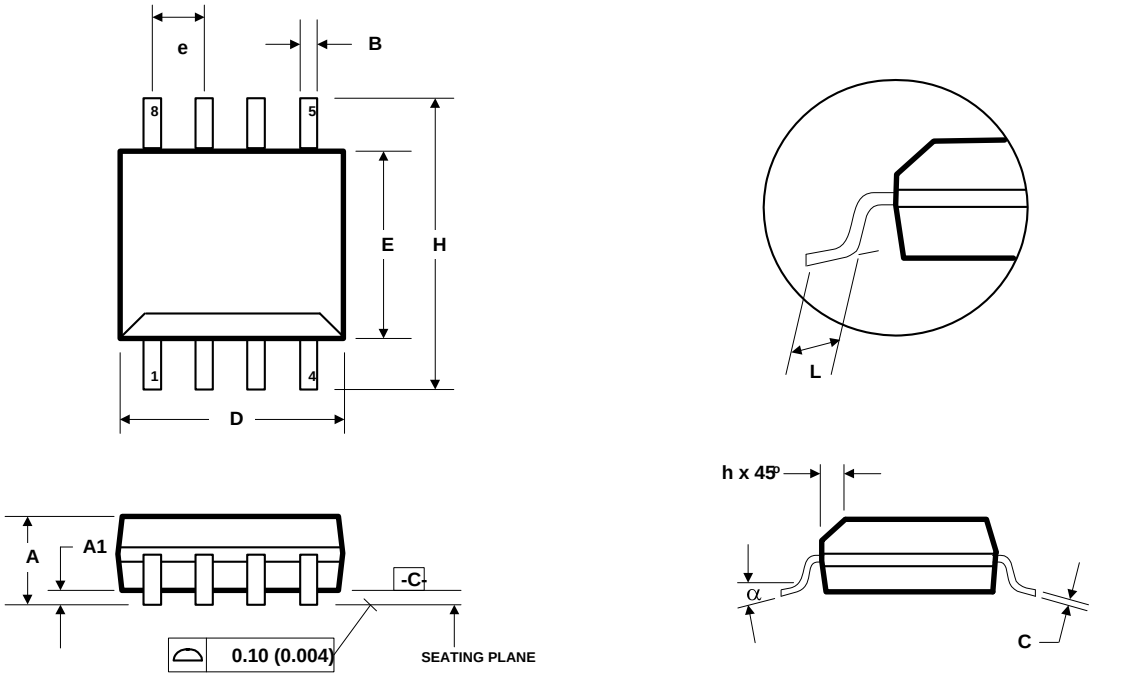
2. **Separate analogue and digital track routing from each other**. The device is split into analogue (pins 5 – 9) and digital (pins 1 – 4 and pins 10 – 14) sections that allow the routing of these signals to be easily separated. By physically separating analogue and digital signals, crosstalk from the PCB can be minimized.

3. **Use an unbroken solid GND plane**. To achieve best performance from the device, it is advisable to have either a GND plane layer on a multilayer PCB or to dedicate one side of a 2 layer PCB to be a GND plane. For double sided implementations it is best to route as many signals as possible on the device mounted side of the board, with the opposite side acting as a GND plane. The use of a GND plane greatly reduces any electrical emissions from the PCB and minimizes crosstalk between signals.

An evaluation board is available for the WM8726 that demonstrates the above techniques and the excellent performance achievable from the device. This can be ordered or the User manual downloaded from the Wolfson web site at www.wolfsonmicro.com

PACKAGE DRAWING

D: 8 PIN SOIC 3.9mm **DM009.B**



Symbols	Dimensions (mm)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.0532	0.0688
A_1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.0130	0.0200
C	0.19	0.25	0.0075	0.0098
D	4.80	5.00	0.1890	0.1968
e	1.27 BSC		0.050 BSC	
E	3.80	4.00	0.1497	0.1574
h	0.25	0.50	0.0099	0.0196
H	5.80	6.20	0.2284	0.2440
L	0.40	1.27	0.0160	0.0500
α	0^o	8^o	0^o	8^o
REF:	JEDEC.95, MS-012			

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
D. MEETS JEDEC.95 MS-012, VARIATION = AA. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
23/12/03	4.0	JMacD	Updated to Production Data Order codes: leadfree and T&R options added, peak soldering temp added p3
29//09/04	4.1	JC	Pin Configuration: Pin 8 changed to VOUTR and Pin 5 changed to VOUTL, p3 Pin Description: changes as above, p3 Recommended External Component Diagram, changes as above, p12
25/07/06	4.2	JMacD	Order Codes – removed leaded codes, p3 Important Notice updated, p15
21/04/08	4.3	ID	Added DAC phase invertion comment – P9 Added POR description and changed POR threshold from 1.8V to 2.4V. to be consistent with other devices. Removed "WIDE BODY" from package information.
04/11/08	4.4	JMacD	Minimum Temp updated from -25 to -40^{o}C, p2, p4
28/06/11	4.5	BT	Added 192fs and 384fs recommended operating conditions to avoid unspecified operation in Audio Data Sampling Rates section, p10 and p11.
26/09/11	4.6	JMacD	Order codes changed from WM8762GED/V and WM8762GED/RV to WM8762CGED and WM8762CGED/R to reflect change to copper wire bonding.
26/09/11	4.6	JMacD	MSL changed from MSL2 to MSL1.