WM8951L

Stereo ADC with Microphone Input and Clock Generator

DESCRIPTION

The WM8951L is a low power stereo ADC with an integrated microphone interface and crystal oscillator for clock generation. The WM8951L is ideal for voice recorders, wireless microphones and games console accessories.

Stereo line and mono microphone level audio inputs are provided, along with a mute function, programmable line level volume control and a bias voltage output suitable for an electret type microphone.

Stereo 24-bit multi-bit sigma delta ADCs are used with oversampling decimation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported.

The device is controlled via a 2 or 3 wire serial interface. The interface provides access to all features including volume controls, mutes and extensive power management facilities. The device is available in a small 28 lead 5x5mm quad flat leadless package (QFN).

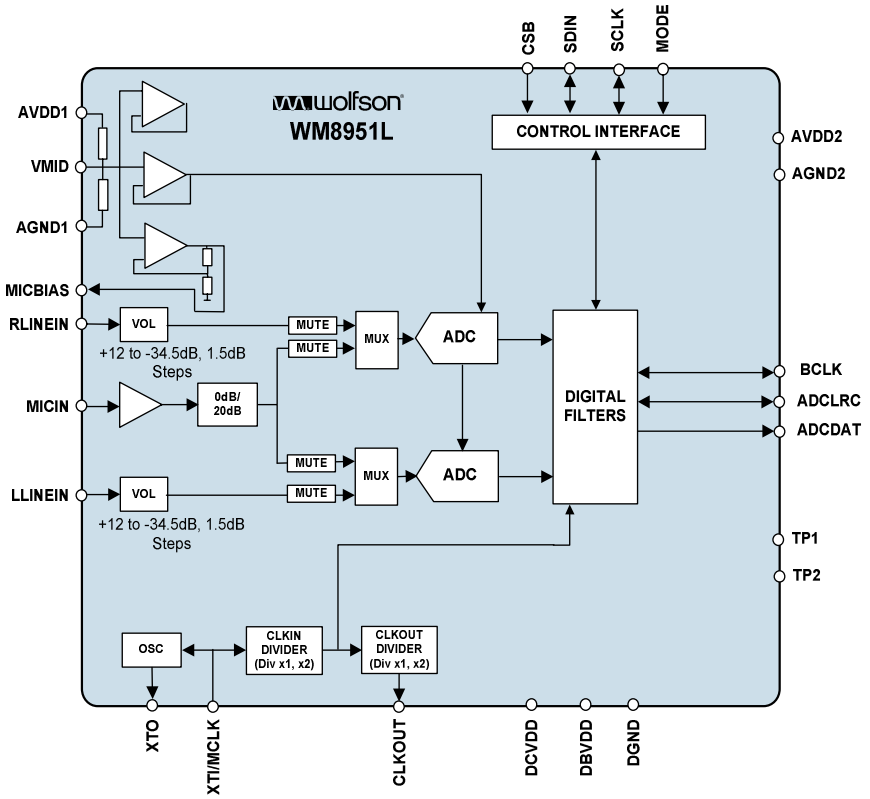
FEATURES

- Audio Performance
  - ADC SNR 90dB ('A' weighted) at 3.3V, 85dB at 1.8V
  - Low Power
  - 1.42 – 3.6V Digital Supply Operation
  - 1.8 – 3.6V Analogue Supply Operation
- Sampling Frequency: 8kHz – 96kHz
- Selectable ADC High Pass Filter
- 2 or 3-Wire MPU Serial Control Interface
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
  - Master or Slave Clocking Mode
- Microphone Input and Electret Bias with Side Tone Mixer
- Available in 5x5mm 28-lead QFN package

APPLICATIONS

- Wireless microphones
- Voice recorders
- Games console accessories

BLOCK DIAGRAM



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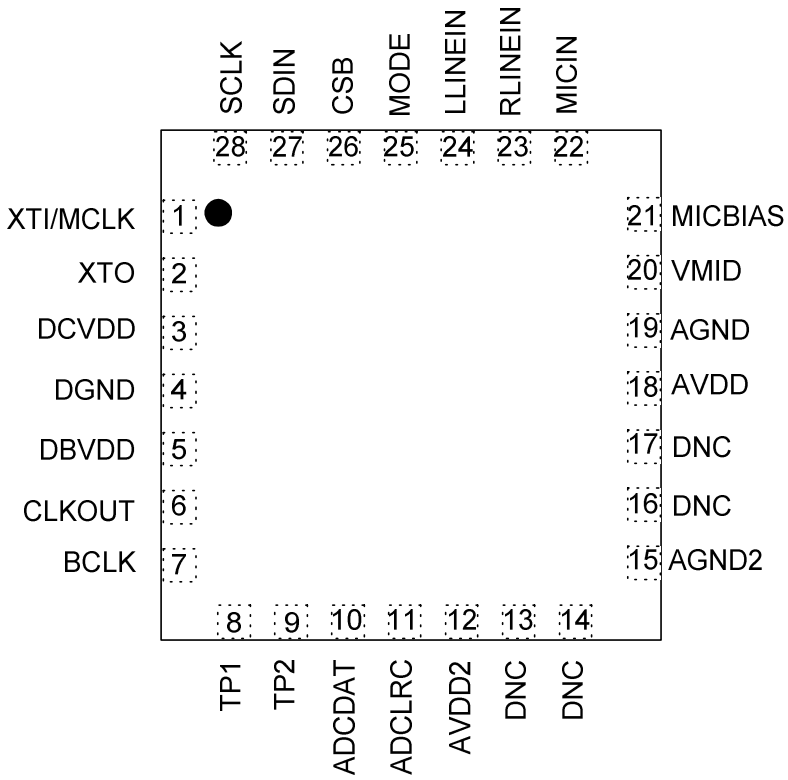
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	AVDD RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8951LGEFL	-25 to +85°C	1.8 to 3.6V	28-lead QFN (lead free)	MSL 1	260°C
WM8951LGEFL/R	-25 to +85°C	1.8 to 3.6V	28-lead QFN (lead free, tape and reel)	MSL 1	260°C

Note:
Reel quantity = 3,500

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	XTI/MCLK	Digital Input	Crystal Input or Master Clock Input (MCLK)
2	XTO	Digital Output	Crystal Output
3	DCVDD	Supply	Digital Core VDD
4	DGND	Ground	Digital GND
5	DBVDD	Supply	Digital Buffers VDD
6	CLKOUT	Digital Output	Buffered Clock Output
7	BCLK	Digital Input/Output	Digital Audio Bit Clock, Pull Down, (see Note 1)
8	TP1	Test Pin	Connect to ground
9	TP2	Test Pin	Connect to ground in slave mode / Leave floating in master mode
10	ADCDAT	Digital Output	ADC Digital Audio Data Output
11	ADCLRC	Digital Input/Output	ADC Sample Rate Left/Right Clock, Pull Down (see Note 1)
12	AVDD2	Supply	Analogue VDD
13	DNC	Do Not Connect	Leave this pin floating
14	DNC	Do Not Connect	Leave this pin floating
15	AGND2	Ground	Analogue GND
16	DNC	Do Not Connect	Leave this pin floating
17	DNC	Do Not Connect	Leave this pin floating
18	AVDD	Supply	Analogue VDD
19	AGND	Ground	Analogue GND
20	VMID	Analogue Output	Mid-rail reference decoupling point
21	MICBIAS	Analogue Output	Electret Microphone Bias
22	MICIN	Analogue Input	Microphone Input (AC coupled)
23	RLINEIN	Analogue Input	Right Channel Line Input (AC coupled)
24	LLINEIN	Analogue Input	Left Channel Line Input (AC coupled)
25	MODE	Digital Input	Control Interface Selection, Pull Up (see Note 1)
26	CSB	Digital Input	3-Wire MPU Chip Select/ 2-Wire MPU interface address selection, active low, Pull up (see Note 1)
27	SDIN	Digital Input/Output	3-Wire MPU Data Input / 2-Wire MPU Data Input
28	SCLK	Digital Input	3-Wire MPU Clock Input / 2-Wire MPU Clock Input

Note:

1. Pull Up/Down only present when Control Register Interface ACTIVE=0 to conserve power.
2. It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+3.63V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND1/AGND2 -0.3V	AVDD1/AVDD2 +0.3V
Operating temperature range, T_A	-25°C	+85°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. The digital supply core voltage (DCVDD) must always be less than or equal to the analogue supply voltage (AVDD1/AVDD2).
3. When DBVDD<2.5V, DCVDD must be at least 0.225V lower than DBVDD.
4. When DBVDD ≥2.5V, DVCVDD must be lower than or equal to DBVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.42	1.5	3.6	V
Digital supply range (Buffer)	DBVDD		1.8		3.6	V
Analogue supply range	AVDD1, AVDD2		1.8		3.6	V
Ground	DGND, AGND1, AGND2			0		V

Notes:

1. USB Mode should not be used with DCVDD lower than 2V

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD1, AVDD2, DBVDD = 3.3V, AGND1, AGND2 = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DBVDD	V
Input HIGH level	V_{IH}		0.7 x DBVDD			V
Output LOW	V_{OL}				0.10 x DBVDD	V
Output HIGH	V_{OH}		0.9 x DBVDD			V
Power On Reset Threshold (DCVDD)						
DCVDD Threshold On -> Off	V_{th}			0.9		V
Hysteresis	V_{IH}			0.3		V
DCVDD Threshold Off -> On	V_{OL}			0.6		V
Analogue Reference Levels						
Reference voltage (VMID)	V_{VMID}			0.5xAVDD		V
Potential divider resistance	R_{VMID}			50k		Ω
Line Input to ADC						
Input Signal Level (0dB)	V_{INLINE}			1.0 AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3) Dynamic Range (Note 3)	SNR DR	AVDD1/2= DBVDD=1.8V DCVDD=1.5V A-weighted, 0dB gain @ fs = 48kHz	75	85		dB dB
		AVDD1/2= DBVDD=1.8V DCVDD=1.5V A-weighted, 0dB gain @ fs = 96kHz		85		
		AVDD1/2= DBVDD=1.8V DCVDD=1.5V A-weighted, -60dB full scale input	80	88		
Total Harmonic Distortion	THD	AVDD1/2= DBVDD=1.8V DCVDD=1.5V -1dB input, 0dB gain		-76	-60	dB
Signal to Noise Ratio (Note 1,3)	SNR	AVDD1/2= DBVDD=1.8V DCVDD=1.5V A-weighted, 0dB gain @ fs = 48kHz	75	85		dB
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp		50		dB
		20Hz to 20kHz, 100mVpp		45		
ADC channel separation		1kHz input		90		dB
Programmable Gain		1kHz input Rsource < 50Ω	-34.5	0	+12	dB
Programmable Gain Step Size		Guaranteed Monotonic		1.5		dB
Mute attenuation		0dB, 1kHz input		80		dB
Input Resistance	R_{INLINE}	0dB gain	20k	30k		Ω
		12dB gain	10k	15k		
Input Capacitance	C_{INLINE}			10		pF

Test Conditions

AVDD1, AVDD2, DBVDD = 3.3V, AGND1, AGND2 = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

Microphone Input to ADC @ 0dB Gain, fs = 48kHz (40kΩ Source Impedance. See Figure 11)						
Input Signal Level (0dB)	V_{INMIC}			1.0 AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR	AVDD1/2= DBVDD=1.8V DCVDD=1.5V A-weighted, 0dB gain		80		dB
Dynamic Range (Note 3)	DR	AVDD1/2= DBVDD=1.8V DCVDD=1.5V A-weighted, -60dB full scale input		70		dB
Total Harmonic Distortion	THD	AVDD1/2= DBVDD=1.8V DCVDD=1.5V 0dB input, 0dB gain		-55		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Programmable Gain Boost	MICBOOST bit set	1kHz input Rsource < 50 Ohms		34		dB
Mic Path gain (MICBOOST gain is additional to this nominal gain)		MICBOOST = 0 Rsource < 50Ω		14		dB
Mute attenuation		0dB, 1kHz input		80		dB
Input Resistance	R_{INMIC}			10k		Ω
Input Capacitance	C_{INMIC}			10		pF
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$		0.75*AVDD1 –100mV	0.75*AVDD1	0.75*AVDD1 + 100mV	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		25		nV/√Hz

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with the input short circuited, measured 'A' weighted over a 20Hz to 20kHz bandwidth using an Audio analyser.
2. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
3. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
4. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

POWER CONSUMPTION

MODE DESCRIPTION	POWEROFF	CLKOUTPD	OSCPD	ADCPD	MICPD	LINEINPD	CURRENT CONSUMPTION TYPICAL				
							AVDD (1.8V)	AVDD2 (1.8V)	DC VDD (1.5V)	DB VDD (1.8V)	UNIT
Record											
Line Record, oscillator enabled	0	0	0	0	1	0	3.9	-	2.4	0.9	mA
Mic Record, oscillator enabled	0	0	0	0	0	1	3.6	-	2.4	0.9	mA
Standby											
Clock stopped	0	1	1	1	1	1	8	-	-	-	µA
Power Down											
Clock stopped	1	1	1	1	1	1	0.2	0.2	0.3	0.2	µA

Table 1 Powerdown Mode Current Consumption Examples

Notes:

1. AVDD, AVDD2, DBVDD = 1.8V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C. Slave Mode, fs = 48kHz, XTI/MCLK = 256fs (12.288MHz).
2. All figures are quiescent, with no signal.
3. All figures are measured with the audio interface in master mode (MS = 1).

MASTER CLOCK TIMING

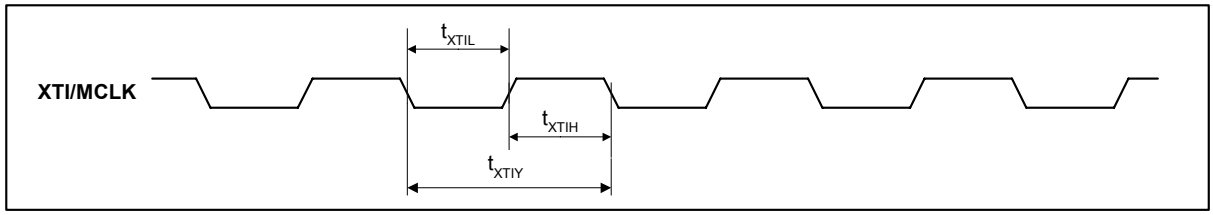


Figure 1 System Clock Timing Requirements

Test Conditions

AVDD1, AVDD2, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
XTI/MCLK System clock pulse width high	t_{XTIH}		18			ns
XTI/MCLK System clock pulse width low	t_{XTIL}		18			ns
XTI/MCLK System clock cycle time	t_{XTIY}		54			ns
XTI/MCLK Duty cycle			40:60		60:40	

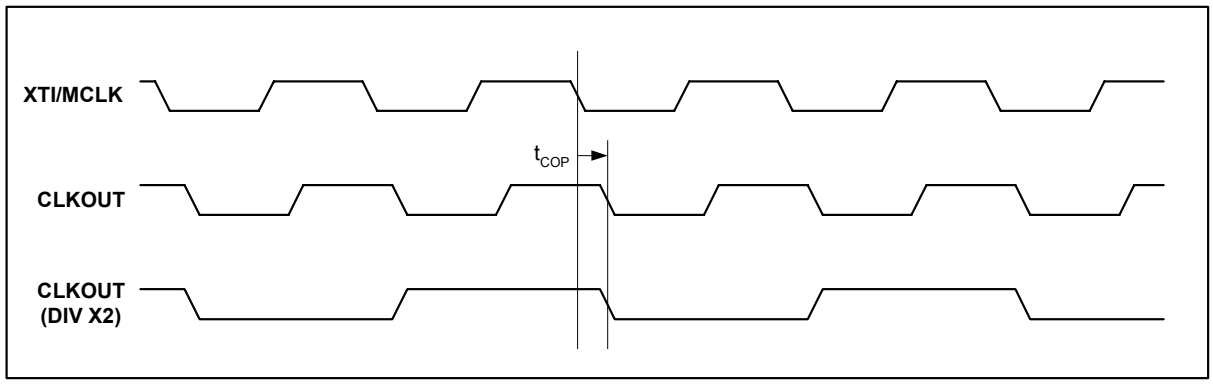


Figure 2 Clock Out Timing Requirements

Test Conditions

AVDD1, AVDD2, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
CLKOUT propagation delay from XTI/MCLK falling edge	t_{COP}		0		10	ns

DIGITAL AUDIO INTERFACE – MASTER MODE

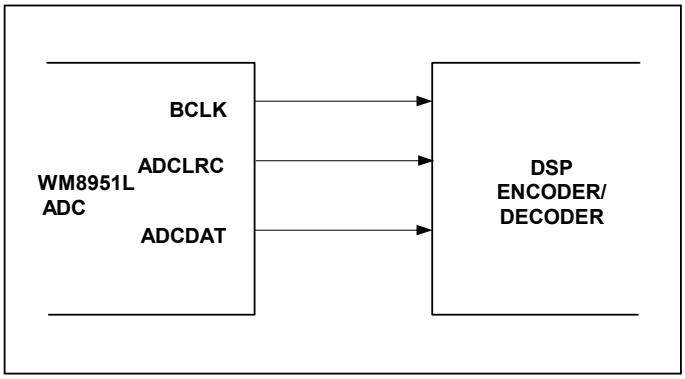


Figure 3 Master Mode Connection

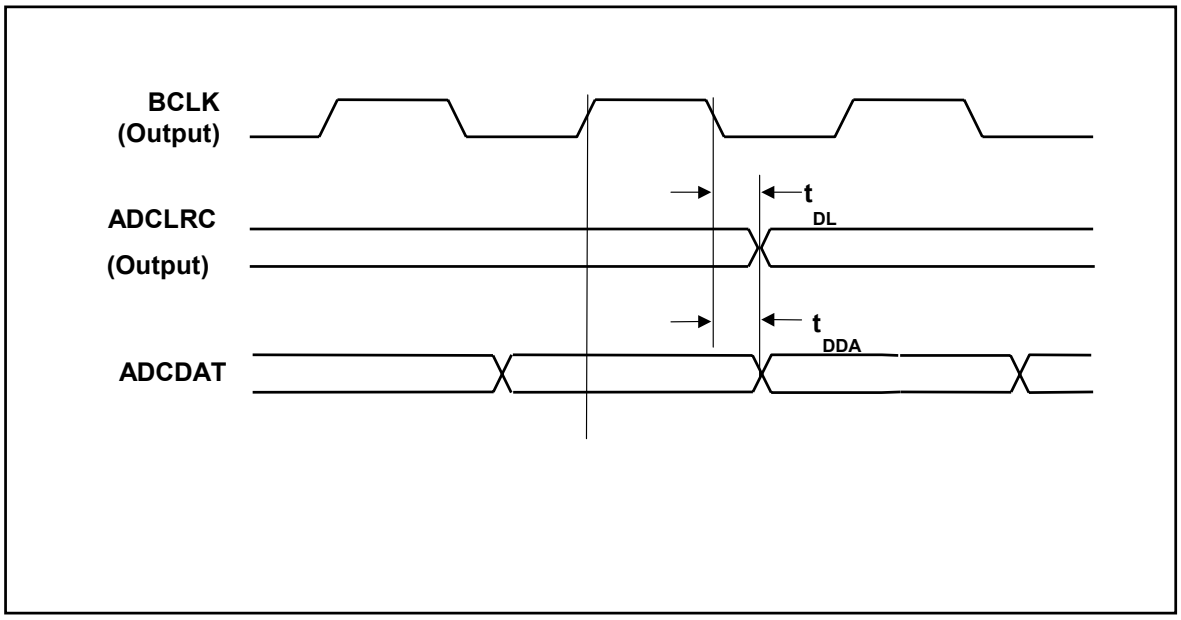


Figure 4 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD1, AVDD2, DBDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADCLRC propagation delay from BCLK falling edge	t_{DL}		0		10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}		0		35	ns

DIGITAL AUDIO INTERFACE – SLAVE MODE

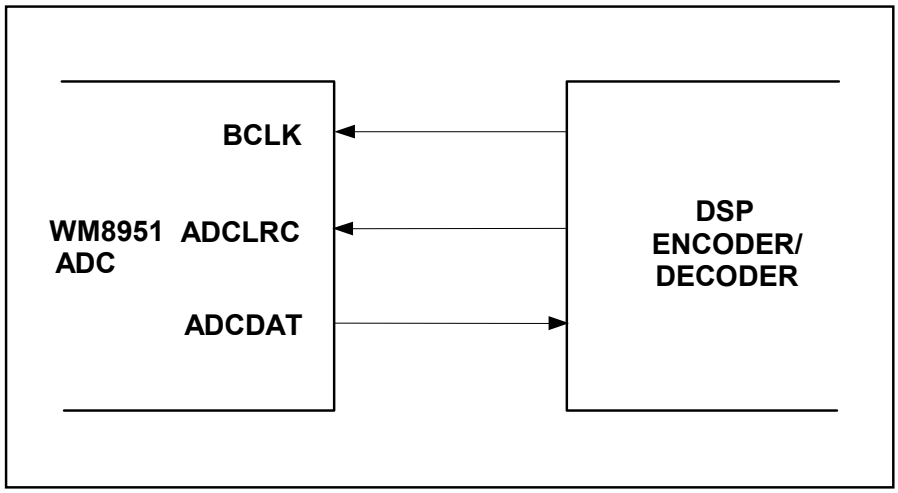


Figure 5 Slave Mode Connection

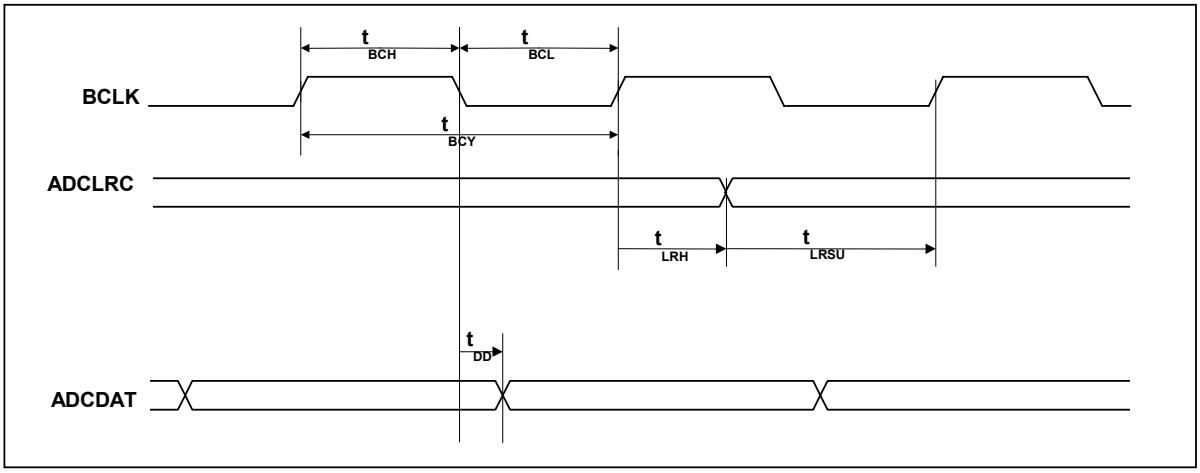


Figure 6 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD1, AVDD2, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
ADCLRC set-up time to BCLK rising edge	t_{LRSU}		10			ns
ADCLRC hold time from BCLK rising edge	t_{LRH}		10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}		0		35	ns

MPU INTERFACE TIMING

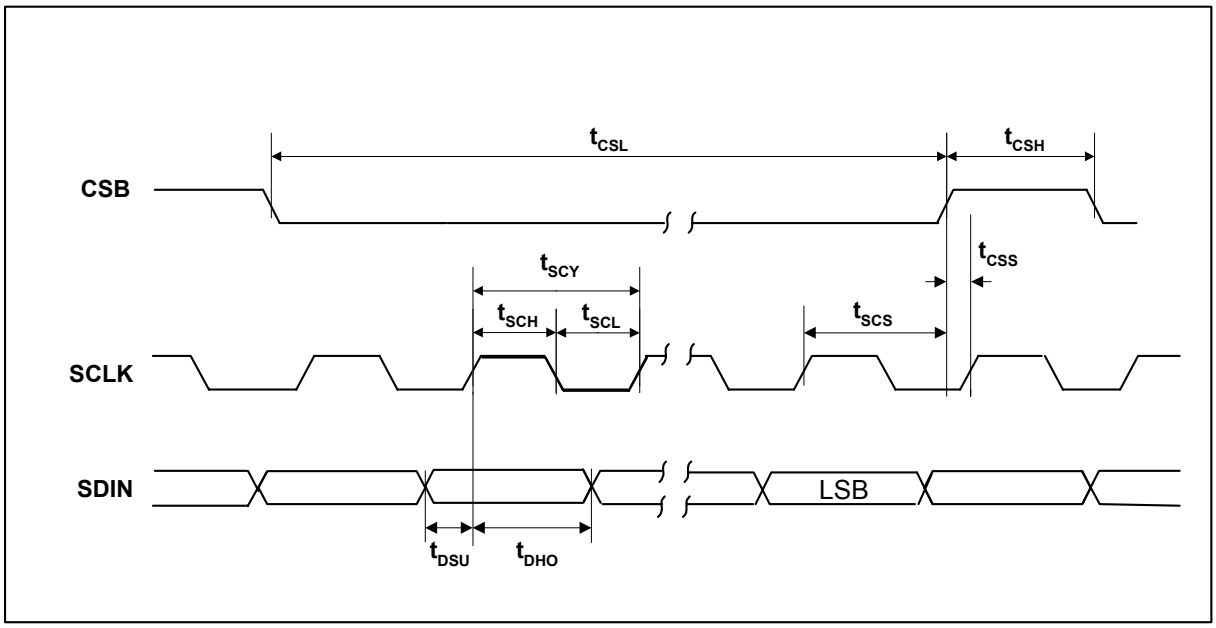


Figure 7 Program Register Input Timing - 3-Wire MPU Serial Control Mode

Test Conditions

AVDD1, AVDD2, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK rising edge to CSB rising edge	t_{SCS}		60			ns
SCLK pulse cycle time	t_{SCY}		80			ns
SCLK pulse width low	t_{SCL}		20			ns
SCLK pulse width high	t_{SCH}		20			ns
SDIN to SCLK set-up time	t_{DSU}		20			ns
SCLK to SDIN hold time	t_{DHO}		20			ns
CSB pulse width low	t_{CSL}		20			ns
CSB pulse width high	t_{CSH}		20			ns
CSB rising to SCLK rising	t_{CSS}		20			ns

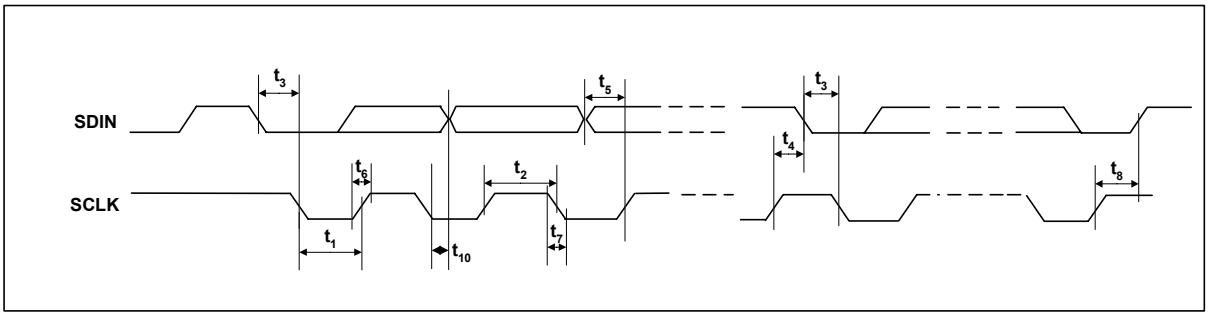


Figure 8 Program Register Input Timing – 2-Wire MPU Serial Control Mode

Test Conditions

AVDD1, AVDD2, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK Frequency			0		526	kHz
SCLK Low Pulsewidth	t_1		1.3			us
SCLK High Pulsewidth	t_2		600			ns
Hold Time (Start Condition)	t_3		600			ns
Setup Time (Start Condition)	t_4		600			ns
Data Setup Time	t_5		100			ns
SDIN, SCLK Rise Time	t_6				300	ns
SDIN, SCLK Fall Time	t_7				300	ns
Setup Time (Stop Condition)	t_8		600			ns
Data Hold Time	t_{10}				900	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8951L is a low power stereo audio ADC designed specifically for portable audio products. It's features, performance and low power consumption make it ideal for portable voice recorders, games console accessories and wireless microphones.

The WM8951L includes line and microphone inputs to the on-board ADC, a crystal oscillator, configurable digital audio interface and a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

The ADC includes three low noise inputs - mono microphone and stereo line. Line inputs have +12dB to -34dB logarithmic volume level adjustments and mute. The Microphone input has -6dB to 34dB volume level adjustment. An electret microphone bias level is also available. All the required input filtering is contained within the device with no external components required.

The on-board stereo analogue to digital converter (ADC) is of a high quality using a multi-bit high-order oversampling architecture delivering optimum performance with low power consumption. The output from the ADC is available on the digital audio interface. The ADC includes an optional digital high pass filter to remove unwanted dc components from the audio signal.

The design of the WM8951L has given much attention to power consumption without compromising performance. It includes the ability to power off selective parts of the circuitry under software control, thus conserving power. Power saving modes be configured under software control including a standby and power off mode.

The device caters for a number of different sampling rates including industry standard 8kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz.

The digitised output is available in a number of audio data formats I^2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified. The digital audio interface can operate in both master or slave modes.

The software control uses either 2 or 3-wire MPU interface.

A crystal oscillator is included on board the device. The device can generate the system master clock or alternatively it can accept an external master clock from the audio system.

AUDIO SIGNAL PATH

LINE INPUTS

The WM8951L provides Left and Right channel line inputs (RLINEIN and LLINEIN). The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external hi-fi or audio equipment.

Both line inputs include independent programmable volume level adjustments and ADC input mute. The scheme is illustrated in Figure 9. Passive RF and active Anti-Alias filters are also incorporated within the line inputs. These prevent high frequencies aliasing into the audio band or otherwise degrading performance.

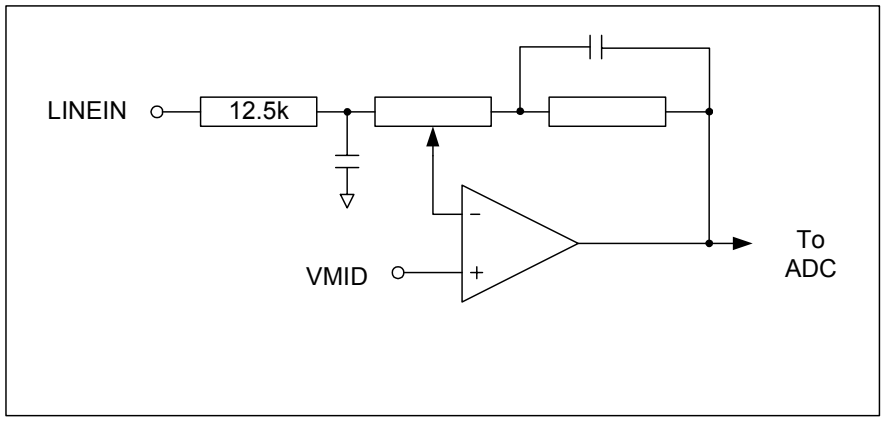


Figure 9 Line Input Schematic

The gain between the line inputs and the ADC is logarithmically adjustable from +12dB to –34.5dB in 1.5dB steps under software control. The ADC Full Scale input is 1.0V rms at AVDD1/2 = 3.3 volts. Any voltage greater than full scale will overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD. The gain is independently adjustable on both Right and Left Line Inputs. However, by setting the INBOTH bit whilst programming the volume control, both channels are simultaneously updated with the same value. Use of INBOTH reduces the required number of software writes required. The line inputs to the ADC can be muted in the analogue domain under software control. The software control registers are shown Table 2. Note that the Line Input Mute only mutes the input to the ADC, this will still allow the Line Input signal to pass to the line output in Bypass Mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000000 Left Line In	4:0	LINVOL[4:0]	10111 (0dB)	Left Channel Line Input Volume Control 11111 = +12dB . . 1.5dB steps down to 00000 = -34.5dB
	7	LINMUTE	1	Left Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	LRINBOTH	0	Left to Right Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of LINVOL[4:0] and LINMUTE to RINVOL[4:0] and RINMUTE 0 = Disable Simultaneous Load
0000001 Right Line In	4:0	RINVOL[4:0]	10111 (0dB)	Right Channel Line Input Volume Control 11111 = +12dB . .1.5dB steps down to 00000 = -34.5dB
	7	RINMUTE	1	Right Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	RLINBOTH	0	Right to Left Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of RINVOL[4:0] and RINMUTE to LINVOL[4:0] and LINMUTE 0 = Disable Simultaneous Load

Table 2 Line Input Software Control

The line inputs are biased internally through the operational amplifier to VMID. Whenever the line inputs are muted or the device placed into standby mode, the line inputs are kept biased to VMID using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when re-activating the inputs.

The external components required to complete the line input application is shown in the Figure 10.

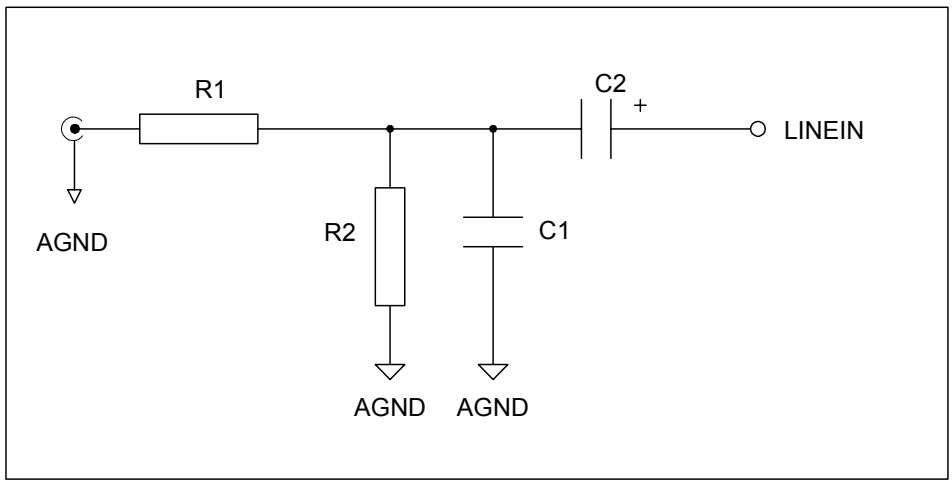


Figure 10 Line Input Application Drawing

For interfacing to a typical CD system, it is recommended that the input is scaled to ensure that there is no clipping of the signal. R1 = 5.6k, R2 = 5.6k, C1 = 220pF, C2 = 1µF.

R1 and R2 form a resistive divider to attenuate the 2 Vrms output from a CD player to a 1 Vrms level, so avoiding overloading the inputs. R2 also provides a discharge path for C2, thus preventing the input to C2 charging to an excessive voltage which may otherwise damage any equipment connected that is not suitably protected against high voltages. C1 forms an RF low pass filter for increasing the rejection of RF interference picked up on any cables. C2 forms a DC blocking capacitor to remove the DC path between the WM8951L and the driving audio equipment. C2 together with the input impedance of the WM8951L form a high pass filter.

MICROPHONE INPUT

MICIN is a high impedance, low capacitance input suitable for connection to a wide range of monophonic microphones of different dynamics and sensitivities.

The MICIN includes programmable volume adjustments and a mute function. The scheme is shown in Figure 11. Passive RF and active Anti-Alias filters are also incorporated within the microphone inputs. These allow a matched interface to the multi-bit oversampling ADC and preventing high frequencies aliasing into the audio band or otherwise degrading performance.

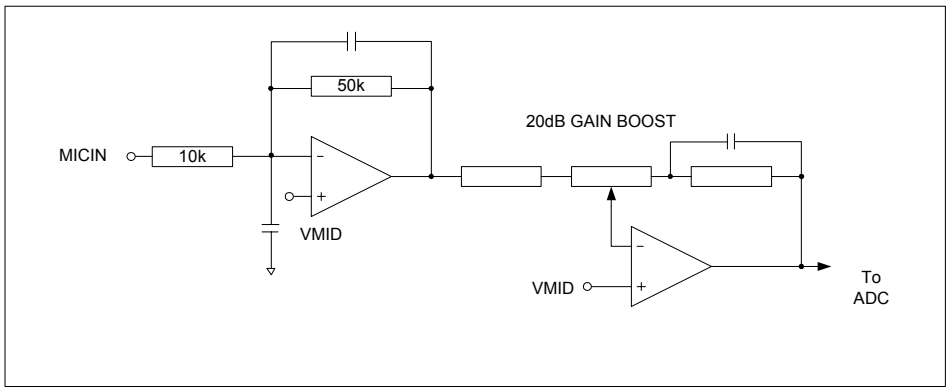


Figure 11 Microphone Input Schematic

There are 2 stages of gain made up of two low noise inverting operational amplifiers.

The 1st stage comprises a nominal gain of G1 = 50k/10k = 5. By adding an external resistor (Rmic) in series with MICIN the gain of stage can be adjusted. For example adding Rmic = 40K sets the gain of stage 1 to x1 (0dB). The equation below can be used to calculate the gain versus Rmic.

$$G1 = 50k/ (Rmic + 10k)$$

Or alternatively to calculate the value of Rmic to achieve a given gain, G1.

$$Rmic = (50k/G1) – 10k$$

The internal 50k and 10k resistors have a tolerance of 15%. For Rmicext = 90k G = 0.5 (-6dB) and for Rmicext = 0 G = x10 (14dB).

The 2nd stage comprises a 0dB gain stage that can be software configured to provide a fixed 20dB of gain for low sensitivity microphones.

The microphone input can therefore be configured with a variable gain of between -6dB and 14dB on the 1st stage, and an additional fixed 0dB or 20dB on the 2nd stage. This allows for all gains to the input signal in the range –6dB to 34dB to be catered for.

The ADC Full Scale input is 1.0V rms at AVDD1/2 = 3.3 volts. Any voltage greater than full scale will overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD1/2. Stage 1 and Stage 2 gains should be configured so that the ADC receives a maximum signal equal to its full scale for maximising the signal to noise.

The software control for the MICIN is shown in Table 3. Note that the Microphone Mute only mutes the input to the ADC, this will still allow the Microphone Input signal to pass to the line output in Sidetone Mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000100 Analogue Audio Path Control	0	MICBOOST	0	Microphone Input Level Boost 1 = Enable Boost 0 = Disable Boost
	1	MUTEMIC	1	Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute

Table 3 Microphone Input Software Control

The microphone input is biased internally through the operational amplifier to VMID. Whenever the line inputs are muted the MICIN input is kept biased to VMID using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when re-activating the input.

The application drawing for the microphone is shown in Figure 12.

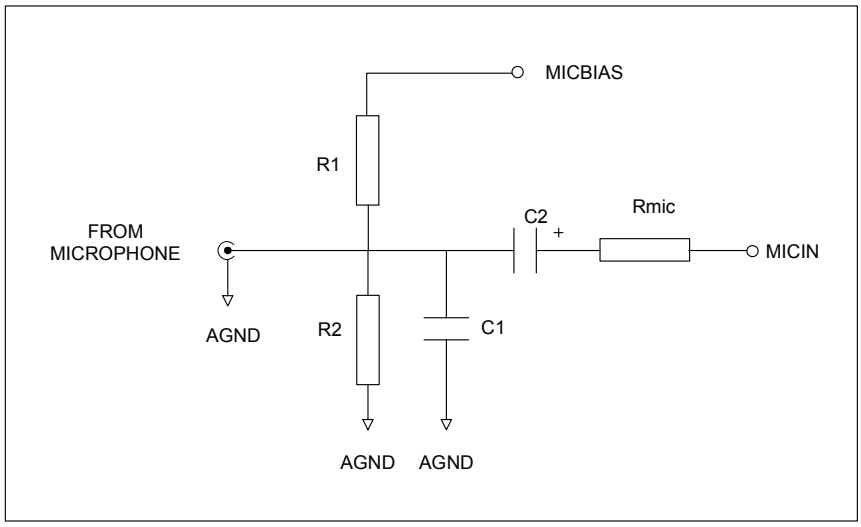


Figure 12 Microphone Input and Bias Application Drawing

Recommended component values are C1 = 220pF (npo ceramic), C2 = 1µF, R1 = 680 ohms, R2 = 47k. Rmic values depends on gain setting (see above).

R1 and R2 form part of the biasing network (refer to Microphone Bias section below). R1 connected to MICBIAS is necessary only for electret type microphones that require a voltage bias. R2 should always be present to prevent the microphone input from charging to a high voltage which may damage the microphone on connection. R1 and R2 should be large so as not to attenuate the signal from the microphone, which can have source impedance greater than 2k. C1 together with the source impedance of the microphone and the input impedance of MICIN forms an RF filter. C2 is a DC blocking capacitor to allow the microphone to be biased at a different DC voltage to the MICIN signal.

MICROPHONE BIAS

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Microphone Input section for an application drawing and further description.

The scheme for MICBIAS is shown in Figure 13. Note that there is a maximum source current capability of 3mA available for the MICBIAS. This limits the smallest value of external biasing resistors that can safely be used.

Note that the MICBIAS output is not active in standby mode.

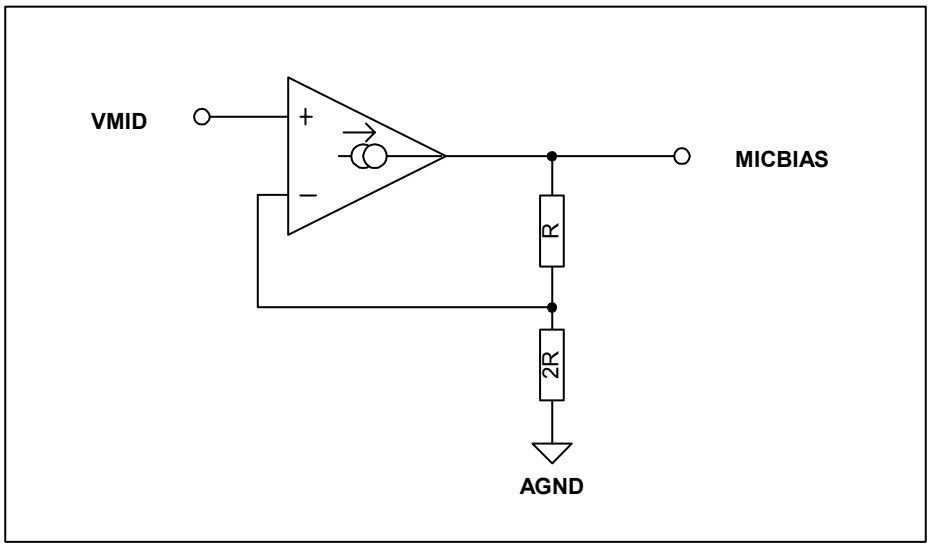


Figure 13 Microphone Bias Schematic

ADC

The WM8951L uses a multi-bit oversampled sigma-delta ADC. A single channel of the ADC is illustrated in the Figure 14.

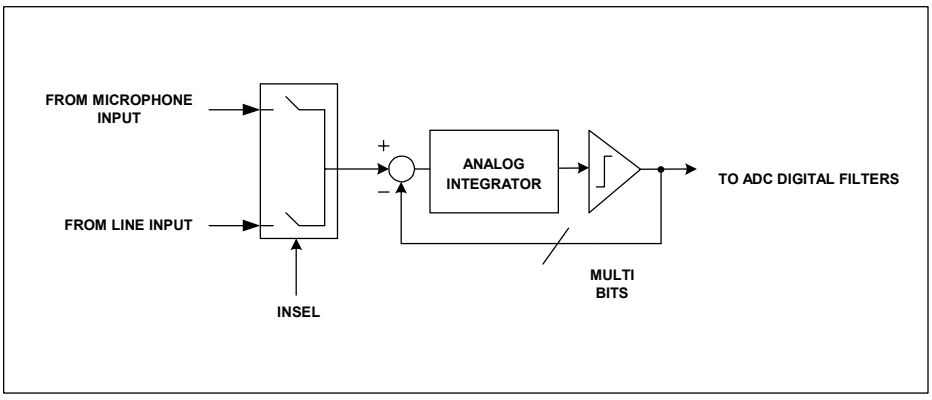


Figure 14 Multi-Bit Oversampling Sigma Delta ADC Schematic

The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise.

The ADC Full Scale input is 1.0V rms at AVDD = 3.3 volts. Any voltage greater than full scale will overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD1/2.

The device employs a pair of ADCs. The input can be selected from either the Line Inputs or the Microphone input under software control. The two channels cannot be selected independently. The control is shown in Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000100 Analogue Audio Path Control	2	INSEL	0	Microphone/Line Input Select to ADC 1 = Microphone Input Select to ADC 0 = Line Input Select to ADC

Table 4 ADC Software Control

The digital data from the ADC is fed for signal processing to the ADC Filters.

ADC FILTERS

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. Figure 15 illustrates the digital filter path.

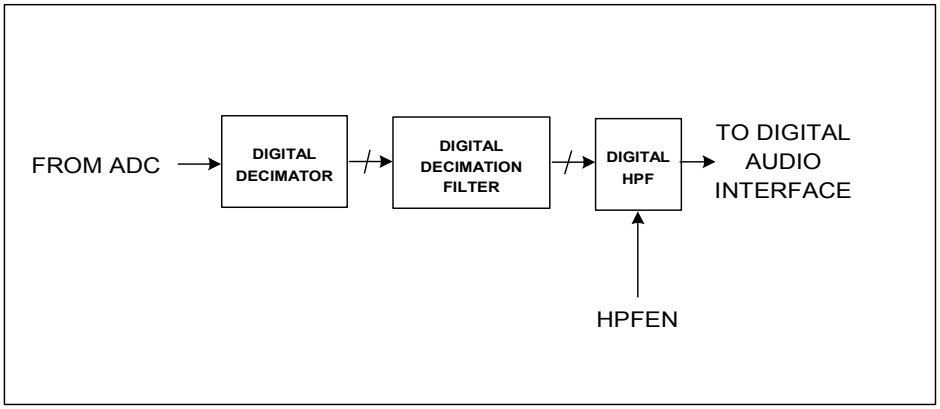


Figure 15 ADC Digital Filter

The ADC digital filters contain a digital high pass filter, selectable via software control. The high-pass filter response detailed in Digital Filter Characteristics. When the high-pass filter is enabled the dc offset is continuously calculated and subtracted from the input signal. By setting HPOR the last calculated dc offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal. If the dc offset changes, the stored and subtracted value will not change unless the high-pass filter is enabled. The software control is shown in Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000101 Digital Audio Path Control	0	ADCHPD	0	ADC High Pass Filter Enable (Digital) 1 = Disable High Pass Filter 0 = Enable High Pass Filter
	4	HPOR	0	Store dc offset when High Pass Filter disabled 1 = store offset 0 = clear offset

Table 5 ADC Software Control

There are several types of ADC filters, frequency and phase responses of these are shown in Digital Filter Characteristics. The filter types are automatically configured depending on the sample rate chosen. Refer to the sample rate section for more details.

DEVICE OPERATION

DEVICE RESETTING

The WM8951L contains a power on reset circuit that resets the internal state of the device to a known condition. The power on reset is applied as DCVDD powers on and released only after the voltage level of DCVDD crosses a minimum turn off threshold. If DCVDD later falls below a minimum turn on threshold voltage then the power on reset is re-applied. The threshold voltages and associated hysteresis are shown in the Electrical Characteristics table.

The user also has the ability to reset the device to a known state under software control as shown in the table below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001111 Reset Register	8:0	RESET	not reset	Reset Register Writing 00000000 to register resets device

Table 6 Software Control of Reset

When using the software reset. In 3-wire mode the reset is applied on the rising edge of CSB and released on the next rising edge of SCLK. In 2-wire mode the reset is applied for the duration of the ACK signal (approximately 1 SCLK period, refer to Figure 24).

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. To allow WM8951L to be used in a centrally clocked system, the WM8951L is capable of either generating this system clock itself or receiving it from an external source as will be discussed.

For applications where it is desirable that the WM8951L is the system clock source, then clock generation is achieved through the use of a suitable crystal connected between the XTI/MCLK input and XTO output pins (see CRYSTAL OSCILLATOR section).

For applications where a component other than the WM8951L will generate the reference clock, the external system can be applied directly through the XTI/MCLK input pin with no software configuration necessary. Note that in this situation, the oscillator circuit of the WM8951L can be safely powered down to conserve power (see POWER DOWN section).

CORE CLOCK

The WM8951L DSP core can be clocked either by MCLK or MCLK divided by 2. This is controlled by software as shown in Table 7 below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001000 Sampling Control	6	CLKIDIV2	0	Core Clock divider select 1 = Core Clock is MCLK divided by 2 0 = Core Clock is MCLK

Table 7 Software Control of Core Clock

Having a programmable MCLK divider allows the device to be used in applications where higher frequency master Clocks are available. For example the device can support 512fs master clocks whilst fundamentally operating in a 256fs mode.

CRYSTAL OSCILLATOR

The WM8951L includes a crystal oscillator circuit that allows the audio system's reference clock to be generated on the device. This is available to the rest of the audio system in buffered form on CLKOUT. The crystal oscillator is a low radiation type, designed for low EMI. A typical application circuit is shown in Figure 16.

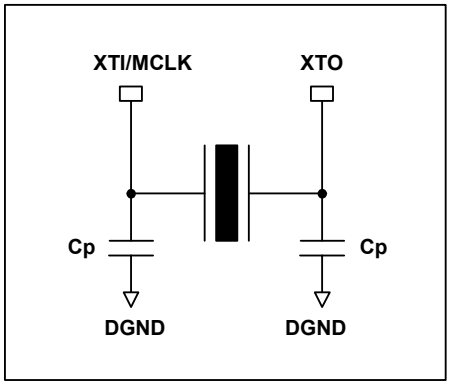


Figure 16 Crystal Oscillator Application Circuit

The WM8951L crystal oscillator provides an extremely low jitter clock source. Low jitter clocks are a requirement for high quality audio ADCs, regardless of the converter architecture. The WM8951L architecture is less susceptible than most converter techniques but still requires clocks with less than approximately 1ns of jitter to maintain performance. In applications where there is more than one source for the master clock, it is recommended that the clock is generated by the WM8951L to minimise such problems.

CLOCKOUT

The Core Clock is internally buffered and made available externally to the audio system on the CLKOUT output pin. CLKOUT provides a replication of the Core Clock, but buffered as suitable for driving external loads.

There is no phase inversion between XTI/MCLK, the Core Clock and CLOCKOUT but there will inevitably be some delay. The delay will be dependent on the load that CLOCKOUT drives. Refer to Electrical Characteristics.

CLKOUT can also be divided by 2 under software control, refer to Table 8. Note that if CLKOUT is not required then the CLKOUT buffer on the WM8951L can be safely powered down to conserve power (see POWER DOWN section). If the system architect has the choice between using $F_{CLKOUT} = F_{MCLK}$ or $F_{CLKOUT} = F_{MCLK}/2$ in the interface, the latter is recommended to conserve power. When the divide by two is selected CLKOUT changes on the rising edge of MCLK. Please refer to Electrical Characteristics for timing information.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001000 Sampling Control	7	CLKODIV2	0	CLKOUT divider select 1 = CLOCKOUT is Core Clock divided by 2 0 = CLOCKOUT is Core Clock

Table 8 Programming CLKOUT

CLKOUT is disabled and set low whenever the device is in reset.

DIGITAL AUDIO INTERFACES

WM8951L may be operated in either one of the 4 offered audio interface modes. These are:

- Right justified
- Left justified
- I^2S
- DSP mode

All four of these modes are MSB first and operate with data 16 to 32 bits.

Note that 32 bit data is not supported in right justified mode.

The digital audio interface takes the data from the internal ADC digital filter and places it on the ADCDAT output. ADCDAT is the formatted digital audio data stream output from the ADC digital filters with left and right channels multiplexed together. ADCLRC is an alignment clock that controls whether Left or Right channel data is present on the ADCDAT lines. ADCDAT and ADCLRC are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. BCLK maybe an input or an output dependent on whether the device is in master or slave mode. Refer to the MASTER/SLAVE OPERATION section

There are four digital audio interface formats accommodated by the WM8951L. These are shown in the figures below. Refer to the Electrical Characteristic section for timing information.

Left Justified mode is where the MSB is available on the first rising edge of BCLK following a ADCLR transition.

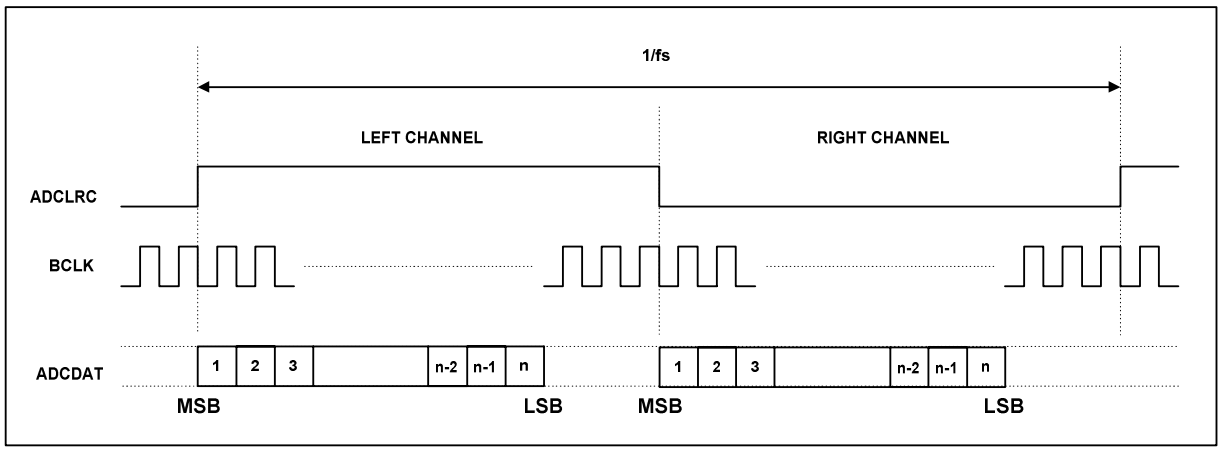


Figure 17 Left Justified Mode

I^2S mode is where the MSB is available on the 2nd rising edge of BCLK following an ADCLRC transition.

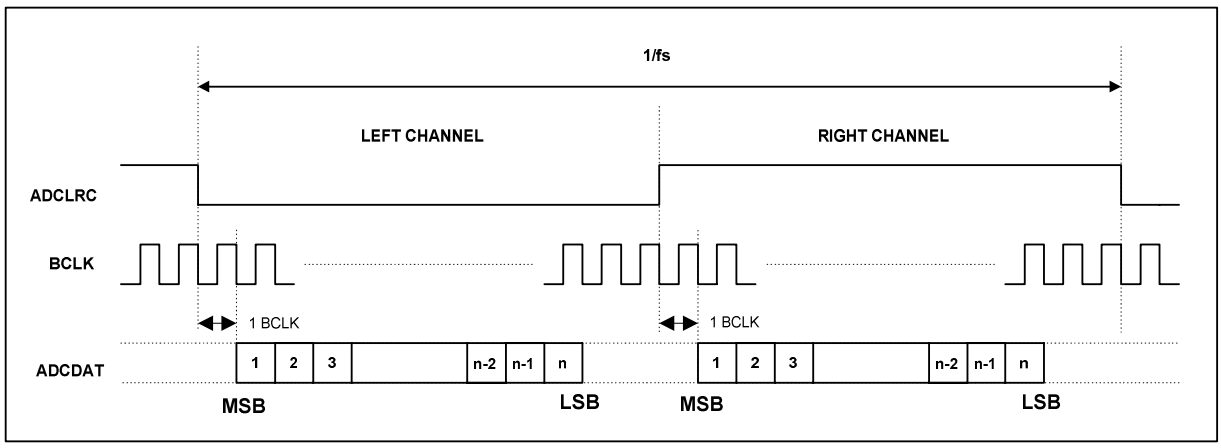


Figure 18 I^2S Mode

Right Justified mode is where the LSB is available on the rising edge of BCLK preceding a ADCLRC transition, yet MSB is still transmitted first.

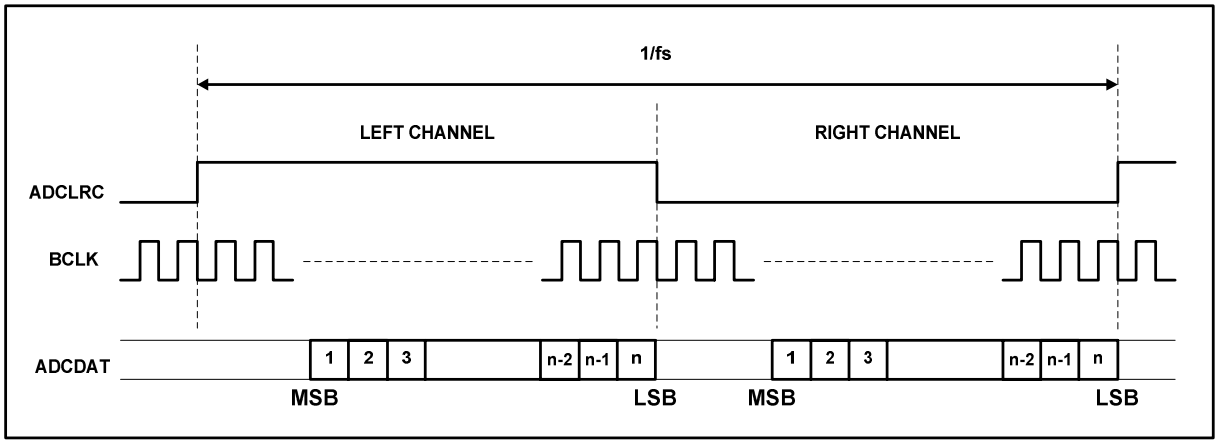


Figure 19 Right Justified Mode

DSP mode is where the left channel MSB is available on either the 1st or 2nd rising edge of BCLK (selectable by LRP) following a LRC transition high. Right channel data immediately follows left channel data.

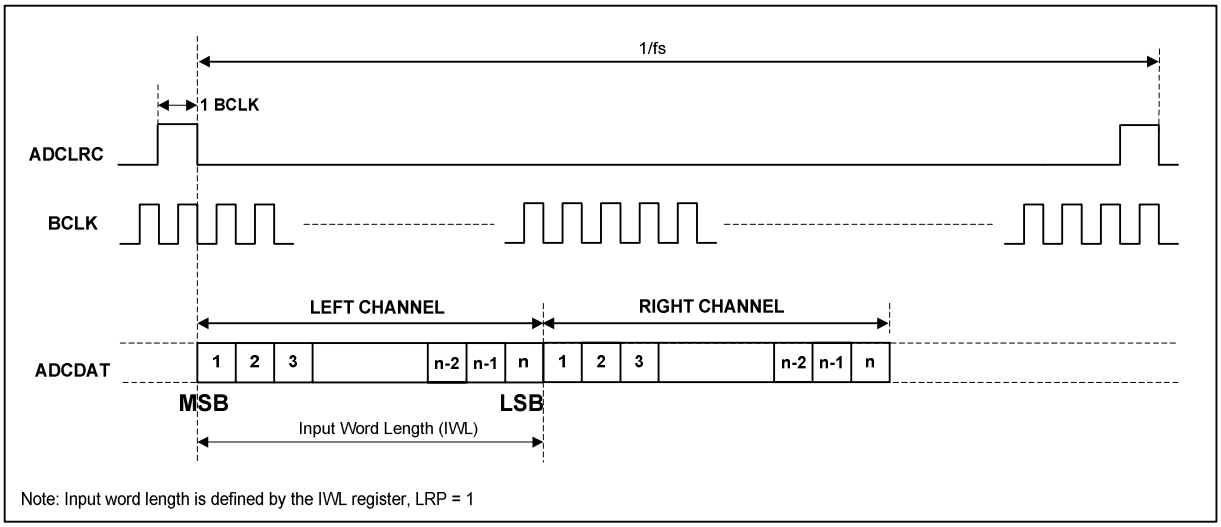


Figure 20 DSP Mode

In all modes ADCLRC must always change on the falling edge of BCLK, refer to Figure 17, Figure 18, Figure 19 and Figure 20.

Operating the digital audio interface in DSP mode allows ease of use for supporting the various sample rates and word lengths. The only requirement is that all data is transferred within the correct number of BCLK cycles to suit the chosen word length.

In order for the digital audio interface to offer similar support in the three other modes (Left Justified, I^2S and Right Justified), the ADCLRC and BCLK frequencies, continuity and mark-space ratios need more careful consideration.

In Slave mode, ADCLRC is not required to have a 50:50 mark-space ratio. BCLK input need not be continuous. It is however required that there are sufficient BCLK cycles for each ADCLRC transition to clock the chosen data word length. The non-50:50 requirement on the LRC is of use in some situations such as with a USB 12MHZ clock. Here simply dividing down a 12MHz clock within the DSP to generate LRC and BCLK will not generate the appropriate ADCLRC since it will no longer change on the falling edge of BCLK. For example, with 12MHz/32k fs mode there are 375 MCLK per LRC. In these situations ADCLRC can be made non 50:50.

In Master mode, ADCLRC will be output with a 50:50 mark-space ratio with BCLK output at 64 x base frequency (i.e. 48 kHz).

The ADC digital audio interface modes are software configurable as indicated in Table 8. Note that dynamically changing the software format may result in erroneous operation of the interfaces and is therefore not recommended.

The length of the digital audio data is programmable at 16/20/24 or 32 bits, in I2S or left justified modes only. Refer to the software control table below. The data is signed 2's complement. The ADC digital filters process data using 24 bits. If the ADC is programmed to output 16 or 20 bit data then it strips the LSBs from the 24 bit data. If the ADC is programmed to output 32 bits then it packs the LSBs with zeros.

To accommodate system timing requirements the interpretation of BCLK maybe inverted, this is controlled vias the software shown in Table 9. This is especially appropriate for DSP mode.

ADCDAT lines are always outputs. They power up and return from standby low.

ADCLRC and BCLK can be either outputs or inputs depending on whether the device is configured as a master or slave. If the device is a master then BCLK is an output that defaults low. If the device is a slave then BCLK is an input. It is expected that these are set low by the audio interface controller when the WM8951L is powered off or in standby.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000111 Digital Audio Interface Format	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode, frame sync + 2 data packed words 10 = I^2S Format, MSB-First left-1 justified 01 = MSB-First, left justified 00 = MSB-First, right justified
	3:2	IWL[1:0]	10	Input Audio Data Bit Length Select 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	7	BCLKINV	0	Bit Clock Invert 1 = Invert BCLK 0 = Don't invert BCLK

Table 9 Digital Audio Interface Control

Note: If right justified 32 bit mode is selected then the WM8951L defaults to 24 bits.

MASTER AND SLAVE MODE OPERATION

The WM8951L can be configured as either a master or slave mode device. As a master mode device the WM8951L controls sequencing of the data and clocks on the digital audio interface. As a slave device the WM8951L responds with data to the clocks it receives over the digital audio interface. The mode is set with the MS bit of the control register as shown in Table 10.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000111 Digital Audio Interface Format	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode

Table 10 Programming Master/Slave Modes

As a master mode device the WM8951L controls the sequencing of data transfer (ADCDAT) and output of clocks (BCLK, ADCLRC) over the digital audio interface. It uses the timing generated from either its on-board crystal or the MCLK input as the reference for the clock and data transitions. This is illustrated in Figure 21. ADCDAT is always an output from the WM8951L independent of master or slave mode.

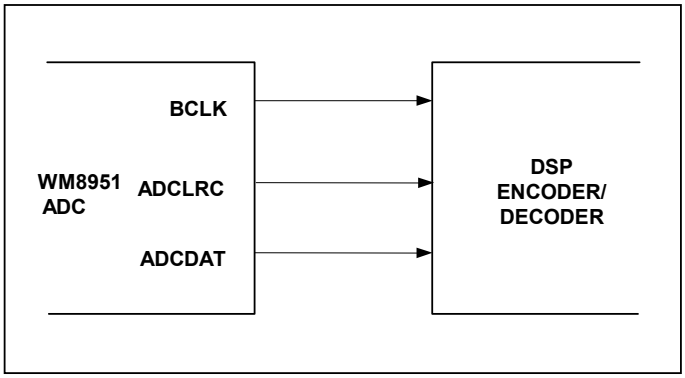


Figure 21 Master Mode

As a slave device the WM8951L sequences the data transfer (ADCDAT) over the digital audio interface in response to the external applied clocks (BCLK, ADCLRC). This is illustrated in Figure 22.

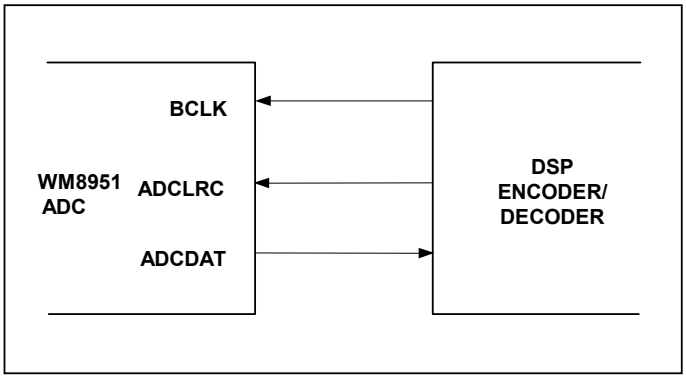


Figure 22 Slave Mode

Note that the WM8951L relies on controlled phase relationships between audio interface BCLK, and the master MCLK or CLKOUT. To avoid any timing hazards, refer to the timing section for detailed information.

AUDIO DATA SAMPLING RATES

The WM8951L provides for two modes of operation (normal and USB) to generate the required ADC sampling rates. Normal and USB modes are programmed under software control according to the table below.

In Normal mode, the user controls the sample rate by using an appropriate MCLK or crystal frequency and the sample rate control register setting. The WM8951L can support sample rates from 8ks/s up to 96ks/s.

In USB mode, the user must use a fixed MLCK or crystal frequency of 12MHz to generate sample rates from 8ks/s to 96ks/s. It is called USB mode since the common USB (Universal Serial Bus) clock is at 12MHz and the WM8951L can be directly used within such systems. WM8951L can generate all the normal audio sample rates from this one Master Clock frequency, removing the need for different master clocks or PLL circuits.

Sample rates listed in the following sections are supported.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
0001000 Sampling Control	0	USB/ NORMAL	0	Mode Select 1 = USB mode (250/272fs) 0 = Normal mode (256/384fs)	
	1	BOSR	0	Base Over-Sampling Rate	
				USB Mode 0 = 250fs 1 = 272fs	Normal Mode 96/88.2kHz 0 = 256fs 1 = 128fs 1 = 384fs 1 = 192fs
	5:2	SR[3:0]	0000	Sample rate control; See USB Mode and Normal Mode Sample Rate sections for operation	

Table 11 Sample Rate Control

NORMAL MODE SAMPLE RATES

In normal mode MCLK/crystal oscillator is set up according to the desired sample rates of the ADC. For ADC sampling rates of 8, 32, 48 or 96kHz, MCLK frequencies of either 12.288MHz (256fs) or 18.432MHz (384fs) can be used. For ADC sampling rates of 8, 44.1 or 88.2kHz from MCLK frequencies of either 11.2896MHz (256fs) or 16.9344MHz (384fs) can be used.

Table 12 should be used to set up the device to work with the various sample rate combinations. For example if the user wishes to use the WM8951L in normal mode with the ADC sample rate at 48kHz then the device should be programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0 with a 12.288MHz MCLK or with BOSR = 1, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0 with a 18.432MHz MCLK. The ADC will then operate with a Digital Filter of type 1, refer to Digital Filter Characteristics section for an explanation of the different filter types.

SAMPLING RATE	MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
kHz	MHz	BOSR	SR3	SR2	SR1	SR0	
48	12.288	0 (256fs)	0	0	0	0	1
	18.432	1 (384fs)	0	0	0	0	
	18.432	1 (384fs)	0	0	1	0	
8	12.288	0 (256fs)	0	0	1	1	1
	18.432	1 (384fs)	0	0	1	1	
32	12.288	0 (256fs)	0	1	1	0	1
	18.432	1 (384fs)	0	1	1	0	
96	12.288	0 (128fs)	0	1	1	1	2
	18.432	1 (192fs)	0	1	1	1	
44.1	11.2896	0 (256fs)	1	0	0	0	1
	16.9344	1 (384fs)	1	0	0	0	
	16.9344	1 (384fs)	1	0	1	0	
8 (Note 1)	11.2896	0 (256fs)	1	0	1	1	1
	16.9344	1 (384fs)	1	0	1	1	
88.2	11.2896	0 (128fs)	1	1	1	1	2
	16.9344	1 (192fs)	1	1	1	1	

Table 12 Normal Mode Sample Rate Look-up Table

Notes:

1. 8k not exact, actual = 8.018kHz
2. All other combinations of BOSR and SR[3:0] that are not in the truth table are invalid

The BOSR bit represents the base over-sampling rate. This is the rate that the WM8951L digital signal processing is carried out at. In Normal mode, with BOSR = 0, the base over-sampling rate is at 256fs, with BOSR = 1, the base over-sampling rate is at 384fs. This can be used to determine the actual audio data rate produced by the ADC.

The exact sample rates achieved are defined by the relationships in Table 13 below.

TARGET SAMPLING RATE	ACTUAL SAMPLING RATE			
	BOSR=0		BOSR=1	
	MCLK=12.288	MCLK=11.2896	MCLK=18.432	MCLK=16.9344
kHz	kHz	kHz	kHz	kHz
8	8	8.018	8	8.018
	(12.288MHz/256) x 1/6	(11.2896MHz/256) x 2/11	(18.432MHz/384) x 1/6	(16.9344MHz/384) x 2/11
32	32	*not available*	32	*not available*
	(12.288MHz/256) x 2/3		(18.432MHz/384) x 2/3	
44.1	*not available*	44.1	*not available*	44.1
		11.2896MHz/256		16.9344MHz /384
48	48	*not available*	48	*not available*
	12.288MHz/256		18.432MHz/384	
88.2	*not available*	88.2	*not available*	88.2
		(11.2896MHz/256) x 2		(16.9344MHz /384) x 2
96	96	*not available*	96	*not available*
	(12.288MHz/256) x 2		(18.432MHz/384) x 2	

Table 13 Normal Mode Actual Sample Rates

128/192fs NORMAL MODE

The Normal Mode sample rates are designed for standard 256fs and 384fs MCLK rates. However the WM8951L is also capable of being clocked from a 128 or 192fs MCLK for application over limited sampling rates as shown in the table below.

SAMPLING RATE kHz	MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
	MHz	BOSR	SR3	SR2	SR1	SR0	
48	6.144	0	0	1	1	1	2
	9.216	1	0	1	1	1	
44.1	5.6448	0	1	1	1	1	2
	8.4672	1	1	1	1	1	

Table 14 128fs Normal Mode Sample Rate Look-up Table

512/768fs NORMAL MODE

512 fs and 768 fs MCLK rates can be accommodated by using the CLKIDIV2 bit (Register 8, bit 6). The core clock to the DSP will be divided by 2 so an external 512/768 fs MCLK will become 256/384 fs internally and the device otherwise operates as in Table 10 but with MCLK at twice the specified rate. See Table 7 for software control.

USB MODE SAMPLE RATES

In USB mode the MCLK/crystal oscillator input is 12MHz only.

SAMPLING RATE ADC	MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
kHz	MHz	BOSR	SR3	SR2	SR1	SR0	
48	12.000	0	0	0	0	0	0
44.1 (Note 2)	12.000	1	1	0	0	0	1
8	12.000	0	0	0	1	1	0
8 (Note 1)	12.000	1	1	0	1	1	1
32	12.000	0	0	1	1	0	0
96	12.000	0	0	1	1	1	3
88.2 (Note 3)	12.000	1	1	1	1	1	2

Table 15 USB Mode Sample Rate Look-up Table

Notes:

1. 8k not exact, actual = 8.021kHz
2. 44.1k not exact, actual = 44.118kHz
3. 88.1k not exact, actual = 88.235kHz
4. All other combinations of BOSR and SR[3:0] that are not in the truth table are invalid

The table above can be used to set up the device to work with various sample rate combinations. For example if the user wishes to use the WM8951L in USB mode with the ADC sample rate at 48kHz then the device should be programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0. The ADC will then operate with a Digital Filter of type 0, refer to Digital Filter Characteristics section for an explanation of the different filter types.

The BOSR bit represents the base over-sampling rate. This is the rate that the WM8951L digital signal processing is carried out at and the sampling rate will always be a sub-multiple of this. In USB mode, with BOSR = 0, the base over-sampling rate is defined at 250fs, with BOSR = 1, the base over-sampling rate is defined at 272fs. This can be used to determine the actual audio sampling rate produced by the ADC.

The exact sample rates supported for all combinations are defined by the relationships in Table 16 below.

TARGET SAMPLING RATE	ACTUAL SAMPLING RATE	
	BOSR=0 (250fs)	BOSR=1 (272fs)
kHz	kHz	kHz
8	8	8.021
	12MHz/(250 x 48/8)	12MHz/(272 x 11/2)
32	32	*not available*
	12MHz/(250 x 48/32)	
44.1	*not available*	44.117
		12MHz/272
48	48	*not available*
	12MHz/250	
88.2	*not available*	88.235
		12MHz/136
96	96	*not available*
	12MHz/125	

Table 16 USB Mode Actual Sample Rates

ACTIVATING DSP AND DIGITAL AUDIO INTERFACE

To prevent any communication problems from arising across the Digital Audio Interface the Audio Interface is disabled (tristate with weak 100k pulldown). Once the Audio Interface and the Sampling Control has been programmed it is activated by setting the ACTIVE bit under Software Control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001001 Active Control	0	ACTIVE	0	Activate Interface 1 = Active 0 = Inactive

Table 17 Activating DSP and Digital Audio Interface

It is recommended that between changing any content of Digital Audio Interface or Sampling Control Register that the active bit is reset then set.

SOFTWARE CONTROL INTERFACE

The software control interface may be operated using either a 3-wire (SPI-compatible) or 2-wire MPU interface. Selection of interface format is achieved by setting the state of the MODE pin.

In 3-wire mode, SDIN is used for the program data, SCLK is used to clock in the program data and CSB is used to latch in the program data. In 2-wire mode, SDIN is used for serial data and SCLK is used for the serial clock. In 2-wire mode, the state of CSB pin allows the user to select one of two addresses.

SELECTION OF SERIAL CONTROL MODE

The serial control interface may be selected to operate in either 2 or 3-wire modes. This is achieved by setting the state of the MODE pin.

MODE	INTERFACE FORMAT
0	2 wire
1	3 wire

Table 18 Control Interface Mode Selection

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

The WM8951L can be controlled using a 3-wire serial interface. SDIN is used for the program data, SCLK is used to clock in the program data and CSB is use to latch in the program data. The 3-wire interface protocol is shown in Figure 23.

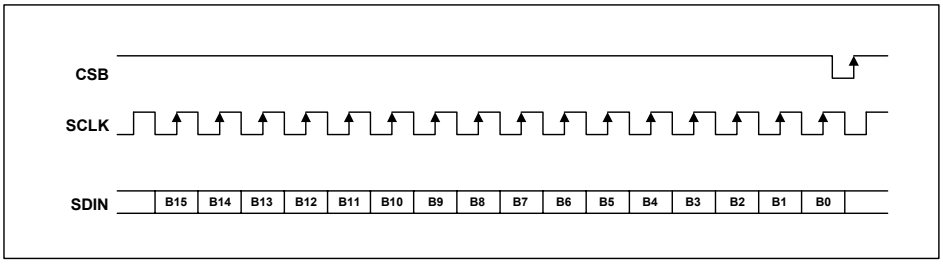


Figure 23 3-Wire Serial Interface

Notes:

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits
3. CSB is edge sensitive not level sensitive. The data is latched on the rising edge of CSB.

2-WIRE SERIAL CONTROL MODE

The WM8951L supports a 2-wire serial interface. The WM8951L has one of two slave addresses that are selected by setting the state of pin 26, (CSB).

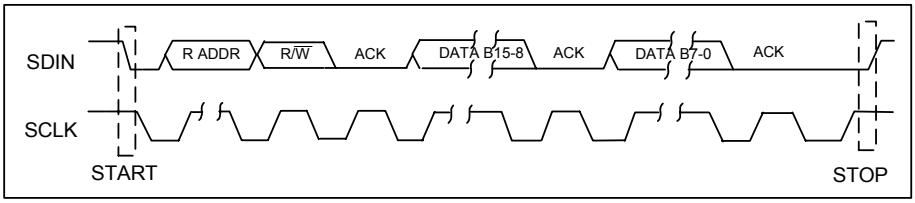


Figure 24 2-Wire Serial Interface

Notes:

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits

CSB STATE	ADDRESS
0	0011010
1	0011011

Table 19 2-Wire MPU Interface Address Selection

To control the WM8951L on the 2-wire bus the master control device must initiate a data transfer by establishing a start condition, defined by a high to low transition on SDIN while SCLK remains high. This indicates that an address and data transfer will follow. All peripherals on the 2-wire bus respond to the start condition and shift in the next eight bits (7-bit address + R/W bit). The transfer is MSB first. The 7-bit address consists of a 6-bit base address + a single programmable bit to select one of two available addresses for this device (see table 24). If the correct address is received and the R/W bit is '0', indicating a write, then the WM8951L will respond by pulling SDIN low on the next clock pulse (ACK). The WM8951L is a write only device and will only respond to the R/W bit indicating a write. If the address is not recognised the device will return to the idle condition and wait for a new start condition and valid address.

Once the WM8951L has acknowledged a correct address, the controller will send eight data bits (bits B15-B8). WM8951L will then acknowledge the sent data by pulling SDIN low for one clock pulse.

The controller will then send the remaining eight data bits (bits B7-B0) and the WM8951L will then acknowledge again by pulling SDIN low.

A stop condition is defined when there is a low to high transition on SDIN while SCLK is high. If a start or stop condition is detected out of sequence at any point in the data transfer then the device will jump to the idle condition.

After receiving a complete address and data sequence the WM8951L returns to the idle state and waits for another start condition. Each write to a register requires the complete sequence of start condition, device address and R/W bit followed by the 16 register address and data bits.

POWER DOWN MODES

The WM8951L contains power conservation modes in which various circuit blocks may be safely powered down in order to conserve power. This is software programmable as shown in the table below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000110 Power Down Control	0	LINEINPD	1	Line Input Power Down 1 = Enable Power Down 0 = Disable Power Down
	1	MICPD	1	Microphone Input an Bias Power Down 1 = Enable Power Down 0 = Disable Power Down
	2	ADCPD	1	ADC Power Down 1 = Enable Power Down 0 = Disable Power Down
	5	OSCPD	0	Oscillator Power Down 1 = Enable Power Down 0 = Disable Power Down
	6	CLKOUTPD	0	CLKOUT power down 1 = Enable Power Down 0 = Disable Power Down
	7	POWEROFF	1	Power Off Device 1 = Device Power Off 0 = Device Power On

Table 20 Power Conservation Modes Software Control

The power down control can be used to either a) permanently disable functions when not required in certain applications or b) to dynamically power up and down functions depending on the operating mode, e.g.: during record. Please follow the special instructions below if dynamic implementations are being used.

LINEINPD: Simultaneously powers down both the Line Inputs. This can be done dynamically without any audible effects on the ADC. This is of use when the device enters Pause or Stop modes or the Microphone input has been selected.

MICPD: Simultaneously powers down both the Microphone Input and Microphone Bias. If this is done dynamically, audible pops through the ADC will result. This will only be audible if the Microphone Input is selected to the ADC at the time. If the state of MICPD is changed then the controlling DSP or microprocessor should switch to select the Line Inputs as input to the ADC (INSEL) before changing MICPD. This is of use when the device enters Pause or Stop modes or the Microphone Input is not selected.

ADCPD: Powers down the ADC and ADC Filters. If this is done dynamically then audible pops will result if any signals were present through the ADC. To overcome this whenever the ADC is to be powered down, either mute the Microphone Input (MUTEIN) or MUTELINEIN, then change ADCPD. This is of use when the device enters Pause or Stop modes regardless of whether Microphone or Line Inputs are selected.

OSCPD: Powers off the on board crystal oscillator. The MCLK input will function independently of the Oscillator being powered down.

CLKOUTPD: Powers down the CLOCKOUT pin. This conserves power, reduces digital noise and RF emissions if not required. CLKOUT is tied low when powered down.

The device can be put into a standby mode (STANDBY) by powering down all the audio circuitry under software control as shown in Table 21. If the crystal oscillator and/or CLOKOUT pins are being used to derive the system master clock, these should probably never be powered off in standby. Provision has been made to independently power off these areas according to Table 21.

POWER OFF	CLKOUTPD	OSCPD	ADCPD	MICPD	LINEINPD	DESCRIPTION
0	0	0	1	1	1	STANDBY, but with Crystal Oscillator OS and CLKOUT available
0	1	0	1	1	1	STANDBY, but with Crystal Oscillator OS available, CLKOUT not-available
0	1	1	1	1	1	STANDBY, Crystal oscillator and CLKOUT not-available.

Table 21 Standby Mode

In STANDBY mode the Control Interface, a small portion of the digital and areas of the analogue circuitry remain active. The active analogue includes the analogue VMID reference so that the analogue line inputs remain biased to VMID. This reduces any audible effects caused by DC glitches when entering or leaving STANDBY mode.

The device can be powered off by writing to the POWEROFF bit of the Power Down register. In POWEROFF mode the Control Interface and a small portion of the digital remain active. The analogue VMID reference is disabled. As in STANDBY mode the crystal oscillator and/or CLKOUT pin can be independently controlled. Refer to Table 22.

POWER OFF	CLKOUTPD	OSCPD	ADCPD	MICPD	LINEINPD	DESCRIPTION
1	0	0	X	X	X	POWEROFF, but with Crystal Oscillator OS and CLKOUT available
1	1	0	X	X	X	POWEROFF, but with Crystal Oscillator OS available, CLKOUT not-available
1	1	1	X	X	X	POWEROFF, Crystal oscillator and CLKOUT not-available.

Table 22 Poweroff Mode

Note:

For minimum power consumption unused control bits 3 and 4 should be set to '1'.

REGISTER MAP

The complete register map is shown in Table 23. The detailed description can be found in Table 24 and in the relevant text of the device description. There are 11 registers with 16 bits per register (7 bit address + 9 bits of data). These can be controlled using either the 2 wire or 3 wire MPU interface.

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R0 (00h) Left Line In	LRINBOTH	LINMUTE	0	0	LINVOL[4:0]					0_1001_0111
R1 (01h) Right Line In	RLINBOTH	RINMUTE	0	0	RINVOL[4:0]					0_1001_0111
R2 (02h) Reserved	Reserved[8:0]									Reserved
R3 (03h) Reserved	Reserved[8:0]									Reserved
R4 (04h) Analogue Audio Path Control	0	00		0	0	0	INSEL	MUTEMIC	MICBOOST	0_0000_0101
R5 (05h) Digital Audio Path Control	0	0	0	0	0	0	00		ADCHPD	0_0000_0000
R6 (06h) Power Down Control	0	POWEROFF	CLKOUTPD	OSCPD	1	1	ADCPD	MICPD	LINEINPD	0_1001_1111
R7 (07h) Digital Audio Interface Format	0	BCLKINV	MS	LRSWAP	LRP	IWL[1:0]		FORMAT[1:0]		0_0000_1010
R8 (08h) Sampling Control	0	CLKODIV2	CLKIDIV2	SR[3:0]				BOSR	USB/ NORMAL	0_0000_0000
R9 (09h) Active Control	0	0	0	0	0	0	0	0	Active	0_0000_0000
R15 (0Fh) Reset	RESET[8:0]									not reset

Table 23 Mapping of Program Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000000 Left Line In	4:0	LINVOL[4:0]	10111 (0dB)	Left Channel Line Input Volume Control 11111 = +12dB . . 1.5dB steps down to 00000 = -34.5dB
	7	LINMUTE	1	Left Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	LRINBOTH	0	Left to Right Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of LINVOL[4:0] and LINMUTE to RINVOL[4:0] and RINMUTE 0 = Disable Simultaneous Load
0000001 Right Line In	4:0	RINVOL[4:0]	10111 (0dB)	Right Channel Line Input Volume Control 11111 = +12dB . .1.5dB steps down to 00000 = -34.5dB
	7	RINMUTE	1	Right Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	RLINBOTH	0	Right to Left Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of RINVOL[4:0] and RINMUTE to LINVOL[4:0] and LINMUTE 0 = Disable Simultaneous Load
0000100 Analogue Audio Path Control	0	MICBOOST	0	Microphone Input Level Boost 1 = Enable Boost 0 = Disable Boost
	1	MUTEMIC	1	Mic Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	2	INSEL	0	Microphone/Line Input Select to ADC 1 = Microphone Input Select to ADC 0 = Line Input Select to ADC
0000101 Digital Audio Path Control	0	ADCHPD	0	ADC High Pass Filter Enable 1 = Disable High Pass Filter 0 = Enable High Pass Filter
	4	HPOR	0	Store dc offset when High Pass Filter disabled 1 = store offset 0 = clear offset
0000110 Power Down Control	0	LINEINPD	1	Line Input Power Down 1 = Enable Power Down 0 = Disable Power Down
	1	MICPD	1	Microphone Input an Bias Power Down 1 = Enable Power Down 0 = Disable Power Down
	2	ADCPD	1	ADC Power Down 1 = Enable Power Down 0 = Disable Power Down

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5	OSCPD	0	Oscillator Power Down 1 = Enable Power Down 0 = Disable Power Down
	6	CLKOUTPD	0	CLKOUT power down 1 = Enable Power Down 0 = Disable Power Down
	7	POWEROFF	1	POWEROFF mode 1 = Enable POWEROFF 0 = Disable POWEROFF
0000111 Digital Audio Interface Format	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode, frame sync + 2 data packed words 10 = I^2S Format, MSB-First left-1 justified 01 = MSB-First, left justified 00 = MSB-First, right justified
	3:2	IWL[1:0]	10	Input Audio Data Bit Length Select 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	7	BCLKINV	0	Bit Clock Invert 1 = Invert BCLK 0 = Don't invert BCLK
0001000 Sampling Control	0	USB/ NORMAL	0	Mode Select 1 = USB mode (250/272fs) 0 = Normal mode (256/384fs)
	1	BOSR	0	Base Over-Sampling Rate USB Mode: 0 = 250fs; 1 = 272fs Normal Mode: 0 = 256fs; 1 = 384fs
	5:2	SR[3:0]	0000	ADC sample rate control; See USB Mode and Normal Mode Sample Rate sections for operation
	6	CLKIDIV2	0	Core Clock divider select 1 = Core Clock is MCLK divided by 2 0 = Core Clock is MCLK
	7	CLKODIV2	0	CLKOUT divider select 1 = CLOCKOUT is Core Clock divided by 2 0 = CLOCKOUT is Core Clock
0001001 Active Control	0	ACTIVE	0	Activate Interface 1 = Active 0 = Inactive
0001111 Reset Register	8:0	RESET	not reset	Reset Register Writing 00000000 to register resets device

Table 24 Register Map Description

DIGITAL FILTER CHARACTERISTICS

The ADC employs different digital filters. There are 4 types of digital filter, called Type 0, 1, 2 and 3. The performance of Types 0 and 1 is listed in the table below, the responses of all filters is shown in the proceeding pages.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter Type 0 (USB Mode, 250fs operation)					
Passband	+/- 0.05dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-60			dB
ADC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.05dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-60			dB
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		

Table 25 Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) - the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

ADC FILTER RESPONSES

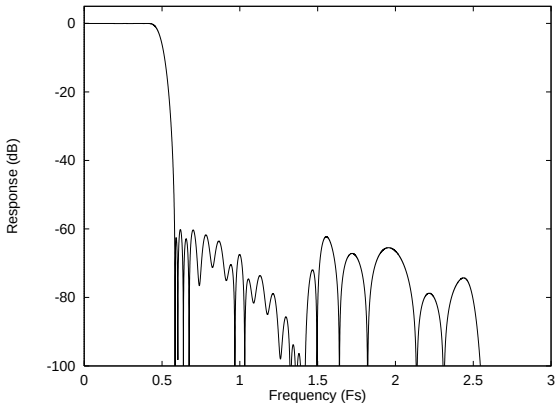


Figure 25 ADC Digital Filter Frequency Response –Type 0

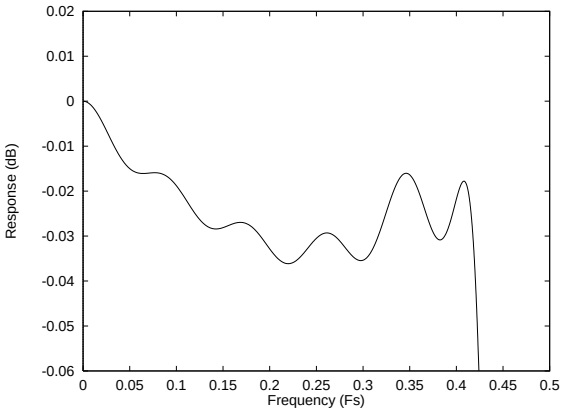


Figure 26 ADC Digital Filter Ripple –Type 0

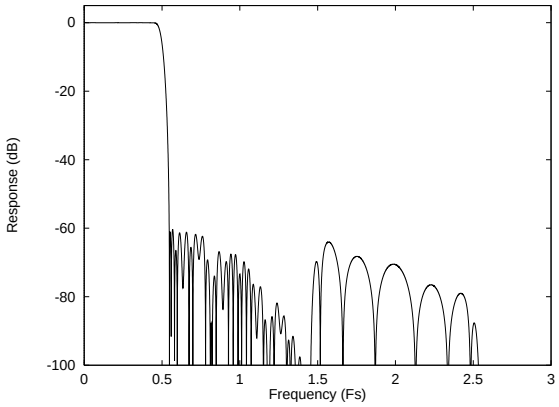


Figure 27 ADC Digital Filter Frequency Response –Type 1

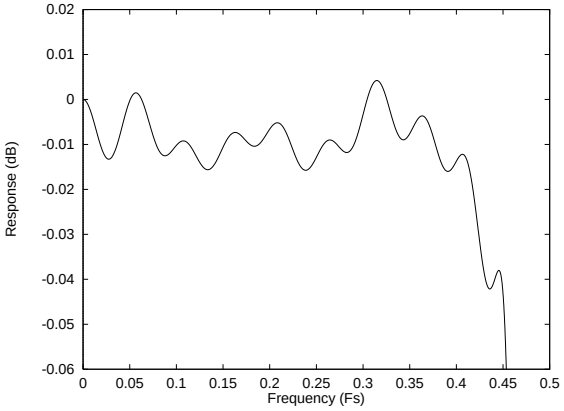


Figure 28 ADC Digital Filter Ripple –Type 1

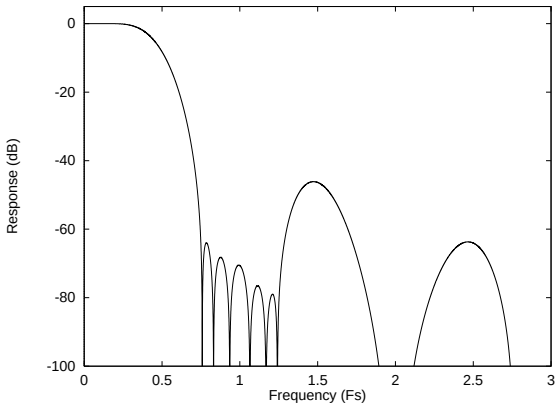


Figure 29 ADC Digital Filter Frequency Response –Type 2

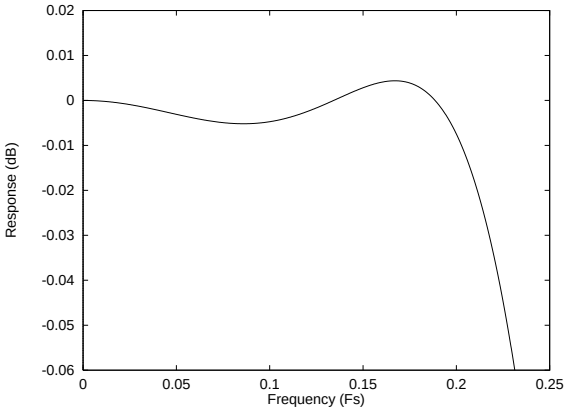


Figure 30 ADC Digital Filter Ripple –Type 2

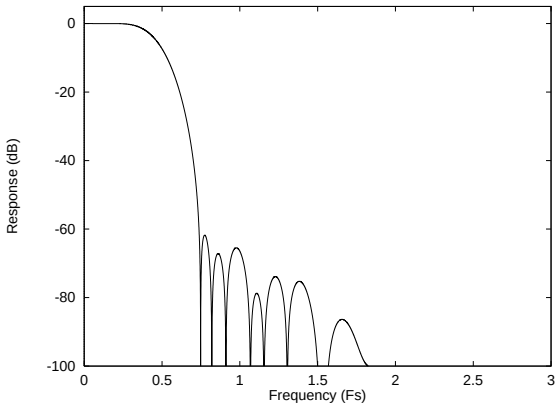


Figure 31 ADC Digital Filter Frequency Response –Type 3

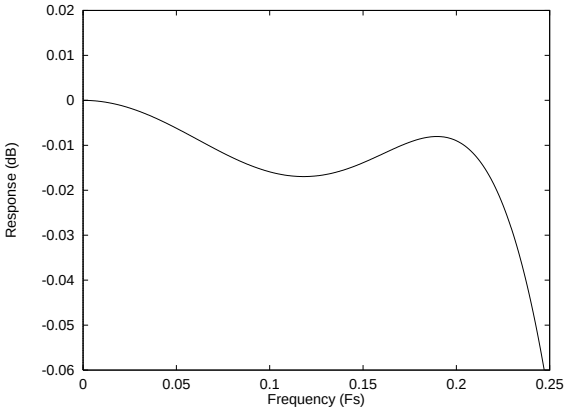


Figure 32 ADC Digital Filter Ripple –Type 3

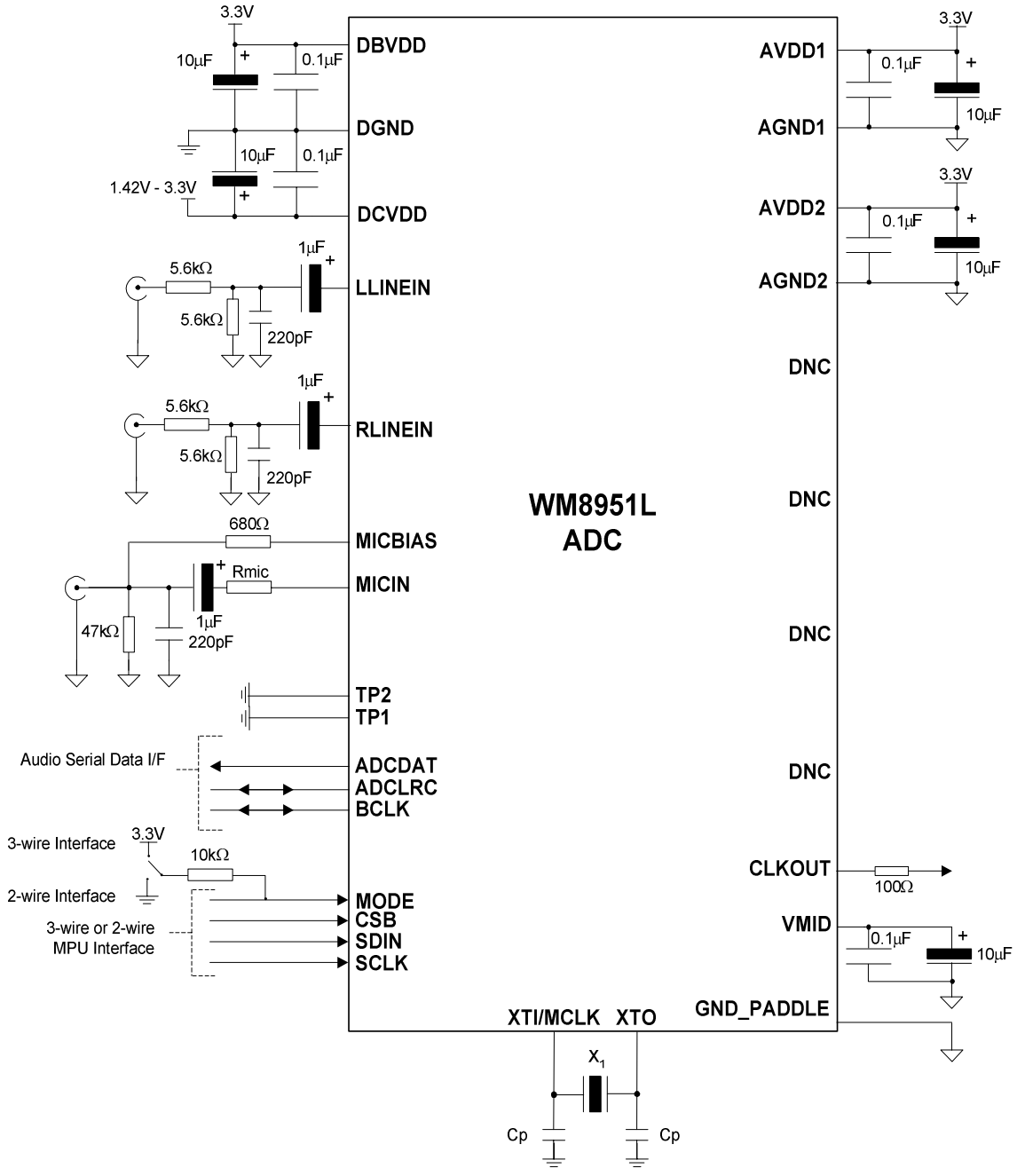
ADC HIGH PASS FILTER

The WM8951L has a selectable digital high pass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995\, z^{-1}}$$

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

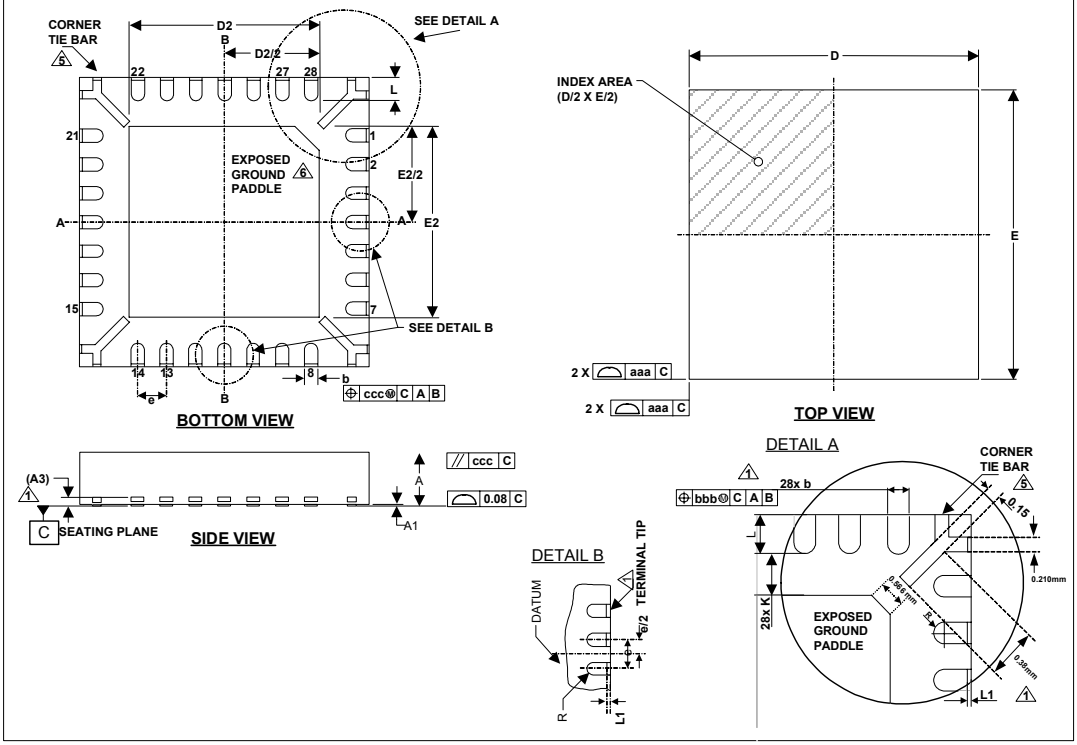


Note:
1. Rmic - The value of this resistor is dependent on the gain setting. Refer to Page 20 for Rmic calculation.
2. Where possible, it is recommended that NPO or COG type capacitors should be used for best performance.
3. TP2 Should be left floating in master mode
4. For added strength and heat dissipation, it is recommended that the GND_PADDLE is connected to AGND.

Figure 33 External Components Diagram

PACKAGE DIMENSIONS

FL: 28 PIN QFN PLASTIC PACKAGE 5 X 5 X 0.9 mm BODY, 0.50 mm LEAD PITCH **DM023.G**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.85	0.90	1.00	
A1	0	0.02	0.05	
A3		0.2 REF		
b	0.18	0.23	0.30	1
D		5.00 BSC		
D2	3.2	3.3	3.4	2
E		5.00 BSC		
E2	3.2	3.3	3.4	2
e		0.5 BSC		
L	0.35	0.4	0.45	
L1			0.1	1
R	b(min)/2			
K	0.20			
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220, VARIATION VHHD-1			

NOTES:
1. **DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL PULL BACK FROM PACKAGE SIDE WALL. MAXIMUM OF 0.1mm IS ACCEPTABLE. WHERE TERMINAL PULL BACK EXISTS, ONLY UPPER HALF OF LEAD IS VISIBLE ON PACKAGE SIDE WALL DUE TO HALF ETCHING OF LEADFRAME.**
2. **FALLS WITHIN JEDEC, MO-220 WITH THE EXCEPTION OF D2, E2: D2,E2: LARGER PAD SIZE CHOSEN WHICH IS JUST OUTSIDE JEDEC SPECIFICATION**
3. **ALL DIMENSIONS ARE IN MILLIMETRES**
4. **THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.**
5. **SHAPE AND SIZE OF CORNER TIE BAR MAY VARY WITH PACKAGE TERMINAL COUNT. CORNER TIE BAR IS CONNECTED TO EXPOSED PAD INTERNALLY**
6. **REFER TO APPLICATION NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.**

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