WM8953

Low Power Stereo ADC with PLL and TDM Interface

DESCRIPTION

The WM8953 is a low power high performance stereo ADC designed for mobile handsets and other portable devices.

Four single-ended or differential input connections are provided, with up to 60dB of analogue gain in each input path. Stereo 24-bit sigma-delta ADCs provide hi-fi quality audio recording of microphones or line input. A programmable high pass filter is available in the ADC path for removing DC offsets and suppressing wind and other low frequency noise.

A low noise microphone bias with programmable current detect and short-circuit detect is provided.

A flexible digital audio interface supports most commonly-used clocking schemes. The audio interface supports TDM and tristate outputs allow multiple devices to share the same interface.

An integrated low power PLL provides support for most commonly-used audio sample rates.

The WM8953 is supplied in very small and thin 42-ball WCSP package, ideal for portable systems.

FEATURES

- SNR 94dB ('A' weighted)
- THD -82dB at 48kHz, 3.3V
- Full stereo microphone / line input interface
- Low noise MICBIAS
- Low power consumption
- Full analogue and digital volume control
- PLL provides flexible clocking scheme
- 2-wire, 3-wire or 4-wire control
- Sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48kHz
- GPIO functions available
- Digital supply: 1.71V – 3.6V
- Analogue supply: 2.7V – 3.6V
- W-CSP package (3.226 x 3.44 x 0.7mm, 0.5mm pitch)

APPLICATIONS

- Multimedia phones
- General purpose low power audio ADC

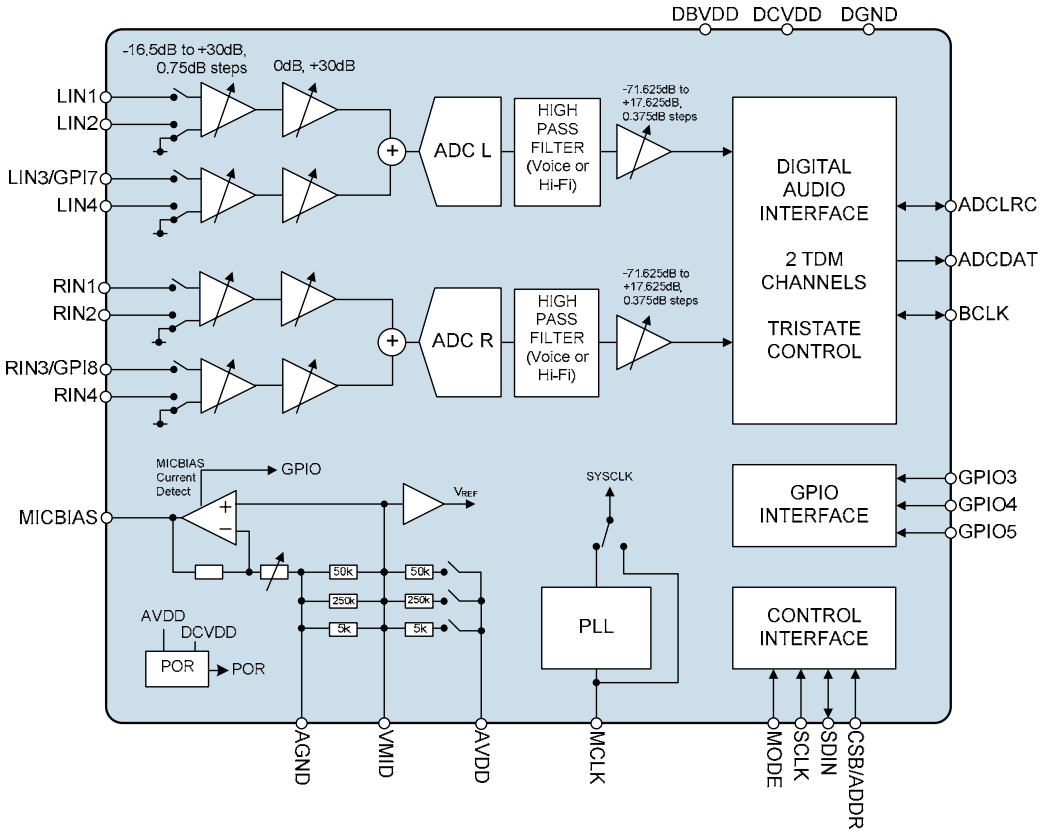
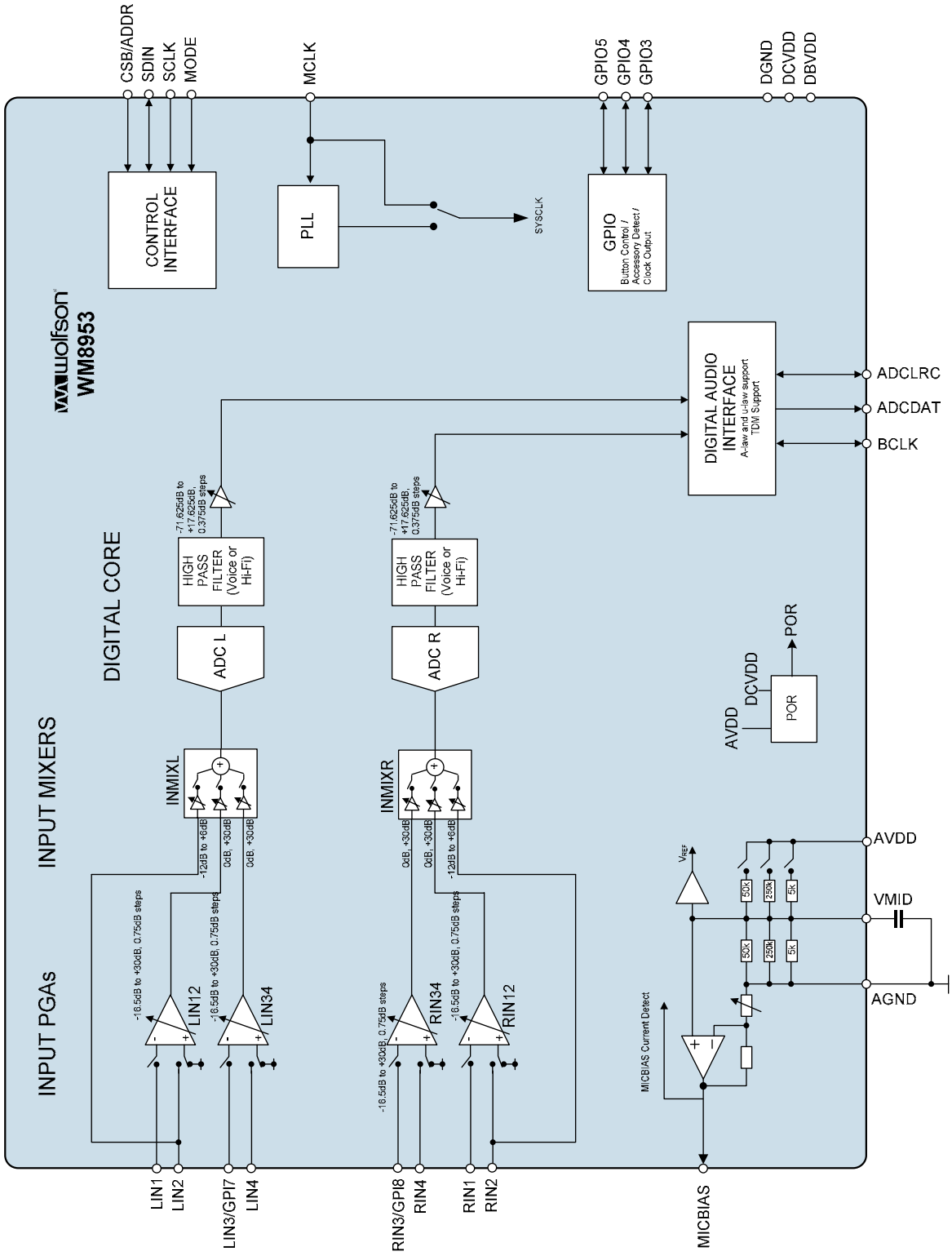
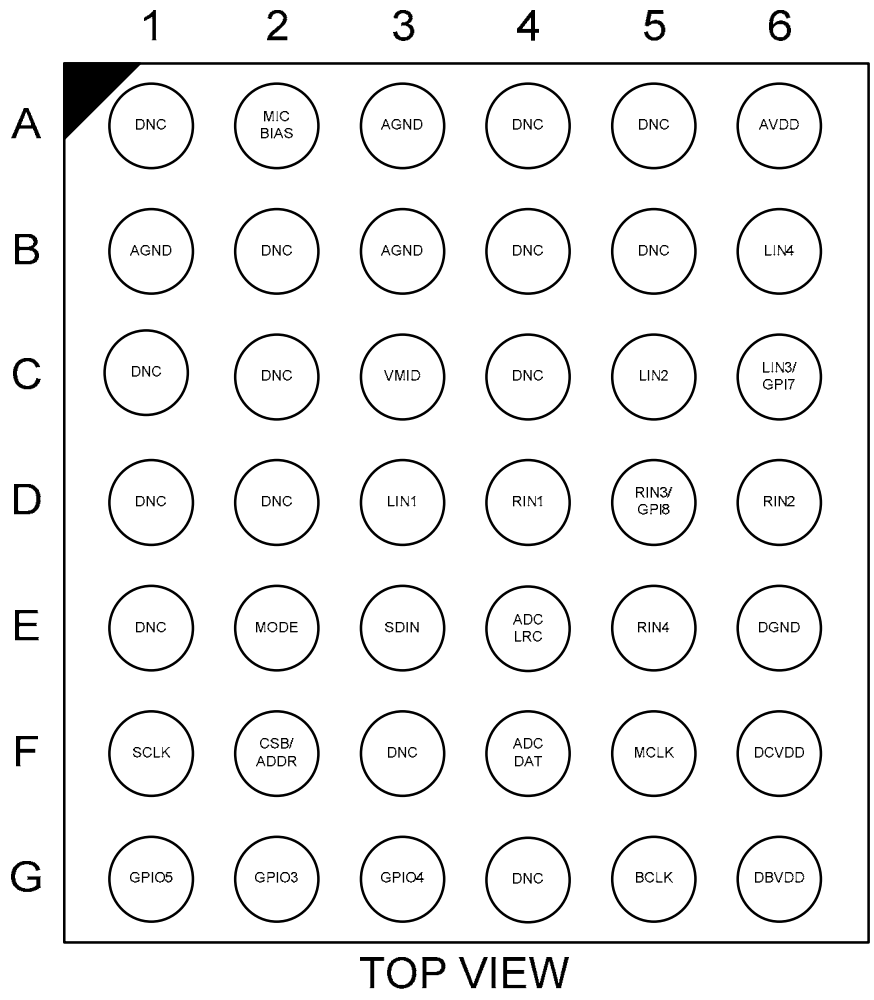


TABLE OF CONTENTS

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8953ECS/RV	-40°C to +85°C	42-ball W-CSP (Pb-free, Tape and reel)	MSL3	260°C

Note:

Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A2	MICBIAS	Analogue Output	Microphone bias
D3	LIN1	Analogue Input	Left channel single-ended MIC input / Left channel negative differential MIC input
C5	LIN2	Analogue Input	Left channel line input / Left channel positive differential MIC input
C6	LIN3 / GPI7	Analogue Input / Digital Input	Left channel line input / Left channel negative differential MIC input / Accessory or button detect input pin
B6	LIN4	Analogue Input	Left channel line input / Left channel positive differential MIC input /
D4	RIN1	Analogue Input	Right channel single-ended MIC input / Right channel negative differential MIC input
D6	RIN2	Analogue Input	Right channel line input / Right channel positive differential MIC input
D5	RIN3 / GPI8	Analogue Input / Digital Input	Right channel line input / Right channel negative differential MIC input / Accessory or button detect input pin
E5	RIN4	Analogue Input	Left channel line input / Left channel positive differential MIC input /
F6	DCVDD	Supply	Digital core supply
E6	DGND	Supply	Digital ground (Return path for both DCVDD and DBVDD)
G6	DBVDD	Supply	Digital buffer (I/O) supply
A6	AVDD	Supply	Analogue supply
A3, B1, B3	AGND	Supply	Analogue ground (Return path for AVDD)
F5	MCLK	Digital Input	Master clock
G5	BCLK	Digital Input / Output	Audio interface bit clock
E4	ADCLRC	Digital Input / Output	Audio interface ADC left / right clock
F4	ADCDAT	Digital Output	ADC digital audio data
E2	MODE	Digital Input	Selects 2-wire or 3/4 -wire control
F2	CSB / ADDR	Digital Input	3/4 -wire chip select or 2-wire address select
F1	SCLK	Digital Input	Control interface clock input
E3	SDIN	Digital Input / Output	Control interface data input / 2-wire acknowledge output
C3	VMID	Analogue Output	Midrail voltage decoupling capacitor
G2	GPIO3	Digital Input / Output	GPIO pin
G3	GPIO4	Digital Input / Output	GPIO pin
G1	GPIO5	Digital Input / Output	GPIO pin
A1, A4, A5, B2, B4, B5, C1, C2, C4, D1, D2, E1, F3, G4	DNC	Do Not Connect	

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages	-0.3V	+4.5V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.71		3.6	V
Digital supply range (Buffer)	DBVDD	1.71		3.6	V
Analogue supply range	AVDD	2.7		3.6	V
Ground	DGND, AGND		0		V

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
3. DCVDD must be less than or equal to AVDD.
4. DCVDD must be less than or equal to DBVDD.

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM8953 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package balls to PCB (conduction).

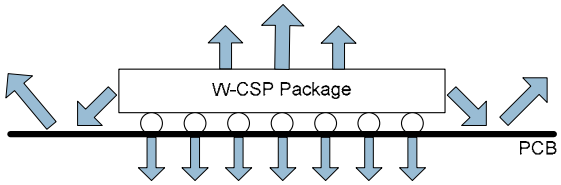


Figure 1 Heat Transfer Paths

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated in the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

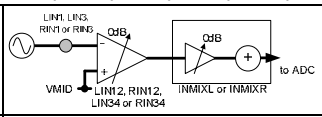
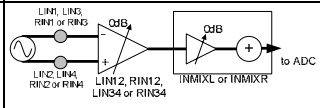
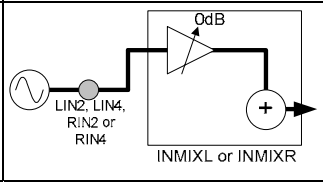
The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_A	-40		85	°C
Operating junction temperature	T_J	-40		100	°C
Thermal Resistance	Θ_{JA}		43		°C/W

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz,
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

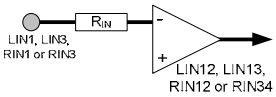
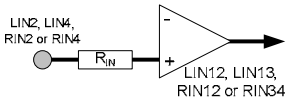
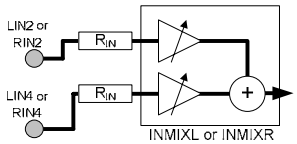
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Input Pin Maximum Signal Levels (LIN1, LIN2, LIN3, LIN4, RIN1, RIN2, RIN3, RIN4)						
Maximum Full-Scale PGA Input Signal Level Note 1; Note 2; Note 3	Single-ended PGA input on LIN1, LIN3, RIN1 or RIN3, output to INMIXL or INMIXR			1.0 0		Vrms dBV
	Differential PGA input on LIN1/LIN2, LIN3/LIN4, RIN1/RIN2 or RIN3/RIN4, output to INMIXL or INMIXR			1.0 0		Vrms dBV
Maximum Full-Scale Line Input Signal Level Note 1; Note 2; Note 3	Line input on LIN2, LIN4, RIN2 or RIN4 to INMIXL or INMIXR			1.0 0		Vrms dBV

Notes

1. Maximum full scale signal changes in proportion to AVDD (AVDD/3.3).
2. When mixing input PGA outputs and line inputs, the total signal must not exceed 1Vrms (0dBV).
3. A 1.0Vrms differential signal equates to 0.5Vrms/-6dBV per input.

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz,
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Input Pin Impedances (LIN1, LIN2, LIN3, LIN4, RIN1, RIN2, RIN3, RIN4)						
PGA Input Resistance Note: this will be seen in parallel with the resistance of other enabled input paths from the same pin	LIN1, LIN3, RIN1 or RIN3 (PGA Gain = -16.5dB)			57		kΩ
	LIN1, LIN3, RIN1 or RIN3 (PGA Gain = 0dB)			33		kΩ
	LIN1, LIN3, RIN1 or RIN3 (PGA Gain = +30dB)			2		kΩ
	LIN2, LIN4, RIN2 or RIN4 (Constant for all gains)			65		kΩ
Line Input Resistance Note: this will be seen in parallel with the resistance of other enabled input paths from the same pin	LIN2 or RIN2 to INMIXL or INMIXR (-12dB)			60		kΩ
	LIN2 or RIN2 to INMIXL or INMIXR (0dB)			15		kΩ
	LIN2 or RIN2 to INMIXL or INMIXR (+6dB)			7.5		kΩ
Input Capacitance	All analogue input pins			10		pF

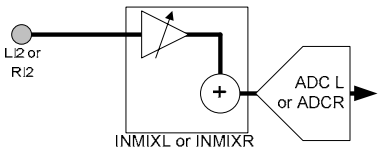
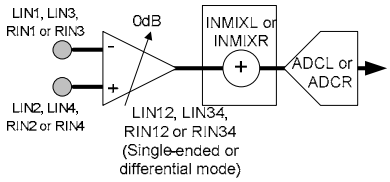
Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz,
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Programmable Gain Amplifiers (PGAs) LIN12, LIN34, RIN12 and RIN34					
Minimum Programmable Gain			-16.5		dB
Maximum Programmable Gain			30		dB
Programmable Gain Step Size	Guaranteed monotonic		1.5		dB
Mute Attenuation	Inputs disconnected		90		dB
Common Mode Rejection Ratio (1kHz input)	Single PGA in differential mode, gain = +30dB		60		dB
	Single PGA in differential mode, gain = 0dB		50		
	Single PGA in differential mode, gain = -16.5dB		50		
Input Mixers INMIXL and INMIXR					
Minimum Programmable Gain	PGA Outputs to INMIXL and INMIXR		0		dB
Maximum Programmable Gain	PGA Outputs to INMIXL and INMIXR		+30		dB
Programmable Gain Step Size	PGA Outputs to INMIXL and INMIXR		30		dB
Minimum Programmable Gain	Line Inputs to INMIXL and INMIXR		-12		dB
Maximum Programmable Gain	Line Inputs to INMIXL and INMIXR		+6		dB
Programmable Gain Step Size	Line Inputs to INMIXL and INMIXR		3		dB
Mute attenuation			95		dB

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz,
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC Input Path Performance						
SNR (A-weighted)	Line inputs to ADC via INMIXL and INMIXR, AVDD = 3.3V		84	94		dB
THD (-1dBFS input)				-84	-75	dB
THD+N (-1dBFS input)				-82	-73	dB
Crosstalk (L/R)				-100		dB
AVDD PSRR (217Hz)				45		dB
DCVDD PSRR (217Hz)				80		dB
SNR (A-weighted)	Line inputs to ADC via INMIXL and INMIXR, AVDD = 2.7V			93		dB
THD (-1dBFS input)				-78		dB
THD+N (-1dBFS input)				-76		dB
SNR (A-weighted)	Input PGAs to ADC via INMIXL or INMIXR, AVDD = 3.3V		84	94		dB
THD (-1dBFS input)				-84	-75	dB
THD+N (-1dBFS input)				-82	-73	dB
Crosstalk (L/R)				-100		dB
AVDD PSRR (217Hz)				45		dB
SNR (A-weighted)	Input PGAs to ADC via INMIXL or INMIXR, AVDD = 2.7V			92		dB
THD (-1dBFS input)				-78		dB
THD+N (-1dBFS input)				-76		dB

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz,
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Levels					
VMID Midrail Reference Voltage		-3%	AVDD/2	+3%	V
Microphone Bias					
Bias Voltage	3mA load current MBSEL=0	-5%	0.9×AVDD	+5%	V
	3mA load current MBSEL=1	-5%	0.65×AVDD	+5%	V
Bias Current Source				3	mA
Output Noise Density	1kHz to 20kHz		100		nV/√Hz
AVDD PSRR (217Hz)	100mV pk-pk @217Hz on AVDD		45		dB
Digital Input / Output					
Input HIGH Level		0.7×DBVDD			V
Input LOW Level				0.3×DBVDD	V
Note that digital input pins should not be left unconnected / floating. Internal pull-up/pull-down resistors may be enabled on GPIO3, GPIO4 and GPIO5 if required.					
Output HIGH Level	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	I_{OH}=-1mA			0.1×DBVDD	V
Input capacitance			10		pF
Input leakage		-0.9		0.9	uA
PLL					
Input Frequency	PRESCALE = 0b	7.7		18	MHz
	PRESCALE = 1b	14.4		36	MHz
Lock time			200		us
GPIO					
Clock output duty cycle (Integer OPCLKDIV)	SYSCLK=MCLK; OPCLKDIV=0000	35		65	%
	SYSCLK=MCLK; OPCLKDIV=1000	45		55	%
	SYSCLK=PLL output; OPCLKDIV=0000	45		55	%
	SYSCLK=PLL output; OPCLKDIV=1000	45		55	%
Clock output duty cycle (Non-integer OPCLKDIV)	SYSCLK=MCLK; OPCLKDIV=0100	33		66	%
	SYSCLK=PLL output; OPCLKDIV=0100	33		66	%
Interrupt response time for accessory / button detect	Input de-bounced	2^{21} / f_{SYSCLK}		2^{22} / f_{SYSCLK}	s
	Input de-bounced TOCLKSEL=1	2^{19} / f_{SYSCLK}		2^{20} / f_{SYSCLK}	s
	Input not de-bounced		0		s

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum theoretical full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. Crosstalk (L/R) (dB) – left-to-right and right-to-left channel crosstalk is the measured signal level in the idle channel at the test signal frequency relative to the signal level at the output of the active channel. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel. For example, measured signal level on the output of the idle right channel (RIN2 to ADCR) with a full scale signal level at the output of the active left channel (LIN1 to ADCL).
5. Multi-Path Channel Separation (dB) – is the measured signal level in the idle path at the test signal frequency relative to the signal level at the output of the active path. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
6. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
7. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

TYPICAL POWER CONSUMPTION

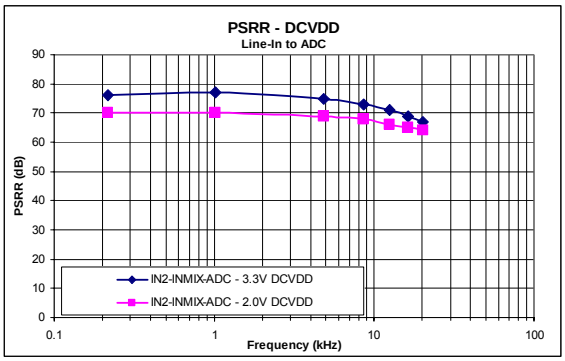
Mode	Other settings	AVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IDBVDD (mA)	IDCVDD (mA)	Total Power (mW)
Standby/Sleep								
OFF (default state at power-up)	No Clocks	2.7	1.8	1.8	0.028	0.000	0.000	0.075
		3.0	2.5	2.5	0.029	0.000	0.000	0.087
		3.3	3.3	3.3	0.030	0.000	0.000	0.099
		3.6	3.6	3.6	0.031	0.000	0.000	0.114
OFF (thermal sensor disabled)	No Clocks	2.7	1.8	1.8	0.008	0.000	0.000	0.020
		3.0	2.5	2.5	0.008	0.000	0.000	0.024
		3.3	3.3	3.3	0.009	0.000	0.000	0.029
		3.6	3.6	3.6	0.009	0.000	0.000	0.035
SLEEP (VMID enabled, thermal sensor anabled)	With Clocks	2.7	1.8	1.8	0.087	0.004	0.459	1.068
		3.0	2.5	2.5	0.096	0.008	0.694	2.044
		3.3	3.3	3.3	0.106	0.014	1.025	3.780
		3.6	3.6	3.6	0.117	0.017	1.162	4.667
ADC Record								
Stereo Line Record (L/RIN2 to INMIXL/R bypassing PGA)	fs=44.1kHz	2.7	1.8	1.8	5.272	0.023	2.285	18.389
		3.0	2.5	2.5	5.603	0.039	3.317	25.199
		3.3	3.3	3.3	5.927	0.060	4.728	35.358
		3.6	3.6	3.6	6.261	0.063	5.295	41.830
Stereo Line Record (L/RIN2 to INMIXL/R bypassing PGA)	fs=8kHz	2.7	1.8	1.8	5.125	0.017	0.758	15.233
		3.0	2.5	2.5	5.434	0.027	1.123	19.177
		3.3	3.3	3.3	5.738	0.061	1.634	24.528
		3.6	3.6	3.6	6.053	0.062	1.841	28.642

Notes:

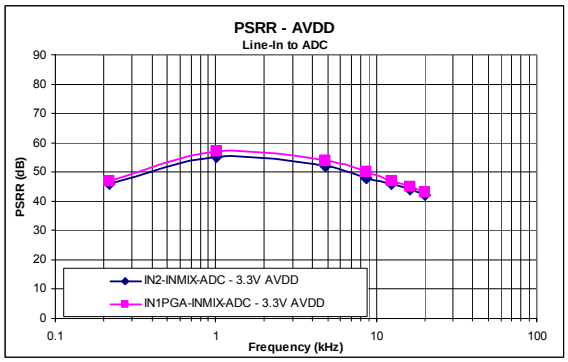
1. All figures are quoted at T_A = +25ºC
2. All figures are quoted as quiescent current unless otherwise stated.

PSRR PERFORMANCE

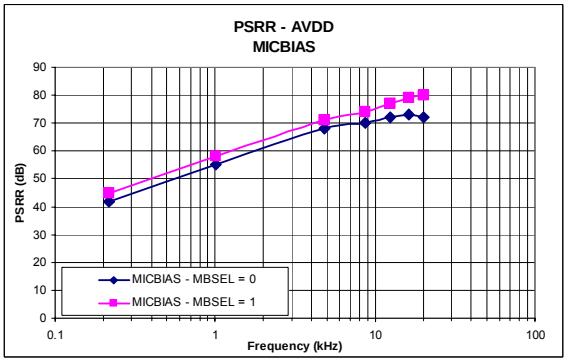
DCVDD – Line-In to ADC



AVDD – Line-In to ADC

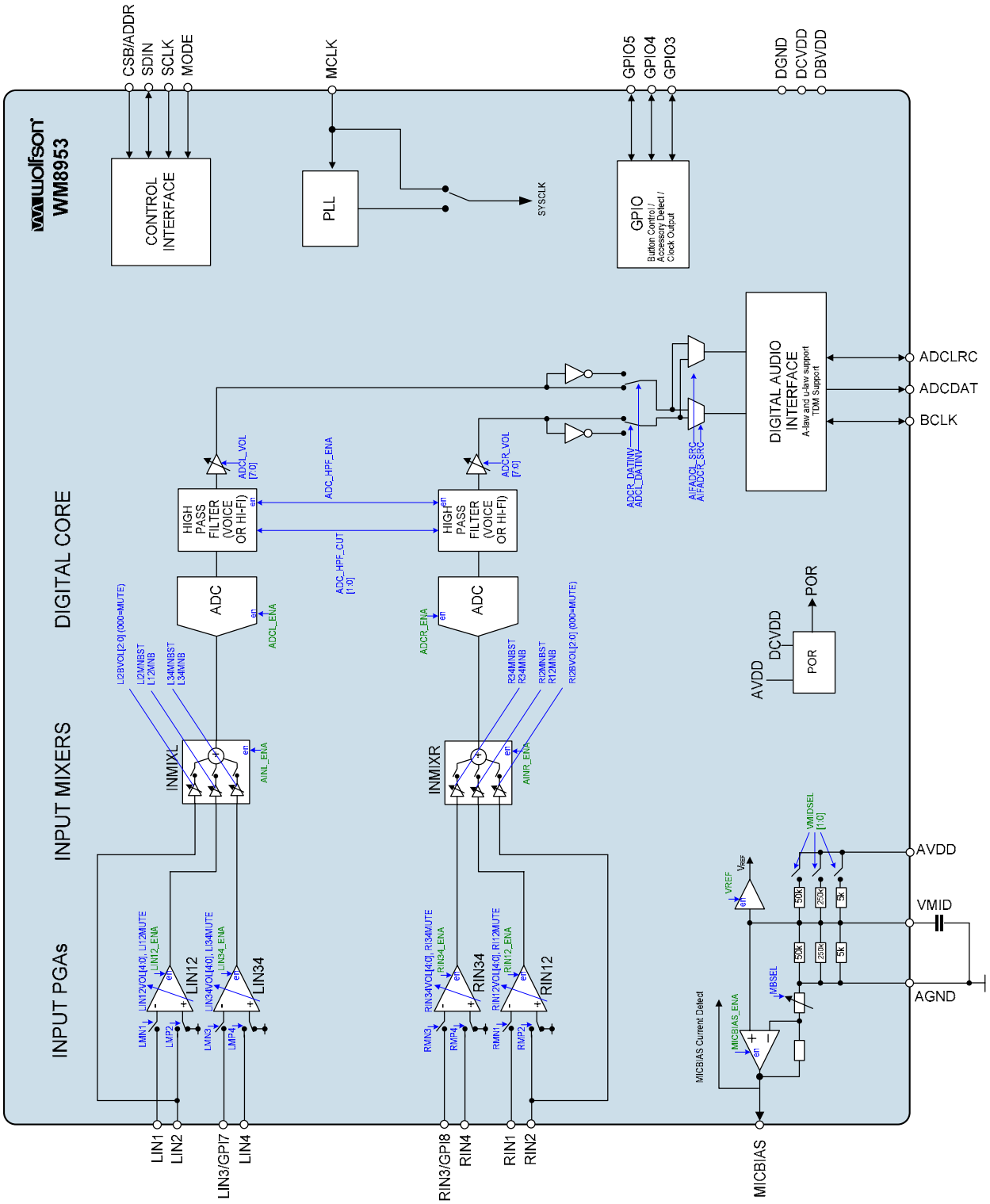


AVDD – MICBIAS



Note: All figures based on 100mVp-p injected on the supply at the relevant test frequency.

AUDIO SIGNAL PATHS



SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

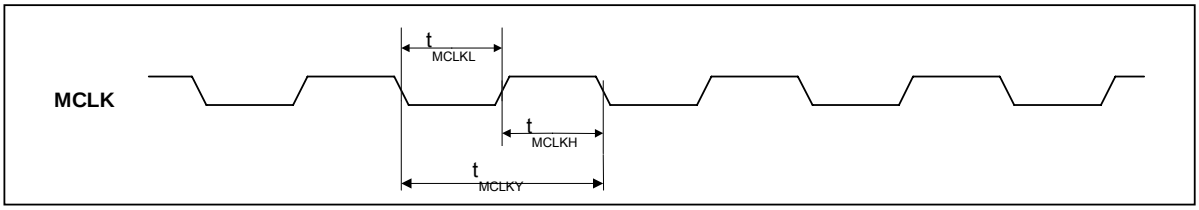


Figure 2 System Clock Timing Requirements

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}		33.33			ns
MCLK duty cycle		= T_{MCLKH}/T_{MCLKL}	60:40		40:60	

AUDIO INTERFACE TIMING – MASTER MODE

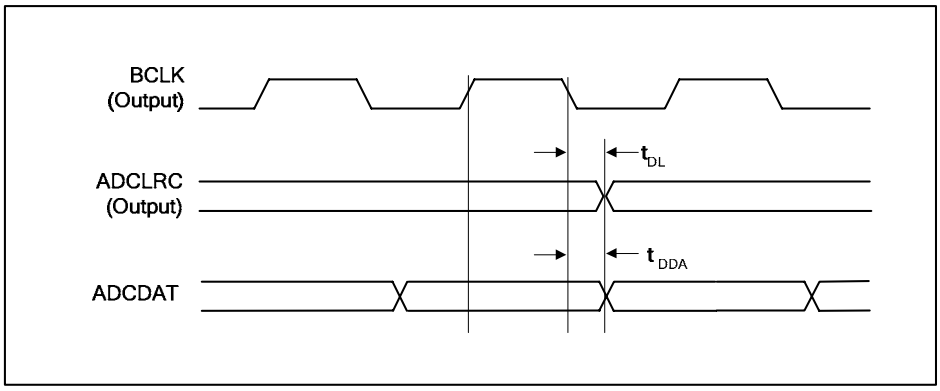


Figure 3 Digital Audio Data Timing - Master Mode (see Control Interface)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
ADCLRC propagation delay from BCLK falling edge	t_{DL}			20	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			20	ns

AUDIO INTERFACE TIMING – SLAVE MODE

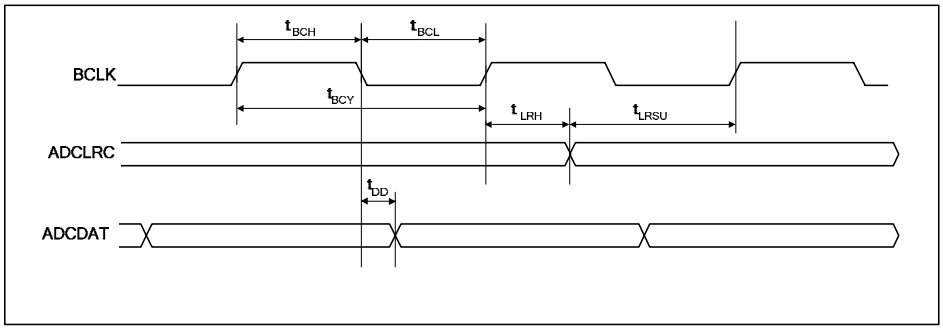


Figure 4 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
ADCLRC set-up time to BCLK rising edge	t_{LRSU}	20			ns
ADCLRC hold time from rising edge	t_{LRH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

AUDIO INTERFACE TIMING – TDM MODE

In TDM mode, it is important that two ADC devices to not attempt to drive the ADCDAT pin simultaneously. The timing of the WM8953 ADCDAT tri-stating at the start and end of the data transmission is described in Figure 5 and the table below.

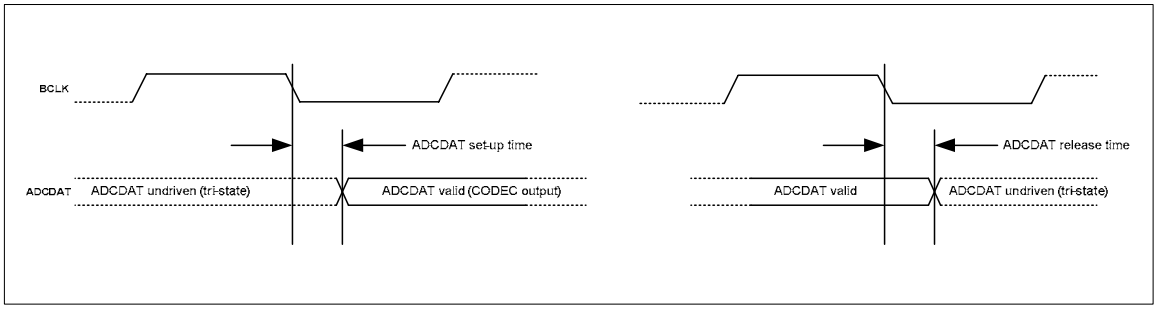


Figure 5 Digital Audio Data Timing - TDM Mode

Test Conditions

AVDD=3.3V, DGND=AGND=0V, T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
ADCDAT setup time from BCLK falling edge	DCVDD = DBVDD = 3.6V		5		ns
	DCVDD = DBVDD = 1.71V		15		ns
ADCDAT release time from BCLK falling edge	DCVDD = DBVDD = 3.6V		5		ns
	DCVDD = DBVDD = 1.71V		15		ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

2-wire mode is selected by connecting the MODE pin low.

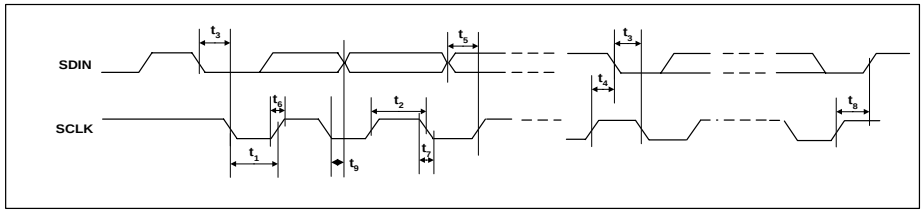


Figure 6 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 3-WIRE MODE

3-wire mode is selected by connecting the MODE pin high.

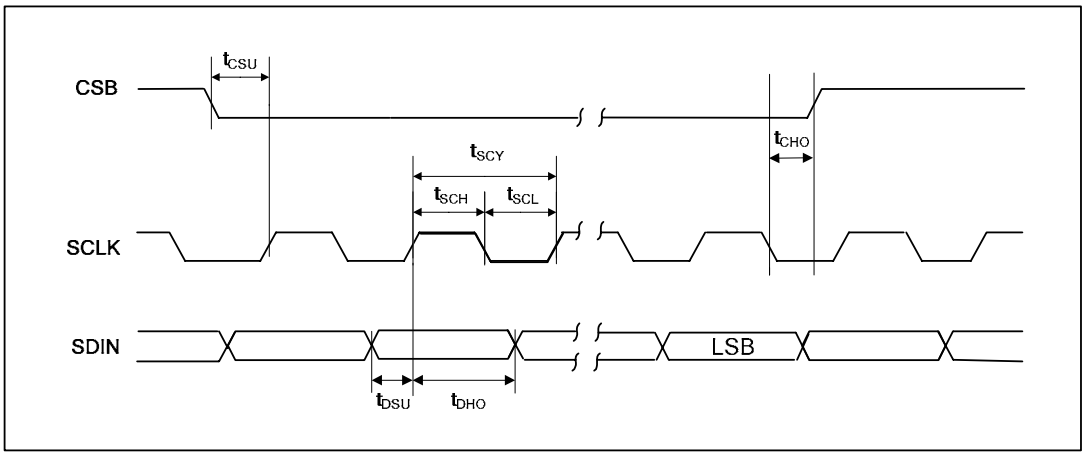


Figure 7 Control Interface Timing – 3-Wire Serial Control Mode (Write Cycle)

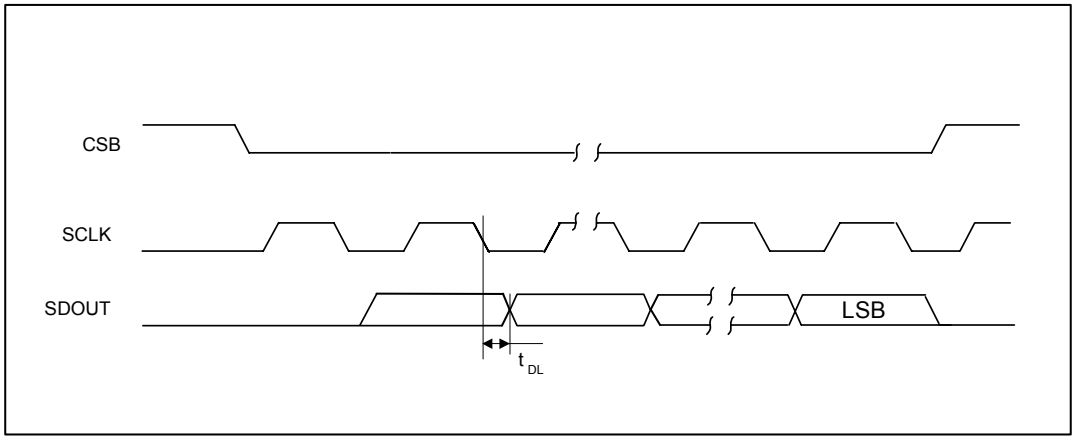


Figure 8 Control Interface Timing – 3-Wire Serial Control Mode (Read Cycle)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
CSB falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK falling edge to CSB rising edge	t_{CHO}	40			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SDIN to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

CONTROL INTERFACE TIMING – 4-WIRE MODE

4-wire mode supports readback via SDOUT which is available as a GPIO pin function.

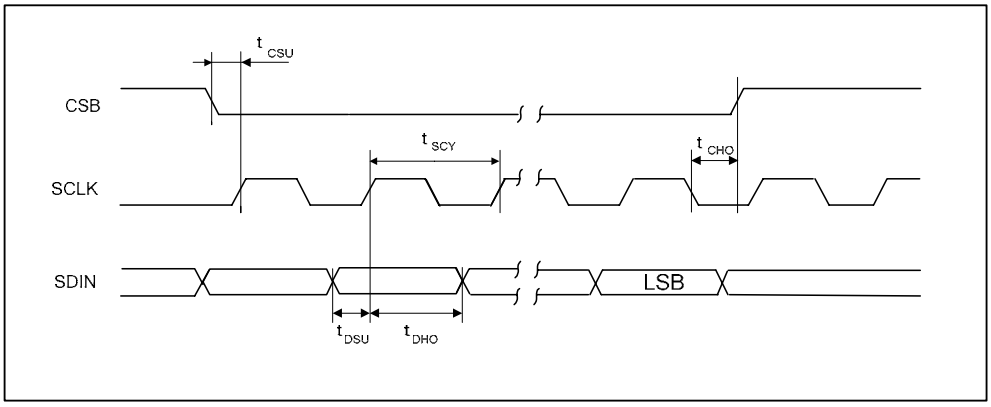


Figure 9 Control Interface Timing – 4-Wire Serial Control Mode (Write Cycle)

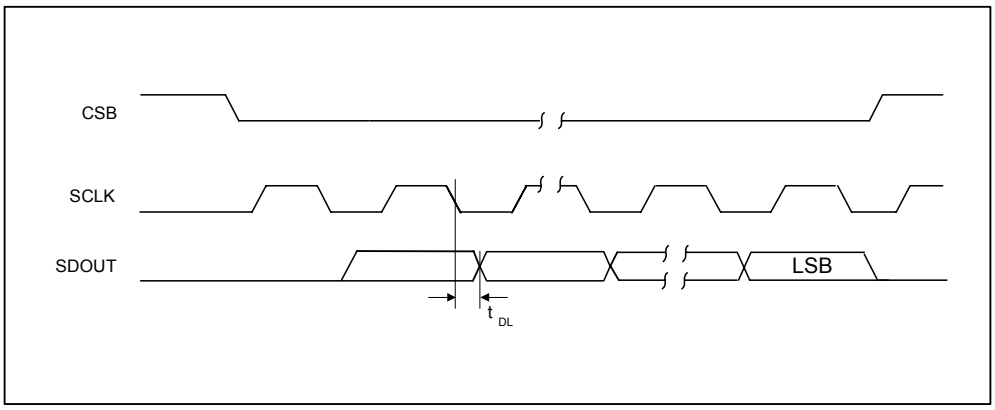


Figure 10 Control Interface Timing – 4-Wire Serial Control Mode (Read Cycle)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A =+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB falling edge	t_{CSU}	40			ns
SCLK falling edge to CSB rising edge	t_{CHO}	40			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SDIN to SCLK hold time	t_{DHO}	10			ns
SDOUT propagation delay from SCLK rising edge	t_{DL}			10	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

INTERNAL POWER ON RESET CIRCUIT

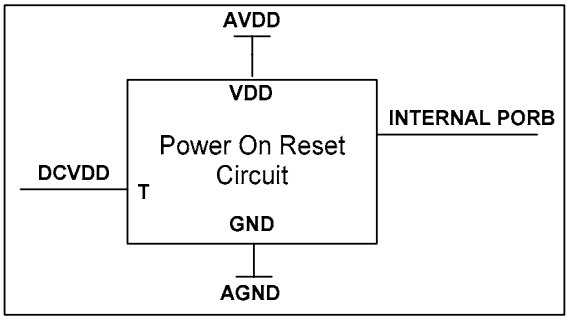


Figure 11 Internal Power on Reset Circuit Schematic

The WM8953 includes an internal Power-On-Reset Circuit, as shown in Figure 11, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DCVDD. It asserts PORB low if AVDD or DCVDD is below a minimum threshold.

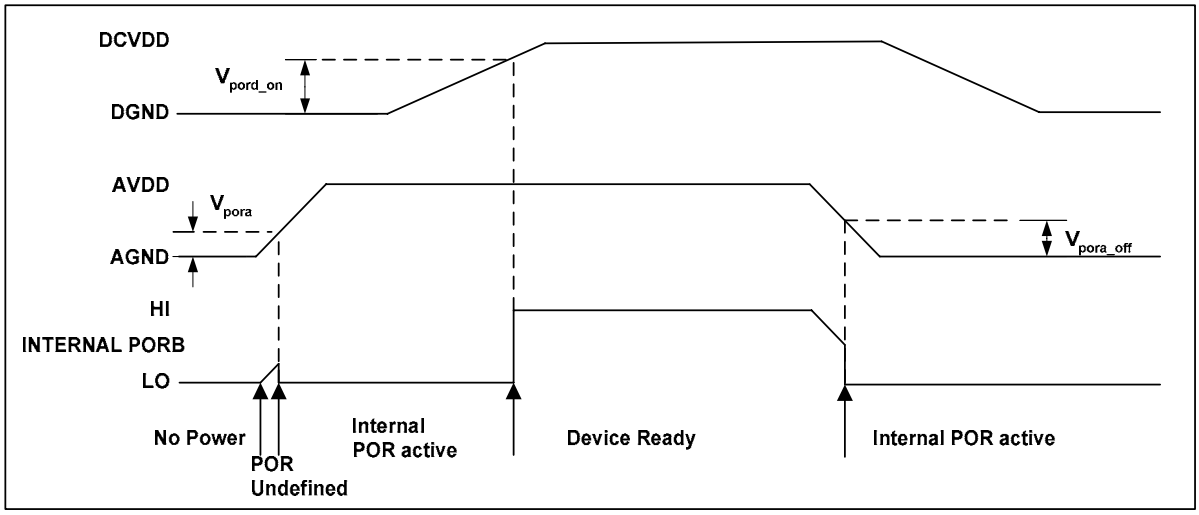


Figure 12 Typical Power up Sequence where AVDD is Powered before DCVDD

Figure 12 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DCVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold V_{pora_off}.

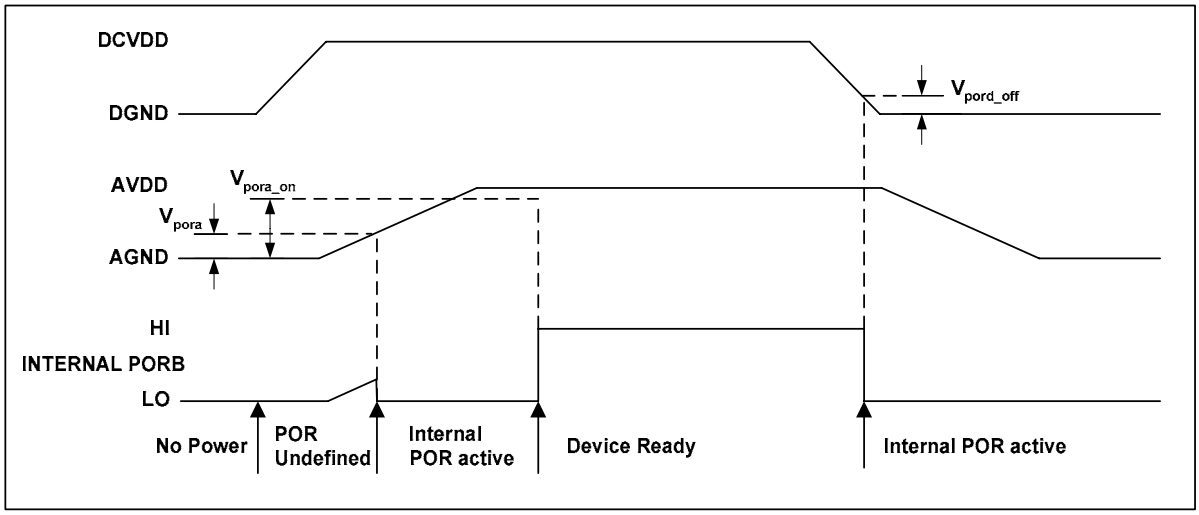


Figure 13 Typical Power up Sequence where DCVDD is Powered before AVDD

Figure 13 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
Vpora		0.6		V
Vpora_on		1.52		V
Vpora_off		1.5		V
Vpord_on		0.92		V
Vpord_off		0.9		V

Table 1 Typical POR Operation (typical values, not tested)

Notes:

1. If AVDD and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.
2. The chip will enter reset at power down when AVDD or DCVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.
3. The minimum t_{por} period is maintained even if DCVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

DEVICE DESCRIPTION

INTRODUCTION

The WM8953 is a low power, high quality audio ADC designed to interface with a wide range of processors and analogue components. A high level of mixed-signal integration in a very small 3.226x3.44mm footprint makes it ideal for portable applications such as mobile phones.

Eight highly flexible analogue inputs allow interfacing to up to four microphone inputs plus multiple stereo or mono line inputs (single-ended or differential).

The stereo ADCs are of hi-fi quality using a 24-bit, low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports a wide variety of clock inputs and sample rates; the integrated ultra-low power PLL provides additional flexibility. A high pass filter is available in the ADC path for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise.

The WM8953 has a highly flexible digital audio interface, supporting a number of protocols, including I^2S, DSP, MSB-first left/right justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and μ-law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power.

The SYSCLK (system clock) provides clocking for the ADCs, DSP core and the digital audio interface. SYSCLK can be derived directly from the MCLK pin or via an integrated PLL, providing flexibility to support a wide range of clocking schemes. All MCLK frequencies typically used in portable systems are supported for sample rates between 8kHz and 48kHz.

To allow full software control over all its features, the WM8953 uses a standard 2-wire or 3/4-wire control interface with readback of key registers supported. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled via software to save power, while low leakage currents extend standby and off time in portable battery-powered applications. The device address can be selected using the CSB/ADDR pin.

Versatile GPIO functionality is provided, with support for up to five button/accessory detect inputs with interrupt and status readback and flexible de-bouncing options, clock output, and logic '1' / logic '0' for control of additional external circuitry.

INPUT SIGNAL PATH

The WM8953 has eight highly flexible analogue input channels, configurable in many combinations of the following:

1. Up to four pseudo-differential or single-ended microphone inputs

2. Up to eight mono line inputs or 4 stereo line inputs

The input paths are mixed together as illustrated in Figure 14.

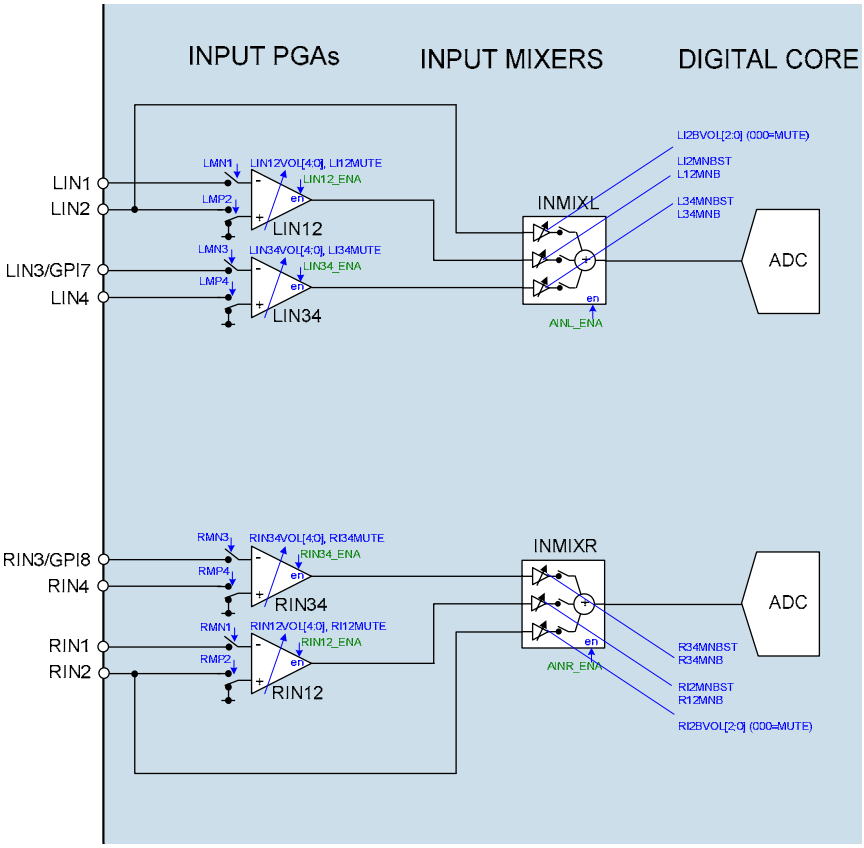


Figure 14 Control Registers for Input Signal Path

MICROPHONE INPUTS

Up to four microphones can be connected to the WM8953, either in single-ended or pseudo-differential mode. A low noise microphone bias is fully integrated to reduce the need for external components.

In single-ended microphone input configuration, the microphone signal is connected to the inverting input of the PGA (LIN1, LIN3, RIN1 or RIN3). The non-inverting input of the PGAs should be internally connected to VMID in this configuration. This is enabled via the Input PGA configuration register settings. In this configuration, LIN2, LIN4, RIN2 or RIN4 may be free to be used as line inputs.

In pseudo-differential microphone input configuration, the non-inverted microphone signal is connected to the non-inverting input of the PGA (LIN2, LIN4, RIN2 or RIN4) and the inverted (or noisy ground) signal is connected to the inverting input (LIN1, LIN3, RIN1 or RIN3).

Any PGA input pin that is used in either microphone configuration should not be enabled as a line input path at the same time.

The gain of the input PGAs is controlled via register settings. Note that the input impedance of LIN1, LIN3, RIN1 and RIN3 changes with the input PGA gain setting, as described under “Electrical Characteristics”. (Note this does not apply to input paths which bypass the input PGA.) The input impedance of LIN2, LIN4, RIN2 and RIN4 does not change with input PGA gain. The inverting and non-inverting inputs are therefore not matched and the differential configuration is not fully differential.

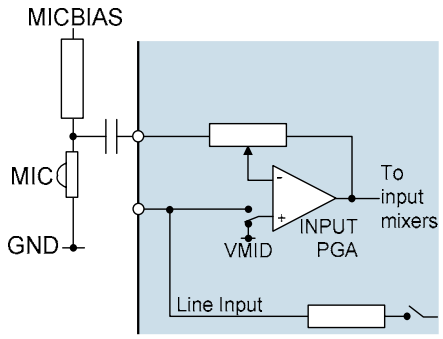


Figure 15 Single-Ended Microphone Input

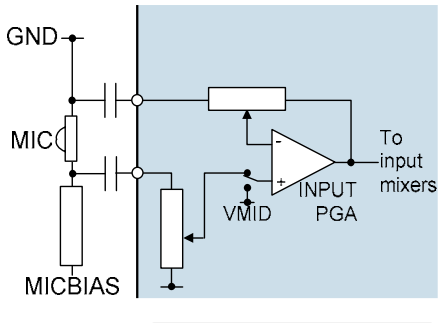


Figure 16 Differential Microphone Input

LINE INPUTS

All eight analogue input pins may be configured as line inputs with up to six single-ended inputs available, and up to four pseudo differential inputs.

LIN1, LIN3, RIN1 and RIN3 can operate as single-ended line inputs to the Input PGAs to provide high gain if required for small input signals. In this configuration the non-inverting input of the PGAs should be internally connected to Vmid.

LIN2 and RIN2 can operate as line inputs to the Input PGAs LIN12 and RIN12 or directly to the input mixers. Direct routing to the mixers minimises power consumption by reducing the number of active amplifiers in the signal path.

LIN4 and RIN4 should only be used as part of a differential line input with LIN3 and LIN4. Up to four differential line inputs can be connected to LIN1+LIN2, LIN3+LIN4, RIN1+RIN2 and RIN3+RIN4.

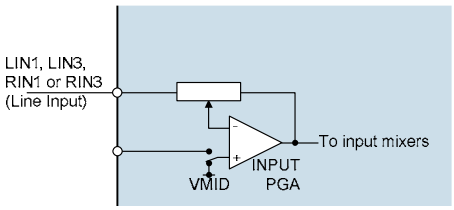


Figure 17 LIN1, RIN1, LIN3 or RIN3 as Line Inputs

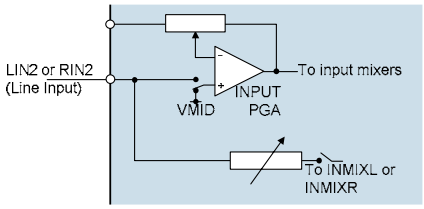


Figure 18 LIN2 or RIN2 as Line Inputs

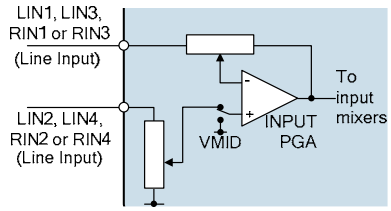


Figure 19 Differential Line Inputs

INPUT PGA ENABLE

The Input PGAs are enabled using register bits LIN12_ENA, LIN34_ENA, RIN12_ENA and RIN34_ENA as described in Table 2.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h)	7	LIN34_ENA (rw)	0b	LIN34 Input PGA Enable 0 = disabled 1 = enabled
	6	LIN12_ENA (rw)	0b	LIN12 Input PGA Enable 0 = disabled 1 = enabled
	5	RIN34_ENA (rw)	0b	RIN34 Input PGA Enable 0 = disabled 1 = enabled
	4	RIN12_ENA (rw)	0b	RIN12 Input PGA Enable 0 = disabled 1 = enabled

Table 2 Input PGA Enable

REFERENCE VOLTAGES

The analogue circuits in the WM8953 are referenced to VMID (AVDD/2). This voltage is generated from AVDD via a programmable resistor chain as shown in the audio signal paths diagram on page 15. Together with the external decoupling capacitor on VMID, the programmable resistor chain results in a slow, normal or fast charging characteristic on VMID. The VMID reference is controlled by VMID_MODE[1:0].

The analogue circuits in the WM8953 require a bias current. The bias current is enabled by setting VREF_ENA. Note that the bias current source requires VMID to be enabled also.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h)	2:1	VMID_MODE [1:0] (rw)	00b	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50kΩ divider (Normal mode) 10 = 2 x 250kΩ divider (Standby mode) 11 = 2 x 5kΩ divider (for fast start-up)
	0	VREF_ENA (rw)	0b	VREF Enable (Bias for all analogue functions) 0 = VREF bias disabled 1 = VREF bias enabled

Table 3 Reference Voltages

MICROPHONE BIAS CONTROL

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones via an external resistor. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be enabled or disabled using the MICBIAS_ENA control bit and the voltage can be selected using the MBSEL register bit as detailed in Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h)	4	MICBIAS_ENA (rw)	0b	Microphone Bias 0 = OFF (high impedance output) 1 = ON
R58 (3Ah)	0	MBSEL	0b	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD

Table 4 Microphone Bias Control

Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistance must be large enough to limit the MICBIAS current to 3mA.

MICROPHONE CURRENT DETECT

A MICBIAS current detect function allows detection of accessories such as headset microphones. When the MICBIAS load current exceeds one of two programmable thresholds, (e.g. short circuit current or normal operating current), an interrupt or GPIO output can be generated. The current detection circuit is enabled by the MCD bit; the current thresholds are selected by the MCDTHR and MCDSCTH register fields as described in Table 24- see “General Purpose Input/Output” for a full description of these fields.

DISABLED INPUT CONTROL

After start-up, it may be desirable to disable an input stage, in order to reduce power consumption on an unused PGA or Input Mixer.

In order to avoid audible pops caused by a disabling any part of the input circuits, the WM8953 can maintain the input at VMID even when the PGA or Input Mixer is disabled. This is achieved by connecting a buffered VMID reference to the input. The buffered VMID is enabled by setting BUFIOEN.

When BUFIOEN is enabled, the WM8953 maintains the charge on the input capacitors connected to any disabled input amplifier. This suppresses the audible artefacts that would otherwise arise when an input amplifier is disabled or enabled. In some applications, a pop generated at an input stage can be entirely suppressed by correctly managing the output stages (eg. using the ADC mute). However, it may be desirable to use the buffered VMID feature in order to eliminate the input PGA start-up delay (the input capacitor charging time) in addition to suppressing any mute/un-mute pops. In applications where frequent enabling and configuration of signal paths is used, it is recommended to enable BUFIOEN at all times.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R57 (39h) Anti-Pop	3	BUFIOEN	0b	Enables the Buffered VMID reference at disabled inputs 0 = Disabled 1 = Enabled

Table 5 Disabled Input/Output Control

INPUT PGA CONFIGURATION

Each of the four Input PGAs can be configured in single-ended or pseudo-differential mode.

Single-ended microphone operation of an Input PGA is selected by connecting the input source to the inverting PGA input. The non-inverting PGA input must be connected to VMID by setting the appropriate register bits.

For pseudo-differential microphone operation, the inverting and non-inverting PGA inputs are both connected to the input source and not to VMID.

For any line input or other connection not using the Input PGA, the appropriate PGA input should be disconnected from the external pin and connected to VMID.

Register bits LMN1, LMP2, LMN3, LMP4, RMN1, RMP2, RMN3 and RMP4 control connection of the PGA inputs to the device pins as shown in Table 6. The maximum available attenuation on any of these input paths is achieved using these bits to disable the input path to the applicable PGA.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h)	7	LMP4	0b	LIN34 PGA Non-Inverting Input Select 0 = LIN4 not connected to PGA 1 = LIN4 connected to PGA
	6	LMN3	0b	LIN34 PGA Inverting Input Select 0 = LIN3 not connected to PGA 1 = LIN3 connected to PGA
	5	LMP2	0b	LIN12 PGA Non-Inverting Input Select 0 = LIN2 not connected to PGA 1 = LIN2 connected to PGA
	4	LMN1	0b	LIN12 PGA Inverting Input Select 0 = LIN1 not connected to PGA 1 = LIN1 connected to PGA
	3	RMP4	0b	RIN34 PGA Non-Inverting Input Select 0 = RIN4 not connected to PGA 1 = RIN4 connected to PGA
	2	RMN3	0b	RIN34 PGA Inverting Input Select 0 = RIN3 not connected to PGA 1 = RIN3 connected to PGA
	1	RMP2	0b	RIN12 PGA Non-Inverting Input Select 0 = RIN2 not connected to PGA 1 = RIN2 connected to PGA
	0	RMN1	0b	RIN12 PGA Inverting Input Select 0 = RIN1 not connected to PGA 1 = RIN1 connected to PGA

Table 6 Input PGA Configuration

INPUT PGA VOLUME CONTROL

Each of the four Input PGAs has an independently controlled gain range of -16.5dB to +30dB in 1.5dB steps. The gains on the inverting and non-inverting inputs to the PGAs are always equal. Each Input PGA can be independently muted using the PGA mute bits as described in Table 7, with specified mute attenuation achieved by simultaneously disconnecting the corresponding inputs described in Table 6.

To prevent "zipper noise", a zero-cross function is provided, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOCLK_ENA register bit), the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout period is set by TOCLK_RATE. See “Clocking and Sample Rates” for more information on these fields.

The IPVU bit controls the loading of the input PGA volume data. When IPVU is set to 0, the PGA volume data will be loaded into the respective control register, but will not actually change the gain setting. The LIN12, RIN12, LIN34, RIN34 volume settings are all updated when a 1 is written to IPVU. This makes it possible to update the gain of all input paths simultaneously.

The Input PGA Volume Control register fields are described in Table 7 and Table 8.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h)	8	IPVU[0]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	LI12MUTE	1b	LIN12 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	LI12ZC	0b	LIN12 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	LIN12VOL [4:0]	01011b (0dB)	LIN12 Volume (See Table 8 for volume range)
R25 (19h)	8	IPVU[1]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	LI34MUTE	1b	LIN34 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	LI34ZC	0b	LIN34 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	LIN34VOL [4:0]	01011b (0dB)	LIN34 Volume (See Table 8 for volume range)
R26 (1Ah)	8	IPVU[2]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	RI12MUTE	1b	RIN12 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	RI12ZC	0b	RIN12 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4:0	RIN12VOL [4:0]	01011b (0dB)	RIN12 Volume (See Table 8 for volume range)
R27 (1Bh)	8	IPVU[3]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	RI34MUTE	1b	RIN34 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	RI34ZC	0b	RIN34 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	RIN34VOL [4:0]	01011b (0dB)	RIN34 Volume (See Table 8 for volume range)

Table 7 Input PGA Volume Control

LIN12VOL[4:0], LIN34VOL[4:0], RIN12VOL[4:0], RIN34VOL[4:0]	VOLUME (DB)
00000	-16.5
00001	-15.0
00010	-13.5
00011	-12.0
00100	-10.5
00101	-9.0
00110	-7.5
00111	-6.0
01000	-4.5
01001	-3.0
01010	-1.5
01011	0
01100	+1.5
01101	+3.0
01110	+4.5
01111	+6.0
10000	+7.5
10001	+9.0
10010	+10.5
10011	+12.0
10100	+13.5
10101	+15.0
10110	+16.5
10111	+18.0
11000	+19.5
11001	+21.0
11010	+22.5
11011	+24.0
11100	+25.5
11101	+27.0
11110	+28.5
11111	+30.0

Table 8 Input PGA Volume Range

INPUT MIXER ENABLE

The WM8953 has two analogue input mixers which allow the Input PGAs and Line Inputs to be combined in a number of ways and output to the ADCs.

The input mixers INMIXL and INMIXR are enabled by the AINL_ENA and AINR_ENA register bits, as described in Table 9.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h)	9	AINL_ENA (rw)	0b	Left Input Path Enable 0 = Input Path disabled 1 = Input Path enabled
	8	AINR_ENA (rw)	0b	Right Input Path Enable 0 = Input Path disabled 1 = Input Path enabled

Table 9 Input Mixer Enable

INPUT MIXER VOLUME CONTROL

The Input Mixer volume controls are described in Table 10 for the Left Channel and Table 11 for the Right Channel. The Input PGA levels may be set to Mute, 0dB or 30dB boost. The other gain controls provide adjustment from -12dB to +6dB in 3dB steps.

To prevent pop noise it is recommended that gain and mute controls for the input mixers are not modified while the signal paths are active. If volume control is required on the input signal path it is recommended that the input PGA volume controls or the ADC volume controls are used instead of the input mixer gain registers.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R41 (29h)	8	L34MNB	0b	LIN34 PGA Output to INMIXL Mute 0 = Mute 1 = Un-Mute
	7	L34MNBST	0b	LIN34 PGA Output to INMIXL Gain 0 = 0dB 1 = +30dB
	5	L12MNB	0b	LIN12 PGA Output to INMIXL Mute 0 = Mute 1 = Un-Mute
	4	L12MNBST	0b	LIN12 PGA Output to INMIXL Gain 0 = 0dB 1 = +30dB
R43 (2Bh)	8:6	LI2BVOL [2:0]	000b (Mute)	LIN2 Pin to INMIXL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB

Table 10 Left Input Mixer Volume Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2A)	8	R34MNB	0b	RIN34 PGA Output to INMIXR Mute 0 = Mute 1 = Un-Mute
	7	R34MNBST	0b	RIN34 PGA Output to INMIXR Gain 0 = 0dB 1 = +30dB
	5	R12MNB	0b	RIN12 PGA Output to INMIXR Mute 0 = Mute 1 = Un-Mute
	4	R12MNBST	0b	RIN12 PGA Output to INMIXR Gain 0 = 0dB 1 = +30dB
R44 (2Ch)	8:6	RI2BVOL [2:0]	000b (Mute)	RIN2 Pin to INMIXR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB

Table 11 Right Input Mixer Volume Control

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8953 uses stereo 24-bit, 64x oversampled sigma-delta ADCs. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC full scale input level is proportional to AVDD. See "Electrical Characteristics" for further details. Any input signal greater than full scale may overload the ADC and cause distortion.

The ADCs are enabled by the ADCL_ENA and ADCR_ENA register bits. If both ADCs are to be enabled, they should be enabled simultaneously, i.e. with the same register write. If there is a requirement to enable the ADCs independently of one another and use them simultaneously, the ADCL_ADCR_LINK bit should be set. The EXT_ACCESS_ENA bit must be set before writing to the ADCL_ADCR_LINK bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h)	1	ADCL_ENA (rw)	0b	Left ADC Enable 0 = ADC disabled 1 = ADC enabled
	0	ADCR_ENA (rw)	0b	Right ADC Enable 0 = ADC disabled 1 = ADC enabled
R117 (75h)	1	EXT_ACCESS_ENA	0b	Extended Register Map Access 0 = disabled 1 = enabled
R122 (7Ah)	15	ADCL_ADCR_LINK	0b	0 = ADC Sync disabled 1 = ADC Sync enabled

Table 12 ADC Enable Control

ADC DIGITAL VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from -71.625dB to +17.625dB in 0.375dB steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 239$; MUTE for $X = 0$ +17.625dB for $239 \leq X \leq 255$

The ADC_VU bit controls the loading of digital volume control data. When ADC_VU is set to 0, the ADCL_VOL or ADCR_VOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to ADC_VU. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 (0Fh)	8	ADC_VU	N/A	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCL_VOL [7:0]	1100_0000b (0dB)	Left ADC Digital Volume (See Table 14 for volume range)
R16 (10h)	8	ADC_VU	N/A	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCR_VOL [7:0]	1100_0000b (0dB)	Right ADC Digital Volume (See Table 14 for volume range)

Table 13 ADC Digital Volume Control

ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.375
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.750
3h	-70.875	43h	-46.875	83h	-22.875	C3h	1.125
4h	-70.500	44h	-46.500	84h	-22.500	C4h	1.500
5h	-70.125	45h	-46.125	85h	-22.125	C5h	1.875
6h	-69.750	46h	-45.750	86h	-21.750	C6h	2.250
7h	-69.375	47h	-45.375	87h	-21.375	C7h	2.625
8h	-69.000	48h	-45.000	88h	-21.000	C8h	3.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	3.375
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	3.750
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	4.125
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	4.500
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	4.875
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	5.250
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	5.625
10h	-66.000	50h	-42.000	90h	-18.000	D0h	6.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	6.375
12h	-65.250	52h	-41.250	92h	-17.250	D2h	6.750
13h	-64.875	53h	-40.875	93h	-16.875	D3h	7.125
14h	-64.500	54h	-40.500	94h	-16.500	D4h	7.500
15h	-64.125	55h	-40.125	95h	-16.125	D5h	7.875
16h	-63.750	56h	-39.750	96h	-15.750	D6h	8.250
17h	-63.375	57h	-39.375	97h	-15.375	D7h	8.625
18h	-63.000	58h	-39.000	98h	-15.000	D8h	9.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	9.375
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	9.750
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	10.125
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	10.500
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	10.875
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	11.250
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	11.625
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	12.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	12.375
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	12.750
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	13.125
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	13.500
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	13.875
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	14.250
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	14.625
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	15.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	15.375
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	15.750
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	16.125
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	16.500
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	16.875
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	17.250
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	17.625
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	17.625
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	17.625
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	17.625
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	17.625
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	17.625
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	17.625
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	17.625
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	17.625
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	17.625
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	17.625
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	17.625
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	17.625
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	17.625
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	17.625
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	17.625
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	17.625

Table 14 ADC Digital Volume Range

HIGH PASS FILTER

A digital high pass filter is applied by default to the ADC path to remove DC offsets. This filter can also be programmed to remove low frequency noise in voice applications (e.g. wind noise or mechanical vibration). This filter is controlled using the ADC_HPF_ENA and ADC_HPF_CUT register bits.

In hi-fi mode the high pass filter is optimised for removing DC offsets without degrading the bass response and has a cut-off frequency of 3.7Hz at fs=44.1kHz.

In voice mode the high pass filter is optimised for voice communication and it is recommended to program the cut-off frequency below 300Hz (e.g. ADC_HPF_CUT=11 at fs=8kHz or ADC_HPF_CUT=10 at fs=16kHz).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 (0Eh)	8	ADC_HPF_ENA	1b	ADC Digital High Pass Filter Enable 0 = disabled 1 = enabled
	6:5	ADC_HPF_CUT [1:0]	00b	ADC Digital High Pass Filter Cut-Off Frequency (fc) 00 = Hi-fi mode (fc=4Hz at fs=48kHz) 01 = Voice mode 1 (fc=127Hz at fs=16kHz) 10 = Voice mode 2 (fc=130Hz at fs=8kHz) 11 = Voice mode 3 (fc=267Hz at fs=8kHz) (Note: fc scales with sample rate. See Table 16 for cut-off frequencies at all supported sample rates)

Table 15 ADC High Pass Filter Control Registers

Sample Frequency (kHz)	Cut-off frequency (Hz)			
	ADC_HPF_CUT =00	ADC_HPF_CUT =01	ADC_HPF_CUT =10	ADC_HPF_CUT =11
8.000	0.7	64	130	267
11.025	0.9	88	178	367
16.000	1.3	127	258	532
22.050	1.9	175	354	733
24.000	2.0	190	386	798
32.000	2.7	253	514	1063
44.100	3.7	348	707	1464
48.000	4.0	379	770	1594

Table 16 ADC High Pass Filter Cut-Off Frequencies

The high pass filter characteristics are shown in the "Digital Filter Characteristics" section.

DIGITAL AUDIO PATHS

The ADC data can be routed in different ways to the digital audio interface. Data from either of the two ADCs can be routed to either the left or the right channel of the digital audio interface. Independent functions enable either of the audio channels to be digitally inverted if required. See "Digital Audio Interface" for more information on the audio interface.

Figure 20 shows the digital audio paths available in the WM8953 digital core.

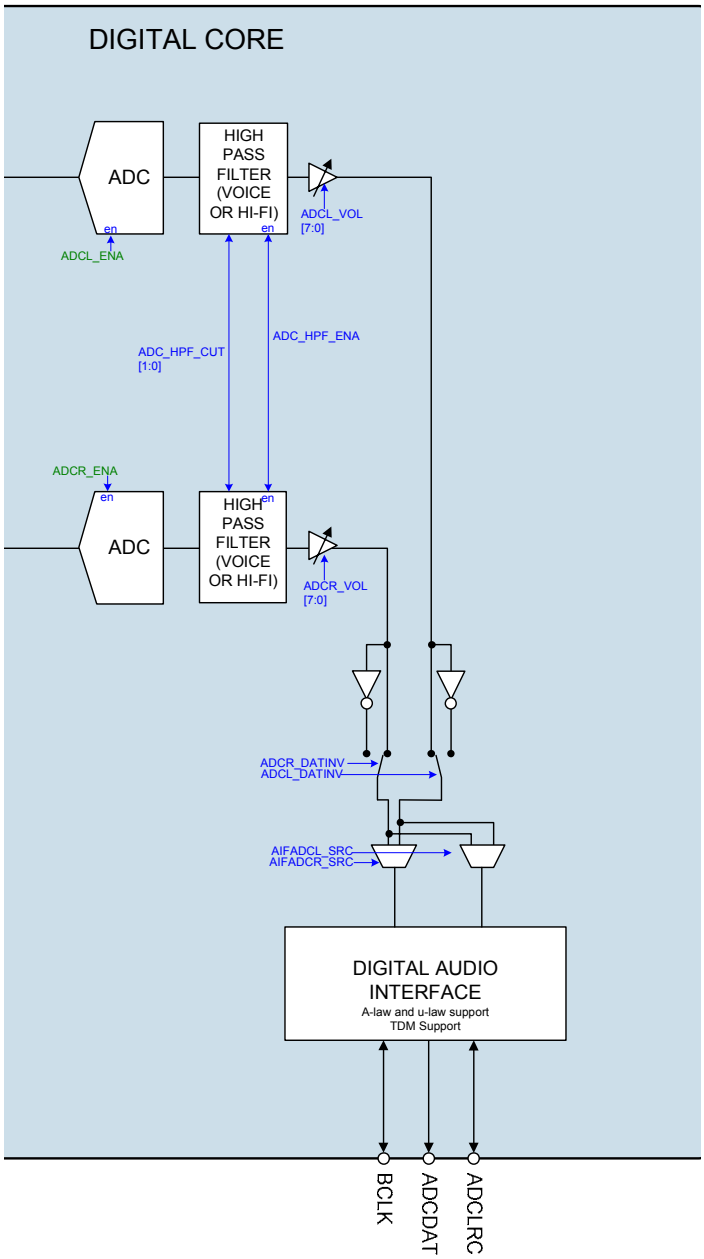


Figure 20 Digital Audio Paths

The polarity of each ADC output signal can be changed under software control using the ADCL_DATINV and ADCR_DATINV register bits. The AIFADCL_SRC and AIFADCR_SRC register bits may be used to select which ADC is used for the left and right digital audio interface data. These register bits are described in Table 17.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h)	15	AIFADCL_SRC	0b	Left Digital Audio channel source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel
	14	AIFADCR_SRC	1b	Right Digital Audio channel source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
R14 (0Eh)	1	ADCL_DATINV	0b	Left ADC Invert 0 = Left ADC output not inverted 1 = Left ADC output inverted
	0	ADCR_DATINV	0b	Right ADC Invert 0 = Right ADC output not inverted 1 = Right ADC output inverted

Table 17 ADC Routing and Control

THERMAL SENSING

The WM8953 incorporates a thermal sensor in order to provide protection from overheating. The sensor is enabled by setting TSHUT_ENA. The status of the thermal sensor can be output on a GPIO pin and/or read from the GPIO registers. Alternatively, the temperature sensor can be configured to cause an Interrupt event. See “General Purpose Input/Output” for further details.

Note that, if thermal shutdown is required, this must be implemented by the host processor, in response to the thermal status indication generated by the WM8953.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h)	14	TSHUT_ENA (rw)	1b	Thermal Sensor Enable 0 = Thermal sensor disabled 1 = Thermal sensor enabled

Table 18 Thermal Shutdown

GENERAL PURPOSE INPUT/OUTPUT

The WM8953 provides a number of versatile GPIO functions to enable features such as button and accessory detection and clock output.

The WM8953 has five multi-purpose pins for these functions.

- GPIO3, GPIO4 and GPIO5: Dedicated GPIO pins.
- LIN3/GPI7 and RIN3/GPI8: Analogue inputs or button/accessory detect inputs.

The following functions are available on some or all of the GPIO pins.

- Button detect (latched with programmable de-bounce)
- MICBIAS / Accessory current or short circuit detect
- Clock output
- Temperature sensor output
- PLL lock output
- Logic '1' and logic '0' output
- Interrupt event output
- Serial data output (register readback)

The functions available on each of the GPIO pins are identified in Table 19.

	GPIO PINS				
GPIO Pin Function	**GPIO3**	**GPIO4**	**GPIO5**	**GPI7**	**GPI8**
Button/Accessory Detect Input	Y	Y	Y	Y	Y
Clock Output	Y	Y	Y		
Temperature OK	Y	Y	Y		
PLL Lock	Y	Y	Y		
Logic 1 and Logic 0	Y	Y	Y		
Interrupt	Y	Y	Y		
SDOUT (Readback Data)	Y	Y	Y		
Pull-up and Pull-down Available	Y	Y	Y		

Table 19 Functions Available on GPIO Pins

The GPIO pins are configured by a combination of register settings described in Table 20 to Table 23 in the following section. The order of precedence for the control of the GPIO pins is as listed below.

1. Pin pull-up or pull-down (GPIOn_PU, GPIOn_PD)
2. Audio Interface and GPIO Tristate (AIF_TRIS)
3. GPIO functionality (GPIOn_SEL)

GPIO CONTROL REGISTERS

Register bit AIF_TRIS, when set, tri-states all audio interface and GPIO pins.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h)	13	AIF_TRIS	0b	Audio Interface and GPIO Tristate 0 = Audio interface and GPIO pins operate normally 1 = Tristate all audio interface and GPIO pins

Table 20 GPIO and GPI Pin Function Select

The GPIO pins are also controlled by the register fields described in Table 21. Note the order of precedence described earlier applies.

Pull-up and pull-down resistors may be enabled on any of GPIO3, GPIO4 or GPIO5. If enabled, these settings take precedence over all other GPIO selections for that pin. Note that, by default, the pull-down resistors on GPIO3, GPIO4 and GPIO5 are enabled.

When the GPIO pins are used as inputs, de-bounce and interrupt masking may be controlled on all GPIO pins (including GPI7 and GPI8) using GPIOn_DEB_ENA and GPIOn_IRQ_ENA bits as shown in Table 22.

For each of GPIO3, GPIO4 and GPIO5, the register field GPIOn_SEL is used to select the pin functions of the individual GPIO pins as shown in Table 22. Note that this control has the lowest precedence and is only effective when GPIOn_PU, GPIOn_PD and AIF_TRIS are set to allow GPIO functionality on that GPIO pin.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h)	15	GPIO4_DEB_ENA	0b	See Table 22 for GPIO4 control bit description
	14	GPIO4_IRQ_ENA	0b	
	13	GPIO4_PU	0b	
	12	GPIO4_PD	1b	
	11:8	GPIO4_SEL[3:0]	0000b	
	7	GPIO3_DEB_ENA	0b	See Table 22 for GPIO3 control bit description
	6	GPIO3_IRQ_ENA	0b	
	5	GPIO3_PU	0b	
	4	GPIO3_PD	1b	
	3:0	GPIO3_SEL[3:0]	0000b	
R21 (15h)	7	GPIO5_DEB_ENA	0b	See Table 22 for GPIO5 control bit description
	6	GPIO5_IRQ_ENA	0b	
	5	GPIO5_PU	0b	
	4	GPIO5_PD	1b	
	3:0	GPIO5_SEL[3:0]	0000b	
R22 (16h)	7	GPI8_DEB_ENA	0b	See Table 22 for GPIn control bit description
	6	GPI8_IRQ_ENA	0b	
	4	GPI8_ENA	0b	
	3	GPI7_DEB_ENA	0b	See Table 22 for GPIn control bit description
	2	GPI7_IRQ_ENA	0b	
	0	GPI7_ENA	0b	

Table 21 GPIO and GPI Control

The following table describes the coding of the fields listed in Table 21.

REGISTER ADDRESS	LABEL	DEFAULT	DESCRIPTION
Registers R20 (14h) to R21 (15h) (See Table 21)	GPIOn_DEB_ENA (n = 3, 4, 5, 7, 8)	0b	De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA = 1)
	GPIOn_IRQ_ENA (n = 3, 4, 5, 7, 8)	0b	IRQ Enable 0 = disabled 1 = enabled
	GPIOn_PU (n = 3, 4, 5)	0b	GPIO Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	GPIOn_PD (n = 3, 4, 5)	See Table 21	GPIO Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)
	GPIOn_SEL[3:0] (n = 3, 4, 5)	0000b	GPIOn Pin Function Select 0000 = Input pin 0001 = Clock output (SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = PLL Lock output 0101 = Temperature OK output 0110 = SDOUT data output 0111 = IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 to 1111 = Reserved
	GPIn_ENA (n = 7, 8)	0b	GPIn Input Pin Enable 0 = pin disabled as GPIn input 1 = pin enabled as GPIn input

Table 22 GPIO Function Control Bits

The polarity of GPIO/GPI inputs may be configured using the GPIO_POL register bits. This is described in Table 23.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h)	7:0	GPIO_POL [7:0] (rw)	00h	GPIOn Input Polarity 0 = Non-inverted 1 = Inverted GPIO_POL[7] = GPI8 polarity GPIO_POL[6] = GPI7 polarity GPIO_POL[5] = Reserved GPIO_POL[4] = GPIO5 polarity GPIO_POL[3] = GPIO4 polarity GPIO_POL[2] = GPIO3 polarity GPIO_POL[1] = Reserved GPIO_POL[0] = Reserved

Table 23 GPIO Polarity

Each of the available GPIO functions is described in turn in the following sections.

BUTTON CONTROL

The WM8953 GPIO supports button control detection with full status readback for up to four inputs (and one IRQ output). All inputs are latched at the IRQ Register, with de-bounce available for normal operation. De-bouncing may be disabled in order to allow the device to respond to wake-up events while the processor is disabled and is unable to provide a clock for de-bouncing.

To enable button control and accessory detection, the following register settings are required:

- LMN3 = 0 (only required if using GPI7)
- RMN3 = 0 (only required if using GPI8)
- AIF_TRIS = 0
- GPIOn_SEL = 0000 for each required GPIO button input

Programmable pull-up and pull-down resistors are available on GPIO3, GPIO4 and GPIO5. These should be set according to the external circuit configuration. Note that pull-up and pull-down resistors are not available on the GPI7 and GPI8 input pins. Note that the analogue input paths to GPI7 and GPI8 must be disabled as described above when using these as digital inputs.

In this application, one or more of the GPIO pins may be configured as an Interrupt event if desired. This is controlled by the GPIOn_IRQ_ENA bits described in Table 21. The GPIO Pin status fields contained in the IRQ Register (R18) may be read at any time or else in response to an Interrupt event. See Table 30 for more details of the Interrupt function.

An example configuration of the button control GPIO function is illustrated in Figure 21.

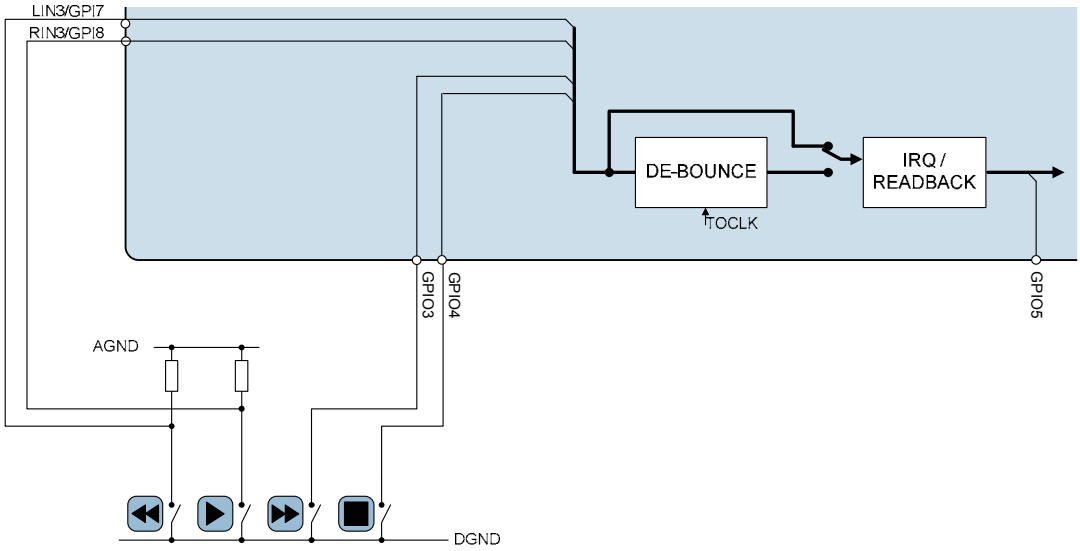


Figure 21 Example of Button Control Using GPIO Pins

Note:

- The GPIOs 3, 4, and 5 are referenced to DBVDD
- The GPIs 7 and 8 are referenced to AVDD

MICBIAS CURRENT AND ACCESSORY DETECT

A MICBIAS current detect function is provided for accessory detection. When a microphone current is detected (e.g. when a headset is inserted), an interrupt event can be generated and the microphone status read back via the control interface.

The MICBIAS current detect threshold is programmable. A short-circuit current detection is also available, with a programmable threshold. These functions are enabled by register bit MCD; the thresholds are programmable via register fields MCDTHR and MCDSCTR as shown in Table 24. Current detect and short circuit detect thresholds are subject to a +/- 30% temperature, supply and part-to-part variation. This should be factored into any application design.

The polarity of the current detect GPIO signals may be controlled by register bits MICDET_POL and MICSHRT_POL. Note that these polarity inversion bits apply to the Interrupt register behaviour only; they do not affect the direct GPIO output of the Current Detect functions. The respective interrupt events may be masked or enabled by register bits MICDET_IRQ_ENA and MICSHRT_IRQ_ENA. The MICBIAS current threshold status bits contained in the IRQ Register (R18) may be read at any time or else in response to an Interrupt event. See Table 30 for more details of the Interrupt function.

If direct output of the MICBIAS current detect function is required to the external pins of the WM8953, the following register settings are required:

- AIF_TRIS = 0
- GPIOn_SEL = 1000 for the selected GPIO MICBIAS Current Detect output pin
- GPIOn_SEL = 1001 for the selected GPIO MICBIAS Short Circuit Detect output pin
- GPIOn_PU = 0 for the selected GPIO MICBIAS output pin or pins
- GPIOn_PD = 0 for the selected GPIO MICBIAS output pin or pins

The register fields used to configure the MICBIAS Current Detect function are described in Table 24.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R58 (3Ah)	7:6	MCDSCTH [1:0]	00b	MICBIAS Short Circuit Detect Threshold 00 = 600uA 01 = 1200uA 10 = 1800uA 11 = 2400uA These values are for AVDD=3.3V and scale proportionally with AVDD.
	5:3	MCDTHR [2:0]	000b	MICBIAS Current Detect Threshold 000 = 200uA 001 = 350uA 010 = 500uA 011 = 650uA 100 = 800uA 101 = 950uA 110 = 1100uA 111 = 1250uA These values are for AVDD=3.3V and scale proportionally with AVDD.
	2	MCD	0b	MICBIAS Current and Short Circuit Detect Enable 0 = disabled 1 = enabled
R23 (17h)	10	MICSHRT_POL (rw)	0b	MICBIAS short circuit detect polarity 0 = Non-inverted 1 = Inverted
	9	MICDET_POL (rw)	0b	MICBIAS current detect polarity 0 = Non-inverted 1 = Inverted

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h)	10	MICSHRT_IRQ_ENA	0b	MICBIAS short circuit detect IRQ Enable 0 = disabled 1 = enabled
	9	MICDET_IRQ_ENA	0b	MICBIAS current detect IRQ Enable 0 = disabled 1 = enabled

Table 24 MICBIAS Current Detect Control

The current detect function operates according to the following the truth table:

LABEL	VALUE	DESCRIPTION
Mic Short Circuit Detect	0	MCDSCTH current threshold not exceeded
Mic Short Circuit Detect	1	MCDSCTH current threshold exceeded
Mic Current Detect	0	MCDTHR current threshold not exceeded
Mic Current Detect	1	MCDTHR current threshold exceeded

Table 25 Truth Table for GPIO Output of MICBIAS Current Detect Function

CLOCK OUTPUT

A clock output (OPCLK) derived from SYSCLK may be output via GPIO3, GPIO4 or GPIO5. SYSCLK is derived from MCLK (either directly, or in conjunction with the PLL), and is used to provide all internal clocking for the WM8953 (see "Clocking and Sample Rates" section for more information).

A programmable clock divider OPCLKDIV controls the frequency of the OPCLK output. This clock is enabled by register bit OPCLK_ENA. See “Clocking and Sample Rates” for a definition of this register field.

To enable clock output via one or more GPIO pins, the following register settings are required:

- AIF_TRIS = 0
- GPIOn_SEL = 0001 for the selected GPIO clock output pin
- GPIOn_PU = 0 for the selected GPIO clock output pin
- GPIOn_PD = 0 for the selected GPIO clock output pin

TEMPERATURE SENSOR OUTPUT

To protect the device from overheating a thermal shutdown function is provided (see "Thermal Shutdown" section for more information).

The polarity of the Thermal Shutdown sensor may be controlled by register bit TEMPOK_POL. Note that this polarity inversion bit applies to the Interrupt register behaviour only; it does not affect the direct GPIO output of the Temperature Sensor function. The associated interrupt event may be masked or enabled by register bit TEMPOK_IRQ_ENA. The Temperature status bit contained in the IRQ Register (R18) may be read at any time or else in response to an Interrupt event. See Table 30 for more details of the Interrupt function.

If direct output of the Temperature status bit is required to the external pins of the WM8953, the following register settings are required:

- AIF_TRIS = 0
- GPIOn_SEL = 0101 for the selected GPIO Temperature status output pin
- GPIOn_PU = 0 for the selected GPIO Temperature status output pin
- GPIOn_PD = 0 for the selected GPIO Temperature status output pin

The register fields used to configure the Temperature Sensor GPIO function are described in Table 26.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h)	11	TEMPOK_POL (rw)	1b	Temperature Sensor polarity 0 = Non-inverted 1 = Inverted
R22 (16h)	11	TEMPOK_IRQ_ ENA	0b	Temperature Sensor IRQ Enable 0 = disabled 1 = enabled

Table 26 Temperature Sensor GPIO Control

The temperature sensor function operates according to the following truth table:

LABEL	VALUE	DESCRIPTION
Temperature Sensor output	0	Overheat temperature exceeded
Temperature Sensor output	1	Overheat temperature not exceeded

Table 27 Truth Table for GPIO Output of Temperature Sensor Function

PLL LOCK OUTPUT

An internal signal used to indicate the lock status of the PLL can be output to a GPIO pin or used to trigger an Interrupt event. The polarity of the PLL Lock indication may be controlled by register bit PLL_LCK_POL. Note that this polarity inversion bit applies to the Interrupt register behaviour only; it does not affect the direct GPIO output of the PLL Lock function. The associated interrupt event may be masked or enabled by register bit PLL_LCK_IRQ_ENA. The PLL Lock status bit in the IRQ Register (R18) may be read at any time or else in response to an Interrupt event. See Table 30 for more details of the Interrupt function.

If direct output of the PLL Lock status bit is required to the external pins of the WM8953, the following register settings are required:

- AIF_TRIS = 0
- GPIOn_SEL = 0100 for the selected PLL Lock status output pin
- GPIOn_PU = 0 for the selected PLL Lock status output pin
- GPIOn_PD = 0 for the selected PLL Lock status output pin

The register fields used to configure the PLL Lock GPIO function are described in Table 28.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h)	8	PLL_LCK_POL (rw)	0b	PLL Lock polarity 0 = Non-inverted 1 = Inverted
R22 (16h)	8	PLL_LCK_IRQ_ ENA	0b	PLL Lock IRQ Enable 0 = disabled 1 = enabled

Table 28 PLL Lock GPIO Control

The PLL Lock function operates according to the following truth table:

LABEL	VALUE	DESCRIPTION
PLL Lock output	0	PLL not Locked
PLL Lock output	1	PLL Locked

Table 29 Truth Table for GPIO Output of PLL Lock Function

LOGIC '1' AND LOGIC '0' OUTPUT

The GPIO pins can be programmed to drive a logic high or logic low signal. The following register settings are required:

- AIF_TRIS = 0
- GPIOn_SEL = 0010 for each Logic ‘0’ output pin
- GPIOn_SEL = 0011 for each Logic ‘1’ output pin
- GPIOn_PU = 0 for each Logic ‘0’ or Logic ‘1’ GPIO pin
- GPIOn_PD = 0 for each Logic ‘0’ or Logic ‘1’ GPIO pin

INTERRUPT EVENT OUTPUT

An interrupt can be generated by any of the following events described earlier:

- Button Control input (on GPIO3, GPIO4, GPIO5, GPI7 or GPI8)
- MICBIAS current / short circuit / accessory detect
- PLL Lock
- Temperature Sensor

The interrupt status flag IRQ is asserted when any un-masked Interrupt input is asserted. It is the OR'd combination of all the un-masked Interrupt inputs. If required, this flag may be inverted using the IRQ_INV register bit. The GPIO pins can be configured to output the IRQ signal.

The interrupt behaviour is driven by level detection (not edge detection) of the un-masked inputs. Therefore, if an input remains asserted after the interrupt register has been reset, then the interrupt status flag IRQ will be triggered again even though no transition has occurred. If edge detection is required (eg. confirming that the input has been de-asserted), then the polarity inversion may be used after each event in order to detect each rising and falling edge separately. This is described further in the "GPIO Summary" section.

The status of the IRQ flag may be read back via the control interface. The status of each GPIO pin and the internal signals PLL_LCK, TEMPOK, MICSHRT and MICDET may also be read back in the same way.

The IRQ register (R18) is described in Table 30. The status of the GPIO pins or other Interrupt inputs can be read back via the read/write bits R18[11:0]. The Interrupt inputs are latched once set. Each input may be reset by writing a 1 to the appropriate bit. The IRQ bit cannot be reset; it is the OR'd combination of all other registers and will reset only if R18[11:0] are all 0.

If direct output of the Interrupt signal is required to external pins of the WM8953, the following register settings are required:

- AIF_TRIS = 0
- GPIOn_SEL = 0111 for the selected Interrupt (IRQ) output pin
- GPIOn_PU = 0 for the selected Interrupt (IRQ) output pin
- GPIOn_PD = 0 for the selected Interrupt (IRQ) output pin

The IRQ register (R18) is described in Table 30.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h)	12	IRQ (ro)	Read Only	IRQ Readback (Allows polling of IRQ status)
	11	TEMPOK (rr)	Read or Reset	Temperature OK status Read- 0 = Device temperature NOT ok 1 = Device temperature ok Write - 1 = Reset TEMPOK latch
	10	MICSHRT (rr)	Read or Reset	MICBIAS short status Read- 0 = MICBIAS ok 1 = MICBIAS shorted Write- 1 = Reset MICSHRT latch
	9	MICDET (rr)	Read or Reset	MICBIAS detect status MICBIAS microphone detect Readback Read- 0 = No Microphone detected 1 = Microphone detected Write- 1 = Reset MICDET latch
	8	PLL_LCK (rr)	Read or Reset	PLL Lock status Read- 0 = PLL NOT locked 1 = PLL locked Write- 1 = Reset PLL_LCK latch
	7:0	GPIO_STATUS [7:0] (rr)	Read or Reset	GPIO and GPI Input Pin Status GPIO_STATUS[7] = GPI8 pin status GPIO_STATUS[6] = GPI7 pin status GPIO_STATUS[5] = Reserved GPIO_STATUS[4] = GPIO5 status GPIO_STATUS[3] = GPIO4 status GPIO_STATUS[2] = GPIO3 status GPIO_STATUS[1] = Reserved GPIO_STATUS[0] = Reserved
R23 (17h) GPIO Control (2)	12	IRQ_INV (rw)	0b	IRQ Invert 0 = IRQ output active high 1 = IRQ output active low

Table 30 GPIO Interrupt and Status Readback

SERIAL DATA OUTPUT (REGISTER READBACK)

The GPIO pins can be configured to output serial data during register readback in 3-wire (open-drain) or 4-wire mode. The readback mode is configured using the register bits RD_3W_ENA and MODE_3W4W as described in Table 31.

Setting the RD_3W_ENA bit to 1 enables 3-wire readback using the SDIN pin in open-drain mode. Setting the RD_3W_ENA bit to 0 requires the use of a GPIO pin as SDOUT. To enable SDOUT on a GPIO pin, the following register settings are required:

- AIF_TRIS = 0
- GPIOn_SEL = 0110 for the selected SDOUT output pin
- GPIOn_PU = 0 for the selected SDOUT output pin
- GPIOn_PD = 0 for the selected SDOUT output pin

The register fields used to configure SDOUT on the GPIO pins are described in Table 31. Refer to "Control Interface" for more details of 3-wire and 4-wire interfacing.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h)	15	RD_3W_ENA	1b	3- / 4-wire readback configuration 1 = 3-wire mode 0 = 4-wire mode, using GPIO pin
	14	MODE_3W4W	0b	3-wire mode 0 = push 0/1 1 = open-drain 4-wire mode 0 = push 0/1 1 = wired-OR

Table 31 GPIO 3-Wire Readback Enable

GPIO SUMMARY

The GPIO functions are summarised in Figure 22.

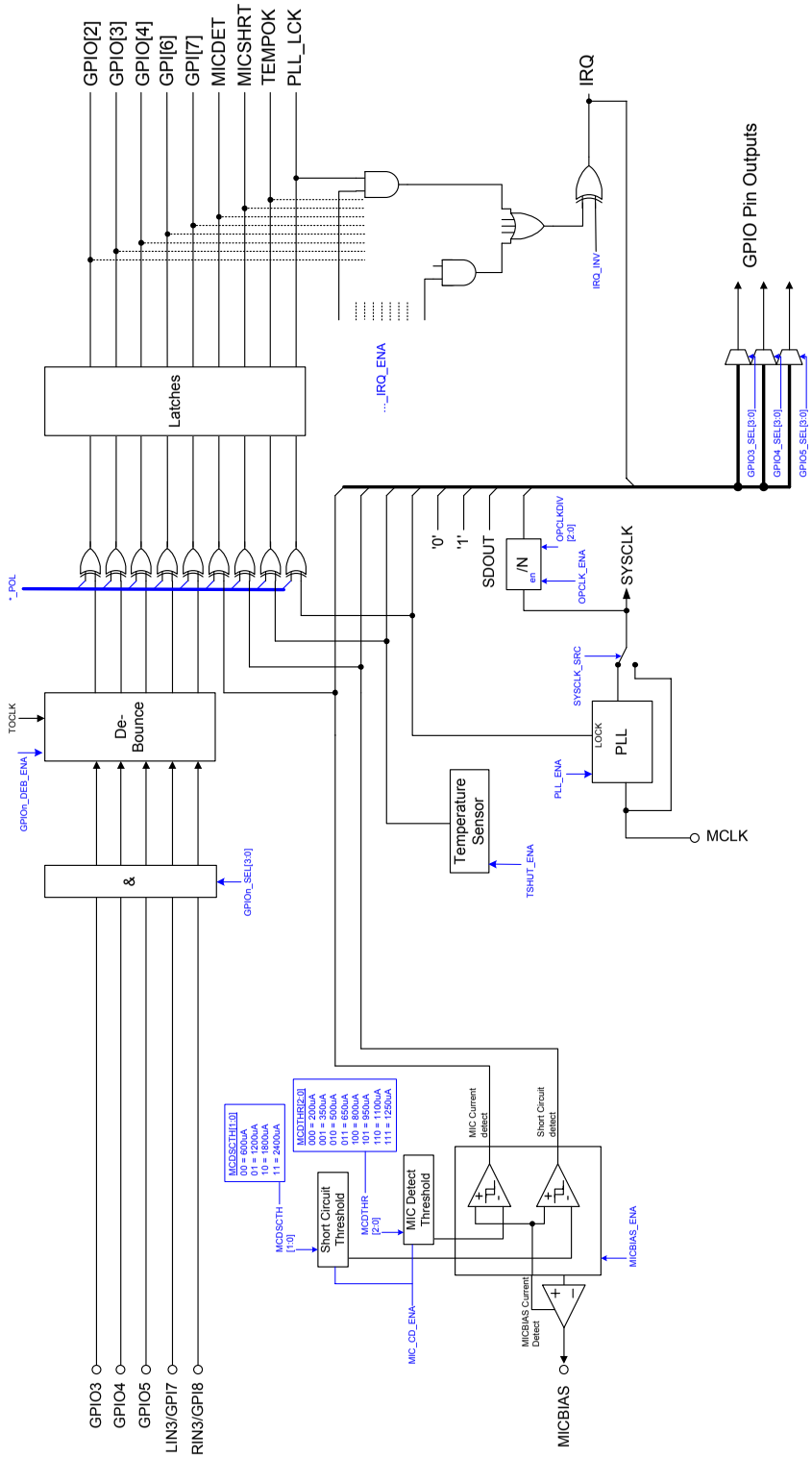


Figure 22 GPIO Control Diagram

Details of the GPIO implementation are shown below. In order to avoid GPIO loops if a GPIO is configured as an output the corresponding input is disabled, as shown in Figure 23 below.

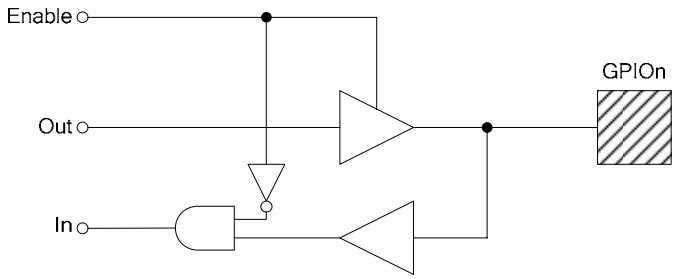


Figure 23 GPIO Pad

The GPIO register, i.e. latch structure, is shown in Figure 24 below. The de-bounce Control fields GPIOn_DEB_ENA determine whether the signal is de-bounced or not. (Note that TOCLK (via SYSCLK) needs to be present in order for the debounce circuit to work.) The polarity bits GPIO_POL[7:0] control whether an interrupt is triggered by a logic 1 level (for GPIO_POL[n] = 0) or a logic 0 level (for GPIO_POL[n] = 1). The latch will cause the interrupt to be stored until it is reset by writing to the Interrupt Register. The latched signal is processed by the IRQ circuit, shown in Figure 22 above. The interrupt status bits can be read at any time from Register R18 (see Table 30) and are reset by writing a "1" to the applicable bit in Register R18.

Note that the interrupt behaviour is driven by level detection (not edge detection). Therefore, if an input remains asserted after the interrupt register has been reset, then the interrupt event will be triggered again even though no transition has occurred. If edge detection is required, this may be implemented as described in the following paragraphs.

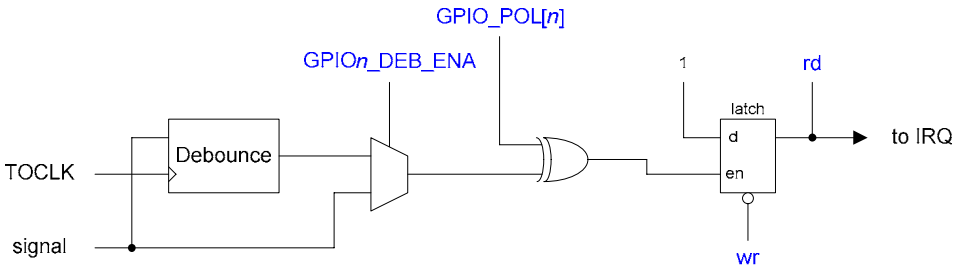


Figure 24 GPIO Function

Three typical scenarios are presented in the following Figure 25, Figure 26 and Figure 27. The examples are:

- Latch a GPIO input (Figure 25)
- Debounce and latch a GPIO input (Figure 26)
- Use the GPIOn_POL bit to implement an IRQ edge detect function (Figure 27)

The GPIO input or internal Interrupt event (eg. MICBIAS current detect) is latched as illustrated below:

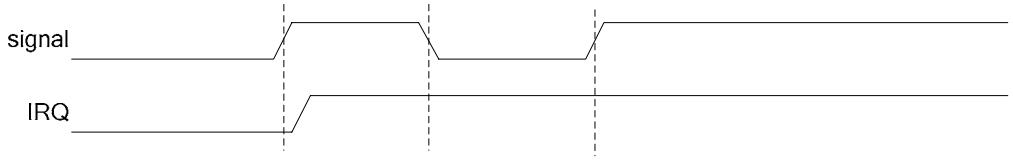


Figure 25 GPIO Latch

The de-bounce function on the GPIO input pins enables transient behaviour to be filtered as illustrated below:

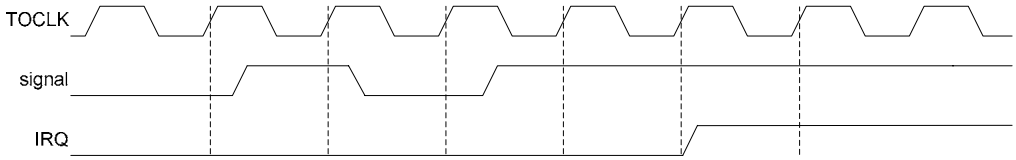


Figure 26 GPIO De-bounce

To implement an edge detect function on a GPIO input, the GPIOn_POL bits may be used to alternate the GPIO polarity after each edge transition. For example, after a logic 1 has caused an Interrupt event, the polarity may be inverted prior to resetting the Interrupt register bit. In this way, the next interrupt event generated by this GPIO will occur when it returns to the logic 0 state. The GPIOn_POL bit must be reversed after every GPIO edge transition, as illustrated below:

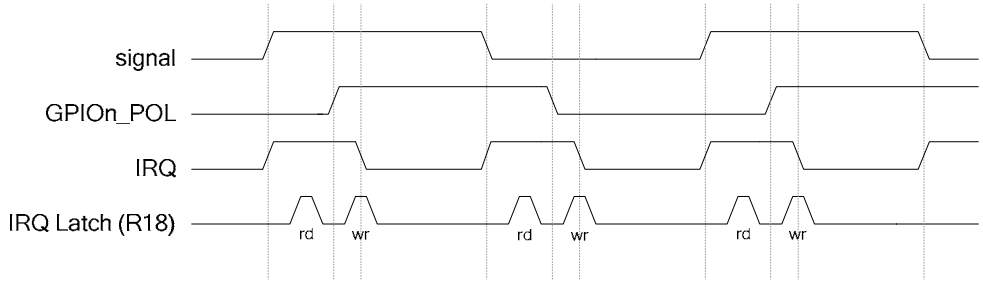


Figure 27 GPIO Edge Detect

GPIO IRQ HANDLING

In the following diagram Figure 28 a typical IRQ scenario is illustrated.

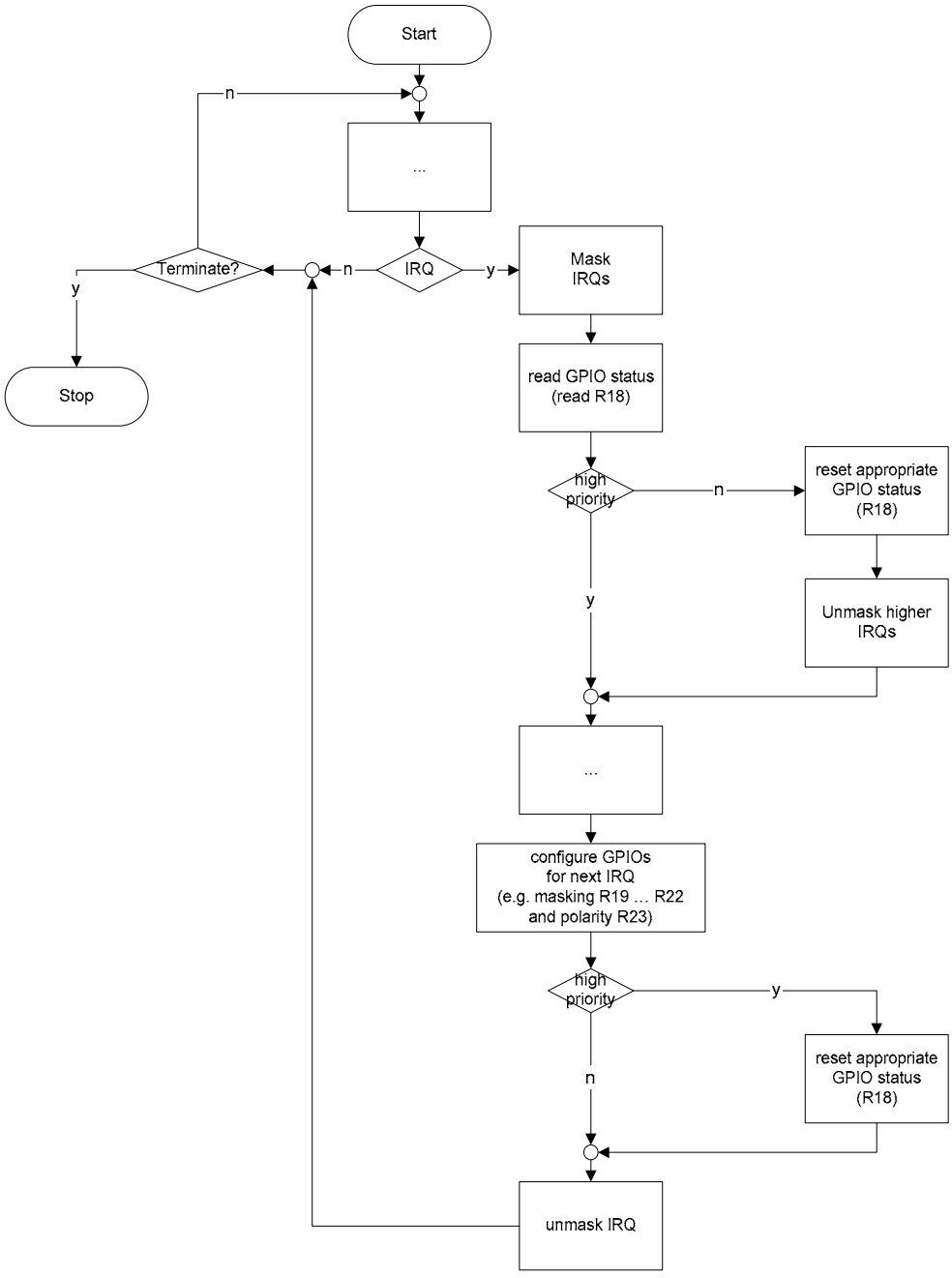


Figure 28 GPIO IRQ Handling

DIGITAL AUDIO INTERFACE

The digital audio interface is used for outputting ADC data from the WM8953. It uses three pins:

- ADCDAT: ADC data output
- ADCLRC: ADC data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK and ADCLRC can be outputs when the WM8953 operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- I^2S
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the "Electrical Characteristics" section for timing information.

Time Division Multiplexing (TDM) is available in all four data format modes. The WM8953 can be programmed to send and receive data in one of two time slots.

PCM operation is supported using the DSP mode.

MASTER AND SLAVE MODE OPERATION

The WM8953 digital audio interface can operate as a master or slave as shown in Figure 29 and Figure 30.

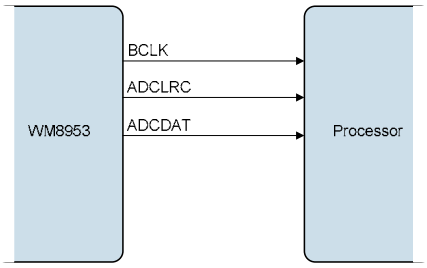


Figure 29 Master Mode

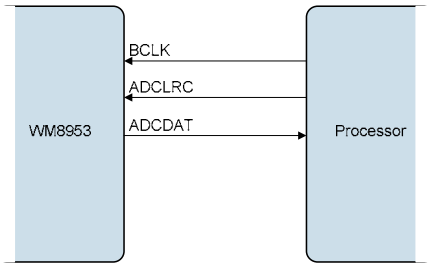


Figure 30 Slave Mode

The dual Audio Interface approach of the WM8953 has been implemented in such a way that it gives the user and application as much flexibility as possible. The application needs to be carefully analysed and the WM8953 configured accordingly. The Audio Interface Output Control is illustrated in Figure 31.

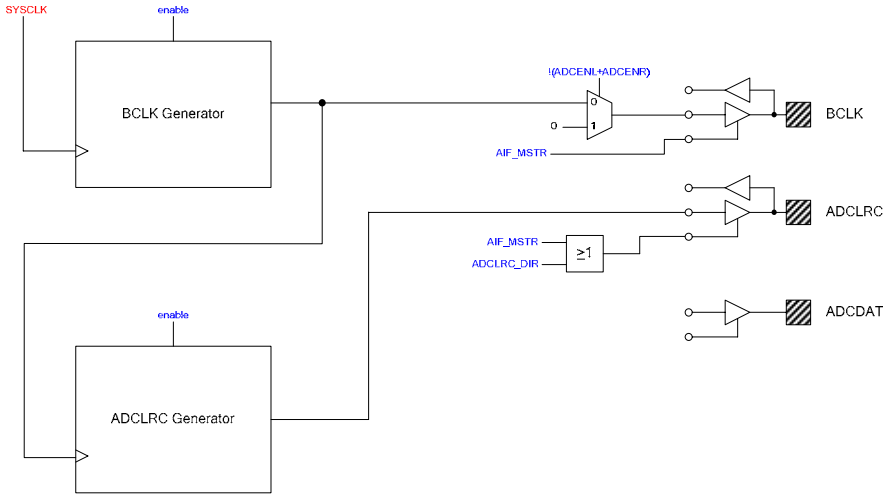


Figure 31 Audio Interface Output Control

The Audio Interface output control is illustrated above. The master mode control register AIF_MSTR and the left-right clock control register ADCLRC_DIR determine whether the WM8953 generates the associated clocks. These registers are described in Table 32 below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h)	15	AIF_MSTR	0b	Audio Interface Master Mode Select 0 = Slave mode 1 = Master mode
	11	ADCLRC_DIR	0b	ADCLRC Direction (Forces ADCLRC clock to be output in slave mode) 0 = ADCLRC normal operation 1 = ADCLRC clock output enabled

Table 32 Audio Interface Output Function Control

OPERATION WITH TDM

Time division multiplexing (TDM) allows multiple devices to transfer data simultaneously on the same bus. The WM8953 supports TDM in master and slave modes for all data formats and word lengths. TDM is enabled using register bit AIFADC_TDM. The TDM data slot is programmed using register bit AIFADC_TDM_CHAN.

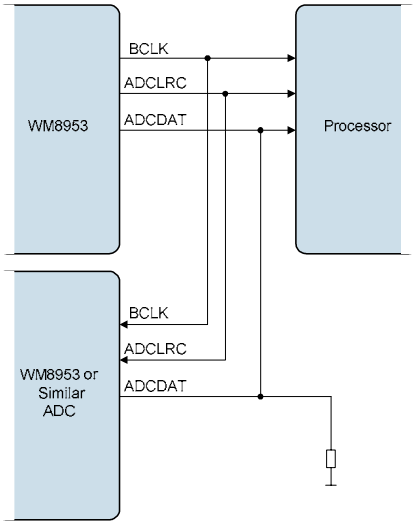


Figure 32 TDM with WM8953 as Master

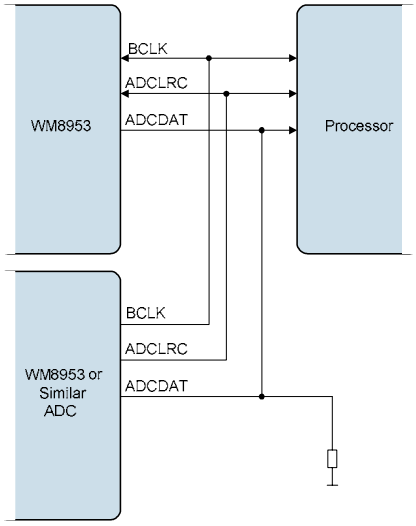


Figure 33 TDM with Other ADC as Master

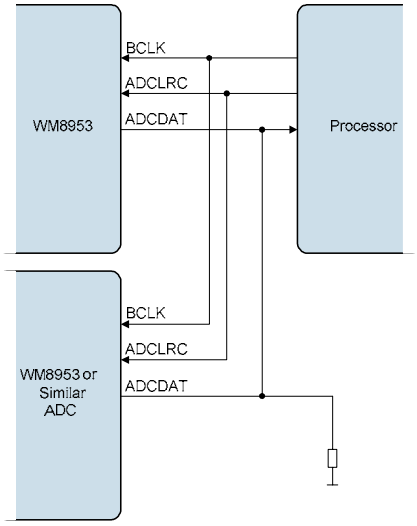


Figure 34 TDM with Processor as Master

Note: The WM8953 is a 24-bit device. If the user operates the WM8953 in 32-bit mode then the 8 LSBs are not driven. It is therefore recommended to add a pull-down resistor if necessary to the ADCDAT line in TDM mode.

BCLK DIVIDE

The BCLK frequency is controlled by BCLK_DIV. The BCLK frequency must be set appropriately to support the sample rate of the ADC.

Internal clock divide and phase control mechanisms ensure that the BCLK and ADCLRC edges will occur in a predictable and repeatable position relative to each other and to the data for a given combination of ADC sample rate and BCLK_DIV settings.

See “Clocking and Sample Rates” section for more information.

AUDIO DATA FORMATS (NORMAL MODE)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a ADCLRC transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each ADCLRC transition.

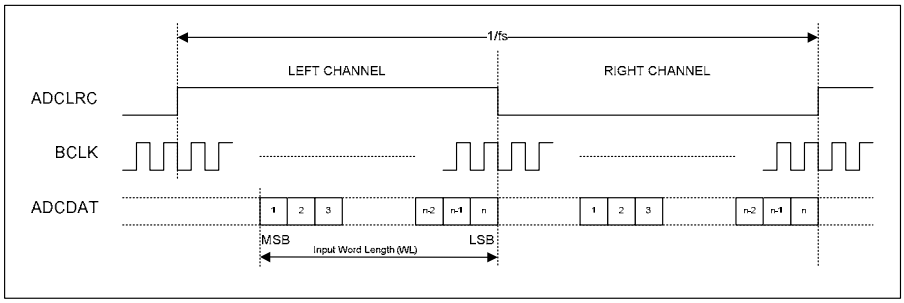


Figure 35 Right Justified Audio Interface (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a ADCLRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each ADCLRC transition.

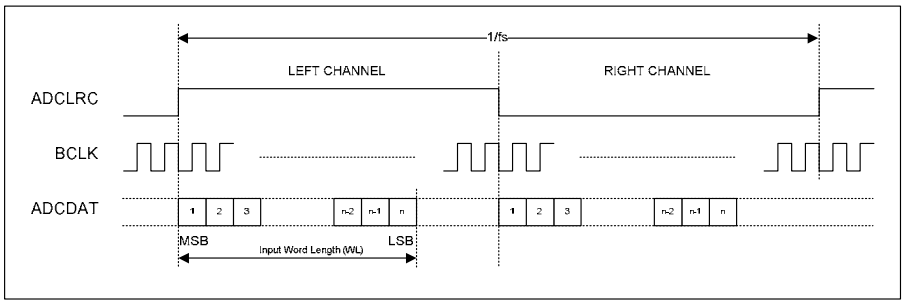


Figure 36 Left Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a ADCLRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

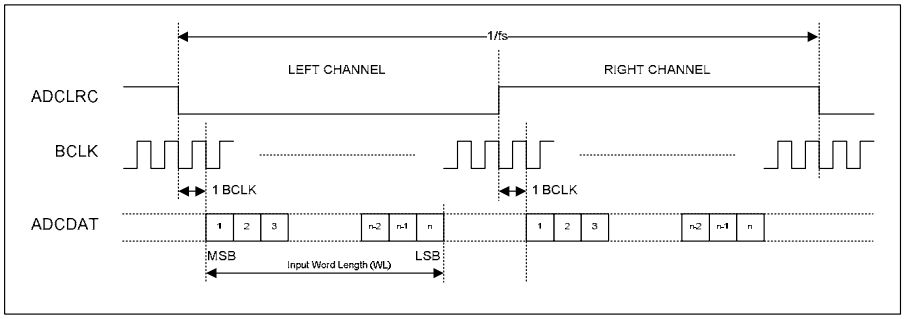


Figure 37 I2S Justified Audio Interface (assuming n-bit word length)

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by AIF_LRCLK_INV) following a rising edge of ADCLRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the ADCLRC output will resemble the frame pulse shown in Figure 38 and Figure 39. In device slave mode, Figure 40 and Figure 41, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

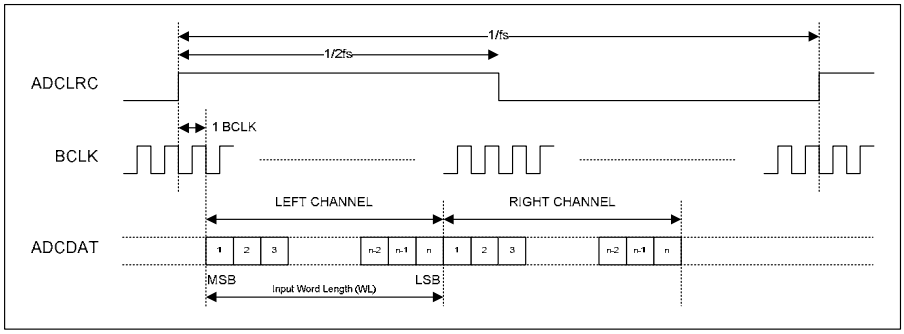


Figure 38 DSP Mode Audio Interface (mode A, AIF_LRCLK_INV=0, Master)

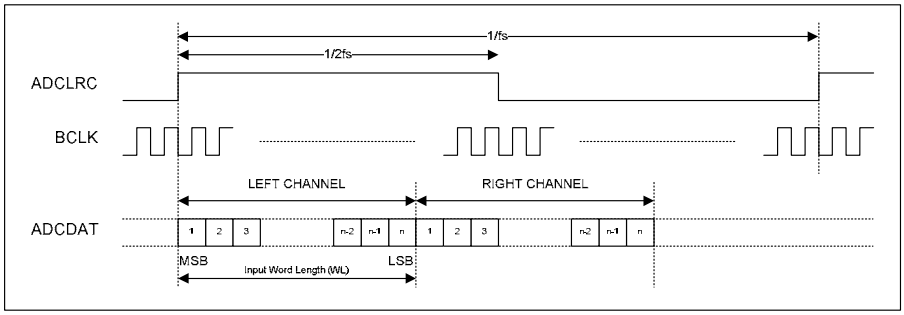


Figure 39 DSP Mode Audio Interface (mode B, AIF_LRCLK_INV=1, Master)

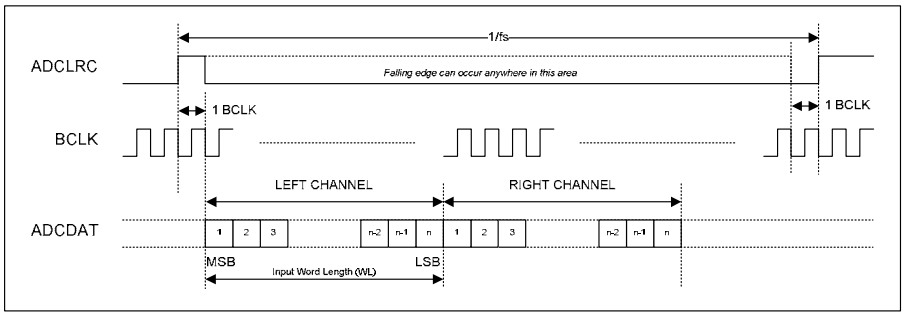


Figure 40 DSP Mode Audio Interface (mode A, AIF_LRCLK_INV=0, Slave)

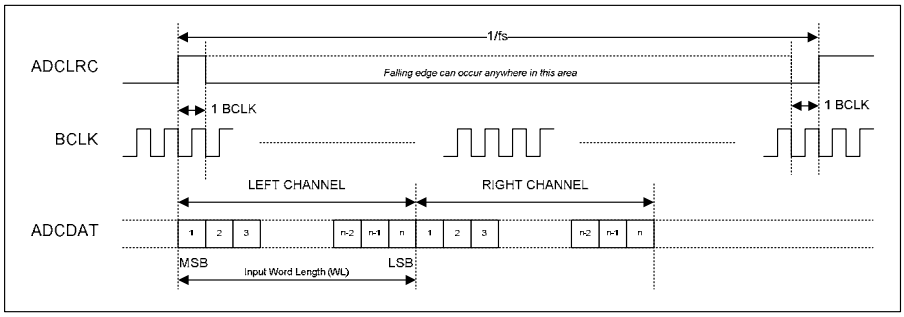


Figure 41 DSP Mode Audio Interface (mode B, AIF_LRCLK_INV=1, Slave)

PCM operation is supported in DSP interface mode. WM8953 ADC data that is output on the Left Channel will be read as mono PCM data by the receiving equipment.

AUDIO DATA FORMATS (TDM MODE)

TDM is supported in master and slave mode and is enabled by register bit AIF_ADC_TDM. All audio interface data formats support time division multiplexing (TDM).

Two time slots are available (Slot 0 and Slot 1), selected by register bit AIFADC_TDM_CHAN.

When TDM is enabled, the ADCDAT pin will be tri-stated immediately before and immediately after data transmission, to allow another ADC device to drive this signal line for the remainder of the sample period. Note that it is important that two ADC devices do not attempt to drive the data pin simultaneously. A short circuit may occur if the transmission time of the two ADC devices overlap with each other. See “Audio Interface Timing - TDM Mode” for details of the ADCDAT output relative to BCLK signal. Note that it is possible to ensure a gap exists between transmissions by setting the transmitted word length to a value higher than the actual length of the data. For example, if 32-bit word length is selected where only 24-bit data is available, then the WM8953 interface will tri-state after transmission of the 24-bit data, ensuring a gap after the WM8953’s TDM slot.

When TDM is enabled, BCLK frequency must be high enough to allow data from both time slots to be transferred. The relative timing of Slot 0 and Slot 1 depends upon the selected data format as shown in Figure 42 to Figure 46.

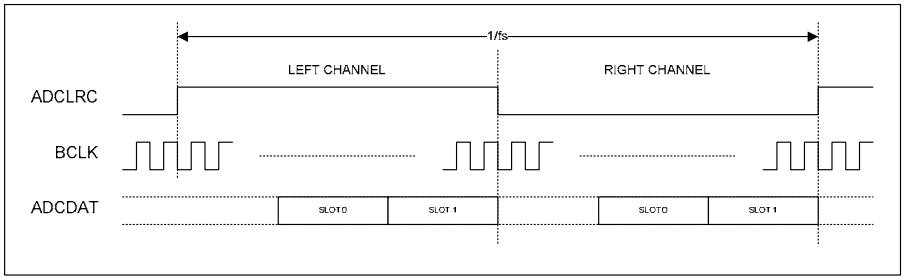


Figure 42 TDM in Right-Justified Mode

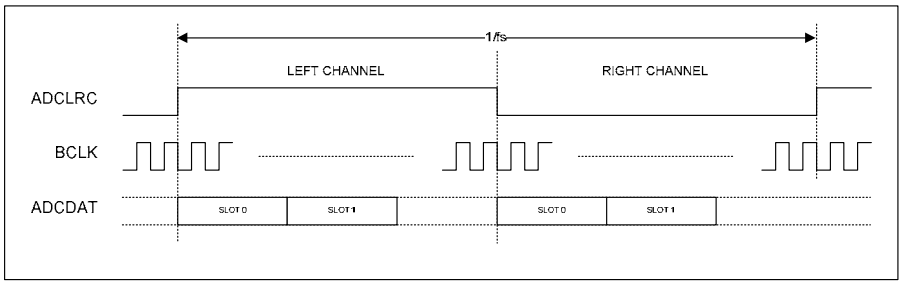


Figure 43 TDM in Left-Justified Mode

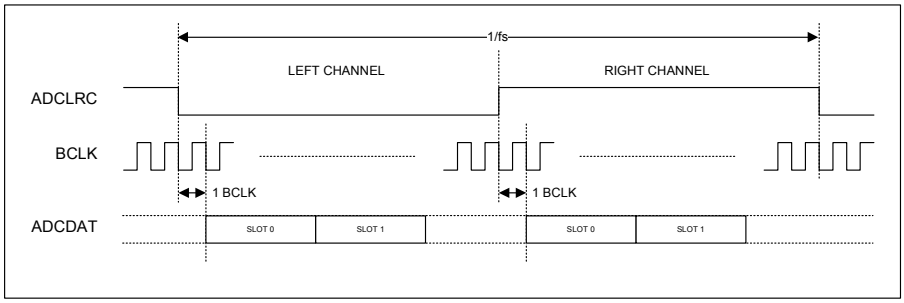


Figure 44 TDM in I²S Mode

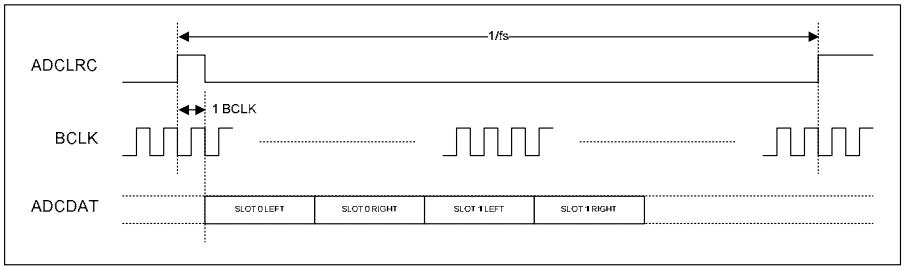


Figure 45 TDM in DSP Mode A

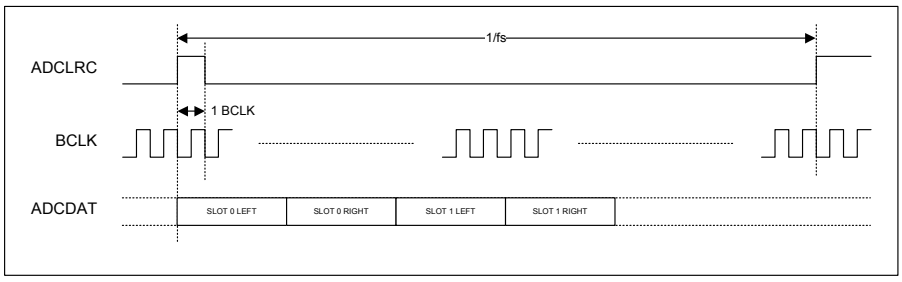


Figure 46 TDM in DSP Mode B

DIGITAL AUDIO INTERFACE CONTROL

The register bits controlling audio data format, word length, left/right channel data source and TDM are summarised in Table 33.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h)	15	AIFADCL_SRC	0b	Left ADC Data Source Select 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel
	14	AIFADCR_SRC	1b	Right ADC Data Source Select 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
	13	AIFADC_TDM	0b	ADC TDM Enable 0 = Normal ADCDAT operation 1 = TDM enabled on ADCDAT
	12	AIFADC_TDM_CHAN	0b	ADCDAT TDM Channel Select 0 = ADCDAT outputs data on slot 0 1 = ADCDAT output data on slot 1
	8	AIF_BCLK_INV	0b	BCLK Invert 0 = BCLK not inverted 1 = BCLK inverted
	7	AIF_LRCLK_INV	0b	Right, left and I^2S modes – LRCLK polarity 0 = normal LRCLK polarity 1 = invert LRCLK polarity
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)
	6:5	AIF_WL [1:0]	10b	Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits Note - see “Companding” for the selection of 8-bit mode.
	4:3	AIF_FMT [1:0]	10b	Digital Audio Interface Format 00 = Right justified 01 = Left justified 10 = I^2S Format 11 = DSP Mode

Table 33 Audio Data Format Control

AUDIO INTERFACE OUTPUT AND GPIO TRISTATE

Register bit AIF_TRIS can be used to tristate the audio interface and GPIO pins as described in Table 34.

All GPIO pins and digital audio interface pins will be tristated by this function, regardless of the state of other registers which control these pin configurations.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h)	13	AIF_TRIS	0	Audio Interface and GPIO Tristate 0 = Audio interface and GPIO pins operate normally 1 = Tristate all audio interface and GPIO pins

Table 34 Tri-stating the Audio Interface and GPIO Pins

MASTER MODE BCLK AND ADCLRC ENABLE

The audio interface pins BCLK, ADCLRC and ADCDAT can be independently programmed to operate in master mode or slave mode using register bit AIF_MSTR.

When the audio interface is operating in slave mode, the BCLK and ADCLRC clock outputs to these pins are by default disabled to allow the digital audio source to drive these pins.

It is also possible to force the ADCLRC to be output using register bit ADCLRC_DIR, allowing mixed master and slave mode.

The clock generators for the audio interface are enabled according to the control signals shown in Figure 47.

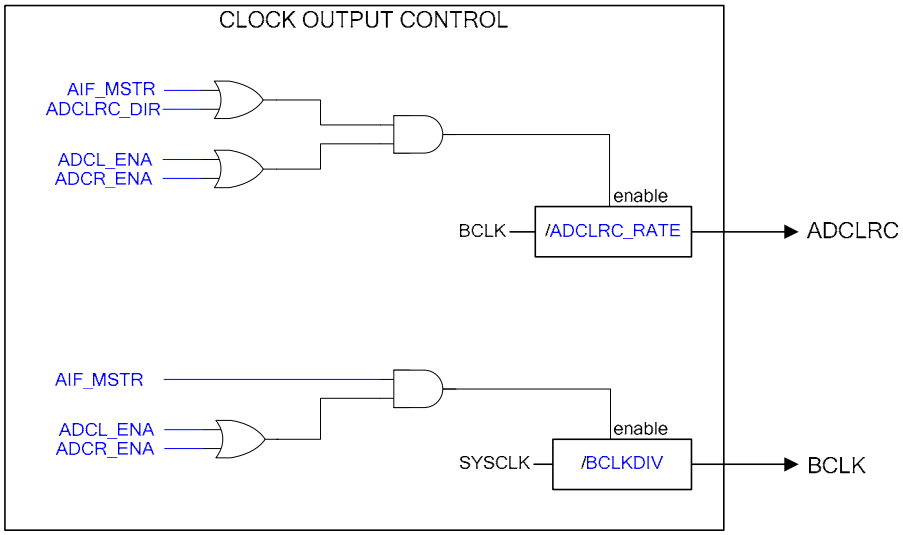


Figure 47 Clock Output Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h)	15	AIF_MSTR	0b	Audio Interface Master Mode Select 0 = Slave mode 1 = Master mode
	11	ADCLRC_DIR	0b	ADCLRC Direction (Forces ADCLRC clock to be output in slave mode) 0 = ADCLRC normal operation 1 = ADCLRC clock output enabled
	10:0	ADCLRC_RATE [10:0]	040h	ADCLRC Rate ADCLRC clock output = BCLK / ADCLRC_RATE Integer (LSB = 1) Valid from 8..2047

Table 35 Digital Audio Interface Clock Output Control

COMPANDING

The WM8953 supports A-law and μ-law companding. This is selected as shown in Table 36.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h)	2	ADC_COMP	0b	ADC Companding Enable 0 = disabled 1 = enabled
	1	ADC_COMPMODE	0b	ADC Companding Type 0 = μ-law 1 = A-law

Table 36 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

μ-law (where μ=255 for the U.S. and Japan):

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \qquad -1 \le x \le 1$

A-law (where A=87.6 for Europe):

$F(x) = A|x| / (1 + \ln A)$ } for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ } for $1/A \le x \le 1$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ-law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSBs of data.

Companding converts 13 bits (μ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. This provides greater precision for low amplitude signals than for high amplitude signals, resulting in a greater usable dynamic range than 8 bit linear quantization. The companded signal is an 8-bit word comprising sign (1 bit), exponent (3 bits) and mantissa (4 bits).

8-bit mode is selected whenever ADC_COMP=1. The use of 8-bit data allows samples to be passed using as few as 8 BCLK cycles per LRC frame. When using DSP mode B, 8-bit data words may be transferred consecutively every 8 BCLK cycles.

8-bit mode (without Companding) may be enabled by setting ADC_COMPMODE=1, when ADC_COMP=0.

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 37 8-bit Companded Word Composition

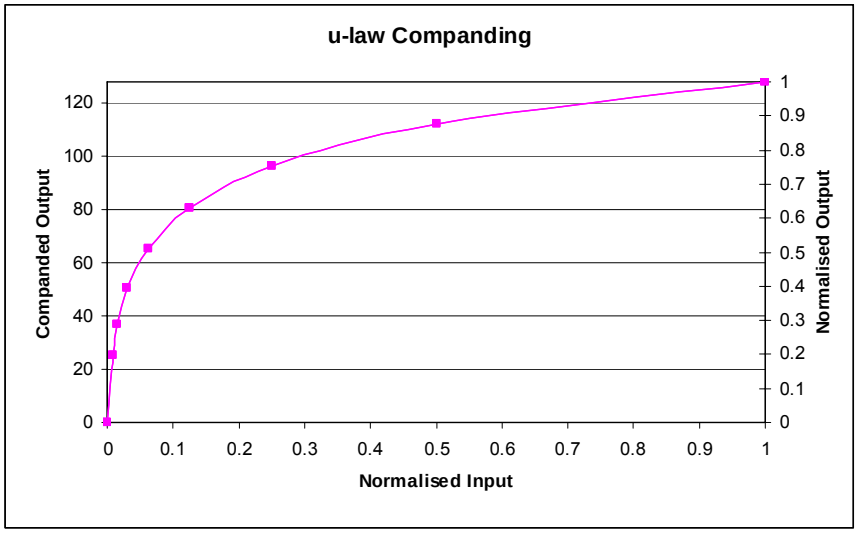


Figure 48 µ-Law Companding

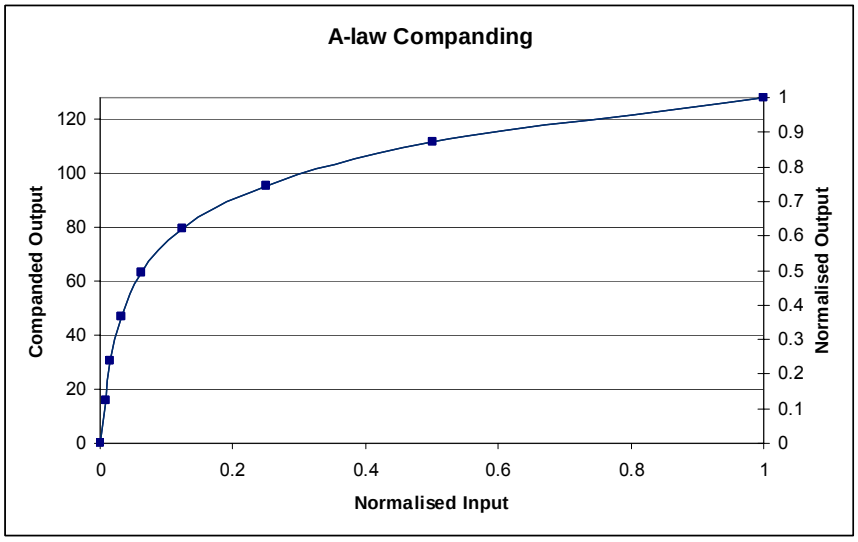


Figure 49 A-Law Companding

CLOCKING AND SAMPLE RATES

The internal clocks for the ADCs, DSP core functions and digital audio interface are derived from a common internal clock source, SYSCLK.

SYSCLK can either be derived directly from MCLK, or may be generated from a PLL using MCLK as an external reference. Many commonly-used audio sample rates can be derived directly from typical MCLK frequencies; the PLL provides additional flexibility for a wide range of MCLK frequencies. All clock configurations must be set up before enabling playback to avoid glitches.

The ADC sample rate is selectable, relative to SYSCLK, using ADC_CLKDIV. This must be set according to the required sampling frequency and depending on the selected clocking mode (AIF_LRCLKRATE).

In master mode, BCLK is also derived from SYSCLK via a programmable division set by BCLK_DIV. The BCLK frequency must be set appropriately to support the sample rate of the ADC. The ADCLRC signal does not automatically match the ADC sample rate; this must be configured using ADCLRC_RATE as described under “Digital Audio Interface Control”.

A clock (OPCLK) derived from SYSCLK can be output on the GPIO pins to provide clocking for other parts of the system. This clock is enabled by OPCLK_ENA and its frequency is set by OPCLKDIV.

A slow clock (TOCLK) derived from SYSCLK can be used to de-bounce the button/accessory detect inputs, and to set the timeout period for volume updates when zero-cross detect is used. This clock is enabled by TOCLK_ENA and its frequency is set by TOCLK_RATE.

Table 38 to Table 43 show the clocking and sample rate controls for MCLK input, BCLK output (in master mode), ADCs, and GPIO clock output.

The overall clocking scheme for the WM8953 is illustrated in Figure 50.

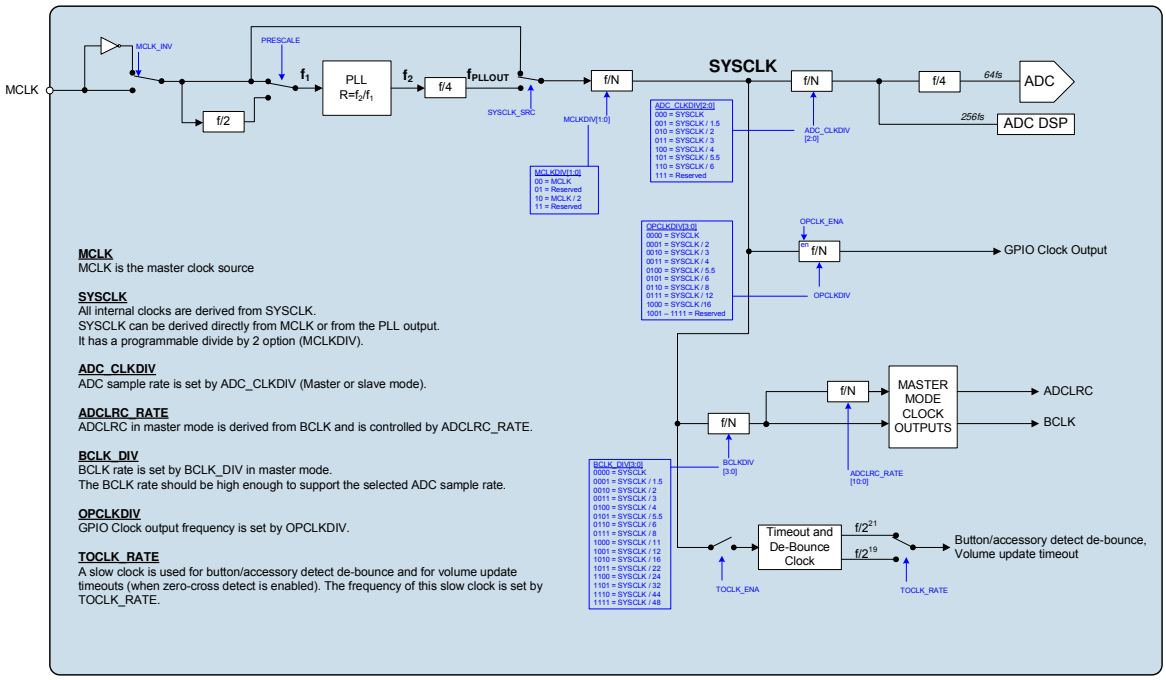


Figure 50 Clocking Scheme

SYSCLK CONTROL

MCLK may be inverted by setting register bit MCLK_INV. Note that it is not recommended to change the control bit MCLK_INV while the WM8953 is processing data as this may lead to clock glitches and signal pop and clicks.

The SYSCLK_SRC bit is used to select the source for SYSCLK. The source may be either MCLK or the PLL output. The selected source is divided by the SYSCLK pre-divider MCLK_DIV to generate SYSCLK. The selected source may also be adjusted by the MCLK_DIV divider. These register fields are described in Table 38. See "PLL" for more details of the Phase Locked Loop clock generator.

The WM8953 supports glitch-free SYSCLK source selection. When both clock sources are running and SYSCLK_SRC is modified to select one of these clocks, a glitch-free clock transition will take place. The de-glitching circuit will ensure that the minimum pulse width will be no less than the pulse width of the faster of the two clock sources.

When the initial clock source is to be disabled before changing to the new clock source, the CLK_FORCE bit must also be used to force the clock source transition to take place. In this case, glitch-free operation cannot be guaranteed.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h)	14	SYSCLK_SRC	0b	SYSCLK Source Select 0 = MCLK 1 = PLL output
	13	CLK_FORCE	0b	Forces Clock Source Selection 0 = Existing SYSCLK source (MCLK or PLL output) must be active when changing to a new clock source. 1 = Allows existing MCLK source to be disabled before changing to a new clock source.
	12:11	MCLK_DIV [1:0]	00b	SYSCLK Pre-divider. Clock source (MCLK or PLL output) will be divided by this value to generate SYSCLK. 00 = Divide SYSCLK by 1 01 = Reserved 10 = Divide SYSCLK by 2 11 = Reserved
	10	MCLK_INV	0b	MCLK Invert 0 = Master clock not inverted 1 = Master clock inverted

Table 38 MCLK and SYSCLK Control

ADC SAMPLE RATE

The ADC sample rate is selectable, relative to SYSCLK, by setting the register fields ADC_CLKDIV. This must be set according to the SYSCLK frequency, and according to the selected clocking mode.

Two clocking modes are provided - Normal Mode (AIF_LRCLKRATE = 0) allows selection of the commonly used sample rates from typical audio system clocking frequencies (eg. 12.288MHz); USB Mode (AIF_LRCLKRATE = 1) allows many of these sample rates to be generated from a 12MHz USB clock. Depending on the available clock sources, the USB mode may be used to save power by supporting 44.1kHz operation without requiring the PLL.

The AIF_LRCLKRATE field must be set as described in Table 39 to ensure correct operation of internal functions according to the SYSCLK / Fs ratio. Table 40 describes the available sample rates using four different common MCLK frequencies.

In Normal mode, the programmable division set by ADC_CLKDIV must ensure that a 256 * ADC Fs clock is generated for the ADC DSP.

In USB mode, the programmable division set by ADC_CLKDIV must ensure that a 272 * ADC Fs clock is generated for the ADC DSP.

Note that in USB mode, the ADC sample rates do not match exactly with the commonly used sample rates (e.g. 44.118 kHz instead of 44.100 kHz). At most, the difference is less than 0.5%. Data recorded at 44.100 kHz sample rate and replayed at 44.118 kHz will experience a slight (sub 0.5%) pitch shift as a result of this difference. Note also that the USB mode cannot be used to generate a 48kHz samples rate from a 12MHz MCLK; the PLL should be used in this case.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h)	7:5	ADC_CLKDIV [2:0]	000b	ADC Sample Rate Divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2.0 011 = SYSCLK / 3.0 100 = SYSCLK / 4.0 101 = SYSCLK / 5.5 110 = SYSCLK / 6.0 111= Reserved
R10 (0Ah)	10	AIF_LRCLKRATE	0b	LRCLK Rate 0 = Normal mode (256 * fs) 1 = USB mode (272 * fs)

Table 39 ADC Sample Rate Control

SYSCLK	ADC SAMPLE RATE DIVIDER	CLOCKING MODE	ADC SAMPLE RATE
12.288 MHz	000 = SYSCLK / 1	Normal (256 * Fs)	48 kHz
	001 = SYSCLK / 1.5		32 kHz
	010 = SYSCLK / 2		24 kHz
	011 = SYSCLK / 3		16 kHz
	100 = SYSCLK / 4		12 kHz
	101 = SYSCLK / 5.5		Not used
	110 = SYSCLK / 6		8 kHz
	111 = Reserved		Reserved
11.2896 MHz	000 = SYSCLK / 1	Normal (256 * Fs)	44.1 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		22.05 kHz
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		11.025 kHz
	101 = SYSCLK / 5.5		8.018 kHz
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved
12 MHz	000 = SYSCLK / 1	USB Mode (272 * Fs)	44.118 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		22.059 kHz
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		11.029 kHz
	101 = SYSCLK / 5.5		8.021 kHz
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved
2.048 MHz	000 = SYSCLK / 1	Normal (256 * Fs)	8 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		Not used
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		Not used
	101 = SYSCLK / 5.5		Not used
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved

Table 40 ADC Sample Rates

BCLK CONTROL

In Master Mode, BCLK is derived from SYSCLK via a programmable division set by BCLK_DIV, as described in Table 41. BCLK_DIV must be set to an appropriate value to ensure that there are sufficient BCLK cycles to transfer the complete data words from the ADCs.

In Slave Mode, BCLK is generated externally and appears as an input to the ADC. The host device must provide sufficient BCLK cycles to transfer complete data words from the ADCs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h)	4:1	BCLK_DIV [3:0]	0100b	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 = SYSCLK / 32 1110 = SYSCLK / 44 1111 = SYSCL:K / 48

Table 41 BCLK Control

OPCLK CONTROL

A clock output (OPCLK) derived from SYSCLK may be output via GPIO3, GPIO4 or GPIO5. This clock is enabled by register bit OPCLK_ENA, and its frequency is controlled by OPCLKDIV.

This output of this clock is also dependent upon the GPIO register settings described under “General Purpose Input/Output”.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h)	12:9	OPCLKDIV [3:0]	0000b	GPIO Output Clock Divider 0000 = SYSCLK 0001 = SYSCLK / 2 0010 = SYSCLK / 3 0011 = SYSCLK / 4 0100 = SYSCLK / 5.5 0101 = SYSCLK / 6 0110 = SYSCLK / 8 0111 = SYSCLK / 12 1000 = SYSCLK / 16 1001 to 1111 = Reserved
R2 (02h)	11	OPCLK_ENA (rw)	0b	GPIO Clock Output Enable 0 = disabled 1 = enabled

Table 42 OPCLK Control

TOCLK CONTROL

A slow clock (TOCLK) is derived from SYSCLK to enable input de-bouncing and volume update timeout functions. This clock is enabled by register bit TOCLK_ENA, and its frequency is controlled by TOCLK_RATE, as described in Table 43.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h)	15	TOCLK_RATE	0b	Timeout Clock Rate (Selects clock to be used for volume update timeout and GPIO input de-bounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)
	14	TOCLK_ENA	0b	Timeout Clock Enable (This clock is required for volume update timeout and GPIO input de-bounce) 0 = disabled 1 = enabled

Table 43 TOCLK Control

USB MODE

It is possible to reduce power consumption by disabling the PLL in some applications. One such application is when SYSCLK is generated from a 12MHz USB clock source. Setting the AIF_LRCLKRATE bit as described earlier (see “ADC Sample Rates”) allows a sample rate close to 44.1kHz to be generated with no additional PLL power consumption.

In this configuration, SYSCLK must be driven directly from MCLK and by disabling the PLL. This is achieved by setting SYSCLK_SRC=0, PLL_ENA=0.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah)	10	AIF_LRCLKRATE	0b	LRCLK Rate 0 = Normal mode (256 * fs) 1 = USB mode (272 * fs)

Table 44 USB Mode Control

PLL

The integrated PLL can be used to generate SYSCLK for the WM8953 from a wide range of MCLK reference frequencies. The PLL is enabled by the PLL_ENA register bit. If required, the input reference clock can be divided by 2 by setting the register bit PRESCALE.

The PLL frequency ratio R is equal to f_2/f_1 (see Figure 50). This ratio is the real number represented by register fields PLLN and PLLK, where PLLN is an integer (LSB = 1) and PLLK is the fractional portion of the number (MSB = 0.5). The fractional portion is only valid when enabled by the field SDM. De-selection of fractional mode results in lower power consumption.

For PLL stability, input frequencies and divisions must be chosen so that $5 \leq PLLN \leq 13$. Best performance is achieved for $7 \leq N \leq 9$. Also, the PLL performs best when f_2 is set between 90MHz and 100MHz.

If PLLK is regarded as a 16-bit integer (instead of a fractional quantity), then PLLN and PLLK may be determined as follows:

- PLLN = int R
- PLLK = int (2^{16} (R - PLLN))

The PLL Control register settings are described in Table 45.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h)	15	PLL_ENA (rw)	0	PLL Enable 0 = disabled 1 = enabled
R60 (3Ch)	7	SDM	0	Enable PLL Integer Mode 0 = Integer mode 1 = Fractional mode
	6	PRESCALE	0b	Divide MCLK by 2 at PLL input 0 = Divide by 1 1 = Divide by 2
	3:0	PLLN[3:0]	8h	Integer (N) part of PLL frequency ratio.
R61 (3Dh)	7:0	PLLK [15:8]	31h	Fractional (K) part of PLL frequency ratio. (Most significant bits)
R62 (3Eh)	7:0	PLLK [7:0]	26h	Fractional (K) part of PLL frequency ratio. (Least significant bits)

Table 45 PLL Control

EXAMPLE PLL CALCULATION

To generate 12.288MHz SYSCLK from a 12MHz reference clock:

There is a fixed divide by 4 at the PLL output (see Figure 50) followed by a selectable divide by 2 in the same path. PLL output f_2 should be set in the range 90MHz - 100MHz. Enabling the divide by 2 (MCLK_DIV = 10b) sets the required $f_2 = 4 \times 2 \times 12.288\text{MHz} = 98.304\text{MHz}$.

There is a selectable pre-scale (divide MCLK by 2) at the PLL input (f_1 - see Figure 75). The PLL frequency ratio f_2/f_1 must be set in the range 5 - 13. Disabling the MCLK pre-scale (PRESCALE = 0b) sets the required ratio $f_2/f_1 = 8.192$.

The required settings for this example are:

- MCLK_DIV = 10b
- PRESCALE = 0b
- PLL_ENA = 1
- SDM = 1
- PLLN = 8 = 8h
- PLLK = 0.192 = 3126h

EXAMPLE PLL SETTINGS

Table 46 provides example PLL settings for generating common SYSCLK frequencies from a variety of MCLK reference frequencies.

MCLK (MHz)	SYSCLK (MHz)	MCLKDIV	F2 = SYSCLK * 4 * MCLKDIV	PRESCALE	F1 = MCLK/ PRESCALE	R = F2/F1	N	K
12	11.2896	2	90.3168	1	12	7.5264	7H	86C2H
12	12.288	2	98.304	1	12	8.192	8H	3126H
13	11.2896	2	90.3168	1	13	6.947446	6H	F28BH
13	12.288	2	98.304	1	13	7.561846	7H	8FD5H
14.4	11.2896	2	90.3168	1	14.4	6.272	6H	45A1H
14.4	12.288	2	98.304	1	14.4	6.826667	6H	D3A0H
19.2	11.2896	2	90.3168	2	9.6	9.408	9H	6872H
19.2	12.288	2	98.304	2	9.6	10.24	AH	3D70H
19.68	11.2896	2	90.3168	2	9.84	9.178537	9H	2DB4H
19.68	12.288	2	98.304	2	9.84	9.990243	9H	FD80H
19.8	11.2896	2	90.3168	2	9.9	9.122909	9H	1F76H
19.8	12.288	2	98.304	2	9.9	9.929697	9H	EE00H
24	11.2896	2	90.3168	2	12	7.5264	7H	86C2H
24	12.288	2	98.304	2	12	8.192	8H	3126H
26	11.2896	2	90.3168	2	13	6.947446	6H	F28BH
26	12.288	2	98.304	2	13	7.561846	7H	8FD5H
27	11.2896	2	90.3168	2	13.5	6.690133	6H	B0ACH
27	12.288	2	98.304	2	13.5	7.281778	7H	4822H

Table 46 PLL Frequency Examples

CONTROL INTERFACE

The WM8953 is controlled by writing to its control registers. Readback is available for certain registers, including device ID, power management registers and some GPIO status bits. The control interface can operate as either a 2-, 3- or 4-wire control interface, with additional variants as detailed below:

1. 2-wire
   - open-drain
2. 3-wire
   - push 0/1
   - open drain
3. 4-wire
   - push 0/1
   - wired-OR

Readback is provided on the bi-directional pin SDIN in 2-/3-wire modes and on a GPIO pin in 4-wire mode.

SELECTION OF CONTROL MODE

The MODE pin determines the 2- or 3-/4-wire mode as shown in Table 47.

MODE	INTERFACE FORMAT
Low	2 wire
High	3- or 4- wire

Table 47 Control Interface Mode Selection

2-WIRE SERIAL CONTROL MODE

The WM8953 is controlled by writing to registers through a 2-wire serial control interface. A control word consists of 24 bits. The first 8 bits (B23 to B16) are address bits that select which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 8-bit address of each register in the WM8953). The default device address is 0011010 (0x34h).

The WM8953 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8953, then the WM8953 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1' when operating in write only mode, the WM8953 returns to the idle condition and wait for a new start condition and valid address.

The WM8953 supports a multitude of read and write operations, which are:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

These modes are shown in the section below. Terminology used in the following figures:

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge	
P	Stop Condition	
$R\overline{W}$	ReadNotWrite	0 = Write 1 = Read

Table 48 Terminology

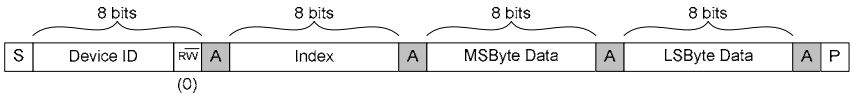


Figure 51 2-Wire Serial Control Interface (single write)

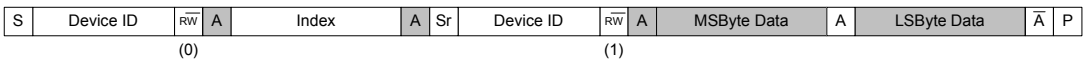


Figure 52 2-Wire Serial Control Interface (single read)

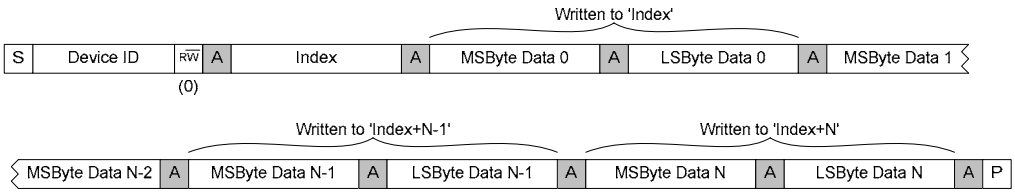


Figure 53 2-Wire Serial Control Interface (multiple write using auto-increment)

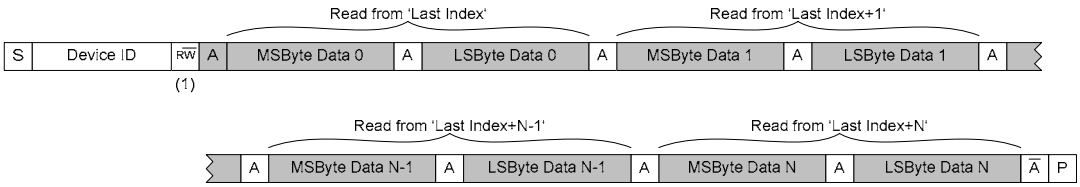


Figure 54 2-Wire Serial Control Interface (multiple read using auto-increment)

In 2-wire mode, the WM8953 has two possible device addresses, which can be selected using the CSB/ADDR pin.

CSB/ADDR STATE	DEVICE ADDRESS
Low	0011010 (0 x 34h)
High	0011011 (0 x 36h)

Table 49 2-Wire Control Interface Address Selection

3-WIRE / 4-WIRE SERIAL CONTROL MODES

The WM8953 is controlled by writing to registers through a 3- or 4-wire serial control interface. A control word consists of 24 bits. The first bit is the read/write bit (R/W), which is followed by 7 address bits (A6 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

The 3- or 4-wire modes are selected by the RD_3W_ENA register bit. Additionally the MODE_3W4W control bit can be used to select between push 0/1 and open-drain or wired-OR modes, as described in Table 50 below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h)	15	RD_3W_ENA	1b	3- / 4-wire readback configuration 1 = 3-wire mode 0 = 4-wire mode, using GPIO pin
	14	MODE_3W4W	0b	3-wire mode 0 = push 0/1 1 = open-drain 4-wire mode 0 = push 0/1 1 = wired-OR

Table 50 3-Wire / 4-Wire Control Interface selection

3-wire control mode is selected by setting RD_3W_ENA = 1. In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB/ADDR latches in a complete control word consisting of the last 24 bits.

In Write operations (R/W=0), all SDIN bits are driven by the controlling device.

In Read operations (R/W=1), the SDIN pin is driven by the controlling device to clock in the register address, after which the WM8953 drives the SDIN pin to output the applicable data bits.

The 3-wire control mode timing is illustrated in Figure 55.

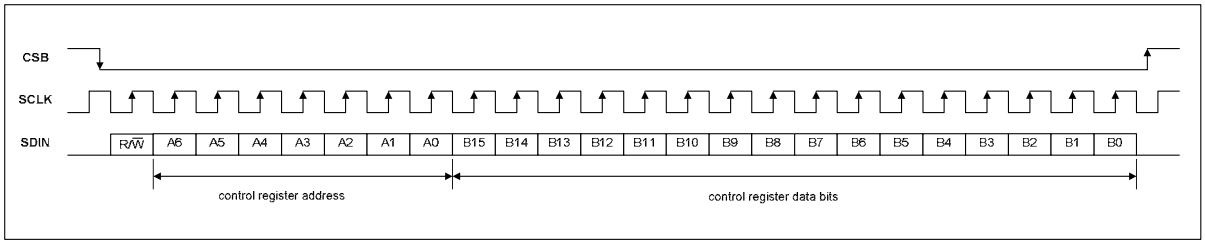


Figure 55 3-Wire Serial Control Interface

4-wire control mode is selected by setting RD_3W_ENA = 0.

In Write operations (R/W=0), this mode is the same as 3-wire mode described above.

In Read operations (R/W=1), a GPIO pin must be selected to output SDOUT by setting GPIOn_SEL=0110b (n= 3, 4 or 5). In this mode, the SDIN pin is ignored following receipt of the valid register address. SDOUT is driven by the WM8953.

In 4-wire Push 0/1 mode, SDOUT is driven low when not outputting register data bits. In Wired-OR mode, SDOUT is undriven when not outputting register data bits.

The 4-wire control mode timing is illustrated in Figure 56 and Figure 57.

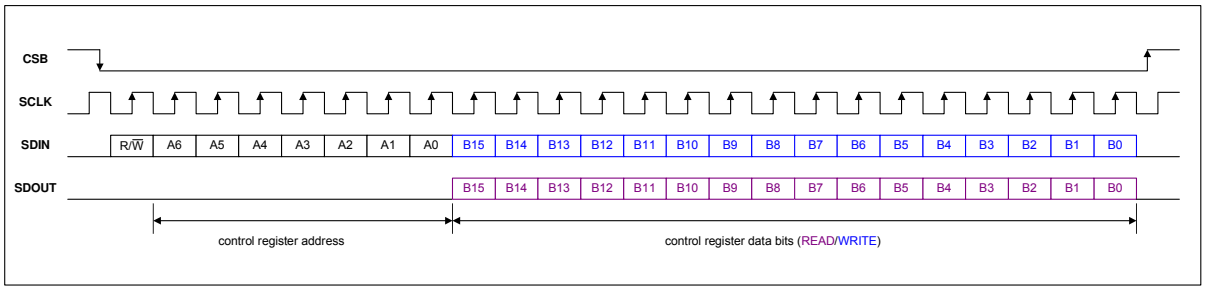


Figure 56 4-Wire Readback (Push 0/1)

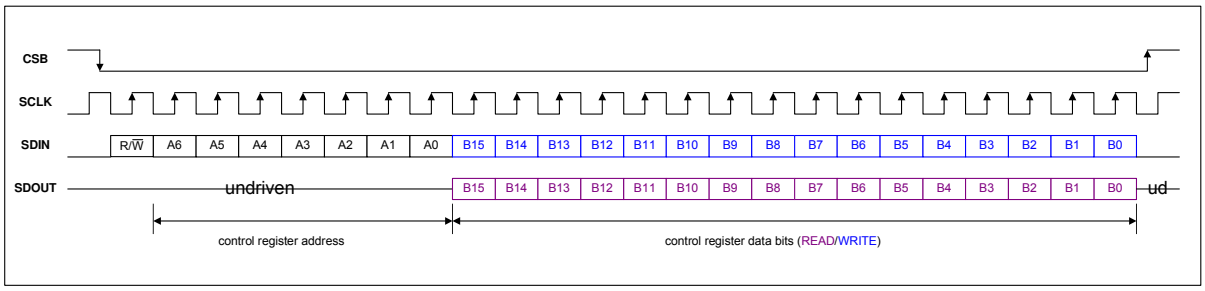


Figure 57 4-Wire Readback (wired-OR)

POWER MANAGEMENT

POWER MANAGEMENT REGISTERS

The WM8953 has two control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To minimise pop or click noise, it is important to enable or disable functions in the correct order.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (1h)	4	MICBIAS_ENA (rw)	0b	MICBIAS Enable 0 = OFF (high impedance output) 1 = ON
	2:1	VMID_MODE [1:0] (rw)	00b	Vmid Divider Enable and Select 00 = Vmid disabled (for OFF mode) 01 = 2 x 50kΩ divider (Normal mode) 10 = 2 x 250kΩ divider (Standby mode) 11 = 2 x 5kΩ divider (for fast start-up)
	0	VREF_ENA (rw)	0b	VREF Enable (Bias for all analogue functions) 0 = VREF bias disabled 1 = VREF bias enabled
R2 (02h)	15	PLL_ENA (rw)	0b	PLL Enable 0 = disabled 1 = enabled
	14	TSHUT_ENA (rw)	0b	Thermal Sensor Enable 0 = Thermal sensor disabled 1 = Thermal sensor enabled
	11	OPCLK_ENA (rw)	0b	GPIO Clock Output Enable 0 = disabled 1 = enabled
	9	AINL_ENA (rw)	0b	Left Input Path Enable 0 = disabled 1 = enabled
	8	AINR_ENA (rw)	0b	Left Input Path Enable 0 = disabled 1 = enabled
	7	LIN34_ENA (rw)	0b	LIN34 Input PGA Enable 0 = disabled 1 = enabled
	6	LIN12_ENA (rw)	0b	LIN12 Input PGA Enable 0 = disabled 1 = enabled
	5	RIN34_ENA (rw)	0b	RIN34 Input PGA Enable 0 = disabled 1 = enabled
	4	RIN12_ENA (rw)	0b	RIN12 Input PGA Enable 0 = disabled 1 = enabled
	1	ADCL_ENA (rw)	0b	Left ADC Enable 0 = disabled 1 = enabled
	0	ADCR_ENA (rw)	0b	Right ADC Enable 0 = disabled 1 = enabled

Table 51 Power Management

CHIP RESET AND ID

The device ID can be read back from register 0. Writing to this register will reset the device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Reset / ID	15:0	SW_RESET_CHIP_ID [15:0] (rr)	8990h	Writing to this register resets all registers to their default state. Reading from this register will indicate device family ID 8990h.

Table 52 Chip Reset and ID

POWER DOMAINS

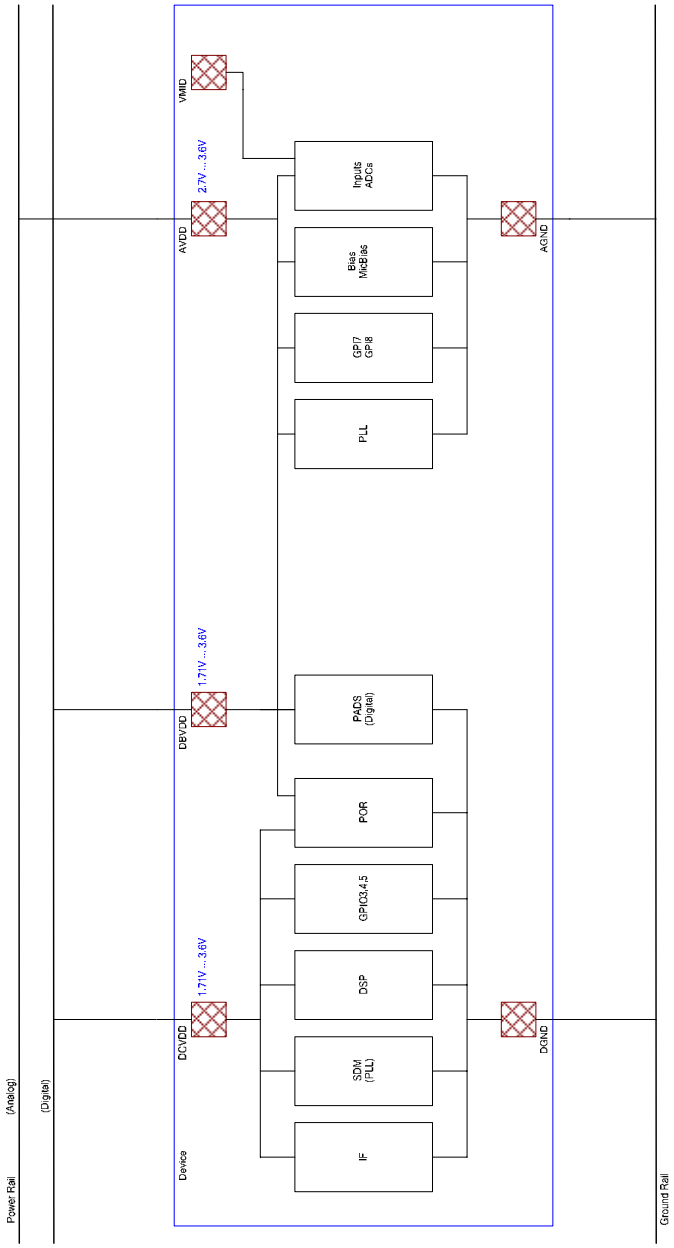


Figure 58 WM8953 Power Domains

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
0	0	Reset	SW_RESET_CHIP_ID[15:0]																1000_1001_1001_0000
1	1	Power Management (1)	0	0	0	0	0	0	0	0	0	0	0	MICBIAS_ENA	0	VMID_MODE[1:0]		VREF_ENA	0000_0000_0000_0000
2	2	Power Management (2)	PLL_ENA	TSHUT_ENA	1	0	OPCLK_ENA	0	AINL_ENA	AINR_ENA	LIN34_ENA	LIN12_ENA	RIN34_ENA	RIN12_ENA	0	0	ADCL_ENA	ADCR_ENA	0110_0000_0000_0000
3	3	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
4	4	Audio Interface (1)	AIFADCL_SRC	AIFADCR_SRC	AIFADC_TDM	AIFADC_TDM_CHAN	0	0	0	AIF_BCLK_INV	AIF_LRCLK_INV	AIF_WL[1:0]		AIF_FMT[1:0]		0	0	0	0100_0000_0101_0000
5	5	Audio Interface (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	ADC_COMP	ADC_COMPMODE	0	0100_0000_0000_0000
6	6	Clocking (1)	TOCLK_RATE	TOCLK_ENA	0	OPCLKDIV[3:0]				1	1	1	0	BCLK_DIV[3:0]				0	0000_0001_1100_1000
7	7	Clocking (2)	0	SYSCLK_SRC	CLK_FORCE	MCLK_DIV[1:0]		MCLK_INV	0	0	ADC_CLKDIV[2:0]			0	0	0	0	0	00p0_0000_0000_0000
8	8	Audio Interface (3)	AIF_MSTR	0	0	0	ADCLRC_DIR	ADCLRC_RATE[10:0]											0000_0000_0100_0000
9	9	Audio Interface (4)	0	0	AIF_TRIS	0	0	0	0	0	0	1	0	0	0	0	0	0	0000_0000_0100_0000
10	A	LRCLK Rate	0	0	0	0	0	AIF_LRCLKRATE	0	0	0	0	0	0	0	1	0	0	0000_0000_0000_0100
11	B	Reserved	0	0	0	0	0	0	0	p	1	1	0	0	0	0	0	0	0000_000p_1100_0000
12	C	Reserved	0	0	0	0	0	0	0	p	1	1	0	0	0	0	0	0	0000_000p_1100_0000
13	D	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
14	E	ADC CTRL	0	0	0	0	0	0	0	ADC_HPF_ENA	0	ADC_HPF_CUT[1:0]		0	0	0	ADCL_DATINV	ADCR_DATINV	0000_0001_0000_0000
15	F	Left ADC Digital Volume	0	0	0	0	0	0	0	ADC_VU	ADCL_VOL[7:0]								0000_000p_1100_0000
16	10	Right ADC Digital Volume	0	0	0	0	0	0	0	ADC_VU	ADCR_VOL[7:0]								0000_000p_1100_0000
17	11	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
18	12	GPIO CTRL 1	0	0	0	IRQ	TEMPOK	MICSHRT	MICDET	PLL_LCK	GPIO_STATUS[7:0]								0000_pppp_pppp_pppp
19	13	Reserved	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0001_0000_0000_0000
20	14	GPIO3 & GPIO4	GPIO4_DEB_ENA	GPIO4_IRQ_ENA	GPIO4_PU	GPIO4_PD	GPIO4_SEL[3:0]				GPIO3_DEB_ENA	GPIO3_IRQ_ENA	GPIO3_PU	GPIO3_PD	GPIO3_SEL[3:0]				0001_0000_0001_0000
21	15	GPIO5	0	0	0	1	0	0	0	0	GPIO5_DEB_ENA	GPIO5_IRQ_ENA	GPIO5_PU	GPIO5_PD	GPIO5_SEL[3:0]				0001_0000_0001_0000
22	16	GPIOCTRL 2	RD_3W_ENA	MODE_3W4W	0	0	TEMPOK_IRQ_ENA	MICSHRT_IRQ_ENA	MICDET_IRQ_ENA	PLL_LCK_IRQ_ENA	GPI8_DEB_ENA	GPI8_IRQ_ENA	0	GPI8_ENA	GPI7_DEB_ENA	GPI7_IRQ_ENA	0	GPI7_ENA	1000_0000_0000_0000
23	17	GPIO_POL	0	0	0	IRQ_INV	TEMPOK_POL	MICSHRT_POL	MICDET_POL	PLL_LCK_POL	GPIO_POL[7:0]								0000_1000_0000_0000
24	18	Left Line Input 1&2 Volume	0	0	0	0	0	0	0	IPVU[0]	LI12MUTE	LI12ZC	0	LIN12VOL[4:0]					0000_000p_1000_1011
25	19	Left Line Input 3&4 Volume	0	0	0	0	0	0	0	IPVU[1]	LI34MUTE	LI34ZC	0	LIN34VOL[4:0]					0000_000p_1000_1011
26	1A	Right Line Input 1&2 Volume	0	0	0	0	0	0	0	IPVU[2]	RI12MUTE	RI12ZC	0	RIN12VOL[4:0]					0000_000p_1000_1011
27	1B	Right Line Input 3&4 Volume	0	0	0	0	0	0	0	IPVU[3]	RI34MUTE	RI34ZC	0	RIN34VOL[4:0]					0000_000p_1000_1011
28	1C	Reserved	0	0	0	0	0	0	0	p	0	0	0	0	0	0	0	0	0000_000p_0000_0000
29	1D	Reserved	0	0	0	0	0	0	0	p	0	0	0	0	0	0	0	0	0000_000p_0000_0000
30	1E	Reserved	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0000_0000_0110_0110
31	1F	Reserved	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0000_0000_0010_0010

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
32	20	Reserved	0	0	0	0	0	0	0	p	0	1	1	1	1	0	0	1	0000_000p_0111_1001
33	21	Reserved	0	0	0	0	0	0	0	p	0	1	1	1	1	0	0	1	0000_000p_0111_1001
34	22	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0000_0000_0000_0011
35	23	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0000_0000_0000_0011
36	24	Reserved	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0000_0000_0101_0101
37	25	Reserved	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0000_0001_0000_0000
38	26	Reserved	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0000_0000_0111_1001
39	27	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
40	28	Input Mixer2	0	0	0	0	0	0	0	0	LMP4	LMN3	LMP2	LMN1	RMP4	RMN3	RMP2	RMN1	0000_0000_0000_0000
41	29	Input Mixer3	0	0	0	0	0	0	0	L34MNB	L34MNBST	0	L12MNB	L12MNBST	0	0	0	0	0000_0000_0000_0000
42	2A	Input Mixer4	0	0	0	0	0	0	0	R34MNB	R34MNBST	0	R12MNB	R12MNBST	0	0	0	0	0000_0000_0000_0000
43	2B	Input Mixer5	0	0	0	0	0	0	0	LI2BVOL[2:0]			0	0	0	0	0	0	0000_0000_0000_0000
44	2C	Input Mixer6	0	0	0	0	0	0	0	RI2BVOL[2:0]			0	0	0	0	0	0	0000_0000_0000_0000
45	2D	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
46	2E	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
47	2F	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
48	30	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
49	31	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
50	32	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
51	33	Reserved	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0000_0001_1000_0000
52	34	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
53	35	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
54	36	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
55	37	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
56	38	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
57	39	Anti-Pop	0	0	0	0	0	0	0	0	0	0	0	0	BUFIOEN	0	0	0	0000_0000_0000_0000
58	3A	MICBIAS	0	0	0	0	0	0	0	0	MCDSCTH[1:0]		MCDTHR[2:0]			MCD	0	MBSEL	0000_0000_0000_0000
59	3B	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
60	3C	PLL1	0	0	0	0	0	0	0	0	SDM	PRESCALE	0	0	PLLN[3:0]				0000_0000_0000_1000
61	3D	PLL2	0	0	0	0	0	0	0	0	PLLK1[7:0]								0000_0000_0011_0001
62	3E	PLL3	0	0	0	0	0	0	0	0	PLLK2[7:0]								0000_0000_0010_0110
117	75	Access Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EXT_ACCESS_ENA	0	0000_0000_0000_0000
122	7A	Extended ADC Control	ADCL_ADCR_LINK	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0010_0000_0000_0011

Note:

A bin default value of 'p' indicates a register field where a default value is not applicable e.g. a volume update bit.

REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Reset / ID	15:0	SW_RESET_CHIP_ID [15:0] (rr)	8990h	Writing to this register resets all registers to their default state. Reading from this register will indicate device family ID 8990h.
R1 (01h) Power Management (1)	15:8		00h	Reserved - Do Not Change
	7:5		000b	Reserved - Do Not Change
	4	MICBIAS_ENA (rw)	0b	MICBIAS Enable 0 = OFF (high impedance output) 1 = ON
	3		0b	Reserved - Do Not Change
	2:1	VMID_MODE [1:0] (rw)	00b	Vmid Divider Enable and Select 00 = Vmid disabled (for OFF mode) 01 = 2 x 50kΩ divider (Normal mode) 10 = 2 x 250kΩ divider (Standby mode) 11 = 2 x 5kΩ divider (for fast start-up)
	0	VREF_ENA (rw)	0b	VREF Enable (Bias for all analogue functions) 0 = VREF bias disabled 1 = VREF bias enabled
R02 (02h) Power Management (2)	15	PLL_ENA (rw)	0b	PLL Enable 0 = disabled 1 = enabled
	14	TSHUT_ENA (rw)	1b	Thermal Sensor Enable 0 = Thermal sensor disabled 1 = Thermal sensor enabled
	13:12		10b	Reserved - Do Not Change
	11	OPCLK_ENA (rw)	0b	GPIO Clock Output Enable 0 = disabled 1 = enabled
	10		0b	Reserved - Do Not Change
	9	AINL_ENA (rw)	0b	Left Input Path Enable 0 = disabled 1 = enabled
	8	AINR_ENA (rw)	0b	Right Input Path Enable 0 = disabled 1 = enabled
	7	LIN34_ENA (rw)	0b	LIN34 Input PGA Enable 0 = disabled 1 = enabled
	6	LIN12_ENA (rw)	0b	LIN12 Input PGA Enable 0 = disabled 1 = enabled
	5	RIN34_ENA (rw)	0b	RIN34 Input PGA Enable 0 = disabled 1 = enabled
	4	RIN12_ENA (rw)	0b	RIN12 Input PGA Enable 0 = disabled 1 = enabled
	3:2		00b	Reserved - Do Not Change
	1	ADCL_ENA (rw)	0b	Left ADC Enable 0 = disabled 1 = enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	ADCR_ENA (rw)	0b	Right ADC Enable 0 = disabled 1 = enabled
R03 (03h) Power Management (3)	15:0		0000h	Reserved - Do Not Change
R04 (04h) Audio Interface (1)	15	AIFADCL_SRC	0b	Left Digital Audio channel source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel
	14	AIFADCR_SRC	1b	Right Digital Audio channel source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
	13	AIFADC_TDM	0b	ADC TDM Enable 0 = Normal ADCDAT operation 1 = TDM enabled on ADCDAT
	12	AIFADC_TDM_ CHAN	0b	ADCDAT TDM Channel Select 0 = ADCDAT outputs data on slot 0 1 = ADCDAT output data on slot 1
	11:9		0b	Reserved - Do Not Change
	8	AIF_BCLK_INV	0b	BCLK Invert 0 = BCLK not inverted 1 = BCLK inverted
	7	AIF_LRCLK_INV	0b	Right, left and I^2S modes – LRCLK polarity 0 = normal LRCLK polarity 1 = invert LRCLK polarity
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)
	6:5	AIF_WL [1:0]	10b	Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits
	4:3	AIF_FMT [1:0]	10b	Digital Audio Interface Format 00 = Right justified 01 = Left justified 10 = I^2S Format 11 = DSP Mode
	2:0		0b	Reserved - Do Not Change
R05 (05h) Audio Interface (2)	15:8		40h	Reserved - Do Not Change
	7:3		00000b	Reserved - Do Not Change
	2	ADC_COMP	0b	ADC Companding Enable 0 = disabled 1 = enabled
	1	ADC_COMPMODE	0b	ADC Companding Type 0 = µ-law 1 = A-law
	0		0b	Reserved - Do Not Change

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R06 (06h) Clocking (1)	15	TOCLK_RATE	0b	Timeout Clock Rate (Selects clock to be used for volume update timeout and GPIO input de-bounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)
	14	TOCLK_ENA	0b	Timeout Clock Enable (This clock is required for volume update timeout and GPIO input de-bounce) 0 = disabled 1 = enabled
	13		0b	Reserved - Do Not Change
	12:9	OPCLKDIV [3:0]	0000b	GPIO Output Clock Divider 0000 = SYSCLK 0001 = SYSCLK / 2 0010 = SYSCLK / 3 0011 = SYSCLK / 4 0100 = SYSCLK / 5.5 0101 = SYSCLK / 6 0110 = SYSCLK / 8 0111 = SYSCLK / 12 1000 = SYSCLK / 16 1001 to 1111 = Reserved
	8:5		1110b	Reserved - Do Not Change
	4:1	BCLK_DIV [3:0]	0100b	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 = SYSCLK / 32 1110 = SYSCLK / 44 1111 = SYSCL:K / 48
	0		0b	Reserved - Do Not Change
R07 (07h) Clocking (2)	15		0b	Reserved - Do Not Change
	14	SYSCLK_SRC	0b	SYSCLK Source Select 0 = MCLK 1 = PLL output
	13	CLK_FORCE	0b	Forces Clock Source Selection 0 = Existing SYSCLK source (MCLK or PLL output) must be active when changing to a new clock source. 1 = Allows existing MCLK source to be disabled before changing to a new clock source.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	12:11	MCLK_DIV [1:0]	00b	SYSCLK Pre-divider. Clock source (MCLK or PLL output) will be divided by this value to generate SYSCLK. 00 = Divide SYSCLK by 1 01 = Reserved 10 = Divide SYSCLK by 2 11 = Reserved
	10	MCLK_INV	0b	MCLK Invert 0 = Master clock not inverted 1 = Master clock inverted
	9:8		00b	Reserved - Do Not Change
	7:5	ADC_CLKDIV [2:0]	000b	ADC Sample Rate Divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2.0 011 = SYSCLK / 3.0 100 = SYSCLK / 4.0 101 = SYSCLK / 5.5 110 = SYSCLK / 6.0 111= Reserved
	4:0		00000b	Reserved - Do Not Change
R08 (08h) Audio Interface (3)	15	AIF_MSTR	0b	Audio Interface Master Mode Select 0 = Slave mode 1 = Master mode
	14:12		000b	Reserved - Do Not Change
	11	ADCLRC_DIR	0b	ADCLRC Direction (Forces ADCLRC clock to be output in slave mode) 0 = ADCLRC normal operation 1 = ADCLRC clock output enabled
	10:0	ADCLRC_RATE [10:0]	040h	ADCLRC Rate ADCLRC clock output = BCLK / ADCLRC_RATE Integer (LSB = 1) Valid from 8..2047
R09 (09h) Audio Interface (4)	15:14		00b	Reserved - Do Not Change
	13	AIF_TRIS	0b	Audio Interface and GPIO Tristate 0 = Audio interface and GPIO pins operate normally 1 = Tristate all audio interface and GPIO pins
	12		0b	Reserved - Do Not Change
	11:0		040h	Reserved - Do Not Change
R10 (0Ah) LRCLK Rate	15:11		00000b	Reserved - Do Not Change
	10	AIF_LRCLKRATE	0b	LRCLK Rate 0 = Normal mode (256 * fs) 1 = USB mode (272 * fs)
	9:8		00b	Reserved - Do Not Change
	7:0		04h	Reserved - Do Not Change
R11 (0Bh)	15:0		0060h	Reserved - Do Not Change
R12 (0Ch)	15:0		0060h	Reserved - Do Not Change
R13 (0Dh)	15:0		0000h	Reserved - Do Not Change
R14 (0Eh) ADC Control	15:9		00h	Reserved - Do Not Change
	8	ADC_HPF_ENA	1b	ADC Digital High Pass Filter Enable 0 = disabled 1 = enabled
	7		0b	Reserved - Do Not Change

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:5	ADC_HPF_CUT [1:0]	00b	ADC Digital High Pass Filter Cut-Off Frequency (fc) 00 = Hi-fi mode (fc=4Hz at fs=48kHz) 01 = Voice mode 1 (fc=127Hz at fs=16kHz) 10 = Voice mode 2 (fc=130Hz at fs=8kHz) 11 = Voice mode 3 (fc=267Hz at fs=8kHz) (Note: fc scales with sample rate. See Table 16 for cut-off frequencies at all supported sample rates)
	4:2		000b	Reserved - Do Not Change
	1	ADCL_DATINV	0b	Left ADC Invert 0 = Left ADC output not inverted 1 = Left ADC output inverted
	0	ADCR_DATINV	0b	Right ADC Invert 0 = Right ADC output not inverted 1 = Right ADC output inverted
R15 (0Fh) Left ADC Digital Volume	15:9		00h	Reserved - Do Not Change
	8	ADC_VU	N/A	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCL_VOL [7:0]	1100_ 0000b (0dB)	Left ADC Digital Volume (See Table 14 for volume range)
R16 (10h) Right ADC Digital Volume	15:9		00h	Reserved - Do Not Change
	8	ADC_VU	N/A	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCR_VOL [7:0]	1100_ 0000b (0dB)	Right ADC Digital Volume (See Table 14 for volume range)
R17 (11h)	15:0		0000h	Reserved - Do Not Change
R18 (12h) GPIO Control (1)	15:13		000b	Reserved - Do Not Change
	12	IRQ (ro)	Read Only	IRQ Readback (Allows polling of IRQ status)
	11	TEMPOK (rr)	Read or Reset	Temperature OK status Read- 0 = Device temperature NOT ok 1 = Device temperature ok Write - 1 = Reset TEMPOK latch
	10	MICSHRT (rr)	Read or Reset	MICBIAS short status Read- 0 = MICBIAS ok 1 = MICBIAS shorted Write- 1 = Reset MICSHRT latch
	9	MICDET (rr)	Read or Reset	MICBIAS detect status MICBIAS microphone detect Readback Read- 0 = No Microphone detected 1 = Microphone detected Write- 1 = Reset MICDET latch

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8	PLL_LCK (rr)	Read or Reset	PLL Lock status Read- 0 = PLL NOT locked 1 = PLL locked Write- 1 = Reset PLL_LCK latch
	7:0	GPIO_STATUS [7:0] (rr)	Read or Reset	GPIO and GPI Input Pin Status GPIO_STATUS[7] = GPI8 pin status GPIO_STATUS[6] = GPI7 pin status GPIO_STATUS[5] = Reserved GPIO_STATUS[4] = GPIO5 pin status GPIO_STATUS[3] = GPIO4 pin status GPIO_STATUS[2] = GPIO3 pin status GPIO_STATUS[1] = Reserved GPIO_STATUS[0] = Reserved
R19 (13h)	15:0		1000h	Reserved - Do Not Change
R20 (14h) GPIO3 and GPIO4	15	GPIO4_DEB_ENA	0b	GPIO4 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	14	GPIO4_IRQ_ENA	0b	GPIO4 IRQ Enable 0 = disabled 1 = enabled (GPIO4 input will generate IRQ)
	13	GPIO4_PU	0b	GPIO4 Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	12	GPIO4_PD	1b	GPIO4 Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)
	11:8	GPIO4_SEL [3:0]	0000b	GPIO4 Function Select 0000 = Input pin 0001 = Clock output (f=SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = PLL Lock output 0101 = Temperature OK output 0110 = SDOUT data output 0111 = IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 to 1111 = Reserved
	7	GPIO3_DEB_ENA	0b	GPIO3 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	6	GPIO3_IRQ_ENA	0b	GPIO3 IRQ Enable 0 = disabled 1 = enabled (GPIO3 input will generate IRQ)
	5	GPIO3_PU	0b	GPIO3 Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	4	GPIO3_PD	1b	GPIO3 Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	GPIO3_SEL [3:0]	0000b	GPIO3 Function Select 0000 = Input pin 0001 = Clock output (f=SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = PLL Lock output 0101 = Temperature OK output 0110 = SDOUT data output 0111 = IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 to 1111 = Reserved
R21 (15h) GPIO5	15:8		10h	Reserved - Do Not Change
	7	GPIO5_DEB_ENA	0b	GPIO5 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	6	GPIO5_IRQ_ENA	0b	GPIO5 IRQ Enable 0 = disabled 1 = enabled (GPIO5 input will generate IRQ)
	5	GPIO5_PU	0b	GPIO5 Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	4	GPIO5_PD	1b	GPIO5 Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)
	3:0	GPIO5_SEL [3:0]	0000b	GPIO5 Function Select 0000 = Input pin 0001 = Clock output (f=SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = PLL Lock output 0101 = Temperature OK output 0110 = SDOUT data output 0111 = IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 to 1111 = Reserved
R22 (16h) GPI7 and GPI8	15	RD_3W_ENA	1b	3- / 4-wire readback configuration 1 = 3-wire mode 0 = 4-wire mode, using GPIO pin
	14	MODE_3W4W	0b	3-wire mode 0 = push 0/1 1 = open-drain 4-wire mode 0 = push 0/1 1 = wired-OR
	13:12		00b	Reserved - Do Not Change
	11	TEMPOK_IRQ_ENA	0b	Temperature Sensor IRQ Enable 0 = disabled 1 = enabled
	10	MICSHRT_IRQ_ENA	0b	MICBIAS short circuit detect IRQ Enable 0 = disabled 1 = enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	9	MICDET_IRQ_ENA	0b	MICBIAS current detect IRQ Enable 0 = disabled 1 = enabled
	8	PLL_LCK_IRQ_ENA	0b	PLL Lock IRQ Enable 0 = disabled 1 = enabled
	7	GPI8_DEB_ENA	0b	GPI8 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	6	GPI8_IRQ_ENA	0b	GPI8 IRQ Enable 0 = disabled 1 = enabled (GPI8 input will generate IRQ)
	5		0b	Reserved - Do Not Change
	4	GPI8_ENA	0b	GPI8 Input Pin Enable 0 = RIN3/GPI8 pin disabled as GPI8 input 1 = RIN3/GPI8 pin enabled as GPI8 input
	3	GPI7_DEB_ENA	0b	GPI7 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	2	GPI7_IRQ_ENA	0b	GPI7 IRQ Enable 0 = disabled 1 = enabled (GPI7 input will generate IRQ)
	1		0b	Reserved - Do Not Change
	0	GPI7_ENA	0b	GPI7 Input Pin Enable 0 = LIN3/GPI7 pin disabled as GPI7 input 1 = LIN3/GPI7 pin enabled as GPI7 input
R23 (17h) GPIO Control (2)	15:13		0000b	Reserved - Do Not Change
	12	IRQ_INV (rw)	0b	IRQ Invert 0 = IRQ output active high 1 = IRQ output active low
	11	TEMPOK_POL (rw)	1b	Temperature Sensor polarity 0 = Non-inverted 1 = Inverted
	10	MICSHRT_POL (rw)	0b	MICBIAS short circuit detect polarity 0 = Non-inverted 1 = Inverted
	9	MICDET_POL (rw)	0b	MICBIAS current detect polarity 0 = Non-inverted 1 = Inverted
	8	PLL_LCK_POL (rw)	0b	PLL Lock Polarity 0 = Non-inverted 1 = Inverted
	7:0	GPIO_POL[7:0] (rw)	00h	GPIOn Input Polarity 0 = Non-inverted 1 = Inverted GPIO_POL[7]: GPI8 polarity GPIO_POL[6]: GPI7 polarity GPIO_POL[5]: Reserved GPIO_POL[4]: GPIO5 polarity GPIO_POL[3]: GPIO4 polarity GPIO_POL[2]: GPIO3 polarity GPIO_POL[1]: Reserved GPIO_POL[0]: Reserved
R24 (18h)	15:9		00h	Reserved - Do Not Change

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
LIN12 Input PGA Volume	8	IPVU[0]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	LI12MUTE	1b	LIN12 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	LI12ZC	0b	LIN12 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	5		0b	Reserved - Do Not Change
	4:0	LIN12VOL [4:0]	01011b	LIN12 Volume (See Table 8 for PGA volume range)
R25 (19h)	15:9		00h	Reserved - Do Not Change
LIN34 Input PGA Volume	8	IPVU[1]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	LI34MUTE	1b	LIN34 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	LI34ZC	0b	LIN34 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	5		0b	Reserved - Do Not Change
	4:0	LIN34VOL [4:0]	01011b	LIN34 Volume (See Table 8 for PGA volume range)
R26 (1Ah)	15:9		00h	Reserved - Do Not Change
RIN12 Input PGA Volume	8	IPVU[2]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	RI12MUTE	1b	RIN12 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	RI12ZC	0b	RIN12 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	5		0b	Reserved - Do Not Change
	4:0	RIN12VOL [4:0]	01011b	RIN12 Volume (See Table 8 for PGA volume range)
R27 (1Bh)	15:9		00h	Reserved - Do Not Change
RIN34 Input PGA Volume	8	IPVU[3]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	RI34MUTE	1b	RIN34 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	RI34ZC	0b	RIN34 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	5		0b	Reserved - Do Not Change
	4:0	RIN34VOL [4:0]	01011b	RIN34 Volume (See Table 8 for PGA volume range)
R28 (1Ch)	15:0		0000h	Reserved - Do Not Change
R29 (1Dh)	15:0		0000h	Reserved - Do Not Change
R30 (1Eh)	15:0		0066h	Reserved - Do Not Change

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh)	15:0		0022h	Reserved - Do Not Change
R32 (20h)	15:0		0079h	Reserved - Do Not Change
R33 (21h)	15:0		0079h	Reserved - Do Not Change
R34 (22h)	15:0		0003h	Reserved - Do Not Change
R35 (23h)	15:0		0003h	Reserved - Do Not Change
R36 (24h)	15:0		0055h	Reserved - Do Not Change
R37 (25h)	15:0		0100h	Reserved - Do Not Change
R38 (26h)	15:0		0079h	Reserved - Do Not Change
R39 (27h)	15:0		0000h	Reserved - Do Not Change
R40 (28h)	15:8		00h	Reserved - Do Not Change
Input Mixers (2)	7	LMP4	0b	LIN34 PGA Non-Inverting Input Select 0 = LIN4 not connected to PGA 1 = LIN4 connected to PGA
	6	LMN3	0b	LIN34 PGA Inverting Input Select 0 = LIN3 not connected to PGA 1 = LIN3 connected to PGA
	5	LMP2	0b	LIN12 PGA Non-Inverting Input Select 0 = LIN2 not connected to PGA 1 = LIN2 connected to PGA
	4	LMN1	0b	LIN12 PGA Inverting Input Select 0 = LIN1 not connected to PGA 1 = LIN1 connected to PGA
	3	RMP4	0b	RIN34 PGA Non-Inverting Input Select 0 = RIN4 not connected to PGA 1 = RIN4 connected to PGA
	2	RMN3	0b	RIN34 PGA Inverting Input Select 0 = RIN3 not connected to PGA 1 = RIN3 connected to PGA
	1	RMP2	0b	RIN12 PGA Non-Inverting Input Select 0 = RIN2 not connected to PGA 1 = RIN2 connected to PGA
	0	RMN1	0b	RIN12 PGA Inverting Input Select 0 = RIN1 not connected to PGA 1 = RIN1 connected to PGA
R41 (29h)	15:9		00h	Reserved - Do Not Change
Input Mixers (3)	8	L34MNB	0b	LIN34 PGA Output to INMIXL Mute 0 = Mute 1 = Un-Mute
	7	L34MNBST	0b	LIN34 PGA Output to INMIXL Gain 0 = 0dB 1 = +30dB
	6		0b	Reserved - Do Not Change
	5	L12MNB	0b	LIN12 PGA Output to INMIXL Mute 0 = Mute 1 = Un-Mute
	4	L12MNBST	0b	LIN12 PGA Output to INMIXL Gain 0 = 0dB 1 = +30dB
	3:0		0h	Reserved - Do Not Change

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2Ah) Input Mixers (4)	15:9		00h	Reserved - Do Not Change
	8	R34MNB	0b	RIN34 PGA Output to INMIXR Mute 0 = Mute 1 = Un-Mute
	7	R34MNBST	0b	RIN34 PGA Output to INMIXR Gain 0 = 0dB 1 = +30dB
	6		0b	Reserved - Do Not Change
	5	R12MNB	0b	RIN12 PGA Output to INMIXR Mute 0 = Mute 1 = Un-Mute
	4	R12MNBST	0b	RIN12 PGA Output to INMIXR Gain 0 = 0dB 1 = +30dB
	3:0		0h	Reserved - Do Not Change
R43 (2Bh) Input Mixers (5)	15:9		00h	Reserved - Do Not Change
	8:6	LI2BVOL [2:0]	000b	LIN2 Pin to INMIXL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	5:0		000000b	Reserved - Do Not Change
R44 (2Ch) Input Mixers (6)	15:9		00h	Reserved - Do Not Change
	8:6	RI2BVOL [2:0]	000b	RIN2 Pin to INMIXR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	5:0		000000b	Reserved - Do Not Change
R45 (2Dh)	15:0		0000h	Reserved - Do Not Change
R46 (2Eh)	15:0		0000h	Reserved - Do Not Change
R47 (2Fh)	15:0		0000h	Reserved - Do Not Change
R48 (30h)	15:0		0000h	Reserved - Do Not Change
R49 (31h)	15:0		0000h	Reserved - Do Not Change
R50 (32h)	15:0		0000h	Reserved - Do Not Change
R51 (33h)	15:0		0180h	Reserved - Do Not Change
R52 (34h)	15:0		0000h	Reserved - Do Not Change
R53 (35h)	15:0		0000h	Reserved - Do Not Change
R54 (36h)	15:0		0000h	Reserved - Do Not Change
R55 (37h)	15:0		0000h	Reserved - Do Not Change
R56 (38h)	15:0		0000h	Reserved - Do Not Change
R57 (39h)	15:7		00h	Reserved - Do Not Change
Anti-Pop	6:4		000b	Reserved - Do Not Change

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	BUFIOEN	0b	Enables the VGS / R current generator and the analogue input bias 0 = Disabled 1 = Enabled
	2:0		000b	Reserved - Do Not Change
R58 (3Ah)	15:8		00h	Reserved - Do Not Change
Microphone Bias	7:6	MCDSCTH [1:0]	00b	MICBIAS Short Circuit Current Detect Threshold 00 = 600uA 01 = 1200uA 10 = 1800uA 11 = 2400uA These values are for AVDD=3.3V and scale proportionally with AVDD.
	5:3	MDCTHR [2:0]	000b	MICBIAS Current Detect Threshold 000 = 200uA 001 = 350uA 010 = 500uA 011 = 650uA 100 = 800uA 101 = 950uA 110 = 1100uA 111 = 1200uA These values are for AVDD=3.3V and scale proportionally with AVDD.
	2	MCD	0b	MICBIAS Current and Short Circuit Detect Enable 0 = disabled 1 = enabled
	1		0b	Reserved - Do Not Change
	0	MBSEL	0b	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD
R59 (3Bh)	15:0		0000h	Reserved - Do Not Change
R60 (3Ch)	15:8		00h	Reserved - Do Not Change
PLL (1)	7	SDM	0b	Enable PLL Integer Mode 0 = Integer mode 1 = Fractional mode
	6	PRESCALE	0b	Divide MCLK by 2 at PLL input 0 = Divide by 1 1 = Divide by 2
	5:4		00b	Reserved - Do Not Change
	3:0	PLLN [3:0]	8h	Integer (N) part of PLL frequency ratio. Use values greater than 5 and less than 13.
R61 (3Dh)	15:8		00h	Reserved - Do Not Change
PLL (2)	7:0	PLLK [15:8]	31h	Fractional (K) part of PLL frequency ratio (Most significant bits)
R62 (3Eh)	15:8		00h	Reserved - Do Not Change
PLL (2)	7:0	PLLK [7:0]	26h	Fractional (K) part of PLL frequency ratio (Least significant bits)
R63 (3Fh) to R116 (74h)	Reserved			
R117 (75h)	15:2		0000h	Reserved - Do Not Change
Access Control	1	EXT_ACCESS_ENA	0b	Extended Register Map Access 0 = disabled 1 = enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0		0b	Reserved - Do Not Change
R118 (76h) to R121 (79h)	Reserved			
R122 (7Ah) Extended ADC Control	15	ADCL_ADCR_LINK	0b	0 = ADC Sync disabled 1 = ADC Sync enabled
	14:0		2003h	Reserved - Do Not Change
R123 (7Bh) to R127 (7Fh)	Reserved			

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.05dB	0		0.454 fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.546s			
Stopband Attenuation	f > 0.546 fs	-60			dB
Group Delay			18/fs		

ADC FILTER RESPONSES

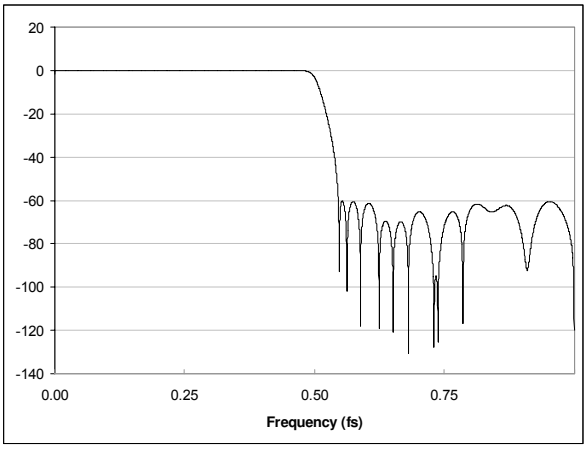


Figure 59 ADC Digital Filter Frequency Response

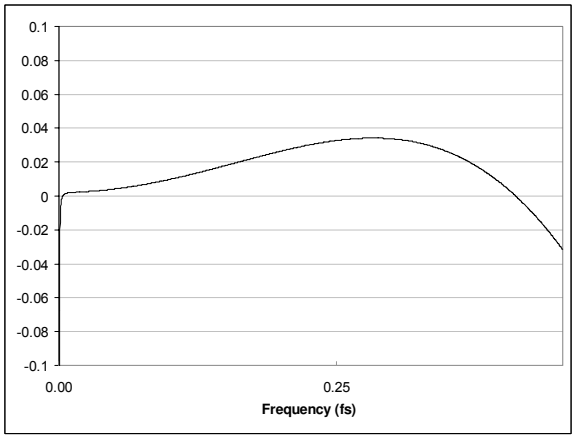


Figure 60 ADC Digital Filter Ripple

ADC HIGH PASS FILTER RESPONSES

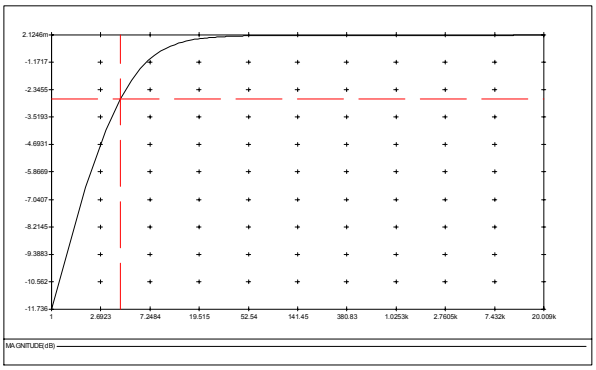


Figure 61 ADC Digital High Pass Filter Frequency Response (48kHz, Hi-Fi Mode, ADC_HPF_CUT[1:0]=00)

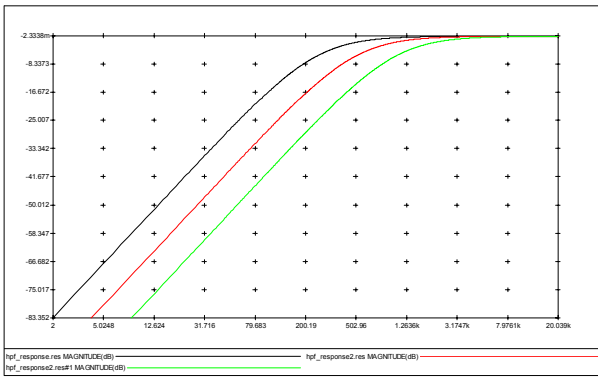
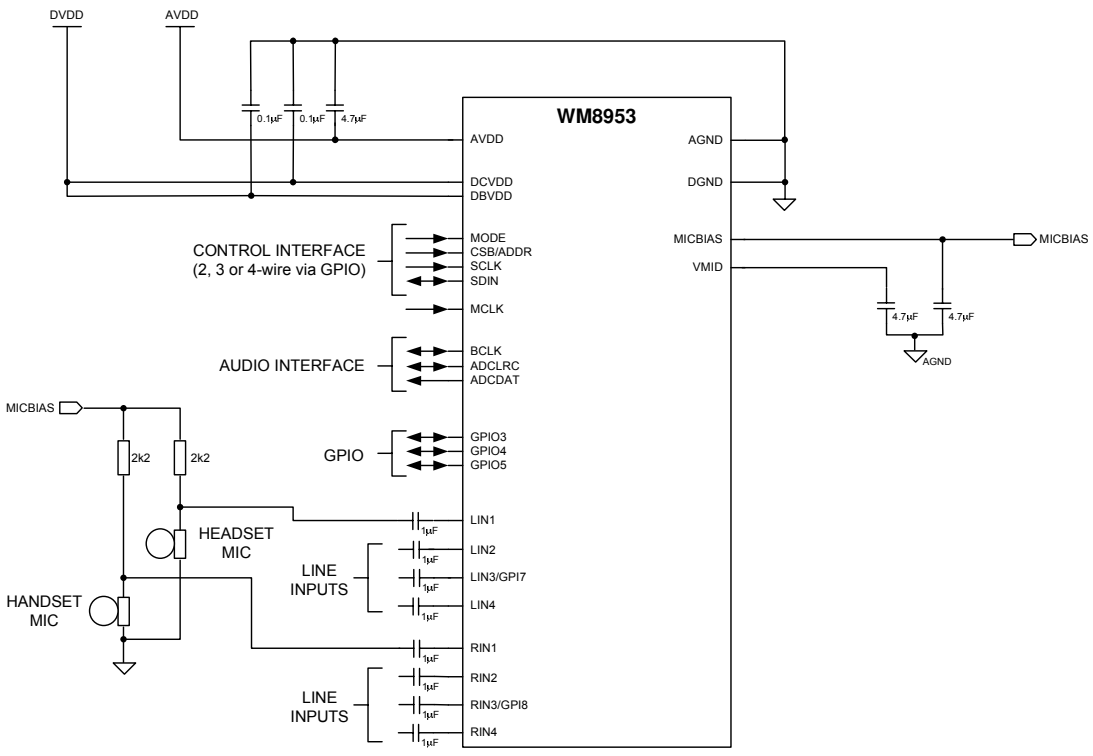


Figure 62 ADC Digital High Pass Filter Ripple (48kHz, Voice Mode, ADC_HPF_CUT=01, 10 and 11)

APPLICATIONS INFORMATION

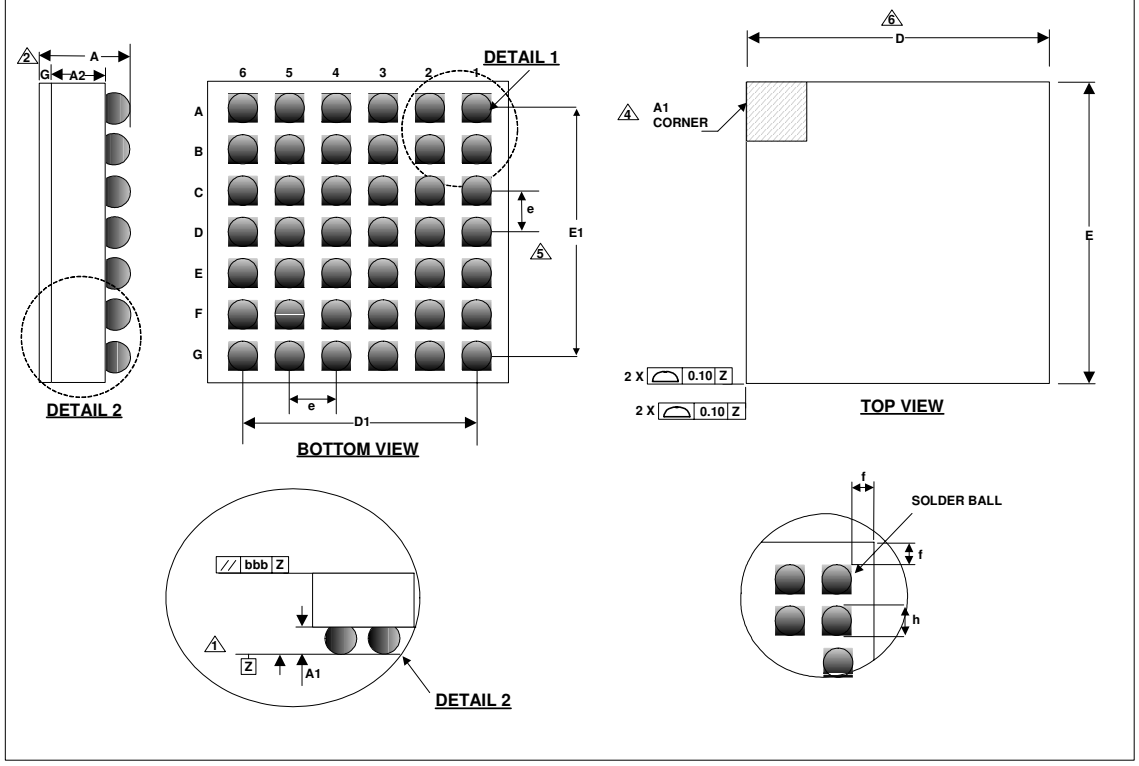
RECOMMENDED EXTERNAL COMPONENTS



Notes:
1. Wolfson recommend using a single, common ground reference. Where this is not possible care should be taken to optimise split ground configuration for audio performance.
2. Supply decoupling capacitors on DCVDD, DBVDD and AVDD should be positioned as close to the WM8953 as possible. Values indicated are minimum requirements.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.
4. The 2k2 MICBIAS resistors on each of the MIC inputs are typical values and will be suitable for many electret type microphones. However, it is recommended that engineers refer to individual microphone specifications prior to finalising the value of this component.

PACKAGE DIMENSIONS

B: 42 BALL W-CSP PACKAGE 3.226 x 3.440 x 0.7mm BODY, 0.50 mm BALL PITCH **DM049.C**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.615	0.7	0.785	
A1	0.225	0.250	0.275	
A2	0.355	0.380	0.405	
D		3.226 BSC		
D1		2.500 BSC		
E		3.440 BSC		
E1		3.00 BSC		
e		0.50 BSC		5
f	0.060 BSC			
g	0.035	0.070	0.105	
h		0.315 BSC		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

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