WM8900

Ultra Low Power CODEC for Portable Multimedia Applications Featuring Class G Ground Referenced Headphone Driver

DESCRIPTION

The WM8900 is designed for portable multimedia applications requiring low power consumption, high performance audio and a compact form factor. Pop and click optimised ground referenced headphone amplifiers provide high quality audio performance and improved bass response whilst also eliminating bulky headphone capacitors. Headphone amplifier playback power consumption is minimised by implementing an efficient class G amplifier powered by adaptive charge pump technology. Flexible analogue signal routing and digital signal processing capabilities enable advanced audio signal manipulation for fully featured multimedia applications whilst minimising power consumption.

Stereo 24bit multi-bit sigma-delta ADCs and DACs are used with over-sampling digital interpolation and decimation filters. The master clock can be input directly or generated internally by an integrated low power FLL. WM8900 operates at analogue supply voltages down to 2.4v. The digital core can operate at voltages down to 1.8v to save power. Different sections of the chip can also be powered down under software control. The WM8900 is supplied in a very small and thin 5x5x0.55mm QFN package, ideal for use in hand-held and portable systems

Low power, high performance audio features can be realized with a minimal set of small form factor external components, reducing BOM costs and PCB dimensions

FEATURES

- DAC to HP SNR 97dB ('A' weighted, 2.4V)
- DAC to HP THD -82dB at 48kHz Fs, 2.4V
- ADC SNR 95dB ('A' weighted, 3.3V)
- ADC THD -84dB at 48kHz Fs, 2.4V

- **Highly Flexible Input and Output Configuration**
  - 2 single ended or pseudo differential mic inputs
  - 2 stereo line inputs (eg. Line In / FM tuner)
  - Up to +48dB microphone/line input gain
  - Stereo output mixers with -15dB to +6dB gain range; mixing DAC outputs, line, auxiliary and mic inputs

- **Class-G Ultra-low Power Headphone Driver**
  - Up to 12.4mW per channel output power into 32Ω at 3.3V
  - Up to 6.6mW per channel output power into 32Ω at 2.4V
  - Ground referenced outputs
  - Pop and click suppression circuitry

- **Soft Mute Control**

- **Low Power Consumption with User Selectable Modes**
  - 9 mW stereo headphone playback (32Ω) (AVDD = 2.4V, DCVDD = 1.8V, 48k fs)
  - 6 mW stereo headphone playback (32Ω) (AVDD = 2.4V, DCVDD = 1.8V, 8k fs, quiescent)
  - 5 mW bypass mode. Line in to stereo headphone playback (32Ω) (AVDD = 2.4V, DCVDD = 1.8V)

- **Low Supply Voltages**
  - Analogue: 2.4V to 3.3V
  - Digital core: 1.8V to 3.3V
  - Digital I/O: 1.8V to 3.3V
  - Charge Pump High: 2.4V to 3.3V
  - Charge Pump Low: 1.6V to 3.3V

- **Low Power FLL**
  - Supports MCLK input up to 19.2MHz or DACLRC input down to 8kHz

- **TDM Mode –** dual data time slots for ADC and DAC

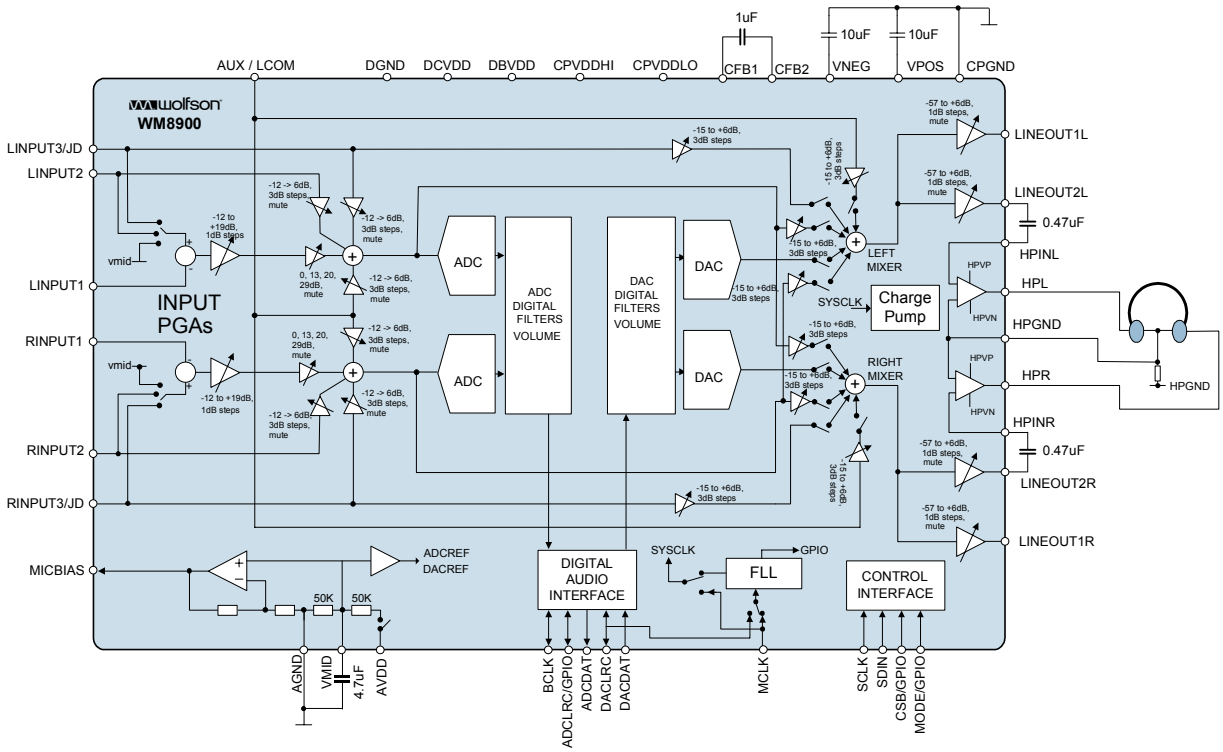
- **Audio Sample Rates (kHz):** 8, 11.025, 16, 22.05, 24, 32, 44.1, 48 generated internally from master clock

- 5 x 5 x 0.55mm 40 lead QFN package
- -25 ºC - +85ºC temperature range

APPLICATIONS

- MP3 players
- Portable Multimedia Applications
- Multimedia Handsets

BLOCK DIAGRAM



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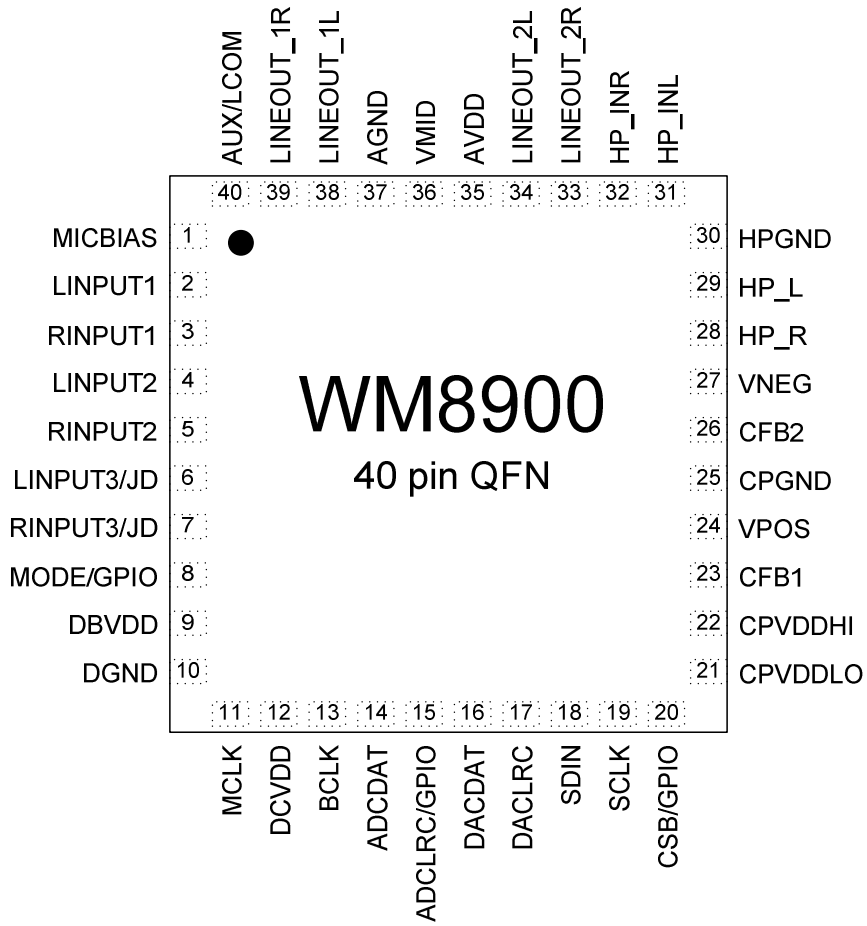
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8900LGEFK/V	-25°C to +85°C	40-lead QFN (5x5x0.55mm) (Pb-free)	MSL3	260°C
WM8900LGEFK/RV	-25°C to +85°C	40-lead QFN (5x5x0.55mm) (Pb-free, tape and reel)	MSL3	260°C

Note:
Reel quantity = 3500
Tube quantity = 95

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	MICBIAS	Analogue Output	Microphone Bias
2	LINPUT1	Analogue Input	Left Channel Input 1 (inverting)
3	RINPUT1	Analogue Input	Right Channel Input 1 (inverting)
4	LINPUT2	Analogue Input	Left Channel Input 2 (non-inverting)
5	RINPUT2	Analogue Input	Right Channel Input 2 (non-inverting)
6	LINPUT3 / JD	Analogue Input	Left Channel Input 3 or Jack Detect (non-inverting)
7	RINPUT3 / JD	Analogue Input	Right Channel Input 3 or Jack Detect (non-inverting)
8	MODE / GPIO	Digital Input / Output	2-wire / 3-wire control interface mode select or GPIO
9	DBVDD	Supply	Digital Buffer (I/O) Supply
10	DGND	Supply	Digital Ground (return path for both DCVDD and DBVDD)
11	MCLK	Digital Input	Master Clock
12	DCVDD	Supply	Digital Supply (Digital Core and FLL Digital)
13	BCLK	Digital Input / Output	Audio Interface Bit Clock
14	ADCDAT	Digital Output	ADC Digital Audio Data
15	ADCLRC / GPIO	Digital Input / Output	Audio Interface ADC Left/Right Clock or GPIO pin
16	DACDAT	Digital Input	DAC Digital Audio Data
17	DACLRC	Digital Input / Output	Audio Interface DAC Left / Right Clock
18	SDIN	Digital Input/Output	Control Interface Data Input / 2-wire Acknowledge output
19	SCLK	Digital Input	Control Interface Clock Input
20	CSB / GPIO	Digital Input / Output	Chip select or GPIO
21	CPVDDLO	Supply	Lower Supply for charge pump typically 1.8v
22	CPVDDHI	Supply	Supply for charge pump 2.4 to 3.3v
23	CFB1	Analogue Output	Flyback capacitor connection 1
24	VPOS	Analogue Output	Headphone positive supply decoupling capacitor
25	CPGND	Supply	Ground for Headphone Charge Pump
26	CFB2	Analogue Output	Flyback capacitor connection 2
27	VNEG	Analogue Output	Headphone negative supply decoupling capacitor
28	HP_R	Analogue Output	Right headphone output
29	HP_L	Analogue Output	Left headphone output
30	HPGND	Analogue Input	Headphone ground reference
31	HP_INL	Analogue Input	Left channel input to headphone driver
32	HP_INR	Analogue Input	Right channel input to headphone driver
33	LINEOUT_2R	Analogue Output	Right channel line output 2
34	LINEOUT_2L	Analogue Output	Left channel line output 2
35	AVDD	Supply	Analogue Supply (DAC, ADC, Input Amps, Lineout, Mixers & FLL Analogue)
36	VMID	Analogue Output	Midrail Voltage Decoupling Capacitor
37	AGND	Supply	Analogue Ground
38	LINEOUT_1L	Analogue Output	Left channel line output 1
39	LINEOUT_1R	Analogue Output	Right channel line output 1
40	AUX / LCOM	Analogue Input	Aux Mono Input / Low noise Line input ground connection

Note:

It is recommended that the PCB is laid out with a single ground plane. The QFN ground paddle should be tracked directly to AGND on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages	-0.3V	+3.63V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
3. DCVDD must be <= DBVDD.
4. DBVDD and DCVDD must be <= AVDD.
5. CPVDDLO must be <= CPVDDHI

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.7		3.6	V
Digital supply range (Buffer)	DBVDD	1.7		3.6	V
Analogue supply AVDD	AVDD	2.28		3.6	V
Charge Pump Analog Supply	CPVDDLO	1.6		3.6	V
Charge Pump Analog Supply	CPVDDHI	2.28		3.6	V
Ground	DGND, AGND, CPGND		0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD=1.8V, DBVDD=1.8V, DGND=AGND=CPGND=HPGND=0V, AVDD=CPVDDHI=2.4V, CPVDDLO=1.8V; T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, LINPUT3, RINPUT2, RINPUT3)						
Full-scale Input Signal Level – AVDD = 3.3v V_{INFS} is proportional to AVDD - V_{INFS} = (AVDD/3.3) x 1Vrms	V_{INFS}	L/RINPUT1 Single-ended		1.0 0		Vrms dBV
		L/RINPUT2/3 Differential MIC		0.5 -6		Vrms dBV
		L/RINPUT2/3 Boost or bypass path		1.0 0		Vrms dBV
		L/RINPUT3 Boost + bypass path		1.0 0		Vrms dBV
Full-scale Input Signal Level – AVDD = 3.0v	V_{INFS}	L/RINPUT1 Single-ended		0.9091 -0.828		Vrms dBV
		L/RINPUT2/3 Differential MIC		0.455 -6.84		Vrms dBV
		L/RINPUT2/3 Boost or bypass path		0.9091 -0.828		Vrms dBV
		L/RINPUT3 Boost + bypass path		0.9091 -0.828		Vrms dBV
Full-scale Input Signal Level – AVDD = 2.4v	V_{INFS}	L/RINPUT1 Single-ended		0.727 -2.77		Vrms dBV
		L/RINPUT2/3 Differential MIC		0.364 -8.79		Vrms dBV
		L/RINPUT2/3 Boost or bypass path		0.727 -2.77		Vrms dBV
		L/RINPUT3 Boost + bypass path		0.727 -2.77		Vrms dBV
Mic PGA equivalent input noise		0 to 20kHz, +19dB gain		150		uV

Test Conditions

DCVDD=1.8V, DBVDD=1.8V, DGND=AGND=CPGND=HPGND=0V, AVDD=CPVDDHI=2.4V, CPVDDLO=1.8V; T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input resistance (Note that input boost and bypass path resistances will be seen in parallel with PGA input resistance when these paths are enabled)	R_{INPUT1}	+19dB PGA gain Differential or single-ended MIC configuration		2		kΩ
	R_{INPUT1}	0dB PGA gain Differential or single-ended MIC configuration		10		kΩ
	R_{INPUT1}	-12dB PGA gain Differential or single-ended MIC configuration		16		kΩ
	R_{INPUT2}, R_{INPUT3}	(Constant for all gains) Differential MIC configuration		20		kΩ
	R_{INPUT2}, R_{INPUT3}	Max boost gain L/RINPUT2/3 to boost		7.5		kΩ
	R_{INPUT2}, R_{INPUT3}	0dB boost gain L/RINPUT2/3 to boost		15		kΩ
	R_{INPUT2}, R_{INPUT3}	Min boost gain L/RINPUT2/3 to boost		60		kΩ
	R_{INPUT3}	Max bypass gain L/RINPUT2/3 to bypass		10		kΩ
	R_{INPUT3}	Min bypass gain L/RINPUT2/3 to bypass		112		kΩ
	R_{AUX}	Max boost gain AUX to boost		4.4		kΩ
	R_{AUX}	0dB boost gain AUX to boost		8.61		kΩ
	R_{AUX}	Min boost gain AUX to boost		34.3		kΩ
	R_{AUX}	Max boost gain AUX to bypass		5.75		kΩ
	R_{AUX}	0dB boost gain AUX to bypass		11.41		kΩ
	R_{AUX}	Min boost gain AUX to bypass		63.65		kΩ
Input capacitance				10		pF
MIC Programmable Gain Amplifier (PGA)						
Programmable Gain			-12		+19	dB
Programmable Gain Step Size		Guaranteed monotonic		1		dB
Mute Attenuation				100		dB
Selectable Input Gain Boost						
Gain Boost Steps		Input from PGA		0, 13, 20, 29, MUTE		dB
		Input from L/RINPUT2 or L/RINPUT3		-12, -6, 0, 6, MUTE		dB

Test Conditions

DCVDD=1.8V, DBVDD=1.8V, DGND=AGND=CPGND=HPGND=0V, AVDD=CPVDDHI=2.4V, CPVDDLO=1.8V; TA = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, RINPUT2, LINPUT3, RINPUT3) to ADC Out						
Signal to Noise Ratio (A-weighted)	SNR	AVDD=3.3V		95		dB
		AVDD = 2.4V	83	91		
Signal to Noise Ratio (Unweighted)	SNR	AVDD=3.3V		93		dB
		AVDD = 2.4V		90		
Total Harmonic Distortion	THD	-1dBFs input, AVDD = 3.3V		-84		dB
		-1dBFs input, AVDD = 2.4V		-84	-76	
Total Harmonic Distortion + Noise	THD+N	-1dBFs input, AVDD = 3.3V		-82		dB
		-1dBFs input, AVDD = 2.4V		-82	-73	
ADC Channel Separation		1kHz full scale signal into ADC via L/RINPUT1, MIC amp (single-ended) and boost		90		dB
		1kHz full scale signal into ADC via L/RINPUT1/2, MIC amp (differential) and boost		90		dB
		1kHz full scale signal into ADC via L/RINPUT2 and boost		90		dB
		1kHz full scale signal into ADC via L/RINPUT3 and boost		90		dB
Line Input / MIC Separation (Quiescent input to ADC via boost; Output on ADC; 1kHz on L/RINPUT3 to HP out via bypass path)		Single-ended MIC input on L/RINPUT1		90		dB
		Differential MIC input using L/RINPUT2		90		dB
Boost / Bypass Separation (Quiescent L/RINPUT3 to HP outputs via bypass)		1kHz on LINPUT2 to ADC via boost only		90		dB
		1kHz on LINPUT1 to ADC via single-ended MIC PGA & boost		90		dB
Channel Matching		1kHz signal		0.2		dB
DAC to Line-Out (LINEOUT_1L / LINEOUT_1R or LINEOUT_2L / LINEOUT_2R with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD=2.4V	90	97		dB
Total Harmonic Distortion	THD	AVDD=2.4V		-89	-80	dB
Total Harmonic Distortion + Noise	THD+N	AVDD=2.4V		-88	-79	dB
DAC to Line-Out (LINEOUT_1L / LINEOUT_1R or LINEOUT_2L / LINEOUT_2R with 10kΩ / 50pF load) – Reduced Power Mode (DAC_BIAS = 01 = Half Bias)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 2.4V		92		dB
Signal to Noise Ratio (Unweighted)	SNR	AVDD = 2.4V		89		dB
Total Harmonic Distortion	THD	AVDD = 2.4V		-83		dB
Total Harmonic Distortion + Noise	THD+N	AVDD = 2.4V		-81		dB

Test Conditions

DCVDD=1.8V, DBVDD=1.8V, DGND=AGND=CPGND=HPGND=0V, AVDD=CPVDDHI=2.4V, CPVDDLO=1.8V; TA = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel Separation		1kHz signal		100		dB
L/RINPUT3 to HP_L / HP_R via bypass path						
Channel Separation				85		dB
DAC to LINEOUT_2L / LINEOUT_2R to HP_L / HP_R						
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 2.4V	90	97		dB
Total Harmonic Distortion	THD	AVDD = 2.4V		-92	-82	dB
Total Harmonic Distortion + Noise	THD+N	AVDD = 2.4V		-90	-80	dB
DAC to LINEOUT_2L / LINEOUT_2R to HP_L / HP_R – Reduced Power Mode (DAC_BIAS = 01 = Half Bias)						
0dB Full scale output voltage				AVDD/3.3		Vrms
Mute attenuation		1kHz, full scale signal		90		dB
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 2.4V		92		dB
Signal to Noise Ratio (Unweighted)	SNR	AVDD = 2.4V		90		dB
Total Harmonic Distortion	THD	AVDD=2.4V, R_L=32Ω, P_O= 5mW		-86		dB
		AVDD=2.4V, R_L=16Ω, P_O= 5mW		-82		dB
Total Harmonic Distortion + Noise	THD+N	AVDD=2.4V, R_L=32Ω, P_O=5mW		-84		dB
		AVDD=2.4V, R_L=16Ω, P_O= 5mW		-80		dB
PGA for LINEOUT_2L and LINEOUT_2R (can be used to control HP_L and HP_R amplitude or as a separate LINE OUT)						
Minimum Gain				-57		dB
Maximum Gain				+6		dB
Programmable Gain Step Size		Guaranteed monotonic		1		dB
PGA for LINEOUT_1L and LINEOUT_1R						
Minimum Gain				-57		dB
Maximum Gain				+6		dB
Programmable Gain Step Size		Guaranteed monotonic		1		dB
Analogue Reference Levels						
Midrail Reference Voltage	VMID		–3%	AVDD/2	+3%	V
Buffered Reference Voltage	VREF		–3%	AVDD/2	+3%	V
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	3mA load current MBSEL = 0	–5%	0.9×AVDD	+ 5%	V
		3mA load current MBSEL = 1	–5%	0.65×AVDD	+ 5%	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1kHz to 20kHz MICB_LVL = 0		25		nV/√Hz
		1K to 20kHz MICB_LVL = 1		17		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OH}-1mA			0.1×DBVDD	V

Test Conditions

DCVDD=1.8V, DBVDD=1.8V, DGND=AGND=CPGND=HPGND=0V, AVDD=CPVDDHI=2.4V, CPVDDLO=1.8V; TA = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capacitance				10		pF
Input leakage				1		uA
FLL						
Lock Time **See note 3**	Lock	FLL_SLOW_LOCK_REF = 0			509	Reference Clock Periods
		FLL_SLOW_LOCK_REF = 1			49	
Reference Clock Frequency	F_{REF}	LRCLK_REF_ENA = 0	48kHz		19.2MHz	
		LRCLK_REF_ENA = 1	8		48	kHz
Output Clock Frequency	F_{OUT}		10		20	MHz
Charge Pump						
Efficiency	CP_{EFF}		90			%
Startup Time	CP_{ST}				500	us
High Input	CPVDDHI		2.4		3.3	V
Low Input	CPVDDLO		1.6		3.3	V
VPOS	VPOS	Using CPVDDHI		CPVDDHI/2		V
		Using CPVDDLO		CPVDDLO/2		
VNEG	VNEG	Using CPVDDHI		-CPVDDHI/2		V
		Using CPVDDLO		-CPVDDLO/2		
Charge Pump output switching frequency	CPFREQ				1.536	MHz
Internal clock (SYSCLK) when using charge pump	SYSCLK	Using analog bypass e.g. LRIN1 to HP out	**See note 2**	12		MHz
Standby mode (All modules powered down, clocks stopped)						
Current consumption	$Idd_{(standby)}$			75	150	uA

Table 1 Electrical characteristics (see Note 1)

Notes:

1. The bias conditions are explained in Table 45 on page 12.
2. For a given headphone load, it is expected that the HP_L/HP_R output will begin to clip at 6dB lower amplitude for every 50% reduction in charge pump SYSCLK.
3. The FLL lock time is the time from last CSB edge of serial interface write to first clock edge of f_{OUT} from FLL (see Figure 46).

POWER CONSUMPTION

MODE	AVDD		DCVDD		DBVDD		CPVDDLO		CPVDDHI		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
Headphone Playback											
DAC to HP playback	3.3	2.2640	1.8	0.3600	1.8	0.0016	1.8	0.0000	3.3	0.8680	10.9865
32ohm load, quiescent	3.0	2.0490	1.8	0.3600	1.8	0.0016	1.8	0.0000	3.0	0.7560	9.0659
8kHz sample rate	2.4	1.6240	1.8	0.3600	1.8	0.0007	1.8	0.0000	2.4	0.5560	5.8812
DAC to HP playback	3.3	2.3720	1.8	0.4160	1.8	0.0024	1.8	1.6570	3.3	0.0233	11.6401
32ohm load, 0.1mW/channel	3.0	2.1480	1.8	0.4140	1.8	0.0021	1.8	1.6620	3.0	0.0207	10.2466
8kHz sample rate	2.4	1.7050	1.8	0.4150	1.8	0.0012	1.8	1.6270	2.4	0.0156	7.8073
DAC to HP playback	3.3	2.3860	1.8	0.4140	1.8	0.0023	1.8	6.7160	3.3	0.0762	20.9633
32ohm load, 2.0mW/channel	3.0	2.1620	1.8	0.4140	1.8	0.0020	1.8	6.8210	3.0	0.0683	19.7174
8kHz sample rate	2.4	1.7200	1.8	0.4150	1.8	0.0009	1.8	6.8700	2.4	0.0534	17.3835
LINE OUT 1 Playback											
DAC to Line Out 1 playback	3.3	2.4530	1.8	2.5350	1.8	0.0112	1.8	0.0000	3.3	0.0042	12.6918
10k load, quiescent	3.0	2.2090	1.8	2.5350	1.8	0.0096	1.8	0.0000	3.0	0.0033	11.2171
48kHz sample rate	2.4	1.7340	1.8	2.5350	1.8	0.0046	1.8	0.0000	2.4	0.0019	8.7374
DAC to Line Out 1 playback	3.3	2.2950	1.8	0.3590	1.8	0.0020	1.8	0.0000	3.3	0.0140	8.2372
10k load, quiescent	3.0	2.0680	1.8	0.3590	1.8	0.0014	1.8	0.0000	3.0	0.0033	6.8626
8kHz sample rate	2.4	1.6240	1.8	0.3590	1.8	0.0007	1.8	0.0000	2.4	0.0019	4.5496
MIC/LINE Record											
Mic to ADC record, quiescent	3.3	4.5250	1.8	2.4310	1.8	0.0451	1.8	0.0000	3.3	0.0041	19.4031
	3.0	4.3220	1.8	2.4380	1.8	0.0377	1.8	0.0001	3.0	0.0033	17.4323
48kHz sample rate	2.4	3.9280	1.8	2.4440	1.8	0.0225	1.8	0.0000	2.4	0.0019	13.8714
Mic to ADC record, quiescent	3.3	4.2830	1.8	0.4090	1.8	0.0077	1.8	0.0000	3.3	0.0042	14.8978
	3.0	4.1050	1.8	0.4100	1.8	0.0069	1.8	0.0000	3.0	0.0033	13.0753
8kHz sample rate	2.4	3.7540	1.8	0.4100	1.8	0.0037	1.8	0.0000	2.4	0.0018	9.7587
Line In to ADC record, quiescent	3.3	4.5030	1.8	2.4310	1.8	0.0467	1.8	0.0000	3.3	0.0042	19.3336
	3.0	4.3020	1.8	2.4370	1.8	0.0409	1.8	0.0000	3.0	0.0033	17.3761
48kHz sample rate	2.4	3.9100	1.8	2.4410	1.8	0.0222	1.8	0.0000	2.4	0.0019	13.8222
Line In to ADC record, quiescent	3.3	4.2590	1.8	0.4090	1.8	0.0074	1.8	0.0001	3.3	0.0042	14.8181
	3.0	4.0820	1.8	0.4100	1.8	0.0074	1.8	0.0000	3.0	0.0033	13.0070
8kHz sample rate	2.4	3.7360	1.8	0.4110	1.8	0.0038	1.8	0.0000	2.4	0.0018	9.7176
Bypass Path to Headphone											
Line In to HP bypass path	3.3	0.7900	1.8	0.5410	1.8	0.0086	1.8	0.0000	3.3	1.6490	9.0380
32ohm load, quiescent	3.0	0.7220	1.8	0.5400	1.8	0.0071	1.8	0.0000	3.0	1.4570	7.5219
	2.4	0.5870	1.8	0.5410	1.8	0.0035	1.8	0.0000	2.4	1.1010	5.0312
Line In to HP bypass path	3.3	0.8680	1.8	0.5350	1.8	0.0086	1.8	1.5490	3.3	0.1130	7.0040
32ohm load, 0.1mW/channel	3.0	0.7950	1.8	0.5350	1.8	0.0071	1.8	1.5540	3.0	0.1020	6.4639
	2.4	0.6540	1.8	0.5350	1.8	0.0034	1.8	1.6410	2.4	0.0801	5.6849
Line In to HP bypass path	3.3	0.8920	1.8	0.5410	1.8	0.0087	1.8	6.1740	3.3	0.4310	16.4685
32ohm load, 2.0mW/channel	3.0	0.8200	1.8	0.5410	1.8	0.0070	1.8	6.2770	3.0	0.3890	15.9121
	2.4	0.6840	1.8	0.5410	1.8	0.0036	1.8	6.8540	2.4	0.3070	15.6958

Table 2 Power Consumption

Note: All parameters in this table were measured at default bias conditions, and at 48kHz sample rate unless otherwise stated.

DAC TO HEADPHONE POWER CONSUMPTION

The following tables detail the DAC to Headphone power consumption differences and SNR differences (where applicable) between 4 different playback conditions and 3 different biasing modes. The biasing modes are detailed in Table 45 on page 12.

SUPPLIES	AVDD		DCVDD		DBVDD		CPVDDLO		CPVDDHI		TOTAL
MODE	V	mA	V	mA	V	mA	V	mA	V	mA	mW
Default mode	3.30	4.11	1.80	2.27	1.80	0.01	1.80	0.00	3.30	1.70	23.26
	3.00	3.71	1.80	2.27	1.80	0.01	1.80	0.00	3.00	1.49	19.72
	2.40	2.93	1.80	2.27	1.80	0.00	1.80	0.00	2.40	1.12	13.82
Reduced power mode											
	3.30	2.57	1.80	2.27	1.80	0.01	1.80	0.00	3.30	1.70	18.20
	3.00	2.33	1.80	2.27	1.80	0.01	1.80	0.00	3.00	1.49	15.57
	2.40	1.85	1.80	2.27	1.80	0.01	1.80	0.00	2.40	1.12	11.22
Ultra Low power mode											
	3.30	2.09	1.80	2.27	1.80	0.01	1.80	0.00	3.30	1.58	16.20
	3.00	1.89	1.80	2.27	1.80	0.01	1.80	0.00	3.00	1.39	13.95
	2.40	1.51	1.80	2.27	1.80	0.00	1.80	0.00	2.40	1.05	10.24

Table 3 DAC to Headphone Power Consumption: Quiescent (DAC input all zeroes and OUT2VOL PGA set to 0dB)

SUPPLIES	AVDD		DCVDD		DBVDD		CPVDDLO		CPVDDHI		TOTAL	SNR (SEE NOTE 2)
MODE	V	mA	V	mA	V	mA	V	mA	V	mA	mW	(dB)
Default mode	3.30	4.18	1.80	2.56	1.80	0.01	1.80	0.40	3.30	0.06	15.54	-101
	3.00	3.78	1.80	2.56	1.80	0.01	1.80	0.67	3.00	0.13	14.51	-100
	2.40	2.99	1.80	2.56	1.80	0.01	1.80	0.31	2.40	0.04	12.46	-98
	2.40	2.99	1.80	2.57	1.80	0.01	1.60	0.29	2.40	0.04	12.42	-98
Reduced power mode												
	3.30	2.67	1.80	2.56	1.80	0.01	1.80	0.41	3.30	0.06	11.92	-102
	3.00	2.42	1.80	2.56	1.80	0.01	1.80	0.68	3.00	0.13	11.25	-101
	2.40	1.92	1.80	2.56	1.80	0.01	1.80	0.31	2.40	0.04	9.91	-98.
	2.40	1.92	1.80	2.57	1.80	0.01	1.60	0.29	2.40	0.04	9.87	-98
Ultra Low power mode												
	3.30	2.20	1.80	2.56	1.80	0.01	1.80	0.33	3.30	0.06	10.65	-101
	3.00	2.00	1.80	2.56	1.80	0.01	1.80	0.56	3.00	0.13	10.10	-100
	2.40	1.59	1.80	2.56	1.80	0.01	1.80	0.26	2.40	0.04	9.01	-98
	2.40	1.59	1.80	2.57	1.80	0.01	1.60	0.24	2.40	0.04	8.99	-98

Table 4 DAC to Headphone Power Consumption: -57dB Playback (DAC input 0dBFS 1kHz sine and OUT2VOL PGA set to -57dB)

SUPPLIES	AVDD		DCVDD		DBVDD		CPVDDLO		CPVDDHI		TOTAL	SNR (SEE NOTE 2)
MODE	V	mA	V	mA	V	mA	V	mA	V	mA	mW	(dB)
Default mode	3.30	4.77	1.80	2.57	1.80	0.01	1.80	18.07	3.30	0.44	49.66	-99
	3.00	4.08	1.80	2.57	1.80	0.01	1.80	16.90	3.00	0.40	45.81	-98
	2.40	3.03	1.80	2.57	1.80	0.01	1.80	13.90	2.40	0.31	37.68	-96
	2.40	3.11	1.80	2.57	1.80	0.01	1.60	13.76	2.40	0.31	37.59	-96
Reduced power mode												
	3.30	3.28	1.80	2.57	1.80	0.01	1.80	18.13	3.30	0.44	46.18	-99
	3.00	2.73	1.80	2.57	1.80	0.01	1.80	16.97	3.00	0.40	42.68	-98
	2.40	1.96	1.80	2.57	1.80	0.01	1.80	13.98	2.40	0.31	35.27	-96
	2.40	2.05	1.80	2.57	1.80	0.01	1.60	13.82	2.40	0.31	35.16	-96
Ultra Low power mode												
	3.30	2.82	1.80	2.57	1.80	0.01	1.80	18.13	3.30	0.44	45.08	-99
	3.00	2.31	1.80	2.57	1.80	0.01	1.80	16.98	3.00	0.40	41.70	-98
	2.40	1.63	1.80	2.57	1.80	0.01	1.80	13.99	2.40	0.31	34.48	-95
	2.40	1.72	1.80	2.57	1.80	0.01	1.60	13.83	2.40	0.31	34.38	-95

Table 5 DAC to Headphone Power Consumption: -9dB Playback (DAC input 0dBFS 1kHz sine and OUT2VOL PGA set to -9dB)

SUPPLIES	AVDD		DCVDD		DBVDD		CPVDDLO		CPVDDHI		TOTAL	SNR (SEE NOTE 2)
MODE	V	mA	V	mA	V	mA	V	mA	V	mA	mW	(dB)
Default mode	3.30	5.08	1.80	2.57	1.80	0.01	1.80	0.00	3.30	39.87	112.53	-95
	3.00	4.48	1.80	2.57	1.80	0.01	1.80	0.00	3.00	35.93	101.62	-94
	2.40	3.37	1.80	2.57	1.80	0.01	1.80	0.00	2.40	27.88	79.64	-92.
	2.40	3.37	1.80	2.57	1.80	0.01	1.60	0.00	2.40	27.86	79.57	-92
Reduced power mode												
	3.30	3.59	1.80	2.57	1.80	0.01	1.80	0.00	3.30	39.95	109.13	-94
	3.00	3.13	1.80	2.57	1.80	0.01	1.80	0.00	3.00	36.00	98.55	-93
	2.40	2.31	1.80	2.57	1.80	0.01	1.80	0.00	2.40	27.92	77.19	-91
	2.40	2.31	1.80	2.57	1.80	0.01	1.60	0.00	2.40	27.90	77.14	-91
Ultra Low power mode												
	3.30	3.13	1.80	2.57	1.80	0.01	1.80	0.00	3.30	39.95	108.03	-93
	3.00	2.72	1.80	2.57	1.80	0.01	1.80	0.00	3.00	36.00	97.56	-93
	2.40	1.98	1.80	2.57	1.80	0.01	1.80	0.00	2.40	27.91	76.39	-91
	2.40	1.98	1.80	2.57	1.80	0.01	1.60	0.00	2.40	27.90	76.35	-91

Table 6 DAC to Headphone Power Consumption: 0dB Playback (DAC input 0dBFS 1kHz sine and OUT2VOL PGA set to 0dB)

Notes:

1. Quiescent power consumption with OUT2VOL = 0dB is slightly higher than would be measured under typical listening levels. The headphone amplifier is being powered by CPVDDHI under quiescent test conditions. During typical playback listening levels (no more than 2mW into a 32Ohm headphone load), the headphone amplifier is powered by CPVDDLO, and a more realistic measure of power consumption can be estimated. A typical listening level would result in OUT2VOL being -9dB or lower, as shown in the above table.

2. SNR measured with a -60dBFS DAC input signal. The most accurate measure of SNR is when OUT2VOL = 0dB, as no noise is attenuated.

EXTERNAL COMPONENTS

Figure 1 illustrates the recommended external components for the WM8900. The configuration illustrated shows two pseudo-differential microphone inputs, two line inputs, two line outputs and the ground-referenced headphone output driver. Other configurations may require fewer external components. Table 7 describes the function of each component shown in Figure 1, showing which components are only required for specific input/output signal paths.

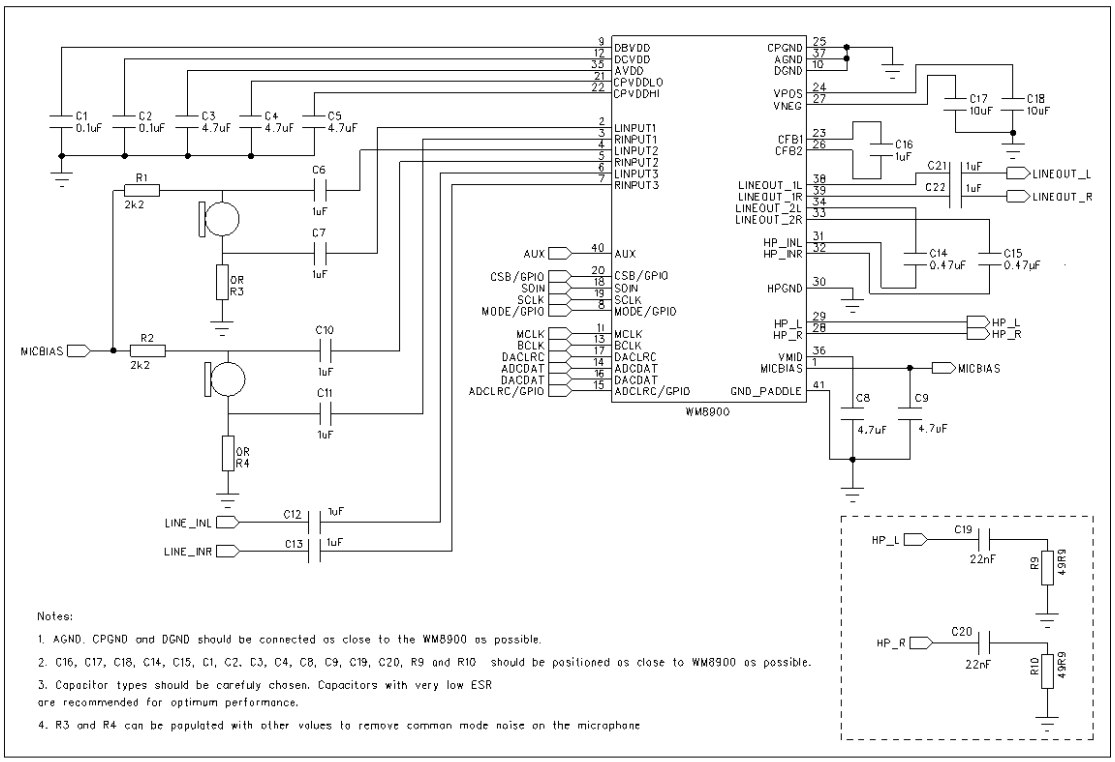


Figure 1 External Component Connectivity

Note: In order to achieve stability of the Headphone output, the Zobel network (C19, C20, R9, R10) must be fitted.

IDENTIFIER	VALUE	FUNCTION	REQUIRED FOR
C1	0.1 uF	DBVDD decoupling	All applications
C2	0.1 uF	DCVDD decoupling	
C3	4.7 uF	AVDD decoupling	
C4	4.7 uF	CPVDDLO decoupling	Ground Referenced Headphone Amplifier
C5	4.7 uF	CPVDDHI decoupling	
C6	1 uF	LINPUT2 DC blocking	Left Microphone Input
C7	1 uF	LINPUT1 DC blocking	
C8	4.7 uF	VMID decoupling	All applications
C9	4.7 uF	MICBIAS decoupling	
C10	1 uF	RINPUT2 DC blocking	Right Microphone Input
C11	1 uF	RINPUT1 DC blocking	
C12	1 uF	LINPUT3 DC blocking	Left Line Input
C13	1 uF	RINPUT3 DC blocking	Right Line Input
C14	0.47 uF	HP_INL DC blocking	Ground Referenced Headphone Amplifier
C15	0.47 uF	HP_INR DC blocking	
C16	1 uF	Charge Pump capacitor	
C17	10 uF	VNEG decoupling	
C18	10 uF	VPOS decoupling	
C19	22 nF	Headphone zobel network	Headphone Amp
C20	22 nF	Headphone zobel network	
C21	1 uF	LINEOUT_L DC blocking	Left Line Output
C22	1 uF	LINEOUT_R DC blocking	Right Line Output
R1	2.2 kΩ	LINPUT2 Bias Current limit	Left Microphone Input
R2	2.2 kΩ	RINPUT2 Bias Current limit	Right Microphone Input
R3	0 Ω	LINPUT1 Ground	Left Microphone Input
R4	0 Ω	RINPUT1 Ground	Right Microphone Input
R9	49.9 Ω	Headphone zobel network	Headphone Amp in Normal mode
R10	49.9 Ω	Headphone zobel network	

Table 7 External Components for WM8900

Please refer to WAN0188 for further details on the selection of external components for WM8900

RECOMMENDED TEST METHOD FOR TESTING AUDIO OUTPUTS

Most modern lab test equipment contains high speed A-D converter circuits hence can be sensitive to frequencies outside of the audio band which appear at their inputs. The software or hardware filters included in such test equipment may not be sufficient to attenuate out of band frequencies from the WM8900 charge pump. Although this does not affect performance within the audio band, false triggering of the test equipment outside the audio band can give inaccurate results. An external filter with a very steep attenuation curve above the audio band is recommended, such as the AUX0025 from Audio Precision (http://www.ap.com), or any filter which has a similar frequency response.

The connection method is shown in Figure 2. The 100k resistance at each channel of the Audio Analyzer Input represents the Analyser's input impedance. These resistors are not required as additional components during measurement.

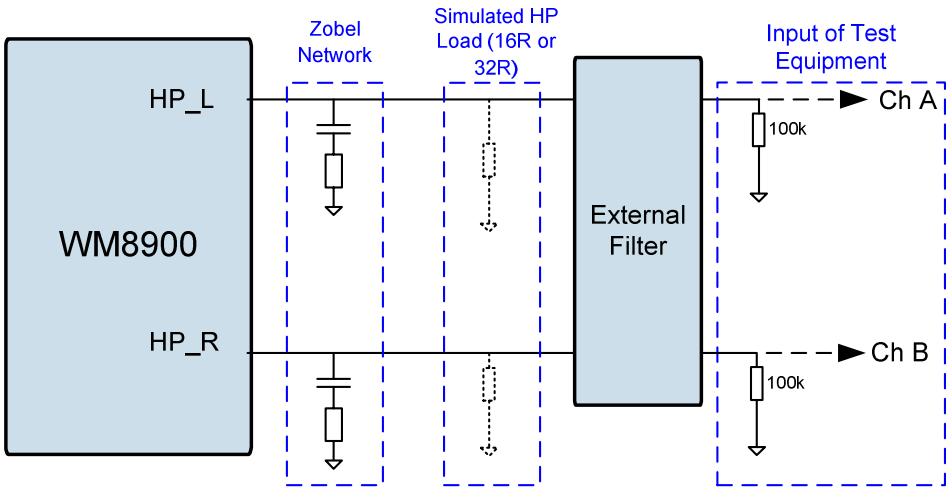


Figure 2 Recommended Filter Connections between WM8900 Audio Outputs and Audio Analyser for Measurement and Testing Only

AUDIO PATHS OVERVIEW

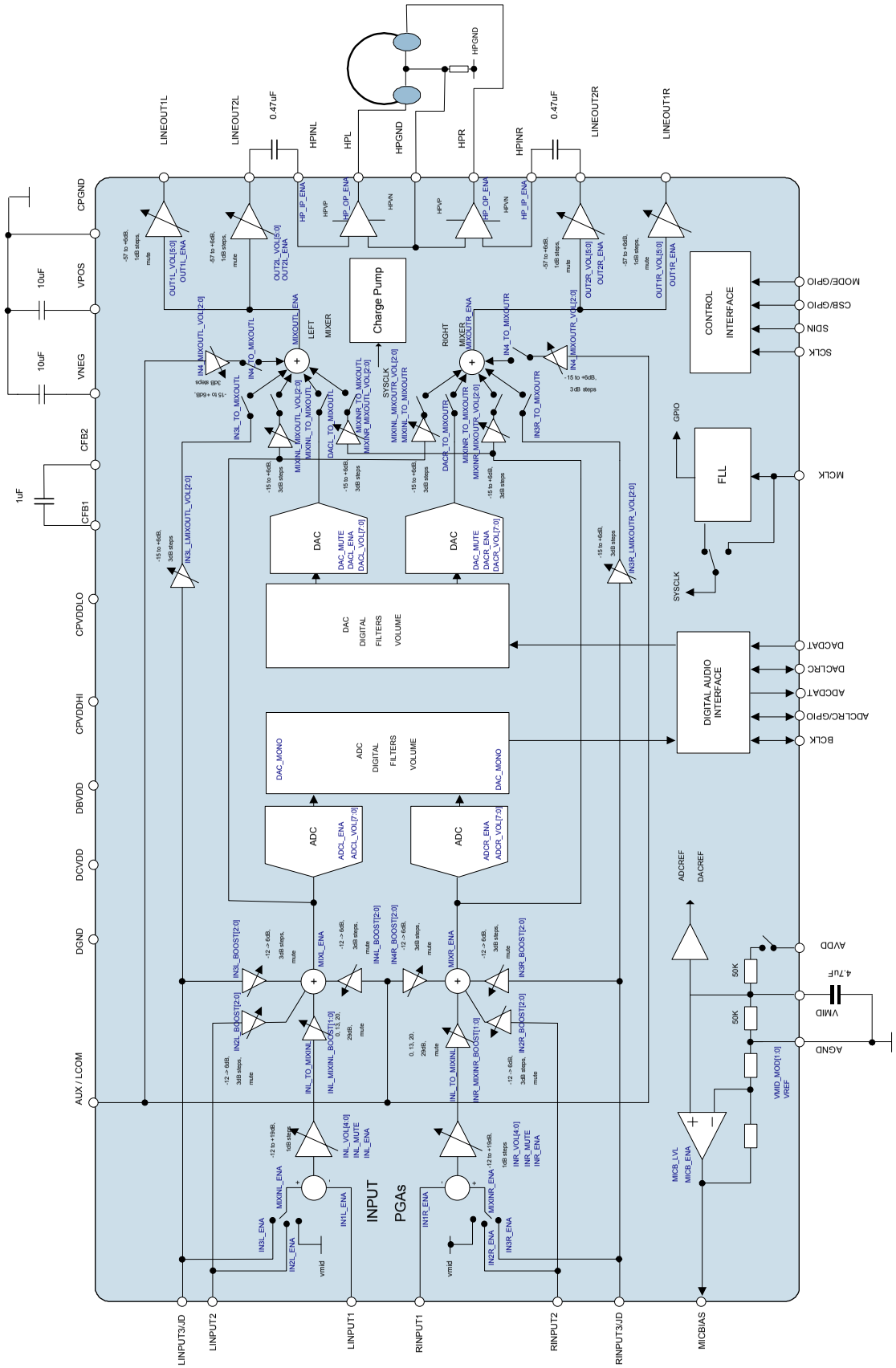


Figure 3 Signal Path Overview and Control Diagram

SYSTEM CLOCK TIMING

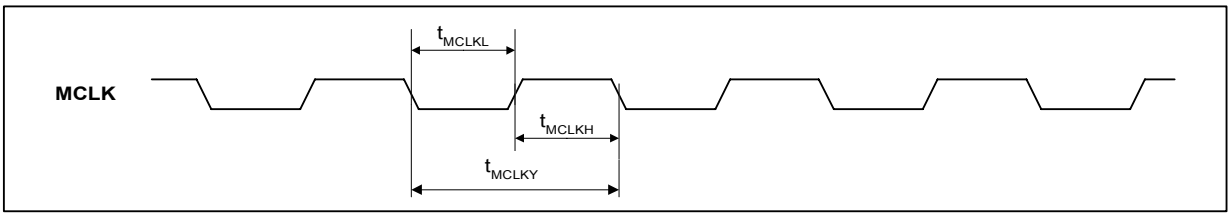


Figure 4 System Clock Timing Requirements

Test Conditions
DCVDD=1.8V, DBVDD=1.8V, DGND=AGND=CPGND=HPGND=0V, AVDD=CPVDDHI=2.4V, CPVDDLO=1.6V; T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time (Codec clocked directly)	T_{MCLKY}		80			ns
MCLK cycle time (Codec clocked via FLL)	T_{MCLKY}		50			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

AUDIO INTERFACE TIMING

MASTER MODE

The Digital Audio Data timing in Master Mode is illustrated in Figure 5. See "Digital Audio Interface" for further details.

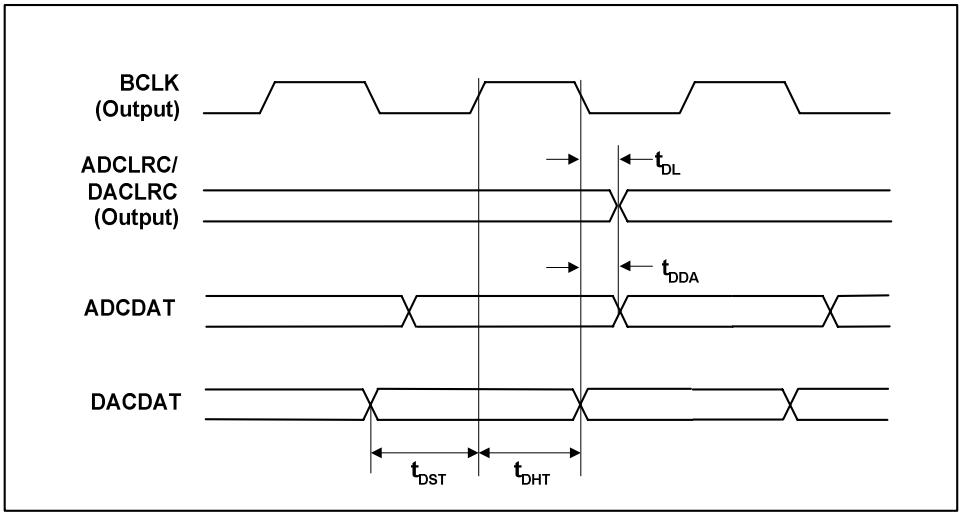


Figure 5 Digital Audio Data Timing - Master Mode

Test Conditions

DCVDD=1.8V, DBVDD=1.8V, DGND=AGND=0V, AVDD=2.4V; T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
ADCLRC/DACLRC propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			10	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

SLAVE MODE

The Digital Audio Data timing in Slave Mode is illustrated in Figure 6. See "Digital Audio Interface" for further details.

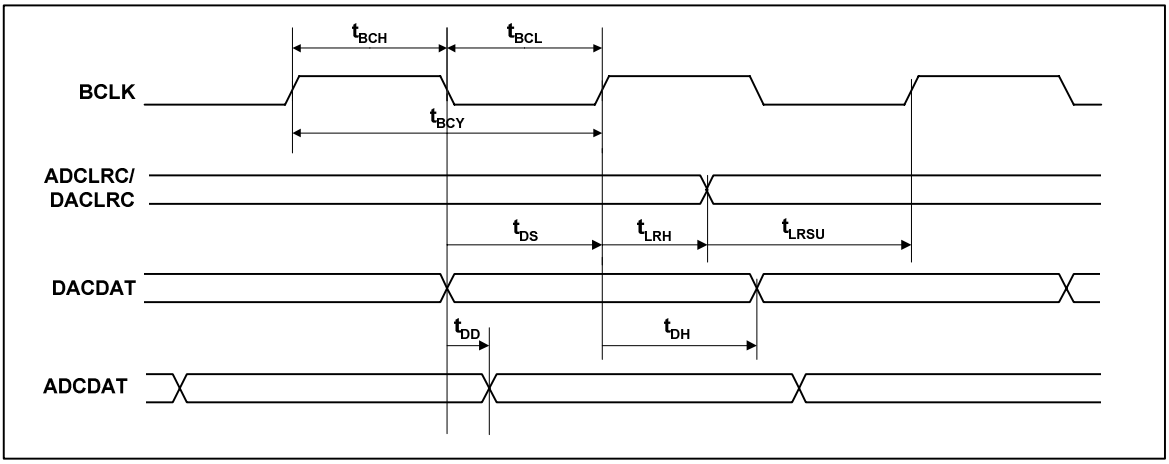


Figure 6 Digital Audio Data Timing – Slave Mode

Test Conditions DCVDD=1.8V, DBVDD=1.8V, DGND=AGND=0V, AVDD=2.4V; T_A=+25°C, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	80			ns
BCLK pulse width high	t_{BCH}	35			ns
BCLK pulse width low	t_{BCL}	35			ns
ADCLRC/DACLRC set-up time to BCLK rising edge	t_{LRSU}	10			ns
ADCLRC/DACLRC hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			15	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING

2-WIRE MODE

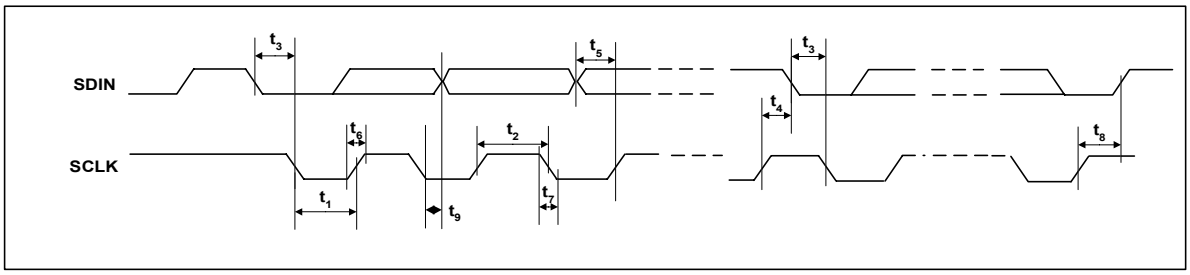


Figure 7 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=1.8V, DGND=AGND=0V, AVDD=2.4V; T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

3-WIRE MODE

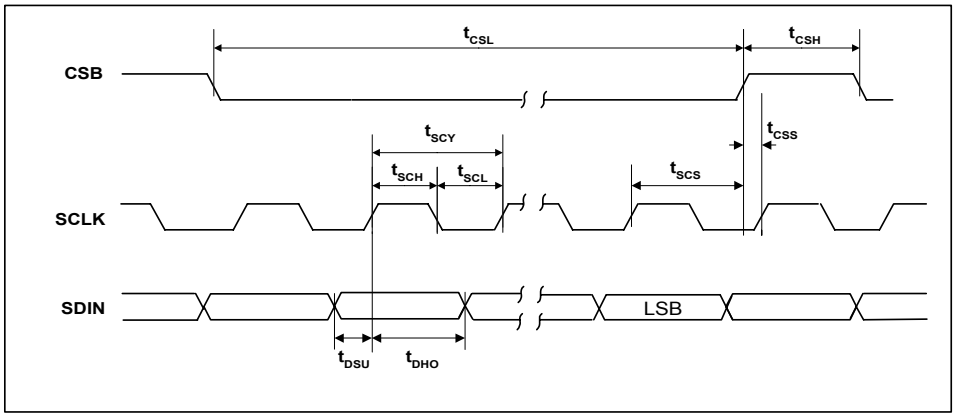


Figure 8 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=1.8V, DGND=AGND=0V, AVDD=2.4V; T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

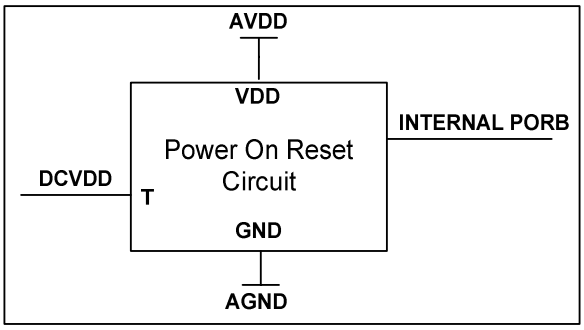


Figure 9 Internal Power on Reset Circuit Schematic

The WM8900 includes an internal Power-On-Reset Circuit, as shown in Figure 9, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DCVDD. It asserts PORB low if AVDD or DCVDD is below a minimum threshold.

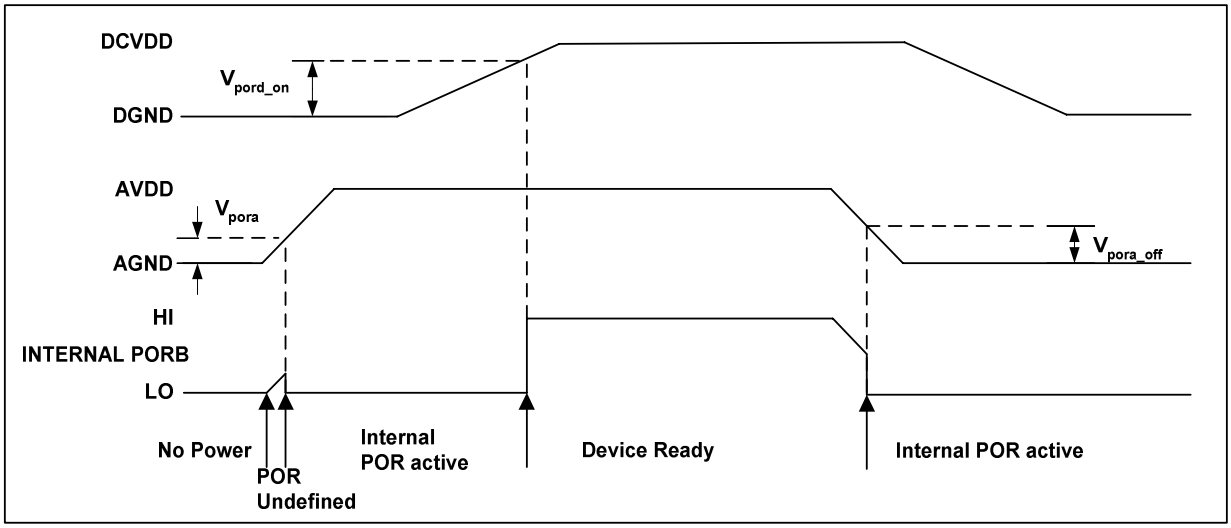


Figure 10 Typical Power up Sequence where AVDD is Powered before DCVDD

Figure 10 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DCVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold V_{pora_off}.

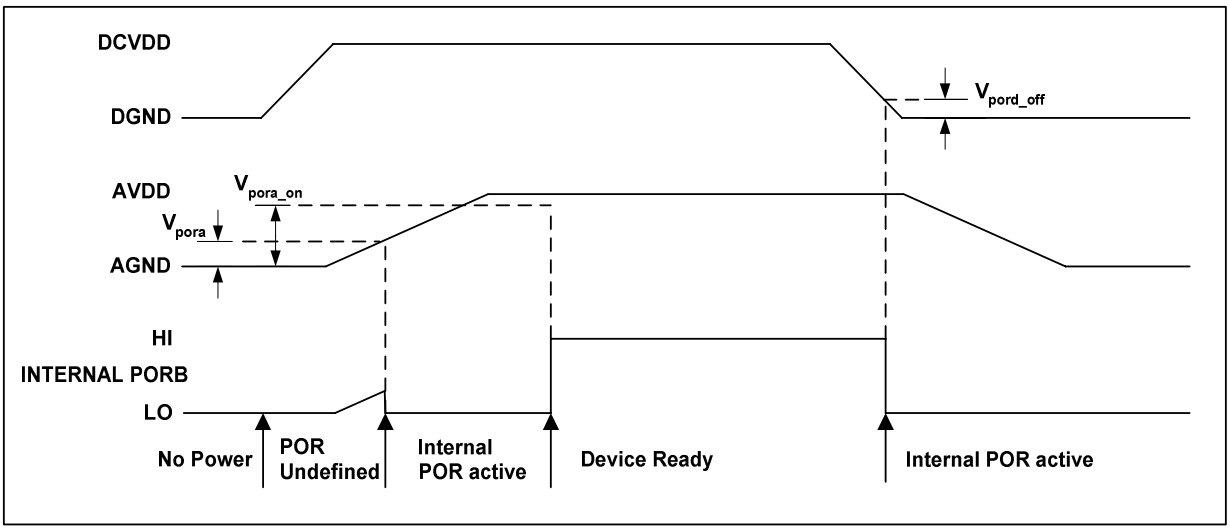


Figure 11 Typical Power up Sequence where DCVDD is Powered before AVDD

Figure 11 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.4	0.6	0.8	V
V_{pora_on}	0.9	1.2	1.6	V
V_{pora_off}	0.4	0.6	0.8	V
V_{pord_on}	0.5	0.7	0.9	V
V_{pord_off}	0.4	0.6	0.8	V

Table 8 Typical POR Operation (typical values, not tested)

Notes:

1. If AVDD and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.

2. The chip will enter reset at power down when AVDD or DCVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.

3. The minimum t_{por} period is maintained even if DCVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

POP-CLICK MINIMISATION CONTROL REGISTERS

It is recommended that the power management control bits are used to enable/disable the required blocks within the WM8900 according to the desired application or mode. The sequencing of these controls may be important in the reduction of audible pops and clicks. Detailed information is available for specific requirements - see “Applications Information”.

The additional control bits described in Table 9 are normally set to default only but may be used to control pops and clicks under certain conditions.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Power Management 1	8	STARTUP_BIAS_ENA	0	Bias Startup control. Normally 0 but can be temporarily set to 1 during startup to minimise pops and clicks.
	2	VMID_BUF_ENA	0	Provides VMID to input and output analogue pins when not enabled. Normally 0 but can be temporarily set to 1 during startup to minimise pops and clicks.
R30 (1Eh) Additional Control	8	OUT1_DIS	0	1 = Clamps LINEOUT_1L and LINEOUT_1R to GND via 8K resistance 0 = 8k resistance not connected to GND
	7	OUT2_DIS	0	1 = Clamps LINEOUT_2L and LINEOUT_2R to GND via 8K resistance 0 = 8k resistance not connected to GND
	5	VMID_DISCH	0	Enables fast discharge of Vmid to GND
	4	BIAS_SRC	0	Vmid bias select. Normally 0 but can be temporarily set to 1 during startup to select the soft-start Vmid source.
	3	VMID_SOFTST	0	Vmid soft-start control. Normally 0 but can be temporarily set to 1 during startup to ramp Vmid in a controlled manner.
R58 (3Ah) Headphone Control 1	5	HP_CLAMP_IP	0	Clamps HP_INL and HP_INR to GND
	4	HP_CLAMP_OP	0	Clamps HP_L and HP_R outputs to GND
	3	HP_SHORT	0	Shorts the inputs to the outputs
	2	HP_SHORT2	0	Shorts the feedback resistor. 0 = Normal operation 1 = Shorts feedback resistor. About 20dB ‘mute’ attenuation

Table 9 Pop and Click Minimisation Register Settings

DEVICE DESCRIPTION

INTRODUCTION

The WM8900 is an ultra low power audio codec offering a combination of high quality audio, advanced features, low power consumption and small package size. These characteristics make it ideal for portable multimedia applications with stereo headphone outputs such as games consoles, portable media players and multimedia phones.

Class G, Stereo ultra low power ground-referenced headphone drivers provide reduced power consumption during DAC playback at typical listening levels, with user selectable low power modes allowing a trade off between optimal audio performance and lowest power consumption .

A flexible input configuration includes support for two stereo microphone interfaces (single-ended or pseudo-differential), additional stereo line inputs and auxiliary line input which can also be used a common input ground connection. Up to three stereo analogue input sources are available, removing the need for external analogue switches in many applications. Boost amplifiers are available for additional gain on the microphone inputs and a programmable gain amplifier.

The stereo ADC and DAC are of hi-fi quality using a 24-bit, low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports mixed ADC and DAC sample rates.

The DAC output signal can be mixed with analogue input signals from the line inputs, auxiliary input, mic boost stage or bypass paths. This mix is available on both headphone and line outputs.

The WM8900 has a configurable digital audio interface where ADC data can be read and digital audio playback data fed to the DAC. It supports a number of audio data formats including I^2S, DSP Mode (a burst mode in which frame sync plus two data packed words are transmitted), MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes. In PCM mode A-law and μ-law companding is supported.

The SYSCLK (system clock) provides clocking for the ADCs, DACs, DSP core, integrated charge pump and the digital audio interface. SYSCLK can be derived directly from the MCLK pin or via an integrated FLL, providing flexibility to support a wide range of clocking schemes. All MCLK frequencies typically used in portable systems are supported for sample rates between 8kHz and 48kHz. A flexible switching clock for the ultra low power ground-referenced headphone drivers (synchronous with the audio DSP clocks for best performance) is also derived from SYSCLK.

To allow full software control over all its features, the WM8900 uses a 2 or 3 wire control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled via software to save power, while low leakage currents extend standby and off time in portable battery-powered applications.

INPUT SIGNAL PATH

The WM8900 has three stereo analogue input channels which can be configured in many combinations as line inputs, single-ended microphone or differential microphone connections. Line inputs and microphone PGA outputs can be routed to the hi-fi ADCs or directly to the output mixers via a bypass path. Multiple inputs can be connected simultaneously and mixed together or each can be individually enabled or muted as required.

SINGLE-ENDED MICROPHONE INPUTS

- LINPUT1 (RINPUT1) only

In this configuration, the microphone signal is connected to LINPUT1 (RINPUT1), and the non-inverting input of the input PGA is connected to Vmid. The Left (Right) channel input PGA and boost PGA must both be enabled in this configuration. The gain of the input PGA and boost PGA can be controlled via register settings, as described in Table 14 and Table 15.

In this configuration, LINPUT2 (RINPUT2) and LINPUT3 (RINPUT3) must not be connected to the input PGA, but these connections are available for use as Line inputs directly to the input mixers.

Note that the input impedance at LINPUT1 (RINPUT1) changes with the input PGA gain setting, as described under “Electrical Characteristics”. The input impedance can be determined for any gain setting according to the following formula:

Rin = 20k / [1/GAIN)+1], where GAIN is voltage gain of the input PGA stage.

For example, if the input PGA gain is +13dB, then GAIN = 4.47 and Rin = 16.3k.

The external connections for this configuration and the required register settings are detailed below:

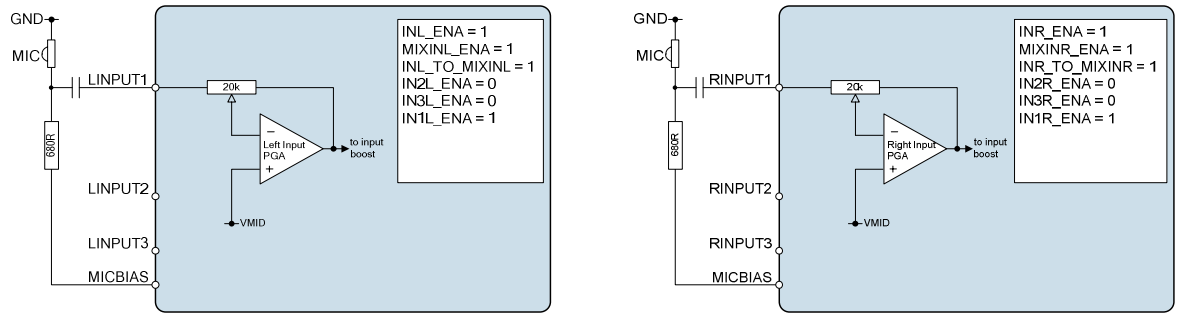


Figure 12 Single-ended Microphone Configurations

Note that setting IN2L_ENA and IN3L_ENA to 0 automatically causes Vmid to be connected to the non-inverting Left PGA input. Similarly setting IN2R_ENA and IN3R_ENA to 0 automatically causes Vmid to be connected to the non-inverting Right PGA input.

DIFFERENTIAL MICROPHONE INPUTS

- LINPUT1 (RINPUT1) and LINPUT2 (RINPUT2) or
- LINPUT1 (RINPUT1) and LINPUT3 (RINPUT3)

In this configuration, the non-inverted microphone signal is connected to LINPUT2 (RINPUT2) or LINPUT3 (RINPUT3) and the inverted (or noisy ground) signal is connected to LINPUT1 (RINPUT1). The remaining input must not be connected to the input PGA, and is available for use as an additional Line input. The Left (Right) channel input PGA and boost PGA must both be enabled in this configuration. The gain of the input PGA and Boost PGA can be controlled via register settings, as described in Table 14 and Table 15.

Note that the input impedance LINPUT1 (RINPUT1) changes with the input PGA gain setting, as described under “Electrical Characteristics”. In this configuration, the input impedance LINPUT2 (RINPUT2) or LINPUT3 (RINPUT3) does not change with the gain setting. The inverting and non-inverting inputs are therefore not matched and this configuration is not fully differential. The LINPUT1 (RINPUT1) input impedance can be determined for any gain setting as described above for the Single-Ended configuration.

The external connections for this configuration and the required register settings are detailed below:

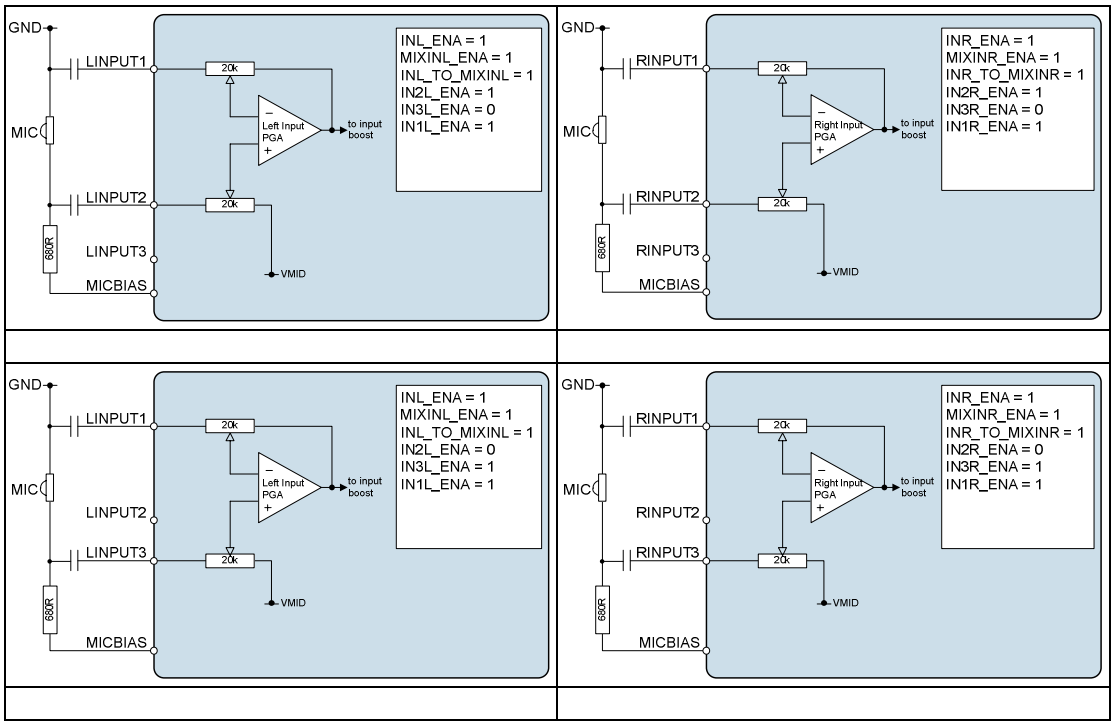


Figure 13 Differential Microphone Input Configurations

LINE INPUTS

- LINPUT2 (RINPUT2)
- LINPUT3 (RINPUT3)
- AUX

Two pairs of stereo line inputs are available as analogue inputs. Each of these may be an internal source (e.g. FM radio IC) or an external signal source. These can be mixed with the microphone input or can be enabled individually in the ADC input path. The Left (Right) channel boost PGA must be enabled in this configuration. The gain of the boost PGA can be controlled via register settings, as described in Table 16.

LINPUT3 (RINPUT3) may also be routed directly to the output mixer, including when the boost PGA is powered down. If a differential microphone connection is used, then only one of the line inputs is available. For example, if LINPUT1 and LINPUT2 are used as a differential microphone, then LINPUT3 can be used as a line input

Note that, in this configuration, the input impedance LINPUT2 (RINPUT2) or LINPUT3 (RINPUT3) changes with the boost gain setting, as described under “Electrical Characteristics”. The input impedance can be determined for any gain setting as described above for the Single-Ended microphone configuration, but based upon the boost gain amplification instead of the microphone input PGA.

A mono input, AUX, is also provided. This input may be mixed with the Left and Right channel ADC inputs and may also be routed directly to the output mixers. The gain of this input on the ADC input path is described in Table 16.

The external connections for this configuration and the required register settings are detailed below:

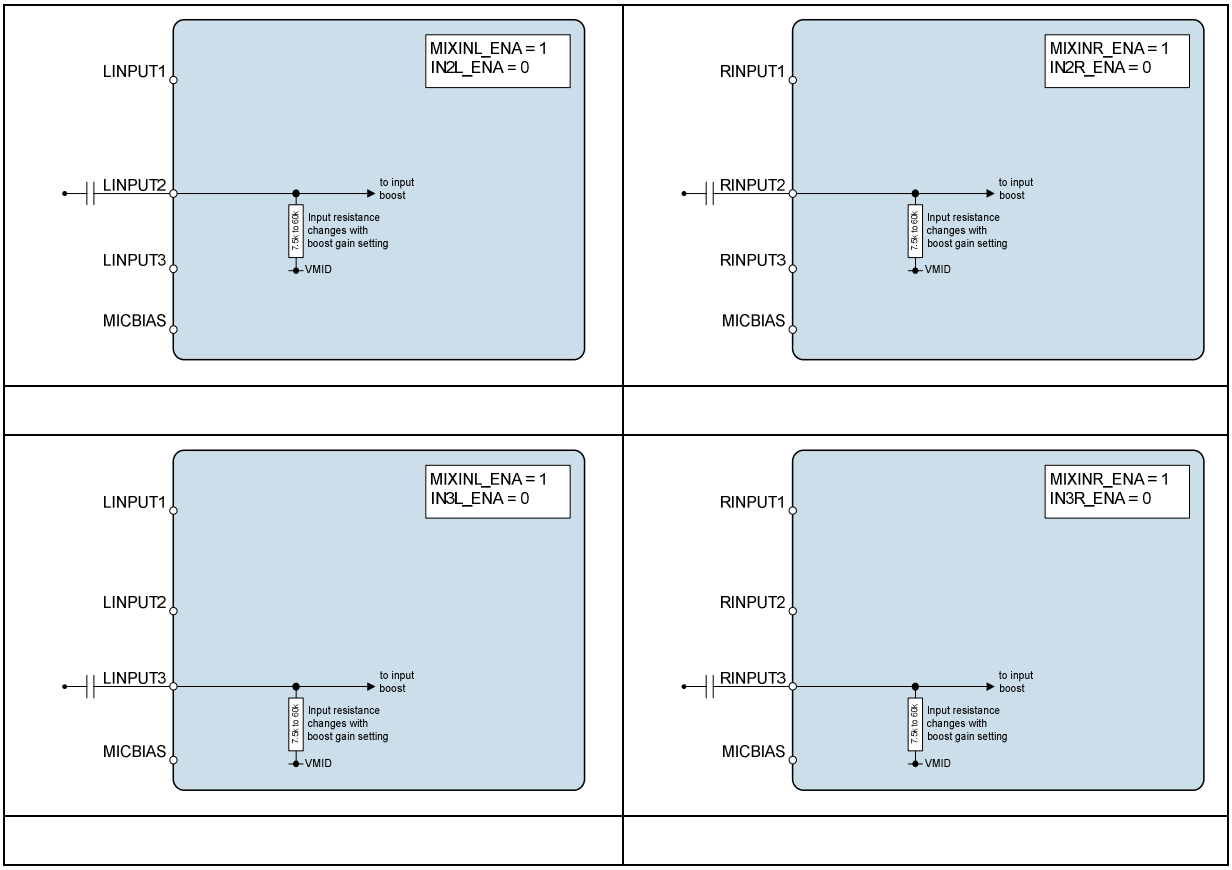


Figure 14 Line Input Configurations

Note that when using LRINPUT2 or LRINPUT3, there is inherent feedback signal to LRINPUT1 as shown in Figure 15.

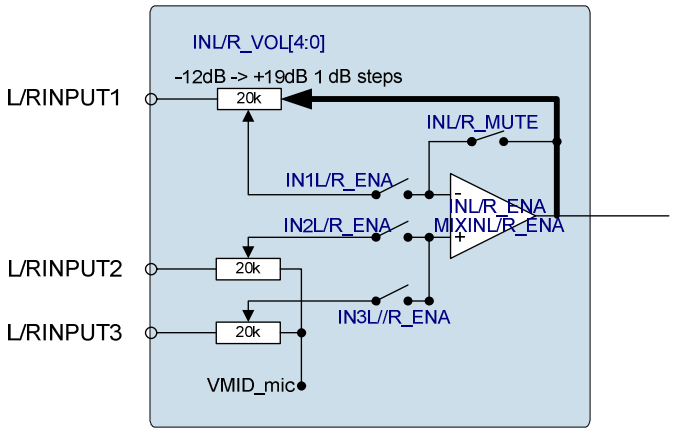


Figure 15 Input Feedback

INPUT PGA / BOOST MIXER ENABLE

The input boost mixers are enabled by the MIXINL_ENA and MIXINR_ENA register bits, as described in Table 10. The microphone input PGAs are enabled by the INL_ENA and INR_ENA register bits and can be disabled independently of the boost mixer to save power. The microphone input PGAs cannot be enabled if the associated boost mixer is not enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 2	5	MIXINL_ENA	0	Left channel input boost enable 0 = Boost disabled 1 = Boost enabled
	4	MIXINR_ENA	0	Right channel input boost enable 0 = Boost disabled 1 = Boost enabled
	3	INL_ENA	0	Left channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if MIXINL_ENA = 1)
	2	INR_ENA	0	Right channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if MIXINR_ENA = 1)

Table 10 Input PGA and Boost Mixer Enable Register Settings

INPUT PGA CONFIGURATION

The input PGAs are configured by the input signal path control registers, as described in Table 11. The input PGA is connected to the ADC signal path under the control of the ADC signal path input register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) ADC Signal Path	6	INL_TO_MIXINL	0	Connect Left Input PGA to Left Input Boost mixer 0 = Not connected 1 = Connected
R21 (15h) Input Control	6	IN1L_ENA	1	Connect LINPUT1 to inverting input of Left Input PGA 0 = LINPUT1 not connected to PGA 1 = LINPUT1 connected to PGA
	5	IN2L_ENA	0	Connect LINPUT2 to non-inverting input of Left Input PGA 0 = LINPUT2 not connected to PGA 1 = LINPUT2 connected to PGA
	4	IN3L_ENA	0	Connect LINPUT3 to non-inverting input of Left Input PGA 0 = LINPUT3 not connected to PGA 1 = LINPUT3 connected to PGA
R26 (1Ah) ADC Signal Path	2	INR_TO_MIXINR	0	Connect Right Input PGA to Right Input Boost mixer 0 = Not connected 1 = Connected
R21 (15h) Input Control	2	IN1R_ENA	1	Connect RINPUT1 to inverting input of Right Input PGA 0 = RINPUT1 not connected to PGA 1 = RINPUT1 connected to PGA
	1	IN2R_ENA	0	Connect RINPUT2 to non-inverting input of Right Input PGA 0 = RINPUT2 not connected to PGA 1 = RINPUT2 connected to PGA
	0	IN3R_ENA	0	Connect RINPUT3 to non-inverting input of Right Input PGA 0 = RINPUT3 not connected to PGA 1 = RINPUT3 connected to PGA

Table 11 Input PGA Control

MICROPHONE BIAS

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones via an external resistor. Refer to the Applications Information section for recommended external components. The MICBIAS can be enabled or disabled using the MICB_ENA control bit and the voltage can be selected using the MICB_LVL register bit as detailed in Table 12.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Power Management 1	4	MICB_ENA	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON
R21 (15h) Input Control	8	MICB_LVL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD

Table 12 Microphone Bias Control

Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistance must be large enough to limit the MICBIAS current to 3mA.

REFERENCE VOLTAGES

All internal analogue input and output circuitry requires a reference voltage AVDD/2 (VMID). This voltage is generated internally using 5kΩ, 50kΩ or 250kΩ resistors and is buffered as required. These functions are controlled using register bits VMID_MODE and BIAS_ENA.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Power Management 1	3	BIAS_ENA	0	VREF (necessary for all analogue functions) 0 = V_{REF} buffer disabled 1 = V_{REF} buffer enabled
	1:0	VMID_MODE [1:0]	00	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50kΩ divider (Normal mode) 10 = 2 x 250kΩ divider (Standby mode) 11 = 2 x 5kΩ divider (for fast start-up)

Table 13 Reference Voltages

INPUT PGA VOLUME CONTROL

The input PGAs have a gain range from -12dB to +19dB in 1dB steps. The gain on the inverting and non-inverting inputs to the PGA are always equal and are controlled by the register bits INL_VOL[4:0] and INR_VOL[4:0]. The left and right input PGAs can be independently muted using the INL_MUTE and INR_MUTE register bits.

To allow simultaneous volume updates of left and right channels, PGA gains are not altered until a 1 is written to either of the IN_VU bits.

To prevent "zipper noise", a zero-cross function is provided, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOCLK_ENA register bit), the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout period is set by TOCLK_RATE. See Table 46 in the “Headphone Jack Detect” section for the definition of these register bits,

The Input PGA Volume Control register fields are described in Table 14. Note that these volume/mute settings have no effect on Line inputs routed directly to the boost mixer.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h) Left Input Volume	8	IN_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause left and right Input PGA volume to be updated simultaneously
	7	INL_ZC	0	Left Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	6	INL_MUTE	1	Left Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IN_VU must be set to un-mute.
	4:0	INL_VOL [4:0]	01100 (0dB)	Left Input PGA Volume Control 11111 = +19dB 11110 = +18dB . . 1dB steps down to 00000 = -12dB
R23 (17h) Right Input Volume	8	IN_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause left and right Input PGA volume to be updated simultaneously
	7	INR_ZC	0	Right Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	6	INR_MUTE	1	Right Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IN_VU must be set to un-mute.
	4:0	INR_VOL [4:0]	01100 (0dB)	Right Input PGA Volume Control 11111 = +19dB 11110 = +18dB . . 1dB steps down to 00000 = -12dB

Table 14 Input PGA Volume Control

See "Volume Updates" for more information on volume update bits, zero cross and timeout operation.

See “Headphone Jack Detect” for more information on jack detect / debounce.

INPUT BOOST VOLUME CONTROL

The input path to the ADCs is via a boost stage, which mixes the signals from the microphone input PGAs and from the line inputs.

The boost stage can apply up to +29dB gain to the microphone input PGA path, providing a total maximum available analogue gain of +48dB from microphone to ADC input. The microphone PGA path to the boost mixer may be muted using INL_MUTE and INR_MUTE as described in Table 14. The Microphone PGA to boost gain settings are shown in Table 15. It is recommended that maximum gain is applied to the input signals at the input PGA stage, with minimal boost gain being applied where necessary. This prevents unnecessary amplification of small DC offsets from the input PGA output.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) ADC Signal Path	5:4	INL_MIXINL_BOOST [1:0]	00	Left Channel PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB
	1:0	INR_MIXINR_BOOST [1:0]	00	Right Channel PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB

Table 15 Microphone Input PGA Boost Control

The boost stage can apply -12dB to +6dB gain to the line inputs. The line inputs may also be muted via the boost gain settings, as shown in Table 16.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Input Boost Mixer 1	6:4	IN3L_BOOST [2:0]	100	LINPUT3 to Boost Gain 000 = -12dB ...6dB steps up to 011 = +6dB 1XX = Mute
	2:0	IN2L_BOOST [2:0]	100	LINPUT2 to Boost Gain 000 = -12dB ...6dB steps up to 011 = +6dB 1XX = Mute
R25 (19h) Input Boost Mixer 2	6:4	IN3R_BOOST [2:0]	100	RINPUT3 to Boost Gain 000 = -12dB ...6dB steps up to 011 = +6dB 1XX = Mute
	2:0	IN2R_BOOST [2:0]	100	RINPUT2 to Boost Gain 000 = -12dB ...6dB steps up to 011 = +6dB 1XX = Mute
R27 (1Bh) Aux Boost	6:4	IN4L_BOOST [2:0]	100	AUX input to Boost Gain 000 = -12dB ...6dB steps up to 011 = +6dB 1XX = Mute
	2:0	IN4R_BOOST [2:0]	100	AUX input to Boost Gain 000 = -12dB ...6dB steps up to 011 = +6dB 1XX = Mute

Table 16 Line Input Boost Control

Note that, when all input paths to the boost mixer are disabled, the boost mixer will automatically be muted.

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8900 uses stereo 24-bit, 64x oversampled sigma-delta ADCs. The use of multi-bit feedback and high oversampling rates reduce the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is $1.0V_{rms}$. Any voltage greater than full scale may overload the ADC and cause distortion.

The ADCs are enabled by the ADCL_ENA/ADCR_ENA register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 2	1	ADCL_ENA	0	Enable ADC left channel: 0 = ADC disabled 1 = ADC enabled
	0	ADCR_ENA	0	Enable ADC right channel: 0 = ADC disabled 1 = ADC enabled

Table 17 ADC Enable Control

ADC DIGITAL VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from –71.625dB to +17.625dB in 0.375dB steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 239$; MUTE for $X = 0$ +17.625dB for $239 \leq X \leq 255$

The ADC_VU bit controls the loading of digital volume control data. When ADC_VU is set to 0, the ADCL_VOL or ADCR_VOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to ADC_VU. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 (0Fh) Left ADC Digital Volume	8	ADC_VU	0	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCL_VOL [7:0]	1100 0000 (0dB)	Left ADC Digital Volume (See Table 19 for volume range)
R16 (10h) Right ADC Digital Volume	8	ADC_VU	0	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCR_VOL [7:0]	1100 0000 (0dB)	Right ADC Digital Volume (See Table 19 for volume range)

Table 18 ADC Digital Volume Control

ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.375
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.750
3h	-70.875	43h	-46.875	83h	-22.875	C3h	1.125
4h	-70.500	44h	-46.500	84h	-22.500	C4h	1.500
5h	-70.125	45h	-46.125	85h	-22.125	C5h	1.875
6h	-69.750	46h	-45.750	86h	-21.750	C6h	2.250
7h	-69.375	47h	-45.375	87h	-21.375	C7h	2.625
8h	-69.000	48h	-45.000	88h	-21.000	C8h	3.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	3.375
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	3.750
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	4.125
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	4.500
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	4.875
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	5.250
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	5.625
10h	-66.000	50h	-42.000	90h	-18.000	D0h	6.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	6.375
12h	-65.250	52h	-41.250	92h	-17.250	D2h	6.750
13h	-64.875	53h	-40.875	93h	-16.875	D3h	7.125
14h	-64.500	54h	-40.500	94h	-16.500	D4h	7.500
15h	-64.125	55h	-40.125	95h	-16.125	D5h	7.875
16h	-63.750	56h	-39.750	96h	-15.750	D6h	8.250
17h	-63.375	57h	-39.375	97h	-15.375	D7h	8.625
18h	-63.000	58h	-39.000	98h	-15.000	D8h	9.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	9.375
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	9.750
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	10.125
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	10.500
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	10.875
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	11.250
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	11.625
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	12.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	12.375
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	12.750
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	13.125
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	13.500
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	13.875
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	14.250
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	14.625
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	15.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	15.375
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	15.750
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	16.125
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	16.500
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	16.875
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	17.250
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	17.625
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	17.625
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	17.625
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	17.625
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	17.625
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	17.625
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	17.625
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	17.625
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	17.625
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	17.625
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	17.625
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	17.625
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	17.625
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	17.625
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	17.625
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	17.625
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	17.625

Table 19 ADC Digital Volume Range

ADC DIGITAL FILTERS

The ADC filters perform true 24-bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface.

HIGH PASS FILTER

A digital high pass filter is applied by default to the ADC path to remove DC offsets. This filter can also be programmed to remove low frequency noise in voice applications (e.g. wind noise or mechanical vibration). This filter is controlled using the ADC_HPF_ENA and ADC_HPF_CUT register bits.

In hi-fi mode the high pass filter is optimised for removing DC offsets without degrading the bass response and has a cut-off frequency of 3.7Hz at fs=44.1kHz.

In voice mode the high pass filter is optimised for voice communication and it is recommended to program the cut-off frequency below 300Hz (e.g. ADC_HPF_CUT=11 at fs=8kHz or ADC_HPF_CUT=10 at fs=16kHz).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 (0Eh) ADC Control	8	ADC_HPF_ENA	1	ADC Digital High Pass Filter Enable 0 = disabled 1 = enabled
	6:5	ADC_HPF_CUT [1:0]	00	ADC Digital High Pass Filter Cut-Off Frequency (fc) 00 = Hi-fi mode (fc=4Hz at fs=48kHz) 01 = Voice mode 1 (fc=127Hz at fs=16kHz) 10 = Voice mode 2 (fc=130Hz at fs=8kHz) 11 = Voice mode 3 (fc=267Hz at fs=8kHz) (Note: fc scales with sample rate. See Table 21 for cut-off frequencies at all supported sample rates.)

Table 20 ADC High Pass Filter Control Registers

Sample Frequency (kHz)	CUT-OFF FREQUENCY (HZ)			
	ADC_HPF_CUT = 00	ADC_HPF_CUT = 01	ADC_HPF_CUT = 10	ADC_HPF_CUT = 11
8.000	0.7	64	130	267
11.025	0.9	88	178	367
16.000	1.3	127	258	532
22.050	1.9	175	354	733
24.000	2.0	190	386	798
32.000	2.7	253	514	1063
44.100	3.7	348	707	1464
48.000	4.0	379	770	1594

Table 21 ADC High Pass Filter Cut-Off Frequencies

The high pass filter characteristics are shown in the "Digital Filter Characteristics" section.

DIGITAL MIXING

The ADC and DAC data can be combined in various ways to support a range of different usage modes.

Data from either of the two ADCs can be routed to either the left or the right channel of the digital audio interface. In addition, data from either of the digital audio interface channels can be routed to either the left or right DAC. See "Digital Audio Interface" section for more information on the audio interface.

DIGITAL MIXING PATHS

Figure 16 shows the digital mixing paths available in the WM8900 digital core.

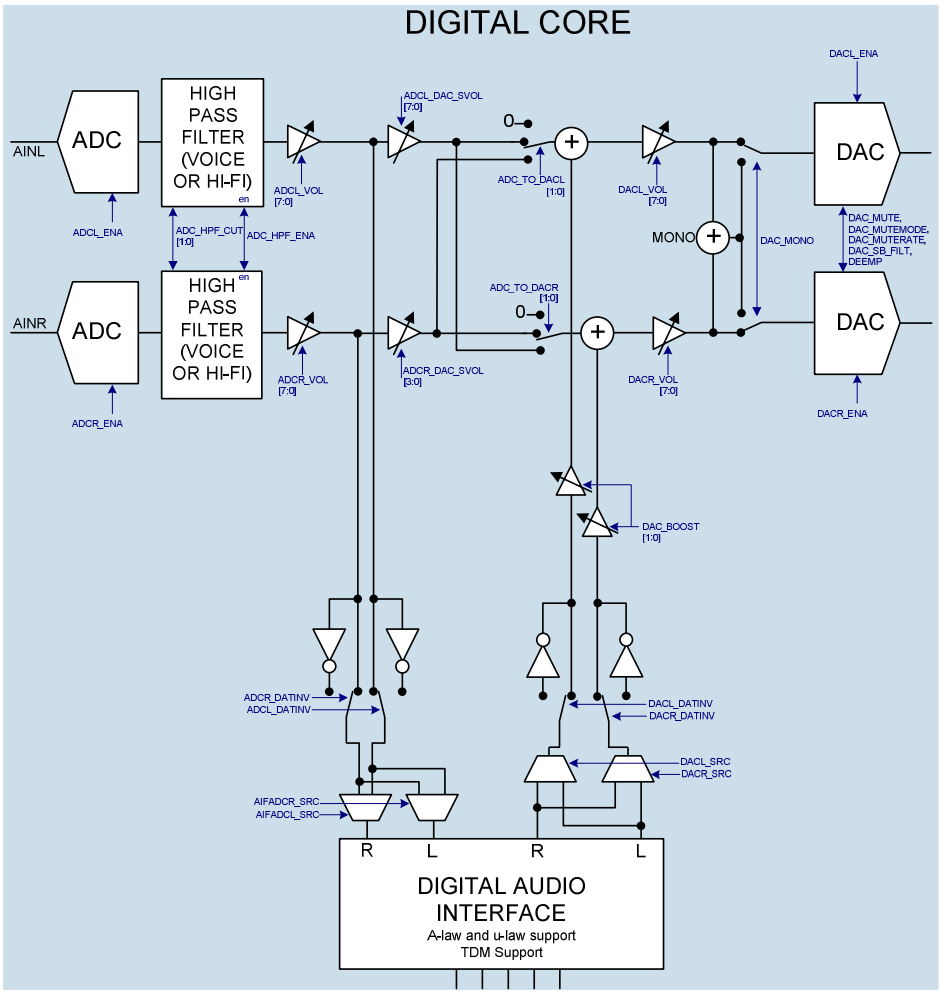


Figure 16 Digital Mixing Paths

The polarity of each ADC output signal can be changed under software control using the ADCL_DATINV and ADCR_DATINV register bits. The AIFADCL_SRC and AIFADCR_SRC register bits may be used to select which ADC is used for the left and right digital audio interface data. These register bits are described in Table 22.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Audio Interface 1	15	AIFADCL_SRC	0	Left Digital Audio channel source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel
	14	AIFADCR_SRC	1	Right Digital Audio channel source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
R14 (0Eh) ADC Control	1	ADCL_DATINV	0	Left ADC Invert 0 = Left ADC output not inverted 1 = Left ADC output inverted
	0	ADCR_DATINV	0	Right ADC Invert 0 = Right ADC output not inverted 1 = Right ADC output inverted

Table 22 ADC Routing and Control

The input data source for each DAC can be changed under software control using register bits DACL_SRC and DACR_SRC. The polarity of each DAC input may also be modified using register bits DACL_DATINV and DAVR_DATINV. These register bits are described in Table 23.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) Audio Interface 2	15	DACL_SRC	0	Left DAC Data Source Select 0 = Left DAC outputs left channel data 1 = Left DAC outputs right channel data
	14	DACR_SRC	1	Right DAC Data Source Select 0 = Right DAC outputs left channel data 1 = Right DAC outputs right channel data
R10 (0Ah) DAC Control	1	DACL_DATINV	0	Left DAC Invert 0 = Left DAC output not inverted 1 = Left DAC output inverted
	0	DACR_DATINV	0	Right DAC Invert 0 = Right DAC output not inverted 1 = Right DAC output inverted

Table 23 DAC Routing and Control

DAC INTERFACE VOLUME BOOST

A digital gain function is available at the audio interface to boost the DAC volume when a small signal is received on DACDAT. This is controlled using register bits DAC_BOOST[1:0]. To prevent clipping at the DAC input, this function should not be used when the boosted DAC data is expected to be greater than 0dBFS.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) Audio Interface 2	11:10	DAC_BOOST [1:0]	00	DAC Input Volume Boost 00 = 0dB 01 = +6dB (Input data must not exceed -6dBFS) 10 = +12dB (Input data must not exceed -12dBFS) 11 = +18dB (Input data must not exceed -18dBFS)

Table 24 DAC Interface Volume Boost

DIGITAL SIDETONE

A digital sidetone is available when ADCs and DACs are operating at the same sample rate. Digital data from either left or right ADC can be mixed with the audio interface data on the left and right DAC channels. Sidetone data is taken from the ADC high pass filter output, to reduce low frequency noise in the sidetone (e.g. wind noise or mechanical vibration).

The digital sidetone will not function when ADCs and DACs are operating at different sample rates.

When using the digital sidetone it is recommended that the ADCs are enabled before un-muting the DACs to prevent pop noise. The DAC volumes and sidetone volumes should be set to an appropriate level to prevent clipping at the DAC input.

The digital sidetone is controlled as shown in Table 25.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 (0Dh) Digital Sidetone	12:9	ADCL_DAC_SVOL [3:0]	0000	Left Digital Sidetone Volume (See Table 26 for volume range)
	8:5	ADCR_DAC_SVOL [3:0]	0000	Right Digital Sidetone Volume (See Table 26 for volume range)
	3:2	ADC_TO_DACL [1:0]	00	Left DAC Digital Sidetone Source 00 = No sidetone 01 = Left ADC 10 = Right ADC 11 = Reserved
	1:0	ADC_TO_DACR [1:0]	00	Right DAC Digital Sidetone Source 00 = No sidetone 01 = Left ADC 10 = Right ADC 11 = Reserved

Table 25 Digital Sidetone Control

ADCL_DAC_SVOL or ADCR_DAC_SVOL	Sidetone Volume
0000	-36
0001	-33
0010	-30
0011	-27
0100	-24
0101	-21
0110	-18
0111	-15
1000	-12
1001	-9
1010	-6
1011	-3
1100	0
1101	0
1110	0
1111	0

Table 26 Digital Sidetone Volume

DIGITAL TO ANALOGUE CONVERTER (DAC)

The WM8900 DACs receive digital input data from the DACDAT pin and via the digital sidetone path. The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

The analogue outputs from the DACs can then be mixed with other analogue inputs using the output mixers. This mix is fed to the output drivers for headphone or line outputs.

The DACs are enabled by the DACL_ENA and DACR_ENA register bits as defined in Table 27.

The DAC output stage bias current can be optimised by the DAC_BIAS register bits. Note that the optimum setting for minimum power consumption is not the power-on default value.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) Power Management 3	1	DACL_ENA	0	Left DAC Enable 0 = DAC disabled 1 = DAC enabled
	0	DACR_ENA	0	Right DAC Enable 0 = DAC disabled 1 = DAC enabled
R115 (73h) Output Bias Control	2:1	DAC_BIAS [1:0]	00	Adjusts DAC bias 00 = Full bias 01 = Half bias (recommended) 10 = Reserved 11 = Reserved

Table 27 DAC Enable Control

DAC DIGITAL VOLUME CONTROL

The output level of each DAC can be controlled digitally over a range from–71.625dB to 0dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 192$; MUTE for $X = 0$ 0dB for $192 \leq X \leq 255$

The DAC_VU bit controls the loading of digital volume control data. When DAC_VU is set to 0, the DACL_VOL or DACR_VOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to DAC_VU. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh) Left DAC Digital Volume	8	DAC_VU	0	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously
	7:0	DACL_VOL [7:0]	11000000 (0dB)	Left DAC Digital Volume (See Table 29 for volume range)
R12 (0Ch) Right DAC Digital Volume	8	DAC_VU	0	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously
	7:0	DACR_VOL [7:0]	11000000 (0dB)	Right DAC Digital Volume (See Table 29 for volume range)

Table 28 Digital Volume Control

DACL_VOL or DACR_VOL	Volume (dB)	DACL_VOL or DACR_VOL	Volume (dB)	DACL_VOL or DACR_VOL	Volume (dB)	DACL_VOL or DACR_VOL	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.000
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.000
3h	-70.875	43h	-46.875	83h	-22.875	C3h	0.000
4h	-70.500	44h	-46.500	84h	-22.500	C4h	0.000
5h	-70.125	45h	-46.125	85h	-22.125	C5h	0.000
6h	-69.750	46h	-45.750	86h	-21.750	C6h	0.000
7h	-69.375	47h	-45.375	87h	-21.375	C7h	0.000
8h	-69.000	48h	-45.000	88h	-21.000	C8h	0.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	0.000
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	0.000
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	0.000
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	0.000
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	0.000
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	0.000
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	0.000
10h	-66.000	50h	-42.000	90h	-18.000	D0h	0.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	0.000
12h	-65.250	52h	-41.250	92h	-17.250	D2h	0.000
13h	-64.875	53h	-40.875	93h	-16.875	D3h	0.000
14h	-64.500	54h	-40.500	94h	-16.500	D4h	0.000
15h	-64.125	55h	-40.125	95h	-16.125	D5h	0.000
16h	-63.750	56h	-39.750	96h	-15.750	D6h	0.000
17h	-63.375	57h	-39.375	97h	-15.375	D7h	0.000
18h	-63.000	58h	-39.000	98h	-15.000	D8h	0.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	0.000
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	0.000
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	0.000
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	0.000
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	0.000
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	0.000
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	0.000
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	0.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	0.000
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	0.000
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	0.000
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	0.000
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	0.000
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	0.000
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	0.000
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	0.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	0.000
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	0.000
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	0.000
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	0.000
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	0.000
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	0.000
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	0.000
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	0.000
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	0.000
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	0.000
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	0.000
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	0.000
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	0.000
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	0.000
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	0.000
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	0.000
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	0.000
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	0.000
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	0.000
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	0.000
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	0.000
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	0.000
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	0.000

Table 29 DAC Digital Volume Range

DAC SOFT MUTE AND SOFT UN-MUTE

The WM8900 has a soft mute and un-mute function, which, when enabled, gradually attenuates or amplifies the volume of the DAC output. When the DAC is un-muted the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DAC_MUTEMODE register bit. Conversely, when the DAC is muted the gain will either gradually ramp down to the digital mute level, or drop instantly to the digital mute level, depending on the DAC_MUTEMODE register bit setting.

The DAC is muted by default (DAC_MUTE = 1). To play back an audio signal, this function must first be disabled by setting the DAC_MUTE bit to 0.

Soft Mute Mode would typically be enabled (DAC_MUTEMODE = 1) when using DAC_MUTE during playback of audio data. When DAC_MUTE is set to logic 0 and the DAC is un-muted, the sudden volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing during a track).

Soft Mute Mode would typically be disabled (DAC_MUTEMODE = 0) when un-muting at the start of a music file, in order that the first part of the track is not attenuated (e.g. when starting playback of a new track, or resuming playback after pausing between tracks).

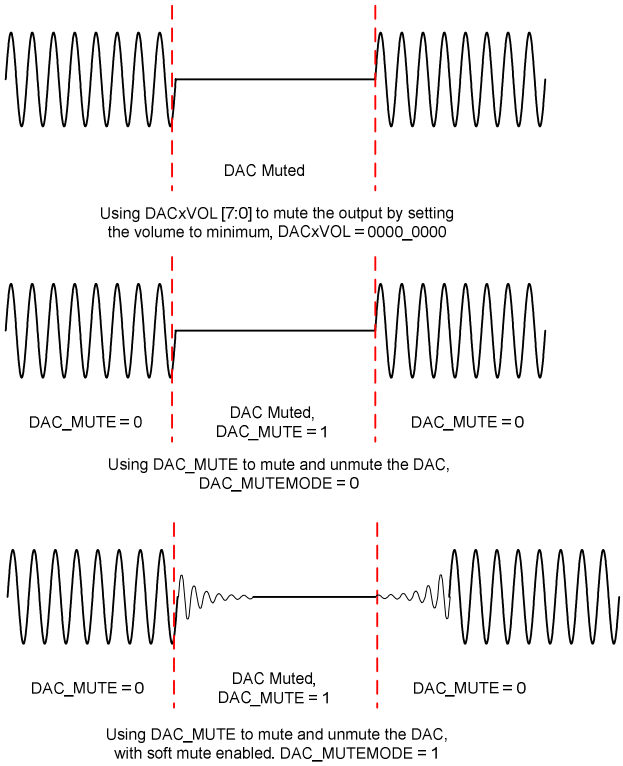


Figure 17 DAC Mute Control

The volume ramp rate during soft mute and un-mute is controlled by the DAC_MUTERATE bit. Ramp rates of fs/32 and fs/2 are selectable as shown in Table 30. The ramp rate determines the rate at which the volume will be increased or decreased. The actual ramp time depends on the extent of the difference between the muted and un-muted volume settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) DAC Control	7	DAC_MUTERATE	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k)
	6	DAC_MUTEMODE	0	DAC Soft Mute and Un-mute Mode 0 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to change immediately to DACL_VOL and DACR_VOL settings or change to digital mute level immediately 1 = Enabling soft-mute (DAC_MUTE=0) will cause the DAC volume to ramp up gradually to the DACL_VOL and DACR_VOL settings or gradually ramp down to digital mute level
	2	DAC_MUTE	1	DAC Mute Control 0 = DAC Un-mute 1 = DAC Mute

Table 30 DAC Soft-Mute Control

DAC MONO MIX

A DAC digital mono-mix mode can be enabled using the DAC_MONO register bit. This mono mix will be output on the enabled DACs. To prevent clipping, a -6dB attenuation is automatically applied to the mono mix.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) DAC Control	9	DAC_MONO	0	DAC Mono Mix 0 = Stereo 1 = Mono (Mono mix output on enabled DACs)

Table 31 DAC Mono Mix

DAC DE-EMPHASIS

Digital de-emphasis can be applied to the DAC playback data (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz. See "Digital Filter Characteristics" section for details of de-emphasis filter characteristics.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) DAC Control	5:4	DEEMP [1:0]	00	De-Emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No de-emphasis

Table 32 DAC De-Emphasis Control

DAC SLOPING STOPBAND FILTER

Two DAC filter types are available, selected by the register bit DAC_SB_FILT. When operating at lower sample rates (e.g. during voice communication) it is recommended that the sloping stopband filter type is selected (DAC_SB_FILT = 1) to reduce out-of-band noise which can be audible at low

DAC sample rates. See "Digital Filter Characteristics" section for details of DAC filter characteristics.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) DAC Control	8	DAC_SB_FILT	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband mode

Table 33 DAC Sloping Stopband Filter

DAC SIGMA-DELTA CLOCK RATE

When operating the DAC at lower sample rates (e.g. during voice communication) it is recommended that the DAC sigma-delta modulator clock is enabled by default (DAC_SDMCLK_RATE = 1) to maintain an independent clock rate and reduce idle channel noise. Setting DAC_SDMCLK_RATE to 0 will allow the DAC clock to scale with sample rate and give a minimal power consumption improvement, at the expense of idle channel noise increasing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) DAC Control	12	DAC_SDMCLK_RATE	1	DAC sigma delta modulator clock 0 = DAC clock scales with sample rate 1 = DAC clock independent of sample rate

Table 34 DAC Sigma-delta Modulator Clock Rate

OUTPUT SIGNAL PATH

The WM8900 has two analogue output mixers which allow the ADC bypass, DAC output and LINPUT3 (RINPUT3) and AUX signals to be combined as desired. The flexible configuration of these mixers allows a mono mix to be generated as well as combining audio signals (eg. speech) from the input bypass path. The output mixers are connected to two stereo line outputs; the built-in ground-referenced headphone driver may be connected to one of these line output pairs.

OUTPUT MIXER ENABLE

The output mixers are independently enabled by the MIXOUTL_ENA and MIXOUTR_ENA register bits, as described in Table 35.

The output mixers bias current can be optimised by the MIXOUT_BIAS register bits. Note that the optimum setting for minimum power consumption is not the power-on default value.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) Power Management 3	3	MIXOUTL_ENA	0	Left output mixer enable 0 = Mixer disabled 1 = Mixer enabled
	2	MIXOUTR_ENA	0	Right output mixer enable 0 = Mixer disabled 1 = Mixer enabled
R115 (R73h) Output Bias Control	8:7	MIXOUT_BIAS	00	Adjusts output mixer bias 00 = Full bias 01 = Half bias (recommended) 10 = Reserved 11 = Reserved

Table 35 Output Mixers Enable

OUTPUT MIXER CONFIGURATION

The output mixers are configured by the output mixer control registers, as described in Table 36. Each mixer input can be independently enabled/disabled. With the exception of the DAC output, each signal's gain can be controlled in the range -15dB to +6dB, as shown in Figure 18.

The DAC volume can be adjusted in the digital domain if required, see Table 28.

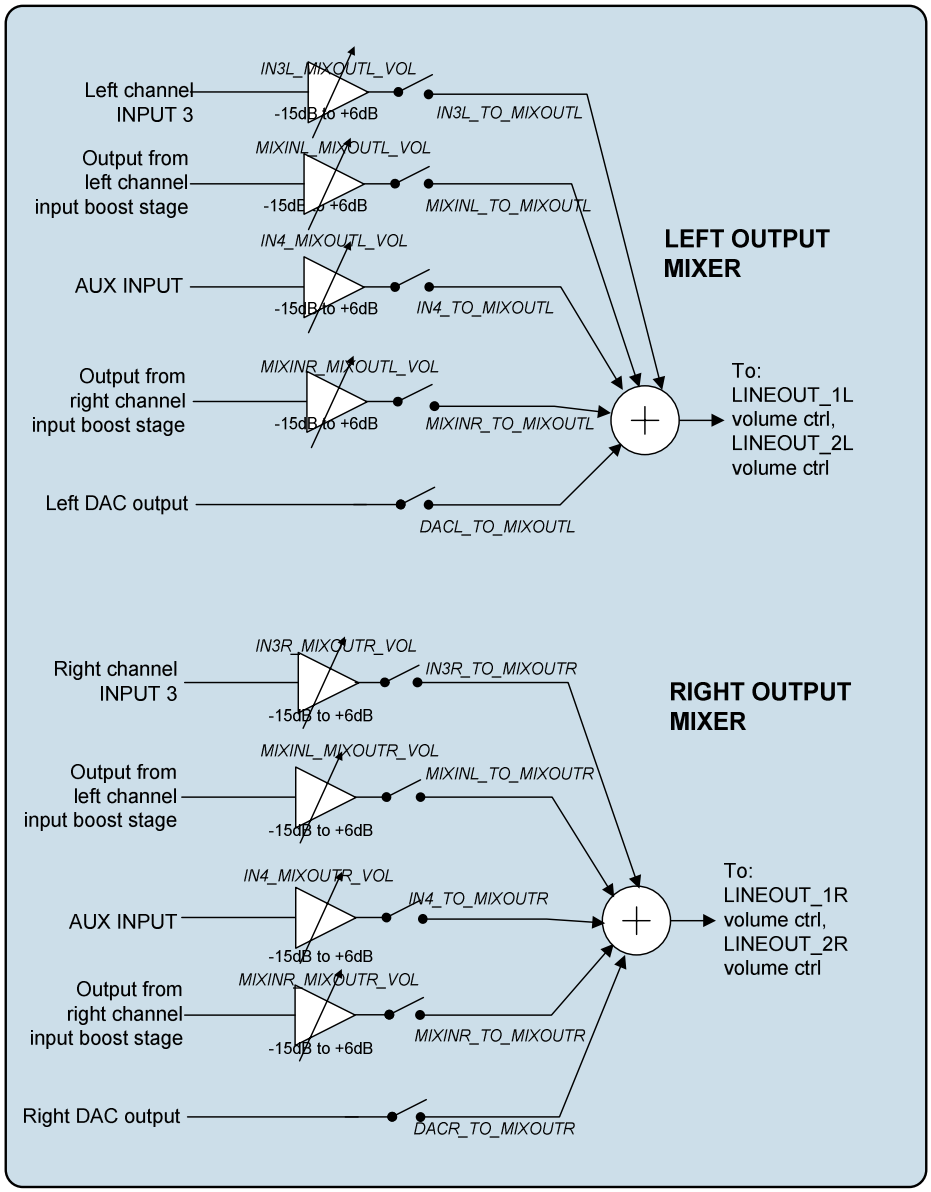


Figure 18 Output Mixers Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 (2Ch) Left Output Mixer Control 1	8	DACL_TO_MIXOUTL	0	Left DAC output to left output mixer 0 = not selected 1 = selected
	7	IN3L_TO_MIXOUTL	0	Left input 3 channel to left output mixer path 0 = not selected 1 = selected
	6:4	IN3L_MIXOUTL_VOL	101	Left input 3 channel to left output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
R45 (2Dh) Right Output Mixer Control 1	8	DACR_TO_MIXOUTR	0	Right DAC output to right output mixer 0 = not selected 1 = selected
	7	IN3R_TO_MIXOUTR	0	Right input 3 channel to right output mixer path 0 = not selected 1 = selected
	6:4	IN3R_MIXOUTR_VOL	101	Right input 3 channel to right output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
R46 (2Eh) Bypass 1	7	MIXINL_TO_MIXOUTL	0	Left bypass path (from the Left channel ADC input) to left output mixer 0 = not selected 1 = selected
	6:4	MIXINL_MIXOUTL_VOL	101	Left bypass path to left output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
	3	MIXINL_TO_MIXOUTR	0	Left bypass path (from the Left channel ADC input) to right output mixer 0 = not selected 1 = selected
	2:0	MIXINL_MIXOUTR_VOL	101	Left bypass path to right output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Bypass 2	7	MIXINR_TO_MIXOUTR	0	Right bypass path (from the Right channel ADC input) to right output mixer 0 = not selected 1 = selected
	6:4	MIXINR_MIXOUTR_VOL	101	Right bypass path to right output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
	3	MIXINR_TO_MIXOUTL	0	Right bypass path (from the Right channel ADC input) to left output mixer 0 = not selected 1 = selected
	2:0	MIXINR_MIXOUTL_VOL	101	Right bypass path to left output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
R48 (30h) AUX to Mixer Output Control	7	IN4_TO_MIXOUTL	0	AUX input channel to left output mixer path 0 = not selected 1 = selected
	6:4	IN4_MIXOUTL_VOL	101	AUX input channel to left output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
	3	IN4_TO_MIXOUTR	0	AUX input channel to right output mixer path 0 = not selected 1 = selected
	2:0	IN4_MIXOUTR_VOL	101	AUX input channel to right output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB

Table 36 Output Mixer Control

LINE OUTPUT ENABLE

Each analogue output driver can be independently enabled via the Power Management register bits, as described in Table 37. Muting and volume control of the outputs is only possible when the correct power management register bits are enabled. When the correct power management bit for an output is not set, some signal leakage to the output pin may occur.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 2	8	OUT1L_ENA	0	Left channel LINEOUT1 enable 0 = LINEOUT_1L disabled 1 = LINEOUT_1L enabled
	7	OUT1R_ENA	0	Right channel LINEOUT1 enable 0 = LINEOUT_1R disabled 1 = LINEOUT_1R enabled
R3 (03h) Power Management 3	6	OUT2L_ENA	0	Left channel LINEOUT2 enable 0 = LINEOUT_2L disabled 1 = LINEOUT_2L enabled
	5	OUT2R_ENA	0	Right channel LINEOUT2 enable 0 = LINEOUT_2R disabled 1 = LINEOUT_2R enabled

Table 37 Line Output Enable

LINEOUT_1L AND LINEOUT_1R OUTPUTS

The outputs LINEOUT_1L and LINEOUT_1R are capable of driving a 16Ω headphone load and are independently controlled by the register bits described in Table 38.

The outputs can be independently muted and the volumes controlled in the range -57dB to +6dB.

To allow simultaneous volume updates of left and right channels, output gains are not altered until a 1 is written to the OUT1_VU bit.

To prevent "zipper noise", a zero-cross function is provided, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOCLK_ENA register bit), the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout period is set by TOCLK_RATE. Note that this timer is the same timer as applied to the Input PGA zero-cross function.

LCOM FUNCTION

Common ground noise on LINEOUT1L and LINEOUT1R outputs can be eliminated by enabling the OUT1_FB_ENA bit. This allows the connection of the AUX/LCOM pin to the shared LINEOUT ground via a 4.7µF capacitor. Note that the AUX/LCOM pin cannot be used as an auxiliary input when used as a common ground connection. It is recommended that the AUX input is not connected to the output mixers (see register R48; IN4_TO_MIXOUTL and IN4_TO_MIXOUTR bits) and that the AUX boost stages are muted (R27; IN4L_BOOST and IN4R_BOOST) when using this configuration. This configuration can be seen below.

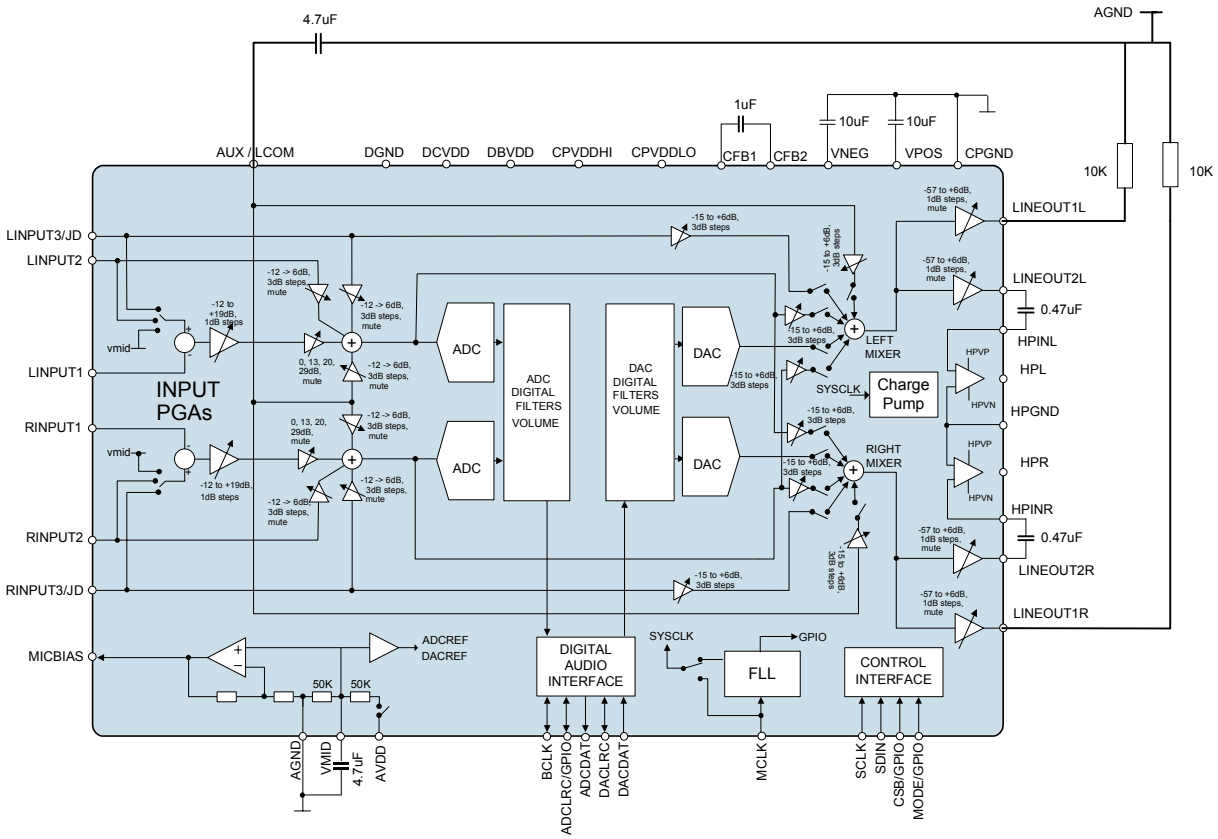


Figure 19 LCOM Common Ground Connection for LINEOUT1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R51 (33h) Left OUT1 Control	8	OUT1_VU	0	Left Channel LINEOUT1 Volume Update Writing a 1 to this bit will cause left and right LINEOUT1 volume to be updated simultaneously
	7	OUT1L_ZC	0	Left Channel LINEOUT1 Zero Cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6	OUT1L_MUTE	1	Left Channel LINEOUT1 Mute 0 = LINEOUT_1L Unmuted 1 = LINEOUT_1L Mute
	5:0	OUT1L_VOL [5:0]	111001	Left Channel LINEOUT1 Volume Control (-57dB -> +6dB in 1dB steps) 111111 = +6dB 000000 = -57dB
R52 (34h) Right OUT1 Control	8	OUT1_VU	0	Right Channel LINEOUT1 Volume Update Writing a 1 to this bit will cause left and right LINEOUT1 volume to be updated simultaneously
	7	OUT1R_ZC	0	Right Channel LINEOUT1 Zero Cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6	OUT1R_MUTE	1	Right Channel LINEOUT1 Mute 0 = LINEOUT_1R Unmuted 1 = LINEOUT_1R Mute
	5:0	OUT1R_VOL [5:0]	111001	Right Channel LINEOUT1 Volume Control (-57dB -> +6dB in 1dB steps) 111111 = +6dB 000000 = -57dB
R3 (03h) Power Management 3	8	OUT1_FB_ENA	0	Common mode feedback for Lineout1 0: Disable common mode feedback 1: Enable common mode feedback

Table 38 LINEOUT_1L/ LINEOUT_1R Volume Control

LINEOUT_2L AND LINEOUT_2R OUTPUTS

The outputs LINEOUT_2L and LINEOUT_2R are independently controlled by the register bits described in Table 39. The outputs can be independently muted and the volumes controlled in the range -57dB to +6dB.

To allow simultaneous volume updates of left and right channels, output gains are not altered until a 1 is written to the OUT2_VU bit.

To prevent "zipper noise", a zero-cross function is provided, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOCLK_ENA register bit), the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout period is set by TOCLK_RATE. Note that this timer is the same timer as applied to the Input PGA zero-cross function.

With the addition of small capacitors linking the LINEOUT_2L and LINEOUT_2R signals to the Headphone driver, the HP_L and HP_R pins can drive a 16Ω or 32Ω headphone. The headphone output is ground referenced and therefore no further capacitors are required and no headphone click noise is produced when muting or un-muting. See “Ultra Low Power Ground-Referenced Headphone Output” for further details.

The Line Output 2 Volume Control register fields are described in Table 39.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R53 (35h) Left OUT2 Control	8	OUT2_VU	0	Left Channel LINEOUT2 Volume Update Writing a 1 to this bit will cause left and right LINEOUT2 volume to be updated simultaneously
	7	OUT2L_ZC	0	Left Channel LINEOUT2 Zero Cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6	OUT2L_MUTE	1	Left Channel LINEOUT2 Mute 0 = LINEOUT_2L Unmuted 1 = LINEOUT_2L Mute
	5:0	OUT2L_VOL [5:0]	111001	Left Channel LINEOUT2 Volume Control (-57dB -> +6dB in 1dB steps) 111111 = +6dB 000000 = -57dB
R54 (36h) Right OUT2 Control	8	OUT2_VU	0	Right Channel LINEOUT2 Volume Update Writing a 1 to this bit will cause left and right LINEOUT2 volume to be updated simultaneously
	7	OUT2R_ZC	0	Right Channel LINEOUT2 Zero Cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6	OUT2R_MUTE	1	Right Channel LINEOUT2 Mute 0 = LINEOUT_2R Unmuted 1 = LINEOUT_2R Mute
	5:0	OUT2R_VOL [5:0]	111001	Right Channel LINEOUT2 Volume Control (-57dB -> +6dB in 1dB steps) 111111 = +6dB 000000 = -57dB

Table 39 LINEOUT_2L/ LINEOUT_2R Volume Control

See "Volume Updates" for more information on volume update bits, zero cross and timeout operation.

ULTRA-LOW POWER GROUND-REFERENCED HEADPHONE OUTPUT

The WM8900 headphone amplifier architecture offers highly efficient DAC playback at typical listening levels. A level-shifting charge pump enables the headphone output to be ground referenced, eliminating the need for large DC blocking capacitors on the output. Class G operation provides additional benefits to power consumption. Typical power consumption figures are detailed in Table 2, Table 3, Table 4,Table 5 and Table 6.

The headphone amplifier configuration is illustrated in Figure 20.

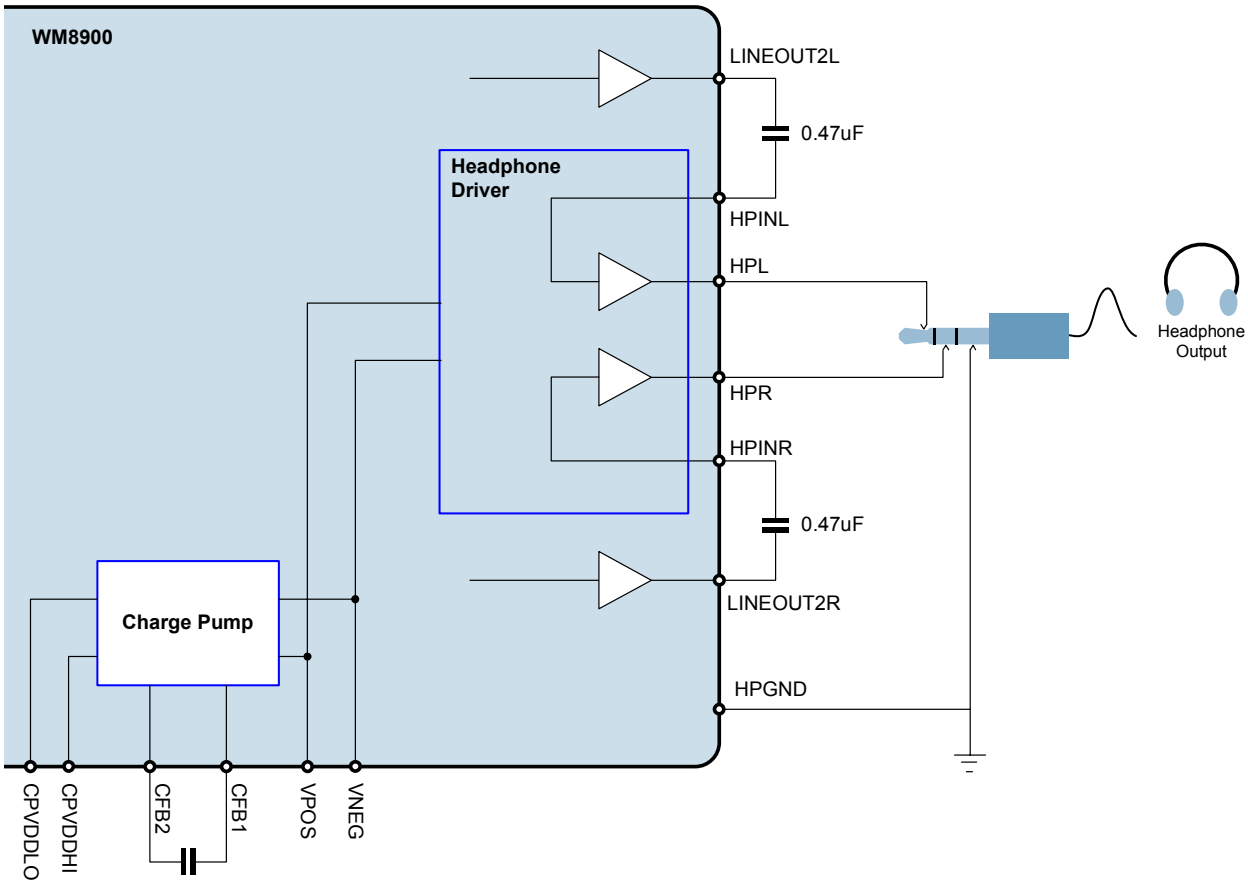


Figure 20 Ultra-Low Power Ground-Referenced Headphone Output

The Charge Pump and the Headphone Amplifier are described separately in the following two sections.

CHARGE PUMP

The level shifting charge pump has two outputs (VPOS and VNEG) and two inputs (CPVDDHI and CPVDDLO). The input voltage selection is automatically determined by the output volume required. For correct functionality, CPVDDHI should be higher than CPVDDLO.

The positive output, VPOS, generated by the charge pump will be half the input voltage. The negative output, VNEG, will be a negative voltage of the same magnitude. The Charge Pump is enabled by CP_ENA, as defined in Table 40.

The charge pump requires SYSCLK to be present at all times when the headphone amplifier is in use.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) Power Management 3	7	CP_ENA	0	Charge Pump Enable 0 = Disable charge pump 1 = Enable charge pump Must be enabled when the headphone output is used.

Table 40 Charge Pump Control

HEADPHONE AMPLIFIER

The Headphone amplifier input (HP_INL / HP_INR) must be coupled to the LINEOUT_2L / LINEOUT_2R via a small DC blocking capacitor as illustrated in Figure 20. A high pass filter is formed between this capacitor and the impedance of the headphone amplifier, which is approximately 20kΩ. The choice of capacitor determines the high pass filter cut-off frequency as detailed in Table 41, and can be chosen to fit the desired bass response requirements.

CAPACITOR VALUE	-3DB CUT-OFF FREQUENCY
0.47 uF	17 Hz
1 uF	8 Hz

Table 41 Headphone AC Coupling Capacitor

A zobel network is required to stabilise the amplifier. The zobel network should comprise a 50 ohm (±5%) resistor and a 20nF (±20%) capacitor, as illustrated in the recommended external components diagram..

The Headphone amplifier can be controlled via the register settings described in Table 42. See also Table 9 for additional control fields that may be used to minimise pops and clicks under certain mode changes.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R58 (3Ah) Headphone Control 1	7	HP_IPSTAGE_ENA	0	Headphone input stage Enable 0 = Headphone input stage disabled 1 = Headphone input stage enabled
	6	HP_OPSTAGE_ENA	0	Headphone output stage Enable 0 = Headphone output stage disabled 1 = Headphone output stage enabled

Table 42 Headphone Amplifier Control

If the headphone output is being used in a mono configuration, it is a requirement that the un-used OUT2 volume PGA (R53 (0x35) or R54 (0x36)) should be set up with minimum volume setting and not muted, i.e. must clear bits 6:0. This ensures that the Class G power saving features of WM8900 will function correctly for the mono output channel.

MASTER BIAS

The overall analogue master bias current can be optimised by the MASTER_BIAS register bits. Note that the optimum setting for minimum power consumption is not the power-on default value. The various power saving options are discussed in Table 45.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R116 (74h) Master Bias Control	8:7	MASTER_BIAS	10	Adjusts master bias 00 = Reserved 01 = 0.75 bias 10 = full bias - default 11 = Reserved

Table 43 Master Bias Control

OPTIMAL PLAYBACK POWER CONSUMPTION

During DAC to Headphone playback, reduced bias modes are available to optimise power consumption, giving increased battery life with a slight performance trade-off. These modes are selected using the register bits DAC_BIAS (R115 bits 2:1),MIXOUT_BIAS (R115 bits 8:7), and MASTER_BIAS (R116 bits 8:7).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R115 (73h) Output Bias Control	8:7	MIXOUT_BIAS	00	Adjusts output mixer bias 00 = Full bias 01 = Half bias (recommended) 10 = Reserved 11 = Reserved
	2:1	DAC_BIAS	00	Adjusts DAC bias 00 = Full bias 01 = Half bias (recommended) 10 = Reserved 11 = Reserved
R116 (74h) Master Bias Control	8:7	MASTER_BIAS	10	Adjusts master bias 00 = Reserved 01 = 0.75 bias 10 = full bias - default 11 = Reserved

Table 44 Playback Power Management

The reduced bias modes are available using the combination of register settings as shown.

Default:	DAC_BIAS = 00 (Full bias)	MIXOUT_BIAS = 00 (Full bias)	MASTER_BIAS = 10 (Full bias)
Reduced Power Mode:	DAC_BIAS = 01 (Half bias)	MIXOUT_BIAS = 00 (Full bias)	MASTER_BIAS = 10 (Full bias)
Ultra Low Power Mode:	DAC_BIAS = 01 (Half bias)	MIXOUT_BIAS = 01 (Half bias)	MASTER_BIAS = 01 (x0.75 bias)

Table 45 Bias Conditions for Default, Reduced and Ultra Low Power Modes

The performance and power consumption differences between these modes are detailed in Table 3, Table 4, Table 5, and Table 6 on page 15, and in Table 1.

VOLUME UPDATES

Volume settings will not be applied to input or output PGAs until a '1' is written to one of the update bits. This is to allow left and right channels to be updated at the same time, as shown in Figure 21.

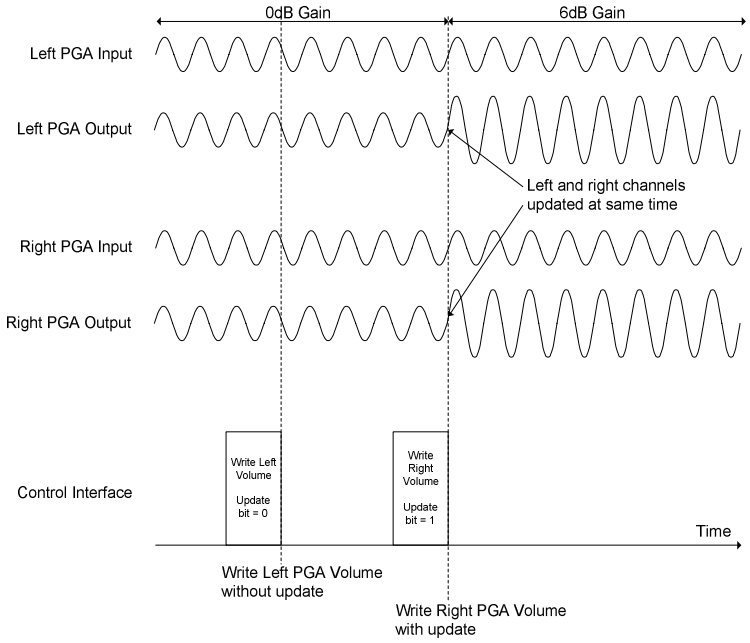


Figure 21 Simultaneous Left and Right Volume Updates

If the volume is adjusted while the signal is a non-zero value, an audible click can occur as shown in Figure 22.

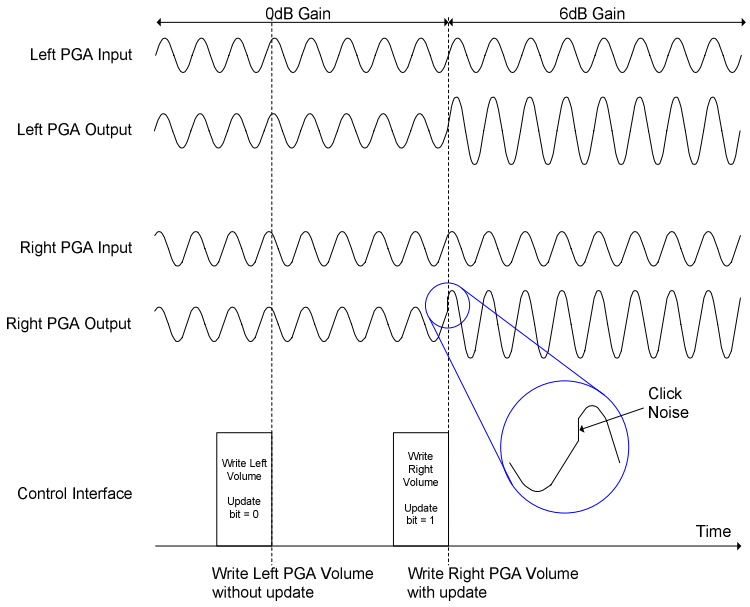


Figure 22 Click Noise During Volume Update

In order to prevent this click noise, a zero cross function is provided. When enabled, this will cause the PGA volume to update only when a zero crossing occurs, minimising click noise as shown in Figure 23.

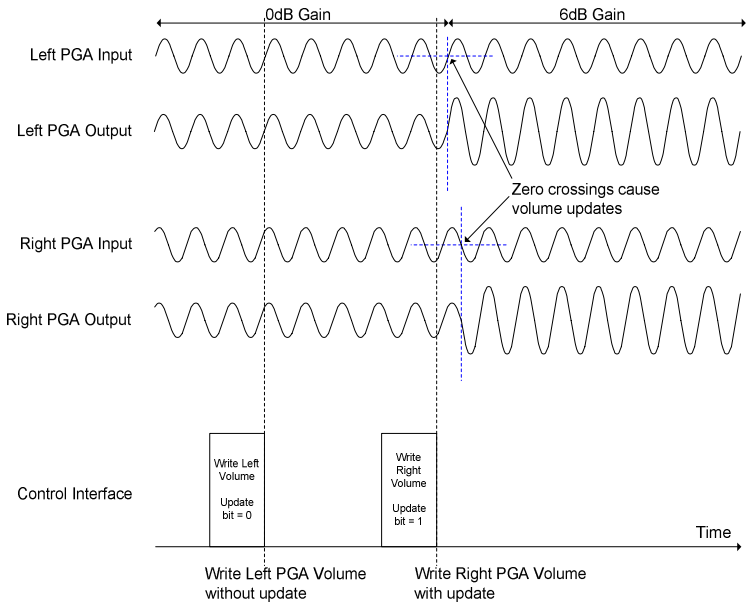


Figure 23 Volume Update Using Zero Cross Detection

If there is a long period where no zero-crossing occurs, a timeout circuit in the WM8900 will automatically update the volume. The volume updates will occur between one and two timeout periods, depending on when the volume update bit is set as shown in Figure 24. The TOCLK_ENA register bit must be set to enable this timeout function. The timeout period is set by TOCLK_RATE.

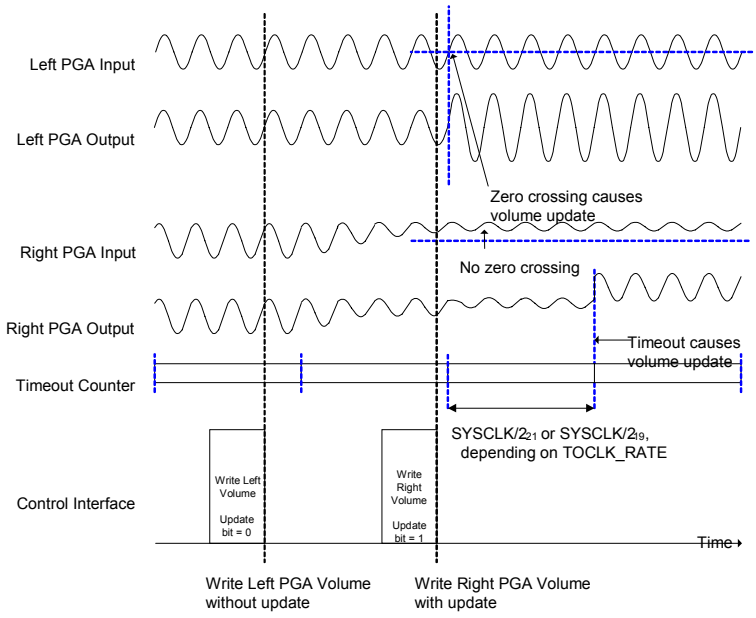


Figure 24 Volume Update after Timeout

HEADPHONE JACK DETECT

The headphone jack detect feature may be used to automatically control any of the Line outputs and Headphone outputs when a connection is made to a jack socket. Any of the ADCLRC/GPIO, LINPUT3/JD, RINPUT3/JD, MODE/GPIO or CSB/GPIO pins may be selected as headphone jack detect input to control the lineout enables. The most likely usage of this feature would be to disable the Line outputs when a headphone is plugged into a jack socket.

The Jack Detect mode is enabled via the JD_ENA register bit. When enabled, the Jack Detect input is selected via the JD_SRC field - this determines which pin of the WM8900 is used to activate the Jack Detect feature. The JD_MODE bit may be used to reverse the polarity of the selected Jack Detect input.

The selected Jack Detect input has two states - logic 0 and logic 1. For each of these two states, the desired combination of Line output enables can be set by the user. The JD_EN0 register field controls which outputs are enabled in the logic 0 Jack Detect state. The JD_EN1 field controls which outputs are enabled in the logic 1 Jack Detect state.

The Line output and Headphone outputs controlled by the Jack Detect mode are controlled via an AND function with their normal enable signals. Therefore, any output that is enabled via the JD_EN0 or JD_EN1 fields will only be active if its normal enable signal (see Table 37) is also enabled. Any output that is disabled via its normal enable signal will be unaffected by the Jack Detect mode.

Any Line or Headphone output that is to be controlled by the Jack Detect mode must have its normal enable signal active. Any Line or Headphone output that is to be unaffected by the Jack Detect mode must set enabled in both the JD_EN0 and JD_EN1 fields.

The Jack Detect input must be de-bounced for correct operation. To do this, TOCLK_ENA must be set and TOCLK_RATE set according to the desired fast/slow response time.

The de-bounced headphone Jack Detect signal may be output to the GPIO pin (see “General Purpose Input/Output”). This is not possible if the pin is used for any other GPIO function.

Note that, when LINPUT3/JD or RINPUT3/JD is used as the Jack Detect input, the logic levels are CMOS levels (0.3 AVDD / 0.7 AVDD).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h) GPIO Control	9	JD_ENA	0	Jack Detect Switch Enable 0 = Jack Detect disabled 1 = Jack Detect enabled
	8	JD_MODE	0	Jack Detect Switch Polarity 0 = Jack Detect active high 1 = Jack Detect active low
	3:1	JD_SRC[2:0]	000	Jack Detect Input Select 000 = ADCLRC/GPIO used for jack detect 001 = CSB/GPIO used for jack detect 010 = LINPUT3/JD used for jack detect 011 = RINPUT3/JD used for jack detect 100 = MODE/GPIO used for jack detect 101 to 111 Reserved
R17 (11h) Jack Detect Control	13:8	JD_EN1[5:0]	000000	Output enables when selected jack detection input is logic 1 JD_EN1[0] =1 enables LINEOUT_1L JD_EN1[1] =1 enables LINEOUT_1R JD_EN1[2] =1 enables LINEOUT_2R JD_EN1[3] =1 enables LINEOUT_2R JD_EN1[4] =1 enables Headphone JD_EN1[5] =1 enables Charge Pump

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5:0	JD_EN0[5:0]	000000	Output enables when selected jack detection input is logic 0 JD_EN0[0] =1 enables LINEOUT_1L JD_EN0[1] =1 enables LINEOUT_1R JD_EN0[2] =1 enables LINEOUT_2R JD_EN0[3] =1 enables LINEOUT_2R JD_EN0[4] =1 enables Headphone JD_EN0[5] =1 enables Charge Pump
R7 (07h) Clocking 2	1	TOCLK_RATE	0	Slow Clock Selection (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)
	0	TOCLK_ENA	0	Slow Clock Enable (Must be enabled for jack detect de-bounce) 0 = Slow Clock Disabled 1 = Slow Clock Enabled

Table 46 Jack Detect Control

DISABLED OUTPUTS

Whenever an analogue output is disabled, it remains connected to VREF through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between VREF and each output can be controlled using register bit VROI. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 20kΩ.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (1Eh) Additional Control	0	VROI	0	VREF to Analogue Output Resistance (Disabled Outputs) 0 = 500Ω from buffered VMID to output 1 = 20kΩ from buffered VMID to output

Table 47 Disabled Outputs to VREF Resistance

THERMAL SHUTDOWN

The headphone outputs can drive very large currents. To protect the WM8900 from overheating a thermal shutdown circuit is included. If the device temperature reaches approximately 150^0C and the thermal shutdown circuit is enabled (TEMP_SD = 1; TEMP_ENA = 1) the headphone amplifiers (HP_L, HP_R) and the Line Outputs (LINEOUT_1L, LINEOUT_1R, LINEOUT_2L and LINEOUT_2R) will be disabled.

TEMP_ENA must be set to 1 to enable the temperature sensor when using the TEMP_SD thermal shutdown function. The output of the temperature sensor can also be output to the GPIO pin.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (1Eh) Additional Control	1	TEMP_SD	1	Thermal Shutdown Enable 0 = Thermal shutdown disabled 1 = Thermal shutdown enabled (TEMP_ENA must be enabled for this function to work)
R18 (12h) GPIO Control	0	TEMP_ENA	1	Temperature Sensor Enable 0 = Temperature sensor disabled 1 = Temperature sensor enabled

Table 48 Thermal Shutdown

GENERAL PURPOSE INPUT/OUTPUT

The WM8900 has three dual purpose input/output pins which may be configured according to the selected control mode and according to GPIO register settings. The three pins are as follows:

- ADCLRC/GPIO - ADC Left/Right frame clock or GPIO pin
- CSB - Control Interface control or GPIO pin
- MODE - Control Interface control or GPIO pin

Two analogue inputs may also be configured as headphone jack detect inputs, by use of some of the same GPIO register fields. These two inputs are as listed below. The default configuration for these pins is to be analogue inputs.

- LINPUT3/JD2 - Analogue input or headphone detect input
- RINPUT3/JD3 - Analogue input or headphone detect input

The ADCLRC/GPIO pin can be configured as a left/right frame clock for the ADC, a headphone jack detect input, or as one of a number of GPIO output functions. The configuration of this pin as ADCLRC or as GPIO is determined by the ADCLRC_FN bit.

During power-up, if the MODE pin is low, the serial interface mode of operation is selected as 2 wire, in this case CSB is sampled in order to select the correct device address according to Table 69. Thereafter, the normal CSB function is not required in 2-wire control mode, and the CSB pin is automatically configured as one of the GPIO functions.

In 3-wire control mode, the MODE pin may be configured as GPIO by register bit MODE_FN. (See “Control Interface” for further details of this bit.)

The GPIO function of the pin (or pins) selected as GPIO is controlled by the ADCLRC_SRC register. It is possible for more than one of the GPIO pins to output the same function simultaneously. The polarity of the GPIO output may be inverted by setting the ADCLRC_INV bit. If headphone jack detect input is selected, then only one of the possible sources may be selected as the jack detect input; the chosen input will be determined by the JD_SRC field. (See “Headphone Jack Detect” for further details of this bit.)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) Audio Interface 2	6	ADCLRC_FN	0	ADCLRC/GPIO Pin Function Select 0 = ADCLRC frame clock for ADC 1 = GPIO pin
R18 (12h) GPIO Control	7	ADCLRC_INV	0	GPIO Output Polarity Invert 0 = Non inverted 1 = Inverted
	6:4	ADCLRC_SRC [2:0]	000	GPIO Pin Function Select: 000 = Jack detect input 001 = Reserved 010 = Temperature ok 011 = Debounced jack detect output 100 = SYSCLK output 101 = FLL lock 110 = Logic 0 111 = Logic 1

Table 49 GPIO Control

The slow clock must be enabled when using the Jack Detect function. This is used to de-bounce the jack detect input. See “Headphone Jack Detect” for further details of the associated controls.

The temperature sensor must be enabled for the ‘Temperature ok’ GPIO output to function properly. See “Thermal Shutdown” for further details.

The SYSCLK GPIO output is derived from SYSCLK and also set by a programmable divider OPCLK_DIV. See “Clocking and Sample Rates” for further details of this field.

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data into the WM8900 and outputting ADC data from it. It uses five pins:

- ADCDAT: ADC data output
- ADCLRC: ADC data alignment clock
- DACDAT: DAC data input
- DACLRC: DAC data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK, ADCLRC and DACLRC can be outputs when the WM8900 operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

ADCLRC can also be configured as a GPIO pin. In this case, the ADC will use DACLRC as a frame clock. The ADCLRC/GPIO pin function should not be modified while the ADC is enabled.

Four different audio data formats are supported:

- Left justified
- Right justified
- I2S
- DSP mode

All four of these modes are MSB first. They are described in the “Audio Data Formats” section below. Refer to the “Electrical Characteristics” section for timing information.

Time division multiplexing (TDM) is available in all four data format modes. The WM8900 can be programmed to send and receive data in one of two time slots.

MASTER AND SLAVE MODE OPERATION

The WM8900 can be configured as either a master or slave mode device. As a master device the WM8900 generates BCLK, ADCLRC and DACLRC and thus controls sequencing of the data transfer on ADCDAT and DACDAT. In slave mode, the WM8900 responds with data to clocks it receives over the digital audio interface. The mode can be selected by writing to the BCLK_DIR, ADCLRC_DIR and DACLRC_DIR register bits. Master and slave modes are illustrated below.

Note that the WM8900 also supports mixed master and slave modes - see “Audio Interface Control”.

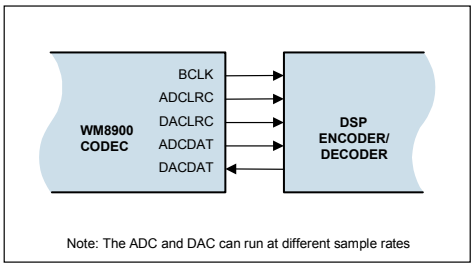


Figure 25 Master Mode

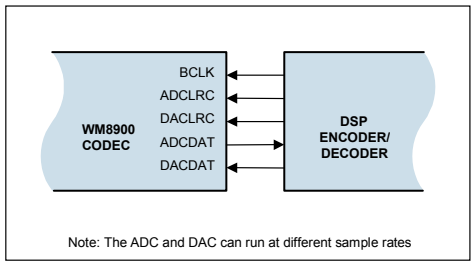


Figure 26 Slave Mode

OPERATION WITH ADCLRC AS GPIO

When the ADCLRC/GPIO pin is configured as a GPIO pin (ADCLRC_FN = 1), the DACLRC pin is used as a frame clock for ADCs and DACs as shown below. The ADCs and DACs must operate at the same sample rate in this mode. See “General Purpose Input/Output” section for details of GPIO pin configuration.

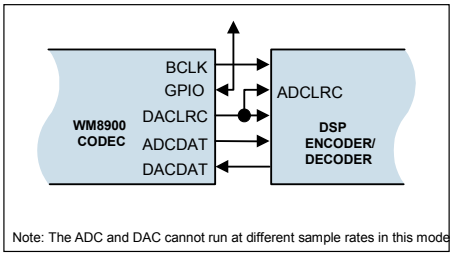


Figure 27 Master Mode with ADCLRC as GPIO

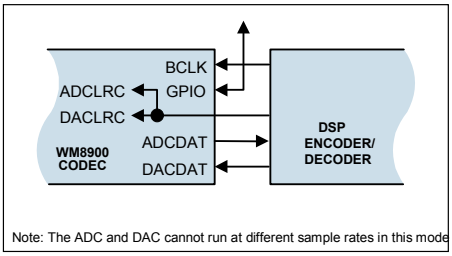


Figure 28 Slave Mode with ADCLRC as GPIO

The Audio Interface output control is illustrated above. The left-right clock control bits, ADCLRC_DIR and DACLRC_DIR, determine whether the corresponding clock output is enabled (see "Audio Interface Control" for the definition of these bits). The ADCLRC_FN register bit controls the mode of operation of the ADCLRC/GPIO pin (see "GPIO" for the definition of this bit).

OPERATION WITH TDM

The digital audio interface on WM8900 has the facility of tri-stating the ADCDAT pin to allow multiple data sources on the same bus. Time division multiplexing (TDM) is also supported, allowing audio output data to be transferred simultaneously from two different sources. The WM8900 ADCs and DACs support TDM in master and slave modes, on both interfaces, and for all data formats and word lengths.

TDM is enabled using register bits AIFADC_TDM and AIFDAC_TDM. The TDM data slot is programmed using register bits AIFADC_TDM_CHAN and AIFDAC_TDM_CHAN. (See "Audio Interface Control" for the definition of these bits.)

When operating in TDM mode with another device, the possible connections are as follows:

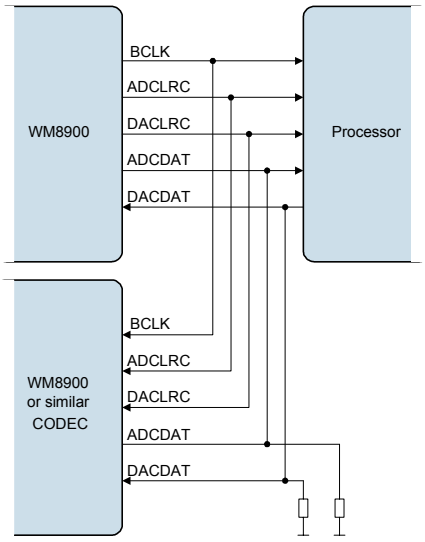


Figure 29 TDM with WM8900 as Master

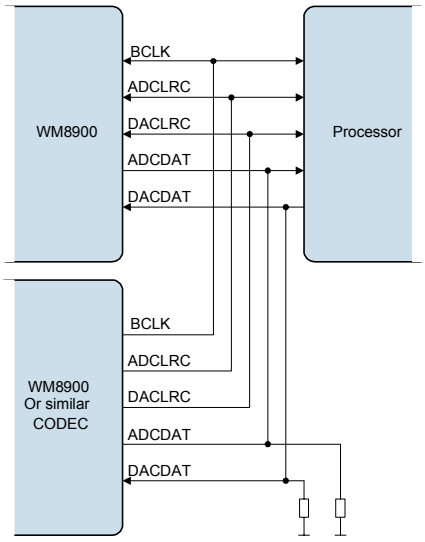


Figure 30 TDM with Other CODEC as Master

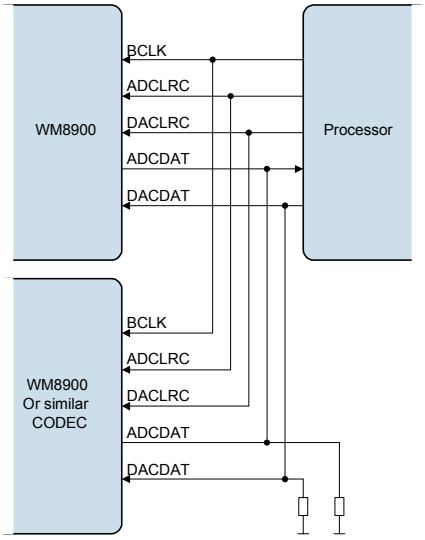


Figure 31 TDM with Processor as Master

Note: The WM8900 is a 24-bit device. If the user operates the WM8900 in 32-bit mode then the 8 LSBs will be ignored on the receiving side and not driven on the transmitting side. It is therefore recommended to add a pull-down resistor if necessary to the DACDAT line and the ADCDAT line in TDM mode.

AUDIO DATA FORMATS (NORMAL MODE)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

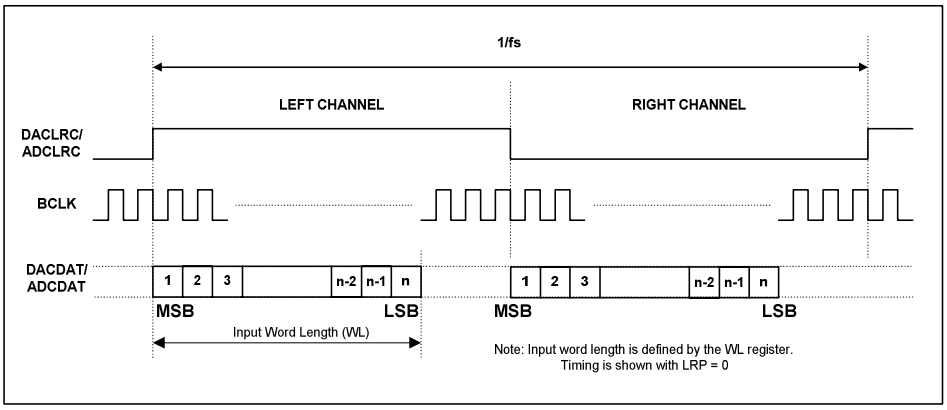


Figure 32 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

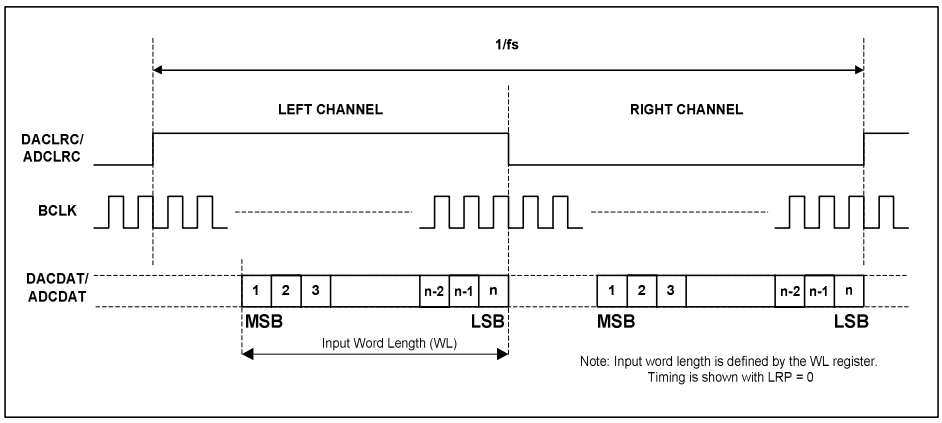


Figure 33 Right Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

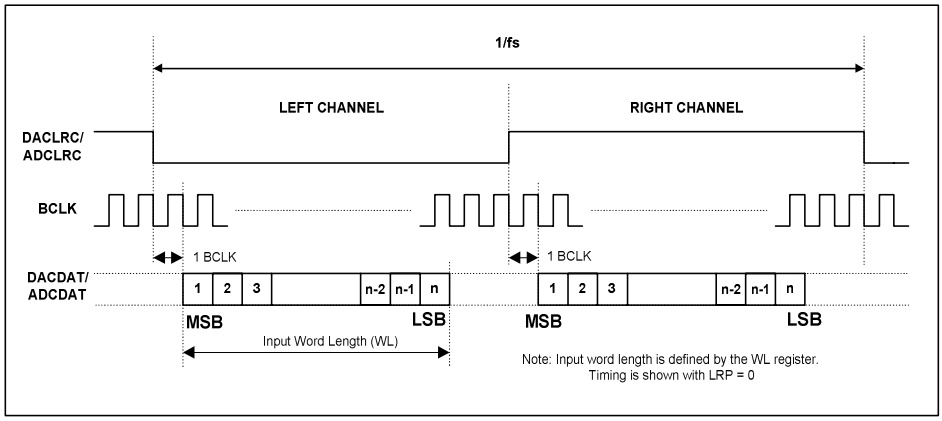


Figure 34 I^2S Justified Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by AIF_LRCLKINV) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 35 and Figure 36. In device slave mode, Figure 37 and Figure 38, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

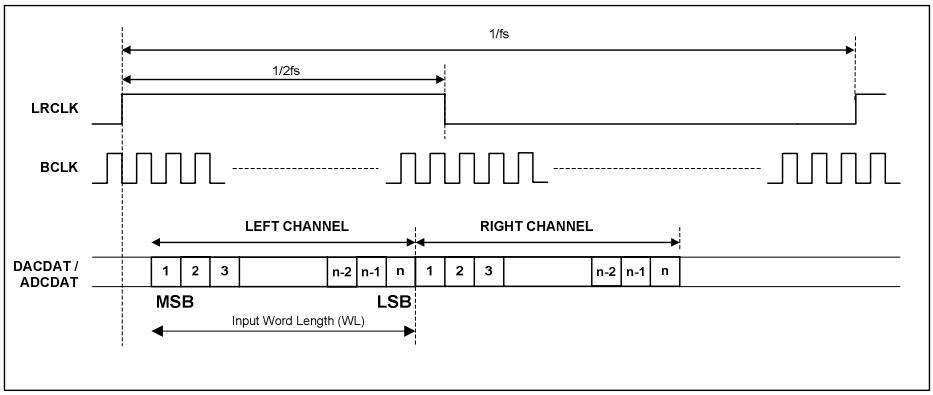


Figure 35 DSP/PCM Mode Audio Interface (mode A, AIF_LRCLKINV=0, Master)

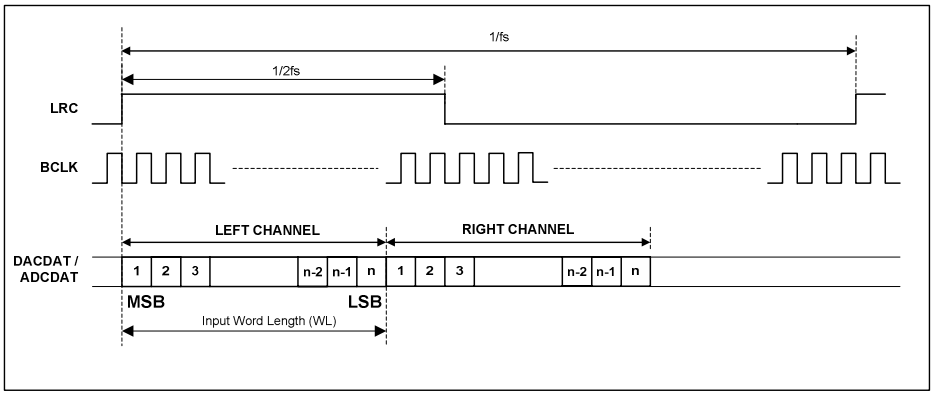


Figure 36 DSP/PCM Mode Audio Interface (mode B, AIF_LRCLKINV =0, Master)

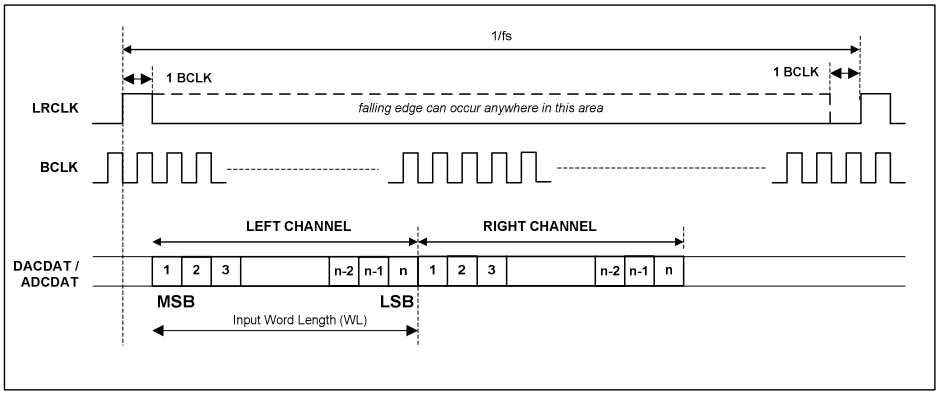


Figure 37 DSP/PCM Mode Audio Interface (mode A, AIF_LRCLKINV =0, Slave)

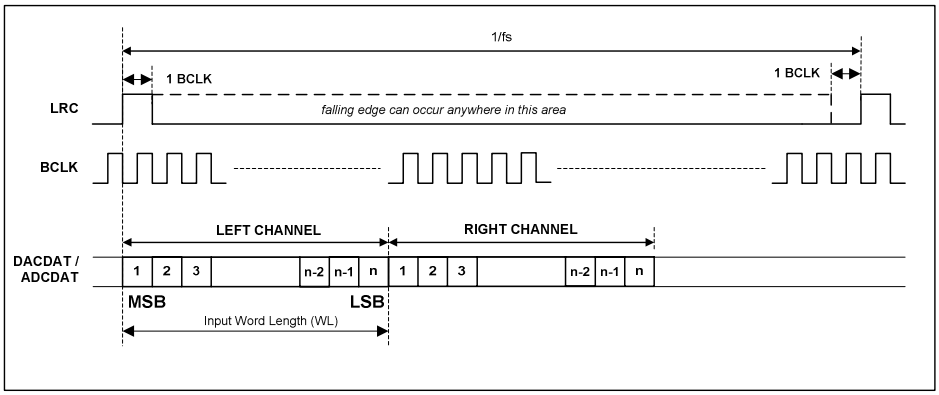


Figure 38 DSP/PCM Mode Audio Interface (mode B, AIF_LRCLKINV =0, Slave)

AUDIO DATA FORMATS (TDM MODE)

TDM is supported in master and slave mode and is enabled by register bits AIF_ADC_TDM and AIF_DAC_TDM. All audio interface data formats support time division multiplexing (TDM) for ADC and DAC data.

Two time slots are available (Slot 0 and Slot 1), selected by register bits AIFADC_TDM_CHAN and AIFDAC_TDM_CHAN which control time slots for the ADC data and the DAC data.

When TDM is enabled, the ADCDAT pin will be tri-stated immediately before and immediately after data transmission, to allow another ADC device to drive this signal line for the remainder of the sample period.

When TDM is enabled, BCLK frequency must be high enough to allow data from both time slots to be transferred. The number of BCLK cycles from the start of Slot 0 to the start of Slot 1 is determined by the selected word length of the applicable interface. The timing of Slot 0 and Slot 1 also depends upon the selected data format as shown in Figure 39 to Figure 43.

Timing diagrams for the various interface formats in TDM mode are shown below for the ADC. Similar timings apply to the DACDAT and DACLRC pins.

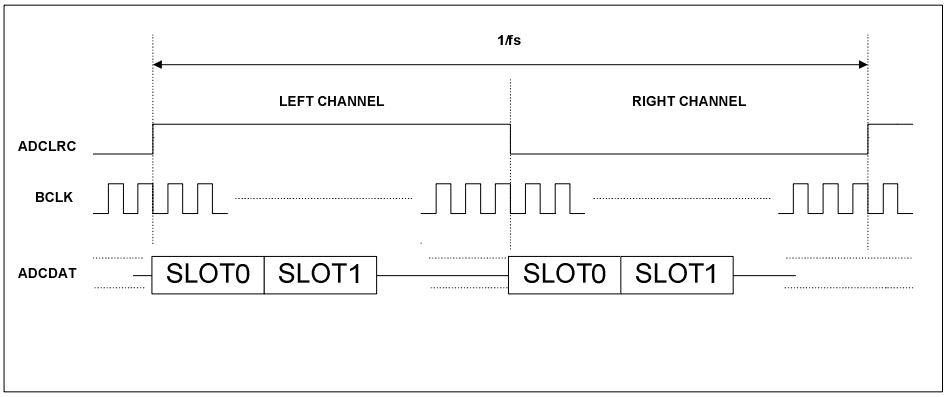


Figure 39 TDM in Left-Justified Mode

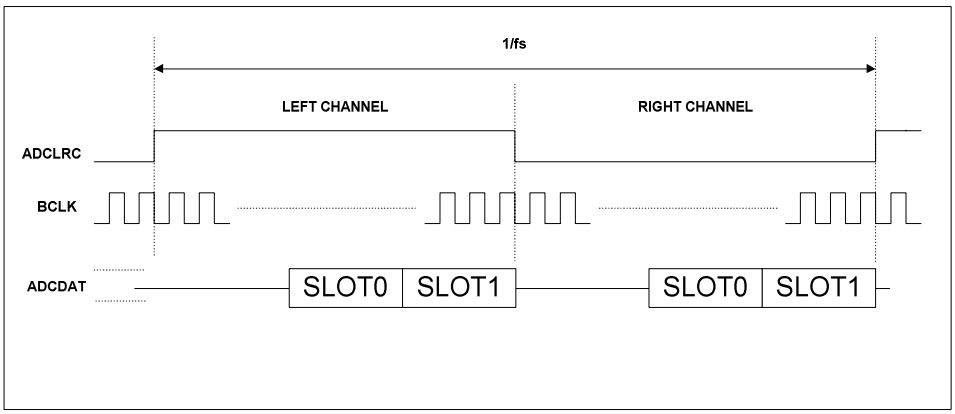


Figure 40 TDM in Right-Justified Mode

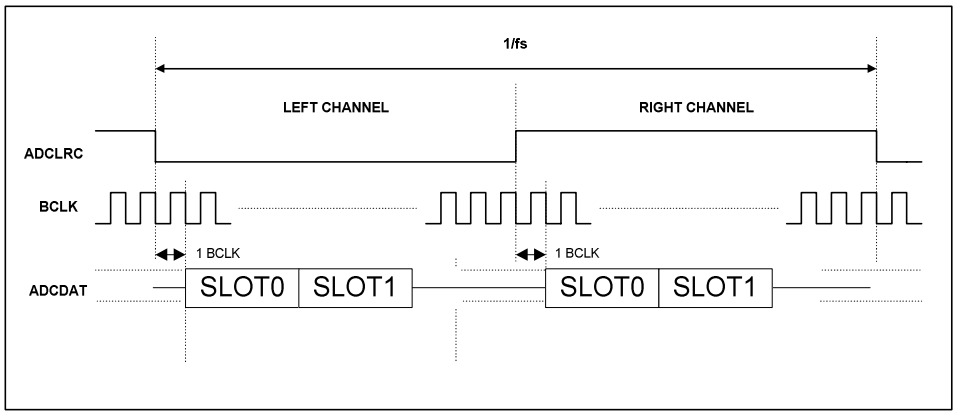


Figure 41 TDM in I²S Mode

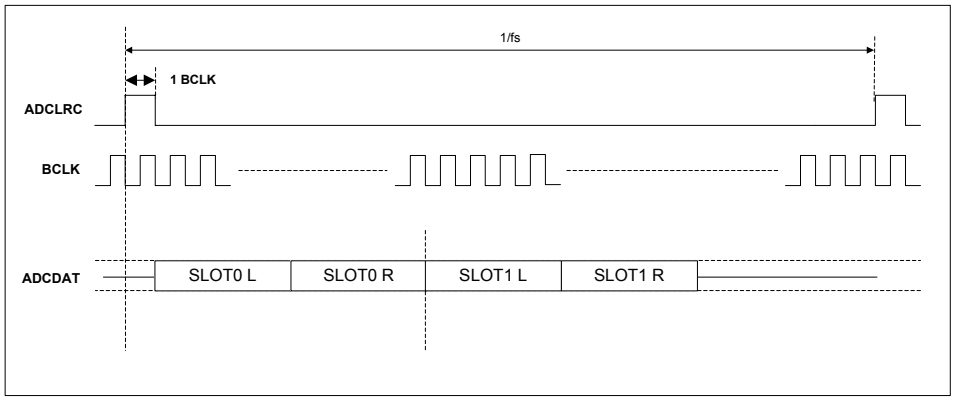


Figure 42 TDM in DSP/PCM Mode A

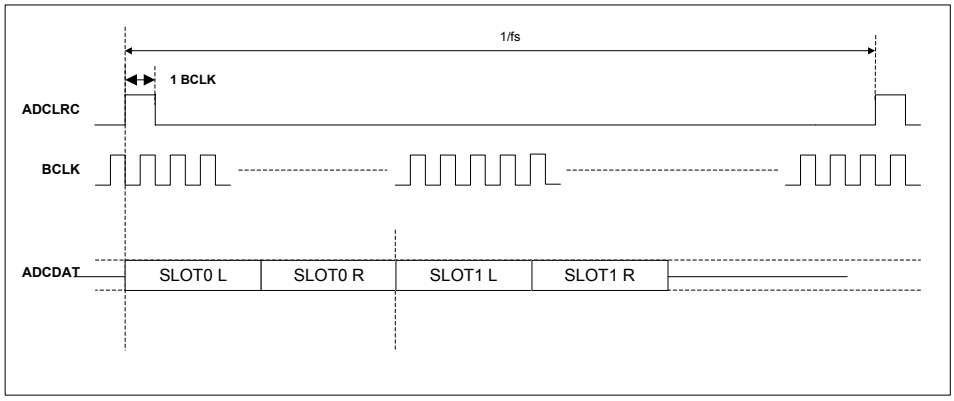


Figure 43 TDM in DSP/PCM Mode B

AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and the TDM parameters are summarised in Table 50.

In Master mode BCLK, ADCLRC and DACLRC are outputs, and the frequency of ADCLRC, DACLRC and BCLK are set by the fields ADCLRC_RATE, DACLRC_RATE and BCLK_DIV (see "Clocking and Sample Rates"). In Slave mode BCLK, ADCLRC and DACLRC are inputs.

It is possible to control these clock outputs individually using register bits ADCLRC_DIR, DACLRC_DIR and BCLK_DIR, allowing mixed master and slave modes for the ADCs and DACs. See Table 52 for a definition of these fields.

BCLK inverted (AIF_BCLK_INV = 1) is not available in Master Mode (BCLK_DIR = 1).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Audio Interface 1	13	AIFADC_TDM	0	ADC TDM Enable 0 = Normal ADCDAT operation 1 = TDM enabled on ADCDAT
	12	AIFADC_TDM_CHAN	0	ADCDAT TDM Channel Select 0 = ADCDAT outputs data on slot 0 1 = ADCDAT output data on slot 1
	8	AIF_BCLK_INV	0	BCLK Invert 0 = BCLK not inverted 1 = BCLK inverted (see note 1)
	7	AIF_LRCLK_INV	0	Right, left and I^2S modes – LRCLK polarity 0 = normal LRCLK polarity 1 = invert LRCLK polarity
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)
	6:5	AIF_WL [1:0]	10	Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits
	4:3	AIF_FMT [1:0]	10	Digital Audio Interface Format 00 = Right justified 01 = Left justified 10 = I^2S Format 11 = DSP Mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) Audio Interface 2	13	AIFDAC_TDM	0	DAC TDM Enable 0 = Normal DACDAT operation 1 = TDM enabled on DACDAT
	12	AIFDAC_TDM_CHAN	0	DACDAT TDM Channel Select 0 = DACDAT data input on slot 0 1 = DACDAT data input on slot 1

Table 50: Audio Data Format Control

Notes

1) AIF_BCLK_INV = 1 is not available in Master Mode (BCLK_DIR = 1).

AUDIO INTERFACE OUTPUT TRISTATE

The audio interface tri-state feature is controlled by register bit AIF_TRI, as described in Table 51.

This bit can be used to tri-state the ADCDAT pin and switch ADCLRC, DACLRC and BCLK to inputs. Note that, in Slave mode, ADCLRC, DACLRC and BCLK are already configured as inputs by default and will be unaffected by the tri-state selection.

When the ADCLRC/GPIO pin is configured as a GPIO, this pin is not affected by the AIF_TRI register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Clocking 2	12	AIF_TRI	0	Tri-states ADCDAT and switches ADCLRC, DACLRC and BCLK to inputs. 0 = ADCDAT is an output; DACLRC and BCLK may be inputs or outputs; ADCLRC is input, output or GPIO. 1 = ADCDAT is tri-stated; DACLRC and BCLK are inputs; ADCLRC is input or GPIO.

Table 51 Tri-stating the Audio Interface

ADCLRC, DACLRC AND BCLK ENABLE

The ADCLRC, DACLRC and BCLK pins may be individually configured as inputs or outputs, allowing mixed master and slave modes for the ADCs and DACs.

ADCLRC may be configured as an input or output by setting the ADCLRC_DIR register bit as defined in Table 52. If AIF_TRI is set to 1, then ADCLRC will be an input irrespective of ADCLRC_DIR. If ADCLRC_FN is set to 1, then ADCLRC will be a GPIO irrespective of ADCLRC_DIR or ADCLRC_FN. When ADCLRC is configured as an output, this clock will be enabled when one or both ADCs are enabled.

DACLRC may be configured as an input or output by setting the DACLRC_DIR register bit as defined in Table 52. If AIF_TRI is set to 1, then DACLRC will be an input irrespective of DACLRC_DIR. When DACLRC is configured as an output, this clock will be enabled when one or both DACs are enabled.

BCLK may be configured as an input or output by setting the BCLK_DIR register bit as defined in Table 52. If AIF_TRI is set to 1, then BCLK will be an input irrespective of BCLK_DIR. When BCLK is configured as an output, this clock will be enabled when any of the ADCs or DACs is enabled.

When ADCLRC is configured as a GPIO (using ADCLRC_FN - see “General Purpose Input/Output”), the DACLRC is used for the ADCs and the DACs and will only be disabled when both ADCs and both DACs are disabled. If one or both DACs are enabled, the DACLRC clock rate will be determined by DACLRC_RATE. If both DACs are disabled, and ADCLRC is configured as a GPIO, then the DACLRC clock rate will be set by ADCLRC_RATE.

Table 52 describes how these clock signals are controlled.

See “Clocking and Sample Rates” for the definition of how the clock frequencies are set.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Clocking 1	0	BCLK_DIR	0	BCLK Direction 0 = BCLK is input 1 = BCLK is output
R8 (08h) Audio Interface 3	11	ADCLRC_DIR	0	ADCLRC Direction 0 = ADCLRC is input 1 = ADCLRC is output
R9 (09h) Audio Interface 4	11	DACLRC_DIR	0	DACLRC Direction 0 = DACLRC is input 1 = DACLRC is output

Table 52 Master Clock Controls

COMPANDING

The WM8900 supports A-law and μ-law companding on both transmit (ADC) and receive (DAC) sides. Companding can be enabled on the DAC or ADC audio interfaces by writing the appropriate value to the DAC_COMP or ADC_COMP register bits respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) Audio Interface 2	4	DAC_COMP	0	DAC Companding enable 0 = off 1 = on
	3	DAC_COMPMODE	0	DAC Companding mode select: 0 = μ-law 1 = A-law
	2	ADC_COMP	0	ADC Companding enable 0 = off 1 = on
	1	ADC_COMPMODE	0	ADC Companding mode select: 0 = μ-law 1 = A-law

Table 53 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

μ-law (where μ=255 for the U.S. and Japan):

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \qquad -1 \le x \le 1$

A-law (where A=87.6 for Europe):

$F(x) = A|x| / (1 + \ln A) \qquad \}$ for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A) \qquad \}$ for $1/A \le x \le 1$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ-law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSB’s of data.

Companding converts 13 bits (μ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. The input data range is separated into 8 levels, allowing low amplitude signals better precision than that of high amplitude signals. This is to exploit the operation of the human auditory system, where louder sounds do not require as much resolution as quieter sounds. The companded signal is an 8-bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits).

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 54 8-bit Companded Word Composition

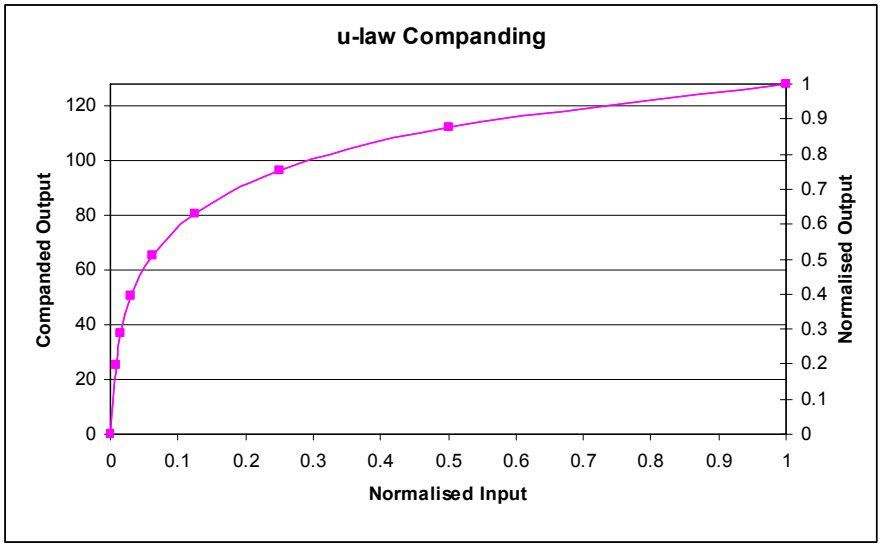


Figure 44 µ-Law Companding

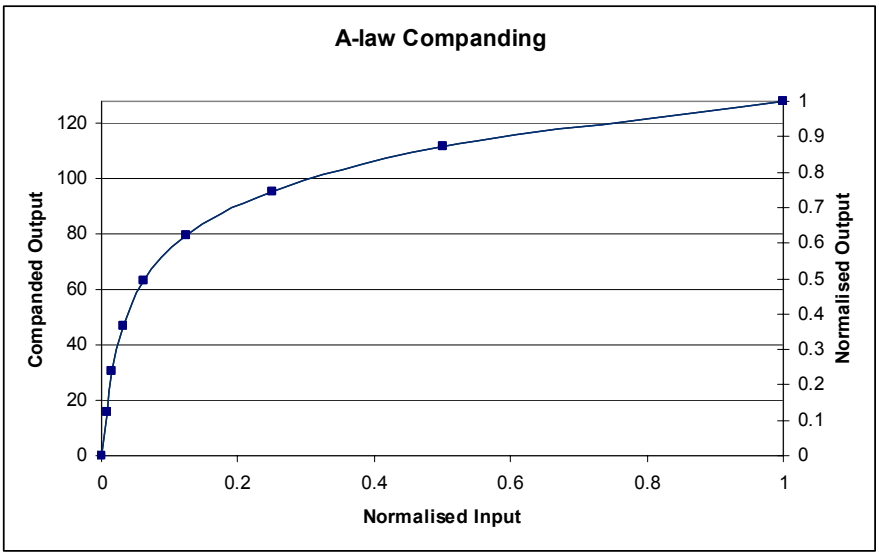


Figure 45 A-Law Companding

LOOPBACK

Setting the LOOPBACK register bit enables digital loopback. When this bit is set, the output data from the ADC audio interface is fed directly into the DAC data input interface.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) Audio Interface 2	0	LOOPBACK	0	Digital Loopback Function 0 = No loopback. 1 = Loopback enabled, ADC data output is fed directly into DAC data input.

Table 55 Loopback Control

Notes:

1. Master Mode: ADC and DAC left/right clocks must be connected together externally, or be of the same frequency and completely synchronised, when using LOOPBACK function (ADCLRC_FN=1)
2. Slave Mode: It is recommended to set ADCLRC_FN = 1 as well, otherwise ADCLRC and DACLRC must be running at the same BCLK rate and in phase.
3. When Loopback is enabled simultaneously to the Digital Sidetone, ADC data will be mixed with DAC data through both signal paths.

CLOCKING AND SAMPLE RATES

Clocks for the ADCs, DACs, DSP core functions, the digital audio interface and the Ground-Referenced Headphone output driver are all derived from a common internal clock source, SYSCLK.

SYSCLK can either be derived directly from MCLK, or may be generated from an FLL using MCLK or DACLRC as an external reference. The SYSCLK source is selected by MCLK_SRC. Many commonly-used audio sample rates can be derived directly from typical MCLK frequencies; the FLL provides additional flexibility for a wider range of MCLK or DACLRC frequencies.

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, using ADC_CLKDIV and DAC_CLKDIV. These fields must be set according to the required sampling frequency and depending upon the selected clocking mode. Two clocking modes are provided - Normal mode allows selection of the commonly used sample rates from typical audio system clocking frequencies (eg. 12.288MHz); USB mode allows many of these sample rates to be generated from a 12MHz USB clock. Depending on the available clock sources, the USB mode may be used to save power by supporting 44.1kHz operation without recourse to the FLL.

In Normal mode,

ADC_SYSCLK = 256 x ADC Sampling Frequency

DAC_SYSCLK = 256 x DAC Sampling Frequency

In USB mode,

ADC_SYSCLK = 272 x ADC Sampling Frequency

DAC_SYSCLK = 272 x DAC Sampling Frequency

The above equations determine the required values for ADC_CLKDIV and DAC_CLKDIV. The clocking mode is selected via the AIF_LRCLKRATE field.

In master mode, BCLK is also derived from SYSCLK via a programmable division set by BCLK_DIV. In the case where the ADCs and DACs are operating at different sample rates, BCLK must be set according to whichever is the faster rate. In Master Mode, internal clock divide and phase control mechanisms ensure that the BCLK, ADCLRC and DACLRC edges will occur in a predictable and repeatable position relative to each other and to the data for a given combination of ADC/DAC sample rates and BCLK settings. In Slave Mode, the host processor must ensure that BCLK, ADCLRC and DACLRC are fully synchronised; if these inputs are not synchronised, unpredictable pops and noise may result.

Changing the clocking or sample rates on the WM8900 may result in audible pops and clicks. It is recommended that the amplifier mute control bits are used to enable/disable the analogue outputs whenever a change is made to any of the clocking or sample rates. The mute control bits for specific amplifier stages within the WM8900 are detailed in the applicable sections within this datasheet. Detailed information is available for specific requirements - see “Applications Information”.

When the ADCLRC/GPIO pin is configured as a GPIO, a clock derived from SYSCLK may be output on this pin to provide clocking for other parts of the system. The frequency of this signal is set by OPCLK_DIV.

A slow clock derived from SYSCLK may be used to provide de-bouncing of the headphone detect function, and to set the timeout period for volume updates when zero-cross functions are used. This clock is enabled by TOCLK_ENA and its frequency is set by TOCLK_RATE.

The overall clocking scheme is illustrated in Figure 46.

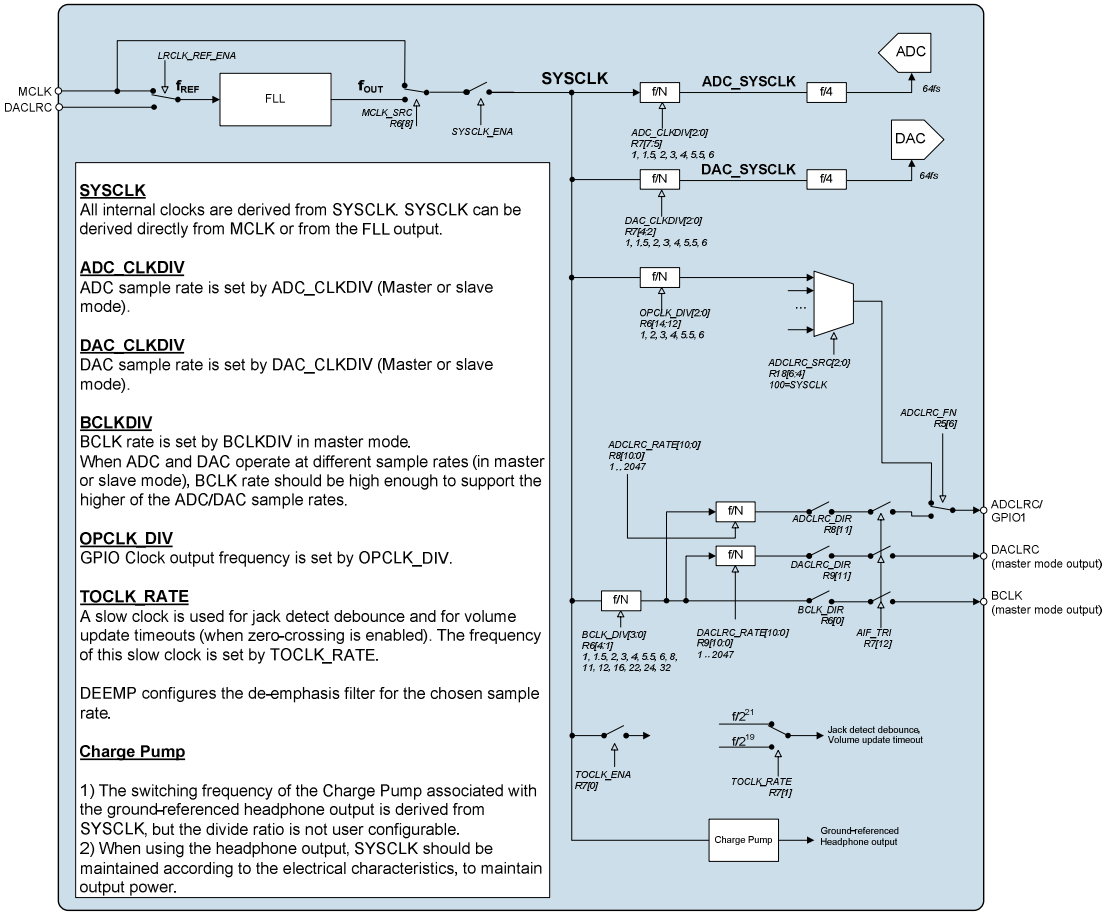


Figure 46 System Clocking

SYSCLK CONTROL

The MCLK_SRC bit is used to select the source for SYSCLK. The source may be either MCLK or the output of the FLL. These fields are described in Table 56. See “FLL” for further details of the Frequency Locked Loop control.

When the internal clock source is switched from one value to another using MCLK_SRC, the change of source will only occur following a falling edge of the source signal that was originally selected. In the case where the clock source is switched from FLL to MCLK, a suitable falling edge can be ensured by disabling the FLL after selection of MCLK as the source.

The recommended sequence of actions to switch from FLL to MCLK source is as follows:

- Select MCLK as source (MCLK_SRC = 0)
- Disable FLL (FLL_ENA = 0)
- Disable FLL oscillator (FLL_OSC_ENA = 0) (Optional)

Note that, as an alternative to the above sequence, a software reset may be used to re-select MCLK as the default SYSCLK source

The recommended sequence of actions to switch from MCLK to FLL source is as follows:

- Enable FLL oscillator (FLL_OSC_ENA = 1)
- Enable FLL (FLL_ENA = 1)
- Allow for FLL lock time to elapse.
- Select FLL as source (MCLK_SRC = 1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Clocking 1	8	MCLK_SRC	0	Clock Source selection 0 = SYSCLK derived from MCLK 1 = SYSCLK derived from FLL output

Table 56 SYSCLK Control

ADC / DAC SAMPLE RATES

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, by setting the register fields ADC_CLKDIV and DAC_CLKDIV. These fields must be set according to the SYSCLK frequency, and according to the selected mode of operation (Normal or USB). The applicable fields are described in Table 57.

Selection of USB mode enables a 12MHz USB clock to be used to generate the required internal clock signals. Table 58 describes the available sample rates using four different common MCLK frequencies. The AIF_LRCLKRATE field must be set as described in Table 57 to ensure correct operation of internal functions according to the SYSCLK / Fs ratio.

In Normal mode, the programmable division set by ADC_CLKDIV must ensure that ADC_SYSCLK is 256 * ADC Sampling Frequency. DAC_CLKDIV must ensure that DAC_SYSCLK is 256 * DAC Sampling Frequency.

There are constraints on the SYSCLK frequency when using the headphone output. SYSCLK should be maintained according to the electrical characteristics shown in Table 1, to maintain output power.

In USB mode, ADC_CLKDIV must ensure that ADC_SYSCLK is 272 * ADC Sampling Frequency. DAC_CLKDIV must ensure that DAC_SYSCLK is 272 * DAC Sampling Frequency.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) DAC Control	10	AIF_LRCLKRATE	0	Mode Select 1 = USB mode (272 * Fs) 0 = Normal mode (256 * Fs)
R7 (07h) Clocking 2	7:5	ADC_CLKDIV [2:0]	000	ADC Sample rate divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2 011 = SYSCLK / 3 100 = SYSCLK / 4 101 = SYSCLK / 5.5 110 = SYSCLK / 6 111 = Reserved
	4:2	DAC_CLKDIV [2:0]	000	DAC Sample rate divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2 011 = SYSCLK / 3 100 = SYSCLK / 4 101 = SYSCLK / 5.5 110 = SYSCLK / 6 111 = Reserved

Table 57 ADC / DAC Sample Rate Control

SYSCLK	ADC / DAC SAMPLE RATE DIVIDER	CLOCKING MODE	ADC / DAC SAMPLE RATE
12.2880 MHz	000 = SYSCLK / 1	Normal (256 * Fs)	48 kHz
	001 = SYSCLK / 1.5		32 kHz
	010 = SYSCLK / 2		24 kHz
	011 = SYSCLK / 3		16 kHz
	100 = SYSCLK / 4		12 kHz
	101 = SYSCLK / 5.5		Not used
	110 = SYSCLK / 6		8 kHz
	111 = Reserved		Reserved
11.2896 MHz	000 = SYSCLK / 1	Normal (256 * Fs)	44.1 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		22.05 kHz
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		11.025 kHz
	101 = SYSCLK / 5.5		8.018 kHz
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved
12.0000 MHz	000 = SYSCLK / 1	USB (272 * Fs)	44.118 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		22.059 kHz
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		11.029 kHz
	101 = SYSCLK / 5.5		8.021 kHz
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved
2.0480 MHz	000 = SYSCLK / 1	Normal (256 * Fs)	8 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		Not used
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		Not used
	101 = SYSCLK / 5.5		Not used
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved

Table 58 Derivation of Sample Rates in Normal / USB Modes

Note that, in USB mode, the ADC / DAC sample rates do not match exactly with the commonly used sample rates (eg. 44.118 kHz instead of 44.100 kHz). At most, the difference is less than 0.5%, which is within normal accepted tolerances. Data recorded at 44.100 kHz sample rate and replayed at 44.118 kHz will experience a slight (sub 0.5%) pitch shift as a result of this difference.

Note USB mode cannot be used to generate a 48kHz samples rate from a 12MHz MCLK. The FLL should be used in this case.

The user must ensure correct synchronisation of data across the digital interfaces. This is particularly important when different sample rates are used, as described above.

BCLK CONTROL

In Master Mode, BCLK is derived from SYSCLK via a programmable division set by BCLK_DIV, as described in Table 59.

BCLK_DIV must be set to an appropriate value to ensure that there are sufficient BCLK cycles to transfer the complete data words from the ADCs and to the DACs.

Note that, although the ADC and DAC can run at different sample rates, they share the same bit clock BCLK. In the case where different ADC / DAC sample rates are used, the BCLK frequency should be set according to the higher of the ADC / DAC bit rates.

In Slave Mode, BCLK is generated externally and appears as an input to the CODEC. The host device must provide sufficient BCLK cycles to transfer complete data words to the ADCs and DACs.

See "Digital Audio Interface" for details of Master/Salve operation. See "Audio Interface Control" for further details of how BCLK is configured as an input or output.

BCLK_DIV = 32 (1101) is not available in USB mode (AIF_LRCLKRATE = 1).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Clocking 1	4:1	BCLK_DIV [3:0]	0000	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 = SYSCLK / 32 (see note 1) 1110 = SYSCLK / 44 1111 = SYSCLK / 48

Table 59 BCLK Control

Notes

1. Not available in USB mode (AIF_LRCLKRATE = 1).

Table 60 shows the maximum word lengths supported for a given SYSCLK and BCLK_DIV, assuming that one or both the ADCs and DACs are running at maximum rate.

SYSCLK	BCLK DIVIDER BCLK_DIV	BCLK RATE (MASTER MODE) (MHz)	MAXIMUM WORD LENGTH
12.288 MHz	0000 = SYSCLK / 1	12.288	32
	0001 = SYSCLK / 1.5	8.192	32
	0010 = SYSCLK / 2	6.144	32
	0011 = SYSCLK / 3	4.096	32
	0100 = SYSCLK / 4	3.072	32
	0101 = SYSCLK / 5.5	2.2341818	20
	0110 = SYSCLK / 6	2.048	20
	0111 = SYSCLK / 8	1.536	16
	1000 = SYSCLK / 11	1.117091	8
	1001 = SYSCLK / 12	1.024	8
	1010 = SYSCLK / 16	0.768	8
	1011 = SYSCLK / 22	0.558545	N/A
	1100 = SYSCLK / 24	0.512	N/A
	1101 = SYSCLK / 32	0.384	N/A
	1110 = SYSCLK / 32	0.384	N/A
	1111 = SYSCLK / 32	0.384	N/A
11.2896 MHz	0000 = SYSCLK / 1	11.2896	32
	0001 = SYSCLK / 1.5	7.5264	32
	0010 = SYSCLK / 2	5.6448	32
	0011 = SYSCLK / 3	3.7632	32
	0100 = SYSCLK / 4	2.8224	32

SYSCLK	BCLK DIVIDER BCLK_DIV	BCLK RATE (MASTER MODE) (MHz)	MAXIMUM WORD LENGTH
	0101 = SYSCLK / 5.5	2.052655	20
	0110 = SYSCLK / 6	1.8816	20
	0111 = SYSCLK / 8	1.4112	16
	1000 = SYSCLK / 11	1.026327	8
	1001 = SYSCLK / 12	0.9408	8
	1010 = SYSCLK / 16	0.7056	8
	1011 = SYSCLK / 22	0.513164	N/A
	1100 = SYSCLK / 24	0.4704	N/A
	1101 = SYSCLK / 32	0.3528	N/A
	1110 = SYSCLK / 32	0.3528	N/A
	1111 = SYSCLK / 32	0.3528	N/A

Table 60 BCLK Divider in Master Mode

ADCLRC / DACLRC CONTROL

In Master Mode, ADCLRC and DACLRC are derived from BCLK via programmable dividers set by ADCLRC_RATE and DACLRC_RATE. The BCLK frequency is derived from SYSCLK according to BCLK_DIV, as described earlier in Table 59. The definitions of ADCLRC_RATE and DACLRC_RATE are described in Table 61.

In Slave Mode, ADCLRC and DACLRC are generated externally and appear as an input to the CODEC.

See “Digital Audio Interface” for details of Master/Salve operation. See “Audio Interface Control” for further details of how ADCLRC and DACLRC are configured as input or output.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Audio Interface 3	10:0	ADCLRC_RATE [10:0]	040h	ADCLRC Frequency (Master Mode). BCLK is divided by this integer. ADCLRC_RATE is an 11-bit integer (LSB = 1). Valid range is 8 .. 2047
R9 (09h) Audio Interface 4	10:0	DACLRC_RATE [10:0]	040h	DACLRC Frequency (Master Mode). BCLK is divided by this integer. DACLRC_RATE is an 11-bit integer (LSB = 1). Valid range is 8 .. 2047

Table 61 ADCLRC / DACLRC Control

OPCLK CONTROL

When the ADCLRC/GPIO pin is configured as a GPIO, a clock derived from SYSCLK may be output on this pin to provide clocking for other parts of the system. The frequency of this signal is derived from SYSCLK and determined by OPCLK_DIV, as described in Table 62.

This output of this clock is dependent upon the ADCLRC_SRC register settings described under “General Purpose Input/Output”.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Clocking 1	14:12	OPCLK_DIV [2:0]	000	OPCLK Frequency (GPIO function) 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 5.5 101 = SYSCLK / 6 110 = Reserved 111 = Reserved

Table 62 OPCLK Control

SLOWCLK CONTROL

A slow clock derived from SYSCLK may be generated for de-bouncing of the headphone detect function or to set the timeout period for volume updates when zero-cross functions are used. This clock is enabled by TOCLK_ENA and its frequency is set by TOCLK_RATE, as described in Table 46 in the "Headphone Jack Detect" section.

FLL

The integrated FLL can be used to generate SYSCLK from a wide variety of different reference sources and frequencies. The FLL can uses MCLK as its reference, which may be a high frequency (e.g. 13 MHz) reference. The FLL is tolerant of jitter and may be used to generate a stable SYSCLK from a less stable input signal. The FLL characteristics are summarised in "Electrical Characteristics".

The analogue and digital portions of the FLL may be enabled independently via FLL_OSC_ENA and FLL_ENA. When initialising the FLL, the analogue circuit must be enabled first by setting FLL_OSC_ENA. The digital circuit may then be enabled on the next register write or later. When changing FLL settings, it is recommended that the digital circuit be disabled via FLL_ENA and then re-enabled after the other register settings have been updated. When changing the input reference frequency F_{REF}, it is recommended that the FLL be reset by setting FLL_ENA to 0. It is recommended that the analogue circuit should remain enabled throughout any change of FLL settings.

The FLL output frequency is directly determined from FLL_FRATIO, FLLCLK_DIV and the real number represented by FLL_N and FLL_K. The field FLL_N is an integer (LSB = 1); FLL_K is the fractional portion of the number (MSB = 0.5). The fractional portion is only valid when enabled by the field FLL_FRACN_ENA. De-selection of fractional mode results in lower power consumption.

The FLL frequency is determined according to the following equation:

$$F_{OUT} = (F_{VCO} / FLLCLK\_DIV)$$

$$F_{VCO} = F_{REF} \times (N + K) \times FLL\_FRATIO$$

F_{VCO} must be in the range 90-100 MHz. The value of FLLCLK_DIV should be selected as follows according to the desired output F_{OUT}.

OUTPUT FREQUENCY F_{OUT}	FLLCLK_DIV
2.8125 MHz - 3.125 MHz	4h (divide by 32)
5.625 MHz - 6.25 MHz	3h (divide by 16)
11.25 MHz - 12.5 MHz	2h (divide by 8)

Table 63 Choice of FLLCLK_DIV

Note that the output frequencies that do not lie within the ranges quoted above cannot be guaranteed across the full range of device operating temperatures.

When setting up the FLL, after the register write to enable the FLL (FLL_ENA = 1), the FLL output clock will be available after the FLL lock time has elapsed. The FLL lock time is the time from last CSB edge of the serial interface write to first clock edge of f_{OUT} from FLL. The FLL lock time is specified in Table 1. The FLL lock status can be monitored using a GPIO pin, see Table 49.

The register fields that control the FLL are described in Table 64. Example settings for a variety of reference frequencies and output frequencies are shown in Table 65.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Power Management 1	6	FLL_ENA	0	FLL Digital Enable 0 = Power down 1 = Power up FLL_OSC_ENA must be enabled before enabling FLL_ENA. The order is important.
R36 (24h) FLL Control 1	8	FLL_OSC_ENA	0	Analogue enable 0 = FLL disabled 1 = FLL enabled FLL_OSC_ENA must be enabled before enabling FLL_ENA. The order is important.
	4:0	FLL_FRATIO [4:0]	8h	CLK_VCO is divided by this integer, valid from 1 .. 31. Value 1 recommended for Reference clock > 96kHz Value 8 recommended for Reference clock < 96kHz
R37 (25h) FLL Control 2	8	FLL_FRACN_ENA	0	Fractional enable 0 = Integer Mode 1 = Fractional Mode
	7:0	FLL_K [15:8]	0h	Fractional multiply for CLK_REF (Most Significant Bits)
R38 (26h) FLL Control 3	7:0	FLL_K [7:0]	0h	Fractional multiply for CLK_REF (Least Significant Bits)
R39 (27h) FLL Control 4	4:0	FLL_N [9:5]	0Bh	Integer multiply for CLK_REF (Most Significant Bits)
R40 (28h) FLL Control 5	8:6	FLLCLK_DIV [2:0]	3h	F_{OUT} clock divider 000 = F_{VCO} / 2 001 = F_{VCO} / 4 010 = F_{VCO} / 8 (best performance) 011 = F_{VCO} / 16 100 = F_{VCO} / 32 101-111 = Reserved
	4:0	FLL_N [4:0]	17h	Integer multiply for CLK_REF (Least Significant Bits)
R41 (29h) FLL Control 6	8	FLL_SLOW_LOCK_REF	1	Low frequency reference locking 0 = Lock achieved after 509 ref clks (Recommended for Reference clock > 48kHz) 1 = Lock achieved after 49 ref clks (Recommended for Reference clock <= 48kHz)
	7	LRCLK_REF_ENA	0	FLL reference clock input selector 0 = MCLK 1 = DACLRC

Table 64 FLL Register Map

EXAMPLE FLL SETTINGS

Table 65 provides example FLL settings for generating common SYSCLK frequencies from a variety of reference inputs.

F_{REF}	F_{OUT}	F_{VCO}	FLL_N	FLL_K	FLL_F RATIO	FLLCLK _DIV	FRACN _ENA	FLL_SLOW _LOCK_REF
12.000 MHz	12.288 MHz	98.3040 MHz	8 (008h)	0.192 (3127h)	1	2h (divide by 8)	1	0
12.000 MHz	11.289597 MHz	90.3168 MHz	7 (007h)	0.526398 (86C2h)	1	2h (divide by 8)	1	0
12.288 MHz	11.2896 MHz	90.3168 MHz	7 (007h)	0.35 (599Ah)	1	2h (divide by 8)	1	0
13.000 MHz	12.287990 MHz	98.3040 MHz	7 (007h)	0.56184 (8FD5h)	1	2h (divide by 8)	1	0
13.000 MHz	11.289606 MHz	90.3168 MHz	6 (006h)	0.94745 (F28Ch)	1	2h (divide by 8)	1	0
19.200 MHz	12.287988 MHz	98.3040 MHz	5 (005h)	0.119995 (1EB8h)	1	2h (divide by 8)	1	0
19.200 MHz	11.289588 MHz	90.3168 MHz	4 (004h)	0.703995 (B439h)	1	2h (divide by 8)	1	0

Table 65 Example FLL Settings

CONTROL INTERFACE

The WM8900 is controlled by writing to registers through a serial control interface. The interface may be either a 2-wire or 3-wire configuration.

SELECTION OF CONTROL MODE

At power-up, the MODE pin determines which control mode is selected, as described in Table 66. An internal pull-up causes default selection of 3-wire mode.

MODE	INTERFACE FORMAT
Low	2 wire
High (default)	3 wire

Table 66 Control Interface Mode Selection

In 3-wire mode, the MODE pin can also be used as GPIO. To achieve this, the MODE_FN register bit must be set to 1. This causes the WM8900 to select 3-wire mode regardless of the MODE pin. Note that GPIO is not supported on the MODE pin in 2-wire mode and setting MODE_FN to 1 has no effect in 2-wire mode. Therefore, 3-wire mode must be initially selected as per Table 66 before writing to MODE_FN to select the GPIO function.

The MODE pull-up can be enabled / disabled by register bit MODE_PU_ENA. When using the MODE pin as a GPIO output, it may be desirable to disable the pull-up to reduce power consumption. The value of MODE_PU_ENA has no effect on Mode selection when 3-wire mode has been selected by setting MODE_FN to 1.

The register bits that determine the 2-wire or 3-wire mode selection are described in Table 67. See "General Purpose Input/Output" for more details on the use of the MODE pin as GPIO.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h) GPIO Control	12	MODE_PU_ENA	1	Enables the MODE Pull-Up resistor 0 = MODE Pull-Up disabled 1 = MODE Pull-Up enabled
	11	MODE_FN	0	Selects Interface Control Mode 0 = MODE pin selects 2-wire mode when low and 3-wire mode when high. 1 = Interface operates in 3-wire mode regardless of the MODE pin. MODE can be an input or output under the control of the GPIO control register.

Table 67 MODE Pin Function Control

3-WIRE CONTROL MODE

3-wire mode uses the CSB, SCLK and SDIN pins on the WM8900. In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB/GPIO latches in a complete control word consisting of the last 16 bits.

In 3-wire mode, the data comprises 24 bits in total. The first bit is the read/write (R/W) bit. This is followed by 7 address bits (A6 to A0), which identify the register to be accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in the WM8900 register.

The following timing diagram shows the supported read and write implementation in 3 wire mode.

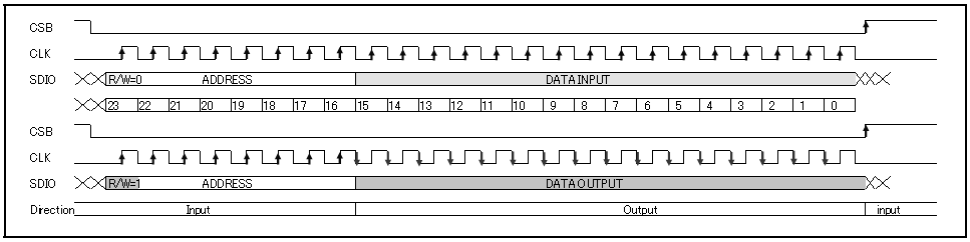


Figure 47 3-Wire Serial Control Timing

The same sequence applies to both Read and Write operations. The only difference is that the data bits are driven by the controlling device in Write mode, and by the WM8900 in Read mode. The R/W bit is set to 0 for Write operations and is set to 1 for Read operations. Register Read operations are only supported from a limited set of registers, as described in Table 68.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Reset	15:0	SW_RESET_ CHIP_ID		CHIP ID 16 data bits
R1 (01h) Power Management 1	15:12	CHIP_REV [3:0]		DEVICE_REVISON 4 data bits

Table 68 Readback Registers

2-WIRE SERIAL CONTROL MODE

The WM8900 supports software control via a 2-wire serial bus. 2-wire mode uses the SCLK and SDIN pins only. Many devices can be controlled by the same bus, and each device has a unique 7-bit device address (this is not the same as the 7-bit address of each register in the WM8900). To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8900 transmits logic 1 by tri-stating the SDIN pin, rather than by pulling it high. An external pull-up resistor is required to pull the SDIN line high so that the logic 1 can be recognised by the master.

The device address of the WM8900 can be one of two values and is determined by the CSB input pin when the device is powered up, as described in Table 69. An internal pull-down causes default selection of the device address. After CSB is sampled on power up, it reverts to a GPIO function and is not used in 2 wire mode.

CSB	DEVICE ADDRESS
Low (default)	0011010
High	0011011

Table 69 2-Wire Interface Device Address Selection

The WM8900 operates as a slave device only. The controller indicates the START of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the START condition and shift in the next eight bits on SDIN (7-bit address, MSB first + Read/Write bit = 0). Hence the first byte should equal 0x34 or 0x36. If the device address received matches the address of the WM8900 (configured by the CSB pin on power up), then the WM8900 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised, the WM8900 returns to the idle condition and waits for a new start condition and valid device address.

During a write, once the WM8900 has acknowledged a correct device address, the controller sends the WM8900 register address (MSB first). The WM8900 then acknowledges the register address byte by pulling SDIN low for one clock pulse. The controller then sends bits 15-8 of register data (MSB first), and the WM8900 acknowledges again by pulling SDIN low for one clock pulse. The controller then sends bits 7-0 of register data (MSB first), and the WM8900 acknowledges again by pulling SDIN low for one clock pulse.

Transfers are complete when there is a low to high transition on SDIN while SCLK is high (STOP). After a complete sequence the WM8900 returns to the idle state and waits for another start condition. If a START or STOP condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

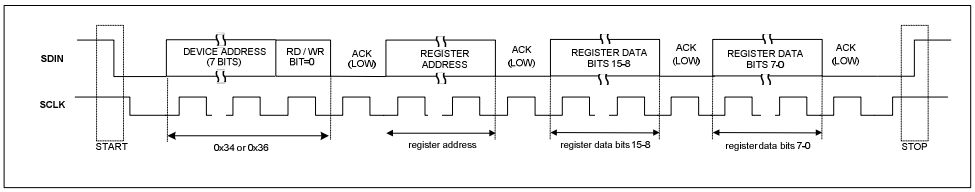


Figure 48 2-Wire Serial Control Interface Writes

In 2-wire mode, Auto-Incremental Write operations are supported. In this type of transfer, additional bytes of data (B15-B8 and B7-B0) are transmitted in sequence without the need to re-transmit the device address or register address. The WM8900 automatically increments the register address for each additional set of data bits received. This continues until the controlling device indicates the transfer is complete by a rising edge on SDIN while SCLK is held high. Auto-Incremental Writes are enabled by default; this can be set by the user as described in Table 70.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h) GPIO Control	15	AUTO_INC	1	Auto-Incremental write enable 0 = Auto-Incremental writes disabled 1 = Auto-Incremental writes enabled
	13	CSB_PD_ENA	1	Enables the CSB Pull-Down resistor 0 = CSB Pull-Down disabled 1 = CSB Pull-Down enabled

Table 70 2-Wire Interface Control

READBACK IN 2-WIRE MODE

Readback is supported from the registers listed in Table 68.

The controller indicates the START of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the START condition and shift in the next eight bits on SDIN (7-bit address, MSB first + Read/Write bit = 0). Hence the first byte should equal 0x34 or 0x36. If the device address received matches the address of the WM8900 (configured by the CSB pin on power up), then the WM8900 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised the WM8900 returns to the idle condition and waits for a new start condition and valid device address.

During a read, once the WM8900 has acknowledged a correct device address, the controller sends the WM8900 register address (MSB first). The WM8900 then acknowledges the register address byte by pulling SDIN low for one clock pulse. The controller then issues a repeated START with a high to low transition on SDIN while SCLK remains high. The controller then sends the WM8900 device read address (7-bit address, MSB first + Read/Write bit = 1). Hence this byte should equal 0x35 or 0x37. If the device address received matches the address of the WM8900 (configured by the CSB pin on power up), then the WM8900 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised the WM8900 returns to the idle condition and waits for a new start condition and valid device address.

During the next 9 SCLK cycles from the controller, WM8900 clocks out register data (bits 15-8, MSB first) on the first 8 cycles, and on the 9th cycle, the controller responds by pulling SDIN low. During the next 9 SCLK cycles from the controller, WM8900 clocks out register data (bits 7-0, MSB first) on the first 8 cycles, and on the 9th SCLK cycle, the controller responds by pulling SDIN low.

Transfers are complete when there is a low to high transition on SDIN while SCLK is high (STOP). After a complete sequence the WM8900 returns to the idle state and waits for another start condition. If a START or STOP condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

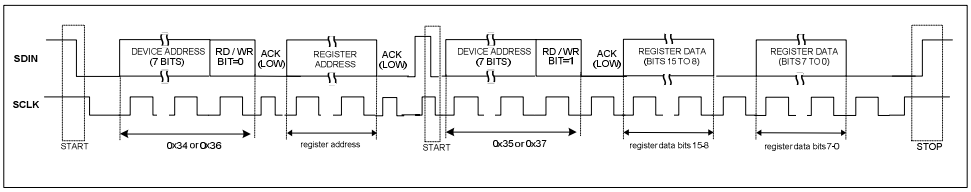


Figure 49 2-Wire Serial Control Interface Reads

RESETTING THE CHIP

The WM8900 can be reset by performing a write of any value to the software reset register (address 00h). This will cause all register values to be reset to their default values. In addition to this there is a Power-On Reset (POR) circuit which ensures that the registers are set to default when the device is powered up.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Reset	15:0	SW_RESET_ CHIP_ID		Read: CHIP ID (0x8900) Write: Software Reset

Table 71 Software Reset Register

POWER MANAGEMENT

The WM8900 has three control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled and bias currents set to the recommended values. To avoid any pop or click noise, it is important to enable or disable functions in the correct order (see "Applications Information"). VMID_MODE is the enable for the Vmid reference, which defaults to disabled and can be enabled as a 2x50kΩ potential divider or, for low power maintenance of Vref when all other blocks are disabled, as a 2x250kΩ potential divider.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Power Management 1	8	STARTUP_BIAS_ENA	0	Bias Startup control. Normally 0 but can be temporarily set to one during startup to minimise pops and clicks.
	6	FLL_ENA	0	FLL Digital Enable 0 = Power down 1 = Power up FLL_OSC_ENA must be enabled before enabling FLL_ENA. The order is important.
	4	MICB_ENA	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON
	3	BIAS_ENA	0	VREF (necessary for all analogue functions) 0 = Power down 1 = Power up
	2	VMID_BUF_ENA	0	Provides VMID to input and output analogue pins when not enabled. Normally 0 but can be temporarily set to one during startup to minimise pops and clicks.
	1:0	VMID_MODE [1:0]	00	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50kΩ divider (Normal mode) 10 = 2 x 250kΩ divider (Standby mode) 11 = 2 x 5kΩ divider (for fast start-up)
R2 (02h) Power Management 2	15	SYSCLK_ENA	0	Master Clock Disable 0 = Master clock disabled 1 = Master clock enabled
	8	OUT1L_ENA	0	Left LINEOUT1 Output Buffer 0 = Power down 1 = Power up

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7	OUT1R_ENA	0	Right LINEOUT1 Output Buffer 0 = Power down 1 = Power up
	5	MIXINL_ENA	0	Left channel input boost enable 0 = Boost disabled 1 = Boost enabled
	4	MIXINR_ENA	0	Right channel input boost enable 0 = Boost disabled 1 = Boost enabled
	3	INL_ENA	0	Left channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if MIXINL_ENA = 1)
	2	INR_ENA	0	Right channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if MIXINR_ENA = 1)
	1	ADCL_ENA	0	Enable ADC left channel: 0 = ADC disabled 1 = ADC enabled
	0	ADCR_ENA	0	Enable ADC right channel: 0 = ADC disabled 1 = ADC enabled
R3 (03h) Power Management 3	7	CP_ENA	0	Charge Pump Enable 0: Disable charge pump 1: Enable charge pump Must be enabled when the headphone output is used.
	6	OUT2L_ENA	0	Left LINEOUT2 Output Buffer 0 = Power down 1 = Power up
	5	OUT2R_ENA	0	Right LINEOUT2 Output Buffer 0 = Power down 1 = Power up
	3	MIXOUTL_ENA	0	Left output mixer enable 0 = Mixer disabled 1 = Mixer enabled
	2	MIXOUTR_ENA	0	Right output mixer enable 0 = Mixer disabled 1 = Mixer enabled
	1	DACL_ENA	0	Left DAC Enable 0 = DAC disabled 1 = DAC enabled
	0	DACR_ENA	0	Right DAC Enable 0 = DAC disabled 1 = DAC enabled

Table 72 Power Management

STOPPING THE MASTER CLOCK

In order to minimise power consumed in the digital core of the WM8900, the master clock may be stopped in Standby and OFF modes. If this cannot be done externally at the clock source, the SYSCLK_ENA bit (R2, bit 15) can be set to stop the MCLK signal from propagating into the device core. In Standby mode, setting SYSCLK_ENA will typically provide an additional power saving on DCVDD of 20uA. However, since setting SYSCLK_ENA has no effect on the power consumption of other system components external to the WM8900, it is preferable to disable the master clock at its source wherever possible. Figure 46 on page 76 shows the clock distribution within WM8900.

MCLK should not be stopped while the Headphone outputs are enabled, as this would prevent the charge pump from functioning**.**

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 2	15	SYSCLK_ENA	0	Master clock disable 0 = Master clock disabled 1 = Master clock enabled

Table 73 Stopping the Master Clock

Note:

Before SYSCLK_ENA can be set, the control bits ADCL_ENA, ADCR_ENA, DACL_ENA and DACR_ENA must be set to zero and a waiting time of 1ms must be observed. Any failure to follow this procedure may prevent DACs and ADCs from re-starting correctly.

REGISTER MAP

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R0 (0h)	RESET	SW_RESET_CHIP_ID[15:0]																8900h
R1 (1h)	PWR MGMT (1)	CHIP_REV[3:0]				0	0	0	STARTUP_BIAS_ENA	0	FLL_ENA	0	MICB_ENA	BIAS_ENA	VMID_BUF_ENA	VMID_MODE[1:0]		2000h
R2 (2h)	PWR MGMT (2)	SYSCLK_ENA	1	0	0	0	0	0	OUtT1L_ENA	OUT1R_ENA	0	MIXINL_ENA	MIXINR_ENA	INL_ENA	INR_ENA	ADCL_ENA	ADCR_ENA	C000h
R3 (3h)	PWR MGMT (3)	0	0	0	0	0	0	0	OUT1_FB_ENA	CP_ENA	OUT2L_ENA	OUT2R_ENA	0	MIXOUTL_ENA	MIXOUTR_ENA	DACL_ENA	DACR_ENA	0000h
R4 (4h)	AUDIO INTERFACE (1)	AIFADCL_SRC	AIFADCR_SRC	AIFADC_TDM	AIFADC_TDM_CHAN	0	0	0	AIF_BCLK_INV	AIF_LRCLK_INV	AIF_WL[1:0]		AIF_FMT[1:0]		0	0	0	4050h
R5 (5h)	AUDIO INTERFACE (2)	DACL_SRC	DACR_SRC	AIFDAC_TDM	AIFDAC_TDM_CHAN	DAC_BOOST[1:0]		0	0	0	ADCLRC_FN	0	DAC_COMP	DAC_COMPMODE	ADC_COMP	ADC_COMPMODE	LOOPBACK	4000h
R6 (6h)	CLOCKING (1)	0	OPCLK_DIV[2:0]			0	0	0	MCLK_SRC	0	0	0	BCLK_DIV[3:0]				BCLK_DIR	0008h
R7 (7h)	CLOCKING (2)	0	0	0	AIF_TRI	0	0	0	0	ADC_CLKDIV[2:0]			DAC_CLKDIV[2:0]			TOCLK_RATE	TOCLK_ENA	0000h
R8 (8h)	AUDIO INTERFACE (3)	0	0	0	0	ADCLRC_DIR	ADCLRC_RATE[10:0]											0040h
R9 (9h)	AUDIO INTERFACE (4)	0	0	0	0	DACLRC_DIR	DACLRC_RATE[10:0]											0040h
R10 (Ah)	DAC CTRL	0	0	0	DAC_SDMCLK_RATE	0	AIF_LRCLKRATE	DAC_MONO	DAC_SB_FILT	DAC_MUTERATE	DAC_MUTEMODE	DEEMP[1:0]		0	DAC_MUTE	DACL_DATINV	DACR_DATINV	1004h
R11 (Bh)	LEFT DAC DIGITAL VOLUME	0	0	0	0	0	0	0	DAC_VU	DACL_VOL[7:0]								00C0h
R12 (Ch)	RIGHT DAC DIGITAL VOLUME	0	0	0	0	0	0	0	DAC_VU	DACR_VOL[7:0]								00C0h
R13 (Dh)	DIGITAL SIDE TONE	0	0	0	ADCL_DAC_SVOL[3:0]				ADCR_DAC_SVOL[3:0]				0	ADC_TO_DACL[1:0]		ADC_TO_DACR[1:0]		0000h
R14 (Eh)	ADC CTRL	0	0	0	0	0	0	0	ADC_HPF_ENA	0	ADC_HPF_CUT[1:0]		0	0	0	ADCL_DATINV	ADCR_DATINV	0100h
R15 (Fh)	LEFT ADC DIGITAL VOLUME	0	0	0	0	0	0	0	ADC_VU	ADCL_VOL[7:0]								00C0h
R16 (10h)	RIGHT ADC DIGITAL VOLUME	0	0	0	0	0	0	0	ADC_VU	ADCR_VOL[7:0]								00C0h
R17 (11h)	JACK DETECT CTRL	0	0	JD_EN1[5:0]						0	0	JD_EN0[5:0]						0000h
R18 (12h)	GPIOCTRL	AUTO_INC	0	CSB_PD_ENA	MODE_PU_ENA	MODE_FN	0	JD_ENA	JD_MODE	ADCLRC_INV	ADCLRC_SRC[2:0]			JD_SRC[2:0]			TEMP_ENA	B001h
R21 (15h)	INPUT CTRL	0	0	0	0	0	0	0	MICB_LVL	0	IN1L_ENA	IN2L_ENA	IN3L_ENA	0	IN1R_ENA	IN2R_ENA	IN3R_ENA	0044h
R22 (16h)	LEFT INPUT VOLUME	0	0	0	0	0	0	0	IN_VU	INL_ZC	INL_MUTE	0	INL_VOL[4:0]					004Ch
R23 (17h)	RIGHT INPUT VOLUME	0	0	0	0	0	0	0	IN_VU	INR_ZC	INR_MUTE	0	INR_VOL[4:0]					004Ch
R24	INPUT BOOST	0	0	0	0	0	0	0	0	0	IN3L_BOOST[2:0]			0	IN2L_BOOST[2:0]			0044h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
(18h)	MIXER (1)																	
R25 (19h)	INPUT BOOST MIXER (2)	0	0	0	0	0	0	0	0	0	IN3R_BOOST[2:0]			0	IN2R_BOOST[2:0]			0044h
R26 (1Ah)	ADC SIGNAL PATH	0	0	0	0	0	0	0	0	0	INL_TO_MIXINL	INL_MIXINL_BOOST[1:0]		0	INR_TO_MIXINR	INR_MIXINR_BOOST[1:0]		0000h
R27 (1Bh)	AUX BOOST	0	0	0	0	0	0	0	0	0	IN4L_BOOST[2:0]			0	IN4R_BOOST[2:0]			0044h
R30 (1Eh)	ADDITIONAL CTRL	0	0	0	0	0	0	0	OUT1_DIS	OUT2_DIS	0	VMID_DISCH	BIAS_SRC	VMID_SOFTST	0	TEMP_SD	VROI	0002h
R36 (24h)	FLL 1	0	0	0	0	0	0	0	FLL_OSC_ENA	0	0	0	FLL_FRATIO[4:0]					0008h
R37 (25h)	FLL 2	0	0	0	0	0	0	0	FLL_FRACN_ENA	FLL_K[7:0]								0000h
R38 (26h)	FLL 3	0	0	0	0	0	0	0	0	FLL_K[7:0]								0000h
R39 (27h)	FLL 4	0	0	0	0	0	0	0	DF_GAIN[3:0]				FLL_N[4:0]					000Bh
R40 (28h)	FLL 5	0	0	0	0	0	0	0	FLL_CLKDIV[2:0]			0	FLL_N[4:0]					0097h
R41 (29h)	FLL 6	0	0	0	0	0	0	0	FLL_SLOW_LOCK_REF	LRCLK_REF_ENA	0	0	0	0	0	0	0	0100h
R44 (2Ch)	LEFT OUT MIXER CTRL (1)	0	0	0	0	0	0	0	DACL_TO_MIXOUTL	IN3L_TO_MIXOUTL	IN3L_MIXOUTL_VOL[2:0]			0	0	0	0	0050h
R45 (2Dh)	RIGHT OUT MIXER CTRL (1)	0	0	0	0	0	0	0	DACR_TO_MIXOUTR	IN3R_TO_MIXOUTR	IN3R_MIXOUTR_VOL[2:0]			0	0	0	0	0050h
R46 (2Eh)	BYPASS (1)	0	0	0	0	0	0	0	0	MIXINL_TO_MIXOUTL	MIXINL_MIXOUTL_VOL[2:0]			MIXINL_TO_MIXOUTR	MIXINL_MIXOUTR_VOL[2:0]			0055h
R47 (2Fh)	BYPASS (2)	0	0	0	0	0	0	0	0	MIXINR_TO_MIXOUTR	MIXINR_MIXOUTR_VOL[2:0]			MIXINR_TO_MIXOUTL	MIXINR_MIXOUTL_VOL[2:0]			0055h
R48 (30h)	AUX TO MIXER OUT CTRL	0	0	0	0	0	0	0	0	IN4_TO_MIXOUTL	IN4_MIXOUTL_VOL[2:0]			IN4_TO_MIXOUTR	IN4_MIXOUTR_VOL[2:0]			0055h
R51 (33h)	LEFT OUT1 CTRL	0	0	0	0	0	0	0	OUT1_VU	OUT1L_ZC	OUT1L_MUTE	OUT1L_VOL[5:0]						0079h
R52 (34h)	RIGHT OUT1 CTRL	0	0	0	0	0	0	0	OUT1_VU	OUT1R_ZC	OUT1R_MUTE	OUT1R_VOL[5:0]						0079h
R53 (35h)	LEFT OUT2 CTRL	0	0	0	0	0	0	0	OUT2_VU	OUT2L_ZC	OUT2L_MUTE	OUT2L_VOL[5:0]						0079h
R54 (36h)	RIGHT OUT2 CTRL	0	0	0	0	0	0	0	OUT2_VU	OUT2R_ZC	OUT2R_MUTE	OUT2R_VOL[5:0]						0079h
R58 (3Ah)	HEADPHONE CTRL 1	0	0	0	0	0	0	0	0	HP_IPSTAGE_ENA	HP_OPSTAGE_ENA	HP_CLAMP_IP	HP_CLAMP_OP	HP_SHORT	HP_SHORT2	HP_BIAS[1:0]		0000h
R115 (73h)	OUTPUT BIAS CTRL	0	0	0	0	0	0	0	MIXOUT_BIAS[1:0]		0	0	0	0	DAC_BIAS[1:0]		0	0000h
R116 (74h)	MASTER BIAS CTRL	0	0	0	0	0	0	0	MASTER_BIAS[1:0]		0	0	0	0	0	0	0	0100h

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Reset	15:0	SW_RESET_CHIP_ID		Read: CHIP ID (0x8900) Write: Software Reset
R1 (01h) Power Management 1	15:12	CHIP_REV [3:0]		DEVICE_REVISON 4 data bits
	8	STARTUP_BIAS_ENA	0	Bias Startup control. Normally 0 but can be temporarily set to one during startup to minimise pops and clicks.
	6	FLL_ENA	0	FLL Digital Enable 0 = Power down 1 = Power up FLL_OSC_ENA must be enabled before enabling FLL_ENA. The order is important.
	4	MICB_ENA	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON
	3	BIAS_ENA	0	VREF (necessary for all analogue functions) 0 = Power down 1 = Power up
	2	VMID_BUF_ENA	0	Provides VMID to input and output analogue pins when not enabled. Normally 0 but can be temporarily set to one during startup to minimise pops and clicks.
	1:0	VMID_MODE [1:0]	00	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50kΩ divider (Normal mode) 10 = 2 x 250kΩ divider (Standby mode) 11 = 2 x 5kΩ divider (for fast start-up)
R2 (02h) Power Management 2	15	SYSCLK_ENA	0	Master Clock Disable 0 = Master clock disabled 1 = Master clock enabled
	8	OUT1L_ENA	0	Left channel LINEOUT1 enable 0 = LINEOUT_1L disabled 1 = LINEOUT_1L enabled
	7	OUT1R_ENA	0	Right channel LINEOUT1 enable 0 = LINEOUT_1R disabled 1 = LINEOUT_1R enabled
	5	MIXINL_ENA	0	Left channel input boost enable 0 = Boost disabled 1 = Boost enabled
	4	MIXINR_ENA	0	Right channel input boost enable 0 = Boost disabled 1 = Boost enabled
	3	INL_ENA	0	Left channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if MIXINL_ENA = 1)
	2	INR_ENA	0	Right channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if MIXINR_ENA = 1)
	1	ADCL_ENA	0	Enable ADC left channel: 0 = ADC disabled 1 = ADC enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	ADCR_ENA	0	Enable ADC right channel: 0 = ADC disabled 1 = ADC enabled
R3 (03h) Power Management 3	8	OUT1_FB_ENA	0	Common mode feedback for Lineout1 0: Disable common mode feedback 1: Enable common mode feedback
	7	CP_ENA	0	Charge Pump Enable 0 = Disable charge pump 1 = Enable charge pump Must be enabled when the headphone output is used.
	6	OUT2L_ENA	0	Left channel LINEOUT2 enable 0 = LINEOUT_2L disabled 1 = LINEOUT_2L enabled
	5	OUT2R_ENA	0	Right channel LINEOUT2 enable 0 = LINEOUT_2R disabled 1 = LINEOUT_2R enabled
	3	MIXOUTL_ENA	0	Left output mixer enable 0 = Mixer disabled 1 = Mixer enabled
	2	MIXOUTR_ENA	0	Right output mixer enable 0 = Mixer disabled 1 = Mixer enabled
	1	DACL_ENA	0	Left DAC Enable 0 = DAC disabled 1 = DAC enabled
	0	DACR_ENA	0	Right DAC Enable 0 = DAC disabled 1 = DAC enabled
R4 (04h) Audio Interface 1	15	AIFADCL_SRC	0	Left Digital Audio channel source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel
	14	AIFADCR_SRC	1	Right Digital Audio channel source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
	13	AIFADC_TDM	0	ADC TDM Enable 0 = Normal ADCDAT operation 1 = TDM enabled on ADCDAT
	12	AIFADC_TDM_CHAN	0	ADCDAT TDM Channel Select 0 = ADCDAT outputs data on slot 0 1 = ADCDAT output data on slot 1
	8	AIF_BCLK_INV	0	BCLK Invert 0 = BCLK not inverted 1 = BCLK inverted
	7	AIF_LRCLK_INV	0	Right, left and I^2S modes – LRCLK polarity 0 = normal LRCLK polarity 1 = invert LRCLK polarity
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:5	AIF_WL [1:0]	10	Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits
	4:3	AIF_FMT [1:0]	10	Digital Audio Interface Format 00 = Right justified 01 = Left justified 10 = I^2S Format 11 = DSP Mode
R5 (05h) Audio Interface 2	15	DACL_SRC	0	Left DAC Data Source Select 0 = Left DAC outputs left channel data 1 = Left DAC outputs right channel data
	14	DACR_SRC	1	Right DAC Data Source Select 0 = Right DAC outputs left channel data 1 = Right DAC outputs right channel data
	13	AIFDAC_TDM	0	DAC TDM Enable 0 = Normal DACDAT operation 1 = TDM enabled on DACDAT
	12	AIFDAC_TDM_CHAN	0	DACDAT TDM Channel Select 0 = DACDAT data input on slot 0 1 = DACDAT data input on slot 1
	11:10	DAC_BOOST [1:0]	00	DAC Input Volume Boost 00 = 0dB 01 = +6dB (Input data must not exceed -6dBFS) 10 = +12dB (Input data must not exceed -12dBFS) 11 = +18dB (Input data must not exceed -18dBFS)
	6	ADCLRC_FN	0	ADCLRC/GPIO Pin Function Select 0 = ADCLRC frame clock for ADC 1 = GPIO pin
	4	DAC_COMP	0	DAC Companding enable 0 = off 1 = on
	3	DAC_COMPMODE	0	DAC Companding mode select: 0 = µ-law 1 = A-law
	2	ADC_COMP	0	ADC Companding enable 0 = off 1 = on
	1	ADC_COMPMODE	0	ADC Companding mode select: 0 = µ-law 1 = A-law
	0	LOOPBACK	0	Digital Loopback Function 0 = No loopback. 1 = Loopback enabled, ADC data output is fed directly into DAC data input.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Clocking 1	14:12	OPCLK_DIV [2:0]	000	OPCLK Frequency (GPIO function) 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 5.5 101 = SYSCLK / 6 110 = Reserved 111 = Reserved
	8	MCLK_SRC	0	Clock Source selection 0 = SYSCLK derived from MCLK 1 = SYSCLK derived from FLL output
	4:1	BCLK_DIV [3:0]	0000	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 = SYSCLK / 32 1110 = SYSCLK / 44 1111 = SYSCLK / 48
	0	BCLK_DIR	0	BCLK Direction 0 = BCLK is input 1 = BCLK is output
R7 (07h) Clocking 2	12	AIF_TRI	0	Tri-states ADCDAT and switches ADCLRC, DACLRC and BCLK to inputs. 0 = ADCDAT is an output; DACLRC and BCLK may be inputs or outputs; ADCLRC is input, output or GPIO. 1 = ADCDAT is tri-stated; DACLRC and BCLK are inputs; ADCLRC is input or GPIO.
	7:5	ADC_CLKDIV [2:0]	000	ADC Sample rate divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2 011 = SYSCLK / 3 100 = SYSCLK / 4 101 = SYSCLK / 5.5 110 = SYSCLK / 6 111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4:2	DAC_CLKDIV [2:0]	000	DAC Sample rate divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2 011 = SYSCLK / 3 100 = SYSCLK / 4 101 = SYSCLK / 5.5 110 = SYSCLK / 6 111 = Reserved
	1	TOCLK_RATE	0	Slow Clock Selection (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)
	0	TOCLK_ENA	0	Slow Clock Enable (Must be enabled for jack detect de-bounce) 0 = Slow Clock Disabled 1 = Slow Clock Enabled
R8 (08h) Audio Interface 3	11	ADCLRC_DIR	0	ADCLRC Direction 0 = ADCLRC is input 1 = ADCLRC is output
	10:0	ADCLRC_RATE [10:0]	040h	ADCLRC Frequency (Master Mode). BCLK is divided by this integer. ADCLRC_RATE is an 11-bit integer (LSB = 1). Valid range is 8 .. 2047
R9 (09h) Audio Interface 4	11	DACLRC_DIR	0	DACLRC Direction 0 = DACLRC is input 1 = DACLRC is output
	10:0	DACLRC_RATE [10:0]	040h	DACLRC Frequency (Master Mode). BCLK is divided by this integer. DACLRC_RATE is an 11-bit integer (LSB = 1). Valid range is 8 .. 2047
R10 (0Ah) DAC Control	12	DAC_SDMCLK_RATE	1	DAC sigma delta modulator clock 0 = DAC clock scales with sample rate 1 = DAC clock independent of sample rate
	10	AIF_LRCLKRATE	0	Mode Select 1 = USB mode (272 * Fs) 0 = Normal mode (256 * Fs)
	9	DAC_MONO	0	DAC Mono Mix 0 = Stereo 1 = Mono (Mono mix output on enabled DACs)
	8	DAC_SB_FILT	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband mode
	7	DAC_MUTERATE	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6	DAC_MUTEMODE	0	DAC Soft Mute and Un-mute Mode 0 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to change immediately to DACL_VOL and DACR_VOL settings or change to digital mute level immediately 1 = Enabling soft-mute (DAC_MUTE=0) will cause the DAC volume to ramp up gradually to the DACL_VOL and DACR_VOL settings or gradually ramp down to digital mute level
	5:4	DEEMP [1:0]	00	De-Emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No de-emphasis
	2	DAC_MUTE	1	DAC Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute
	1	DACL_DATINV	0	Left DAC Invert 0 = Left DAC output not inverted 1 = Left DAC output inverted
	0	DACR_DATINV	0	Right DAC Invert 0 = Right DAC output not inverted 1 = Right DAC output inverted
R11 (0Bh) Left DAC Digital Volume	8	DAC_VU	0	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously
	7:0	DACL_VOL [7:0]	11000000 (0dB)	Left DAC Digital Volume (See Table 29 for volume range)
R12 (0Ch) Right DAC Digital Volume	8	DAC_VU	0	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously
	7:0	DACR_VOL [7:0]	11000000 (0dB)	Right DAC Digital Volume (See Table 29 for volume range)
R13 (0Dh) Digital Sidetone	12:9	ADCL_DAC_SVOL [3:0]	0000	Left Digital Sidetone Volume (See Table 26 for volume range)
	8:5	ADCR_DAC_SVOL [3:0]	0000	Right Digital Sidetone Volume (See Table 26 for volume range)
	3:2	ADC_TO_DACL [1:0]	00	Left DAC Digital Sidetone Source 00 = No sidetone 01 = Left ADC 10 = Right ADC 11 = Reserved
	1:0	ADC_TO_DACR [1:0]	00	Right DAC Digital Sidetone Source 00 = No sidetone 01 = Left ADC 10 = Right ADC 11 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 (0Eh) ADC Control	8	ADC_HPF_ENA	1	ADC Digital High Pass Filter Enable 0 = disabled 1 = enabled
	6:5	ADC_HPF_CUT [1:0]	00	ADC Digital High Pass Filter Cut-Off Frequency (fc) 00 = Hi-fi mode (fc=4Hz at fs=48kHz) 01 = Voice mode 1 (fc=127Hz at fs=16kHz) 10 = Voice mode 2 (fc=130Hz at fs=8kHz) 11 = Voice mode 3 (fc=267Hz at fs=8kHz) (Note: fc scales with sample rate. See Table 21 for cut-off frequencies at all supported sample rates.)
	1	ADCL_DATINV	0	Left ADC Invert 0 = Left ADC output not inverted 1 = Left ADC output inverted
	0	ADCR_DATINV	0	Right ADC Invert 0 = Right ADC output not inverted 1 = Right ADC output inverted
R15 (0Fh) Left ADC Digital Volume	8	ADC_VU	0	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCL_VOL [7:0]	1100 0000 (0dB)	Left ADC Digital Volume (See Table 19 for volume range)
R16 (10h) Right ADC Digital Volume	8	ADC_VU	0	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCR_VOL [7:0]	1100 0000 (0dB)	Right ADC Digital Volume (See Table 19 for volume range)
R17 (11h) Jack Detect Control	13:8	JD_EN1[5:0]	000000	Output enables when selected jack detection input is logic 1 JD_EN1[0] =1 enables LINEOUT_1L JD_EN1[1] =1 enables LINEOUT_1R JD_EN1[2] =1 enables LINEOUT_2R JD_EN1[3] =1 enables LINEOUT_2R JD_EN1[4] =1 enables Headphone JD_EN1[5] =1 enables Charge Pump
	5:0	JD_EN0[5:0]	000000	Output enables when selected jack detection input is logic 0 JD_EN0[0] =1 enables LINEOUT_1L JD_EN0[1] =1 enables LINEOUT_1R JD_EN0[2] =1 enables LINEOUT_2R JD_EN0[3] =1 enables LINEOUT_2R JD_EN0[4] =1 enables Headphone JD_EN0[5] =1 enables Charge Pump
R18 (12h) GPIO Control	15	AUTO_INC	1	Auto-Incremental write enable 0 = Auto-Incremental writes disabled 1 = Auto-Incremental writes enabled
	13	CSB_PD_ENA	1	Enables the CSB Pull-Down resistor 0 = CSB Pull-Down disabled 1 = CSB Pull-Down enabled
	12	MODE_PU_ENA	1	Enables the MODE Pull-Up resistor 0 = MODE Pull-Up disabled 1 = MODE Pull-Up enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	11	MODE_FN	0	Selects Interface Control Mode 0 = MODE pin selects 2-wire mode when low and 3-wire mode when high. 1 = Interface operates in 3-wire mode regardless of the MODE pin. MODE can be an input or output under the control of the GPIO control register.
	9	JD_ENA	0	Jack Detect Switch Enable 0 = Jack Detect disabled 1 = Jack Detect enabled
	8	JD_MODE	0	Jack Detect Switch Polarity 0 = Jack Detect active high 1 = Jack Detect active low
	7	ADCLRC_INV	0	GPIO Output Polarity Invert 0 = Non inverted 1 = Inverted
	6:4	ADCLRC_SRC [2:0]	000	GPIO Pin Function Select: 000 = Jack detect input 001 = Reserved 010 = Temperature ok 011 = Debounced jack detect output 100 = SYSCLK output 101 = FLL lock 110 = Logic 0 111 = Logic 1
	3:1	JD_SRC[2:0]	000	Jack Detect Input Select 000 = ADCLRC/GPIO used for jack detect 001 = CSB/GPIO used for jack detect 010 = LINPUT3/JD used for jack detect 011 = RINPUT3/JD used for jack detect 100 = MODE/GPIO used for jack detect 101 to 111 Reserved
	0	TEMP_ENA	1	Temperature Sensor Enable 0 = Temperature sensor disabled 1 = Temperature sensor enabled
R21 (15h) Input Control	8	MICB_LVL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD
	6	IN1L_ENA	1	Connect LINPUT1 to inverting input of Left Input PGA 0 = LINPUT1 not connected to PGA 1 = LINPUT1 connected to PGA
	5	IN2L_ENA	0	Connect LINPUT2 to non-inverting input of Left Input PGA 0 = LINPUT2 not connected to PGA 1 = LINPUT2 connected to PGA
	4	IN3L_ENA	0	Connect LINPUT3 to non-inverting input of Left Input PGA 0 = LINPUT3 not connected to PGA 1 = LINPUT3 connected to PGA
	2	IN1R_ENA	1	Connect RINPUT1 to inverting input of Right Input PGA 0 = RINPUT1 not connected to PGA 1 = RINPUT1 connected to PGA

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	IN2R_ENA	0	Connect RINPUT2 to non-inverting input of Right Input PGA 0 = RINPUT2 not connected to PGA 1 = RINPUT2 connected to PGA
	0	IN3R_ENA	0	Connect RINPUT3 to non-inverting input of Right Input PGA 0 = RINPUT3 not connected to PGA 1 = RINPUT3 connected to PGA
R22 (16h) Left Input Volume	8	IN_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause left and right Input PGA volume to be updated simultaneously
	7	INL_ZC	0	Left Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	6	INL_MUTE	1	Left Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IN_VU must be set to un-mute.
	4:0	INL_VOL [4:0]	01100 (0dB)	Left Input PGA Volume Control 11111 = +19dB 11110 = +18dB . . 1dB steps down to 00000 = -12dB
R23 (17h) Right Input Volume	8	IN_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause left and right Input PGA volume to be updated simultaneously
	7	INR_ZC	0	Right Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	6	INR_MUTE	1	Right Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IN_VU must be set to un-mute.
	4:0	INR_VOL [4:0]	01100 (0dB)	Right Input PGA Volume Control 11111 = +19dB 11110 = +18dB . . 1dB steps down to 00000 = -12dB
R24 (18h) Input Boost Mixer 1	6:4	IN3L_BOOST [2:0]	100	LINPUT3 to Boost Gain 000 = -12dB ...6dB steps up to 011 = +6dB 1XX = Mute
	2:0	IN2L_BOOST [2:0]	100	LINPUT2 to Boost Gain 000 = -12dB ...6dB steps up to 011 = +6dB 1XX = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Input Boost Mixer 2	6:4	IN3R_BOOST [2:0]	100	RINPUT3 to Boost Gain 000 = -12dB …6dB steps up to 011 = +6dB 1XX = Mute
	2:0	IN2R_BOOST [2:0]	100	RINPUT2 to Boost Gain 000 = -12dB …6dB steps up to 011 = +6dB 1XX = Mute
R26 (1Ah) ADC Signal Path	6	INL_TO_MIXINL	0	Connect Left Input PGA to Left Input Boost mixer 0 = Not connected 1 = Connected
	5:4	INL_MIXINL_BOOST [1:0]	00	Left Channel PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB
	2	INR_TO_MIXINR	0	Connect Right Input PGA to Right Input Boost mixer 0 = Not connected 1 = Connected
	1:0	INR_MIXINR_BOOST [1:0]	00	Right Channel PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB
R27 (1Bh) Aux Boost	6:4	IN4L_BOOST [2:0]	100	AUX input to Boost Gain 000 = -12dB ...6dB steps up to 011 = +6dB 1XX = Mute
	2:0	IN4R_BOOST [2:0]	100	AUX input to Boost Gain 000 = -12dB ...6dB steps up to 011 = +6dB 1XX = Mute
R30 (1Eh) Additional Control	8	OUT1_DIS	0	1 = Clamps LINEOUT_1L and LINEOUT_1R to GND via 8K resistance 0 = 8k resistance not connected to GND
	7	OUT2_DIS	0	1 = Clamps LINEOUT_2L and LINEOUT_2R to GND via 8K resistance 0 = 8k resistance not connected to GND
	5	VMID_DISCH	0	Enables fast discharge of Vmid to GND
	4	BIAS_SRC	0	Vmid bias select. Normally 0 but can be temporarily set to one during startup to select the soft-start Vmid source.
	3	VMID_SOFTST	0	Vmid soft-start control. Normally 0 but can be temporarily set to one during startup to ramp Vmid in a controlled manner.
	1	TEMP_SD	1	Thermal Shutdown Enable 0 = Thermal shutdown disabled 1 = Thermal shutdown enabled (TEMP_ENA must be enabled for this function to work)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	VROI	0	VREF to Analogue Output Resistance (Disabled Outputs) 0 = 500Ω from buffered VMID to output 1 = 20kΩ from buffered VMID to output
R36 (24h) FLL Control 1	8	FLL_OSC_ENA	0	Analogue enable 0 = FLL disabled 1 = FLL enabled FLL_OSC_ENA must be enabled before enabling FLL_ENA. The order is important.
	4:0	FLL_FRATIO [4:0]	8h	CLK_VCO is divided by this integer, valid from 1 .. 31. Value 1 recommended for Reference clock > 96kHz Value 8 recommended for Reference clock < 96kHz
R37 (25h) FLL Control 2	8	FLL_FRACN_ENA	0	Fractional enable 0 = Integer Mode 1 = Fractional Mode (Fractional N mode increases digital power consumption of the FLL)
	7:0	FLL_K [15:8]	0h	Fractional multiply for CLK_REF (Most Significant Bits)
R38 (26h) FLL Control 3	7:0	FLL_K [7:0]	0h	Fractional multiply for CLK_REF (Least Significant Bits)
R39 (27h) FLL Control 4	4:0	FLL_N [9:5]	0Bh	Integer multiply for CLK_REF (Most Significant Bits)
R40 (28h) FLL Control 5	8:6	FLLCLK_DIV [2:0]	3h	F_{OUT} clock divider 000 = F_{VCO} / 2 001 = F_{VCO} / 4 010 = F_{VCO} / 8 (best performance) 011 = F_{VCO} / 16 100 = F_{VCO} / 32 101 = Reserved 110 = Reserved 111 = Reserved
	4:0	FLL_N [4:0]	17h	Integer multiply for CLK_REF (Least Significant Bits)
R41 (29h) FLL Control 6	8	FLL_SLOW_LOCK_REF	1	Low frequency reference locking 0 = Lock achieved after 509 ref clks (Recommended for Reference clock > 48kHz) 1 = Lock achieved after 49 ref clks (Recommended for Reference clock <= 48kHz)
	7	LRCLK_REF_ENA	0	FLL reference clock input selector 0 = MCLK 1 = DACLRC
R44 (2Ch) Left Output Mixer Control 1	8	DACL_TO_MIXOUTL	0	Left DAC output to left output mixer 0 = not selected 1 = selected
	7	IN3L_TO_MIXOUTL	0	Left input 3 channel to left output mixer path 0 = not selected 1 = selected

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:4	IN3L_MIXOUTL_VOL	101	Left input 3 channel to left output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
	1	DAC_LP	0	DAC Low power control: 0 = DAC low power path disabled 1 = DAC low power path enabled
	0	DAC_LP_VOL	0	DAC Low power volume control: 0 = 0dB 1 = -12dB
R45 (2Dh) Right Output Mixer Control 1	8	DACR_TO_MIXOUTR	0	Right DAC output to right output mixer 0 = not selected 1 = selected
	7	IN3R_TO_MIXOUTR	0	Right input 3 channel to right output mixer path 0 = not selected 1 = selected
	6:4	IN3R_MIXOUTR_VOL	101	Right input 3 channel to right output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
R46 (2Eh) Bypass 1	7	MIXINL_TO_MIXOUTL	0	Left bypass path (from the Left channel ADC input) to left output mixer 0 = not selected 1 = selected
	6:4	MIXINL_MIXOUTL_VOL	101	Left bypass path to left output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
	3	MIXINL_TO_MIXOUTR	0	Left bypass path (from the Left channel ADC input) to right output mixer 0 = not selected 1 = selected
	2:0	MIXINL_MIXOUTR_VOL	101	Left bypass path to right output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
R47 (2Fh) Bypass 2	7	MIXINR_TO_MIXOUTR	0	Right bypass path (from the Right channel ADC input) to right output mixer 0 = not selected 1 = selected
	6:4	MIXINR_MIXOUTR_VOL	101	Right bypass path to right output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	MIXINR_TO_MIXOUTL	0	Right bypass path (from the Right channel ADC input) to left output mixer 0 = not selected 1 = selected
	2:0	MIXINR_MIXOUTL_VOL	101	Right bypass path to left output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
R48 (30h) AUX to Mixer Output Control	7	IN4_TO_MIXOUTL	0	AUX input channel to left output mixer path 0 = not selected 1 = selected
	6:4	IN4_MIXOUTL_VOL	101	AUX input channel to left output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
	3	IN4_TO_MIXOUTR	0	AUX input channel to right output mixer path 0 = not selected 1 = selected
	2:0	IN4_MIXOUTR_VOL	101	AUX input channel to right output mixer path volume control (-15dB -> +6dB in 3dB steps) 000 = -15dB 101 = 0dB 111 = +6dB
R51 (33h) Left OUT1 Control	8	OUT1_VU	0	Left Channel LINEOUT1 Volume Update Writing a 1 to this bit will cause left and right LINEOUT1 volume to be updated simultaneously
	7	OUT1L_ZC	0	Left Channel LINEOUT1 Zero Cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6	OUT1L_MUTE	1	Left Channel LINEOUT1 Mute 0 = LINEOUT_1L Unmuted 1 = LINEOUT_1L Mute
	5:0	OUT1L_VOL [5:0]	111001	Left Channel LINEOUT1 Volume Control (-57dB -> +6dB in 1dB steps) 111111 = +6dB 000000 = -57dB
R52 (34h) Right OUT1 Control	8	OUT1_VU	0	Left Channel LINEOUT1 Volume Update Writing a 1 to this bit will cause left and right LINEOUT1 volume to be updated simultaneously
	7	OUT1L_ZC	0	Left Channel LINEOUT1 Zero Cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6	OUT1L_MUTE	1	Left Channel LINEOUT1 Mute 0 = LINEOUT_1L Unmuted 1 = LINEOUT_1L Mute
	5:0	OUT1L_VOL [5:0]	111001	Left Channel LINEOUT1 Volume Control (-57dB -> +6dB in 1dB steps) 111111 = +6dB 000000 = -57dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R53 (35h) Left OUT2 Control	8	OUT2_VU	0	Left Channel LINEOUT2 Volume Update Writing a 1 to this bit will cause left and right LINEOUT2 volume to be updated simultaneously
	7	OUT2L_ZC	0	Left Channel LINEOUT2 Zero Cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6	OUT2L_MUTE	1	Left Channel LINEOUT2 Mute 0 = LINEOUT_1L Unmuted 1 = LINEOUT_1L Mute
	5:0	OUT2L_VOL [5:0]	111001	Left Channel LINEOUT2 Volume Control (-57dB -> +6dB in 1dB steps) 111111 = +6dB 000000 = -57dB
R54 (36h) Right OUT2 Control	8	OUT2_VU	0	Right Channel LINEOUT2 Volume Update Writing a 1 to this bit will cause left and right LINEOUT2 volume to be updated simultaneously
	7	OUT2R_ZC	0	Right Channel LINEOUT2 Zero Cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6	OUT2R_MUTE	1	Right Channel LINEOUT2 Mute 0 = LINEOUT_1R Unmuted 1 = LINEOUT_1R Mute
	5:0	OUT2R_VOL [5:0]	111001	Right Channel LINEOUT2 Volume Control (-57dB -> +6dB in 1dB steps) 111111 = +6dB 000000 = -57dB
R58 (3Ah) Headphone Control 1	7	HP_IPSTAGE_ENA	0	Headphone input stage Enable 0 = Headphone input stage disabled 1 = Headphone input stage enabled
	6	HP_OPSTAGE_ENA	0	Headphone output stage Enable 0 = Headphone output stage disabled 1 = Headphone output stage enabled
	5	HP_CLAMP_IP	0	Clamps HP_INL and HP_INR to GND
	4	HP_CLAMP_OP	0	Clamps HP_L and HP_R outputs to GND
	3	HP_SHORT	0	Shorts the inputs to the outputs
	2	HP_SHORT2	0	Shorts the feedback resistor. 0 = Normal operation 1 = Shorts feedback resistor. About 20dB 'mute' attenuation
R115 (R73h) Output Bias Control	8:7	MIXOUT_BIAS	00	Adjusts output mixer bias 00 = Full bias 01 = Half bias (recommended) 10 = Reserved 11 = Reserved
	2:1	DAC_BIAS	00	Adjusts DAC bias 00 = Full bias 01 = Half bias (recommended) 10 = Reserved 11 = Reserved
R116 (R74h) Master Bias Control	8:7	MASTER_BIAS	10	Adjusts master bias 00 = Reserved 01 = 0.75 bias 10 = full bias - default 11 = Reserved

Table 74 Register Map Summary

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.05dB	0		0.454fs	
	-3dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.546s			
Stopband Attenuation	f > 0.546fs	-60			dB
DAC Normal Filter					
Passband	+/- 0.03dB	0		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.454 fs			+/- 0.03	dB
Stopband		0.546 fs			
Stopband Attenuation	F > 0.546 fs	-50			dB
DAC Sloping Stopband Filter					
Passband	+/- 0.03dB	0		0.25 fs	
	+/- 1dB	0.25 fs		0.454 fs	
	-3dB		0.5 fs		
Passband Ripple	0.25 fs			+/- 0.03	dB
Stopband 1		0.546 fs		0.7 fs	
Stopband 1 Attenuation	f > 0.546 fs	-60			dB
Stopband 2		0.7 fs		1.4 fs	
Stopband 2 Attenuation	f > 0.7 fs	-85			dB
Stopband 3		1.4 fs			
Stopband 3 Attenuation	F > 1.4 fs	-55			dB

DAC FILTERS		ADC FILTERS	
Mode	**Group Delay**	**Mode**	**Group Delay**
Normal	18 / fs	Normal	18 / fs
Sloping Stopband	18 / fs		

ADC FILTER RESPONSES

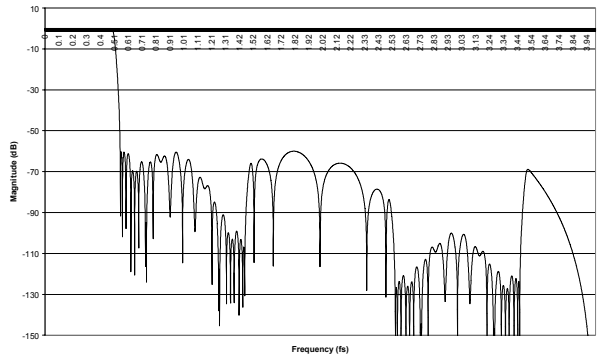


Figure 50 ADC Digital Filter Frequency Response

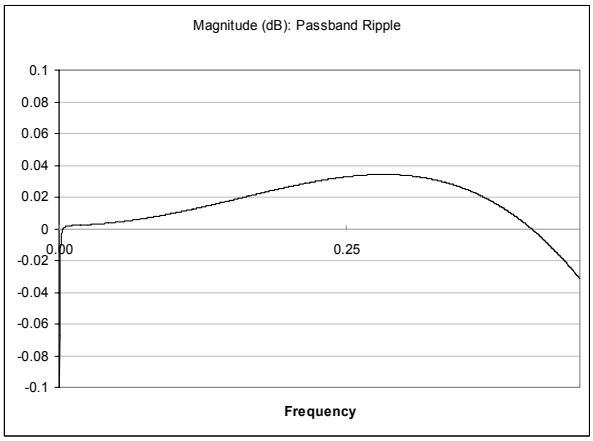


Figure 51 ADC Digital Filter Ripple

DAC FILTER RESPONSES

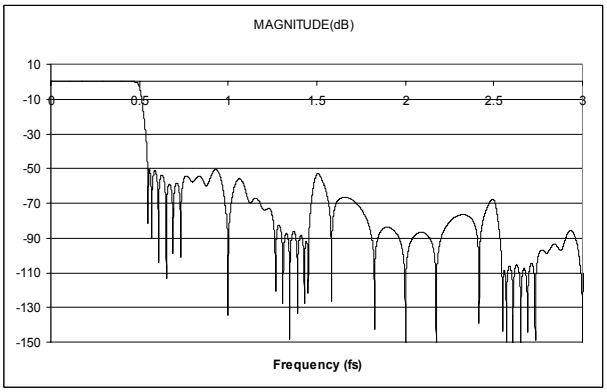


Figure 52 DAC Digital Filter Frequency Response (Normal Mode)

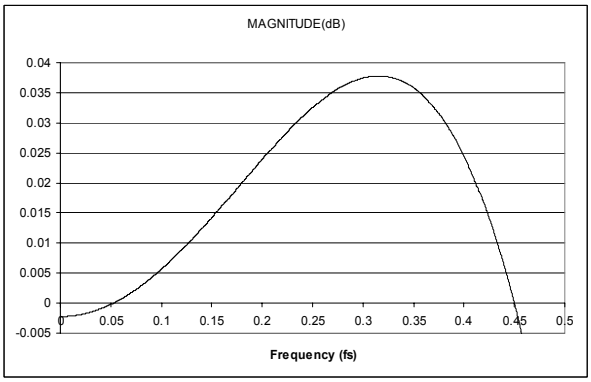


Figure 53 DAC Digital Filter Ripple (Normal Mode)

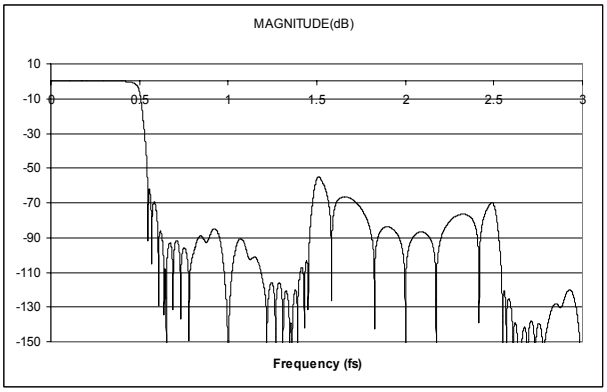


Figure 54 DAC Digital Filter Frequency Response (Sloping Stopband Mode)

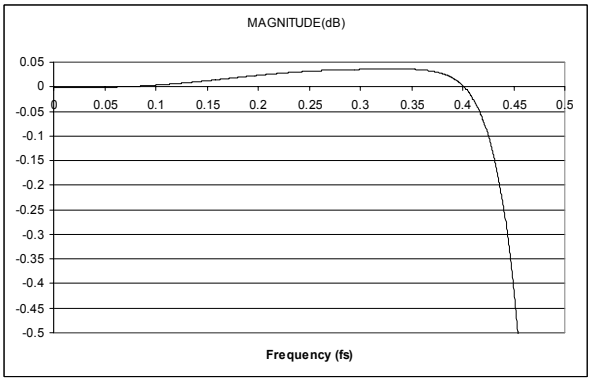


Figure 55 DAC Digital Filter Ripple (Sloping Stopband Mode)

DE-EMPHASIS FILTER RESPONSES

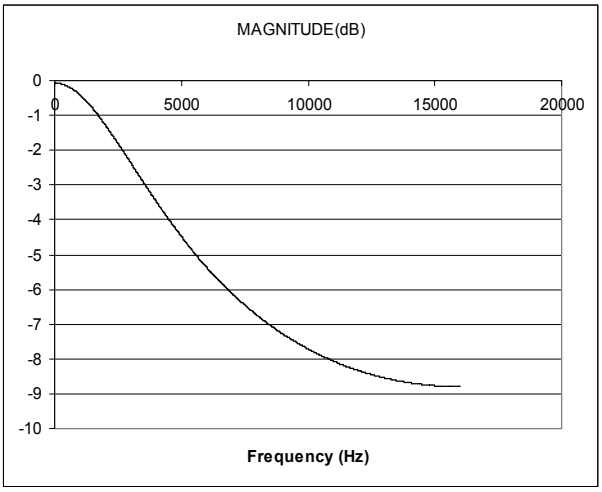


Figure 56 De-Emhpasis Digital Filter Response (32kHz)

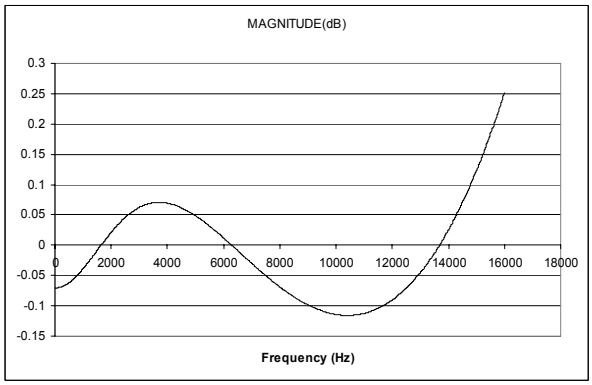


Figure 57 De-Emphasis Error (32kHz)

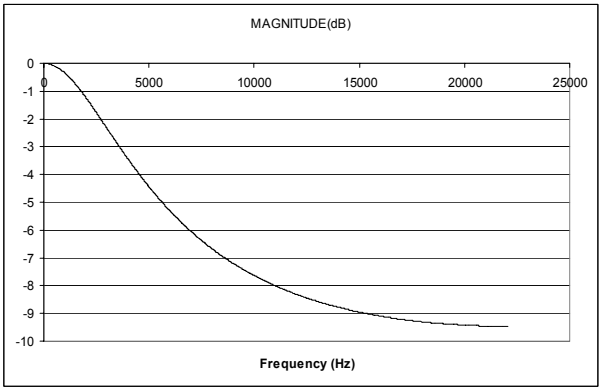


Figure 58 De-Emhpasis Digital Filter Response (44.1kHz)

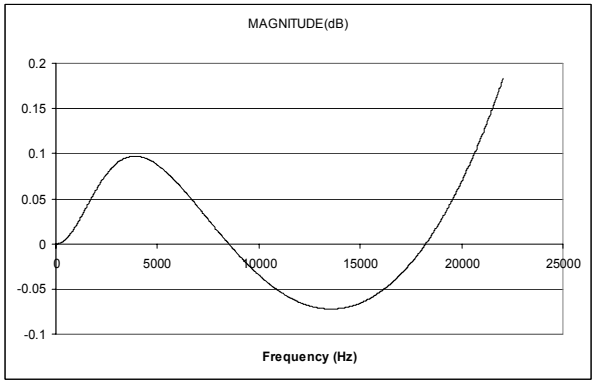


Figure 59 De-Emphasis Error (44.1kHz)

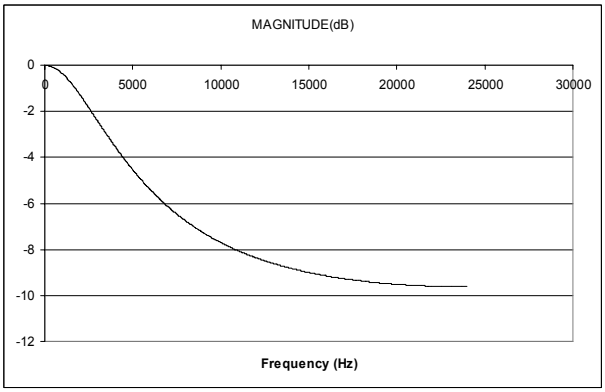


Figure 60 De-Emhpasis Digital Filter Response (48kHz)

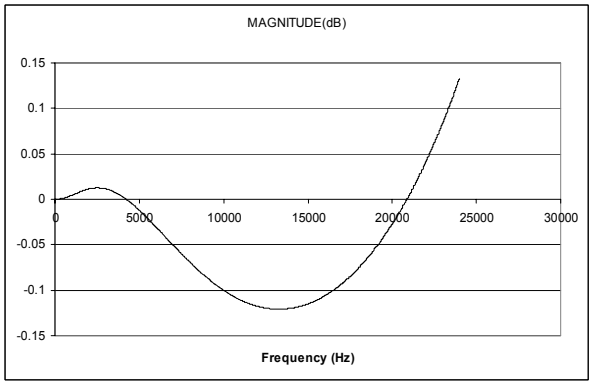
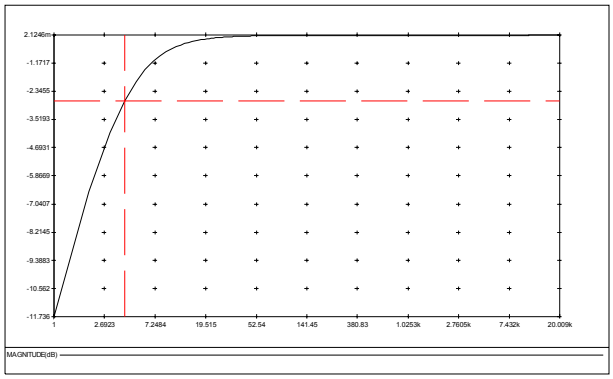
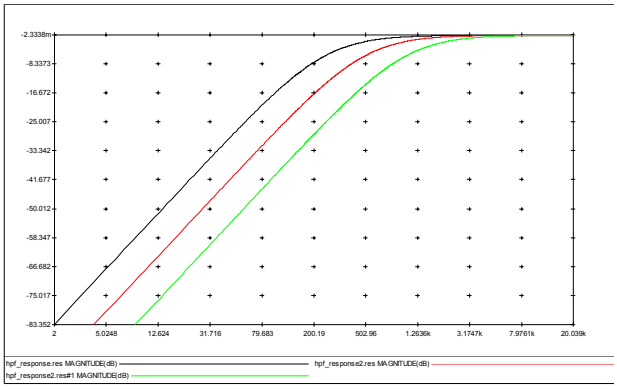


Figure 61 De-Emphasis Error (48kHz)

ADC HIGH PASS FILTER RESPONSES



ADC Digital High Pass Filter Frequency Response (48kHz, Hi-Fi Mode, ADC_HPF_CUT[1:0]=00)



ADC Digital High Pass Filter Ripple.

Fs = 48kHz.

ADC_HPF_CUT= 01 [voice mode 1] - black,

ADC_HPF_CUT= 10 [Voice mode 2] - red

ADC_HPF_CUT= 11 [Voice mode 3] - green

Figure 62 ADD High Pass Filter Characteristics

APPLICATIONS INFORMATION

RECOMMENDED PATHS

STEREO DAC TO HEADPHONE

The following section details the configuration for stereo DAC to headphone output with charge pump enabled. Slave mode, 24-bit I2S digital audio interface.

Block Diagram:

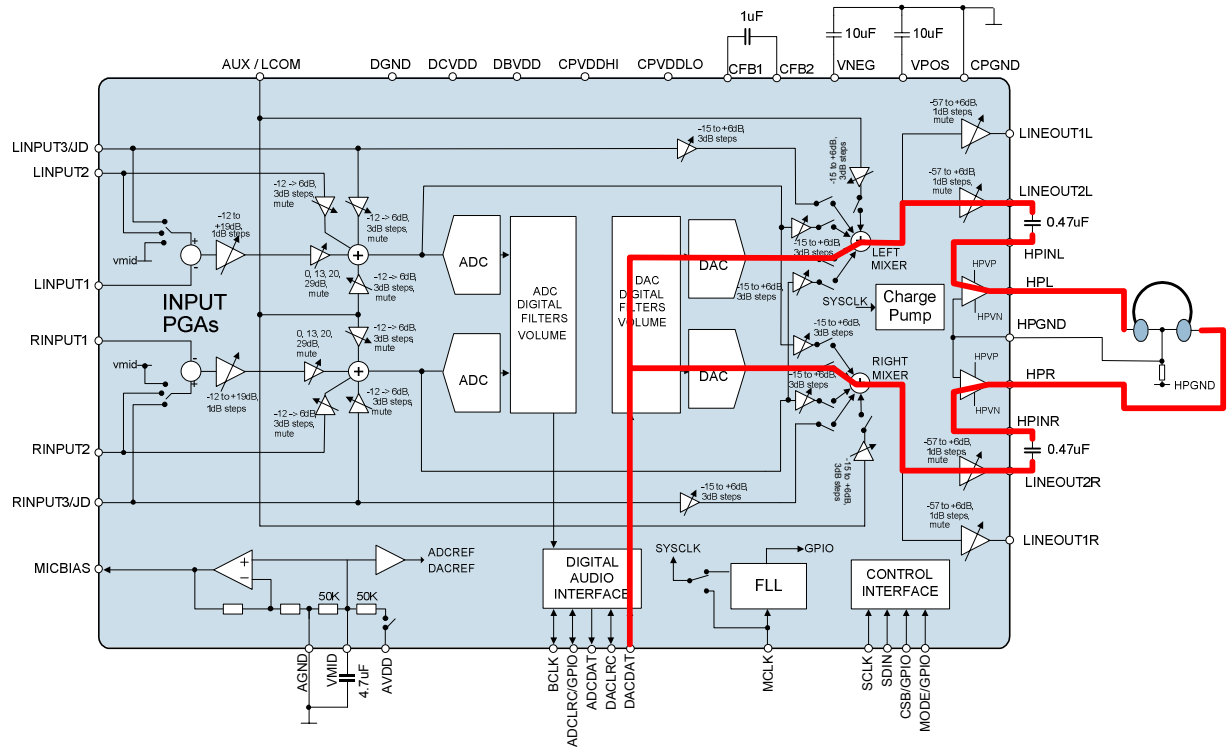


Figure 63 Stereo DAC to Headphone Device Internal Signal Path

Register Settings:

REG INDEX	DATA VALUE	READ OR WRITE	COMMENT
0x3A	0x0030	Write	Set CLAMP_IP=1, CLAMP_OP=1 (HP amp)
0x1E	0x0082	Write	Set OUT2_DIS=1 (Enable), OUT1_DIS=0 (Disable)
0x01	0x0100	Write	Set STARTUP_BIAS_ENA=1
0x1E	0x009A	Write	Set BIAS_SRC=1, VMID_SOFTST=1
0x03	0x0060	Write	Set OUT2L_ENA=1, OUT2R_ENA=1
0x1E	0x001A	Write	Reset OUT2_DIS=0, Leave BIAS_SRC=1, VMID_SOFTST=1
0x01	0x0101	Write	Set VMID_MODE=01 (2x50K Ohm Divider)
	400ms Delay		Delay (400ms) to allow VMID to initially
0x01	0x0109	Write	Set BIAS_ENA=1, VMID_MODE remains the same
0x1E	0x0002	Write	Reset BIAS_SRC=0, VMID_SOFTST=0 (Disable)
0x01	0x0009	Write	CHIP_REV=0000, STARTUP_BIAS_ENA=0, FLL_ENA=0, MICB_ENA=0, BIAS_ENA=1, VMID_BUF_ENA=0, VMID_MODE=01
0x03	0x00EF	Write	CP_ENA=1, OUT2L_ENA=1, OUT2R_ENA=1, MIXOUTL_ENA=1, MIXOUTR_ENA=1, DACL_ENA=1, DACR_ENA=1
0x0A	0x0000	Write	DAC_MUTE=0
0x2C	0x0150	Write	DACL_TO_MIXOUTL=1
0x2D	0x0150	Write	DACR_TO_MIXOUTR=1

REG INDEX	DATA VALUE	READ OR WRITE	COMMENT
0x35	0x0139	Write	OUT2_VU=1, OUT2L_MUTE=0, OUT2L_VOL=11_1001
0x36	0x0139	Write	OUT2_VU=1, OUT2R_MUTE=0, OUT2R_VOL=11_1001
0x3A	0x009C	Write	Set HP_SHORT=1, HP_SHORT2=1, HP_IPSTAGE_ENA=1; Reset CLAMP_IP=0
			400ms Delay
0x3A	0x00CC	Write	Set HP_OPSTAGE_ENA = 1, Reset CLAMP_OP=0
0x3A	0x00C8	Write	Reset HP_SHORT2=0
0x3A	0x00C0	Write	Reset HP_SHORT=0

Table 75 Stereo DAC to Headphone – Recommended Power up Sequence and Device Register Settings

Note:

These sequences are optimised for best audio performance and minimal pops; however a faster power up sequence can be gained by reducing the delay time at the expense of reducing the pop suppression capability of the device

STEREO DAC TO LINE OUTPUT

The following section details the configuration for stereo DAC to line output (LINEOUT1L/R). Slave mode, 24-bit I2S digital audio interface.

Block Diagram:

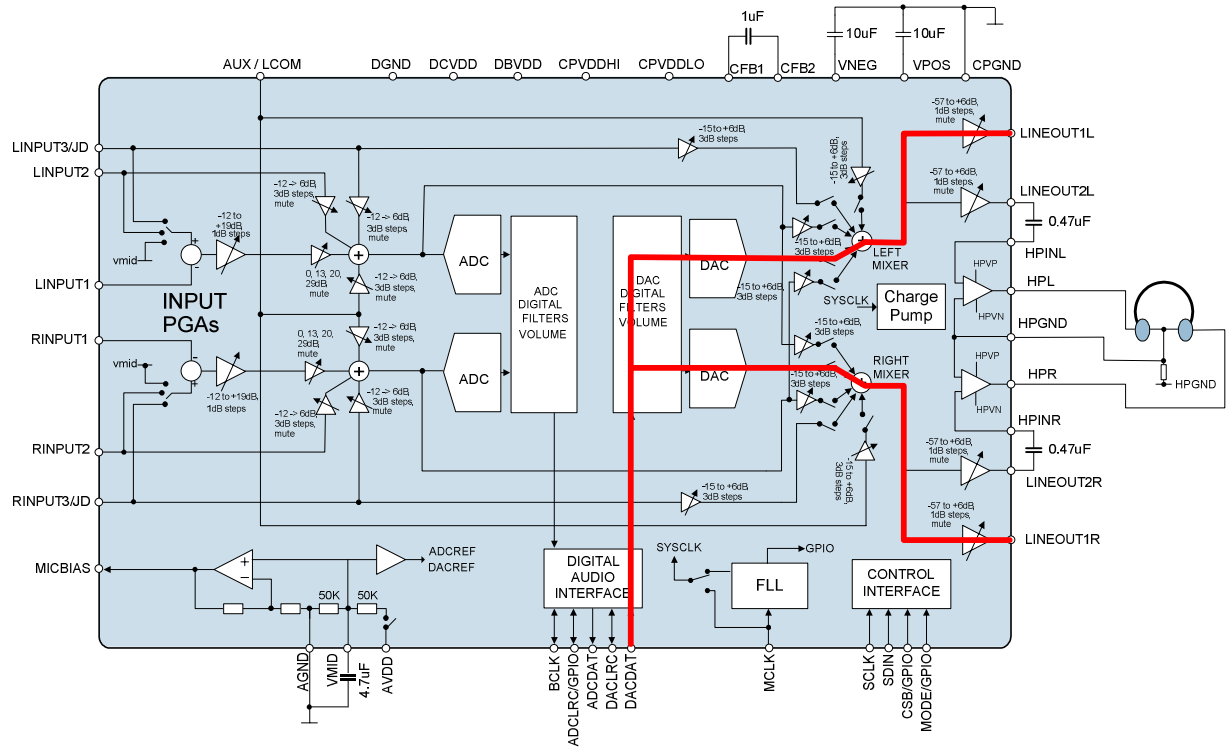


Figure 64 Stereo DAC to Line Output 1 Device Internal Signal Path

Register Settings:

REG INDEX	DATA VALUE	READ OR WRITE	COMMENT
0x1E	0x0102		Set OUT1_DIS=1 (Enable), OUT2_DIS=0
	100ms Delay		Delay (100ms) to remove any residual charge on LINEOUT_1
0x01	0x0100		Set STARTUP_BIAS_ENA=1, BIAS_ENA=0
0x1E	0x011A		Set BIAS_SRC=1, VMID_SOFTST=1
0x02	0xC180		Set OUT1L_ENA=1, OUT1R_ENA=1
0x1E	0x001A		Reset OUT1_DIS=0, Leave BIAS_SRC=1, VMID_SOFTST=1
0x01	0x0101		Set VMID_MODE=01 (2x50K Ohm Divider)
	200 ms Delay		Delay (200ms) to allow VMID to initially charge
0x01	0x0109		Set BIAS_ENA=1, VMID_MODE remains the same
0x1E	0x0002		Reset BIAS_SRC=0, VMID_SOFTST=0 (Disable)
0x01	0x0009		Set BIAS_ENA=0
0x03	0x008F		Set CP_ENA=1, OUT2L_ENA=0, OUT2R_ENA=0, MIXOUTL_ENA=1, MIXOUTR_ENA=1, DACL_ENA=1, DACR_ENA=1
0x0A	0x0000		AIF_LRCLKRATE=0, DAC_MONO=0, DAC_SB_FILT=0, DAC_MUTERATE=0, DAC_MUTEMODE=0, DEEMP=00, DAC_MUTE=0, DACL_DATINV=0, DACR_DATINV=0
0x2C	0x0150		DACL_TO_MIXOUTL=1, IN3L_TO_MIXOUTL=0, IN3L_MIXOUTL_VOL=101, DAC_LP=0, DAC_LP_VOL=0
0x2D	0x0150		DACR_TO_MIXOUTR=1, IN3R_TO_MIXOUTR=0, IN3R_MIXOUTR_VOL=101
0x33	0x01B9		OUT1_VU=1, OUT1L_ZC=1, OUT1L_MUTE=0, OUT1L_VOL=0dB
0x34	0x01B9		OUT1_VU=1, OUT1R_ZC=1, OUT1R_MUTE=0, OUT1R_VOL=0dB

Table 76 Stereo DAC to Line Output 1 - Recommended Power up Sequence and Device Register Settings

Note:

These sequences are optimised for best audio performance and minimal pops; however a faster power up sequence can be gained by reducing the delay time at the expense of reducing the pop suppression capability of the device

SINGLE ENDED MIC INPUT (L/RINPUT1) TO STEREO ADC

The following section details the configuration for single-ended stereo microphone input (L/RINPUT1) to stereo ADC. Slave mode, 24-bit I2S digital audio interface.

Block diagram:

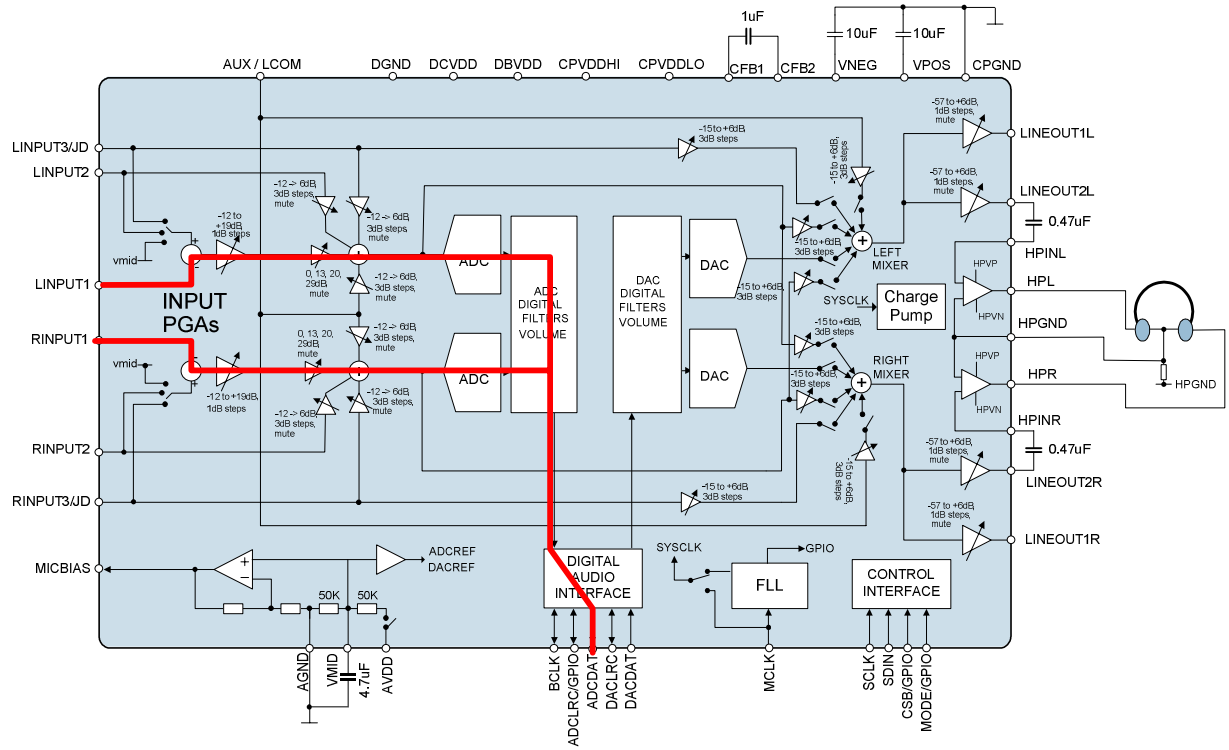


Figure 65 L/RINPUT1 to ADC Internal Signal Path - Recommended Power up Sequence and Device Register Settings

Register Settings:

REG INDEX	DATA VALUE	READ OR WRITE	COMMENT
R0	0x0000	Write	Reset WM8900
R1	0x001D	Write	Enable VMID, VMID_BUF, BIAS, MIC_BIAS
R2	0xC03F	Write	Enable ADC, Input PGA, Input Mixer,
R15	0x01C0	Write	Enable Left ADC Volume Update
R16	0x01C0	Write	Enable Right ADC Volume Update
R22	0x010C	Write	Disable Left Input PGA MUTE, Set Input PGA Volume Update, 0dB Gain
R23	0x010C	Write	Disable Right Input PGA MUTE, Set Input PGA Volume Update, 0dB Gain
R26	0x0044	Write	Set Input PGAs to Input Mixers

Table 77 L/RINPUT1 to ADC Device Register Settings

LINE INPUT 3 TO HEADPHONE (BYPASS PATH)

The following section details the configuration for LINPUT3 and RINPUT3 to stereo headphone mode, Note that SYSCLK is still required to operate the charge pump which powers the headphone amplifiers, even although the digital audio interface is off.

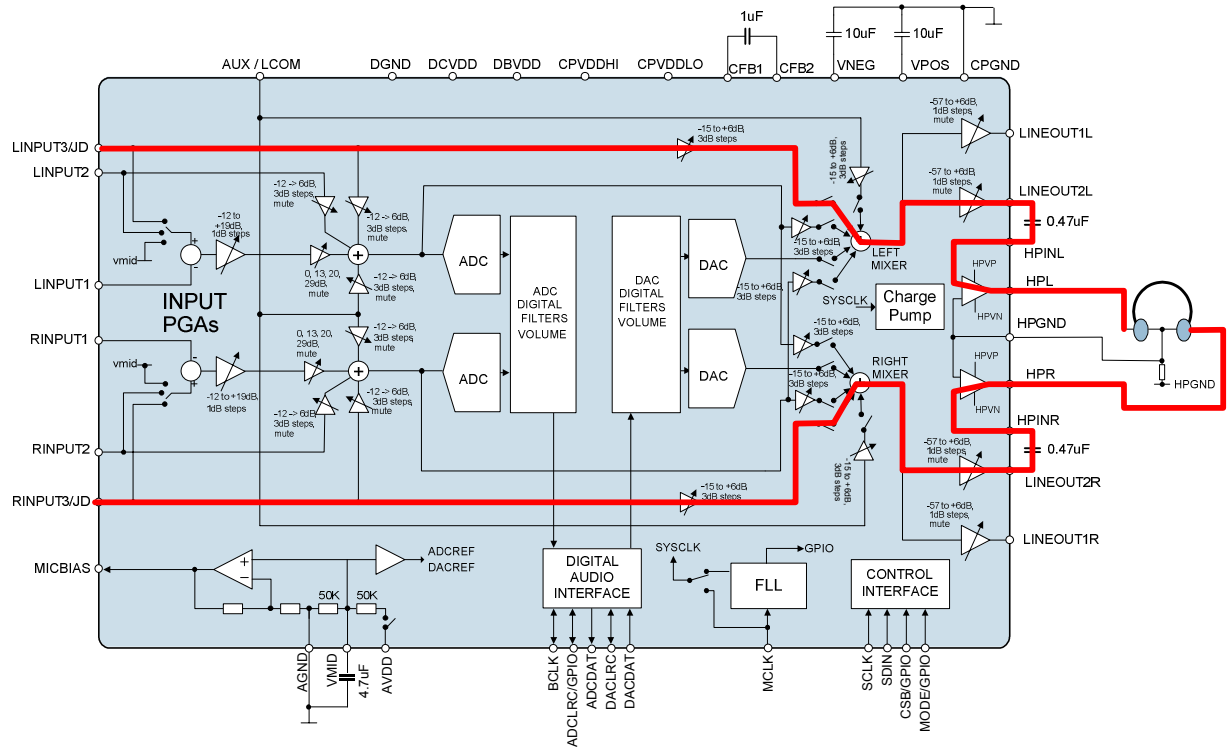


Figure 66 LR Input 3 to Headphone Bypass Path

REG INDEX	DATA VALUE	READ OR WRITE	COMMENT
0x3A	0x0030	Write	HIGHPOW=0, HP_IPSTAGE_ENA=0, HP_OPSTAGE_ENA=0, HP_CLAMP_IP=1, HP_CLAMP_OP=1, HP_SHORT=0, HP_SHORT2=0, HP_BIAS=00
0x1E	0x0082	Write	OUT1_DIS=0, OUT2_DIS=1, VMID_DISCH=0, BIAS_SRC=0, VMID_SOFTST=0, TEMP_SD=1, VROI=0
0x01	0x0100	Write	STARTUP_BIAS_ENA=1, FLL_ENA=0, MICB_ENA=0, BIAS_ENA=0, VMID_BUF_ENA=0, VMID_MODE=00
0x1E	0x009A	Write	OUT1_DIS=0, OUT2_DIS=1, VMID_DISCH=0, BIAS_SRC=1, VMID_SOFTST=1, TEMP_SD=1, VROI=0
0x03	0x0060	Write	CP_ENA=0, OUT2L_ENA=1, OUT2R_ENA=1, MIXOUTL_ENA=0, MIXOUTR_ENA=0, DACL_ENA=0, DACR_ENA=0
0x1E	0x001A	Write	OUT1_DIS=0, OUT2_DIS=0, VMID_DISCH=0, BIAS_SRC=1, VMID_SOFTST=1, TEMP_SD=1, VROI=0
0x01	0x0101	Write	STARTUP_BIAS_ENA=1, FLL_ENA=0, MICB_ENA=0, BIAS_ENA=0, VMID_BUF_ENA=0, VMID_MODE=01
	400ms Delay		INSERT_DELAY_MS 400
0x01	0x0109	Write	STARTUP_BIAS_ENA=1, FLL_ENA=0, MICB_ENA=0, BIAS_ENA=1, VMID_BUF_ENA=0, VMID_MODE=01
0x1E	0x0002	Write	OUT1_DIS=0, OUT2_DIS=0, VMID_DISCH=0, BIAS_SRC=0, VMID_SOFTST=0, TEMP_SD=1, VROI=0
0x01	0x0009	Write	STARTUP_BIAS_ENA=0, FLL_ENA=0, MICB_ENA=0, BIAS_ENA=1, VMID_BUF_ENA=0, VMID_MODE=01
0x03	0x00EC	Write	CP_ENA=1, OUT2L_ENA=1, OUT2R_ENA=1, MIXOUTL_ENA=1, MIXOUTR_ENA=1, DACL_ENA=0, DACR_ENA=0

REG INDEX	DATA VALUE	READ OR WRITE	COMMENT
0x0A	0x1004	Write	DAC_SDMCLK_RATE=1, AIF_LRCLKRATE=0, DAC_MONO=0, DAC_SB_FILT=0, DAC_MUTERATE=0, DAC_MUTEMODE=0, DEEMP=00, DAC_MUTE=1, DACL_DATINV=0, DACR_DATINV=0
0x2C	0x00D0	Write	DACL_TO_MIXOUTL=0, IN3L_TO_MIXOUTL=1, IN3L_MIXOUTL_VOL=101, DAC_LP=0, DAC_LP_VOL=0
0x2D	0x00D0	Write	DACR_TO_MIXOUTR=0, IN3R_TO_MIXOUTR=1, IN3R_MIXOUTR_VOL=101
0x35	0x0139	Write	OUT2_VU=1, OUT2L_ZC=0, OUT2L_MUTE=0, OUT2L_VOL=11_1001
0x36	0x0139	Write	OUT2_VU=1, OUT2R_ZC=0, OUT2R_MUTE=0, OUT2R_VOL=11_1001
0x3A	0x009C	Write	HIGHPOW=0, HP_IPSTAGE_ENA=1, HP_OPSTAGE_ENA=0, HP_CLAMP_IP=0, HP_CLAMP_OP=1, HP_SHORT=1, HP_SHORT2=1, HP_BIAS=00
	400ms Delay		INSERT_DELAY_MS 400
0x3A	0x00CC	Write	HIGHPOW=0, HP_IPSTAGE_ENA=1, HP_OPSTAGE_ENA=1, HP_CLAMP_IP=0, HP_CLAMP_OP=0, HP_SHORT=1, HP_SHORT2=1, HP_BIAS=00
0x3A	0x00C8	Write	HIGHPOW=0, HP_IPSTAGE_ENA=1, HP_OPSTAGE_ENA=1, HP_CLAMP_IP=0, HP_CLAMP_OP=0, HP_SHORT=1, HP_SHORT2=0, HP_BIAS=00
0x3A	0x00C0	Write	HIGHPOW=0, HP_IPSTAGE_ENA=1, HP_OPSTAGE_ENA=1, HP_CLAMP_IP=0, HP_CLAMP_OP=0, HP_SHORT=0, HP_SHORT2=0, HP_BIAS=00

Table 78 LR input 3 to Headphone Bypass Path - Recommended Power Up Sequence and Device Register Settings

Note:

These sequences are optimised for best audio performance and minimal pops; however a faster power up sequence can be gained by reducing the delay time at the expense of reducing the pop suppression capability of the device

RECOMMENDED POWER DOWN SEQUENCE

REG INDEX	DATA VALUE	READ OR WRITE	COMMENT
0x3A	0x00C8	Write	Set HP_SHORT=1
0x3A	0x0088	Write	Reset HP_OPSTAGE_ENA=0
0x3A	0x0030	Write	Set CLAMP_IP=1, CLAMP_OP=1; Reset HP_SHORT=0, HP_IPSTAGE_ENA=0
0x2C	0x0050	Write	Reset DACL_TO_MIXOUTL=0
0x2D	0x0050	Write	Reset DACR_TO_MIXOUTR=0
0x01	0x0109	Write	Set STARTUP_BIAS_ENA=1
0x1E	0x001A	Write	Set BIAS_SRC=1, VMID_SOFTST=1
0x01	0x0100	Write	Reset BIAS_ENA=0, VMIDBUF_ENA=0, VMID_MODE=00, Leave STARTUP_BIAS_ENA=1
	500ms Delay		INSERT_DELAY_MS [500]
0x1E	0x0100	Write	Disable Thermal shutdown, Set OUT1_DIS=1
From here, the user can achieve optimal power saving and a predictable mode of operation by writing the default data value to all registers **except R30 (0x1E)**. These default register writes can be carried out in any order.			

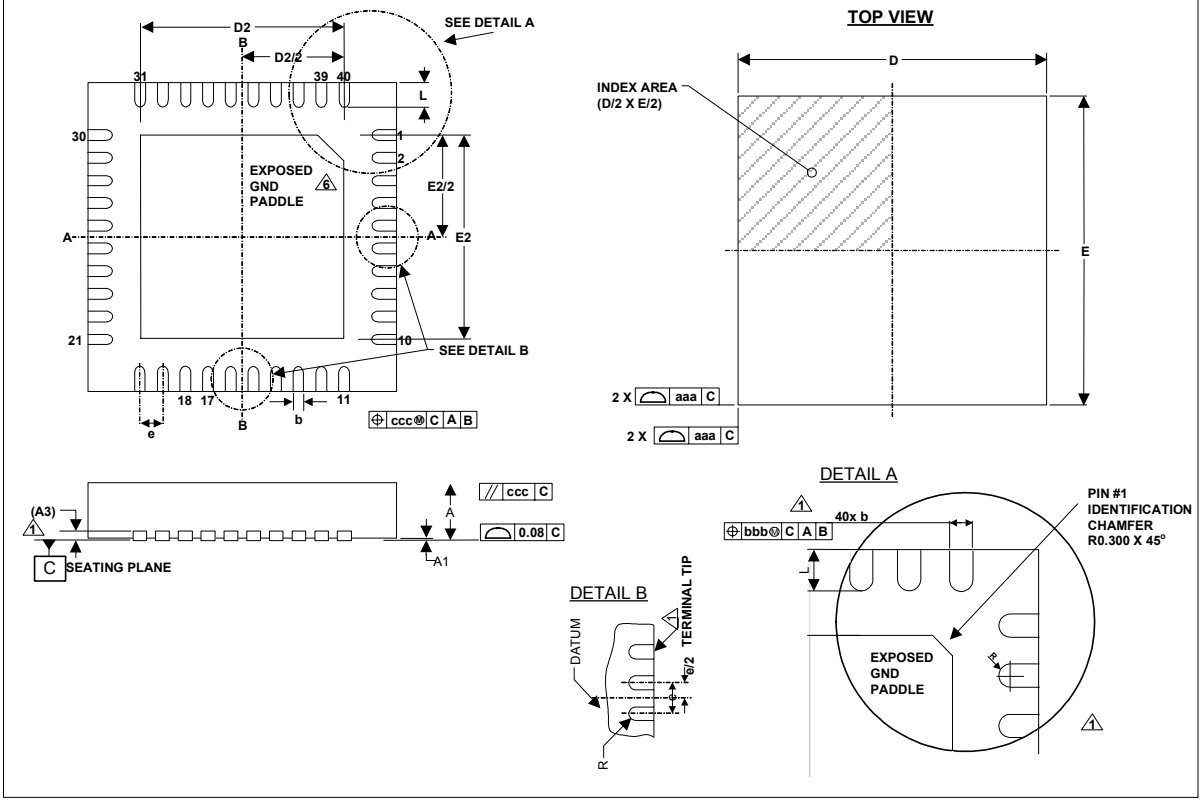
Table 79 Recommended Power Down Sequence

Note:

These sequences are optimised for best audio performance and minimal pops; however a faster power up sequence can be gained by reducing the delay time at the expense of reducing the pop suppression capability of the device.

PACKAGE DIMENSIONS

FL: 40 PIN QFN PLASTIC PACKAGE 5 X 5 X 0.55 mm BODY, 0.40 mm LEAD PITCH **DM051.A**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0	0.02	0.05	
A3		0.203 REF		
b	0.15	0.20	0.25	1
D		5.00 BSC		
D2	3.55	3.6	3.65	2
E		5.00 BSC		
E2	3.55	3.6	3.65	2
e		0.4 BSC		
L	0.35	0.4	0.45	
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220			

NOTES:
1. **DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.**
2. **FALLS WITHIN JEDEC, MO-220.**
3. **ALL DIMENSIONS ARE IN MILLIMETRES**
4. **THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.**
5. **REFER TO APPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION.**

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