WM8400

Wolfson AudioPlus™ Hi-Fi Audio CODEC and Power Management Unit for Mobile Multimedia

DESCRIPTION

The WM8400 is a highly integrated audio CODEC and power management unit which provides a cost-effective companion solution for mobile multimedia applications.

Stereo 24-bit sigma-delta ADCs and DACs provide hi-fi quality audio recording and playback, with a flexible digital audio interface supporting most commonly-used data formats and clocking schemes. An integrated low-power FLL, an alternative DAC interface and TDM support provide additional flexibility.

The ultra-low power audio CODEC is complemented with a powerful 1W speaker driver, which can operate in class D or AB modes. Low leakage, high PSRR and pop/click suppression enable direct battery connection for the speaker supply.

Multiple microphone or line inputs (mono, stereo, single-ended or differential) can be supported. A programmable high-pass filter is provided to remove low frequency noise from the input signal.

Four headphone drivers support fully differential headset drive, providing excellent crosstalk performance and bass response, maximising stereo effects, and allowing the removal of large and expensive headphone capacitors.

The WM8400 incorporates two programmable DC-DC step-down (Buck) converters and four low-dropout (LDO) regulators. The startup sequence and default voltages for the DC-DC converters and two of the LDOs are pin selectable; All the regulators are software programmable. The DC-DCs, LDO1 and LDO2 are intended to power the MMP sub-system, whilst the remaining LDOs are specifically designed to power the on-chip audio CODEC.

The WM8400 is supplied in a 6x6mm 105-ball BGA package, ideal for use in portable systems. The WM8400 forms part of the Wolfson AudioPlus™ series of audio and power management solutions.

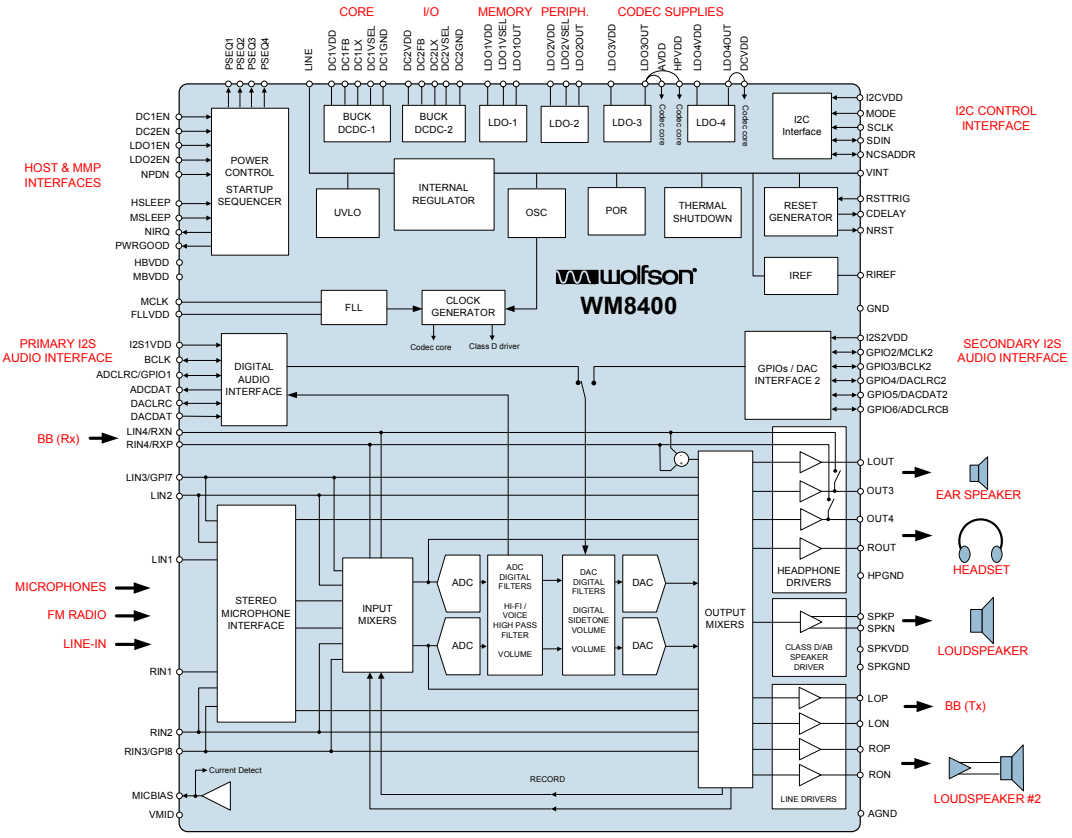
FEATURES

- DAC SNR 93dB ('A' weighted), THD -84dB at 48kHz, 3.0V
- ADC SNR 93dB ('A' weighted), THD -82dB at 44.1kHz, 3.0V
- Microphone interface (Up to four differential microphones)
- 1W Speaker driver
  - 1W into 8Ω BTL speaker at <0.1% THD
  - 80dB PSRR @ 217Hz
  - <1uA leakage with direct battery connection
  - Software-selectable class D or AB mode
  - Filterless connection supported
  - Pop/Click suppression
- Headphone / ear speaker drivers
  - 40mW output power into 16Ω at 3.3V
  - Fully differential and capless modes supported
  - Pop/Click suppression
- 4 Mono or stereo differential line outputs
- On-chip FLL provides flexible clocking scheme
- Sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48kHz
- Powerful GPIO functions
- 2 software-programmable DC-DC buck converters (up to 1A)
- 4 software-programmable LDO regulators (up to 250mA)
- Pin selectable start-up sequence and default voltages
- Ultra-low power consumption
  - 5mW analogue voice call
  - 13mW DAC playback to headphones
- 105-ball 6x6mm BGA package

APPLICATIONS

- Multimedia and feature-rich mobile handsets
- PDAs
- Co-processor companion for multimedia processors
- Digital Photo Frames
- PND
- PMP

BLOCK DIAGRAM



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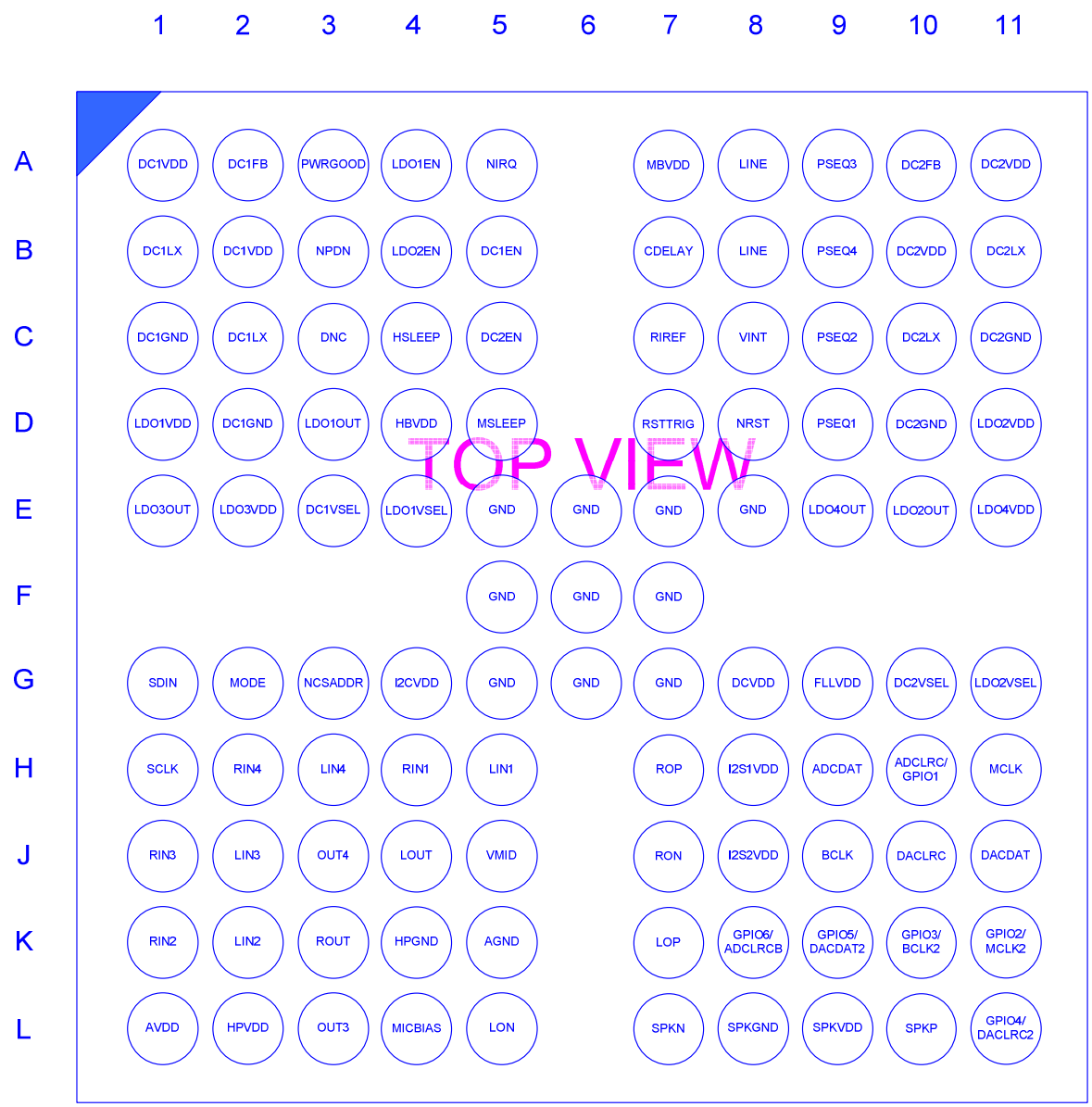
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8400GEB/V	-40°C to +85°C	105-ball BGA (6 x 6 mm) (Pb-free)	MSL3	260°C
WM8400GEB/RV	-40°C to +85°C	105-ball BGA (6 x 6 mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 2,200

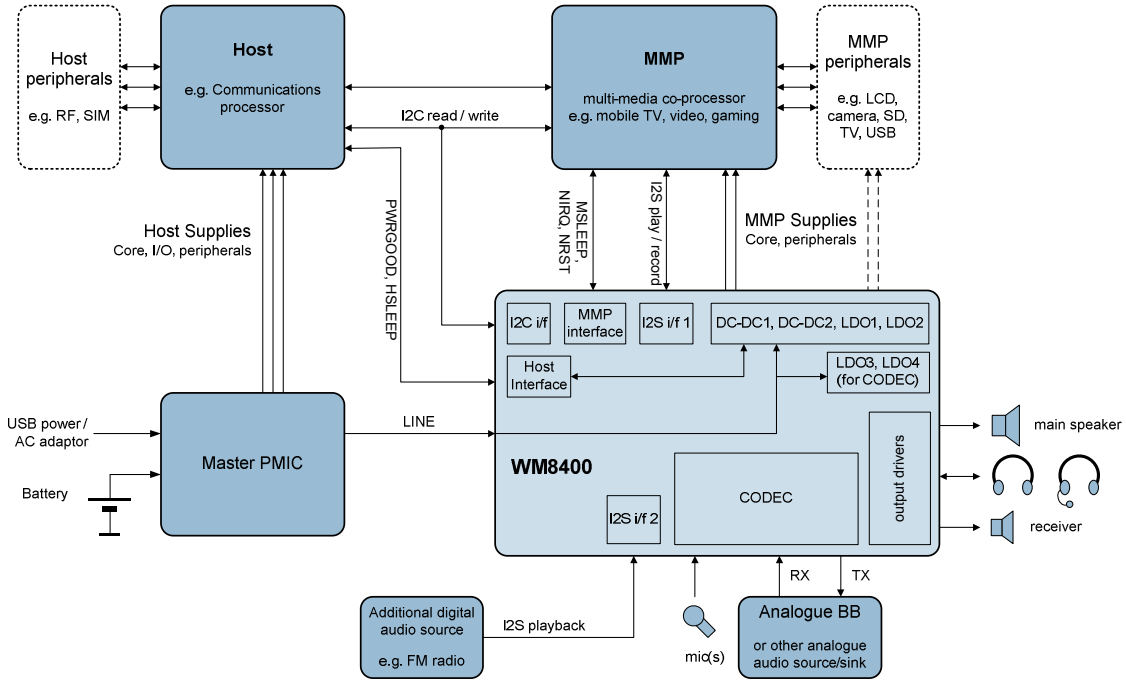
PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION	DOMAIN
H9	ADCDAT	Digital Output	ADC digital audio data output	I2S1VDD
H10	ADCLRC/GPIO1	Digital Input / Output	Audio interface ADC left/right clock / GPIO pin	I2S1VDD
K5	AGND	Supply	Analogue ground (return path for AVDD)	
L1	AVDD	Supply	Analogue supply	
J9	BCLK	Digital Input / Output	Audio interface bit clock	I2S1VDD
B7	CDELAY	Analogue Output	Converter start-up time (external capacitor)	
J11	DACDAT	Digital Input	DAC digital audio data input	I2S1VDD
J10	DACLRC	Digital Input / Output	Audio interface DAC left / right clock	I2S1VDD
B5	DC1EN	Digital Input	Enable pin for DC-DC1	HBVDD
A2	DC1FB	Analogue Input	Feedback for DCDC1	
C1, D2	DC1GND	Supply	DC-DC1 ground (return path for DC-DC1)	DC1VDD
B1	DC1LX	Analogue Input/Output	Connection for DCDC1 Inductor	DC1VDD
C2	DC1LX	Analogue Input/Output	Connection for DCDC1 Inductor	DC1VDD
A1, B2	DC1VDD	Supply	Power input to DC-DC1	
E3	DC1VSEL	Analogue Input	Startup voltage select for DC-DC1	VINT
C5	DC2EN	Digital Input	Enable pin for DC-DC2	HBVDD
A10	DC2FB	Analogue Input	Feedback for DCDC2	
C11, D10	DC2GND	Supply	DC-DC2 ground (return path for DC-DC2)	DC2VDD
B11	DC2LX	Analogue Input/Output	Connection for DCDC2 Inductor	DC2VDD
C10	DC2LX	Analogue Input/Output	Connection for DCDC2 Inductor	DC2VDD
A11, B10	DC2VDD	Supply	Power input to DC-DC2	
G10	DC2VSEL	Analogue Input	Startup voltage select for DC-DC2	VINT
G8	DCVDD	Supply	Digital Core Supply	
C3	DNC	Do Not Connect	Do Not Connect	
G9	FLLVDD	Supply	FLL Supply	
E5, E6, E7, E8, F5, F6, F7, G5, G6, G7	GND	Supply	Ground	
K11	GPIO2/MCLK2	Digital Input / Output	Alternative MCLK / GPIO pin	I2S2VDD
K10	GPIO3/BCLK2	Digital Input / Output	Alternative BCLK / GPIO pin	I2S2VDD
L11	GPIO4/DACLRC2	Digital Input / Output	Alternative DACLRC / GPIO pin	I2S2VDD
K9	GPIO5/DACDAT2	Digital Input / Output	Alternative DACDAT / GPIO pin	I2S2VDD
K8	GPIO6/ADCLRCB	Digital Input / Output	Inverted ADCLRC / GPIO pin	I2S2VDD
D4	HBVDD	Supply	Power supply for Host Buffer interface	
K4	HPGND	Supply	Headphone ground (return path for HPVDD)	
L2	HPVDD	Supply	Headphone supply	
C4	HSLEEP	Digital Input	Sleep pin for Host Buffer interface	HBVDD
G4	I2CVDD	Supply	Power supply for control (I2C) interface	
H8	I2S1VDD	Supply	Power supply for primary digital audio (I2S) interface	
J8	I2S2VDD	Supply	Power supply for secondary digital audio (I2S) interface	
A4	LDO1EN	Digital Input	Enable pin for LDO 1	HBVDD
D3	LDO1OUT	Analogue Output	Power Output from LDO 1	LDO1VDD
D1	LDO1VDD	Supply	LDO 1 Supply	
E4	LDO1VSEL	Analogue Input	Startup voltage select for LDO 1	VINT
B4	LDO2EN	Digital Input	Enable pin for LDO 2	HBVDD
E10	LDO2OUT	Analogue Output	Power Output from LDO 2	LDO2VDD
D11	LDO2VDD	Supply	LDO 2 Supply	
G11	LDO2VSEL	Analogue Input	Startup voltage select for LDO 2	VINT
E1	LDO3OUT	Analogue Output	Power Output from LDO 3	LDO3VDD

PIN NO	NAME	TYPE	DESCRIPTION	DOMAIN
E2	LDO3VDD	Supply	LDO 3 Supply	
E9	LDO4OUT	Analogue Output	Power Output from LDO 4	LDO4VDD
E11	LDO4VDD	Supply	LDO 4 Supply	
H5	LIN1	Analogue Input	Left MIC input / negative diff MIC input	AVDD
K2	LIN2	Analogue Input	Left line input / positive diff MIC input	AVDD
J2	LIN3	Analogue Input / Digital Input	Left line input / negative diff input / button detect	AVDD
H3	LIN4	Analogue Input	Left line input / differential MIC / Mono diff RXN	AVDD
A8, B8	LINE	Supply	Main battery input line	
L5	LON	Analogue Output	Differential Left Line Out (-)ve	AVDD
K7	LOP	Analogue Output	Differential Left Line Out (+)ve	AVDD
J4	LOUT	Analogue Output	Left headphone output	HPVDD
A7	MBVDD	Supply	Power supply for MMP interface	
H11	MCLK	Digital Input	Master clock input	I2S1VDD
L4	MICBIAS	Analogue Output	Microphone bias	AVDD
G2	MODE	Digital Input	Selects 2-wire or 3/4-wire control	I2CVDD
D5	MSLEEP	Digital Input	Sleep pin for MMP interface	MBVDD
G3	NCSADDR	Digital Input	3-wire chip select or 2-wire address select	I2CVDD
A5	NIRQ	Digital Output	Interrupt output (active low)	MBVDD
B3	NPDN	Digital Input	Power down (active low)	HBVDD
D8	NRST	Digital Output	Reset output (active low)	MBVDD
L3	OUT3	Analogue Output	Inverted left headphone output / Mono inverted output	HPVDD
J3	OUT4	Analogue Output	Inverted right headphone output / Mono non-inverted output	HPVDD
D9	PSEQ1	Digital Output	Power Sequencing Output 1	LINE
C9	PSEQ2	Digital Output	Power Sequencing Output 2	LINE
A9	PSEQ3	Digital Output	Power Sequencing Output 3	LINE
B9	PSEQ4	Digital Output	Power Sequencing Output 4	LINE
A3	PWRGOOD	Digital Output	Power Good Signal	HBVDD
H4	RIN1	Analogue Input	Right MIC input / negative diff MIC input	AVDD
K1	RIN2	Analogue Input	Right line input / positive diff MIC input	AVDD
J1	RIN3	Analogue Input / Digital Input	Right line input / negative diff input / button detect	AVDD
H2	RIN4	Analogue Input	Right line input / differential MIC / Mono diff RXP	AVDD
C7	RIREF	Analogue Input	Bias Current Set (external resistor)	
J7	RON	Analogue Output	Differential Right Line Out (-)ve	AVDD
H7	ROP	Analogue Output	Differential Right Line Out (+)ve	AVDD
K3	ROUT	Analogue Output	Right headphone output	HPVDD
D7	RSTTRIG	Digital Input	Trigger input for reset timer	HBVDD
H1	SCLK	Digital Input	Control interface clock input (2/3-wire)	I2CVDD
G1	SDIN	Digital Input / Output	Control interface data input / 2-wire acknowledge	I2CVDD
L8	SPKGND	Supply	Speaker ground (return path for SPKVDD)	
L7	SPKN	Analogue Output	Speaker negative output	SPKVDD
L10	SPKP	Analogue Output	Speaker positive output	SPKVDD
L9	SPKVDD	Supply	Speaker supply	
C8	VINT	Analogue Output	Decoupling point for internal supply	
J5	VMID	Analogue Output	CODEC midrail reference voltage	AVDD

Note: Digital input pins have Schmitt trigger input buffers and are 3.3V tolerant.

TYPICAL CONNECTIONS

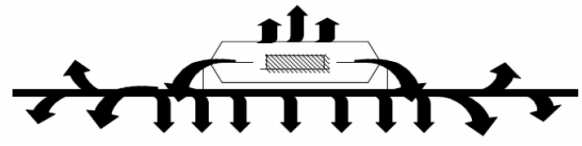


THERMAL CHARACTERISTICS

Thermal analysis must be performed in the intended application to prevent the WM8400 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the ten central GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package leads to PCB (conduction).



The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated by the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air.
- For WM8400, Θ_{JA} = 46°C/W

The junction temperature T_J is given by $T_J = T_A + T_R$

- T_A, is the ambient temperature.

The worst case conditions are when the WM8400 is operating in a high ambient temperature, with low supply voltage, high duty cycle and high output current. Under such conditions, it is possible that the heat dissipated could exceed the maximum junction temperature of the device. Care must be taken to avoid this situation. An example calculation of the junction temperature is given below.

- P_D = 0.98W (example figure)
- Θ_{JA} = 46°C/W
- $T_R = P_D * \Theta_{JA}$ = 45.08°C
- T_A = 85°C (example figure)
- $T_J = T_A + T_R$ = 130.08°C

The minimum and maximum operating junction temperatures for the WM8400 are quoted in the "Absolute Maximum Ratings" section. The maximum recommended operating junction temperature is 125°C. Therefore, the junction temperature in the above example exceeds the operating limits of the WM8400, and is not recommended for sustained operation.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages: MBVDD, HBVDD, I2CVDD, I2S1VDD, I2S2VDD, FLLVDD, HPVDD, AVDD, DCVDD	-0.3V	+4.5V
Supply voltages: LINE, DC1VDD, DC2VDD, LDO1VDD, LDO2VDD, LDO3VDD, LDO4VDD, SPKVDD	-0.3V	+7V
Voltage range digital inputs	GND - 0.3V	HBVDD + 0.3V MBVDD + 0.3V I2CVDD + 0.3V I2S1VDD + 0.3V I2S2VDD + 0.3V
Voltage range analogue inputs	AGND - 0.3V	AVDD + 0.3V FLLVDD + 0.3V
	GND - 0.3V	LINE + 0.3V
	HPGND - 0.3V	HPVDD + 0.3V
Junction temperature, T_J	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.
2. I2CVDD Maximum voltage limit should never be exceeded for any duration of time.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital core supply range	DCVDD	1.71		3.6	V
Digital interfaces supply range	HBVDD, MBVDD, I2CVDD, I2S1VDD, I2S2VDD	1.71		3.6	V
Analogue supplies range	LINE	2.7		5.5	V
	LDO1VDD, LDO2VDD, LDO3VDD, LDO4VDD	2.5		5.5	V
	DC1VDD, DC2VDD	2.7		5.5	V
Analogue supplies range	AVDD, FLLVDD, HPVDD,	2.7		3.6	V
Speaker supply range	SPKVDD	2.7		5.5	V
Ground	GND, AGND, HPGND, SPKGND		0		V
Ambient temperature, T_A		-40		+85	ºC
Junction temperature, T_J		-40		+125	ºC

Notes

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
3. DCVDD must be less than or equal to AVDD.
4. DCVDD must be less than or equal to MBVDD, I2S1VDD and I2S2VDD.
5. AVDD must be less than or equal to SPKVDD.
6. HPVDD must be equal to AVDD
7. SPKVDD must be high enough to support the peak output voltage when using DCGAIN and ACGAIN functions, to avoid output waveform clipping. Peak output voltage is AVDD*(DCGAIN+ACGAIN)/2.
8. The minimum LINE voltage for starting up the WM8400 is also determined by a programmable threshold. See “Battery Monitoring and Undervoltage Lock-Out (UVLO)”.
9. LDOnVDD and DCnVDD must be high enough to support the required output voltage from the respective regulator or converter. See “Electrical Characteristics”.
10. Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and the junction temperature limits must both be observed. See “Thermal Characteristics”.

SPEAKER POWER DE-RATING CURVE

The speaker driver has been designed to drive a maximum of 1W into 8ohm in class D mode, and 0.5W into 8Ω in class AB mode. These figures are based on operation at room temperature but for operation at higher temperatures please refer to the power de-rating curve below. Under no circumstances should the recommended maximum powers or junction temperature of the device be exceeded.

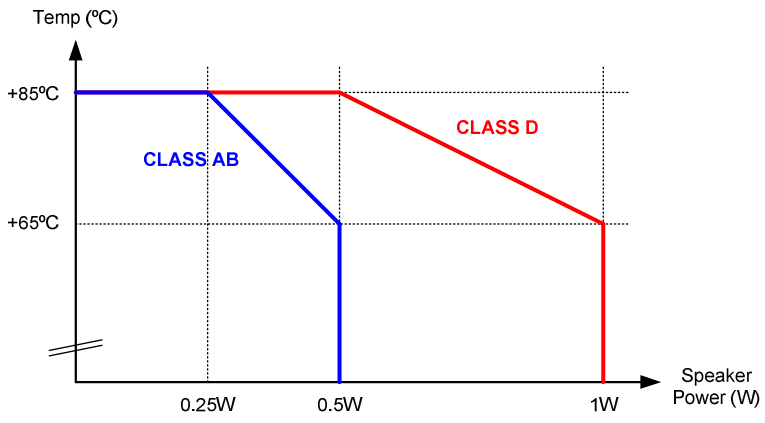
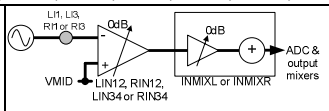
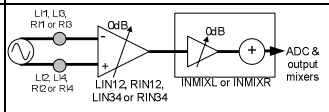
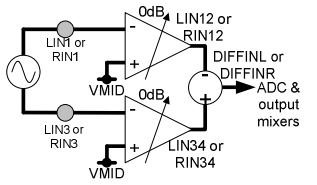
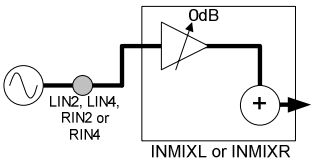
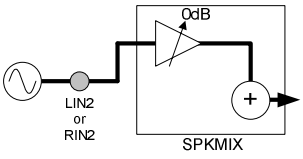
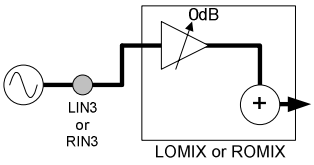
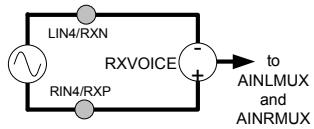
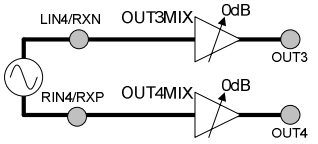


Figure 1 Speaker Power De-Rating Curve

ELECTRICAL CHARACTERISTICS

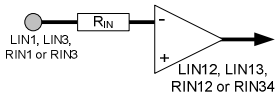
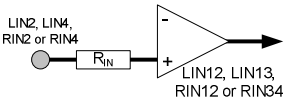
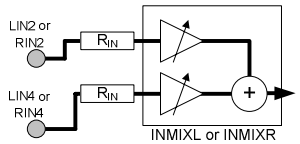
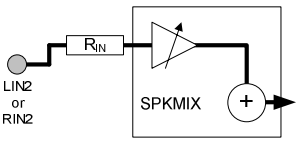
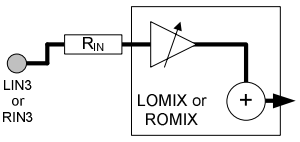
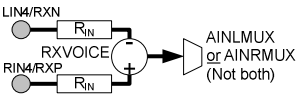
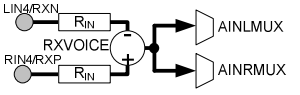
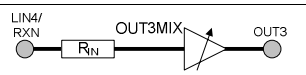
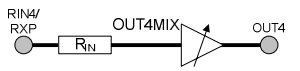
Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Input Pin Maximum Signal Levels (LIN1, LIN2, LIN3, LIN4, RIN1, RIN2, RIN3, RIN4)						
Maximum Full-Scale PGA Input Signal Level **Note 1:** This changes in proportion to AVDD. Full-Scale level is typically AVDD/3.3Vrms **Note 2:** When mixing input PGA outputs and line inputs the total signal must not exceed the values shown here.	Single-ended PGA input on LIN1, LIN3, RIN1 or RIN3, output to INMIXL or INMIXR			0.909 -0.829		Vrms dBV
	Differential PGA input on LIN1/LIN2, LIN3/LIN4, RIN1/RIN2 or RIN3/RIN4, output to INMIXL or INMIXR			0.909 -0.829		Vrms dBV
	Differential input to two single-ended PGA inputs on LIN1/LIN3 or RIN1/RIN3, output to DIFFINL or DIFFINR			0.909 -0.829		Vrms dBV
Maximum Full-Scale Line Input Signal Level **Note 1:** This changes in proportion to AVDD. Full-Scale level is typically AVDD/3.3Vrms **Note 2:** When mixing line inputs, input PGA outputs and DAC outputs the total signal must not exceed the values shown here.	Line input on LIN2, LIN4, RIN2 or RIN4 to INMIXL or INMIXR			0.909 -0.829		Vrms dBV
	Line input on LIN2 or RIN2 to SPKMIX			0.909 -0.829		Vrms dBV
	Line input on LIN3 or RIN3 to LOMIX or ROMIX			0.909 -0.829		Vrms dBV
	Differential mono line input on RXP/RXN to RXVOICE			0.909 -0.829		Vrms dBV
	Differential mono line input on RXP/RXN to differential output on OUT3/OUT4			0.909 -0.829		Vrms dBV

Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Input Pin Impedances (LIN1, LIN2, LIN3, LIN4, RIN1, RIN2, RIN3, RIN4)						
PGA Input Resistance Note: this will be seen in parallel with the resistance of other enabled input paths from the same pin	LIN1, LIN3, RIN1 or RIN3 (PGA Gain = -16.5dB)			57		kΩ
	LIN1, LIN3, RIN1 or RIN3 (PGA Gain = 0dB)			33		kΩ
	LIN1, LIN3, RIN1 or RIN3 (PGA Gain = +30dB)			2		kΩ
	LIN2, LIN4, RIN2 or RIN4 (Constant for all gains)			65		kΩ
Line Input Resistance **Note:** this will be seen in parallel with the resistance of other enabled input paths from the same pin	LIN2 or RIN2 to INMIXL or INMIXR (-12dB)			60		kΩ
	LIN2 or RIN2 to INMIXL or INMIXR (0dB)			15		kΩ
	LIN2 or RIN2 to INMIXL or INMIXR (+6dB)			7.5		kΩ
	LIN2 or RIN2 to SPKMIX (SPKATTN = 0dB)			20		kΩ
	LIN2 or RIN2 to SPKMIX (SPKATTN = -12dB)			20		kΩ
	LIN3 or RIN3 to LOMIX or ROMIX (0dB)			20		kΩ
	LIN3 or RIN3 to LOMIX or ROMIX (-21dB)			224		kΩ
	RXP and RXN via RXVOICE to AINLMUX or AINRMUX (Gain = +6dB)			22		kΩ
	RXP and RXN via RXVOICE to AINLMUX or AINRMUX (Gain = 0dB)			27		kΩ
	RXP and RXN via RXVOICE to AINLMUX or AINRMUX (Gain = -12dB)			60		kΩ
	RXP and RXN via RXVOICE to AINLMUX and AINRMUX (Gain = +6dB)			12		kΩ
	RXP and RXN via RXVOICE to AINLMUX and AINRMUX (Gain = 0dB)			16		kΩ
	RXP and RXN via RXVOICE to AINLMUX and AINRMUX (Gain = -12dB)			30		kΩ
	LIN4 to OUT3 or RIN4 to OUT4 (Gain = -6dB)			20		kΩ
	LIN4 to OUT3 or RIN4 to OUT4 (Gain = 0dB)			20		kΩ
Input Capacitance	All analogue input pins			10		pF

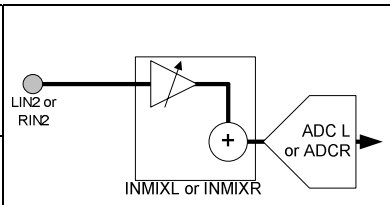
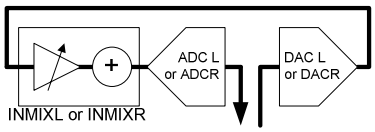
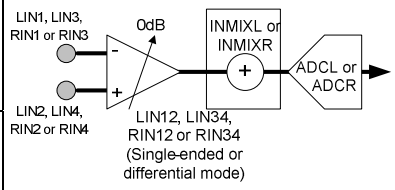
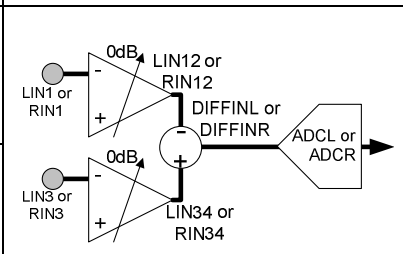
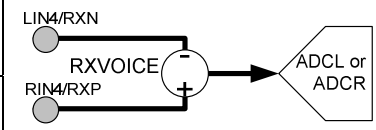
Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Programmable Gain Amplifiers (PGAs) LIN12, LIN34, RIN12 and RIN34					
PGA equivalent input noise	0 to 20kHz, +30dB gain		150		uV
Minimum Programmable Gain			-16.5		dB
Maximum Programmable Gain			30		dB
Programmable Gain Step Size	Guaranteed monotonic		1.5		dB
Mute Attenuation	PGA to ADC		90		dB
	PGA to output mixers (directly)		90		dB
	PGA to output mixers (via AINLMUX or AINRMUX)		90		dB
Common Mode Rejection Ratio (1kHz input)	Single PGA in differential mode, gain = +30dB		40		dB
	Single PGA in differential mode, gain = 0dB		40		
	Single PGA in differential mode, gain = -16.5dB		40		
	Differential input to DIFFINL or DIFFINR via LIN1/LIN3 or RIN1/RIN3, gain = 0dB		40		
Received Voice (RXP-RXN) Differential to Single-Ended Converter RXVOICE					
Minimum Programmable Gain	AINLMODE = 01 or AINRMODE = 01		-12		dB
Maximum Programmable Gain	AINLMODE = 01 or AINRMODE = 01		+6		dB
Programmable Gain Step Size	AINLMODE = 01 or AINRMODE = 01		3		dB
Mute Attenuation	AINLMODE ≠ 01 or AINRMODE ≠ 01		100		dB
PGA Output Differential to Single Ended Converters DIFFINL and DIFFINR					
Fixed Gain	AINLMODE = 10 or AINRMODE = 10		0		dB
Mute Attenuation	AINLMODE ≠ 10 or AINRMODE ≠ 10		100		dB
Input Mixers INMIXL and INMIXR					
Minimum Programmable Gain	PGA Outputs to INMIXL and INMIXR		0		dB
Maximum Programmable Gain	PGA Outputs to INMIXL and INMIXR		+30		dB
Programmable Gain Step Size	PGA Outputs to INMIXL and INMIXR		30		dB
Minimum Programmable Gain	Line Inputs and Record path to INMIXL and INMIXR		-12		dB
Maximum Programmable Gain	Line Inputs and Record path to INMIXL and INMIXR		+6		dB
Programmable Gain Step Size	Line Inputs and Record path to INMIXL and INMIXR		3		dB
Mute attenuation			100		dB

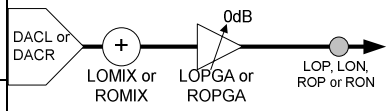
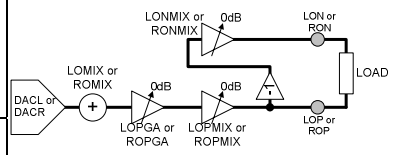
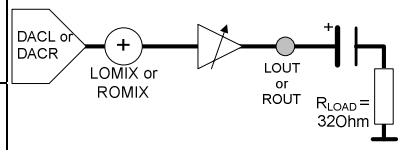
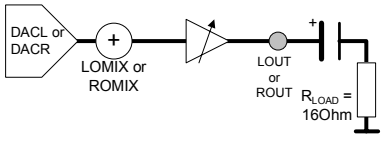
Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC Input Path Performance						
SNR (A-weighted)	Line inputs to ADC via INMIXL and INMIXR, AVDD = 3.0V			94		dB
THD (-1dBFS input)				-83		dB
THD+N (-1dBFS input)				-81		dB
Crosstalk (L/R)				-83		dB
SNR (A-weighted)	Line inputs to ADC via INMIXL and INMIXR, AVDD = 2.7V			92		dB
THD (-1dBFS input)				-78		dB
THD+N (-1dBFS input)				-76		dB
SNR (A-weighted)	Record path (DACs to ADCs via INMIXL and INMIXR), AVDD = 3.0V			92		dB
THD (-1dBFS input)				-83		dB
THD+N (-1dBFS input)				-81		dB
Crosstalk (L/R)				-67		dB
SNR (A-weighted)	Record path (DACs to ADCs via INMIXL and INMIXR), AVDD = 2.7V			92		dB
THD (-1dBFS input)				-78		dB
THD+N (-1dBFS input)				-76		dB
SNR (A-weighted)	Input PGAs to ADC via INMIXL or INMIXR, AVDD = 3.0V			93		dB
THD (-1dBFS input)				-83		dB
THD+N (-1dBFS input)				-81		dB
Crosstalk (L/R)				-67		dB
SNR (A-weighted)	Input PGAs to ADC via INMIXL or INMIXR, AVDD = 2.7V			92		dB
THD (-1dBFS input)				-78		dB
THD+N (-1dBFS input)				-76		dB
SNR (A-weighted)	Input PGAs to ADC via DIFFINL or DIFFINR, AVDD = 3.0V			94		dB
THD (-1dBFS input)				-83		dB
THD+N (-1dBFS input)				-81		dB
Crosstalk (L/R)				-70		dB
SNR (A-weighted)	Input PGAs to ADC via DIFFINL or DIFFINR, AVDD = 2.7V			92		dB
THD (-1dBFS input)				-78		dB
THD+N (-1dBFS input)				-76		dB
SNR (A-weighted)	RXP-RXN to one ADC via RXVOICE, AVDD = 3.0V			92		dB
THD (-1dBFS input)				-80		dB
THD+N (-1dBFS input)				-78		dB
SNR (A-weighted)	RXP-RXN to one ADC via RXVOICE, AVDD = 2.7V			90		dB
THD (-1dBFS input)				-76		dB
THD+N (-1dBFS input)				-74		dB

Test Conditions

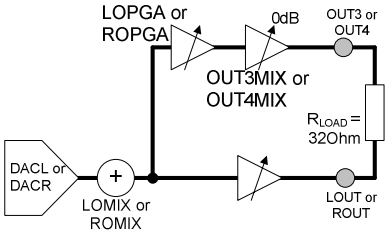
DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

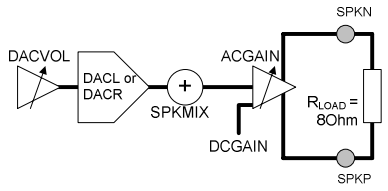
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC Output Path (Line Outputs 10kΩ / 50pF Load, Headphone Outputs 16Ω Load, Speaker Output 8Ω BTL Load)						
SNR (A-weighted)	DAC to single-ended line out, 0dBFS input, AVDD = 3.0V			96		dB
THD				-86		dB
THD+N				-83		dB
Crosstalk (L/R)				-100		dB
AVDD PSRR (217Hz)				45		dB
SNR (A-weighted)	DAC to single-ended line out, 0dBFS input, AVDD = 2.7V			97		dB
THD				-85		dB
THD+N				-83		dB
SNR (A-weighted)	DAC to differential line out, 0dBFS input, AVDD = 3.0V			96		dB
THD				-86		dB
THD+N				-83		dB
Crosstalk (L/R)				-100		dB
AVDD PSRR (217Hz)				60		dB
DC Offset at Load				5		mV
SNR (A-weighted)	DAC to differential line out, 0dBFS input, AVDD = 2.7V			96		dB
THD				-85		dB
THD+N				-83		dB
Minimum Line Out Resistance	LOP, LON, ROP, RON		2			kΩ
Maximum Line Out Capacitance	LOP, LON, ROP, RON				10	nF
SNR (A-weighted)	DAC to LOUT or ROUT, R_L=32Ω, AVDD=HPVDD= 3.0V	32Ω AC-Coupled Headphone Outputs		98		dB
THD (P_O=5mW)				-77		dB
THD+N (P_O=5mW)				-74		dB
Crosstalk (L/R)				-100		dB
AVDD PSRR (217Hz)				45		dB
HPVDD PSRR (217Hz)				85		dB
SNR (A-weighted)	DAC to LOUT or ROUT, R_L=32Ω, AVDD=HPVDD= 2.7V			97		dB
THD (P_O=5mW)				-76		dB
THD+N (P_O=5mW)				-73		dB
SNR (A-weighted)	DAC to LOUT or ROUT, R_L=16Ω, AVDD=HPVDD= 3.0V	16Ω AC-Coupled Headphone Outputs		96		dB
THD (P_O=20mW)				-72		dB
THD+N (P_O=20mW)				-70		dB
THD (P_O=5mW)				-73		dB
THD+N (P_O=5mW)				-71		dB
Crosstalk (L/R)				-100		dB
AVDD PSRR (217Hz)				45		dB
HPVDD PSRR (217Hz)				85		dB
SNR (A-weighted)	DAC to LOUT, or ROUT, R_L=16Ω, AVDD=HPVDD= 2.7V			95		dB
THD (P_O=20mW)				-69		dB
THD+N (P_O=20mW)				-67		dB
THD (P_O=5mW)				-71		dB
THD+N (P_O=5mW)				-69		dB

Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

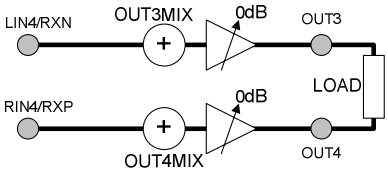
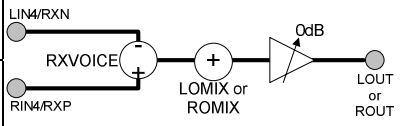
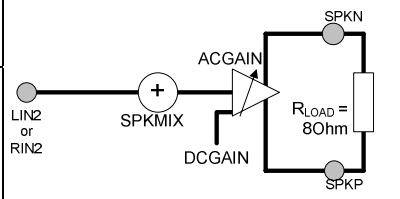
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SNR (A-weighted)	DAC to LOUT/OUT3 or ROUT/OUT4, R_L=32Ω, AVDD=HPVDD= 3.0V	Fully Differential Headphone Outputs		98		dB
THD (P_O=20mW)				-77		dB
THD+N (P_O=20mW)				-75		dB
THD (P_O=5mW)				-79		dB
THD+N (P_O=5mW)				-77		dB
Crosstalk (L/R)				-100		dB
AVDD PSRR (217Hz)				60		dB
HPVDD PSRR (217Hz)				85		dB
DC Offset at Load				5		mV
SNR (A-weighted)	DAC to LOUT/OUT3 or ROUT/OUT4, R_L=32Ω, AVDD=HPVDD= 2.7V			98		dB
THD (P_O=5mW)				-78		dB
THD+N (P_O=5mW)				-76		dB
Minimum Headphone Resistance	LOUT, ROUT, OUT3, OUT4		15			Ω
SNR (A-weighted)	DAC to Speaker Output (Direct) AVDD=3.0V, SPKVDD=5V, class D, P_O controlled using DAC volume, ACGAIN=DCGAIN=1.67			89		dB
THD (P_O=0.5W)				-76		dB
THD+N (P_O=0.5W)				-74		dB
THD (P_O=0.9W)				-76		dB
THD+N (P_O=0.9W)				-74		dB
SPKVDD PSRR(217Hz)				75		dB
SNR (A-weighted)	DAC to Speaker Output (Direct) AVDD=3.0V, SPKVDD=5V, class AB, P_O controlled using DAC volume			96		dB
THD (P_O=0.2W)				-81		dB
THD+N (P_O=0.2W)				-79		dB
THD (P_O=0.45W)				-70		dB
THD+N (P_O=0.45W)				-68		dB
SPKVDD PSRR(217Hz)				75		dB
DC Offset at Load				5		mV





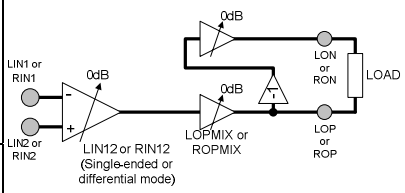
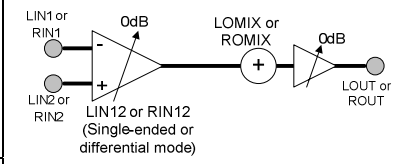
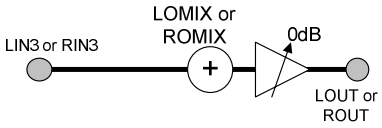
Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Bypass Path Performance (Line Outputs 10kΩ / 50pF load, Headphone Outputs 16Ω load, Speaker Output 8Ω BTL load)						
SNR (A-weighted)	Differential Input on RXP/RXN to Differential Output on OUT3/OUT4, AVDD=HPVDD= 3.0V			110		dB
THD (P_O=5mW)				-74		dB
THD+N (P_O=5mW)				-72		dB
AVDD PSRR (217Hz)				80		dB
HPVDD PSRR (217Hz)				90		dB
DC Offset at Load				5		mV
SNR (A-weighted)	Differential Input on RXP/RXN to Differential Output on OUT3/OUT4, AVDD=HPVDD= 2.7V			108		dB
THD (P_O=5mW)				-73		dB
THD+N (P_O=5mW)				-71		dB
SNR (A-weighted)	RXVOICE via LOMIX or ROMIX to Headphone Outputs, AVDD=HPVDD= 3.0V			100		dB
THD (P_O=5mW)				-73		dB
THD+N (P_O=5mW)				-71		dB
AVDD PSRR (217Hz)				45		dB
HPVDD PSRR (217Hz)				85		dB
SNR (A-weighted)	RXVOICE via LOMIX or ROMIX to Headphone Outputs, AVDD=HPVDD= 2.7V			98		dB
THD (P_O=5mW)				-71		dB
THD+N (P_O=5mW)				-69		dB
SNR (A-weighted)	Line Input to SPKMIX, AVDD=3.0V, SPKVDD=5V, ACGAIN= DCGAIN=1.67, Class D Mode			93		dB
THD (P_O=0.5W)				-87		dB
THD+N (P_O=0.5W)				-85		dB
THD (P_O=0.9W)				-81		dB
THD+N (P_O=0.9W)				-79		dB
AVDD PSRR (217Hz)				45		dB
SPKVDD PSRR(217Hz)				80		dB
SNR (A-weighted)	Line Input to SPKMIX, AVDD=3.0V, SPKVDD=5V, Class AB Mode			101		dB
THD (P_O=0.5W)				-77		dB
THD+N (P_O=0.5W)				-75		dB
AVDD PSRR (217Hz)				45		dB
SPKVDD PSRR(217Hz)				80		dB
DC Offset at Load				5		mV

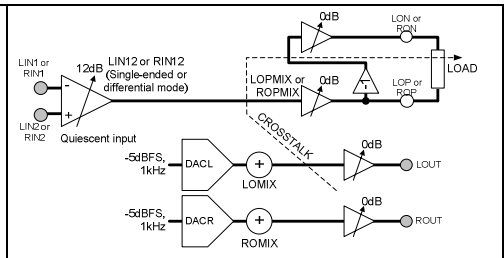
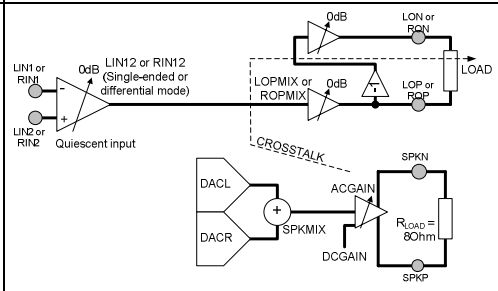
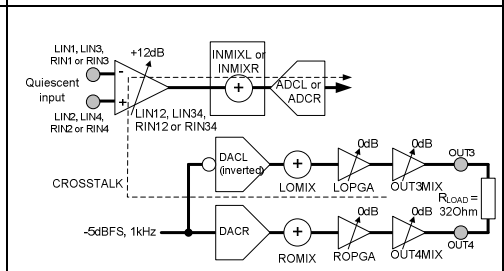
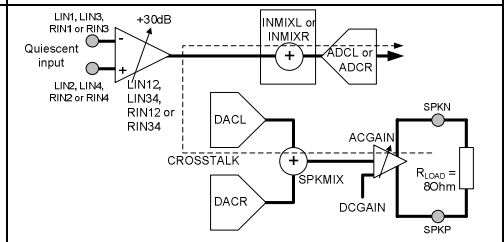
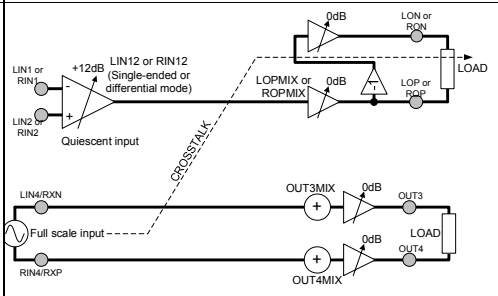
Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SNR (A-weighted)	Input PGA to Differential Line Out, AVDD=3.0V			102		dB
THD (0dB output)				-96		dB
THD+N (0dB output)				-94		dB
AVDD PSRR (217Hz)				45		dB
DC Offset at Load				5		mV
SNR (A-weighted)	Input PGA to Differential Line Out, AVDD=2.7V			100		dB
THD (0dB output)				-95		dB
THD+N (0dB output)				-93		dB
SNR (A-weighted)	Input PGA via LOMIX or ROMIX to LOUT or ROUT, R_L=16Ω, AVDD=HPVDD= 3.0V			102		dB
THD (P_O=20mW)				-80		dB
THD+N (P_O=20mW)				-78		dB
THD (P_O=5mW)				-77		dB
THD+N (P_O=5mW)				-75		dB
AVDD PSRR (217Hz)				45		dB
HPVDD PSRR (217Hz)				85		dB
Crosstalk (L/R)				-95		dB
SNR (A-weighted)	Input PGA via LOMIX or ROMIX to LOUT or ROUT, R_L=16Ω, AVDD=HPVDD= 2.7V			100		dB
THD (P_O=5mW)				-76		dB
THD+N (P_O=5mW)				-74		dB
SNR (A-weighted)	Line Input to Headphones via LOMIX and ROMIX, R_L=16Ω, AVDD=HPVDD= 3.0V			104		dB
THD (P_O=20mW)				-80		dB
THD+N (P_O=20mW)				-78		dB
THD (P_O=5mW)				-77		dB
THD+N (P_O=5mW)				-75		dB
AVDD PSRR (217Hz)				70		dB
HPVDD PSRR (217Hz)				85		dB
Crosstalk (L/R)				-95		dB
SNR (A-weighted)	Line Input to Headphones via LOMIX and ROMIX, R_L=16Ω, AVDD=HPVDD= 2.7V			102		dB
THD (P_O=5mW)				-76		dB
THD+N (P_O=5mW)				-74		dB

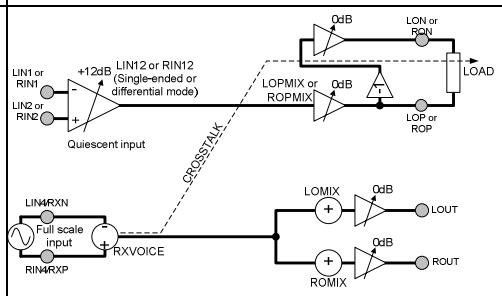
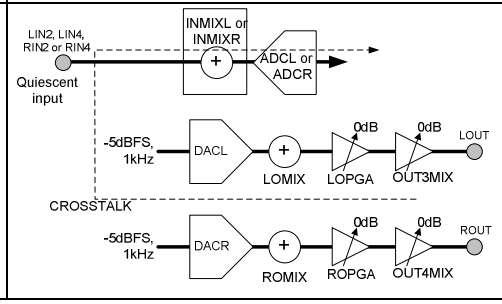
Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Multi-Path Channel Separation					
Headset Voice Call: DAC/Headset to Tx Voice Separation 1kHz 0dBFS DAC playback to LOUT and ROUT; Quiescent input on LIN12 or RIN12 (Gain=+12dB), differential output to LOP/LON or ROP/RON; Measure crosstalk at LOP/LON or ROP/RON output			85		dB
Headset Voice Call: DAC/Speaker to Tx Voice Separation 1kHz 0dBFS DAC playback to speaker, 1W output; Quiescent input on LIN12 or RIN12 (Gain=+12dB), differential output to LOP/LON or ROP/RON; Measure crosstalk at LOP/LON or ROP/RON output			100		dB
PCM Voice Call: Rx Voice to Tx Voice Separation fs=8kHz for ADC and DAC, DAC_SB_FILT=1; -5dBFS differential mono output from DACs to OUT3/OUT4; Quiescent input on input PGA (Gain=+12dB) to ADC via INMIXL or INMIXR; Measure crosstalk at ADC output			90		dB
Speakerphone PCM Voice Call: DAC/Speaker to ADC Separation fs=8kHz for ADC and DAC, DAC_SB_FILT=1; 0dBFS DAC output to speaker (1W output); ADC record from input PGA (Gain=+30dB); Measure crosstalk on ADC output			85		dB
Ear Speaker Voice Call: Tx Voice and Rx Voice Separation 1kHz Full scale differential input on RXP/RXN, output to OUT3/OUT4; Quiescent input on LIN12 or RIN12 (Gain=+12dB), differential output to LOP/LON or ROP/RON; Measure crosstalk at LOP/LON or ROP/RON output			70		dB

Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Headset Voice Call: Tx Voice and Rx Voice Separation 1kHz full scale differential input on RXP/RXN via RXVOICE to LOMIX and ROMIX, output to LOUT and ROUT; Quiescent input on LIN12 or RIN12 (Gain=+12dB), differential output to LOP/LON or ROP/RON; Measure crosstalk at LOP/LON or ROP/RON output			75		dB
Stereo Line Record and Playback: DAC/Headset to ADC Separation -5dBFS input to DACs, playback to LOUT and ROUT1; ADC record from line input; Measure crosstalk on ADC output			90		dB

Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Levels					
VMID Midrail Reference Voltage		-3%	AVDD/2	+3%	V
VREF Buffered Reference Voltage		-3%	AVDD/2	+3%	V
Microphone Bias					
Bias Voltage	3mA load current MBSEL=0	-5%	0.9×AVDD	+5%	V
	3mA load current MBSEL=1	-5%	0.65×AVDD	+5%	V
Bias Current Source				3	mA
Output Noise Density	1kHz to 20kHz		100		nV/√Hz
AVDD PSRR (217Hz)	100mV pk-pk @217Hz on AVDD		45		dB

Test Conditions

DCVDD = 1.8V, HBVDD = MBVDD = I2CVDD = I2S1VDD = I2S2VDD = AVDD = HPVDD = 3.0V, SPKVDD = 5V,
T_A = +25°C, 1kHz signal, fs = 44.1kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output					
Input HIGH Level		0.7xHBVDD 0.7x MBVDD 0.7x I2CVDD 0.7x I2S1VDD 0.7x I2S2VDD			V
Input LOW Level				0.3xHBVDD 0.3x MBVDD 0.3x I2CVDD 0.3x I2S1VDD 0.3x I2S2VDD	V
Output HIGH Level	I_{OL}=1mA	0.9xHBVDD 0.9x MBVDD 0.9x I2CVDD 0.9x I2S1VDD 0.9x I2S2VDD			V
Output LOW Level	I_{OH}=-1mA			0.1xHBVDD 0.1x MBVDD 0.1x I2CVDD 0.1x I2S1VDD 0.1x I2S2VDD	V
Input capacitance			10		pF
Input leakage		-0.9		0.9	µA
FLL					
Input Frequency		32		22000	kHz
Lock time		10		509	Ref Clock Periods
GPIO					
Clock output duty cycle (Integer OPCLKDIV)	SYSCLK=MCLK; OPCLKDIV=0000	35		65	%
	SYSCLK=MCLK; OPCLKDIV=1000	45		55	%
	SYSCLK=FLL output; OPCLKDIV=0000	45		55	%
	SYSCLK=FLL output; OPCLKDIV=1000	45		55	%
Clock output duty cycle (Non-integer OPCLKDIV)	SYSCLK=MCLK; OPCLKDIV=0100	33		66	%
	SYSCLK=FLL output; OPCLKDIV=0100	33		66	%
Interrupt response time for accessory / button detect	Input de-bounced	2^{21} / f_{SYSCLK}		2^{22} / f_{SYSCLK}	s
	Input de-bounced TOCLKSEL=1	2^{19} / f_{SYSCLK}		2^{20} / f_{SYSCLK}	s
	Input not de-bounced		0		s

LDO REGULATOR ELECTRICAL CHARACTERISTICS

Test Conditions

Vin = 3.7V, Vout = 1.8V, T_A = 25°C unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO Regulators - Active LDO Mode					
Input Voltage		2.5		5.5	V
Output Voltage (see notes)		0.9		3.3	V
Regulation accuracy			±4%		V
Dropout voltage	Iout = 150mA, Vout < 1.8V		700		mV
	Iout = 150mA, Vout > 1.8V		200	400	mV
Maximum Load current			150	250	mA
Quiescent current	Iout = 0	27		1% of load	µA
Leakage current			<1		µA
Power supply rejection ratio	1kHz, Vout = 1.8v, 25mA load		-50		dB
	100Hz, Vout = 1.8v, 25mA load				
LDO Regulators - Current Switch Mode					
ON resistance	Vin = 3.7V, <250mA load		700		mΩ

Notes

1. Vin is the LDO supply voltage, connected to LDO1VDD, LDO2VDD, LDO3VDD and LDO4VDD for LDOs1-4 respectively.
2. In addition to the limits noted above, the maximum output voltage, Vout, is also a function of the input voltage. This is a function of the dropout voltage for the applicable operating conditions.

DC-DC CONVERTER ELECTRICAL CHARACTERISTICS

Test Conditions

Vin = 3.7V, Vout = 1.8V, T_A = 25°C unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC Converters					
Input Voltage		2.7		5.5	V
Output Voltage (see notes)		0.85		3.4	V
Output Voltage accuracy (Vin = 3.7V, Vout = 0.85V to 3.4V)	Active Mode; 0.5A		±4%		V
	Standby Mode; 0.1A		±4%		V
	Hibernate/LDO Mode; 5mA		-1.5%, +4.5%		V
Line regulation (Vin = 2.7V to 5.5V; Vout = 1.8V)	Active Mode; 0.5A		±0.5%		V
	Standby Mode; 0.1A		±0.5%		V
	Hibernate/LDO Mode; 5mA		±0.2%		V
Load Regulation	Output current = 1mA to 1A		±0.5%		V
Maximum Load Current (see notes)	Active Mode		600		mA
	Standby Mode		600		mA
	Hibernate/LDO Mode		60		mA
Quiescent current	Active Mode		340		µA
	Standby Mode		120		µA
	Hibernate/LDO Mode		30		µA
Shutdown current			0.01		µA
P-channel On Resistance (R_{DSP})	Vin = 3.7V, Output = 100mA		0.25		Ω
N-channel On Resistance (R_{DSN})	Vin = 3.7V, Output = 100mA		0.2		Ω
P-channel leakage current	Vin = 3.7V, DCnLX = GND		0.1		µA
N-channel leakage current	Vin = 3.7V, DCnLX = 3.7V		0.1		µA
Switching frequency			2.048		MHz

Notes

1. Vin is the DC-DC converter supply voltage, connected to DC1VDD and DC2VDD for DC1 and DC2 respectively.
2. In addition to the limits noted above, the maximum output voltage, Vout, is also a function of the input voltage. This is a function of the P-channel ON Resistance (R_{DSP}) and N-channel On Resistance (R_{DSN}) for the applicable operating conditions.
3. DCnLX is the DC-DC converter output pin DC1LX or DC2LX for DC1 and DC2 respectively.
4. The maximum output current achievable is subject to the current limit of the particular converter being set appropriately, and also the junction temperature of the device.

TYPICAL POWER CONSUMPTION

All data contained within this section is based upon the following test voltage conditions:

Voltages	SPKVDD	HPVDD	AVDD	I2S1VDD	DCVDD	I2CVDD	FLLVDD	HBVDD	VLINE
	3.7000 (5V for DAC to Speaker)	3.00	3.00	1.80	1.80	1.80	3.00	1.80	3.70

LIN2 / RIN2 TO ADC

LIN2/RIN2 to ADC Stereo Record Slave 44.1k

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0001	0.0001	4.0230	0.0496	2.7910	-0.0002	0.0001	0.0000	0.1520	**17.1831**	**17.7456**

LIN2/RIN2 to ADC Stereo Record Slave, 8k

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0000	0.0001	3.8270	0.0104	0.5180	-0.0001	0.0000	-0.0001	0.1520	**12.4328**	**12.9953**

LIN2/RIN2 to ADC Stereo Record Slave, Quiescent, 44.1k

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0001	0.0002	3.9980	0.0336	2.7600	-0.0001	0.0001	-0.0001	0.1520	**17.0239**	**17.5864**

LIN2/RIN2 to ADC Stereo Record Slave, Quiescent, 8k

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0004	0.0000	3.8020	0.0075	0.5100	0.0000	0.0001	0.0000	0.1520	**12.3392**	**12.9017**

LIN2/RIN2 to ADC Stereo Record Master, 44.1k

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0001	0.0001	4.0230	0.2610	2.8130	0.0001	0.0001	-0.0001	0.1520	**17.6033**	**18.1658**

LIN2/RIN2 to ADC Stereo Record Master, 8k

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0000	0.0001	3.8280	0.0487	0.5220	0.0000	0.0001	-0.0001	0.1520	**12.5119**	**13.0745**

LIN2/RIN2 to ADC Stereo Record Master and FLL, 44.1k

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0001	0.0002	4.0250	0.2600	5.1370	-0.0001	0.4010	0.0000	0.1520	**22.9936**	**23.5560**

LIN2/RIN2 to ADC Stereo Record Master and FLL, 8k

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0002	0.0003	3.9600	0.1860	5.1360	-0.0001	0.4270	0.0000	0.1520	**22.7424**	**23.3048**

DAC TO LON/LOP AND RON/ROP

DAC to LON/LOP and RON/ROP Slave 44.1k, 10kΩ

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0001	0.4610	3.9350	0.0121	2.6930	0.0000	0.0000	-0.0001	0.1520	**18.0576**	**18.6201**

DAC to LON/LOP and RON/ROP Slave 8k, 10kΩ

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0001	0.4600	3.8080	0.0022	0.5060	-0.0001	0.0000	0.0001	0.1520	**13.7193**	**14.2819**

DAC to LON/LOP and RON/ROP Master 44.1k, 10kΩ

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0002	0.4610	3.9350	0.2230	2.7150	0.0001	0.0000	0.0000	0.1520	**18.4774**	**19.0398**

DAC to LON/LOP and RON/ROP Master 8k, 10kΩ

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0001	0.4610	3.8090	0.0410	0.5090	-0.0001	0.0001	-0.0001	0.1520	**13.8006**	**14.3631**

DAC to LON/LOP and RON/ROP Master and FLL 44.1k, 10kΩ

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0000	0.4610	3.9340	0.2220	5.0230	-0.0001	0.3990	0.0000	0.1520	**23.8233**	**24.3857**

DAC to LON/LOP and RON/ROP Master and FLL 8k, 10kΩ

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0002	0.4610	3.8920	0.1580	4.9930	0.0000	0.4240	-0.0001	0.1520	**23.6036**	**24.1661**

DAC TO LOUT/ROUT

DAC to LOUT/ROUT Slave 44.1k, 32Ω, 5mW

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0001	11.272	2.9020	0.0117	2.6940	0.0001	0.0001	-0.0001	0.1520	**47.3929**	**47.9555**

DAC to LOUT/ROUT Slave 44.1k, 32Ω, 0.1mW

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0001	1.8270	2.8980	0.0121	2.6930	0.0000	0.0001	0.0000	0.1520	**19.0448**	**19.6072**

DAC to LOUT/ROUT Slave 44.1k, 32Ω, Quiescent

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
-0.0002	0.4640	2.8880	0.0115	2.7360	0.0000	0.0000	-0.0001	0.1520	**15.0022**	**15.5647**

DAC to LOUT/ROUT Slave 8k, 32Ω, 5mW

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0000	11.2740	2.7750	0.0023	0.5050	0.0000	0.0000	-0.0001	0.1520	**43.0603**	**43.6230**

DAC to LOUT/ROUT Slave 8k, 32Ω, 0.1mW

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0000	1.8270	2.7710	0.0023	0.5050	0.0000	0.0000	0.0000	0.1520	**14.7072**	**15.2697**

DAC to LOUT/ROUT Slave 8k, 32Ω, Quiescent

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0000	0.5540	2.7530	0.0021	0.5050	0.0001	0.0001	-0.0001	0.1520	**10.8342**	**11.3967**

DAC TO SPEAKER

DAC to Class AB Speaker Slave 44.1k, 8Ω

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
290.7670	0.0001	1.6890	0.0120	1.7880	0.0000	0.0000	-0.0001	0.1530	**1462.1424**	**1462.7086**

DAC to Class D Speaker Slave 44.1k, 8Ω

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
286.8830	0.0001	2.2590	0.0120	1.7940	0.0000	0.0000	0.0000	0.1530	**1444.4432**	**1445.0094**

DAC to Class AB Speaker Slave 44.1k, 8Ω + 22µH

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
256.8060	0.0002	1.7120	0.0116	1.7570	0.0001	-0.0001	-0.0001	0.1530	**1292.3503**	**1292.9165**

DAC to Class AB Speaker Slave 44.1k, 8Ω + 22µH Quiescent

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
3.9450	0.0000	1.7110	0.0113	1.7680	0.0000	0.0000	0.0000	0.1530	**28.0610**	**28.6271**

DAC to Class D Speaker Slave 44.1k, 8Ω + 22µH

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
213.1460	0.0001	2.2250	0.0116	1.7660	0.0000	0.0000	0.0000	0.1530	**1075.6050**	**1076.1712**

DAC to Class D Speaker Slave 44.1k, 8Ω + 22µH Quiescent

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
6.5820	0.0002	2.2560	0.0114	1.7860	0.0000	0.0000	-0.0001	0.1530	**42.9140**	**43.4802**

LOW POWER STATES

Device Default, No Clocks

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0001	0.0004	0.0078	0.0002	0.0003	0.0003	0.0003	0.0003	0.1512	**0.0274**	**0.5875**

Device Default, Clocks Applied

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0003	0.0004	0.0076	0.0112	0.0002	0.0001	0.0002	0.0002	0.1512	**0.0463**	**0.6062**

CODEC Soft Shutdown (CODEC_SOFTSD = 1, see Table 18 Enabling the Audio CODEC)

SPKVDD Current (mA)	HPVDD Current (mA)	AVDD Current (mA)	I2S1VDD Current (mA)	DCVDD Current (mA)	I2CVDD Current (mA)	FLLVDD Current (mA)	HBVDD Current (mA)	VLINE Current (mA)	Total Power Without VLINE, HBVDD (mW)	Total Power With VLINE, HBVDD (mW)
0.0003	0.0003	0.0075	0.0003	-0.0001	0.0000	0.0000	0.0001	0.1512	**0.0252**	**0.5848**

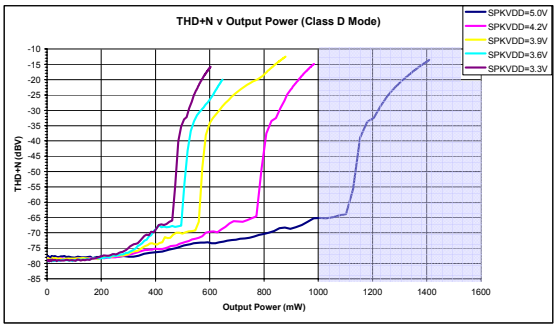
TYPICAL PERFORMANCE DATA

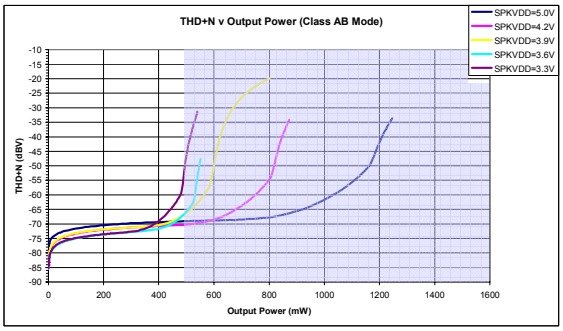
SPEAKER DRIVER PERFORMANCE

Typical THD+N performance of the Speaker Driver is shown below for Class D mode and for Class AB mode. Data is provided for five typical SPKVDD voltages.

Load R_L = 8Ω, Frequency = 1kHz

Note that it is not recommended to operate Class D mode above 1W or Class AB mode above 0.5W due to high thermal dissipation.

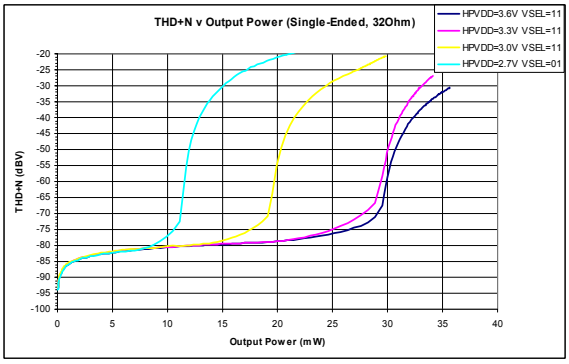


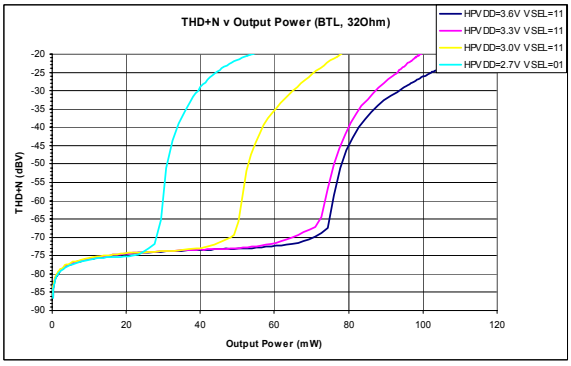


HEADPHONE DRIVER PERFORMANCE

Typical THD+N performance of the Headphone Drivers is shown below for single-ended configuration (LOUT and ROUT) and for BTL configuration (LOUT/OUT3 and ROUT/OUT4). Data is provided for four typical HPVDD voltages, together with the appropriate VSEL value.

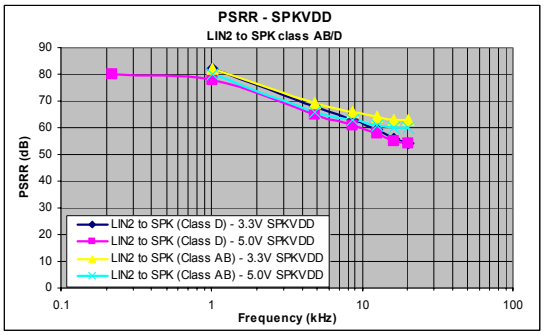
Load R_L = 32Ω, Frequency = 1kHz

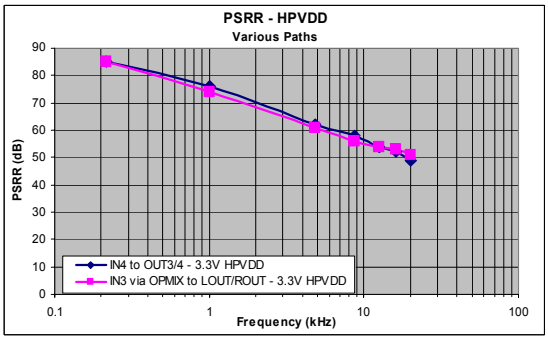


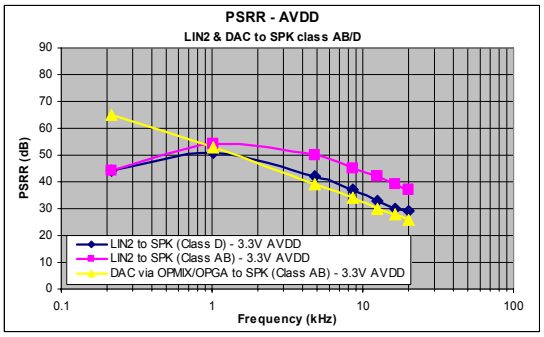


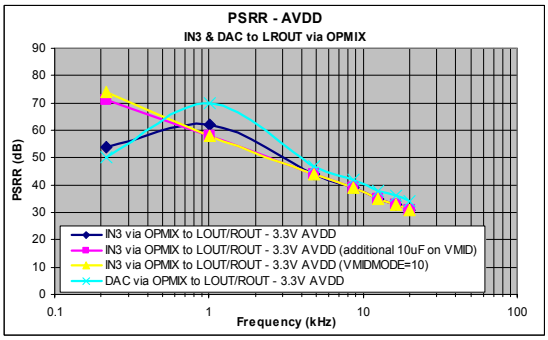
PSRR PERFORMANCE

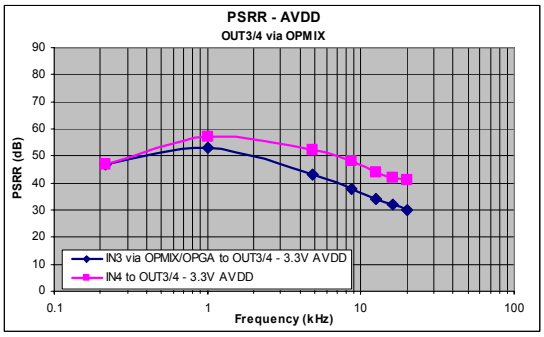
PSRR performance for typical audio paths is illustrated in the graphs below.

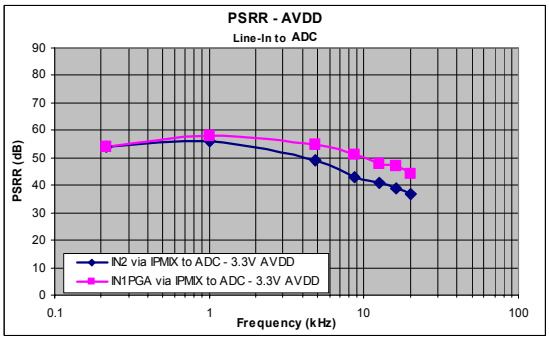


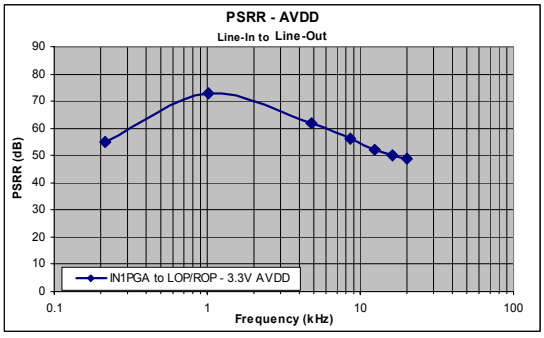


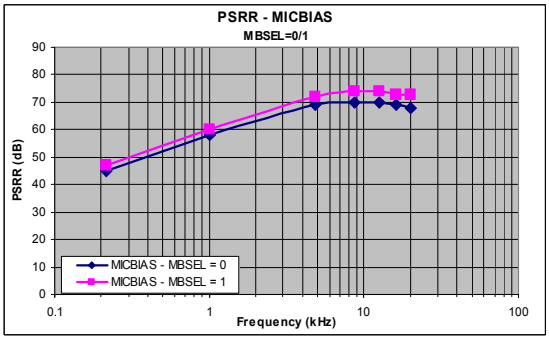












SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

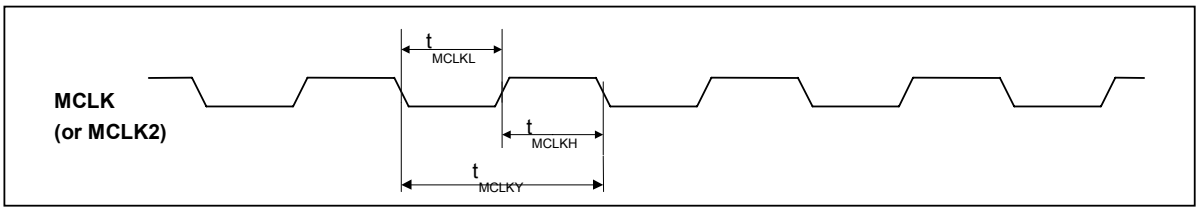


Figure 2 System Clock Timing Requirements

Test Conditions

DCVDD=1.8V, HBVDD=MBVDD=I2CVDD=I2S1VDD=I2S2VDD=AVDD=3.0V, SPKVDD=5V, GND=AGND=SPKGND=0V, T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK or MCLK2 cycle time	T_{MCLKY}		40			ns
MCLK or MCLK2 duty cycle		= T_{MCLKH}/T_{MCLKL}	60:40		40:60	

AUDIO INTERFACE TIMING – MASTER MODE

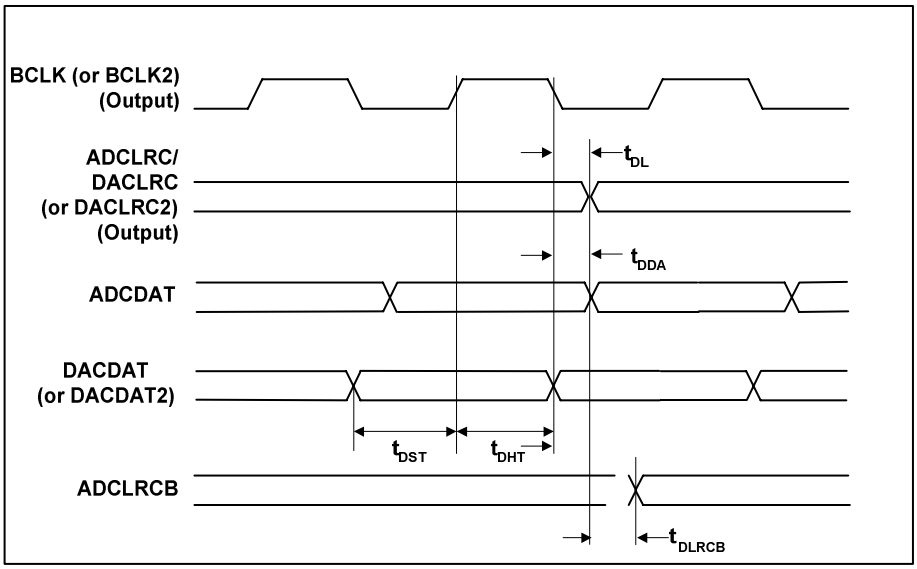


Figure 3 Digital Audio Data Timing - Master Mode (see Control Interface)

Test Conditions

DCVDD=1.8V, HBVDD=MBVDD=I2CVDD=I2S1VDD=I2S2VDD=AVDD=3.0V, SPKVDD=5V, GND=AGND=SPKGND=0V, T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
ADCLRC/ DACLRC (or DACLRC2) propagation delay from BCLK (or BCLK2) falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			10	ns
DACDAT (or DACDAT2) setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT (or DACDAT2) hold time from BCLK rising edge	t_{DHT}	10			ns
ADCLRC to ADCLRCB delay	t_{DLRCB}			10	ns

AUDIO INTERFACE TIMING – SLAVE MODE

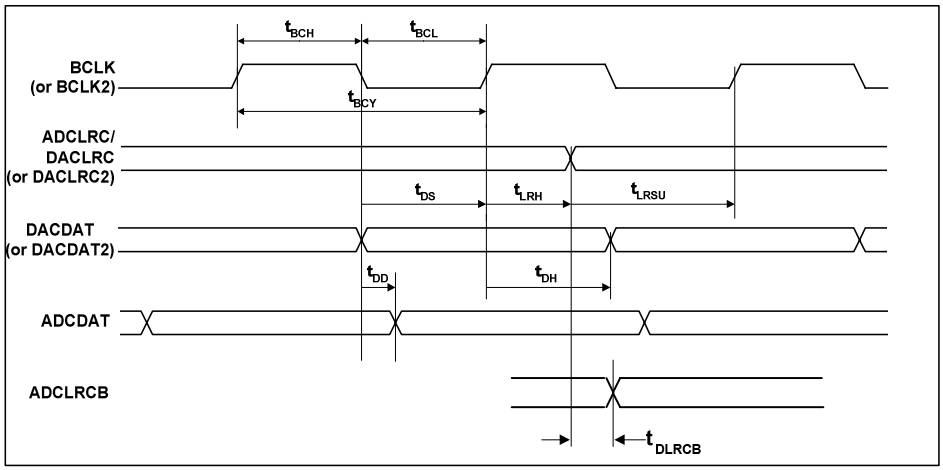


Figure 4 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=1.8V, HBVDD=MBVDD=I2CVDD=I2S1VDD=I2S2VDD=AVDD=3.0V, SPKVDD=5V, GND=AGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
BCLK (or BCLK2) cycle time	t_{BCY}	80			ns
BCLK (or BCLK2) pulse width high	t_{BCH}	32			ns
BCLK (or BCLK2) pulse width low	t_{BCL}	32			ns
ADCLRC/ DACLRC (or DACLRC2) set-up time to BCLK (or BCLK2) rising edge	t_{LRSU}	10			ns
ADCLRC/ DACLRC (or DACLRC2) hold time from BCLK (or BCLK2) rising edge	t_{LRH}	10			ns
DACDAT (or DACDAT2) hold time from BCLK (or BCLK2) rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			10	ns
DACDAT (or DACDAT2) set-up time to BCLK (or BCLK2) rising edge	t_{DS}			40	ns
ADCLRC to ADCLRCB delay	t_{DLRCB}			10	ns

Note:

BCLK (or BCLK2) period should always be greater than or equal to MCLK (or MCLK2) period.

AUDIO INTERFACE TIMING – TDM MODE

In TDM mode, it is important that two ADC devices do not attempt to drive the ADCDAT pin simultaneously. The timing of the WM8400 ADCDAT tri-stating at the start and end of the data transmission is described in Figure 5 and the table below.

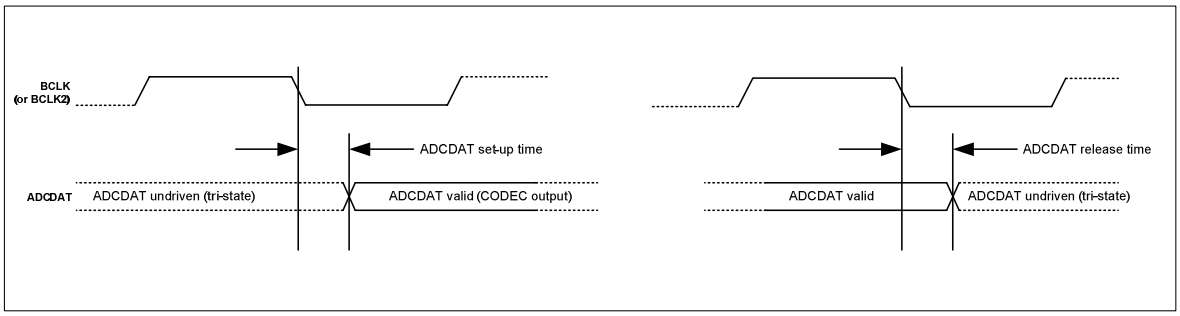


Figure 5 Digital Audio Data Timing - TDM Mode

Test Conditions

HBVDD=MBVDD=I2CVDD=I2S1VDD=I2S2VDD=AVDD=3.0V, SPKVDD=5V, GND=AGND=SPKGND=0V,
T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
ADCDAT setup time from BCLK falling edge	DCVDD = 3.6V		2		ns
	DCVDD = 1.8V		15		ns
ADCDAT release time from BCLK falling edge	DCVDD = 3.6V		2		ns
	DCVDD = 1.8V		15		ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

2-wire mode is selected by connecting the MODE pin low.

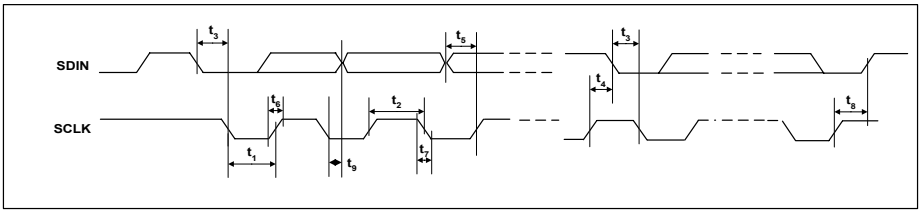


Figure 6 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, HBVDD=MBVDD=I2CVDD=I2S1VDD=I2S2VDD=AVDD=3.0V, SPKVDD=5V,
GND=AGND=HPGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 3-WIRE MODE

3-wire mode is selected by connecting the MODE pin high.

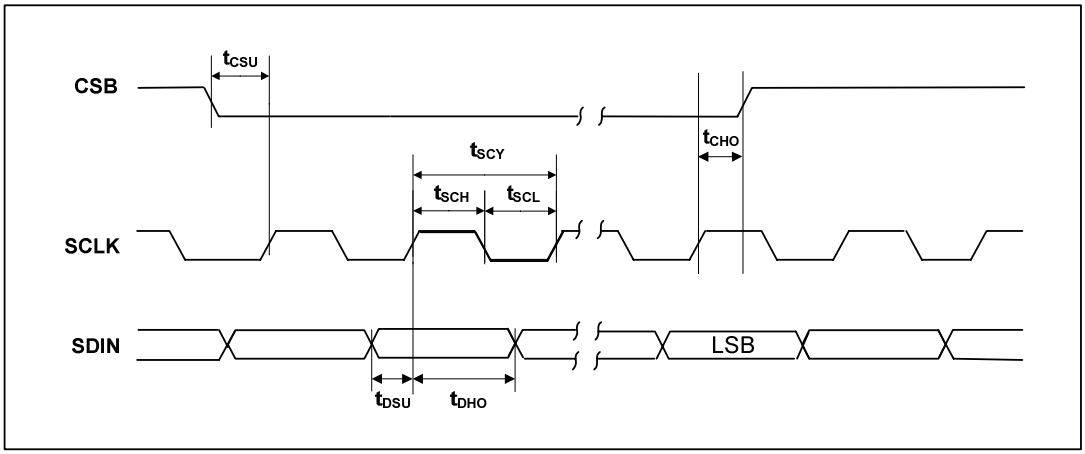


Figure 7 Control Interface Timing – 3-Wire Serial Control Mode (Write Cycle)

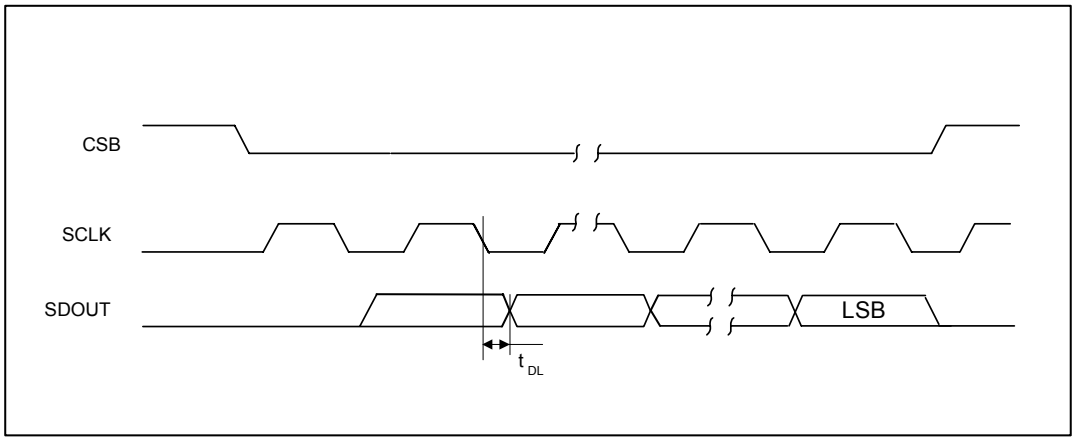


Figure 8 Control Interface Timing - 3-Wire Serial Control Mode (Read Cycle)

Test Conditions

DCVDD=1.8V, HBVDD=MBVDD=I2CVDD=I2S1VDD=I2S2VDD=AVDD=3.0V, SPKVDD=5V,
GND=AGND=HPGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
CSB falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK rising edge to CSB rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SDIN to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

CODEC POWER ON RESET CIRCUIT

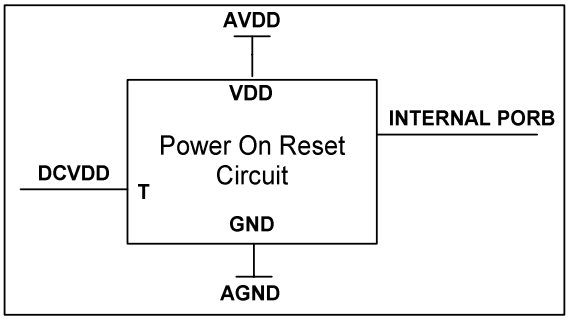


Figure 9 Internal Power on Reset Circuit Schematic

The WM8400 includes an internal CODEC Power-On-Reset Circuit, as shown in Figure 9, which is used to reset the CODEC digital logic into a default state after power up. The CODEC POR circuit is powered from AVDD and monitors DCVDD. It asserts PORB low if AVDD or DCVDD is below a minimum threshold. In a typical application, DCVDD may be supplied from one of the integrated LDO Regulators.

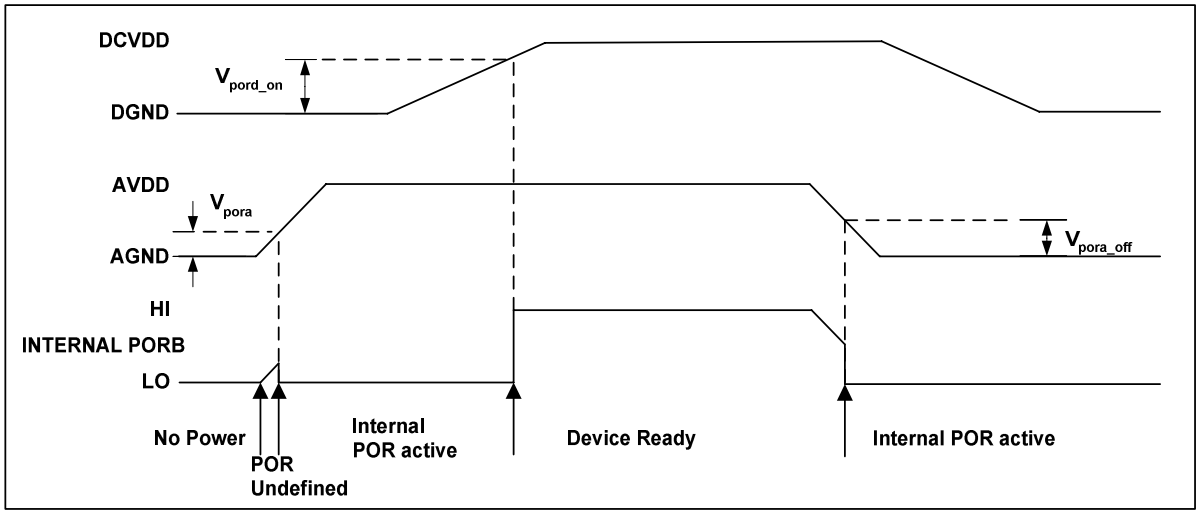


Figure 10 Typical CODEC Power up Sequence where AVDD is Powered before DCVDD

Figure 10 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. After AVDD has reached its full supply level, DCVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold V_{pora_off}.

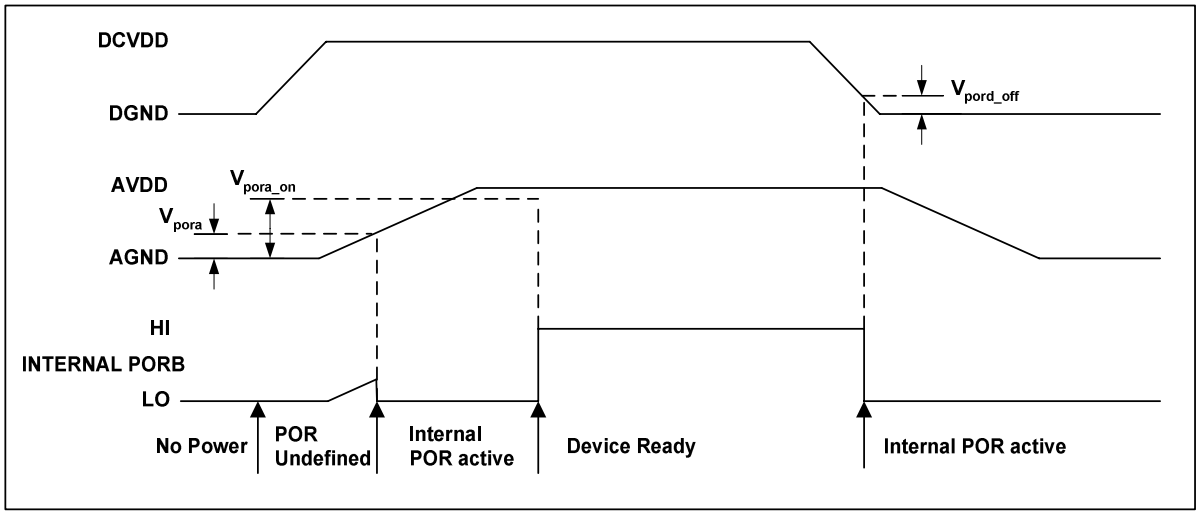


Figure 11 Typical Power up Sequence where DCVDD is Powered before AVDD

Figure 11 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
Vpora		0.6		V
Vpora_on		1.65		V
Vpora_off		1.5		V
Vpord_on		0.92		V
Vpord_off		0.9		V

Table 1 Typical POR Operation (simulated values)

Notes:

1. If AVDD and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.
2. The chip will enter reset at power down when AVDD or DCVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.
3. The minimum t_{por} period is maintained even if DCVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

CONTROL INTERFACE

The WM8400 is controlled by writing to its control registers. Readback is available for certain registers, including device ID, power management registers and some GPIO status bits. The control interface can operate as either a 2-wire or 3-wire control interface, with additional variants as detailed below:

1. 2-wire
   - open-drain
2. 3-wire
   - push 0/1
   - open drain

Readback is provided on the bi-directional pin SDIN in 2-wire and 3-wire modes.

CONTROL INTERFACE POWER DOMAIN

Operation of the Control Interface requires an appropriate power supply to be connected to the I2CVDD power domain. This supply is referenced to GND.

The operating range for this supply is detailed in the “Recommended Operating Conditions” section.

If the I2C bus is shared in an application with other devices, the I2CVDD must be supplied to the Wolfson device at all times the bus is active.

SELECTION OF CONTROL MODE

The MODE pin determines the 2-wire or 3-wire mode as shown in Table 2.

MODE	INTERFACE FORMAT
Low	2 wire
High	3- wire

Table 2 Control Interface Mode Selection

2-WIRE SERIAL CONTROL MODE

The WM8400 is controlled by writing to registers through a 2-wire serial control interface. A control word consists of 24 bits. The first 8 bits (B23 to B16) are address bits that select which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 8-bit address of each register in the WM8400). The default device address is 0011000 (0x30h)

The WM8400 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8400, then the WM8400 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is ‘1’ when operating in write only mode, the WM8400 returns to the idle condition and wait for a new start condition and valid address.

The WM8400 supports a multitude of read and write operations, which are:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

These modes are shown in the section below. Terminology used in the following figures:

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge	
P	Stop Condition	
$R\overline{W}$	ReadNotWrite	0 = Write 1 = Read

Table 3 Terminology

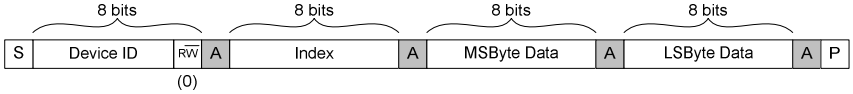


Figure 12 2-Wire Serial Control Interface (single write)

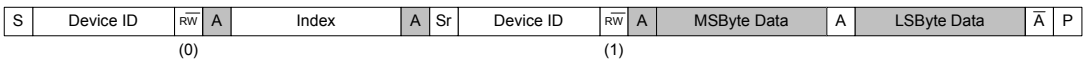


Figure 13 2-Wire Serial Control Interface (single read)

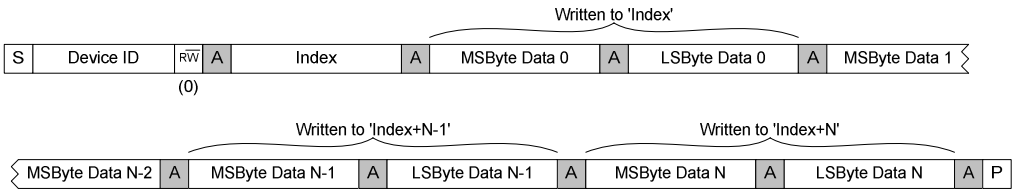


Figure 14 2-Wire Serial Control Interface (multiple write using auto-increment)

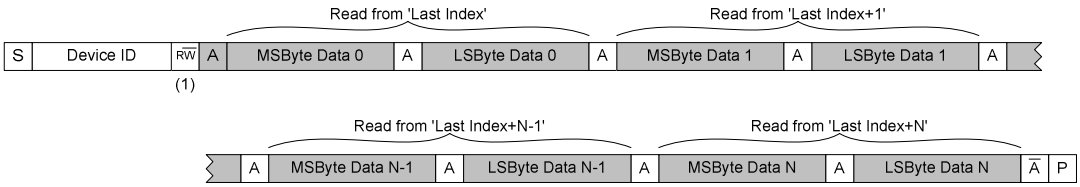


Figure 15 2-Wire Serial Control Interface (multiple read using auto-increment)

In 2-wire mode, the WM8400 has two possible device addresses, which can be selected using the NCSADDR pin.

NCSADDR STATE	DEVICE ADDRESS
Low	0011000 (0 x **30**h)
High	0011010 (0 x **34**h)

Table 4 2-Wire Control Interface Address Selection

Auto-increment mode is only supported when enabled by setting the AUTOINC register bit.

Alert Response Address protocol is supported by the WM8400 when the ARA_ENA register bit is set. This function enables a bus controller to poll multiple devices on the I2C bus simultaneously in order to respond to Interrupt events efficiently. The WM8400 device address used by this protocol is set as described in Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R75 (4Bh)	3	AUTOINC	1b	Enable Auto-Increment function (2-wire I2C mode) 0 = Disabled 1 = Enabled
	2	ARA_ENA	0b	Enable Alert Response Address function (2-wire I2C mode) 0 = Disabled 1 = Enabled

Table 5 2-Wire Control Interface Configuration

3-WIRE SERIAL CONTROL MODE

The WM8400 is controlled by writing to registers through a 3-wire serial control interface. A control word consists of 24 bits. The first bit is the read/write bit (R/W), which is followed by 7 address bits (A6 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

In 3-wire control mode, the SPI_CFG register bit can be used to select between push 0/1 and open-drain modes, as described in Table 6 below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R75 (4Bh)	1	SPI_CFG	0b	3-wire Read mode configuration 0 = CMOS output 1 = Open-drain

Table 6 3-Wire Control Interface Configuration

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on NCSADDR latches in a complete control word consisting of the last 24 bits.

In Write operations (R/W=0), all SDIN bits are driven by the controlling device.

In Read operations (R/W=1), the SDIN pin is driven by the controlling device to clock in the register address, after which the WM8400 drives the SDIN pin to output the applicable data bits.

The 3-wire control mode timing is illustrated in Figure 16.

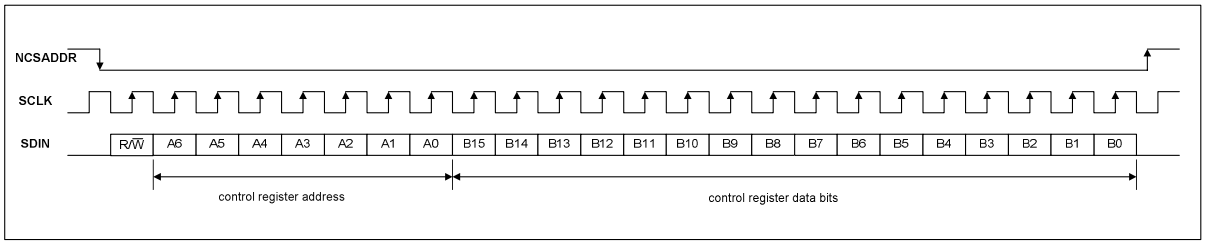


Figure 16 3-Wire Serial Control Interface

CLOCKING AND SAMPLE RATES

The internal clocks for the ADCs, DACs, DSP core functions, digital audio interface and Class D switching amplifier are all derived from a common internal clock source, SYSCLK. This clock is enabled by register bit SYSCLK_ENA. Note that many of the analogue audio circuits of the WM8400 can be operated without SYSCLK enabled.

SYSCLK can either be derived directly from MCLK, or may be generated from a Frequency Locked Loop (FLL) using an external reference. Many commonly-used audio sample rates can be derived directly from typical MCLK frequencies; the FLL provides additional flexibility to generate a wide range of SYSCLK frequencies from the available external reference. An alternative MCLK input may be selected via the GPIO2/MCLK2 pin. All clock configurations must be set up before enabling playback to avoid glitches.

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, using ADC_CLKDIV and DAC_CLKDIV. These fields must be set according to the required sampling frequency and depending on the selected clocking mode (AIF_LRCLKRATE).

In master mode, BCLK is also derived from SYSCLK via a programmable division set by BCLK_DIV. In the case where the ADCs and DACs are operating at different sample rates, BCLK must be set according to whichever is the faster rate. The ADCLRC and DACLRC signals do not automatically match the ADC and DAC sample rates; these must be configured using ADCLRC_RATE and DACLRC_RATE as described under “Digital Audio Interface Control”.

A clock (OPCLK) derived from SYSCLK can be output on the GPIO pins to provide clocking for other parts of the system. This clock is enabled by OPCLK_ENA and its frequency is set by OPCLKDIV.

A slow clock (TOCLK) derived from SYSCLK can be used to de-bounce the button/accessory detect inputs, and to set the timeout period for volume updates when zero-cross detect is used. This clock is enabled by TOCLK_ENA and its frequency is set by TOCLK_RATE.

The Class D switching amplifier requires a clock; by default, this is derived from SYSCLK via a programmable divider DCLKDIV. Alternatively, the Class D amplifier clock may be derived from the WM8400 internal 600kHz clock. (This clock is associated with the DC-DC converters.)

Table 7 to Table 13 show the clocking and sample rate controls for MCLK input, BCLK output (in master mode), ADCs, DACs, class D outputs and GPIO clock output. The overall clocking scheme for the WM8400 is illustrated in Figure 17.

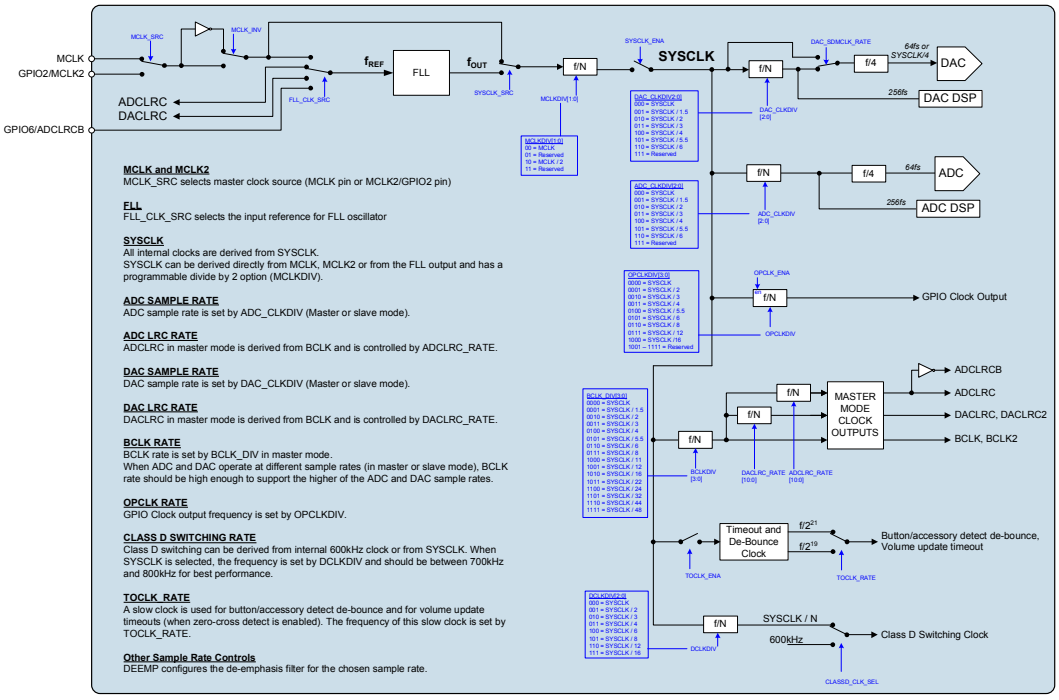


Figure 17 CODEC Clocking Scheme

SYSCLK CONTROL

The MCLK_SRC bit is used to select the MCLK source. The source may be either MCLK or GPIO2/MCLK2. The selected source may also be inverted by setting register bit MCLK_INV. Note that it is not recommended to change the control bit MCLK_INV while the WM8400 is processing data as this may lead to clock glitches and signal pop and clicks.

The SYSCLK_SRC bit is used to select the source for SYSCLK. The source may be either the selected MCLK source or the FLL output. The selected source is divided by the SYSCLK pre-divider MCLK_DIV to generate SYSCLK. The selected source may also be adjusted by the MCLK_DIV divider. These register fields are described in Table 7. See "FLL" for more details of the Frequency Locked Loop clock generator.

The WM8400 supports glitch-free MCLK and SYSCLK source selection. When both clock sources are running and MCLK_SRC or SYSCLK_SRC is modified to select one of these clocks, a glitch-free clock transition will take place. The de-glitching circuit will ensure that the minimum pulse width will be no less than the pulse width of the faster of the two clock sources.

When the initial clock source is to be disabled before changing to the new clock source, the CLK_FORCE bit must also be used to force the clock source transition to take place. In this case, glitch-free operation cannot be guaranteed.

The SYSCLK is enabled by register bit SYSCLK_ENA.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h)	14	SYSCLK_ENA (rw)	0b	SYSCLK enable 0 = disabled 1 = enabled
R8 (08h)	15	MCLK_SRC	0b	MCLK Source Select 0 = MCLK pin 1 = GPIO2/MCLK2 pin
	14	SYSCLK_SRC	0b	SYSCLK Source Select 0 = MCLK (or MCLK2 if MCLK_SRC=1) 1 = FLL output
	13	CLK_FORCE	0b	Forces Clock Source Selection 0 = Existing SYSCLK source (MCLK, MCLK2 or FLL output) must be active when changing to a new clock source. 1 = Allows existing MCLK source to be disabled before changing to a new clock source.
	12:11	MCLK_DIV [1:0]	00b	SYSCLK Pre-divider. Clock source (MCLK, MCLK2 or FLL output) will be divided by this value to generate SYSCLK. 00 = Divide SYSCLK by 1 01 = Reserved 10 = Divide SYSCLK by 2 11 = Reserved
	10	MCLK_INV	0b	MCLK Invert 0 = Master clock (MCLK or MCLK2) not inverted 1 = Master clock (MCLK or MCLK2) inverted

Table 7 MCLK and SYSCLK Control

ADC / DAC SAMPLE RATES

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, by setting the register fields ADC_CLKDIV and DAC_CLKDIV. These fields must be set according to the SYSCLK frequency, and according to the selected clocking mode.

Two clocking modes are provided - Normal Mode (AIF_LRCLKRATE = 0) allows selection of the commonly used sample rates from typical audio system clocking frequencies (eg. 12.288MHz); USB Mode (AIF_LRCLKRATE = 1) allows many of these sample rates to be generated from a 12MHz USB clock. Depending on the available clock sources, the USB mode may be used to save power by supporting 44.1kHz operation without recourse to the FLL.

The AIF_LRCLKRATE field must be set as described in Table 8 to ensure correct operation of internal functions according to the SYSCLK / Fs ratio. Table 9 describes the available sample rates using four different common MCLK frequencies.

In Normal mode, the programmable division set by ADC_CLKDIV must ensure that a 256 * ADC Fs clock is generated for the ADC DSP. DAC_CLKDIV must ensure that a 256 * DAC Fs clock is generated for the DAC DSP.

In USB mode, the programmable division set by ADC_CLKDIV must ensure that a 272 * ADC Fs clock is generated for the ADC DSP. DAC_CLKDIV must ensure that a 272 * DAC Fs clock is generated for the DAC DSP.

Note that in USB mode, the ADC / DAC sample rates do not match exactly with the commonly used sample rates (e.g. 44.118 kHz instead of 44.100 kHz). At most, the difference is less than 0.5%. Data recorded at 44.100 kHz sample rate and replayed at 44.118 kHz will experience a slight (sub 0.5%) pitch shift as a result of this difference. Note also that the USB mode cannot be used to generate a 48kHz samples rate from a 12MHz MCLK; the FLL should be used in this case.

In low sample rate modes (eg. 8kHz voice), the SNR is liable to be degraded if the typical 64fs DAC clocking rate is used (see Figure 17). In this case, it may be possible to improve the SNR by raising the DAC clocking rate by setting the DAC_SDMCLK_RATE register field, causing the DAC clocking rate to be set equal to SYSCLK/4. The DAC_CLKDIV field must still be set as described above to derive the correct clock for the DAC DSP. In 8kHz voice applications, in systems where SYSCLK > 256fs (or 272fs when applicable), setting DAC_SDMCLK_RATE will result in the SNR performance being improved. Note that setting DAC_SDMCLK_RATE will result in an increase in power consumption.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h)	7:5	ADC_CLKDIV [2:0]	000b	ADC Sample Rate Divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2.0 011 = SYSCLK / 3.0 100 = SYSCLK / 4.0 101 = SYSCLK / 5.5 110 = SYSCLK / 6.0 111= Reserved
	4:2	DAC_CLKDIV [2:0]	000b	DAC Sample Rate Divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2.0 011 = SYSCLK / 3.0 100 = SYSCLK / 4.0 101 = SYSCLK / 5.5 110 = SYSCLK / 6.0 111= Reserved
R11 (0Bh)	13	DAC_SDMCLK_ RATE	0b	DAC clocking rate 0 = Normal operation (64fs) 1 = SYSCLK/4
	10	AIF_LRCLKRATE	0b	LRCLK Rate 0 = Normal mode (256 * fs) 1 = USB mode (272 * fs)

Table 8 ADC / DAC Sample Rate Control

SYSCLK	ADC / DAC SAMPLE RATE DIVIDER	CLOCKING MODE	ADC / DAC SAMPLE RATE
12.288 MHz	000 = SYSCLK / 1	Normal Mode (256 * Fs)	48 kHz
	001 = SYSCLK / 1.5		32 kHz
	010 = SYSCLK / 2		24 kHz
	011 = SYSCLK / 3		16 kHz
	100 = SYSCLK / 4		12 kHz
	101 = SYSCLK / 5.5		Not used
	110 = SYSCLK / 6		8 kHz
	111 = Reserved		Reserved
11.2896 MHz	000 = SYSCLK / 1	Normal Mode (256 * Fs)	44.1 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		22.05 kHz
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		11.025 kHz
	101 = SYSCLK / 5.5		8.018 kHz
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved
12 MHz	000 = SYSCLK / 1	USB Mode (272 * Fs)	44.118 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		22.059 kHz
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		11.029 kHz
	101 = SYSCLK / 5.5		8.021 kHz
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved
2.048 MHz	000 = SYSCLK / 1	Normal Mode (256 * Fs)	8 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		Not used
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		Not used
	101 = SYSCLK / 5.5		Not used
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved

Table 9 ADC and DAC Sample Rates

BCLK CONTROL

In Master Mode, BCLK is derived from SYSCLK via a programmable division set by BCLK_DIV, as described in Table 10. BCLK_DIV must be set to an appropriate value to ensure that there are sufficient BCLK cycles to transfer the complete data words from the ADCs and to the DACs.

In Slave Mode, BCLK is generated externally and appears as an input to the CODEC. The host device must provide sufficient BCLK cycles to transfer complete data words to the ADCs and DACs.

Note that, although the ADC and DAC can run at different sample rates, they will normally share the same bit clock pin BCLK. In the case where different ADC / DAC sample rates are used, the BCLK frequency should be set according to the higher of the ADC / DAC bit rates. Note that it is possible for the ADC and DAC to use independent bit clocks when using the Dual Audio Interface capability - see "Digital Audio Interface".

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h)	4:1	BCLK_DIV [3:0]	0100b	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 = SYSCLK / 32 1110 = SYSCLK / 44 1111 = SYSCL:K / 48

Table 10 BCLK Control

OPCLK CONTROL

A clock output (OPCLK) derived from SYSCLK may be output via GPIO1 to GPIO6. This clock is enabled by register bit OPCLK_ENA, and its frequency is controlled by OPCLKDIV.

This output of this clock is also dependent upon the GPIO register settings described under "General Purpose Input/Output".

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h)	12:9	OPCLKDIV [3:0]	0000b	GPIO Output Clock Divider 0000 = SYSCLK 0001 = SYSCLK / 2 0010 = SYSCLK / 3 0011 = SYSCLK / 4 0100 = SYSCLK / 5.5 0101 = SYSCLK / 6 0110 = SYSCLK / 8 0111 = SYSCLK / 12 1000 = SYSCLK / 16 1001 to 1111 = Reserved
R3 (03h)	11	OPCLK_ENA (rw)	0b	GPIO Clock Output Enable 0 = disabled 1 = enabled

Table 11 OPCLK Control

CLASS D SWITCHING CLOCK

The Class D switching clock is derived either from SYSCLK or directly from the WM8400 internal 600kHz oscillator. The source is selected by CLASSD_CLK_SEL. When SYSCLK is used as the Class D clock source, the clock rate is determined by register field DCLKDIV as described in Table 12. This clock should be set to between 700kHz and 800kHz for optimum performance. The class D switching clock should not be disabled when the speaker output is active, as this will prevent the speaker outputs from functioning. The class D switching clock frequency should not be altered while the speaker output is active as this may generate an audible click.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h)	8:6	DCLKDIV [2:0]	111b	Class D Clock Divider 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16
R35 (23h)	7	CLASSD_CLK_ SEL	0b	Class D Clock Source 0 = Derived from SYSCLK (via DCLKDIV) 1 = 600kHz oscillator

Table 12 DCLK Control

TOCLK CONTROL

A slow clock (TOCLK) is derived from SYSCLK to enable input de-bouncing and volume update timeout functions. This clock is enabled by register bit TOCLK_ENA, and its frequency is controlled by TOCLK_RATE, as described in Table 13.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h)	15	TOCLK_RATE	0b	Timeout Clock Rate (Selects clock to be used for volume update timeout and GPIO input de-bounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)
	14	TOCLK_ENA	0b	Timeout Clock Enable (This clock is required for volume update timeout and GPIO input de-bounce) 0 = disabled 1 = enabled

Table 13 TOCLK Control

USB MODE

It is possible to reduce power consumption in the WM8400 by disabling the FLL in some applications. One such application is when SYSCLK is generated from a 12MHz USB clock source. Setting the AIF_LRCLKRATE bit as described earlier (see "ADC / DAC Sample Rates") allows approximate sample rate close to 44.1kHz to be generated with no additional FLL power consumption.

In this configuration, SYSCLK must be driven directly from MCLK (or MCLK2) and by disabling the FLL. This is achieved by setting SYSCLK_SRC=0, FLL_ENA=0 and FLL_OSC_ENA=0.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh)	10	AIF_LRCLKRATE	0b	LRCLK Rate 0 = Normal mode (256 * fs) 1 = USB mode (272 * fs)

Table 14 USB Mode Control

FREQUENCY LOCKED LOOP (FLL)

The integrated FLL can be used to generate SYSCLK from a wide variety of different reference sources and frequencies. The FLL can use either the MCLK or DACLRC input as its reference, which may be a high frequency (eg. 12.288MHz) or low frequency (eg. 32,768kHz) reference. The FLL is tolerant of jitter and may be used to generate a stable SYSCLK from a less stable input signal. The FLL characteristics are summarised in "Electrical Characteristics".

The analogue and digital portions of the FLL may be enabled independently via FLL_OSC_ENA and FLL_ENA. When initialising the FLL, the analogue circuit must be enabled first by setting FLL_OSC_ENA. The digital circuit may then be enabled on the next register write or later. When changing FLL settings, it is recommended that the digital circuit be disabled via FLL_ENA and then re-enabled after the other register settings have been updated. When changing the input reference frequency F_{REF}, it is recommended that the FLL be reset by setting FLL_ENA to 0.

The field FLL_CTRL_RATE controls internal functions within the FLL; it is recommended that only the default setting be used for this parameter. FLL_TRK_GAIN controls the internal loop gain and should be set to the recommended value.

The FLL output frequency is directly determined from FLL_FRATIO, FLL_OUTDIV and the real number represented by FLL_N and FLL_K. The field FLL_N is an integer (LSB = 1); FLL_K is the fractional portion of the number (MSB = 0.5). The fractional portion is only valid when enabled by the field FLL_FRAC. It is recommended that FLL_FRAC is enabled at all times.

The FLL frequency is determined according to the following equation:

$$F_{OUT} = (F_{VCO} / FLL\_OUTDIV)$$

$$F_{VCO} = (F_{REF} \times N.K \times FLL\_FRATIO)$$

F_{VCO} must be in the range 90-100 MHz. The value of FLL_OUTDIV should be selected as follows according to the desired output F_{OUT}.

OUTPUT FREQUENCY F_{OUT}	FLL_OUTDIV
2.8125 MHz - 3.125 MHz	4h (divide by 32)
5.625 MHz - 6.25 MHz	3h (divide by 16)
11.25 MHz - 12.5 MHz	2h (divide by 8)
22.5 MHz - 25 MHz	1h (divide by 4)

Table 15 Choice of FLL_OUTDIV

Note that the output frequencies that do not lie within the ranges quoted above cannot be guaranteed across the full range of device operating temperatures.

Once F_{VCO} has been determined, the value of FLL_FRATIO should be selected in accordance with the recommendations in Table 16. The value of N.K can then be determined using the equation above. FLL_REF_FREQ should be set as described in Table 16.

For best performance, FLL Fractional Mode should always be used. Therefore, if the calculations yield an integer value of N.K, then it is recommended to adjust FLL_FRATIO in order to obtain a non-integer value of N.K. It is also recommended for best audio performance, that high input clocks frequencies (above 1MHz), are used.

The register fields that control the FLL are described in Table 16. Example settings for a variety of reference frequencies and output frequencies are shown in Table 17.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) Power Management 2	15	FLL_ENA	0	FLL Digital enable 0 = FLL disabled 1 = FLL enabled FLL_OSC_ENA must be enabled before enabling FLL_ENA. The order is important.
R60 (3Ch) FLL Control 1	12	FLL_REF_FREQ	1	Low frequency reference locking 0 = Lock achieved after 509 ref clks (Recommended for Reference clock > 48kHz) 1 = Lock achieved after 49 ref clks (Recommended for Reference clock <= 48kHz)
	11:10	FLL_CLK_SRC [1:0]		FLL Clock source 00 = MCLK 01 = DAC LRCLK 10 = ADC LRCLK 11 = GPIO6
	9	FLL_FRAC	0	Fractional enable 0 = Integer Mode 1 = Fractional Mode 1 recommended in all cases
	8	FLL_OSC_ENA	0	FLL Analogue enable 0 = FLL disabled 1 = FLL enabled FLL_OSC_ENA must be enabled before enabling FLL_ENA. The order is important.
	7:5	FLL_CTRL_RATE [2:0]	0h	Frequency of the FLL control block 000 = F_{VCO} / 1 (Recommended value) 001 = F_{VCO} / 2 010 = F_{VCO} / 4 011 = F_{VCO} / 8 100 = F_{VCO} / 16 101 = F_{VCO} / 32 Recommended that these are not changed from default.
	4:0	FLL_FRATIO [4:0]	8	CLK_VCO is divided by this integer, valid from 1 .. 31. 1 recommended for high freq reference 8 recommended for low freq reference
R61 (3Dh) FLL Control 2	15:0	FLL_K[15:0]	0h	Fractional multiply for CLK_REF

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R62 (3Eh) FLL Control 3	9:0	FLL_N[9:0]	0h	Integer multiply for CLK_REF
R63 (3Fh) FLL Control 4	6:3	FLL_TRK_GAIN [3:0]	0h	Gain applied to error 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that these are not changed from default.
	2:0	FLL_OUTDIV [2:0]	3h	F_{OUT} clock divider 000 = F_{VCO} / 2 001 = F_{VCO} / 4 010 = F_{VCO} / 8 (best performance) 011 = F_{VCO} / 16 100 = F_{VCO} / 32 101 = Reserved 110 = Reserved 111 = Reserved

Table 16 FLL Register Map

FLL POWER DOMAIN

Operation of the FLL requires an appropriate power supply to be connected to the FLLVDD power domain. This supply is referenced to AGND. The operating range for this supply is detailed in the "Recommended Operating Conditions" section.

EXAMPLE FLL CALCULATION

To generate 12.288 MHz output (F_{OUT}) from a 12.000 MHz reference clock (F_{REF}):

- Determine FLL_OUTDIV for the required output frequency as given by Table 15:-
  For F_{OUT} = 12.288 MHz, FLL_OUTDIV = 2h (divide by 8)
- Calculate F_{VCO} for the given FLL_OUTDIV:-
  $F_{VCO} = F_{OUT} * FLL\_OUTDIV = 12.288\ MHz * 8 = 98.304\ MHz$
- Calculate the required N.K x FLL_FRATIO for the given F_{REF} and F_{VCO}.:-
  $N.K \times FLL\_FRATIO = F_{VCO} / F_{REF} = 8.192$
- Determine FLL_REF_FREQ for the given F_{REF} as given by Table 16:-
  For F_{REF} = 12MHz, FLL_REF_FREQ = 0
- Determine FLL_FRATIO as given by Table 16:-
  For High Frequency Reference, FLL_FRATIO = 1
- Calculate N.K for the given FLL_FRATIO:-
  N.K = 8.192 / 1 = 8.192
- Determine FLL_N and FLL_K from the integer and fractional portions of N.K:-
  FLL_N is 8. FLL_K is 0.192
- Set FLL_FRAC according to whether fractional mode is required:-
  FLL_K is 0.192, so fractional mode is required; FLL_FRAC = 1

EXAMPLE FLL SETTINGS

Table 17 provides example FLL settings for generating common SYSCLK frequencies from a variety of low and high frequency reference inputs.

F_{REF}	F_{OUT}	F_{VCO}	FLL_N	FLL_K	FLL_ FRATIO	FLL_OUTDIV	FLL_ FRAC	FLL_REF_ FREQ
32.000 kHz	12.288 MHz	98.304 MHz	438 (1B6h)	0.857143 (DB6Eh)	7	2h (divide by 8)	1	1
32.000 kHz	11.2896 MHz	90.3168 MHz	352 (160h)	0.8 (CCCCh)	8	2h (divide by 8)	1	1
32.768 kHz	12.288 MHz	98.304 MHz	428 (1ACh)	0.571429 (9249 h)	7	2h (divide by 8)	1	1
32.768 kHz	11.288576 MHz	90.308608 MHz	344 (158h)	0.500000 (8000 h)	8	2h (divide by 8)	1	1
32.768 kHz	11.2896 MHz	90.3168 MHz	344 (158h)	0.53125 (8800h)	8	2h (divide by 8)	1	1
48 kHz	12.288 MHz	98.304 MHz	292 (124h)	0.571429 (9249 h)	7	2h (divide by 8)	1	1
11.3636 MHz	12.368544 MHz	98.948354 MHz	8 (008h)	0.707483 (B51Dh)	1	2h (divide by 8)	1	0
12.000 MHz	12.288 MHz	98.3040 MHz	8 (008h)	0.192 (3127h)	1	2h (divide by 8)	1	0
12.000 MHz	11.289597 MHz	90.3168 MHz	7 (007h)	0.526398 (86C2h)	1	2h (divide by 8)	1	0
12.288 MHz	12.288 MHz	98.304 MHz	2 (002h)	0.666667 (AAABh)	3	2h (divide by 8)	1	0
12.288 MHz	11.2896 MHz	90.3168 MHz	7 (007h)	0.35 (599Ah)	1	2h (divide by 8)	1	0
13.000 MHz	12.287990 MHz	98.3040 MHz	7 (007h)	0.56184 (8FD5h)	1	2h (divide by 8)	1	0
13.000 MHz	11.289606 MHz	90.3168 MHz	6 (006h)	0.94745 (F28Ch)	1	2h (divide by 8)	1	0
19.200 MHz	12.287988 MHz	98.3040 MHz	5 (005h)	0.119995 (1EB8h)	1	2h (divide by 8)	1	0
19.200 MHz	11.289588 MHz	90.3168 MHz	4 (004h)	0.703995 (B439h)	1	2h (divide by 8)	1	0

Table 17 Example FLL Settings

AUDIO CODEC SUBSYSTEM

INTRODUCTION

The WM8400 incorporates a low power, high quality audio CODEC which is designed to interface with a wide range of processors and analogue components.

Eight highly flexible analogue inputs allow interfacing to up to four microphone inputs plus multiple stereo or mono line inputs (single-ended or differential). Connections to an external voice CODEC, FM radio, melody IC, line input, handset MIC and headset MIC are all fully supported. Signal routing to the output mixers and within the CODEC has been designed for maximum flexibility to support a wide variety of usage modes.

Ten analogue output drivers are integrated, including a high power, high quality speaker driver, capable of providing 1W in class D mode or 0.5W in class AB mode into 8Ω BTL. Four headphone drivers are provided, supporting ear speakers and stereo headsets. Fully differential headphone drive is supported for excellent crosstalk performance and removing the need for large and expensive headphone capacitors. Four line outputs are available for Tx voice output to a voice CODEC, interfacing to an additional speaker driver and single-ended or fully differential line output. All outputs have integrated pop and click suppression. The speaker supply has been designed with low leakage and high PSRR, to support direct connection to a Lithium battery. Six AC and DC gain settings allow output signal levels to be maximised for a number of AVDD and SPKVDD combinations.

Internal signal routing and amplifier configurations have been optimised to provide the lowest possible power consumption for a number of common usage scenarios such as voice calls and music playback.

The stereo ADCs and DACs are of hi-fi quality using a 24-bit, low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports mixed ADC and DAC sample rates, while an integrated ultra-low power FLL provides additional flexibility. A high pass filter is available in the ADC path for removing DC offsets or suppressing low frequency noise such as mechanical vibration and wind noise. A digital mixing path from the ADC to the DAC provides a sidetone of enhanced quality during voice calls. Pop-free DAC soft mute and un-mute is available.

The WM8400 has a highly flexible digital audio interface, supporting a number of protocols, including I^2S, DSP, MSB-First left/right justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and μ-law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power. Alternative DAC interface pins are provided to allow connection to an additional processor.

The SYSCLK (system clock) provides clocking for the ADCs, DACs, DSP core, class D outputs and the digital audio interface. SYSCLK can be derived directly from the MCLK pin or via an integrated FLL, providing flexibility to support a wide range of clocking schemes. All MCLK frequencies typically used in portable systems are supported for sample rates between 8kHz and 48kHz. The switching clock for the class D speaker drivers can be derived from SYSCLK or else provided by an oscillator within the WM8400. (Best speaker driver performance is achieved when this clock is synchronous with the audio DSP clocks.) An additional master clock input pin is provided, to support operation on an alternative clock domain, selectable via a de-glitch circuit.

Versatile GPIO functionality is provided, with support for up to seven button/accessory detect inputs with interrupt and status readback and flexible de-bouncing options, clock output, alternative MCLK input, ADCLRC inversion for simultaneous streaming of ADC data to two separate processors and logic '1' / logic '0' for control of additional external circuitry.

Unused circuit blocks within the CODEC can be disabled via software to save power, while low leakage currents extend standby and off time in portable battery-powered applications.

AUDIO SIGNAL PATHS

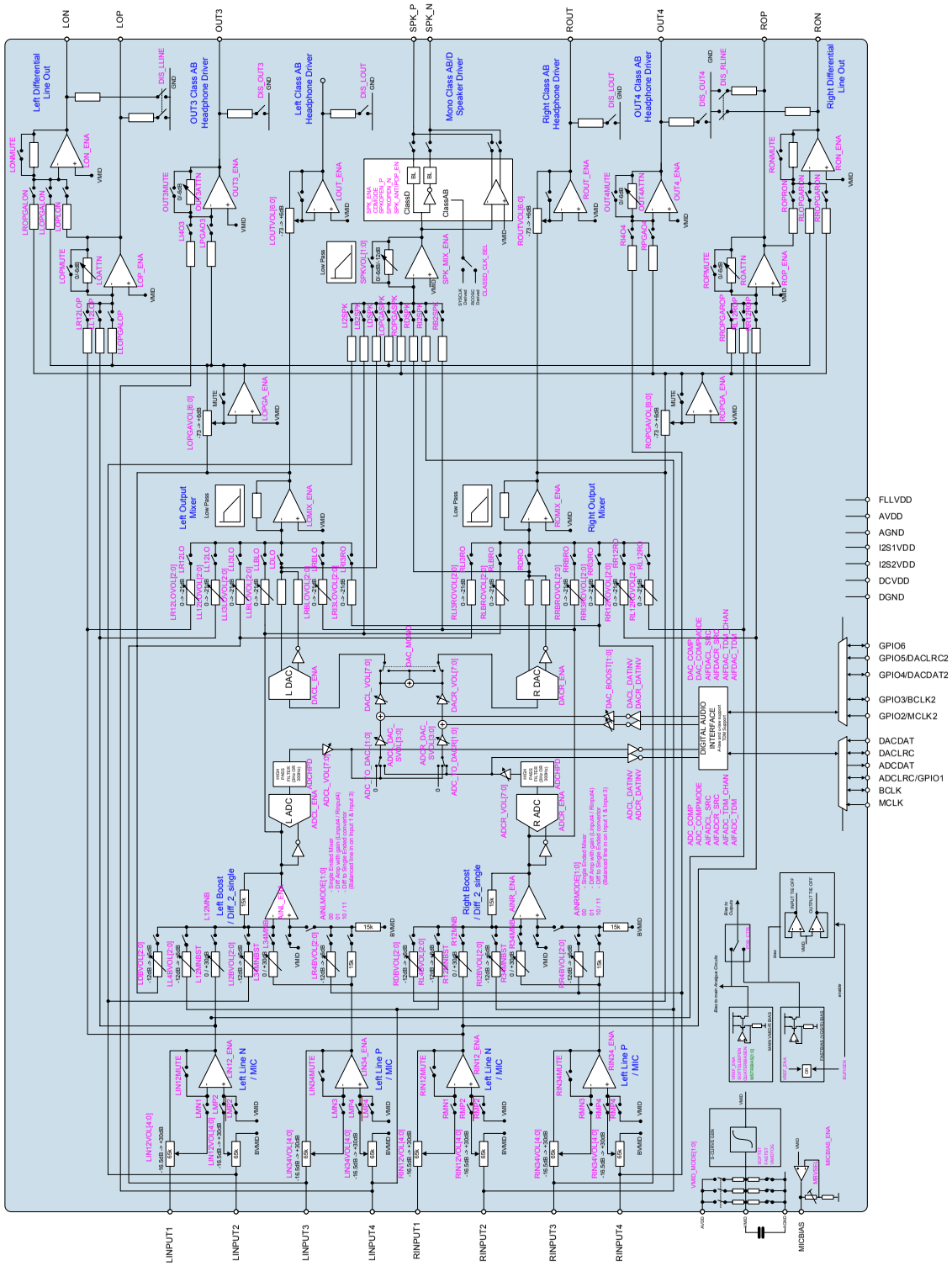


Figure 18 WM8400 Audio Signal Paths

ENABLING THE AUDIO CODEC

AUDIO CODEC POWER DOMAINS

Operation of the audio CODEC requires appropriate power supplies to be connected to the associated power domains. (If the CODEC power supplies are derived from the WM8400's integrated LDO Regulators, then see "Power Management Subsystem" for further details of how these Regulators are configured.)

The analogue input circuits to the CODEC are powered on the AVDD domain. The Line Outputs LOP, LON, ROP, RON are also powered via AVDD. The digital CODEC circuits are powered on the DCVDD domain. The supplies AVDD and DCVDD are both referenced to AGND.

The headphone outputs LOUT, ROUT, OUT3 and OUT4 are powered on the HPVDD domain (referenced to HPGND). The speaker outputs SPKP and SPKN are power on the SPKVDD domain (referenced to SPKGND).

The operating ranges for these supplies are detailed in the "Recommended Operating Conditions" section.

ENABLING THE AUDIO CODEC

Before the audio CODEC can be used, it must be enabled by writing to the CODEC_ENA register bit. When this bit is set to logic '0', all CODEC registers are held in their default states. Setting this bit to logic '0' may be used to reset all CODEC registers to their default values.

The CODEC can also be enabled by writing a logic '1' to the CODEC_SOFTST register bit. Setting this bit will trigger pop-suppressed start-up sequence. As part of this sequence, CODEC_ENA will become set automatically.

The CODEC can be disabled by writing a logic '1' to the CODEC_SOFTSD register bit. Setting this bit will trigger a pop-suppressed CODEC shut-down sequence. As part of this sequence, CODEC_ENA will be reset to logic '0'.

Note that, when the WM8400 is in Deep Sleep mode (see "Power Management Subsystem"), the CODEC will be disabled, and CODEC_ENA will be set to logic '0'. Therefore, on exit from Deep Sleep mode, all the previous CODEC settings will be lost.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h)	15	CODEC_ENA (rw)	0b	Master CODEC enable bit. 0 = CODEC registers held in reset 1 = CODEC registers operate normally
R76 (4Ch)	15	CODEC_SOFTST	0b	CODEC Soft Start Sequence 0 = Disabled 1 = Enabled
	14	CODEC_SOFTSD	0b	CODEC Soft Shutdown Sequence 0 = Disabled 1 = Enabled

Table 18 Enabling the Audio CODEC

INPUT SIGNAL PATH

The WM8400 has eight highly flexible analogue input channels, configurable in many combinations of the following:

1. Up to four pseudo-differential or single-ended microphone inputs

2. Up to eight mono line inputs or 4 stereo line inputs

3. Mono input from external voice CODEC

4. Two fully balanced differential inputs

These inputs may be mixed together or independently routed to different combinations of output drivers. An internal record path is provided at the input mixers to allow DAC output to be mixed with the input signal path (e.g. for karaoke or voice call recording).

The WM8400 input signal paths and control registers are illustrated in Figure 19.

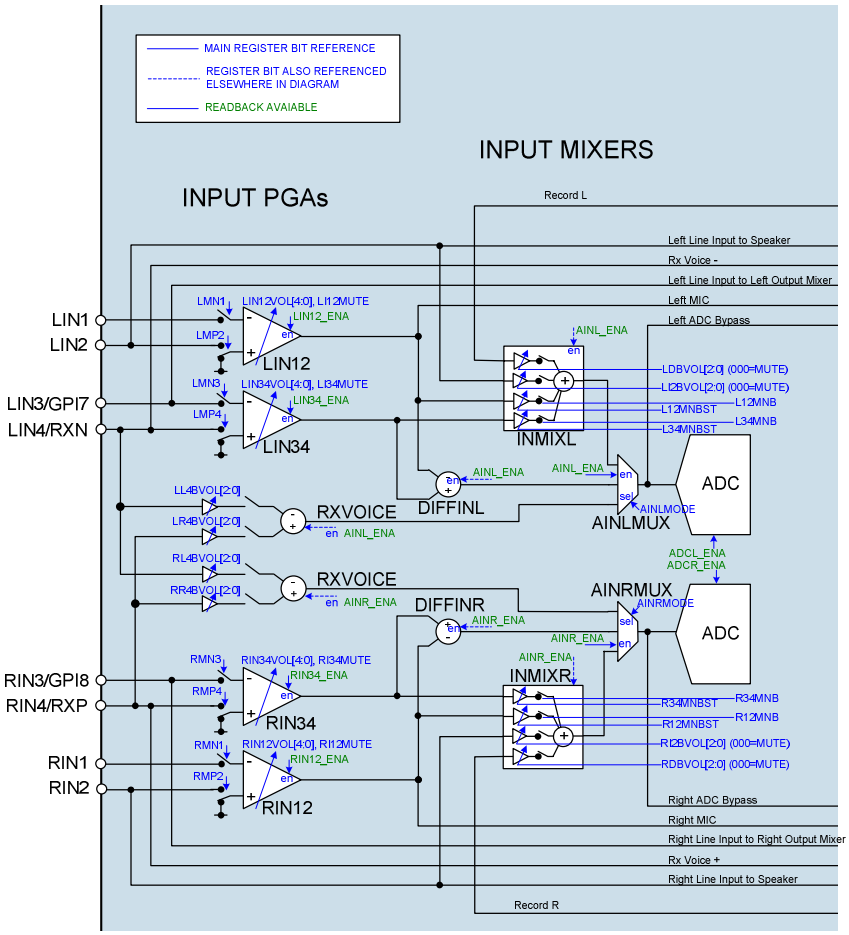


Figure 19 Control Registers for Input Signal Path

MICROPHONE INPUTS

Up to four microphones can be connected to the WM8400, either in single-ended or pseudo-differential mode. A low noise microphone bias is fully integrated to reduce the need for external components.

In single-ended microphone input configuration, the microphone signal is connected to the inverting input of the PGA (LIN1, LIN3, RIN1 or RIN3). The non-inverting input of the PGAs should be internally connected to VMID in this configuration. This is enabled via the Input PGA configuration register settings. In this configuration, LIN2, LIN4, RIN2 or RIN4 may be free to be used as line inputs or ADC bypass inputs.

In pseudo-differential microphone input configuration, the non-inverted microphone signal is connected to the non-inverting input of the PGA (LIN2, LIN4, RIN2 or RIN4) and the inverted (or noisy ground) signal is connected to the inverting input (LIN1, LIN3, RIN1 or RIN3).

Any PGA input pin that is used in either microphone configuration should not be enabled as a line input path at the same time.

The gain of the input PGAs is controlled via register settings. Note that the input impedance of LIN1, LIN3, RIN1 and RIN3 changes with the input PGA gain setting, as described under “Electrical Characteristics”. (Note this does not apply to input paths which bypass the input PGA.) The input impedance of LIN2, LIN4, RIN2 and RIN4 does not change with input PGA gain. The inverting and non-inverting inputs are therefore not matched and the differential configuration is not fully differential.

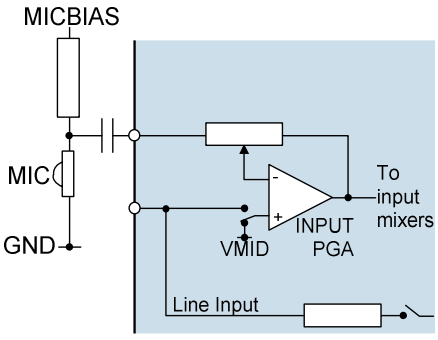


Figure 20 Single-Ended Microphone Input

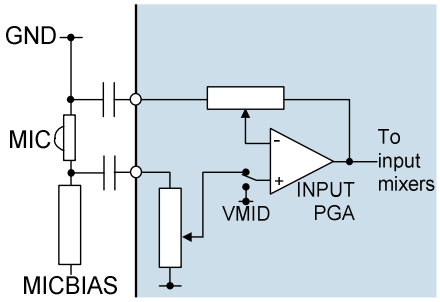


Figure 21 Differential Microphone Input

LINE INPUTS

All eight analogue input pins may be configured as line inputs. Various signal paths exist to provide flexibility, high performance and low power consumption for different usage modes.

LIN1 and RIN1 can operate as line inputs to the Input PGAs LIN12 and RIN12 to provide high gain if required for small input signals.

LIN2 and RIN2 can operate as line inputs directly to the input mixers or to the speaker output mixer. Direct routing to the speaker output minimises power consumption by reducing the number of active amplifiers in the signal path.

LIN3 and RIN3 can operate as line inputs to the Input PGAs or as a line input directly to either of the output mixers LOMIX and ROMIX.

LIN1+LIN3 and RIN1+RIN3 can also be used as fully balanced differential inputs via the Input PGAs to one of the input mixers. (Note that these inputs have matched input impedances.)

LIN4/RXN and RIN4/RXP can operate as line inputs directly to the outputs OUT3 and OUT4, providing an ultra-low power stereo or mono differential signal path (e.g. from an external voice CODEC) to an ear speaker. LIN4/RXN and RIN4/RXP can also operate as a mono differential input to the ADC input signal path and output mixer stages.

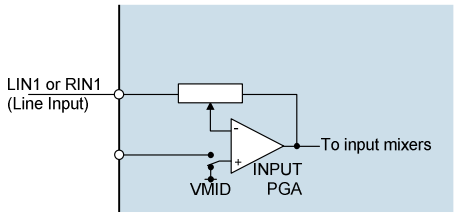


Figure 22 LIN1 or RIN1 as Line Inputs

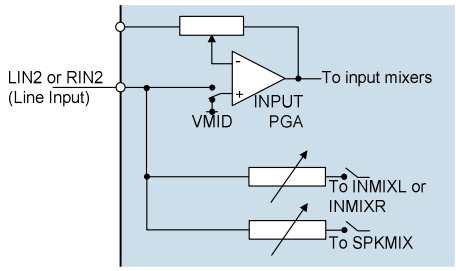


Figure 23 LIN2 or RIN2 as Line Inputs

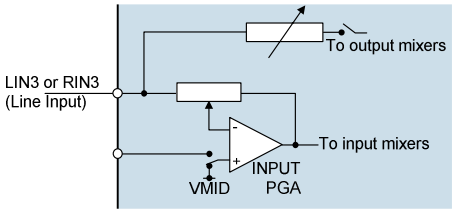


Figure 24 LIN3 or RIN3 as Line Inputs

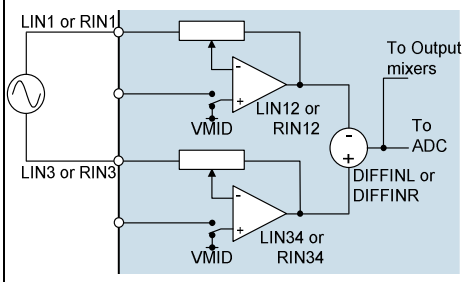


Figure 25 Fully Balanced Differential Input

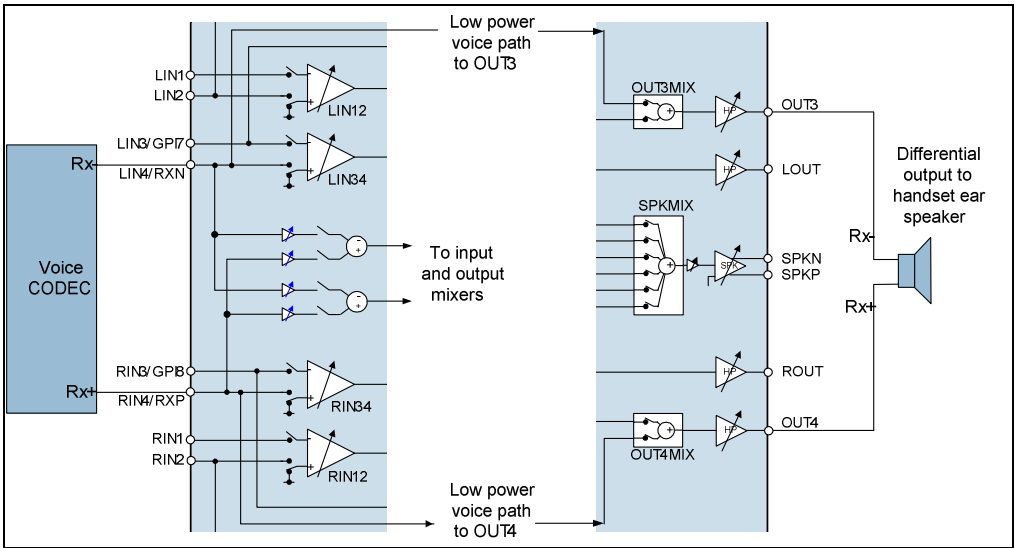


Figure 26 LIN4 and RIN4 as Rx Voice Inputs with Direct Low Power Path to Ear Speaker

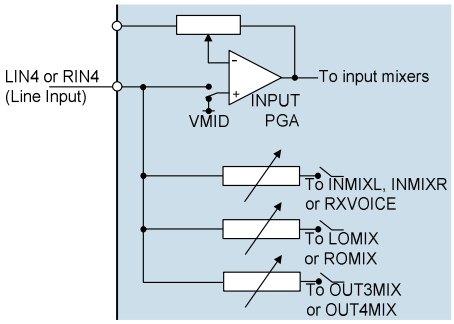


Figure 27 LIN4 or RIN4 as Line Inputs

INPUT PGA ENABLE

The Input PGAs are enabled using register bits LIN12_ENA, LIN34_ENA, RIN12_ENA and RIN34_ENA as described in Table 19.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h)	7	LIN34_ENA (rw)	0b	LIN34 Input PGA Enable 0 = disabled 1 = enabled
	6	LIN12_ENA (rw)	0b	LIN12 Input PGA Enable 0 = disabled 1 = enabled
	5	RIN34_ENA (rw)	0b	RIN34 Input PGA Enable 0 = disabled 1 = enabled
	4	RIN12_ENA (rw)	0b	RIN12 Input PGA Enable 0 = disabled 1 = enabled

Table 19 Input PGA Enable

REFERENCE VOLTAGES

All internal analogue input and output circuitry requires a reference voltage AVDD/2 (VMID). This voltage is generated internally using 6.8kΩ, 50kΩ or 300kΩ (+/- 15%) resistors and is buffered as required. These functions are controlled using register bits VMID_MODE and VREF_ENA.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h)	2:1	VMID_MODE [1:0] (rw)	00b	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50kΩ divider (Normal mode) 10 = 2 x 300kΩ divider (Standby mode) 11 = 2 x 6.8kΩ divider (for fast start-up)
	0	VREF_ENA (rw)	0b	VREF Enable (Bias for all analogue functions) 0 = VREF bias disabled 1 = VREF bias enabled

Table 20 Reference Voltages

MICROPHONE BIAS CONTROL

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones via an external resistor. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be enabled or disabled using the MIC1BIAS_ENA control bit and the voltage can be selected using the MBSEL register bit as detailed in Table 21.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h)	4	MIC1BIAS_ENA (rw)	0b	Microphone Bias 0 = OFF (high impedance output) 1 = ON
R58 (3Ah)	0	MBSEL	0b	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD

Table 21 Microphone Bias Control

Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistance must be large enough to limit the MICBIAS current to 3mA.

MICROPHONE CURRENT DETECT

A MICBIAS current detect function allows detection of accessories such as headset microphones. When the MICBIAS load current exceeds one of two programmable thresholds, (e.g. short circuit current or normal operating current), an interrupt or GPIO output can be generated. The current detection circuit is enabled by the MCD bit; the current thresholds are selected by the MCDTHR and MCDSCTH register fields as described in Table 65- see “General Purpose Input/Output” for a full description of these fields. Note that the MICBIAS current thresholds are subject to a wide tolerance - up to +/-50% of the specified value.

INPUT PGA CONFIGURATION

Each of the four Input PGAs can be configured in single-ended or pseudo-differential mode.

Single-ended microphone operation of an Input PGA is selected by connecting the input source to the inverting PGA input. The non-inverting PGA input must be connected to VMID by setting the appropriate register bits.

For pseudo-differential microphone operation, the inverting and non-inverting PGA inputs are both connected to the input source and not to VMID.

For any line input or other connection not using the Input PGA, the appropriate PGA input should be disconnected from the external pin and connected to VMID.

Register bits LMN1, LMP2, LMN3, LMP4, RMN1, RMP2, RMN3 and RMP4 control connection of the PGA inputs to the device pins as shown in Table 22. The maximum available attenuation on any of these input paths is achieved using these bits to disable the input path to the applicable PGA.

When not enabled as analogue inputs or as General Purpose inputs, the input pins can be biased to VMID via a 1kΩ resistor.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h)	7	LMP4	0b	LIN34 PGA Non-Inverting Input Select 0 = LIN4 not connected to PGA 1 = LIN4 connected to PGA
	6	LMN3	0b	LIN34 PGA Inverting Input Select 0 = LIN3 not connected to PGA 1 = LIN3 connected to PGA
	5	LMP2	0b	LIN12 PGA Non-Inverting Input Select 0 = LIN2 not connected to PGA 1 = LIN2 connected to PGA
	4	LMN1	0b	LIN12 PGA Inverting Input Select 0 = LIN1 not connected to PGA 1 = LIN1 connected to PGA
	3	RMP4	0b	RIN34 PGA Non-Inverting Input Select 0 = RIN4 not connected to PGA 1 = RIN4 connected to PGA
	2	RMN3	0b	RIN34 PGA Inverting Input Select 0 = RIN3 not connected to PGA 1 = RIN3 connected to PGA
	1	RMP2	0b	RIN12 PGA Non-Inverting Input Select 0 = RIN2 not connected to PGA 1 = RIN2 connected to PGA
	0	RMN1	0b	RIN12 PGA Inverting Input Select 0 = RIN1 not connected to PGA 1 = RIN1 connected to PGA

Table 22 Input PGA Configuration

INPUT PGA VOLUME CONTROL

Each of the four Input PGAs has an independently controlled gain range of -16.5dB to +30dB in 1.5dB steps. The gains on the inverting and non-inverting inputs to the PGAs are always equal. Each Input PGA can be independently muted using the PGA Mute bits described in Table 23. Maximum mute attenuation is achieved by simultaneously disconnecting the corresponding inputs, as described in Table 22.

To prevent "zipper noise", a zero-cross function is provided, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOCLK_ENA register bit), the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout period is set by TOCLK_RATE. See “Clocking and Sample Rates” for more information on these fields.

The IPVU bit controls the loading of the input PGA volume data. When IPVU is set to 0, the PGA volume data will be loaded into the respective control register, but will not actually change the gain setting. The LIN12, RIN12, LIN34, RIN34 volume settings are all updated when a 1 is written to IPVU. This makes it possible to update the gain of all input paths simultaneously.

The Input PGA Volume Control register fields are described in Table 23 and Table 24.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h)	8	IPVU[0]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	LI12MUTE	1b	LIN12 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	LI12ZC	0b	LIN12 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	LIN12VOL [4:0]	01011b (0dB)	LIN12 Volume (See Table 24 for volume range)
R25 (19h)	8	IPVU[1]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	LI34MUTE	1b	LIN34 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	LI34ZC	0b	LIN34 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	LIN34VOL [4:0]	01011b (0dB)	LIN34 Volume (See Table 24 for volume range)
R26 (1Ah)	8	IPVU[2]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	RI12MUTE	1b	RIN12 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	RI12ZC	0b	RIN12 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	RIN12VOL [4:0]	01011b (0dB)	RIN12 Volume (See Table 24 for volume range)
R27 (1Bh)	8	IPVU[3]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	RI34MUTE	1b	RIN34 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	RI34ZC	0b	RIN34 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	RIN34VOL [4:0]	01011b (0dB)	RIN34 Volume (See Table 24 for volume range)

Table 23 Input PGA Volume Control

LIN12VOL[4:0], LIN34VOL[4:0], RIN12VOL[4:0], RIN34VOL[4:0]	VOLUME (dB)
00000	-16.5
00001	-15.0
00010	-13.5
00011	-12.0
00100	-10.5
00101	-9.0
00110	-7.5
00111	-6.0
01000	-4.5
01001	-3.0
01010	-1.5
01011	0
01100	+1.5
01101	+3.0
01110	+4.5
01111	+6.0
10000	+7.5
10001	+9.0
10010	+10.5
10011	+12.0
10100	+13.5
10101	+15.0
10110	+16.5
10111	+18.0
11000	+19.5
11001	+21.0
11010	+22.5
11011	+24.0
11100	+25.5
11101	+27.0
11110	+28.5
11111	+30.0

Table 24 Input PGA Volume Range

INPUT MIXER ENABLE

The WM8400 has two analogue input mixers which allow the Input PGAs and Line Inputs to be combined in a number of ways and output to the ADCs or to the Output Mixers via bypass paths.

The input mixers INMIXL and INMIXR are enabled by the AINL_ENA and AINR_ENA register bits, as described in Table 25. These control bits also enable the Input Multiplexers and Differential Input drivers, described in the following section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h)	9	AINL_ENA (rw)	0b	Left Input Path Enable (Enables AINLMUX, INMIXL, DIFFINL and RXVOICE input to AINLMUX) 0 = Input Path disabled 1 = Input Path enabled
	8	AINR_ENA (rw)	0b	Right Input Path Enable (Enables AINRMUX, INMIXR, DIFFINR and RXVOICE input to AINRMUX) 0 = Input Path disabled 1 = Input Path enabled

Table 25 Input Mixer Enable

INPUT MIXER CONFIGURATION

The left and right channel input multiplexers AINLMUX and AINRMUX select one of three input sources for the Left and Right channels independently. The three input sources are as follows:

1. INMIXL or INMIXR output (a combination of Input PGAs, line inputs and the internal record path).

2. RXVOICE (a differential to single-ended conversion of LIN4/RXN and RIN4/RXP inputs).

3. DIFFINL or DIFFINR output (a differential to single-ended conversion of two Input PGAs).

The input source for the multiplexers is controlled by register bits AINLMODE and AINRMODE as described in Table 26.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R39 (27h)	3:2	AINLMODE [1:0]	00b	AINLMUX Input Source 00 = INMIXL (Left Input Mixer) 01 = RXVOICE (RXP - RXN) 10 = DIFFINL (LIN12 PGA - LIN34 PGA) 11 = (Reserved)
	1:0	AINRMODE [1:0]	00b	AINRMUX Input Source 00 = INMIXR (Right Input Mixer) 01 = RXVOICE (RXP - RXN) 10 = DIFFINR (RIN12 PGA - RIN34 PGA) 11 = (Reserved)

Table 26 Input Mixer Configuration

The Input Mixer configuration is described for each of the three modes in the following sections. Note that the Left and Right multiplexer (mode) settings can be set independently.

In Mixer Mode (AINLMODE=00, AINRMODE=00), adjustable gain control is available on the input mixers INMIXL and INMIXR for all available input signals (PGA outputs, line inputs and record paths). This configuration is illustrated in Figure 28. The applicable register settings are shown in Table 27.

CONFIGURATION	REGISTER SETTINGS	
Left Channel Mixer Mode (INMIXL to AINLMUX)	1. Select Mixer Mode	AINLMODE = 00
	2. Enable input paths as required (see Table 23 and Table 30 for full definitions of the applicable settings listed here)	L12MNB, L12MNBST LIN12VOL, LIN12MUTE L34MNB, L34MNBST LIN34VOL, LIN34MUTE LDBVOL LI2BVOL
Right Channel Mixer Mode (INMIXR to AINRMUX)	1. Select Mixer Mode	AINRMODE = 00
	2. Enable input paths as required (see Table 23 and Table 31 for full definitions of the applicable settings listed here)	R12MNB, R12MNBST RIN12VOL, RIN12MUTE R34MNB, R34MNBST RIN34VOL, RIN34MUTE RDBVOL RI2BVOL

Table 27 Mixer Mode Register Settings

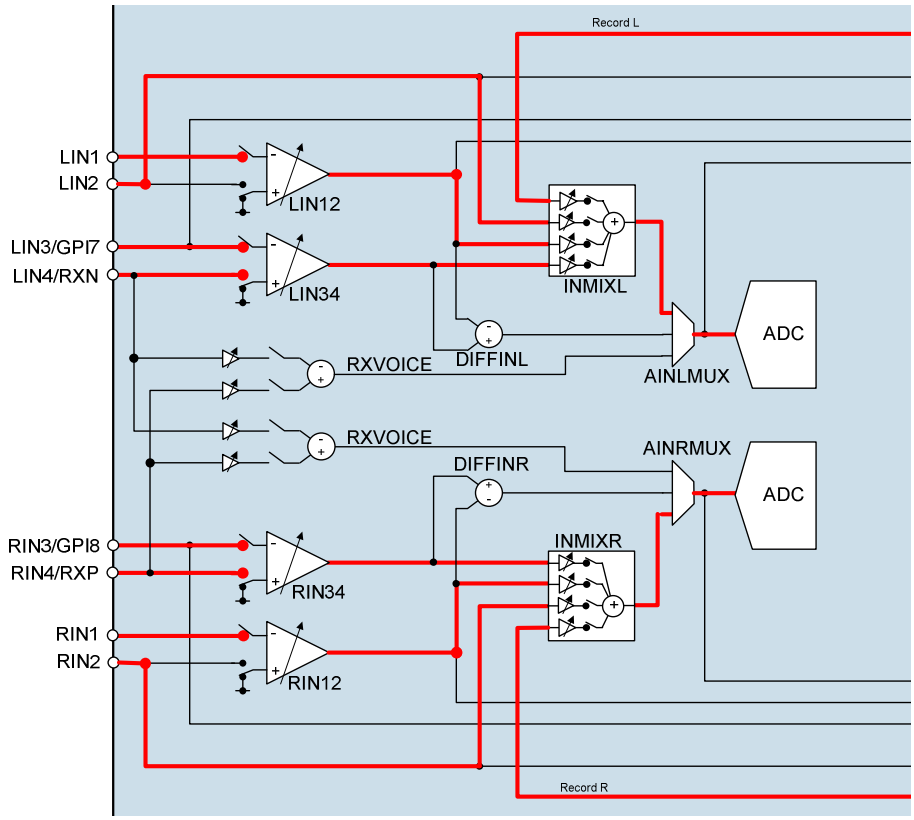


Figure 28 Mixer Mode Signal Paths

In Rx Voice Mode (AINLMODE=01, AINRMODE=01), adjustable gain control is available for the RXVOICE output by use of the LR4BVOL[2:0] and LL4BVOL[2:0] register fields on the left channel and by RL4BVOL[2:0] and RR4BVOL[2:0] on the right channel. Both Volume fields for the desired channel(s) must be set to the same value for true Differential input characteristics. This configuration is illustrated in Figure 29. The applicable register settings are shown in Table 28.

CONFIGURATION	REGISTER SETTINGS	
Left Channel Rx Voice Mode (RXVOICE to AINLMUX)	1. Select Rx Voice Mode	AINLMODE = 01
	2. Enable Rx Voice input as required Important: These two register fields must be set to the same value. See Table 30 for full definitions of these fields.	LL4BVOL LR4BVOL
Right Channel Rx Voice Mode (RXVOICE to AINRMUX)	1. Select Rx Voice Mode	AINRMODE = 01
	2. Enable Rx Voice input as required Important: These two register fields must be set to the same value. See Table 31 for full definitions of these fields.	RL4BVOL RR4BVOL

Table 28 RxVoice Mode Register Settings

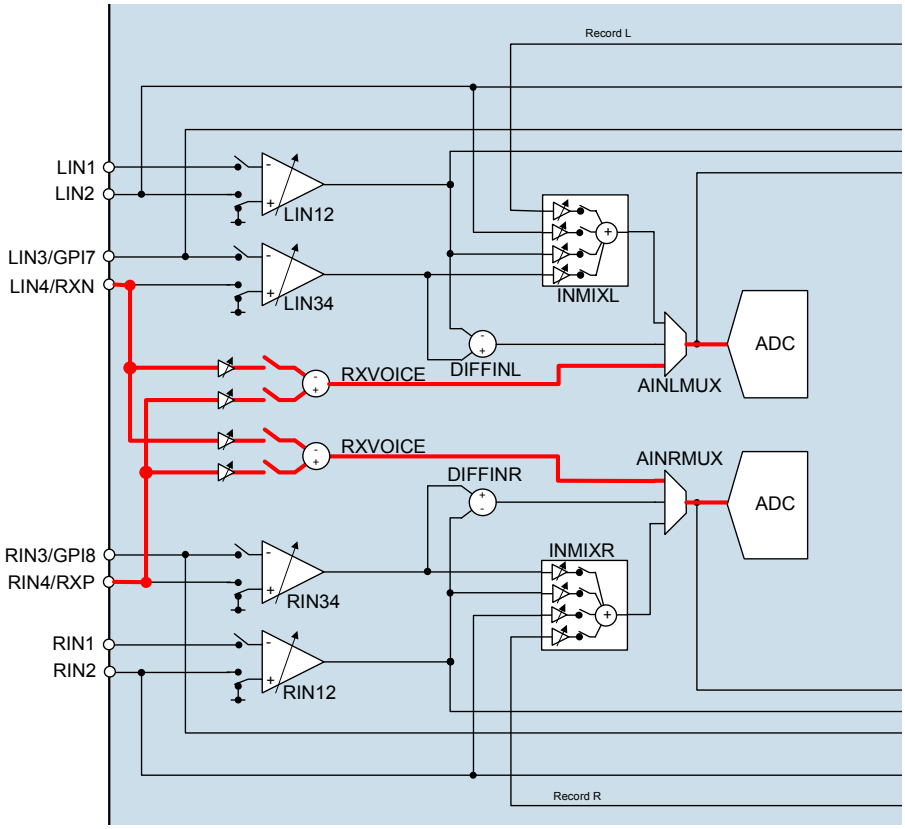


Figure 29 RxVoice Mode Signal Paths

In Differential Mode (AINLMODE=10, AINRMODE=10), no additional volume control is available in the input signal path, but the Input PGA volume control can be used to adjust the signal level as with other modes. Both PGAs on the desired channel(s) must be enabled, and the PGA volumes of each set to the same value for true Differential input characteristics. The PGA Output (LIN12 or RIN12) to Mixer (INMIXL or INMIXR) path must also be enabled on the desired channel(s) by use of register bit L12MNB or R12MNB. This configuration is illustrated in Figure 30. The applicable register settings are shown in Table 29.

CONFIGURATION	REGISTER SETTINGS	
Left Channel Differential Mode (DIFFINL to AINLMUX)	1. Select Differential Mode	AINLMODE = 10
	2. Enable LIN12 input path	L12MNB = 1
	3. Set channel volume as required. Important: The LIN12 and LIN34 volume and mute settings must be set to the same value. See Table 23 for full definitions of these fields.	LIN12VOL, LIN12MUTE LIN34VOL, LIN34MUTE
Right Channel Differential Mode (DIFFINR to AINRMUX)	1. Select Differential Mode	AINRMODE = 10
	2. Enable RIN12 input path	R12MNB = 1
	3. Set channel volume as required. Important: The RIN12 and RIN34 volume and mute settings must be set to the same value. See Table 23 for full definitions of these fields.	RIN12VOL, RIN12MUTE RIN34VOL, RIN34MUTE

Table 29 Differential Mode Register Settings

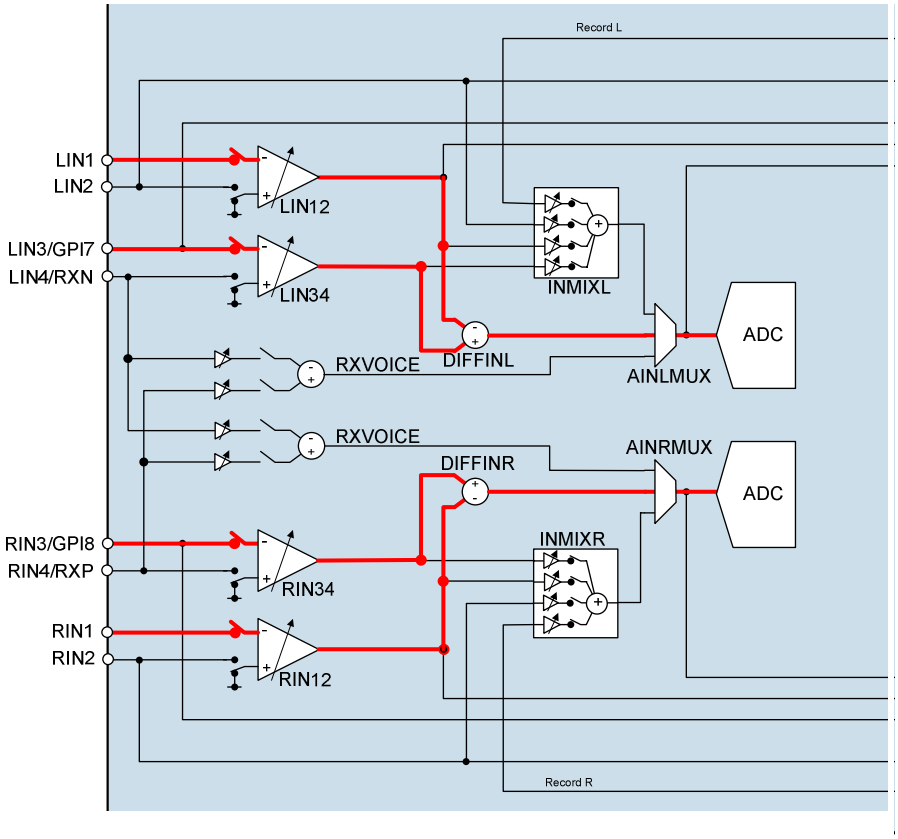


Figure 30 Differential Mode Signal Paths

INPUT MIXER VOLUME CONTROL

The Input Mixer volume controls are described in Table 30 for the Left Channel and Table 31 for the Right Channel. The Input PGA levels may be set to Mute, 0dB or 30dB boost. The other gain controls provide adjustment from -12dB to +6dB in 3dB steps.

To prevent pop noise it is recommended that gain and mute controls for the input mixers are not modified while the signal paths are active. If volume control is required on the input signal path it is recommended that the input PGA volume controls or the ADC volume controls are used instead of the input mixer gain registers.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R41 (29h)	8	L34MNB	0b	LIN34 PGA Output to INMIXL Mute 0 = Mute 1 = Un-Mute
	7	L34MNBST	0b	LIN34 PGA Output to INMIXL Gain 0 = 0dB 1 = +30dB
	5	L12MNB	0b	LIN12 PGA Output to INMIXL Mute 0 = Mute 1 = Un-Mute
	4	L12MNBST	0b	LIN12 PGA Output to INMIXL Gain 0 = 0dB 1 = +30dB
	2:0	LDBVOL [2:0]	000b (Mute)	LOMIX to INMIXL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
R43 (2Bh)	8:6	LI2BVOL [2:0]	000b (Mute)	LIN2 Pin to INMIXL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	5:3	LR4BVOL [2:0]	000b (Mute)	RXVOICE to AINLMUX Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	2:0	LL4BVOL [2:0]	000b (Mute)	RXVOICE to INMIXL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB Note - LR4BVOL must be set to the same value as LL4BVOL when AINLMODE=01.

Table 30 Left Input Mixer Volume Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2A)	8	R34MNB	0b	RIN34 PGA Output to INMIXR Mute 0 = Mute 1 = Un-Mute
	7	R34MNBST	0b	RIN34 PGA Output to INMIXR Gain 0 = 0dB 1 = +30dB
	5	R12MNB	0b	RIN12 PGA Output to INMIXR Mute 0 = Mute 1 = Un-Mute
	4	R12MNBST	0b	RIN12 PGA Output to INMIXR Gain 0 = 0dB 1 = +30dB
	2:0	RDBVOL [2:0]	000b (Mute)	ROMIX to INMIXR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
R44 (2Ch)	8:6	RI2BVOL [2:0]	000b (Mute)	RIN2 Pin to INMIXR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	5:3	RL4BVOL [2:0]	000b (Mute)	RXVOICE to AINRMUX Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	2:0	RR4BVOL [2:0]	000b (Mute)	RXVOICE to INMIXR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB Note - RL4BVOL must be set to the same value as RR4BVOL when AINRMODE=01.

Table 31 Right Input Mixer Volume Control

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8400 uses stereo 24-bit, 64x oversampled sigma-delta ADCs. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC full scale input level is proportional to AVDD. See "Electrical Characteristics" for further details. Any input signal greater than full scale may overload the ADC and cause distortion.

The ADCs are enabled by the ADCL_ENA and ADCR_ENA register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h)	1	ADCL_ENA (rw)	0b	Left ADC Enable 0 = ADC disabled 1 = ADC enabled
	0	ADCR_ENA (rw)	0b	Right ADC Enable 0 = ADC disabled 1 = ADC enabled

Table 32 ADC Enable Control

ADC DIGITAL VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from -71.625dB to +17.625dB in 0.375dB steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 239$; MUTE for $X = 0$ +17.625dB for $239 \leq X \leq 255$

The ADC_VU bit controls the loading of digital volume control data. When ADC_VU is set to 0, the ADCL_VOL or ADCR_VOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to ADC_VU. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (10h)	8	ADC_VU	N/A	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCL_VOL [7:0]	1100_0000b (0dB)	Left ADC Digital Volume (See Table 34 for volume range)
R17 (11h)	8	ADC_VU	N/A	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCR_VOL [7:0]	1100_0000b (0dB)	Right ADC Digital Volume (See Table 34 for volume range)

Table 33 ADC Digital Volume Control

ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.375
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.750
3h	-70.875	43h	-46.875	83h	-22.875	C3h	1.125
4h	-70.500	44h	-46.500	84h	-22.500	C4h	1.500
5h	-70.125	45h	-46.125	85h	-22.125	C5h	1.875
6h	-69.750	46h	-45.750	86h	-21.750	C6h	2.250
7h	-69.375	47h	-45.375	87h	-21.375	C7h	2.625
8h	-69.000	48h	-45.000	88h	-21.000	C8h	3.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	3.375
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	3.750
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	4.125
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	4.500
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	4.875
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	5.250
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	5.625
10h	-66.000	50h	-42.000	90h	-18.000	D0h	6.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	6.375
12h	-65.250	52h	-41.250	92h	-17.250	D2h	6.750
13h	-64.875	53h	-40.875	93h	-16.875	D3h	7.125
14h	-64.500	54h	-40.500	94h	-16.500	D4h	7.500
15h	-64.125	55h	-40.125	95h	-16.125	D5h	7.875
16h	-63.750	56h	-39.750	96h	-15.750	D6h	8.250
17h	-63.375	57h	-39.375	97h	-15.375	D7h	8.625
18h	-63.000	58h	-39.000	98h	-15.000	D8h	9.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	9.375
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	9.750
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	10.125
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	10.500
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	10.875
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	11.250
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	11.625
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	12.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	12.375
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	12.750
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	13.125
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	13.500
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	13.875
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	14.250
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	14.625
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	15.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	15.375
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	15.750
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	16.125
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	16.500
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	16.875
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	17.250
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	17.625
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	17.625
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	17.625
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	17.625
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	17.625
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	17.625
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	17.625
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	17.625
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	17.625
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	17.625
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	17.625
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	17.625
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	17.625
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	17.625
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	17.625
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	17.625
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	17.625

Table 34 ADC Digital Volume Range

HIGH PASS FILTER

A digital high pass filter is applied by default to the ADC path to remove DC offsets. This filter can also be programmed to remove low frequency noise in voice applications (e.g. wind noise or mechanical vibration). This filter is controlled using the ADC_HPF_ENA and ADC_HPF_CUT register bits.

In hi-fi mode the high pass filter is optimised for removing DC offsets without degrading the bass response and has a cut-off frequency of 3.7Hz at fs=44.1kHz.

In voice mode the high pass filter is optimised for voice communication and it is recommended to program the cut-off frequency below 300Hz (e.g. ADC_HPF_CUT=11 at fs=8kHz or ADC_HPF_CUT=10 at fs=16kHz).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 (0Fh)	8	ADC_HPF_ENA	1b	ADC Digital High Pass Filter Enable 0 = disabled 1 = enabled
	6:5	ADC_HPF_CUT [1:0]	00b	ADC Digital High Pass Filter Cut-Off Frequency (fc) 00 = Hi-fi mode (fc=4Hz at fs=48kHz) 01 = Voice mode 1 (fc=127Hz at fs=16kHz) 10 = Voice mode 2 (fc=130Hz at fs=8kHz) 11 = Voice mode 3 (fc=267Hz at fs=8kHz) (Note: fc scales with sample rate. See Table 36 for cut-off frequencies at all supported sample rates)

Table 35 ADC High Pass Filter Control Registers

SAMPLE FREQUENCY (kHz)	CUT-OFF FREQUENCY (Hz)			
	ADC_HPF_CUT =00	ADC_HPF_CUT =01	ADC_HPF_CUT =10	ADC_HPF_CUT =11
8.000	0.7	64	130	267
11.025	0.9	88	178	367
16.000	1.3	127	258	532
22.050	1.9	175	354	733
24.000	2.0	190	386	798
32.000	2.7	253	514	1063
44.100	3.7	348	707	1464
48.000	4.0	379	770	1594

Table 36 ADC High Pass Filter Cut-Off Frequencies

The high pass filter characteristics are shown in the "Digital Filter Characteristics" section.

DIGITAL MIXING

The ADC and DAC data can be combined in various ways to support a range of different usage modes.

Data from either of the two ADCs can be routed to either the left or the right channel of the digital audio interface. In addition, data from either of the digital audio interface channels can be routed to either the left or the right DAC. See "Digital Audio Interface" for more information on the audio interface.

DIGITAL MIXING PATHS

Figure 31 shows the digital mixing paths available in the WM8400 digital core.

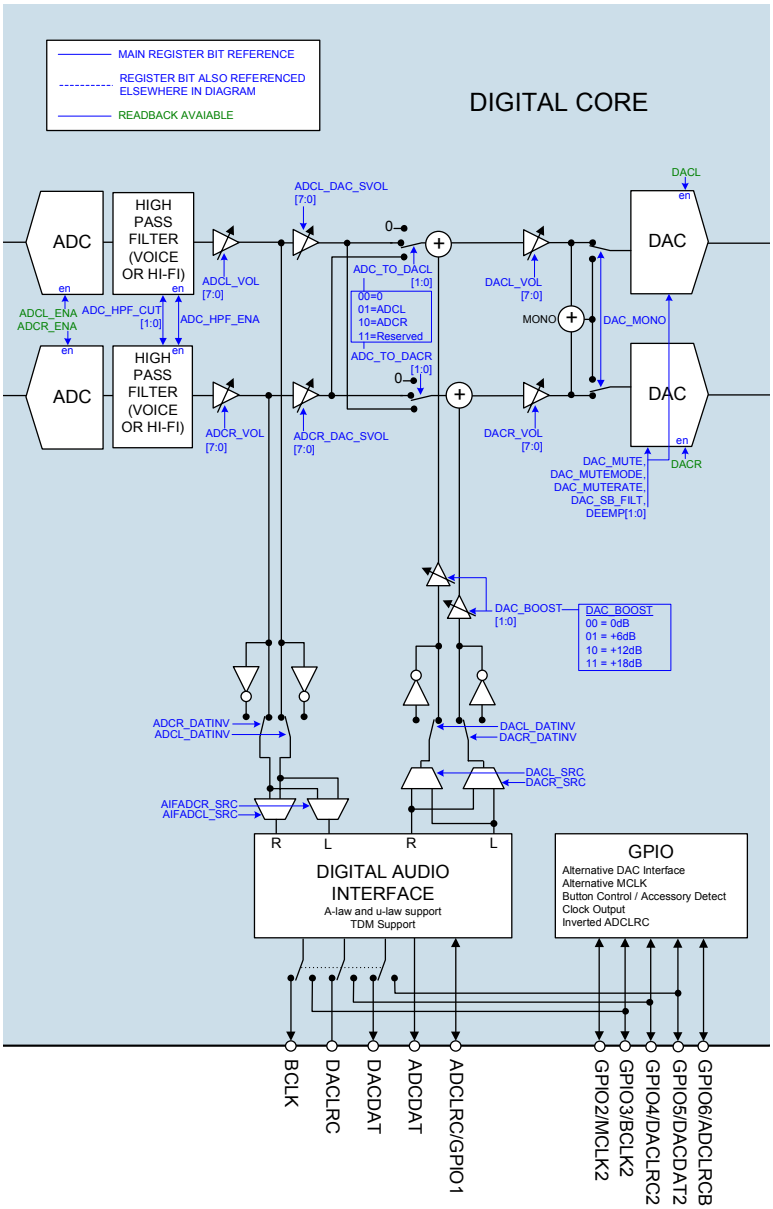


Figure 31 Digital Mixing Paths

The polarity of each ADC output signal can be changed under software control using the ADCL_DATINV and ADCR_DATINV register bits. The AIFADCL_SRC and AIFADCR_SRC register bits may be used to select which ADC is used for the left and right digital audio interface data. These register bits are described in Table 37.

The input data source for each DAC can be changed under software control using register bits DACL_SRC and DACR_SRC. The polarity of each DAC input may also be modified using register bits DACL_DATINV and DACR_DATINV. These register bits are described in Table 37.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h)	15	AIFADCL_SRC	0b	Left Digital Audio channel source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel
	14	AIFADCR_SRC	1b	Right Digital Audio channel source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
R15 (0Fh)	1	ADCL_DATINV	0b	Left ADC Invert 0 = Left ADC output not inverted 1 = Left ADC output inverted
	0	ADCR_DATINV	0b	Right ADC Invert 0 = Right ADC output not inverted 1 = Right ADC output inverted
R6 (06h)	15	DACL_SRC	0b	Left DAC Data Source Select 0 = Left DAC outputs left channel data 1 = Left DAC outputs right channel data
	14	DACR_SRC	1b	Right DAC Data Source Select 0 = Right DAC outputs left channel data 1 = Right DAC outputs right channel data
R11 (0Bh)	1	DACL_DATINV	0b	Left DAC Invert 0 = Left DAC output not inverted 1 = Left DAC output inverted
	0	DACR_DATINV	0b	Right DAC Invert 0 = Right DAC output not inverted 1 = Right DAC output inverted

Table 37 ADC / DAC Routing and Control

DAC INTERFACE VOLUME BOOST

A digital gain function is available at the audio interface to boost the DAC volume when a small signal is received on DACDAT. This is controlled using register bits DAC_BOOST[1:0]. To prevent clipping at the DAC input, this function should not be used when the boosted DAC data is expected to be greater than 0dBFS.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h)	11:10	DAC_BOOST [1:0]	00b	DAC Input Volume Boost 00 = 0dB 01 = +6dB (Input data must not exceed -6dBFS) 10 = +12dB (Input data must not exceed -12dBFS) 11 = +18dB (Input data must not exceed -18dBFS)

Table 38 DAC Interface Volume Boost

DIGITAL SIDETONE

A digital sidetone is available when ADCs and DACs are operating at the same sample rate. Digital data from either left or right ADC can be mixed with the audio interface data on the left and right DAC channels. Sidetone data is taken from the ADC high pass filter output, to reduce low frequency noise in the sidetone (e.g. wind noise or mechanical vibration).

The digital sidetone will not function when ADCs and DACs are operating at different sample rates.

When using the digital sidetone, it is recommended that the ADCs are enabled before un-muting the DACs to prevent pop noise. The DAC volumes and sidetone volumes should be set to an appropriate level to avoid clipping at the DAC input.

The digital sidetone is controlled as shown in Table 39.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 (0Eh)	12:9	ADCL_DAC_SVOL [3:0]	0000b	Left Digital Sidetone Volume (See Table 40 for volume range)
	8:5	ADCR_DAC_SVOL [3:0]	0000b	Right Digital Sidetone Volume (See Table 40 for volume range)
	3:2	ADC_TO_DACL [1:0]	00b	Left DAC Digital Sidetone Source 00 = No sidetone 01 = Left ADC 10 = Right ADC 11 = Reserved
	1:0	ADC_TO_DACR [1:0]	00b	Right DAC Digital Sidetone Source 00 = No sidetone 01 = Left ADC 10 = Right ADC 11 = Reserved

Table 39 Digital Sidetone Control

ADCL_DAC_SVOL or ADCR_DAC_SVOL	SIDETONE VOLUME
0000	-36
0001	-33
0010	-30
0011	-27
0100	-24
0101	-21
0110	-18
0111	-15
1000	-12
1001	-9
1010	-6
1011	-3
1100	0
1101	0
1110	0
1111	0

Table 40 Digital Sidetone Volume

DIGITAL TO ANALOGUE CONVERTER (DAC)

The WM8400 DACs receive digital input data from the DACDAT pin and via the digital sidetone path. The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

The analogue outputs from the DACs can then be mixed with other analogue inputs using the output mixers LOMIX, ROMIX and the speaker output mixer SPKMIX.

The DACs are enabled by the DACL_ENA and DACR_ENA register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h)	1	DACL_ENA (rw)	0b	Left DAC Enable 0 = DAC disabled 1 = DAC enabled
	0	DACR_ENA (rw)	0b	Right DAC Enable 0 = DAC disabled 1 = DAC enabled

Table 41 DAC Enable Control

DAC DIGITAL VOLUME CONTROL

The output level of each DAC can be controlled digitally over a range from -71.625dB to 0dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 192$; MUTE for $X = 0$ 0dB for $192 \leq X \leq 255$

The DAC_VU bit controls the loading of digital volume control data. When DAC_VU is set to 0, the DACL_VOL or DACR_VOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to DAC_VU. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch)	8	DAC_VU	N/A	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously
	7:0	DACL_VOL [7:0]	1100_0000b (0dB)	Left DAC Digital Volume (See Table 43 for volume range)
R13 (0Dh)	8	DAC_VU	N/A	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously
	7:0	DACR_VOL [7:0]	1100_0000b (0dB)	Right DAC Digital Volume (See Table 43 for volume range)

Table 42 DAC Digital Volume Control

DACL_VOL or DACR_VOL	Volume (dB)	DACL_VOL or DACR_VOL	Volume (dB)	DACL_VOL or DACR_VOL	Volume (dB)	DACL_VOL or DACR_VOL	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.000
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.000
3h	-70.875	43h	-46.875	83h	-22.875	C3h	0.000
4h	-70.500	44h	-46.500	84h	-22.500	C4h	0.000
5h	-70.125	45h	-46.125	85h	-22.125	C5h	0.000
6h	-69.750	46h	-45.750	86h	-21.750	C6h	0.000
7h	-69.375	47h	-45.375	87h	-21.375	C7h	0.000
8h	-69.000	48h	-45.000	88h	-21.000	C8h	0.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	0.000
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	0.000
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	0.000
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	0.000
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	0.000
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	0.000
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	0.000
10h	-66.000	50h	-42.000	90h	-18.000	D0h	0.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	0.000
12h	-65.250	52h	-41.250	92h	-17.250	D2h	0.000
13h	-64.875	53h	-40.875	93h	-16.875	D3h	0.000
14h	-64.500	54h	-40.500	94h	-16.500	D4h	0.000
15h	-64.125	55h	-40.125	95h	-16.125	D5h	0.000
16h	-63.750	56h	-39.750	96h	-15.750	D6h	0.000
17h	-63.375	57h	-39.375	97h	-15.375	D7h	0.000
18h	-63.000	58h	-39.000	98h	-15.000	D8h	0.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	0.000
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	0.000
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	0.000
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	0.000
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	0.000
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	0.000
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	0.000
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	0.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	0.000
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	0.000
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	0.000
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	0.000
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	0.000
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	0.000
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	0.000
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	0.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	0.000
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	0.000
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	0.000
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	0.000
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	0.000
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	0.000
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	0.000
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	0.000
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	0.000
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	0.000
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	0.000
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	0.000
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	0.000
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	0.000
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	0.000
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	0.000
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	0.000
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	0.000
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	0.000
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	0.000
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	0.000
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	0.000
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	0.000

Table 43 DAC Digital Volume Range

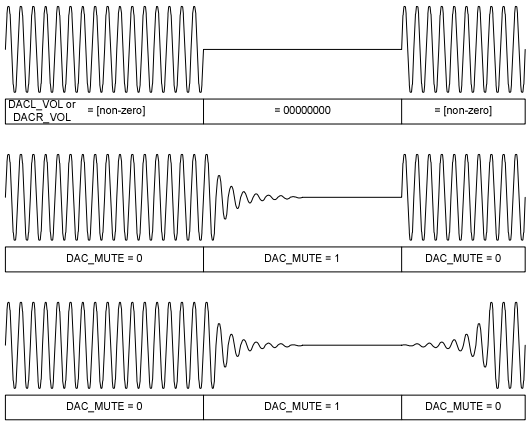
DAC SOFT MUTE AND SOFT UN-MUTE

The WM8400 has a soft mute function which, when enabled, gradually attenuates the volume of the DAC output. When soft mute is disabled, the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DAC_MUTEMODE register bit.

The DAC is soft-muted by default (DAC_MUTE = 1). To play back an audio signal, this function must first be disabled by setting DAC_MUTE to 0.

Soft Mute Mode would typically be enabled (DAC_MUTEMODE = 1) when using DAC_MUTE during playback of audio data so that when DAC_MUTE is subsequently disabled, the sudden volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing during a track).

Soft Mute Mode would typically be disabled (DAC_MUTEMODE = 0) when un-muting at the start of a music file, in order that the first part of the track is not attenuated (e.g. when starting playback of a new track, or resuming playback after pausing between tracks).



DAC muting and un-muting using volume control bits DACL_VOL and DACR_VOL.

DAC muting and un-muting using soft mute bit DAC_MUTE.

Soft Mute Mode not enabled (DAC_MUTEMODE = 0).

DAC muting and un-muting using soft mute bit DAC_MUTE.

Soft Mute Mode enabled (DAC_MUTEMODE = 1).

Figure 32 DAC Mute Control

The volume ramp rate during soft mute and un-mute is controlled by the DAC_MUTERATE bit. Ramp rates of fs/32 and fs/2 are selectable as shown in Table 44. The ramp rate determines the rate at which the volume will be increased or decreased. The actual ramp time depends on the extent of the difference between the muted and un-muted volume settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh)	7	DAC_MUTERATE	0b	DAC Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k)
	6	DAC_MUTEMODE	0b	DAC Soft Mute Mode 0 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to change immediately to DACL_VOL and DACR_VOL settings 1 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to ramp up gradually to the DACL_VOL and DACR_VOL settings
	2	DAC_MUTE	1b	DAC Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute

Table 44 DAC Soft-Mute Control

DAC MONO MIX

A DAC digital mono-mix mode can be enabled using the DAC_MONO register bit. This mono mix will be output on the enabled DACs. To prevent clipping, a -6dB attenuation is automatically applied to the mono mix.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh)	9	DAC_MONO	0b	DAC Mono Mix 0 = Stereo 1 = Mono (Mono mix output on enabled DACs)

Table 45 DAC Mono Mix

DAC DE-EMPHASIS

Digital de-emphasis can be applied to the DAC playback data (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz. See "Digital Filter Characteristics" section for details of de-emphasis filter characteristics.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh) ADC and DAC Control (1)	5:4	DEEMP [1:0]	00b	DAC De-Emphasis Control 00 = No de-emphasis 01 = 32kHz sample rate 10 = 44.1kHz sample rate 11 = 48kHz sample rate

Table 46 DAC De-Emphasis Control

DAC SLOPING STOPBAND FILTER

Two DAC filter types are available, selected by the register bit DAC_SB_FILT. When operating at lower sample rates (e.g. during voice communication) it is recommended that the sloping stopband filter type is selected (DAC_SB_FILT=1) to reduce out-of-band noise which can be audible at low DAC sample rates. See "Digital Filter Characteristics" section for details of DAC filter characteristics.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh)	8	DAC_SB_FILT	0b	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband mode

Table 47 DAC Sloping Stopband Filter

OUTPUT SIGNAL PATH

The WM8400 output routing and mixers provide a high degree of flexibility, allowing operation of many simultaneous signal paths through the device to various analogue outputs. The outputs provide many combinations of headphone, loudspeaker and single-ended line drivers. See “Analogue Outputs” for further details of these outputs.

The WM8400 output signal paths and control registers are illustrated in Figure 33.

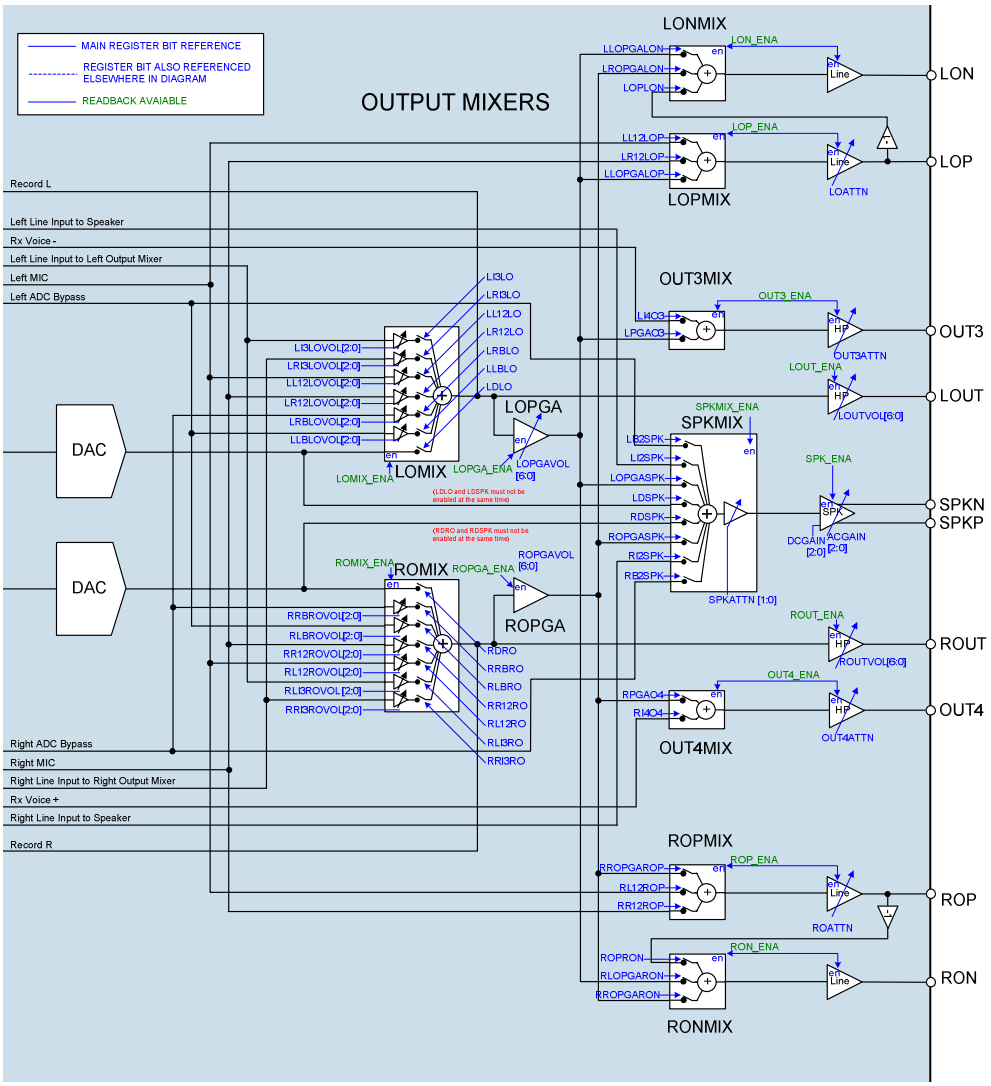


Figure 33 Control Registers for Output Signal Path

OUTPUT SIGNAL PATHS ENABLE

The output mixers and drivers can be independently enabled and disabled as described in Table 48.

Note that the headphone outputs LOUT and ROUT have dedicated volume controls. As a result, the output PGAs LOPGA and ROPGA do not need to be enabled to provide volume control for the LOUT and ROUT outputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h)	13	LON_ENA (rw)	0b	LON Line Out and LONMIX Enable 0 = disabled 1 = enabled
	12	LOP_ENA (rw)	0b	LOP Line Out and LOPMIX Enable 0 = disabled 1 = enabled
	11	RON_ENA (rw)	0b	RON Line Out and RONMIX Enable 0 = disabled 1 = enabled
	10	ROP_ENA (rw)	0b	ROP Line Out and ROPMIX Enable 0 = disabled 1 = enabled
	7	LOPGA_ENA (rw)	0b	LOPGA Left Volume Control Enable 0 = disabled 1 = enabled
	6	ROPGA_ENA (rw)	0b	ROPGA Right Volume Control Enable 0 = disabled 1 = enabled
	5	LOMIX_ENA (rw)	0b	LOMIX Left Output Mixer Enable 0 = disabled 1 = enabled
	4	ROMIX_ENA (rw)	0b	ROMIX Right Output Mixer Enable 0 = disabled 1 = enabled
R2 (02h)	13	SPK_MIX_ENA (rw)	0b	Speaker Mixer Enable 0 = disabled 1 = enabled
	12	SPK_ENA (rw)	0b	Speaker Output Enable 0 = disabled 1 = enabled
	11	OUT3_ENA (rw)	0b	OUT3 and OUT3MIX Enable 0 = disabled 1 = enabled
	10	OUT4_ENA (rw)	0b	OUT4 and OUT4MIX Enable 0 = disabled 1 = enabled
	9	LOUT_ENA (rw)	0b	LOUT (Left Headphone Output) Enable 0 = disabled 1 = enabled
	8	ROUT_ENA (rw)	0b	ROUT (Right Headphone Output) Enable 0 = disabled 1 = enabled

Table 48 Output Signal Paths Enable

OUTPUT MIXER CONTROL

The Output Mixer volume controls are described in Table 49 for the Left Channel and Table 50 for the Right Channel. The gain of each of analogue input paths may be controlled independently in the range described in Table 51. The DAC input levels may be controlled by the DAC digital volume control - see "Digital to Analogue Converter (DAC)" for further details of this control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 (2Dh)	5	LRI3LO	0b	RIN3 to LOMIX Mute 0 = Mute 1 = Un-mute
R49 (31h)	8:6	LRI3LOVOL [2:0]	000b	RIN3 to LOMIX Volume (See Table 51 for Volume Range)
R45 (2Dh)	4	LLI3LO	0b	LIN3 to LOMIX Mute 0 = Mute 1 = Un-mute
R47 (2Fh)	8:6	LLI3LOVOL [2:0]	000b	LIN3 to LOMIX Volume (See Table 51 for Volume Range)
R45 (2Dh)	3	LR12LO	0	RIN12 PGA Output to LOMIX Mute 0 = Mute 1 = Un-mute
R47 (2Fh)	5:3	LR12LOVOL [2:0]	000b	RIN12 PGA Output to LOMIX Volume (See Table 51 for Volume Range)
R45 (2Dh)	2	LL12LO	0b	LIN12 PGA Output to LOMIX Mute 0 = Mute 1 = Un-mute
R47 (2Fh)	2:0	LL12LOVOL [2:0]	000b	LIN12 PGA Output to LOMIX Volume (See Table 51 for Volume Range)
R45 (2Dh)	7	LRBLO	0b	AINRMUX Output (Right ADC bypass) to LOMIX Mute 0 = Mute 1 = Un-mute
R49 (31h)	5:3	LRBLOVOL [2:0]	000b	AINRMUX Output (Right ADC bypass) to LOMIX Volume (See Table 51 for Volume Range)
R45 (2Dh)	6	LLBLO	0b	AINLMUX Output (Left ADC bypass) to LOMIX Mute 0 = Mute 1 = Un-mute
R49 (31h)	2:0	LLBLOVOL [2:0]	000b	AINLMUX Output (Left ADC bypass) to LOMIX Volume (See Table 51 for Volume Range)
R45 (2Dh)	0	LDLO	0b	Left DAC to LOMIX Mute 0 = Mute 1 = Un-mute Note: LDLO must be muted when LDSPK=1

Table 49 Left Output Mixer (LOMIX) Volume Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R46 (2Eh)	5	RLI3RO	0b	LIN3 to ROMIX Mute 0 = Mute 1 = Un-mute
R50 (32h)	8:6	RLI3ROVOL [2:0]	000b	LIN3 to ROMIX Volume (See Table 51 for Volume Range)
R46 (2Eh)	4	RRI3RO	0b	RIN3 to ROMIX Mute 0 = Mute 1 = Un-mute
R48 (30h)	8:6	RRI3ROVOL [2:0]	000b	RIN3 to ROMIX Volume (See Table 51 for Volume Range)
R46 (2Eh)	3	RL12RO	0b	LIN12 PGA Output to ROMIX Mute 0 = Mute 1 = Un-mute
R48 (30h)	5:3	RL12ROVOL [2:0]	000b	LIN12 PGA Output to ROMIX Volume (See Table 51 for Volume Range)
R46 (2Eh)	2	RR12RO	0b	RIN12 PGA Output to ROMIX Mute 0 = Mute 1 = Un-mute
R48 (30h)	2:0	RR12ROVOL [2:0]	000b	RIN12 PGA Output to ROMIX Volume (See Table 51 for Volume Range)
R46 (2Eh)	7	RLBRO	0b	AINLMUX Output (Left ADC bypass) to ROMIX Mute 0 = Mute 1 = Un-mute
R50 (32h)	5:3	RLBROVOL [2:0]	000b	AINLMUX Output (Left ADC bypass) to ROMIX Volume (See Table 51 for Volume Range)
R46 (2Eh)	6	RRBRO	0b	AINRMUX Output (Right ADC bypass) to ROMIX 0 = Mute 1 = Un-mute
R50 (32h)	2:0	RRBROVOL [2:0]	000b	AINRMUX Output (Right ADC bypass) to ROMIX Volume (See Table 51 for Volume Range)
R46 (2Eh)	0	RDRO	0b	Right DAC to ROMIX Mute 0 = Mute 1 = Un-mute Note: RDRO must be muted when RDSPK=1

Table 50 Right Output Mixer (ROMIX) Volume Control

VOLUME SETTING	VOLUME (dB)
000	0
001	-3
010	-6
011	-9
100	-12
101	-15
110	-18
111	-21

Table 51 LOMIX and ROMIX Volume Range

OUTPUT SIGNAL PATH VOLUME CONTROL

The output drivers LOPGA, ROPGA, LOUT and ROUT can be independently controlled as shown in Table 52 and Table 53.

To minimise pop noise it is recommended that only the LOPGAVOL, ROPGAVOL, LOUTVOL and ROUTVOL are modified while the output signal path is active. Other gain controls are provided in the output signal path to provide appropriate relative scaling of signals from different sources, and to prevent clipping when multiple signals are mixed. To prevent pop noise, only the gain controls noted above should be modified while playback is active.

To prevent "zipper noise", a zero-cross function is provided on these output paths, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOCLK_ENA register bit), the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout period is set by TOCLK_RATE. See “Clocking and Sample Rates” for more information on these fields.

The OPVU bit controls the loading of the output driver volume data. When OPVU is set to 0, the volume control data will be loaded into the respective control register, but will not actually change the gain setting. The LOPGA, ROPGA, LOUT and ROUT volume settings are all updated when a 1 is written to OPVU. This makes it possible to update the gain of all output paths simultaneously.

Note that the headphone outputs LOUT and ROUT have dedicated volume controls. As a result, the output PGAs LOPGA and ROPGA do not need to be enabled to provide volume control for the LOUT and ROUT outputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h)	8	OPVU[2]	N/A	Output PGA Volume Update Writing a 1 to this bit will update LOPGA, ROPGA, LOUTVOL and ROUTVOL volumes simultaneously.
	7	LOPGAZC	0b	LOPGA Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6:0	LOPGAVOL [6:0]	79h (0dB)	LOPGA Volume (See Table 53 for output PGA volume control range)
R33 (21h)	8	OPVU[3]	N/A	Output PGA Volume Update Writing a 1 to this bit will update LOPGA, ROPGA, LOUTVOL and ROUTVOL volumes simultaneously.
	7	ROPGAZC	0b	ROPGA Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6:0	ROPGAVOL [6:0]	79h (0dB)	ROPGA Volume (See Table 53 for output PGA volume control range)
R28 (1Ch)	8	OPVU[0]	N/A	Output PGA Volume Update Writing a 1 to this bit will update LOPGA, ROPGA, LOUTVOL and ROUTVOL volumes simultaneously.
	7	LOZC	0b	LOUT (Left Headphone Output) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6:0	LOUTVOL [6:0]	00h (mute)	LOUT (Left Headphone Output) Volume (See Table 53 for output PGA volume control range)
R29 (1Dh)	8	OPVU[1]	N/A	Output PGA Volume Update Writing a 1 to this bit will update LOPGA, ROPGA, LOUTVOL and ROUTVOL volumes simultaneously.
	7	ROZC	0b	ROUT (Right Headphone Output) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6:0	ROUTVOL [6:0]	00h (mute)	ROUT (Right Headphone Output) Volume (See Table 53 for output PGA volume control range)

Table 52 LOPGA, ROPGA, LOUT and ROUT Volume Control

LOPGAVOL, ROPGAVOL, LOUTVOL or ROUTVOL	Volume (dB)	LOPGAVOL, ROPGAVOL, LOUTVOL or ROUTVOL	Volume (dB)
0h	MUTE	40h	-57.000
1h	MUTE	41h	-56.000
2h	MUTE	42h	-55.000
3h	MUTE	43h	-54.000
4h	MUTE	44h	-53.000
5h	MUTE	45h	-52.000
6h	MUTE	46h	-51.000
7h	MUTE	47h	-50.000
8h	MUTE	48h	-49.000
9h	MUTE	49h	-48.000
Ah	MUTE	4Ah	-47.000
Bh	MUTE	4Bh	-46.000
Ch	MUTE	4Ch	-45.000
Dh	MUTE	4Dh	-44.000
Eh	MUTE	4Eh	-43.000
Fh	MUTE	4Fh	-42.000
10h	MUTE	50h	-41.000
11h	MUTE	51h	-40.000
12h	MUTE	52h	-39.000
13h	MUTE	53h	-38.000
14h	MUTE	54h	-37.000
15h	MUTE	55h	-36.000
16h	MUTE	56h	-35.000
17h	MUTE	57h	-34.000
18h	MUTE	58h	-33.000
19h	MUTE	59h	-32.000
1Ah	MUTE	5Ah	-31.000
1Bh	MUTE	5Bh	-30.000
1Ch	MUTE	5Ch	-29.000
1Dh	MUTE	5Dh	-28.000
1Eh	MUTE	5Eh	-27.000
1Fh	MUTE	5Fh	-26.000
20h	MUTE	60h	-25.000
21h	MUTE	61h	-24.000
22h	MUTE	62h	-23.000
23h	MUTE	63h	-22.000
24h	MUTE	64h	-21.000
25h	MUTE	65h	-20.000
26h	MUTE	66h	-19.000
27h	MUTE	67h	-18.000
28h	MUTE	68h	-17.000
29h	MUTE	69h	-16.000
2Ah	MUTE	6Ah	-15.000
2Bh	MUTE	6Bh	-14.000
2Ch	MUTE	6Ch	-13.000
2Dh	MUTE	6Dh	-12.000
2Eh	MUTE	6Eh	-11.000
2Fh	MUTE	6Fh	-10.000
30h	-73.000	70h	-9.000
31h	-72.000	71h	-8.000
32h	-71.000	72h	-7.000
33h	-70.000	73h	-6.000
34h	-69.000	74h	-5.000
35h	-68.000	75h	-4.000
36h	-67.000	76h	-3.000
37h	-66.000	77h	-2.000
38h	-65.000	78h	-1.000
39h	-64.000	79h	0.000
3Ah	-63.000	7Ah	1.000
3Bh	-62.000	7Bh	2.000
3Ch	-61.000	7Ch	3.000
3Dh	-60.000	7Dh	4.000
3Eh	-59.000	7Eh	5.000
3Fh	-58.000	7Fh	6.000

Table 53 LOPGA, ROPGA, LOUT and ROUT Volume Range

The speaker mixer SPKMIX and its outputs SPKN and SPKP are controlled as described in Table 54. Care should be taken to avoid clipping when enabling more than one path to the speaker mixer. Register bits SPKATTN control the speaker output attenuation and can be used to avoid clipping when more than one full scale signal is input to the mixer.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R54 (36h)	7	LB2SPK	0b	AINLMUX Output to SPKMIX 0 = Mute 1 = Un-mute
	6	RB2SPK	0b	AINRMUX Output to SPKMIX 0 = Mute 1 = Un-mute
	5	LI2SPK	0b	LIN2 to SPKMIX 0 = Mute 1 = Un-mute
	4	RI2SPK	0b	RIN2 to SPKMIX 0 = Mute 1 = Un-mute
	3	LOPGASPK	0b	LOPGA to SPKMIX 0 = Mute 1 = Un-mute
	2	ROPGASPK	0b	ROPGA to SPKMIX 0 = Mute 1 = Un-mute
	1	LDSPK	0b	Left DAC to SPKMIX 0 = Mute 1 = Un-mute Note: LDSPK must be muted when LDLO=1
	0	RDSPK	0b	Right DAC to SPKMIX 0 = Mute 1 = Un-mute Note: RDSPK must be muted when RDRO=1
R34 (22h)	1:0	SPKATTN [1:0]	11b	Speaker Output Attenuation (SPKN and SPKP) 00 = 0dB 01 = -6dB 10 = -12dB 11 = mute

Table 54 Speaker Output Volume Control

The output mixers OUT3MIX and OUT4MIX and their outputs OUT3 and OUT4 are controlled as described in Table 55. Care should be taken to avoid clipping when enabling more than one path to OUT3 or OUT4. The OUT3ATTN and OUT4ATTN attenuation controls can be used to prevent clipping when more than one full scale signal is input to the mixers.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh)	5	OUT3MUTE	1b	OUT3 Mute 0 = Un-mute 1 = Mute
	4	OUT3ATTN	0b	OUT3 Attenuation 0 = 0dB 1 = -6dB
	1	OUT4MUTE	1b	OUT4 Mute 0 = Un-mute 1 = Mute
	0	OUT4ATTN	0b	OUT4 Attenuation 0 = 0dB 1 = -6dB
R51 (33h)	5	LI4O3	0b	LIN4/RXN Pin to OUT3MIX 0 = Mute 1 = Un-mute
	4	LPGAO3	0b	LOPGA to OUT3MIX 0 = Mute 1 = Un-mute
	1	RI4O4	0b	RIN4/RXP Pin to OUT4MIX 0 = Mute 1 = Un-mute
	0	RPGAO4	0b	ROPGA to OUT4MIX 0 = Mute 1 = Un-mute

Table 55 OUT3 and OUT4 Volume Control

The output mixers LOPMIX and LONMIX and their outputs LOP and LON are controlled as described in Table 56. Care should be taken to avoid clipping when enabling more than one path to LOP or LON. The LOATTN attenuation control can be used to prevent clipping when more than one full scale signal is input to the LOP mixer.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (1Eh)	6	LONMUTE	1b	LON Line Output Mute 0 = Un-mute 1 = Mute
	5	LOPMUTE	1b	LOP Line Output Mute 0 = Un-mute 1 = Mute
	4	LOATTN	0b	LOP Attenuation 0 = 0dB 1 = -6dB
R52 (34h)	6	LLOPGALON	0b	LOPGA to LONMIX 0 = Mute 1 = Un-mute
	5	LROPGALON	0b	ROPGA to LONMIX 0 = Mute 1 = Un-mute
	4	LOPLON	0b	Inverted LOP Output to LONMIX 0 = Mute 1 = Un-mute
	2	LR12LOP	0b	RIN12 PGA Output to LOPMIX 0 = Mute 1 = Un-mute
	1	LL12LOP	0b	LIN12 PGA Output to LOPMIX 0 = Mute 1 = Un-mute
	0	LLOPGALOP	0b	LOPGA to LOPMIX 0 = Mute 1 = Un-mute

Table 56 LOP and LON Volume Control

The output mixers ROPMIX and RONMIX and their outputs ROP and RON are controlled as described in Table 57. Care should be taken to avoid clipping when enabling more than one path to ROP or RON. The ROATTN attenuation control can be used to prevent clipping when more than one full scale signal is input to the ROP mixer.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (1Eh)	2	RONMUTE	1b	RON Line Output Mute 0 = Un-mute 1 = Mute
	1	ROPMUTE	1b	ROP Line Output Mute 0 = Un-mute 1 = Mute
	0	ROATTN	0b	ROP Attenuation 0 = 0dB 1 = -6dB
R53 (35h)	6	RROPGARON	0b	ROPGA to RONMIX 0 = Mute 1 = Un-mute
	5	RLOPGARON	0b	LOPGA to RONMIX 0 = Mute 1 = Un-mute
	4	ROPRON	0b	Inverted ROP Output to RONMIX 0 = Mute 1 = Un-mute
	2	RL12ROP	0b	LIN12 PGA Output to ROPMIX 0 = Mute 1 = Un-mute
	1	RR12ROP	0b	RIN12 PGA Output to ROPMIX 0 = Mute 1 = Un-mute
	0	RROPGAROP	0b	ROPGA to ROPMIX 0 = Mute 1 = Un-mute

Table 57 ROP and RON Volume Control

ANALOGUE BIAS OPTIMISATION

The AVDD supply of the WM8400 can operate between 2.7V and 3.6V. By default, all analogue circuitry on the device is optimised to run at 3.0V.

At lower voltages, an increased bias current may be selected. The default bias current may still be used (for lower power operation), but this may result in degraded performance of the outputs OUT3, OUT4, LOUT and ROUT. The bias current is controlled as shown in Table 58.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R51 (33h)	8:7	VSEL [1:0]	11	Analogue Bias Optimisation 00 = Reserved 01 = Bias current optimised for AVDD=2.7V 1X = Bias current optimised for AVDD=3.0V

Table 58 Bias Optimisation

ANALOGUE OUTPUTS

The speaker, headphone and line outputs are highly configurable and may be used in many different ways.

SPEAKER OUTPUT CONFIGURATIONS

The speaker outputs SPKP and SPKN are driven by the speaker mixer SPKMIX, which can output a mix that is any combination of the following signals:

- Left DAC and Right DAC outputs
- LOMIX and ROMIX outputs via volume controls LOPGA and ROPGA
- Line inputs LIN2 and RIN2
- Output from left and right input mixers (AINLMUX and AINRMUX)

The speaker mixer is controlled as described under “Output Signal Path”. The speaker mixer output can be attenuated to avoid clipping when mixing multiple signal inputs.

The speaker outputs SPKP and SPKN operate in a BTL configuration in Class AB and Class D amplifier modes. The mode is selected by register bit CDMODE. The outputs are capable of driving 1W into an 8Ω BTL load (or 500mW in class AB mode for thermal reasons) at room temperature. For performance at higher temperatures, see Figure 1 in the “Recommended Operating Conditions” section. Ultra-low leakage and high PSRR allow the speaker supply SPKVDD to be directly connected to a lithium battery.

Six levels of AC and DC signal boost are provided in order to deliver maximum output power for many commonly-used SPKVDD/AVDD combinations. These boost options are available in both Class AB and Class D modes. The AC and DC gain levels from 1.0x to 1.8x are selected using register bits ACGAIN and DCGAIN. To prevent pop noise, DCGAIN and ACGAIN should not be modified while the speaker outputs are enabled.

Note that an appropriate SPKVDD supply voltage must be provided to prevent waveform clipping when speaker boost is used.

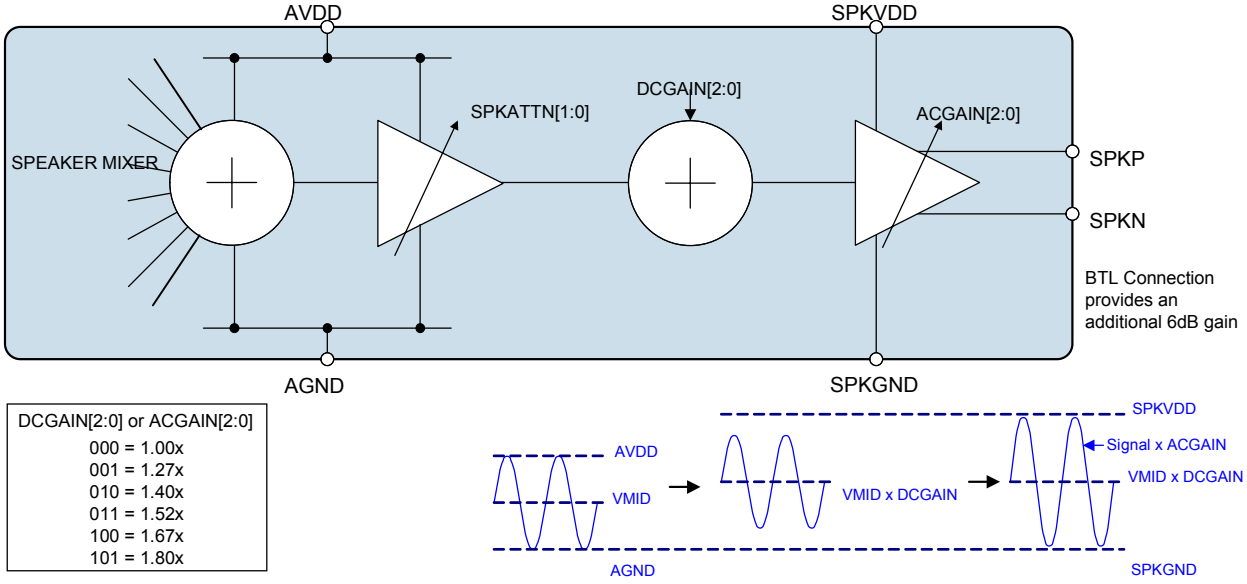


Figure 34 Speaker Boost Operation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 (23h)	8	CDMODE	0b	Speaker Class D Mode Enable 0 = Class D mode 1 = Class AB mode
R37 (25h)	5:3	DCGAIN [2:0]	000b (1.0x)	DC Speaker Boost 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.80x boost (+5.1dB) 110 to 111 = Reserved
	2:0	ACGAIN [2:0]	000b (1.0x)	AC Speaker Boost 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.80x boost (+5.1dB) 110 to 111 = Reserved

Table 59 Speaker Boost Control

In Class D mode, the Class D switching clock must be configured as described earlier (see "Clocking and Sample Rates). See Table 12 for definitions of the associated register fields.

HEADPHONE OUTPUT CONFIGURATIONS

The headphone outputs LOUT, ROUT, OUT3 and OUT4 are each driven by different output mixers as described below.

The LOUT and ROUT pins output the LOMIX and ROMIX outputs respectively.

The output mixer OUT3MIX produces an output OUT3 that is a combination of:

- LIN4/RXN
- LOMIX output via volume control LOPGA

The output mixer OUT4MIX produces an output OUT4 that is a combination of:

- RIN4/RXP
- ROMIX output via volume control ROPGA

Full volume control is available on LOUT and ROUT. 0dB and -6dB attenuation is available on OUT3 and OUT4, with full volume control available using LOPGA and ROPGA for the LOMIX and ROMIX signals.

The outputs LOUT, ROUT, OUT3 and OUT4 are capable of driving 40mW into 16Ω loads such as stereo headsets, headphones, and/or a handset ear speaker. AC-coupled, capless mode and fully differential headphone drive modes are available.

AC-coupled output is possible on each of LOUT, ROUT, OUT3 and OUT4 simultaneously.

Capless headphone output is possible on LOUT and ROUT by using either OUT3 or OUT4 as the common return path. (This is achieved by muting OUT3 or OUT4 as required.)

If RXP and RXN are a mono differential input (e.g. a connection to an external voice CODEC), then OUT3 and OUT4 may be used as a differential output capable of driving a handset ear speaker. The signal paths from RXP to OUT4 and from RXN to OUT3 are direct, and do not pass through any additional amplifiers. This reduces standby and active power consumption and improves signal quality.

When driving a handset ear speaker using OUT3 and OUT4 other than from RXP/RXN, the required phase difference can be provided by inverting one of the DAC outputs or alternatively by mixing Left and Right channels together using either LOMIX or ROMIX and muting the opposite channel.

Note that a differential output will provide an additional 6dB gain at the output pins. Register bits OUT3ATTN and OUT4ATTN can be used to compensate for this gain if required.

Fully differential headphone drive is possible between LOUT and OUT3 and between ROUT and OUT4. Routing LOPGA to OUT3 and ROPGA to OUT4 results in a phase inversion at LOUT with respect to OUT3 and at ROUT with respect to OUT4. This allows fully differential headset drive, with greatly improved crosstalk performance, improved bass response, increased noise immunity and removing the need for large and expensive DC-blocking capacitors.

To ensure fully balanced differential operation, LOUT and OUT3 must be set to the same gain as each other, and ROUT and OUT4 must be set to the same gain as each other. This is best achieved by setting OUT3ATTN and OUT4ATTN to 0dB, whilst setting volume controls LOPGAVOL and LOUTVOL at matching levels and setting volume controls ROPGAVOL and ROUTVOL at matching levels.

Some example headphone output configurations are shown below.

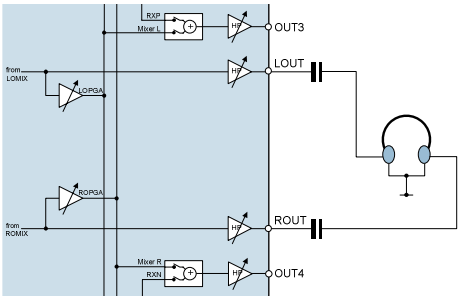


Figure 35 AC-Coupled Headphone Drive

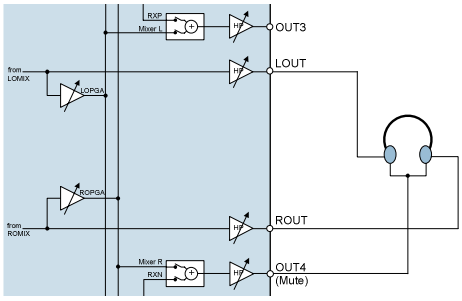


Figure 36 Capless Mode Headphone Drive

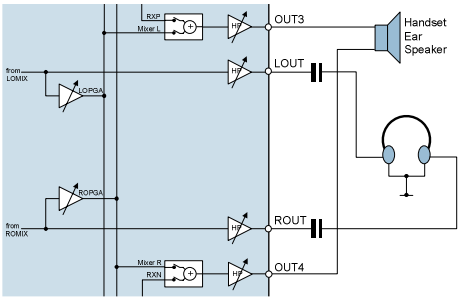


Figure 37 Headphone and Ear Speaker Drive

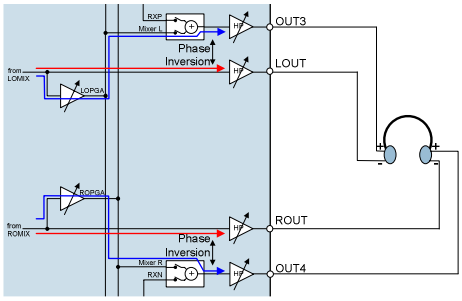


Figure 38 Fully Differential Headphone Drive

LINE OUTPUT CONFIGURATIONS

The line outputs LON, LOP, RON and ROP are each driven by different output mixers as described below.

The LOP and ROP pins output a mix of LIN12 input PGA, RIN12 input PGA and either LOMIX or ROMIX outputs.

The LON output is a mix of ROMIX, LOMIX and a phase-inverted copy of LOP.

The RON output is a mix of LOMIX, ROMIX and a phase-inverted copy of ROP.

Volume control of LOMIX and ROMIX is available in all cases above via LOPGA and ROPGA. An additional -6dB attenuation option is provided on LOP and ROP outputs.

The outputs LON, LOP, RON and ROP are capable of driving line loads only. Single ended output is possible on all these output simultaneously. Differential output is also possible between LOP and LON and between ROP and RON.

Typical applications for the line outputs (single-ended or differential) are:

- Handset or headset microphone output to external voice CODEC
- Stereo line output
- Output to external speaker driver(s) to support stereo loudspeakers

Some example line output configurations are shown below.

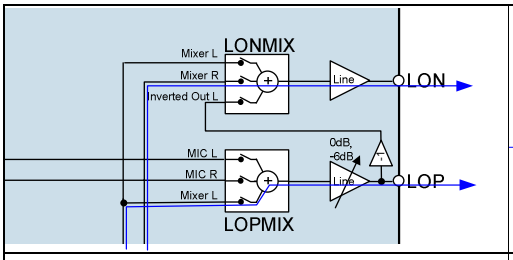


Figure 39 Stereo Line Out (A)

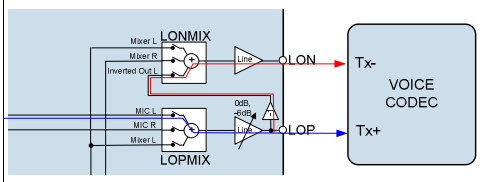


Figure 40 Differential Output of MIC PGA

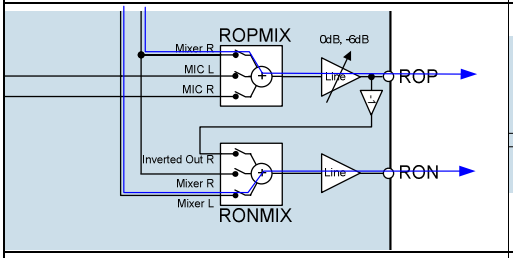


Figure 41 Stereo Line Out (B)

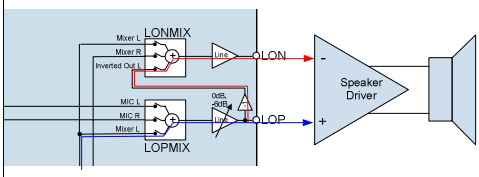


Figure 42 Differential Output to Speaker Driver

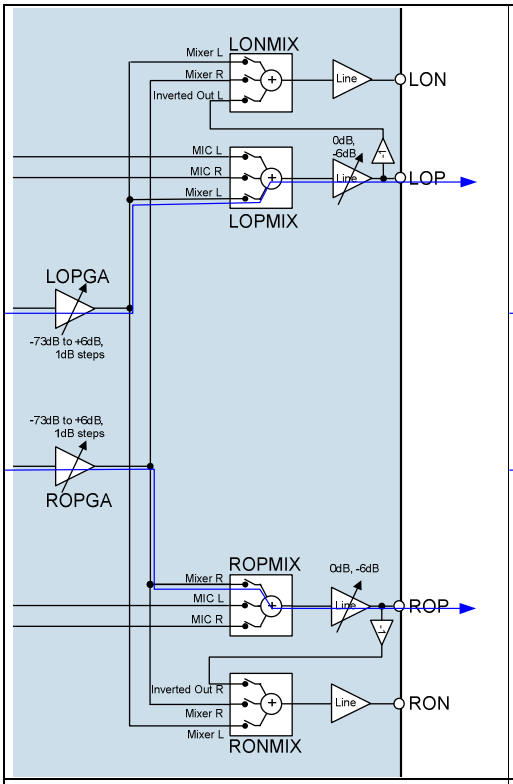


Figure 43 Stereo Line Out (C)

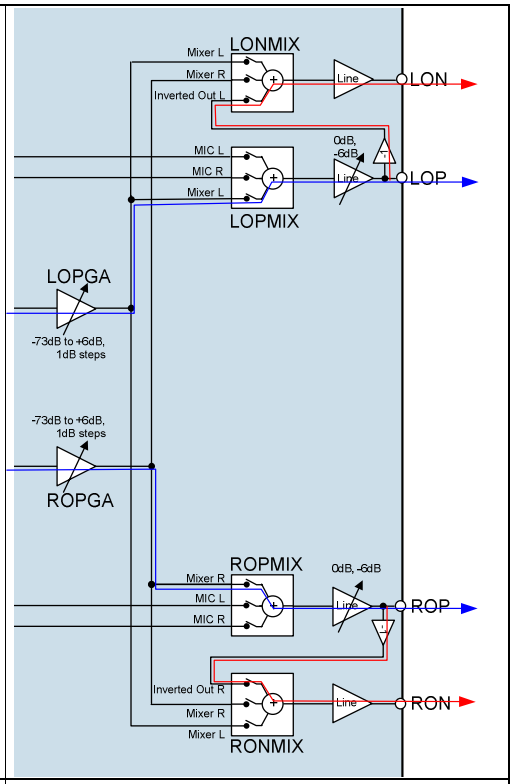


Figure 44 Stereo Differential Line Out

DISABLED OUTPUTS

Whenever an analogue output is disabled, it remains connected to VREF through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between VREF and each output can be controlled using register bit VROI. By default, a high resistance is used - 20kΩ for Headphone outputs (LOUT, ROUT, OUT3 and OUT4) and 10kΩ for Line outputs (LON, LOP, RON and ROP). If a low impedance is desired for disabled outputs, VROI can then be set to 1, decreasing the resistance to about 500Ω in all cases.

Note that a disabled output may be used as a common ground connection for a capless headphone output as described earlier.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R55 (37h) Additional Control	0	VROI	0	VREF to Analogue Output Resistance (Disabled Outputs) 0 = 20kΩ (Headphone) or 10kΩ (Line Out) from buffered VMID to output 1 = 500Ω from buffered VMID to output

Table 60 Disabled Outputs to VREF Resistance

GENERAL PURPOSE INPUT/OUTPUT

The WM8400 provides a number of versatile GPIO functions to enable features such as mobile TV support, Wi-Fi voice call recording, button and accessory detection and clock output.

The WM8400 has eight multi-purpose pins for these functions.

- GPIO1 to GPIO6: Dedicated GPIO pins.
- LIN3/GPI7 and RIN3/GPI8: Analogue inputs or button/accessory detect inputs.

The following functions are available on some or all of the GPIO pins.

- Alternative DAC interface (DACDAT, DACLRC, BCLK)
- Button detect (latched with programmable de-bounce)
- MICBIAS / Accessory current or short circuit detect
- Alternative MCLK input
- Clock output
- Inverted ADCLRC output
- Temperature sensor output
- FLL lock output
- Logic '1' and logic '0' output
- CODEC Interrupt Event output

Note that the CODEC Interrupt relates only to the functions described in this section. The Power Management Interrupt, and the dedicated NIRQ pin, are described separately in the “Interrupt Events” section. The Jack Detect (GPI7 and GPI8), MICBIAS and Temperature sensor functions are effective in both the CODEC Interrupt and Power Management Interrupt circuits.

The functions available on each of the GPIO pins are identified in Table 61.

	GPIO PINS							
GPIO Pin Function	**GPIO1**	**GPIO2**	**GPIO3**	**GPIO4**	**GPIO5**	**GPIO6**	**GPI7**	**GPI8**
ADCLRC	Y							
MCLK2		Y						
BCLK2			Y					
DACLRC2				Y				
DACDAT2					Y			
ADCLRCB						Y		
Button/Accessory Detect Input	Y	Y	Y	Y	Y	Y	Y	Y
Clock Output	Y	Y	Y	Y	Y	Y		
Temperature OK	Y	Y	Y	Y	Y	Y		
FLL Lock	Y	Y	Y	Y	Y	Y		
Logic 1 and Logic 0	Y	Y	Y	Y	Y	Y		
Interrupt	Y	Y	Y	Y	Y	Y		
Pull-up & Pull-down Available	Y	Y	Y	Y	Y	Y		

Table 61 Functions Available on GPIO Pins

The GPIO pins are configured by a combination of register settings described in Table 62 to Table 64 in the following section. The order of precedence for the control of the GPIO pins is as listed below.

1. Pin pull-up or pull-down (GPIOn_PU, GPIOn_PD)
2. Audio Interface and GPIO Tristate (AIF_TRIS)
3. Pin configuration (AIFSEL, MCLK_SRC, ALRCGPIO1, and ALRCBGPIO6)
4. GPIO functionality (GPIOn_SEL)

GPIO POWER DOMAIN

Operation of the GPIO functions or the secondary DAC interface requires an appropriate power supply to be connected to the I2S2VDD power domain. This supply is referenced to GND. The operating range for this supply is detailed in the “Recommended Operating Conditions” section.

GPIO CONTROL REGISTERS

Table 62 shows how the dual-function GPIO pins are configured to operate in their different modes. Note that the order of precedence described earlier applies.

Register field AIF_SEL selects the function of GPIO3, GPIO4 and GPIO5 between Audio Interface 2 and GPIO functions.

Register field ALRCGPIO1 enables the GPIO functionality on GPIO1.

Register field MCLK_SRC enables the GPIO functionality on GPIO2.

Register field ALRCGPIO6 enables the inverted ADCLRC output on GPIO6.

Register bit AIF_TRIS, when set, takes precedence over AIF_SEL, ALRCGPIO1, MCLK_SRC and ALRCBGPIO6 and tri-states all GPIO pins.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h)	15	MCLK_SRC	0b	MCLK Source Select 0 = MCLK pin 1 = GPIO2/MCLK2 pin
R9 (09h)	13	AIF_SEL	0b	Audio Interface Select 0 = Audio interface 1 1 = Audio interface 2 (GPIO3/BCLK2, GPIO4/DACLRC2, GPIO5/DACDAT2)
R10 (0Ah)	15	ALRCGPIO1	0b	ADCLRC/GPIO1 Pin Function Select 0 = ADCLRC 1 = GPIO1 (ADCLRC connected to DACLRC internally)
	14	ALRCBGPIO6	0b	GPIO6/ADCLRCB Pin Function Select 0 = GPIO6 1 = Inverted ADCLRC clock output
	13	AIF_TRIS	0b	Audio Interface and GPIO Tristate 0 = Audio interface and GPIO pins operate normally 1 = Tristate all audio interface and GPIO pins

Table 62 GPIO and GPI Pin Function Select

The GPIO pins are also controlled by the register fields described in Table 63. Note the order of precedence described earlier applies. Accordingly, note that the GPIO*n*_SEL field is only effective when GPIO*n*_PU, GPIO*n*_PD, AIF_TRIS, AIFSEL, MCLK_SRC, ALRCGPIO1 and ALRCBGPIO6 are set to allow GPIO functionality on that GPIO pin.

The function of the GPIO pins can be selected using the GPIO*n*_SEL field, where *n* = 1 to 6, according to the respective GPIO pin. The available functions are described individually in the subsequent sections. Internal pull-up and pull-down resistors can be enabled for interfacing with external signal sources or push-buttons. Pull-down resistors are enabled on GPIO2, GPIO3, GPIO4, GPIO5 and GPIO6 by default.

Each of the GPIO pins (also including GPI7 and GPI8) may be configured as an input. In this configuration, the respective GPIO is an input to the CODEC Interrupt function, with selectable enable, de-bounce and polarity control. The associated interrupt bits (GPIO_STATUS) are latched once set and can be polled at any time or used to generate CODEC Interrupt events. See “CODEC Interrupt Event Output” for more details of the CODEC Interrupt event handling.

The interrupt bits are latched once set; they are reset by writing a logic '1' to the applicable GPIO_STATUS register bits. De-bouncing is provided in order to avoid false event triggers. Note that TOCLK must be enabled when this input de-bouncing is required.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h)	7:0	GPIO_STATUS [7:0] (rr)	0b	GPIO and GPI Input Pin Status GPIO_STATUS[7] = GPI8 pin status GPIO_STATUS[6] = GPI7 pin status GPIO_STATUS[5] = GPIO6 status GPIO_STATUS[4] = GPIO5 status GPIO_STATUS[3] = GPIO4 status GPIO_STATUS[2] = GPIO3 status GPIO_STATUS[1] = GPIO2 status GPIO_STATUS[0] = GPIO1 status These bits are latched once set. The GPIO_POL bits determine the polarity of the input event to set these bits. They are cleared when a '1' is written.
R19 (13h)	15	GPIO2_DEB_ENA	0b	See Table 64 for GPIO2 control bit description
	14	GPIO2_IRQ_ENA	0b	
	13	GPIO2_PU	0b	
	12	GPIO2_PD	1b	
	11:8	GPIO2_SEL[3:0]	0000b	
	7	GPIO1_DEB_ENA	0b	See Table 64 for GPIO1 control bit description
	6	GPIO1_IRQ_ENA	0b	
	5	GPIO1_PU	0b	
	4	GPIO1_PD	0b	
	3:0	GPIO1_SEL[3:0]	0000b	
R20 (14h)	15	GPIO4_DEB_ENA	0b	See Table 64 for GPIO4 control bit description
	14	GPIO4_IRQ_ENA	0b	
	13	GPIO4_PU	0b	
	12	GPIO4_PD	1b	
	11:8	GPIO4_SEL[3:0]	0000b	
	7	GPIO3_DEB_ENA	0b	See Table 64 for GPIO3 control bit description
	6	GPIO3_IRQ_ENA	0b	
	5	GPIO3_PU	0b	
	4	GPIO3_PD	1b	
	3:0	GPIO3_SEL[3:0]	0000b	
R21 (15h)	15	GPIO6_DEB_ENA	0b	See Table 64 for GPIO6 control bit description
	14	GPIO6_IRQ_ENA	0b	
	13	GPIO6_PU	0b	
	12	GPIO6_PD	1b	
	11:8	GPIO6_SEL[3:0]	0000b	
	7	GPIO5_DEB_ENA	0b	See Table 64 for GPIO5 control bit description
	6	GPIO5_IRQ_ENA	0b	
	5	GPIO5_PU	0b	
	4	GPIO5_PD	1b	
	3:0	GPIO5_SEL[3:0]	0000b	
R22 (16h)	7	GPI8_DEB_ENA	0b	See Table 64 for GPI8 control bit description
	6	GPI8_IRQ_ENA	0b	
	4	GPI8_ENA	0b	
	3	GPI7_DEB_ENA	0b	See Table 64 for GPI7 control bit description
	2	GPI7_IRQ_ENA	0b	
	0	GPI7_ENA	0b	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h)	7:0	GPIO_POL [7:0]	00h	GPIOn Input Polarity 0 = Non-inverted 1 = Inverted GPIO_POL[7] = GPI8 polarity GPIO_POL[6] = GPI7 polarity GPIO_POL[5] = GPIO6 polarity GPIO_POL[4] = GPIO5 polarity GPIO_POL[3] = GPIO4 polarity GPIO_POL[2] = GPIO3 polarity GPIO_POL[1] = GPIO2 polarity GPIO_POL[0] = GPIO1 polarity

Table 63 GPIO Configuration and CODEC Interrupt Control

The following table describes the coding of the fields referenced in Table 63.

REGISTER ADDRESS	LABEL	DEFAULT	DESCRIPTION
Registers R19 (13h) to R22 (15h) (See Table 63)	GPIOn_DEB_ENA (n = 1 to 8)	0b	De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA = 1)
	GPIOn_IRQ_ENA (n = 1 to 8)	0b	IRQ Enable 0 = disabled 1 = enabled
	GPIOn_PU (n = 1 to 6)	0b	GPIO Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	GPIOn_PD (n = 1 to 6)	See Table 63	GPIO Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)
	GPIOn_SEL[3:0] (n = 1 to 6)	0000b	GPIOn Pin Function Select 0000 = Input pin 0001 = Clock output (SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = FLL Lock output 0101 = Temperature OK output 0110 = Reserved 0111 = CODEC IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 = MIC Detect 1011 = MIC Short Circuit Detect 1100 to 1111 = Reserved
	GPIn_ENA (n = 7 or 8)	0b	GPIn Input Pin Enable 0 = pin disabled as GPIn input 1 = pin enabled as GPIn input

Table 64 GPIO Function Control Bits

Each of the available GPIO functions is described in turn in the following sections.

ALTERNATIVE DAC INTERFACE

The WM8400 may be configured to select between two different audio interfaces, providing the capability to receive DAC input data via BCLK2, DACLRC2 and DACDAT2 instead of BCLK, DACLRC and DACDAT. This selection is made by register bit AIF_SEL, as described in Table 62.

To use the alternative DAC interface, the following register settings are required:

- AIF_TRIS = 0
- AIF_SEL = 1
- GPIO3_PU = 0, GPIO4_PU = 0, GPIO5_PU = 0
- GPIO3_PD = 0, GPIO4_PD = 0, GPIO5_PD = 0

Note that additional devices can also be connected to the main interface pins using the TDM mode. See "Digital Audio Interface" section for further details on controlling the audio interface pins.

The alternative DAC interface connection is illustrated in Figure 45.

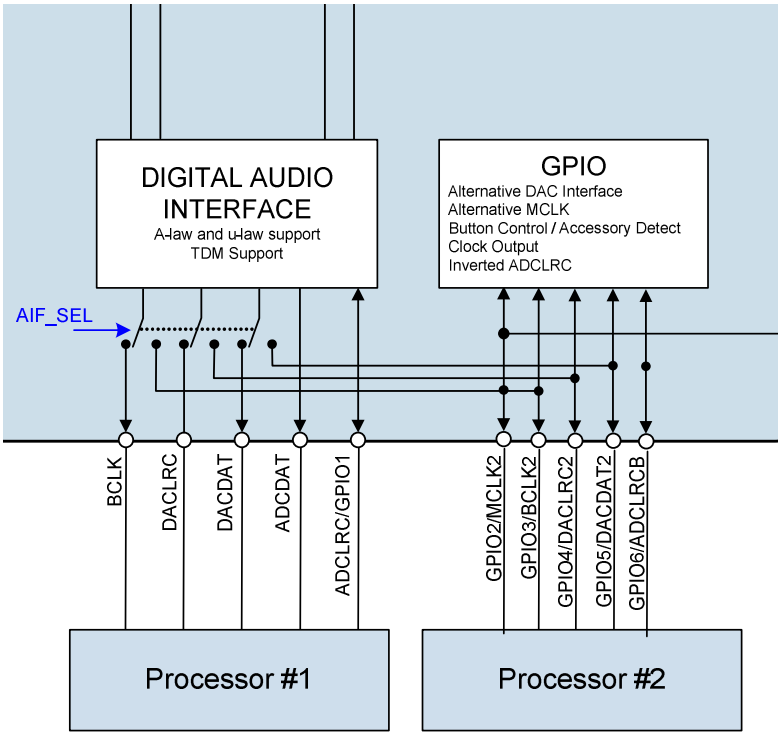


Figure 45 Alternative DAC Interface

BUTTON CONTROL

The WM8400 GPIO supports button control detection with full status readback for up to eight inputs (or seven inputs and one IRQ output). The GPIO and GPI signals are inputs to the CODEC Interrupt function, with selectable enable, de-bounce and polarity control as described in Table 63 and Table 64. The associated interrupt bits are latched once set and can be polled at any time or used as inputs to the IRQ output. See “CODEC Interrupt Event Output” for more details of the CODEC Interrupt event handling.

The interrupt bits are latched once set; they are reset by writing a logic ‘1’ to the GPIO_STATUS register bits in Register R18 (12h). De-bouncing is provided in order to avoid false event triggers. Note that TOCLK must be enabled when this input de-bouncing is required. De-bouncing may be disabled in order to allow the device to respond to wake-up events while the processor is disabled and is unable to provide a clock for de-bouncing.

To enable button control and accessory detection, the following register settings are required:

- ALRCGPIO1 = 1 (only required if using GPIO1)
- MCLK_SRC = 0 (only required if using GPIO2)
- AIF_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- ALRCGPIO6 = 0 (only required if using GPIO6)
- LMN3 = 0, LLI3LO = 0 and RLI3LO = 0 (only required if using GPI7)
- RMN3 = 0, RRI3LO = 0 and LRI3RO = 0 (only required if using GPI8)
- AIF_TRIS = 0
- GPIOn_SEL = 0000 for each required GPIO button input

Programmable pull-up and pull-down resistors are available on GPIO1 to GPIO6. These should be set according to the external circuit configuration. Note that pull-up and pull-down resistors are not available on the GPI7 and GPI8 input pins. Note that the analogue input paths to GPI7 and GPI8 must be disabled as described above when using these as digital inputs.

In this application, one or more of the GPIO pins may be configured as an Interrupt event if desired. This is controlled by the GPIOn_IRQ_ENA bits described in Table 63. The GPIO Pin status fields contained in the GPIO CTRL 1 Register (R18) may be read at any time or else in response to an Interrupt event. See Table 68 for more details of the Interrupt function.

An example configuration of the button control GPIO function is illustrated in Figure 46.

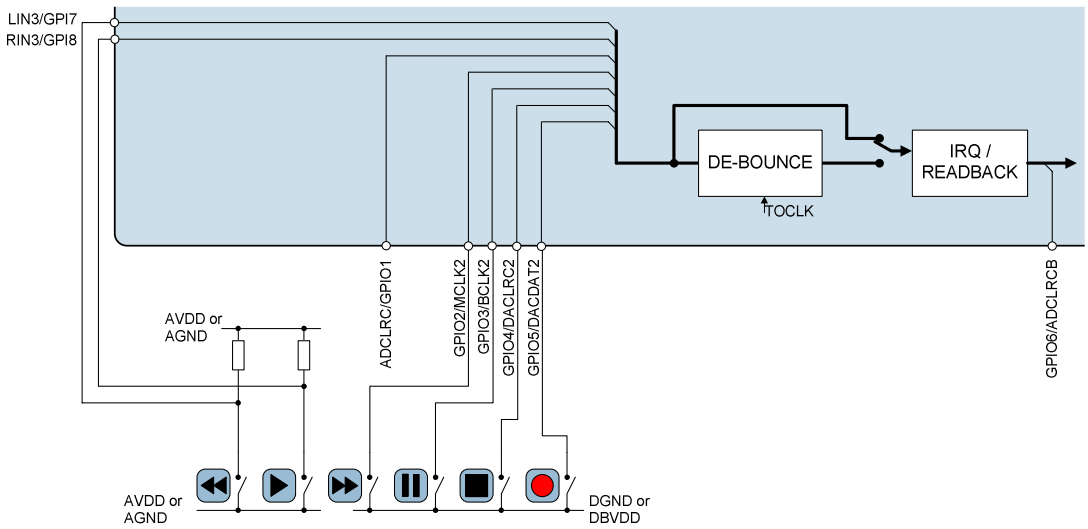


Figure 46 Example of Button Control Using GPIO Pins

Note:

- GPIO 1 is referenced to I2S1VDD
- GPIOs 2to 6 are referenced to I2S2VDD
- The GPIs 7 and 8 are referenced to AVDD

Note that the GPI7 and GPI8 input pins can also be used as inputs to the Main Interrupt circuit on the WM8400, configured in Registers R79 - R81, and signalled externally on the NIRQ pin. In this configuration, the GPI7 and GPI8 inputs represent the Jack Detect Left and Jack Detect Right inputs respectively. See “Interrupt Events” for details of this function.

MICBIAS CURRENT AND ACCESSORY DETECT

Current detection is provided on the microphone bias source MICBIAS. This can be configured to detect when an external accessory (such as a microphone) has been connected. The output voltage of the microphone bias source is selectable; two current detection threshold levels can be set.

The logic signals from the current detect circuits may be output directly on a GPIO pin, and may also be used to generate CODEC Interrupt events. Configuration of the GPIO pins for accessory detect output is described in Table 63 and Table 64 and also in the example settings below.

The accessory detection logic provides inputs to the CODEC Interrupt function, with selectable enable and polarity control. The associated interrupt bits (MIC1_SHRT and MIC1_DET) are latched once set and can be polled at any time or used as inputs to the CODEC IRQ output. The interrupt bits are reset by writing a logic ‘1’ to the MIC1_SHRT and MIC1_DET register bits. See “CODEC Interrupt Event Output” for more details of the CODEC Interrupt event handling.

If direct output of the MICBIAS current detect function is required to the external pins of the WM8400, the following register settings are required:

- ALRCGPIO1 = 1 (only required if using GPIO1)
- MCLK_SRC = 0 (only required if using GPIO2)
- AIF_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- ALRCGPIO6 = 0 (only required if using GPIO6)
- AIF_TRIS = 0
- GPIOn_SEL = 1000 for the selected GPIO MICBIAS Current Detect output pin
- GPIOn_SEL = 1001 for the selected GPIO MICBIAS Short Circuit Detect output pin
- GPIOn_PU = 0 for the selected GPIO MICBIAS output pin or pins
- GPIOn_PD = 0 for the selected GPIO MICBIAS output pin or pins

When GPIOn_SEL = 1000 or 1001, the selected accessory detection status indication is output on the GPIOn pin. A logic 1 indicates that the associated Jack Detect is asserted. Note that the polarity is not programmable for GPIO output; the GPIO_POL register bits in Table 63 affect the Interrupt behaviour only.

The register fields used to configure the MICBIAS Current Detect function are described in Table 65.

Note that the MICBIAS Current Detection function also provides input to the Main Interrupt circuit on the WM8400, configured in Registers R79 - R81, and signalled externally on the NIRQ pin. See “Interrupt Events” for details of this function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h)	10	MIC1SHRT (rr)	0b	MICBIAS Short Circuit CODEC interrupt 0 = interrupt not set 1 = interrupt is set This bit is latched once set. The MIC1SHRT_POL bit determines the polarity of the input event to set this bit. It is cleared when a '1' is written.
	9	MIC1DET (rr)	0b	MICBIAS Current Detect CODEC interrupt 0 = interrupt not set 1 = interrupt is set This bit is latched once set. The MIC1DET_POL bit determines the polarity of the input event to set this bit. It is cleared when a '1' is written.
R22 (16h)	10	MIC1SHRT_IRQ_ENA	0b	MICBIAS short circuit detect CODEC IRQ Enable 0 = disabled 1 = enabled
	9	MIC1DET_IRQ_ENA	0b	MICBIAS current detect CODEC IRQ Enable 0 = disabled 1 = enabled
R23 (17h)	10	MIC1SHRT_POL	0b	MICBIAS short circuit detect polarity 0 = Non-inverted 1 = Inverted
	9	MIC1DET_POL	0b	MICBIAS current detect polarity 0 = Non-inverted 1 = Inverted
R58 (3Ah)	7:6	MCDSCTH [1:0]	00b	MICBIAS Short Circuit Detect Threshold 00 = 450uA 01 = 850uA 10 = 1250uA 11 = 1650uA These values are for AVDD=3.0V
	5:3	MCDTHR [2:0]	000b	MICBIAS Current Detect Threshold 000 = 220uA 001 = 330uA 010 = 440uA 011 = 550uA 100 = 660uA 101 = 770uA 110 = 880uA 111 = 990uA These values are for AVDD=3.0V
	2	MCD	0b	MICBIAS Current and Short Circuit Detect Enable 0 = disabled 1 = enabled

Table 65 MICBIAS Current Detect Control

ALTERNATIVE MCLK INPUT

An alternative MCLK source can be input via the MCLK2/GPIO2 pin. This provides additional flexibility for systems where the CODEC is required to interface with more than one processor. See "Clocking and Sample Rates" for more information on selecting MCLK source.

To enable the alternative MCLK input on GPIO2, the following register settings are required:

- MCLK_SRC = 1
- AIF_TRIS = 0
- GPIO2_PU = 0
- GPIO2_PD = 0
- GPIO2_SEL = 0000

The above register fields are described in Table 62 and Table 63.

CLOCK OUTPUT

A clock output (OPCLK) derived from SYSCLK may be output via GPIO1 to GPIO6. SYSCLK is derived from MCLK (either directly, or in conjunction with the FLL), and is used to provide all internal clocking for the WM8400 (see "Clocking and Sample Rates" section for more information).

A programmable clock divider OPCLKDIV controls the frequency of the OPCLK output. This clock is enabled by register bit OPCLK_ENA. See “Clocking and Sample Rates” for a definition of this register field.

To enable clock output via one or more GPIO pins, the following register settings are required:

- ALRCGPIO1 = 1 (only required if using GPIO1)
- MCLK_SRC = 0 (only required if using GPIO2)
- AIF_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- ALRCGPIO6 = 0 (only required if using GPIO6)
- AIF_TRIS = 0
- GPIOn_SEL = 0001 for the selected GPIO clock output pin
- GPIOn_PU = 0 for the selected GPIO clock output pin
- GPIOn_PD = 0 for the selected GPIO clock output pin

INVERTED ADCLRC OUTPUT

An inverted ADCLRC signal can be output via the GPIO6/ADCLRCB pin.

To enable the Inverted ADCLRC output, the following register settings are required:

- ALRCGPIO6 = 1
- AIF_TRIS = 0
- GPIO6_PU = 0
- GPIO6_PD = 0

TEMPERATURE SENSOR OUTPUT

The WM8400 incorporates a temperature sensor which detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition. The temperature status may be output directly on a GPIO pin, and may also be used to generate CODEC Interrupt events. Configuration of the GPIO pins for Temperature Sensor output is described in Table 63 and Table 64 and also in the example settings below.

The temperature sensor signal is an input to the CODEC Interrupt function, with selectable enable and polarity control. The associated interrupt bit (TEMPOK) is latched once set and can be polled at any time or used to trigger the CODEC IRQ output. The interrupt bit is reset by writing a logic '1' to the TEMPOK register bit. See "CODEC Interrupt Event Output" for more details of the CODEC Interrupt event handling.

Note that the temperature sensor can be configured to automatically disable the audio outputs of the WM8400 (see "Thermal Shutdown"). In some applications, it may be preferable to manage the temperature sensor event through GPIO or Interrupt functions, allowing a host processor to implement a controlled system response to an over-temperature condition.

The temperature sensor must be enabled by setting the TSHUT_ENA register bit. When the TSHUT_OPDIS is also set, then a device over-temperature condition will cause the audio outputs of the WM8400 to be disabled.

The Temperature Sensor output is asserted when the device is within normal operating limits. When configured to generate an interrupt event, the default polarity (TEMPOK_POL = 1) will cause an interrupt event when an overtemperature condition has been reached.

If direct output of the Temperature status bit is required to the external pins of the WM8400, the following register settings are required:

- ALRCGPIO1 = 1 (only required if using GPIO1)
- MCLK_SRC = 0 (only required if using GPIO2)
- AIF_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- ALRCGPIO6 = 0 (only required if using GPIO6)
- AIF_TRIS = 0
- GPIOn_SEL = 0101 for the selected GPIO Temperature status output pin
- GPIOn_PU = 0 for the selected GPIO Temperature status output pin
- GPIOn_PD = 0 for the selected GPIO Temperature status output pin

When GPIOn_SEL = 0101, the Temperature Sensor status is output on the GPIOn pin. A logic 0 indicates that an overtemperature condition has been reached. Note that the polarity is not programmable for GPIO output; the GPIO_POL and TEMPOK_POL fields affect the Interrupt behaviour only.

The register fields used to configure the Temperature Sensor GPIO function are described in Table 66.

Note that the Temperature Sensor also provides input to the Main Interrupt circuit on the WM8400, configured in Registers R79 - R81, and signalled externally on the NIRQ pin. Two different temperature thresholds can be monitored in this way. See "Interrupt Events" for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18	11	TEMPOK (rr)	0b	Temperature OK CODEC interrupt 0 = interrupt not set 1 = interrupt is set This bit is latched once set. The TEMPOK_POL bit determines the polarity of the input event to set this bit. It is cleared when a '1' is written.
R22 (16h)	11	TEMPOK_IRQ_ ENA	0b	Temperature Sensor CODEC IRQ Enable 0 = disabled 1 = enabled
R23 (17h)	11	TEMPOK_POL	1b	Temperature Sensor polarity 0 = Non-inverted 1 = Inverted

Table 66 Temperature Sensor GPIO Control

FLL LOCK OUTPUT

The WM8400 maintains a flag indicating the lock status of the FLL, which may be used to control other events if required. The FLL Lock status may be output directly on a GPIO pin, and may also be used to generate CODEC Interrupt events. Configuration of the GPIO pins for output of the FLL Lock flag is described in Table 63 and Table 64 and also in the example settings below.

The FLL Lock signal is an input to the CODEC Interrupt function, with selectable enable and polarity control. The associated interrupt bit (FLL_LCK) is latched once set and can be polled at any time or used to trigger the CODEC IRQ output. The interrupt bit is reset by writing a logic '1' to the FLL_LCK register bit. See "CODEC Interrupt Event Output" for more details of the CODEC Interrupt event handling.

The FLL Lock signal is asserted when FLL Lock has been reached. When configured to generate an interrupt event, the default polarity (FLL_LCK_POL = 0) will cause an interrupt event when FLL Lock has been reached.

If direct output of the FLL Lock status bit is required to the external pins of the WM8400, the following register settings are required:

- ALRCGPIO1 = 1 (only required if using GPIO1)
- MCLK_SRC = 0 (only required if using GPIO2)
- AIF_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- ALRCGPIO6 = 0 (only required if using GPIO6)
- AIF_TRIS = 0
- GPIOn_SEL = 0100 for the selected FLL Lock status output pin
- GPIOn_PU = 0 for the selected FLL Lock status output pin
- GPIOn_PD = 0 for the selected FLL Lock status output pin

When GPIOn_SEL = 0100, the FLL Lock signal is output on the GPIOn pin. A logic 1 indicates that FLL Lock has been reached. Note that the polarity is not programmable for GPIO output; the GPIO_POL and FLL_LCK_POL fields affect the Interrupt behaviour only.

The register fields used to configure the FLL Lock GPIO function are described in Table 67.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h)	8	FLL_LCK (rr)	0b	FLL Lock CODEC interrupt 0 = interrupt not set 1 = interrupt is set This bit is latched once set. The FLL_LCK_POL bit determines the polarity of the input event to set this bit. It is cleared when a '1' is written.
R22 (16h)	8	FLL_LCK_IRQ_ ENA	0b	FLL Lock CODEC IRQ Enable 0 = disabled 1 = enabled
R23 (17h)	8	FLL_LCK_POL	0b	FLL Lock polarity 0 = Non-inverted 1 = Inverted

Table 67 FLL Lock GPIO Control

LOGIC '1' AND LOGIC '0' OUTPUT

The GPIO pins can be programmed to drive a logic high or logic low signal. The following register settings are required:

- ALRCGPIO1 = 1 (only required if using GPIO1)
- MCLK_SRC = 0 (only required if using GPIO2)
- AIF_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- ALRCGPIO6 = 0 (only required if using GPIO6)
- AIF_TRIS = 0
- GPIOn_SEL = 0010 for each Logic '0' output pin
- GPIOn_SEL = 0011 for each Logic '1' output pin
- GPIOn_PU = 0 for each Logic '0' or Logic '1' GPIO pin
- GPIOn_PD = 0 for each Logic '0' or Logic '1' GPIO pin

CODEC INTERRUPT EVENT OUTPUT

The CODEC interrupt status flag IRQ is asserted when any enabled CODEC interrupt event is asserted. It represents the OR'd combination of all the enabled CODEC interrupt status bits. If required, this flag may be inverted using the IRQ_INV register bit. The IRQ flag can be polled at any time, or may be output directly on a GPIO pin. Configuration of the GPIO pins for output of the IRQ flag is described in Table 63 and Table 64 and also in the example settings below.

An interrupt can be generated by any of the following events described earlier:

- Button Control input (on GPIO1 to GPIO6, GPI7 and GPI8)
- MICBIAS current / short circuit / accessory detect
- FLL Lock
- Temperature Sensor

The CODEC interrupt events are indicated by the interrupt register fields described earlier. The interrupt bits are latched once set; they are reset by writing a logic '1' to the respective bit. Each of these can be enabled as an input to the IRQ function by setting the associated _IRQ_ENA register field. Note that the interrupt bits are always valid, regardless of the setting of the associated _IRQ_ENA register fields.

The IRQ bit cannot be reset directly. This read-only bit is reset whenever none of the enabled interrupts is set.

The interrupt behaviour is driven by level detection (not edge detection) of the enabled inputs. Therefore, if an input remains asserted after the interrupt register has been reset, then the interrupt status flag IRQ will be triggered again even though no transition has occurred. If edge detection is required (eg. confirming that the input has been de-asserted), then the polarity inversion may be used after each event in order to detect each rising and falling edge separately. This is described further in the following "GPIO summary" section.

If direct output of the Interrupt signal is required to external pins of the WM8400, the following register settings are required:

- ALRCGPIO1 = 1 (only required if using GPIO1)
- MCLK_SRC = 0 (only required if using GPIO2)
- AIF_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- ALRCGPIO6 = 0 (only required if using GPIO6)
- AIF_TRIS = 0
- GPIOn_SEL = 0111 for the selected Interrupt (IRQ) output pin
- GPIOn_PU = 0 for the selected Interrupt (IRQ) output pin
- GPIOn_PD = 0 for the selected Interrupt (IRQ) output pin

The IRQ Control fields are described in Table 68.

Note that the CODEC Interrupt relates only to the functions described in this section. The Power Management Interrupt, and the dedicated NIRQ pin, are described separately in the "Interrupt Events" section. The Jack Detect (GPI7 and GPI8), MICBIAS and Temperature sensor functions are effective in both the CODEC Interrupt and Power Management Interrupt circuits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h)	12	IRQ (ro)	Read Only	IRQ Readback (Allows polling of IRQ status)
R23 (17h)	12	IRQ_INV	0b	IRQ Invert 0 = IRQ output active high 1 = IRQ output active low

Table 68 CODEC Interrupt (IRQ) Control

GPIO SUMMARY

The GPIO functions are summarised in Figure 47.

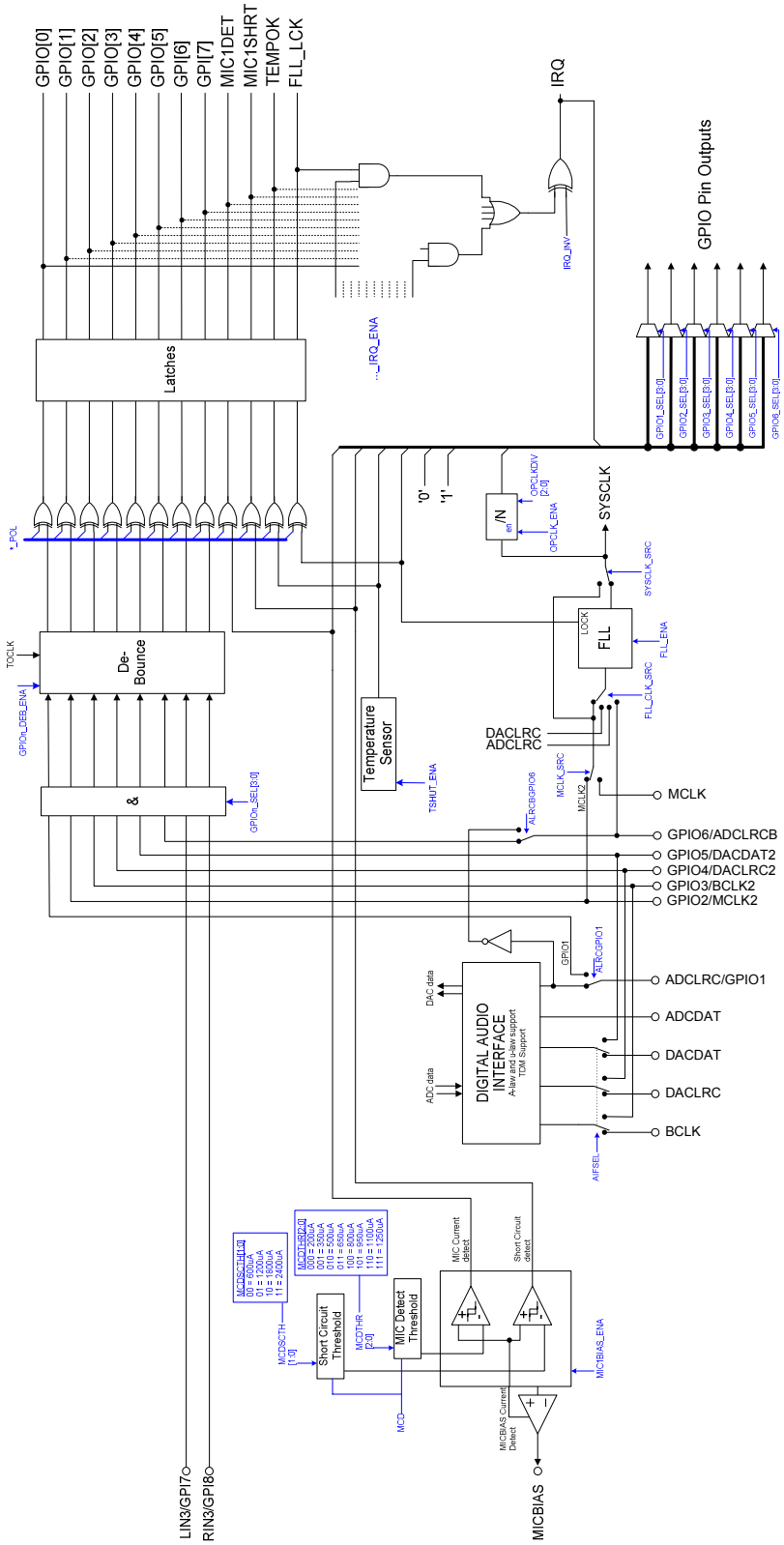


Figure 47 GPIO Control Diagram

Details of the GPIO implementation are shown below. In order to avoid GPIO loops if a GPIO is configured as an output the corresponding input is disabled, as shown in Figure 48 below.

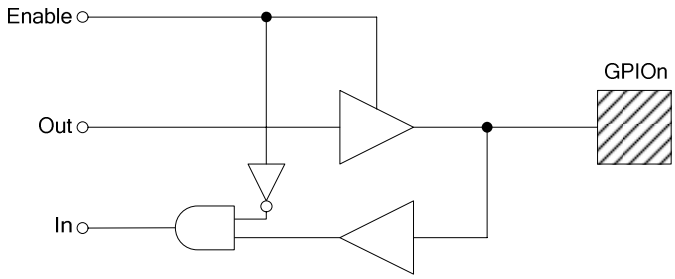


Figure 48 GPIO Pad

The GPIO register, i.e. latch structure, is shown in Figure 49 below. The de-bounce Control fields GPIOn_DEB_ENA determine whether the signal is de-bounced or not. (Note that TOCLK (via SYSCLK) needs to be present in order for the debounce circuit to work.) The polarity bits GPIO_POL[7:0] control whether an interrupt is triggered by a logic 1 level (for GPIO_POL[n] = 0) or a logic 0 level (for GPIO_POL[n] = 1). The latch will cause the interrupt to be stored until it is reset by writing to the Interrupt Register. The latched signal is processed by the IRQ circuit, shown in Figure 47 above. The interrupt status bits can be read at any time from Register R18 (see Table 68) and are reset by writing a "1" to the applicable bit in Register R18.

Note that the interrupt behaviour is driven by level detection (not edge detection). Therefore, if an input remains asserted after the interrupt register has been reset, then the interrupt event will be triggered again even though no transition has occurred. If edge detection is required, this may be implemented as described in the following paragraphs.

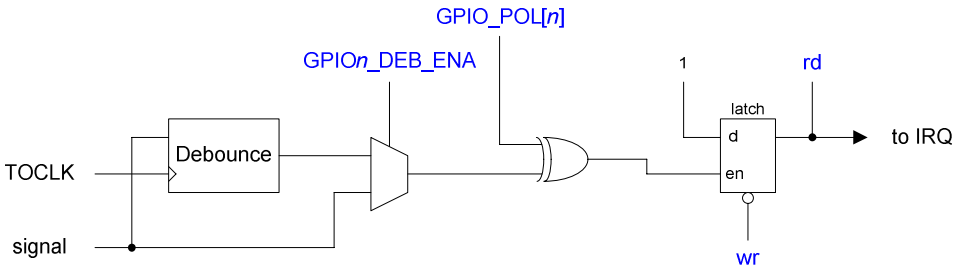


Figure 49 GPIO Function

Three typical scenarios are presented in the following Figure 50, Figure 51 and Figure 52. The examples are:

- Latch a GPIO input (Figure 50)
- Debounce and latch a GPIO input (Figure 51)
- Use the GPIOn_POL bit to implement an IRQ edge detect function (Figure 52)

The GPIO input or internal Interrupt event (eg. MICBIAS current detect) is latched as illustrated below:

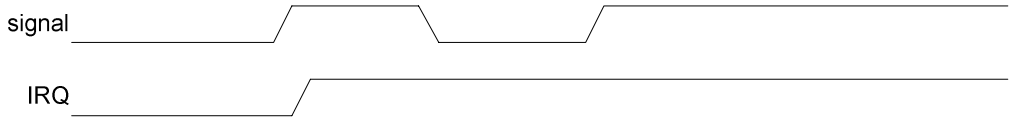


Figure 50 GPIO Latch

The de-bounce function on the GPIO input pins enables transient behaviour to be filtered as illustrated below:

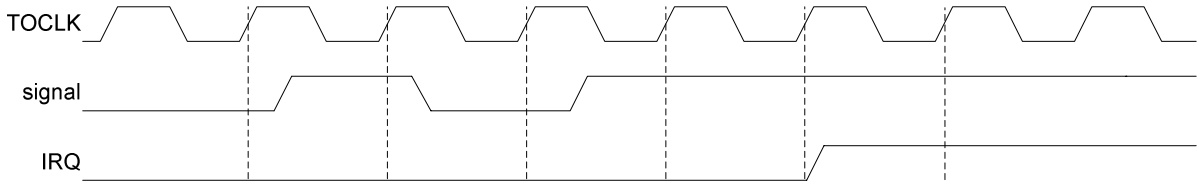


Figure 51 GPIO De-bounce

To implement an edge detect function on a GPIO input, the GPIOn_POL bits may be used to alternate the GPIO polarity after each edge transition. For example, after a logic 1 has caused an Interrupt event, the polarity may be inverted prior to resetting the Interrupt register bit. In this way, the next interrupt event generated by this GPIO will occur when it returns to the logic 0 state. The GPIOn_POL bit must be reversed after every GPIO edge transition, as illustrated below:

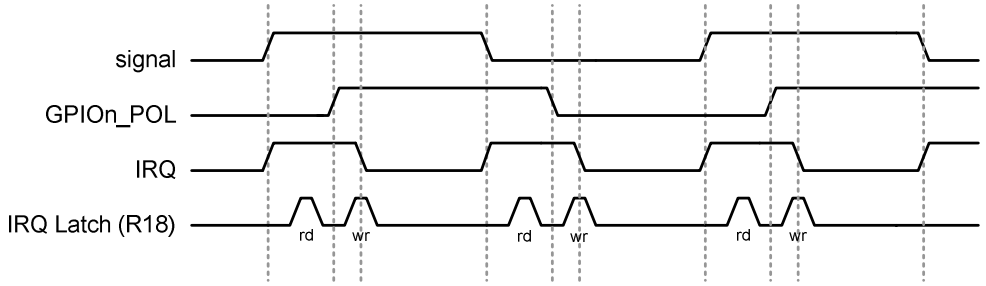


Figure 52 GPIO Edge Detect

GPIO IRQ HANDLING

In the following diagram Figure 53 a typical IRQ scenario is illustrated.

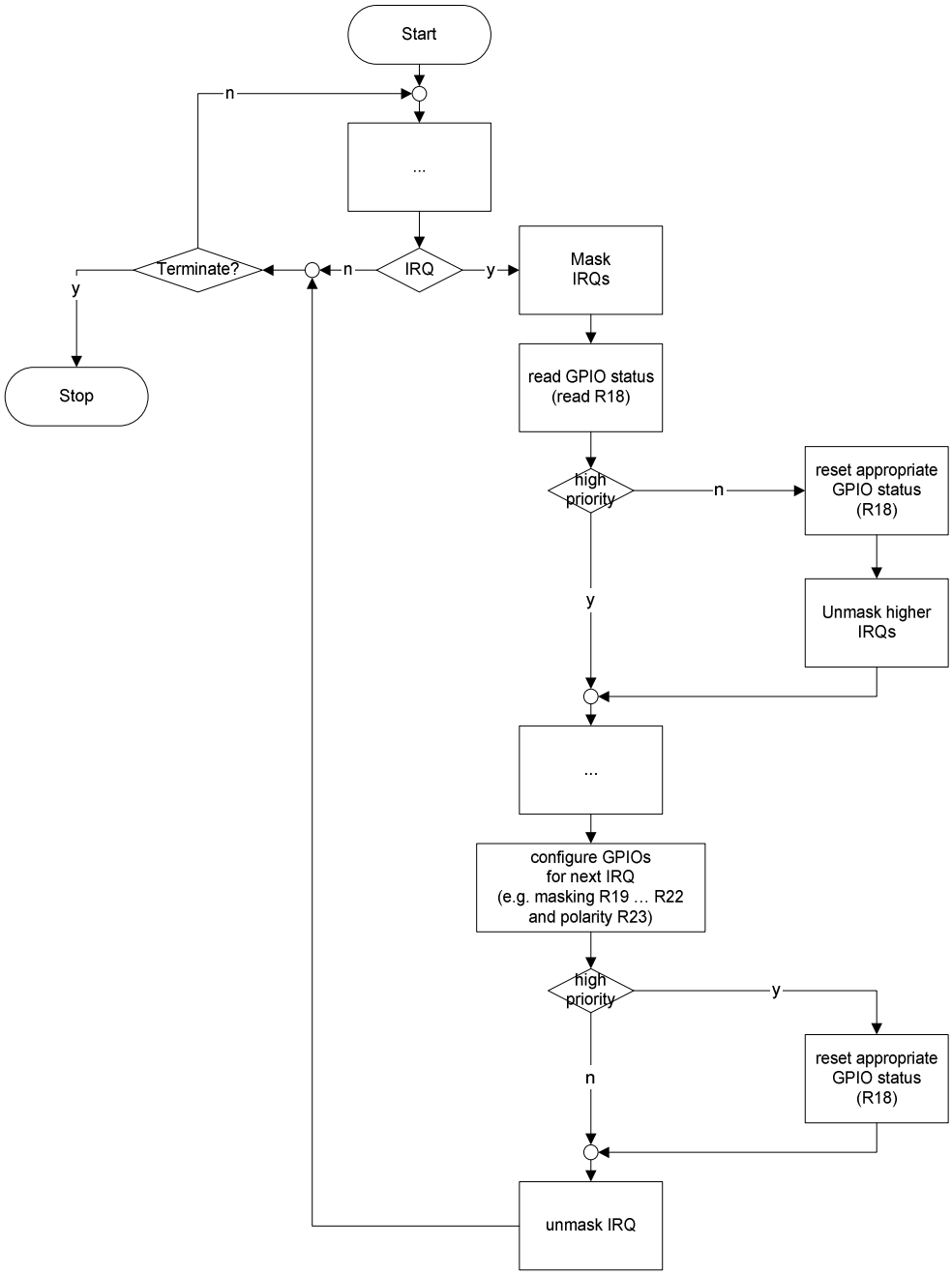


Figure 53 GPIO IRQ Handling

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data to the WM8400 and outputting ADC data from it. The interface uses five pins:

- ADCDAT: ADC data output
- ADCLRC: ADC data alignment clock (An inverted ADCLRC is also available via GPIO)
- DACDAT: DAC data input (An alternative DACDAT is also available via GPIO)
- DACLRC: DAC data alignment clock (An alternative DACLRC is also available via GPIO)
- BCLK: Bit clock, for synchronisation (An alternative BCLK is also available via GPIO)

The clock signals BCLK, ADCLRC and DACLRC can be outputs when the WM8400 operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

ADCLRC can also be configured as a GPIO pin. In this case, the ADC will use DACLRC as a frame clock. The ADCLRC/GPIO1 pin function should not be modified while the ADC is enabled.

DACDAT, DACLRC and BCLK functions can also be supported using GPIO pins. An inverted ADCLRC can also be output via GPIO pins.

Four different audio data formats are supported:

- Left justified
- Right justified
- I^2S
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the "Electrical Characteristics" section for timing information.

Time Division Multiplexing (TDM) is available in all four data format modes. The WM8400 can be programmed to send and receive data in one of two time slots.

PCM operation is supported using the DSP mode.

DIGITAL AUDIO INTERFACE POWER DOMAINS

Operation of the Digital Audio Interface requires an appropriate power supply to be connected to the I2S1VDD power domain. Operation of the secondary DAC interface (via GPIO pins) requires an appropriate power supply to be connected to the I2S2VDD power domain. These supplies are referenced to GND.

The operating ranges for these supplies are detailed in the "Recommended Operating Conditions" section.

MASTER AND SLAVE MODE OPERATION

The WM8400 digital audio interface can operate as a master or slave as shown in Figure 54 and Figure 55.

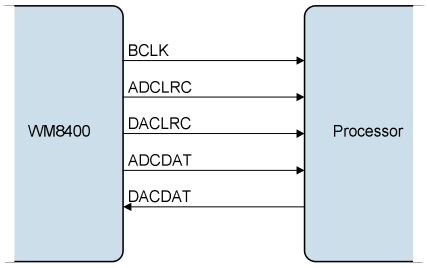


Figure 54 Master Mode

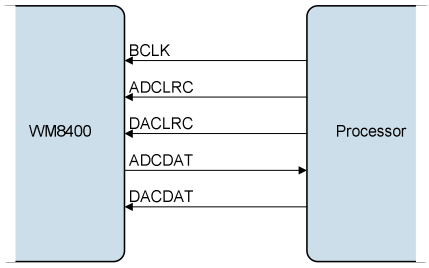


Figure 55 Slave Mode

OPERATION WITH ADCLRC AS GPIO

When the ADCLRC/GPIO1 pin is configured as a GPIO pin (ALRCGPIO=1), the DACLRC pin is used as a frame clock for ADCs and DACs as shown in Figure 56 and Figure 57. The ADCs and DACs must operate at the same sample rate in this configuration.

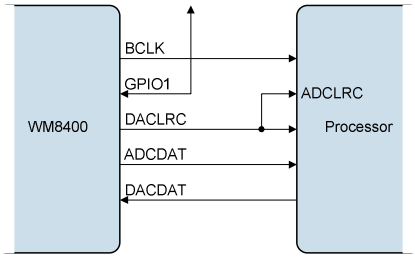


Figure 56 Master Mode with ADCLRC as GPIO

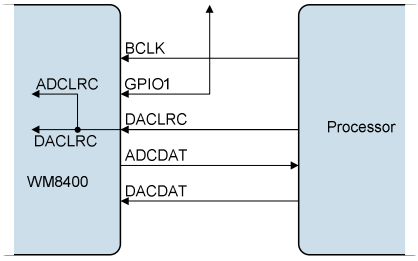


Figure 57 Slave Mode with ADCLRC as GPIO

OPERATION WITH ALTERNATIVE DAC INTERFACE

To allow data to be input to the WM8400 DACs from two separate sources, the GPIO[5:3] pins can be configured as an alternative DAC interface (BCLK2, DACLRC2, DACDAT2) as shown in Figure 60 to Figure 63.

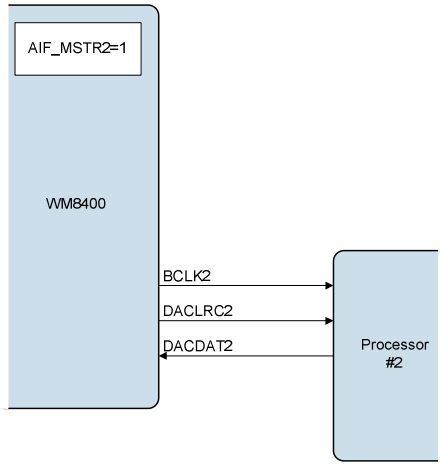


Figure 58 Interface 2 = Master

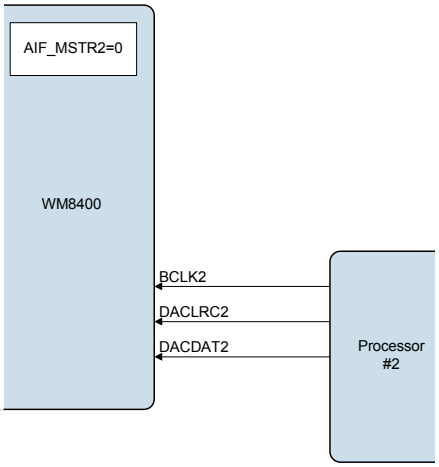


Figure 59 Interface 2 = Slave

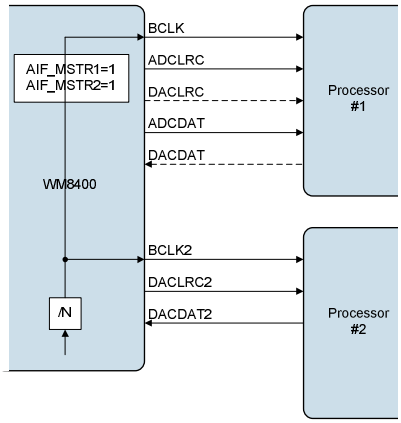


Figure 60 Interface 1 = Master, Interface 2 = Master

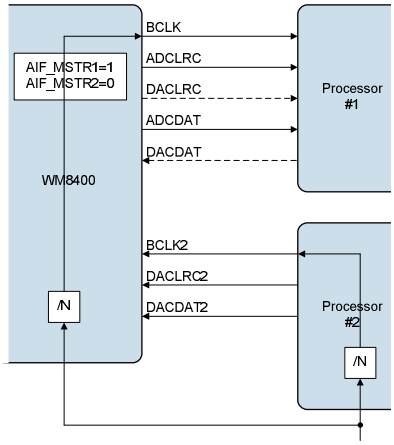


Figure 61 Interface 1 = Master, Interface 2 = Slave

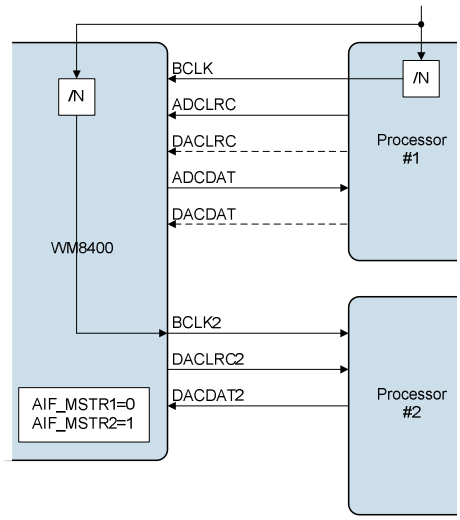


Figure 62 Interface 1 = Slave, Interface 2 = Master

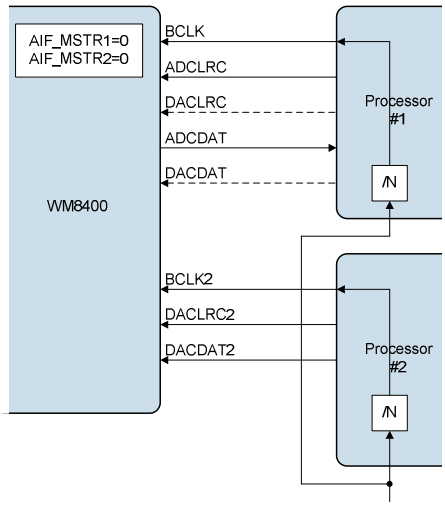


Figure 63 Interface 1 = Slave, Interface 2 = Slave

The dual Audio Interface approach of the WM8400 has been implemented in such a way that it gives the user and application as much flexibility as possible, without any restrictions built into the WM8400.

This means that the application has to be carefully analysed and the WM8400 configured accordingly. In the following Figure 64 and Figure 65 the Audio Interface input flow and the output controlling are illustrated.

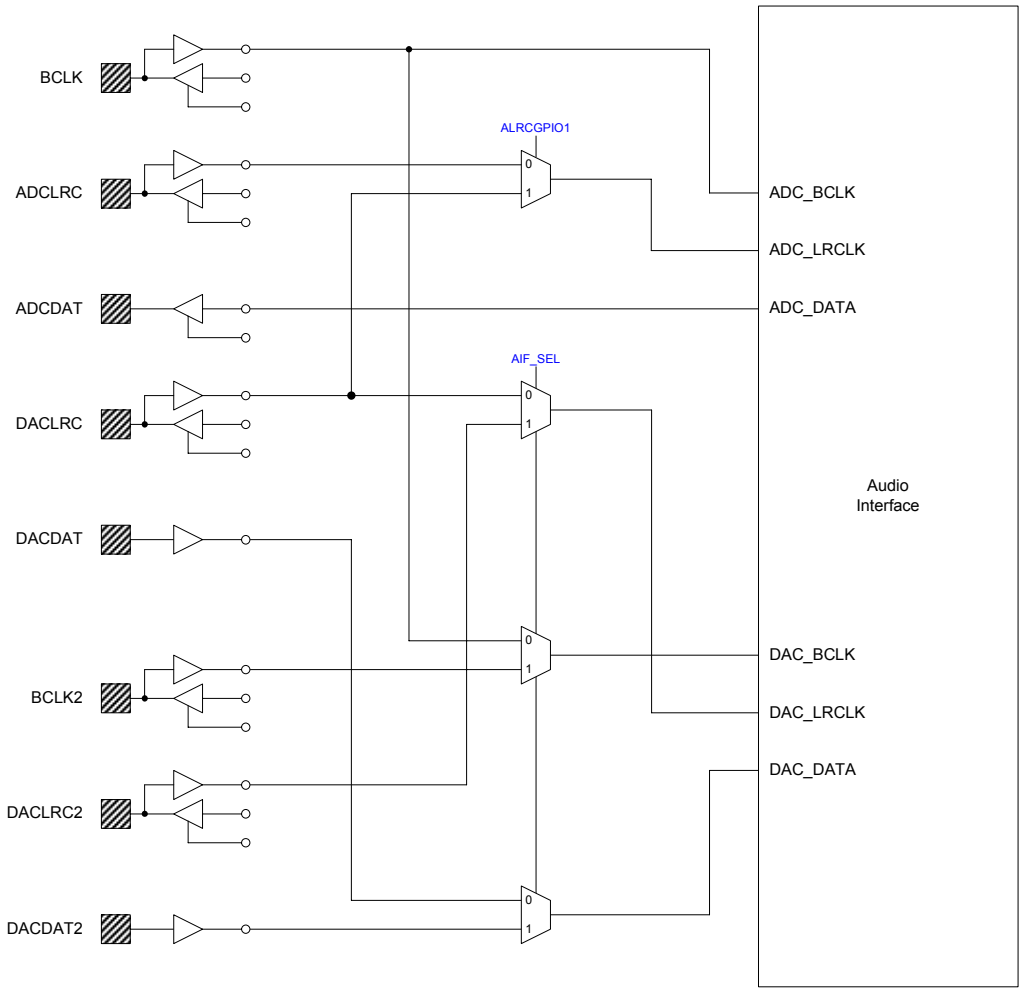


Figure 64 Audio Interface Input Flow

The Audio Interface input flow illustrated above is controlled by only two signals. These are ALRCGPIO1 and AIF_SEL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h)	13	AIF_SEL	0b	Audio Interface Select 0 = Audio interface 1 1 = Audio interface 2 (GPIO3/BCLK2, GPIO4/DACLRC2, GPIO5/DACDAT2)
R10 (0Ah)	15	ALRCGPIO1	0b	ADCLRC/GPIO1 Pin Function Select 0 = ADCLRC pin 1 = GPIO1 pin (ADCLRC connected to DACLRC internally)

Table 69 Audio Interface Pin Function Select

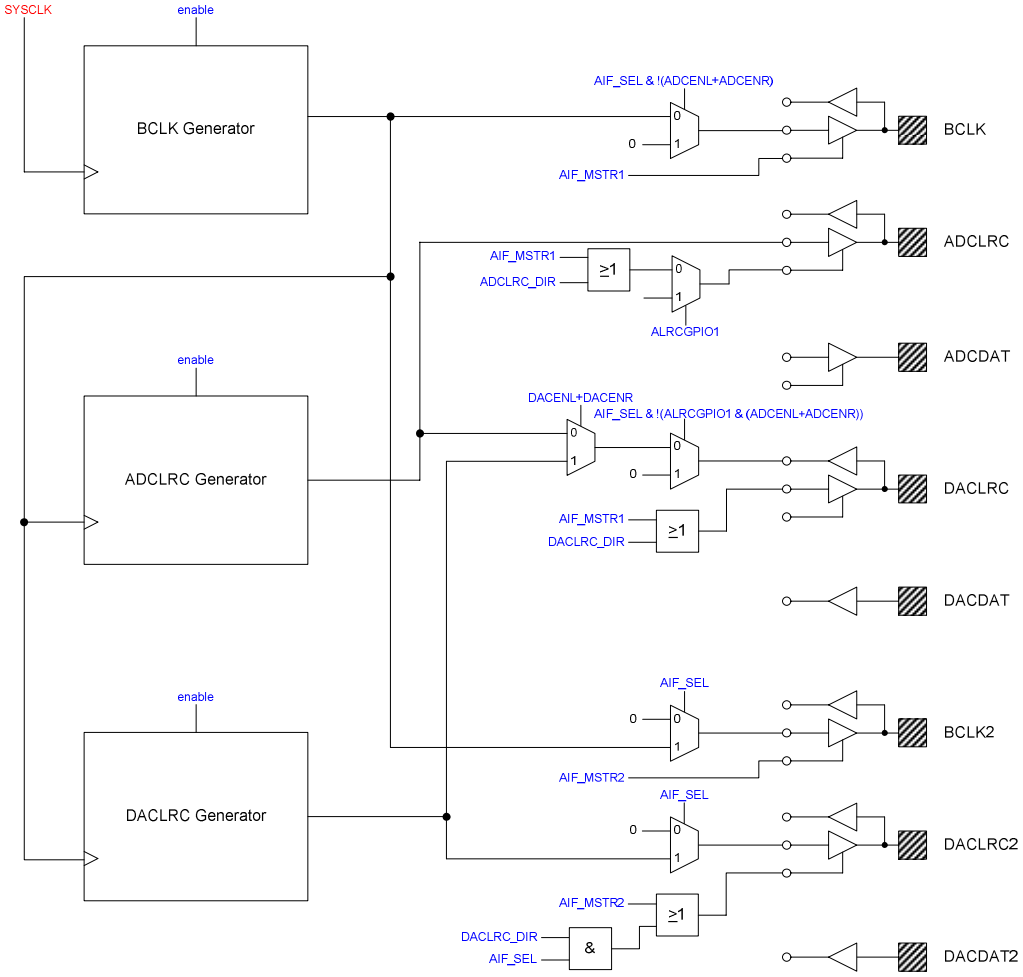


Figure 65 Audio Interface Output Control

The Audio Interface output control is illustrated above. The master mode control registers AIF_MSTR1 and AIF_MSTR2 as well as the left-right clock control registers ADCLRC_DIR and DACLRC_DIR determine whether the WM8400 generates the according clocks and AIF_SEL and ALRCGPIO1 control registers define the pins these clocks are provided from.

These registers are described in Table 70 below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h)	15	AIF_MSTR1	0b	Audio Interface 1 Master Mode Select 0 = Slave mode 1 = Master mode
	14	AIF_MSTR2	0b	Audio Interface 2 Master Mode Select 0 = Slave mode 1 = Master mode
	13	AIF_SEL	0b	Audio Interface Select 0 = Audio interface 1 1 = Audio interface 2 (GPIO3/BCLK2, GPIO4/DACLRC2, GPIO5/DACDAT2)
	11	ADCLRC_DIR	0b	ADCLRC Direction (Forces ADCLRC clock to be output in slave mode) 0 = ADCLRC normal operation 1 = ADCLRC clock output enabled
R10 (0Ah)	15	ALRCGPIO1	0b	ADCLRC/GPIO1 Pin Function Select 0 = ADCLRC pin 1 = GPIO1 pin (ADCLRC connected to DACLRC internally)
	14	ALRCBGPIO6	0b	GPIO6/ADCLRCB Pin Function Select 0 = GPIO6 pin 1 = Inverted ADCLRC clock output
	11	DACLRC_DIR	0b	DACLRC Direction (Forces DACLRC clock to be output in slave mode) 0 = DACLRC normal operation 1 = DACLRC clock output enabled

Table 70 Audio Interface Output Function Control

OPERATION WITH TDM

Time division multiplexing (TDM) allows multiple devices to transfer data simultaneously on the same bus. The WM8400 ADCs and DACs support TDM in master and slave modes, on both interfaces, and for all data formats and word lengths. TDM is enabled using register bits AIFADC_TDM and AIFDAC_TDM. The TDM data slot is programmed using register bits AIFADC_TDM_CHAN and AIFDAC_TDM_CHAN.

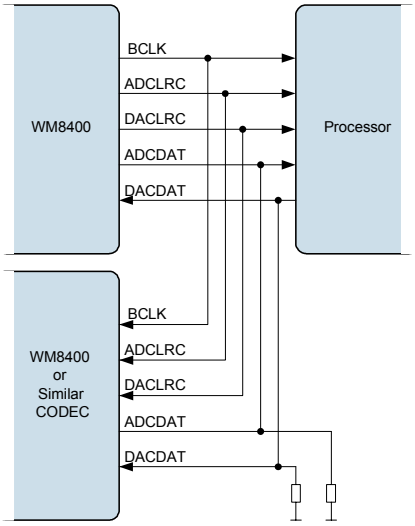


Figure 66 TDM with WM8400 as Master

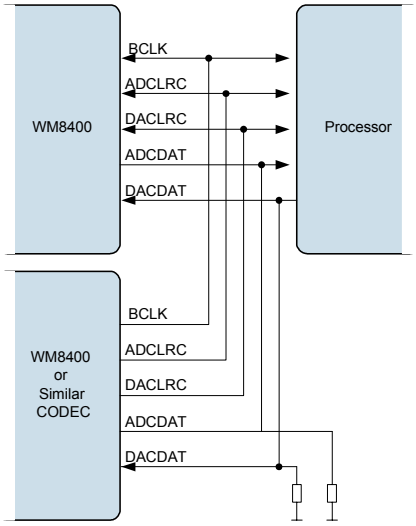


Figure 67 TDM with Other CODEC as Master

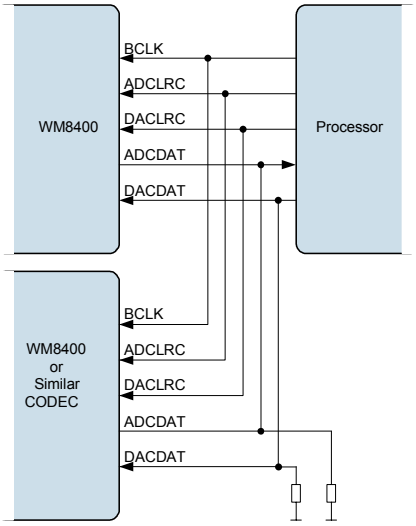


Figure 68 TDM with Processor as Master

Note: The WM8400 is a 24-bit device. If the user operates the WM8400 in 32-bit mode then the 8 LSBs will be ignored on the receiving side and not driven on the transmitting side. It is therefore recommended to add a pull-down resistor if necessary to the DACDAT line and the ADCDAT line in TDM mode.

BCLK DIVIDE

The BCLK frequency is controlled by BCLK_DIV. When the ADCs and DACs are operating at different sample rates, BCLK_DIV must be set appropriately to support the data rate of whichever is the faster.

Internal clock divide and phase control mechanisms ensure that the BCLK, ADCLRC and DACLRC edges will occur in a predictable and repeatable position relative to each other and to the data for a given combination of DAC sample rate, ADC sample rate and BCLK_DIV settings.

See “Clocking and Sample Rates” section for more information.

AUDIO DATA FORMATS (NORMAL MODE)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRC transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRC transition.

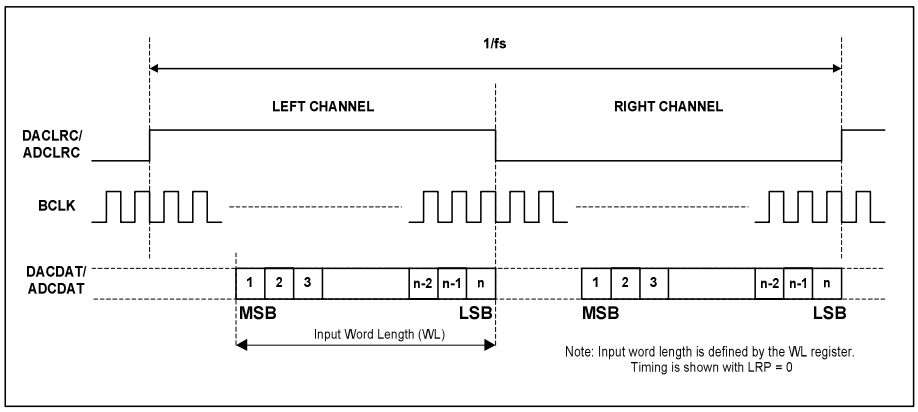


Figure 69 Right Justified Audio Interface (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRC transition.

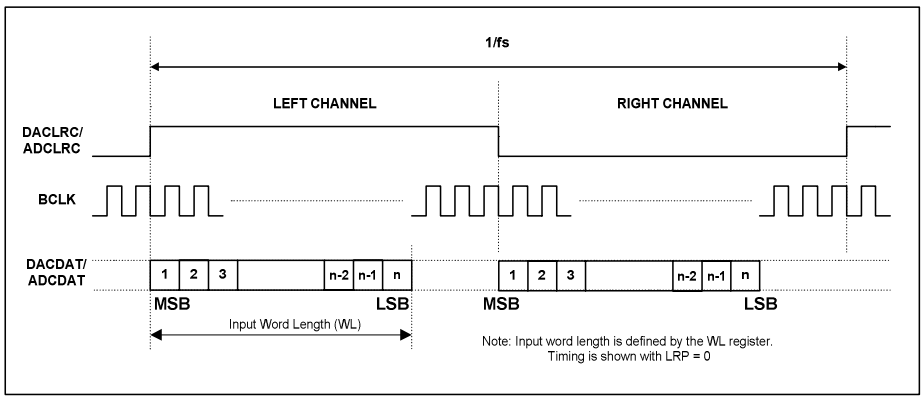


Figure 70 Left Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

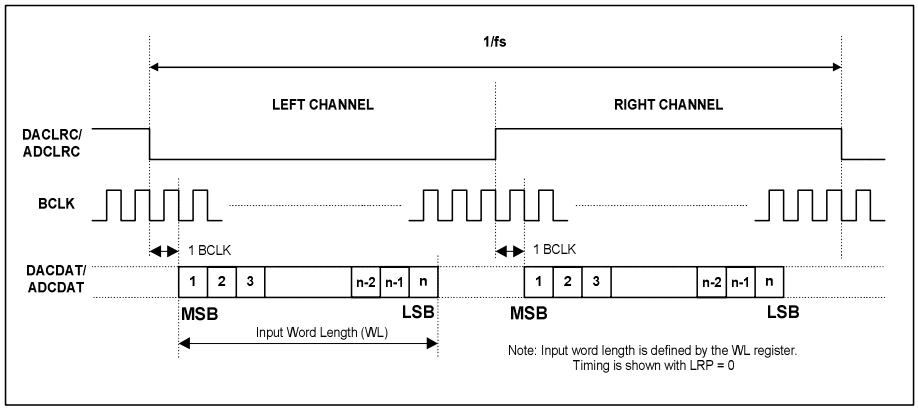


Figure 71 I2S Justified Audio Interface (assuming n-bit word length)

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by AIF_LRCLK_INV) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 72 and Figure 73. In device slave mode, Figure 74 and Figure 75, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

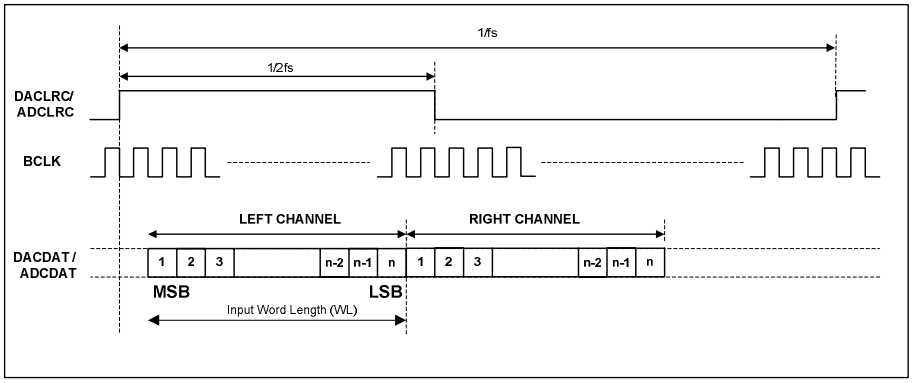


Figure 72 DSP Mode Audio Interface (mode A, AIF_LRCLK_INV=0, Master)

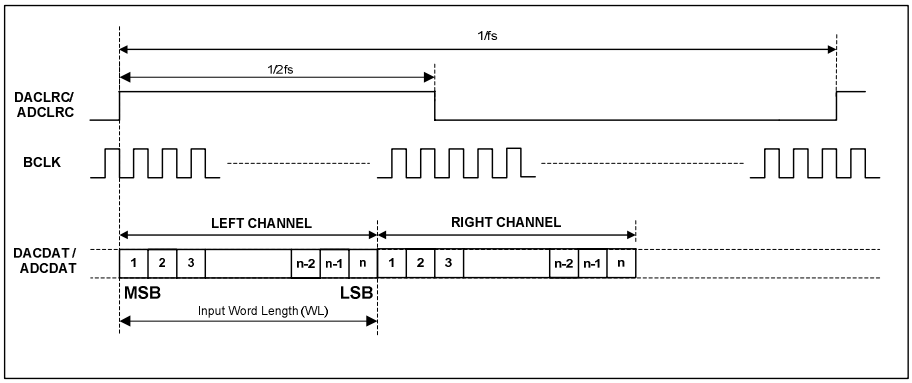


Figure 73 DSP Mode Audio Interface (mode B, AIF_LRCLK_INV=1, Master)

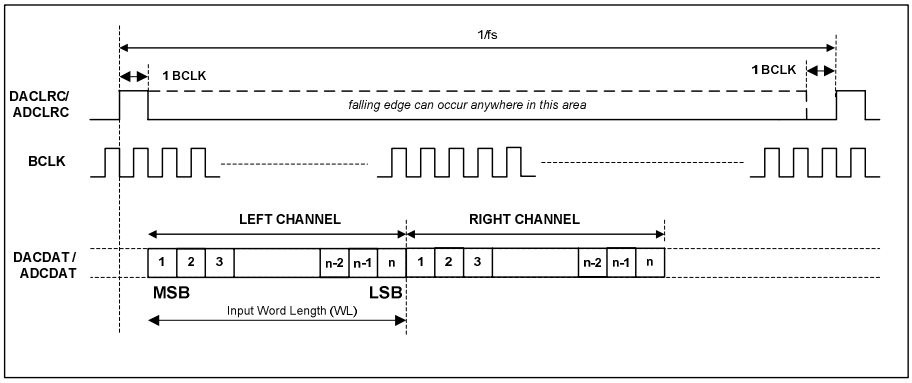


Figure 74 DSP Mode Audio Interface (mode A, AIF_LRCLK_INV=0, Slave)

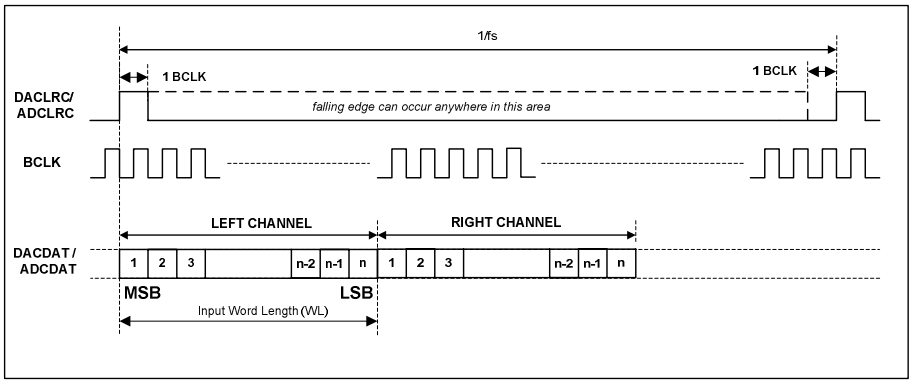


Figure 75 DSP Mode Audio Interface (mode B, AIF_LRCLK_INV=1, Slave)

PCM operation is supported in DSP interface mode. WM8400 ADC data that is output on the Left Channel will be read as mono PCM data by the receiving equipment. Mono PCM data received by the WM8400 will be treated as Left Channel data. This data may be routed to the Left/Right DACs as described in the “Digital Input Path” section.

AUDIO DATA FORMATS (TDM MODE)

TDM is supported in master and slave mode and is enabled by register bits AIF_ADC_TDM and AIF_DAC_TDM. All audio interface data formats support time division multiplexing (TDM) for ADC and DAC data.

Two time slots are available (Slot 0 and Slot 1), selected by register bits AIFADC_TDM_CHAN and AIFDAC_TDM_CHAN which control time slots for the ADC data and the DAC data.

When TDM is enabled, the ADCDAT pin will be tri-stated immediately before and immediately after data transmission, to allow another ADC device to drive this signal line for the remainder of the sample period. Note that it is important that two ADC devices do not attempt to drive the data pin simultaneously. A short circuit may occur if the transmission time of the two ADC devices overlap with each other. See “Audio Interface Timing - TDM Mode” for details of the ADCDAT output relative to BCLK signal. Note that it is possible to ensure a gap exists between transmissions by setting the transmitted word length to a value higher than the actual length of the data. For example, if 32-bit word length is selected where only 24-bit data is available, then the WM8400 interface will tri-state after transmission of the 24-bit data, ensuring a gap after the WM8400’s TDM slot.

When TDM is enabled, BCLK frequency must be high enough to allow data from both time slots to be transferred. The relative timing of Slot 0 and Slot 1 depends upon the selected data format as shown in Figure 76 to Figure 80.

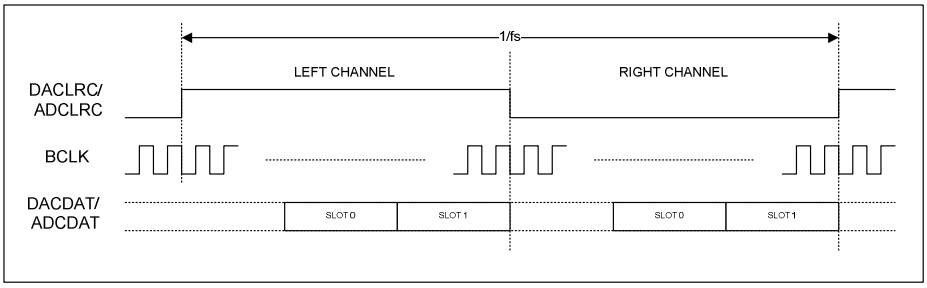


Figure 76 TDM in Right-Justified Mode

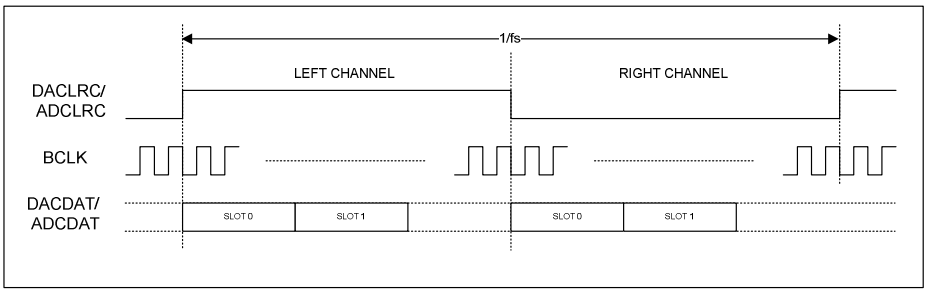


Figure 77 TDM in Left-Justified Mode

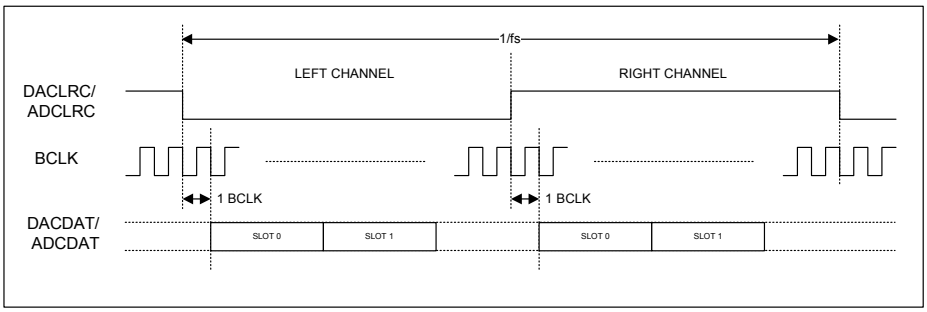


Figure 78 TDM in I²S Mode

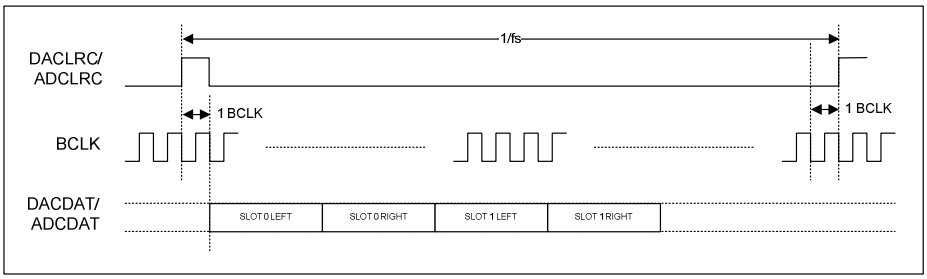


Figure 79 TDM in DSP Mode A

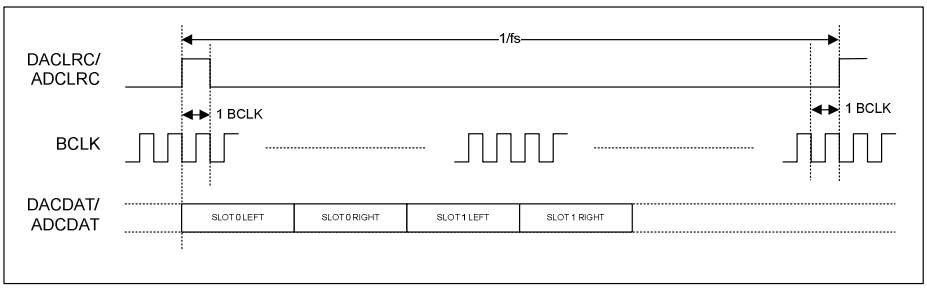


Figure 80 TDM in DSP Mode B

DIGITAL AUDIO INTERFACE CONTROL

The register bits controlling audio data format, word length, left/right channel data source and TDM are summarised in Table 71.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h)	15	AIFADCL_SRC	0b	Left ADC Data Source Select 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel
	14	AIFADCR_SRC	1b	Right ADC Data Source Select 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
	13	AIFADC_TDM	0b	ADC TDM Enable 0 = Normal ADCDAT operation 1 = TDM enabled on ADCDAT
	12	AIFADC_TDM_CHAN	0b	ADCDAT TDM Channel Select 0 = ADCDAT outputs data on slot 0 1 = ADCDAT output data on slot 1
	8	AIF_BCLK_INV	0b	BCLK Invert 0 = BCLK not inverted 1 = BCLK inverted
	7	AIF_LRCLK_INV	0b	Right, left and I^2S modes – LRCLK polarity 0 = normal LRCLK polarity 1 = invert LRCLK polarity
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)
	6:5	AIF_WL [1:0]	10b	Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits Note - see “Companding” for the selection of 8-bit mode
	4:3	AIF_FMT [1:0]	10b	Digital Audio Interface Format 00 = Right justified 01 = Left justified 10 = I^2S Format 11 = DSP Mode
R6 (06h)	15	DACL_SRC	0b	Left DAC Data Source Select 0 = Left DAC outputs left channel data 1 = Left DAC outputs right channel data
	14	DACR_SRC	1b	Right DAC Data Source Select 0 = Right DAC outputs left channel data 1 = Right DAC outputs right channel data
	13	AIFDAC_TDM	0b	DAC TDM Enable 0 = Normal DACDAT operation 1 = TDM enabled on DACDAT
	12	AIFDAC_TDM_CHAN	0b	DACDAT TDM Channel Select 0 = DACDAT data input on slot 0 1 = DACDAT data input on slot 1

Table 71 Audio Data Format Control

AUDIO INTERFACE OUTPUT AND GPIO TRISTATE

Register bit AIF_TRIS can be used to tristate the audio interface and GPIO pins as described in Table 72.

All GPIO[6:1] pins and digital audio interface pins will be tristated by this function, regardless of the state of other registers which control these pin configurations.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah)	13	AIF_TRIS	0	Audio Interface and GPIO Tristate 0 = Audio interface and GPIO pins operate normally 1 = Tristate all audio interface and GPIO pins

Table 72 Tri-stating the Audio Interface and GPIO Pins

MASTER MODE BCLK, ADCLRC AND DACLRC ENABLE

The main audio interface pins (BCLK, ADCLRC, ADCDAT, DACLRC and DACDAT) and the alternative DAC interface pins (BCLK2, DACLRC2, DACDAT2) can be independently programmed to operate in master mode or slave mode using register bits AIF_MSTR1 and AIF_MSTR2.

When the main audio interface is operating in slave mode, the BCLK, ADCLRC and DACLRC clock outputs to these pins are by default disabled to allow the digital audio source to drive these pins. Similarly, when the alternative audio interface is operating in slave mode, the BCLK2 and DACLRC2 clock outputs to these pins are by default disabled.

It is also possible to force the ADCLRC, DACLRC or DACLRC2 to be output using register bits ADCLRC_DIR and DACLRC_DIR, allowing mixed master and slave modes for the ADCs or the active DAC audio interface. The active audio interface is selected by register bit AIF_SEL. Enabled clock outputs on the de-selected audio interface will output logic 0.

When ADCLRC is configured as a GPIO pin (ALRCGPIO1=1), the DACLRC pin is used for the ADCs and the DACs and will only be disabled in master mode when both ADCs and both DACs are disabled.

The clock generators for the audio interface are enabled according to the control signals shown in Figure 81.

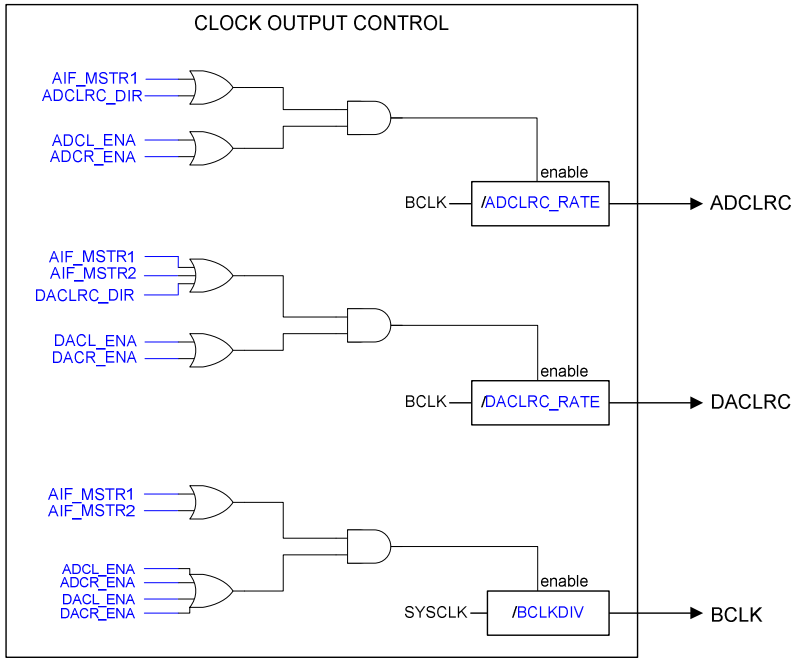


Figure 81 Clock Output Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h)	15	AIF_MSTR1	0b	Audio Interface 1 Master Mode Select 0 = Slave mode 1 = Master mode
	14	AIF_MSTR2	0b	Audio Interface 2 Master Mode Select 0 = Slave mode 1 = Master mode
	13	AIF_SEL	0b	Audio Interface Select 0 = Audio interface 1 1 = Audio interface 2 (GPIO3/BCLK2, GPIO4/DACLRC2, GPIO5/DACDAT2)
	11	ADCLRC_DIR	0b	ADCLRC Direction (Forces ADCLRC clock to be output in slave mode) 0 = ADCLRC normal operation 1 = ADCLRC clock output enabled
	10:0	ADCLRC_RATE [10:0]	040h	ADCLRC Rate ADCLRC clock output = BCLK / ADCLRC_RATE Integer (LSB = 1) Valid from 8..2047
R10 (0Ah)	15	ALRCGPIO1	0b	ADCLRC/GPIO1 Pin Function Select 0 = ADCLRC pin 1 = GPIO1 pin (ADCLRC connected to DACLRC internally)
	11	DACLRC_DIR	0b	DACLRC Direction (Forces DACLRC clock to be output in slave mode) 0 = DACLRC normal operation 1 = DACLRC clock output enabled
	10:0	DACLRC_RATE [10:0]	040h	DACLRC Rate DACLRC clock output = BCLK / DACLRC_RATE Integer (LSB = 1) Valid from 8..2047

Table 73 Digital Audio Interface Clock Output Control

COMPANDING

The WM8400 supports A-law and μ-law companding on both transmit (ADC) and receive (DAC) sides as shown in Table 74.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h)	4	DAC_COMP	0b	DAC Companding Enable 0 = disabled 1 = enabled
	3	DAC_COMPMODE	0b	DAC Companding Type 0 = μ-law 1 = A-law
	2	ADC_COMP	0b	ADC Companding Enable 0 = disabled 1 = enabled
	1	ADC_COMPMODE	0b	ADC Companding Type 0 = μ-law 1 = A-law

Table 74 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

μ-law (where μ=255 for the U.S. and Japan):

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \qquad -1 \le x \le 1$

A-law (where A=87.6 for Europe):

$F(x) = A|x| / (1 + \ln A)$ } for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ } for $1/A \le x \le 1$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ-law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSBs of data.

Companding converts 13 bits (μ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. This provides greater precision for low amplitude signals than for high amplitude signals, resulting in a greater usable dynamic range than 8 bit linear quantization. The companded signal is an 8-bit word comprising sign (1 bit), exponent (3 bits) and mantissa (4 bits).

8-bit mode is selected whenever DAC_COMP=1 or ADC_COMP=1. The use of 8-bit data allows samples to be passed using as few as 8 BCLK cycles per LRC frame. When using DSP mode B, 8-bit data words may be transferred consecutively every 8 BCLK cycles.

8-bit mode (without Companding) may be enabled by setting DAC_COMPMODE=1 or ADC_COMPMODE=1, when DAC_COMP=0 and ADC_COMP=0.

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 75 8-bit Companded Word Composition

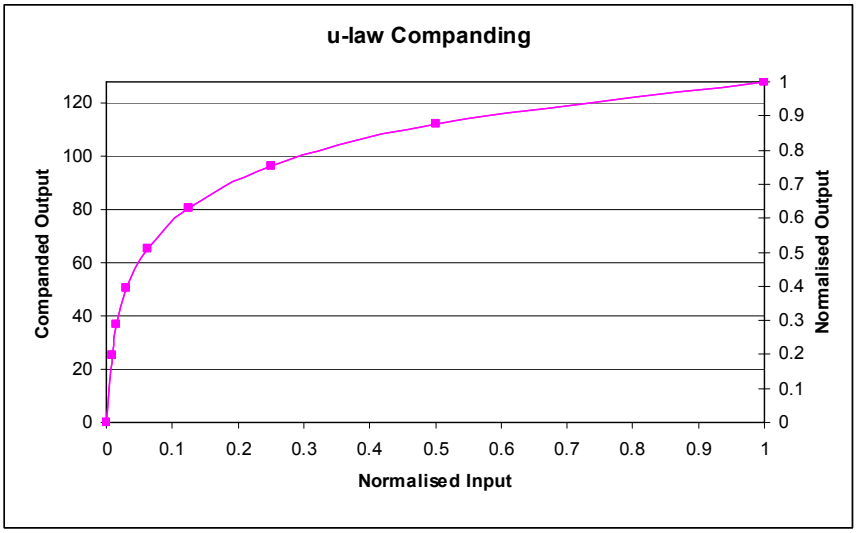


Figure 82 µ-Law Companding

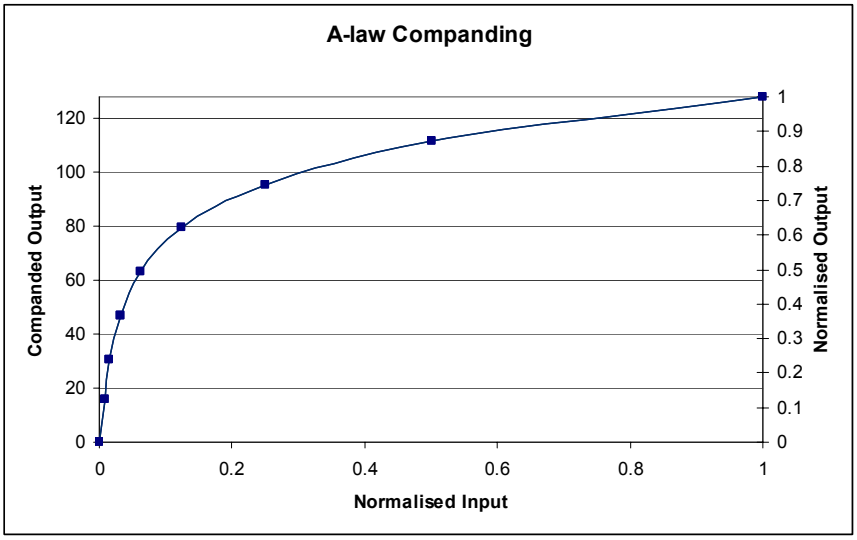


Figure 83 A-Law Companding

LOOPBACK

Setting the LOOPBACK register bit enables digital loopback. When this bit is set the output data from the ADC audio interface is fed directly into the DAC data input.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h)	0	LOOPBACK	0b	Digital Loopback Function 0 = No loopback 1 = Loopback enabled (ADC data output is directly input to DAC data input).

Table 76 Loopback Control

Note:

1. Master Mode: ADC and DAC left/right clocks must be set to the same pin when using LOOPBACK function (ALRCGPIO1=1)
2. Slave Mode: It is recommended to set ALRCGPIO1=1 as well, otherwise ADCLRC and DACLRC must be running at the same BCLK rate and in phase.
3. When the digital sidetone is enabled, ADC data will continue to be added to DAC data when LOOPBACK is enabled

AUDIO CODEC POWER MANAGEMENT

The WM8400 has three control registers that allow users to select which CODEC functions are active. For minimum power consumption, unused functions should be disabled. To avoid any pop or click noise, it is important to enable or disable functions in the correct order.

VMID_MODE is the enable for the Vmid reference, which defaults to disabled and can be enabled as a 2x50kΩ potential divider or, for low power maintenance of Vref when all other blocks are disabled, as a 2x300kΩ potential divider.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h)	13	SPK_MIX_ENA (rw)	0b	Speaker Mixer Enable 0 = disabled 1 = enabled
	12	SPK_ENA (rw)	0b	Speaker Output Enable 0 = disabled 1 = enabled
	11	OUT3_ENA (rw)	0b	OUT3 and OUT3MIX Enable 0 = disabled 1 = enabled
	10	OUT4_ENA (rw)	0b	OUT4 and OUT4MIX Enable 0 = disabled 1 = enabled
	9	LOUT_ENA (rw)	0b	LOUT (Left Headphone Output) Enable 0 = disabled 1 = enabled
	8	ROUT_ENA (rw)	0b	ROUT (Right Headphone Output) Enable 0 = disabled 1 = enabled
	4	MIC1BIAS_ENA (rw)	0b	MICBIAS Enable 0 = OFF (high impedance output) 1 = ON

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:1	VMID_MODE [1:0] (rw)	00b	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50kΩ divider (Normal mode) 10 = 2 x 300kΩ divider (Standby mode) 11 = 2 x 6.8kΩ divider (for fast start-up)
	0	VREF_ENA (rw)	0b	VREF Enable (Bias for all analogue functions) 0 = VREF bias disabled 1 = VREF bias enabled
R3 (03h)	15	FLL_ENA (rw)	0b	FLL Enable 0 = disabled 1 = enabled
	14	TSHUT_ENA (rw)	1b	Audio Components Thermal Sensor Enable 0 = Thermal sensor disabled 1 = Thermal sensor enabled
	13	TSHUT_OPDIS (rw)	1b	Audio Components Thermal Shutdown Enable (Requires thermal sensor to be enabled) 0 = Thermal shutdown disabled 1 = Thermal shutdown enabled
	11	OPCLK_ENA (rw)	0b	GPIO Clock Output Enable 0 = disabled 1 = enabled
	9	AINL_ENA (rw)	0b	Left Input Path Enable (Enables AINLMUX, INMIXL, DIFFINL and RXVOICE input to AINLMUX) 0 = disabled 1 = enabled
	8	AINR_ENA (rw)	0b	Left Input Path Enable (Enables AINRMUX, INMIXR, DIFFINR and RXVOICE input to AINRMUX) 0 = disabled 1 = enabled
	7	LIN34_ENA (rw)	0b	LIN34 Input PGA Enable 0 = disabled 1 = enabled
	6	LIN12_ENA (rw)	0b	LIN12 Input PGA Enable 0 = disabled 1 = enabled
	5	RIN34_ENA (rw)	0b	RIN34 Input PGA Enable 0 = disabled 1 = enabled
	4	RIN12_ENA (rw)	0b	RIN12 Input PGA Enable 0 = disabled 1 = enabled
	1	ADCL_ENA (rw)	0b	Left ADC Enable 0 = disabled 1 = enabled
	0	ADCR_ENA (rw)	0b	Right ADC Enable 0 = disabled 1 = enabled
R4 (04h)	13	LON_ENA (rw)	0b	LON Line Out and LONMIX Enable 0 = disabled 1 = enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	12	LOP_ENA (rw)	0b	LOP Line Out and LOPMIX Enable 0 = disabled 1 = enabled
	11	RON_ENA (rw)	0b	RON Line Out and RONMIX Enable 0 = disabled 1 = enabled
	10	ROP_ENA (rw)	0b	ROP Line Out and ROPMIX Enable 0 = disabled 1 = enabled
	7	LOPGA_ENA (rw)	0b	LOPGA Left Volume Control Enable 0 = disabled 1 = enabled
	6	ROPGA_ENA (rw)	0b	ROPGA Right Volume Control Enable 0 = disabled 1 = enabled
	5	LOMIX_ENA (rw)	0b	LOMIX Left Output Mixer Enable 0 = disabled 1 = enabled
	4	ROMIX_ENA (rw)	0b	ROMIX Right Output Mixer Enable 0 = disabled 1 = enabled
	1	DACL_ENA (rw)	0b	Left DAC Enable 0 = disabled 1 = enabled
	0	DACR_ENA (rw)	0b	Right DAC Enable 0 = disabled 1 = enabled

Table 77 Audio CODEC Power Management Registers

POWER MANAGEMENT SUBSYSTEM

INTRODUCTION

The WM8400 provides 2 DC-DC converters and 4 LDO regulators which each deliver high efficiency across a wide range of line and load conditions. These power management components are designed to support application processors and associated peripherals. They are also suitable for providing power to the analogue and digital functions of the on-board CODEC and GPIO features of the WM8400.

The output voltage of all the converters is programmable in software through control registers. The DC-DC converters and two of the LDOs can also be configured through hardware pins under start-up conditions.

The power control sequencer can be used to enable the on-board DC-DC converters and two of the LDO regulators in accordance with the desired start-up sequence. It can also be used to activate other system peripherals if required.

The WM8400 can be commanded to Soft Sleep mode, from which the CODEC and the converters may be placed in a low power condition, whilst still permitting a rapid return to the previous operating states. The WM8400 also supports a Deep Sleep mode, in which the CODEC is shut down entirely and the converters are placed in a user-configurable low power state.

POWER SEQUENCING AND CONTROL

POWER MANAGEMENT POWER DOMAINS

Operation of the power management functions requires appropriate power supplies to be connected to the HBVDD, MBVDD and LINE power domains. These supplies are referenced to GND. The operating ranges for these supplies are detailed in the “Recommended Operating Conditions” section.

HBVDD and MBVDD are power connections for the digital functions within the Host Buffer and Multi Media Buffer processors. LINE is the power supply input for support functions such as the UVLO, Reset and Oscillator functions. VINT is a regulated supply generated from the LINE input.

See ‘”Applications Informations for further details of external components required for VINT.

ENABLING THE DEVICE

The WM8400 is enabled by setting a logic high level on the NPDN pin (referenced to the HBVDD power domain). On start-up, a controlled sequence of events is initiated. When NPDN is set low to disable the device, a ‘soft shutdown’ is executed, where the CODEC and Power Management functions are disabled in a controlled manner, avoiding audio pops and other undesirable effects.

Note that the NPDN pin should not be connected directly to LINE as this will result in excessive leakage current through the device.

The PWRGOOD is used to indicate whether the device is in an active state or not. During device start-up or under a fault condition the PWRGOOD will be held in a logic low.

See “Chip Reset” for other requirements associated with device Start-Up.

See “Applications Information” for details of external components required to enable correct operation of the WM8400.

POWER SEQUENCING

As part of the start-up sequence (initiated by setting a logic high level on NPDN), the power sequencer outputs PSEQ1, PSEQ2, PSEQ3 and PSEQ4 are asserted according to a fixed sequence described in Table 78 and illustrated in Figure 84.

The sequencer commences operation approximately 40ms after NPDN has been set high.

TIME	OUTPUT
2 ms	PSEQ1 asserted
4 ms	PSEQ1 + PSEQ2 asserted
8 ms	PSEQ1 + PSEQ2 + PSEQ3 asserted
16 ms	PSEQ1 + PSEQ2 + PSEQ3 + PSEQ4 asserted

Table 78 Power Sequencing Outputs

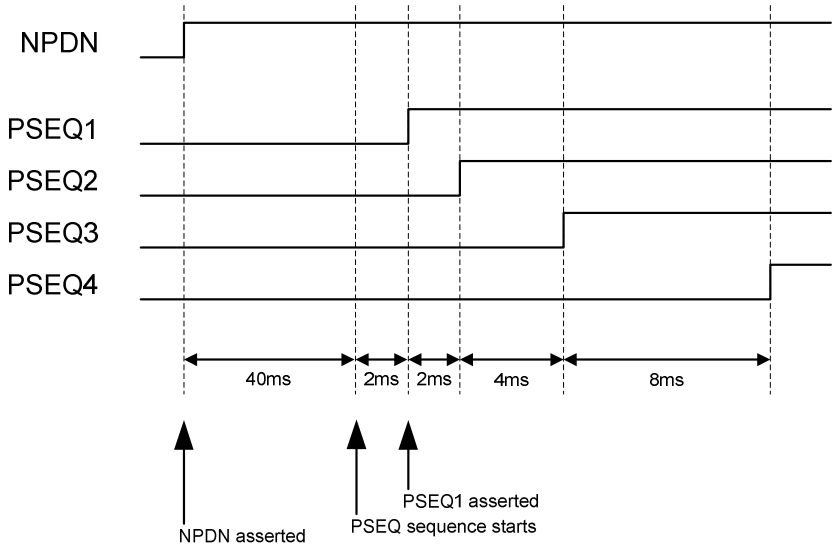


Figure 84 Power Sequencing Timing

The power sequencer outputs are digital outputs referenced to the LINE power domain. Each of these outputs may be connected to one or more of the DC-DC Converter or LDO Regulator hardware enable pins (see “Enabling the Converters”) in order to implement the desired power-up sequencing.

MMP CONTROL

The WM8400 can be used in conjunction with a Multi Media Processor (MMP) device. In such an application, the WM8400 would provide power supplies to the MMP using the integrated DC-DC Converters and LDO Regulators. The WM8400 can also generate a Reset signal for the MMP, which is co-ordinated with the WM8400 power-up sequence.

The WM8400 provides a hardware input RSTTRIG as part of this MMP Control function. Setting RSTTRIG to a logic high level (referenced to the HBVDD power domain) triggers the Reset Delay Timer. In a typical application, the RSTTRIG signal could be wired to the PSEQ4 output; this will trigger the Reset Delay Timer automatically as part of the power-up sequence.

If any of the enabled DC-DC Converters or LDO Regulators is Under Voltage, then RSTTRIG will not immediately trigger the Reset Delay Timer. If the Under Voltage is not cleared within 500ms of the start-up signal NPDN being asserted, the Reset Delay Timer will be triggered at this point.

If RSTTRIG is not asserted within 500ms of the start-up signal NPDN being asserted, the Reset Delay Timer will be triggered at this point. In this event, the interrupt event CDELAY Timeout (CDEL_TO_EINT) will be set.

The duration of the Reset Delay Timer is set by the value of a capacitor connected to CDELAY. See “Applications Information” for more details of this capacitor.

On completion of the Reset Delay Timer, the WM8400 enables the MMP by setting the NRST output to a logic high level (referenced to the MBVDD power domain). This signal is used to hold the MMP in a Reset state whilst the WM8400 starts up.

If a CDELAY error condition occurs (eg. due to CDELAY/GND short circuit or unsuitable CDELAY capacitance), then normal WM8400 functionality cannot be supported and a device shutdown is initiated. The CDEL_TO_EINT is also set under this condition.

POWER MANAGEMENT OPERATING MODES

The WM8400 has three operating modes, including two sleep modes. The sleep modes result in reduced power consumption and restricted functionality. The operating mode may be selected in software via the PWR_STATE register field. Deep Sleep mode may also be selected in hardware by asserting HSLEEP or MSLEEP.

Table 79 provides a summary of the WM8400 functions in Active, Soft Sleep and Deep Sleep Operating modes. Note that the “Hibernate” state of the DC converters and LDO regulators is configurable, as described below.

OPERATING MODE	CODEC	DC-DC CONVERTERS	LDO REGULATORS
Active	Active	Active	Active
Soft Sleep	Half-bias	Standby/Hysteretic	Active
Deep Sleep	Off	Hibernate	Hibernate

Table 79 WM8400 Operating Modes

When the CODEC is placed in Half-Bias mode, full functionality is maintained, but the power savings will result in slightly degraded performance of the analogue functions.

When the DC-DC Converters are placed in Standby/Hysteretic mode, this results in reduced regulation of the DC output, and reduced power consumption. When the DC-DC converters are placed in Hibernate, they are either disabled or operate in a low power LDO mode, depending on user settings.

When the LDOs are placed in Hibernate mode, they are either disabled or operate in a low power mode, depending on user settings.

OPERATING MODE CONTROL

The operating mode may be selected in software using the PWR_STATE register field, as defined in Table 80.

The operating mode may also be selected by a logic level applied to MSLEEP (referenced to MBVDD) or HSLEEP (referenced to HBVDD). By default, these inputs are active high. The polarity of these pins may be inverted using the DSLEEP1_POL and DSLEEP2_POL register fields. When MSLEEP or HSLEEP is asserted, this takes precedence over the PWR_STATE setting, and places the WM8400 in Deep Sleep mode.

In summary, the Deep Sleep state may be entered in three ways: (1) Asserting MSLEEP, or (2) Asserting HSLEEP, or (3) Setting PWR_STATE = 10.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R76 (4Ch)	3	DSLEEP1_POL	0	MSLEEP control 0 = Active high 1 = Active low
	2	DSLEEP2_POL	0	HSLEEP control 0 = Active high 1 = Active low
	1:0	PWR_STATE	00	Power State software control 00 = Active 01 = Soft Sleep 10 = Deep Sleep 11 = Reserved

Table 80 WM8400 Power State Control

CONFIGURING THE DC-DC CONVERTERS AND LDO REGULATORS

ENABLING THE CONVERTERS

The DC-DC converters and the LDO regulators can be enabled in software using register fields as defined in Table 81.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (41h)	15	LDO1_ENA	0b	LDO1 Software enable 0 = Disabled 1 = Enabled
R66 (42h)	15	LDO2_ENA	0b	LDO2 Software enable 0 = Disabled 1 = Enabled
R67 (43h)	15	LDO3_ENA	0b	LDO3 Software enable 0 = Disabled 1 = Enabled
R68 (44h)	15	LDO4_ENA	0b	LDO4 Software enable 0 = Disabled 1 = Enabled
R70 (46h)	15	DC1_ENA	0b	DC1 Software enable 0 = Disabled 1 = Enabled
R72 (48h)	15	DC2_ENA	0b	DC2 Software enable 0 = Disabled 1 = Enabled

Table 81 DC-DC Converter and LDO Regulator Software Enable

The DC-DC converters, LDO1 and LDO2 can also be enabled by asserting a logic high level on the associated hardware pins. These logic inputs are referenced to HBVDD. A logic high on these pins takes precedence over the corresponding software control.

The hardware enable pins may be connected to the power sequencing outputs PSEQ1, PSEQ2, PSEQ3, PSEQ4 or may be driven by another device. These pins should not be left floating (unconnected); the logic state of these inputs is undefined if these pins are floating.

PIN NAME	FUNCTION
DC1EN	DC1 Hardware enable 0 = Disable (software control) 1 = Enable
DC2EN	DC2 Hardware enable 0 = Disable (software control) 1 = Enable
LDO1EN	LDO1 Hardware enable 0 = Disable (software control) 1 = Enable
LDO2EN	LDO2 Hardware enable 0 = Disable (software control) 1 = Enable

Table 82 DC-DC Converter and LDO Regulator Hardware Enable

LDO FUNCTION SELECT

To provide maximum flexibility, the LDOs can be configured to operate as current-limited switches instead of as regulators. This is achieved by writing to the register bits defined below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (41h)	14	LDO1_SWI	0b	LDO1 function select 0 = LDO Regulator 1 = Current Limited switch
R66 (42h)	14	LDO2_SWI	0b	LDO2 Software enable 0 = LDO Regulator 1 = Current Limited switch
R67 (43h)	14	LDO3_SWI	0b	LDO3 Software enable 0 = LDO Regulator 1 = Current Limited switch
R68 (44h)	14	LDO4_SWI	0b	LDO4 Software enable 0 = LDO Regulator 1 = Current Limited switch

Table 83 LDO Function Select

DC-DC CONVERTER OPERATING MODES

The DC-DC Converters have three distinct operating modes, which are as follows:

- Active
- Standby/Hysteretic
- Hibernate

The DC-DC Converter operating modes are selected using the register bits described in Table 84.

In Active mode, the DC-DC Converters operate to their highest level of performance. The DC-DC Converters will automatically select PWM or Pulse-Skipping operation according to the load condition. This enables the power efficiency to be maximised across a wide range of load conditions. It is possible to force the Converters to use the higher performance PWM mode by setting DC1_FRC_PWM or DC2_FRC_PWM.

In Standby/Hysteretic Mode, the DC-DC Converters use a hysteretic mode of operation in order to reduce power consumption. The load regulation is degraded in this mode of operation.

In Hibernate Mode, the DC-DC Converters are either disabled or are reconfigured as low power LDOs, according to user settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R70 (46h)	14	DC1_ACTIVE	1b	DC1 Active Mode select 0 = Standby/Hysteretic Mode selected 1 = Active Mode selected
	13	DC1_SLEEP	0b	DC1 Sleep Mode select 0 = Not selected 1 = Selected
R71 (47h)	13	DC1_FRC_PWM	0b	DC1 Force PWM operation 0 = Not selected 1 = PWM operation forced
R72 (48h)	14	DC2_ACTIVE	1b	DC2 Active Mode select 0 = Standby/Hysteretic Mode selected 1 = Active Mode selected
	13	DC2_SLEEP	0b	DC2 Sleep Mode select 0 = Not selected 1 = Selected
R73 (49h)	13	DC2_FRC_PWM	0b	DC2 Force PWM operation 0 = Not selected 1 = PWM operation forced

Table 84 DC-DC Converter Operating Modes

When the WM8400 is placed in Soft Sleep or Deep Sleep Modes (see Table 79), this may take precedence over the _SLEEP and _ACTIVE register selections. In summary, the DC-DC Converter Operating mode is selected according to the following truth table for DC1. The equivalent logic applies for DC2 Converter.

Note that the DC-DC Converters must also be enabled in hardware or software as described earlier.

WM8400 OPERATING MODE	DC1_SLEEP	DC1_ACTIVE	DC1 OPERATING MODE
Active	0	0	Standby/Hysteretic
	0	1	Active
	1	X	Hibernate
Soft Sleep	0	X	Standby/Hysteretic
	1	X	Hibernate
Deep Sleep	X	X	Hibernate

Table 85 DC1 Converter Operating Mode Selection

DC-DC CONVERTER / LDO REGULATOR VOLTAGE SELECT

The output voltage of the DC-DC Converters and LDO Regulators may be set in hardware or using software control. If software control is used, the output voltages may be set using the register fields detailed in Table 86. The output voltages may be set dynamically, without needing to disable or reset any part of the WM8400. Note that the output voltages in Hibernate Mode are separately configured (see Table 91).

In the case of the DC-DC Converters, note that the performance figures in the Electrical Characteristics are valid for output voltages of up to 3.4v only.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (41h)	4:0	LDO1_VSEL [4:0]	00000b	LDO1 voltage select 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details
R66 (42h)	4:0	LDO2_VSEL [4:0]	00000b	LDO2 voltage select 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details
R67 (43h)	4:0	LDO3_VSEL [4:0]	00000b	LDO3 voltage select 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details
R68 (44h)	4:0	LDO4_VSEL [4:0]	00000b	LDO4 voltage select 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details
R70 (46h)	6:0	DC1_VSEL [6:0]	0000000b	DC1 voltage select 0.85v to 4.025v in 0.025v steps See Table 88 for details
R72 (48h)	6:0	DC2_VSEL [6:0]	0000000b	DC2 voltage select 0.85v to 4.025v in 0.025v steps See Table 88 for details

Table 86 DC-DC Converter and LDO Regulator Voltage Setting (Software)

The coding for the LDO Regulator voltage select fields is detailed in Table 87.

LDO1_VSEL, LDO2_VSEL, LDO3_VSEL, LDO4_VSEL	LDO OUTPUT	LDO1_VSEL, LDO2_VSEL, LDO3_VSEL, LDO4_VSEL	LDO OUTPUT
00000	0.90v	10000	1.80v
00001	0.95v	10001	1.90v
00010	1.00v	10010	2.00v
00011	1.05v	10011	2.10v
00100	1.10v	10100	2.20v
00101	1.15v	10101	2.30v
00110	1.20v	10110	2.40v
00111	1.25v	10111	2.50v
01000	1.30v	11000	2.60v
01001	1.35v	11001	2.70v
01010	1.40v	11010	2.80v
01011	1.45v	11011	2.90v
01100	1.50v	11100	3.00v
01101	1.55v	11101	3.10v
01110	1.60v	11110	3.20v
01111	1.70v	11111	3.30v

Table 87 LDO Regulator Output Voltage

The coding for the DC-DC Converter voltage select fields is detailed in Table 88.

DC1_VSEL, DC2_VSEL	DC OUTPUT	DC1_VSEL, DC2_VSEL	DC OUTPUT	DC1_VSEL, DC2_VSEL	DC OUTPUT
0000000	0.850v	0101011	1.925v	1010110	3.000v
0000001	0.875v	0101100	1.950v	1010111	3.025v
0000010	0.900v	0101101	1.975v	1011000	3.050v
0000011	0.925v	0101110	2.000v	1011001	3.075v
0000100	0.950v	0101111	2.025v	1011010	3.100v
0000101	0.975v	0110000	2.050v	1011011	3.125v
0000110	1.000v	0110001	2.075v	1011100	3.150v
0000111	1.025v	0110010	2.100v	1011101	3.175v
0001000	1.050v	0110011	2.125v	1011110	3.200v
0001001	1.075v	0110100	2.150v	1011111	3.225v
0001010	1.100v	0110101	2.175v	1100000	3.250v
0001011	1.125v	0110110	2.200v	1100001	3.275v
0001100	1.150v	0110111	2.225v	1100010	3.300v
0001101	1.175v	0111000	2.250v	1100011	3.325v
0001110	1.200v	0111001	2.275v	1100100	3.350v
0001111	1.225v	0111010	2.300v	1100101	3.375v
0010000	1.250v	0111011	2.325v	1100110	3.400v
0010001	1.275v	0111100	2.350v	1100111	3.425v
0010010	1.300v	0111101	2.375v	1101000	3.450v
0010011	1.325v	0111110	2.400v	1101001	3.475v
0010100	1.350v	0111111	2.425v	1101010	3.500v
0010101	1.375v	1000000	2.450v	1101011	3.525v
0010110	1.400v	1000001	2.475v	1101100	3.550v
0010111	1.425v	1000010	2.500v	1101101	3.575v
0011000	1.450v	1000011	2.525v	1101110	3.600v
0011001	1.475v	1000100	2.550v	1101111	3.625v
0011010	1.500v	1000101	2.575v	1110000	3.650v

DC1_VSEL, DC2_VSEL	DC OUTPUT	DC1_VSEL, DC2_VSEL	DC OUTPUT	DC1_VSEL, DC2_VSEL	DC OUTPUT
0011011	1.525v	1000110	2.600v	1110001	3.675v
0011100	1.550v	1000111	2.625v	1110010	3.700v
0011101	1.575v	1001000	2.650v	1110011	3.725v
0011110	1.600v	1001001	2.675v	1110100	3.750v
0011111	1.625v	1001010	2.700v	1110101	3.775v
0100000	1.650v	1001011	2.725v	1110110	3.800v
0100001	1.675v	1001100	2.750v	1110111	3.825v
0100010	1.700v	1001101	2.775v	1111000	3.850v
0100011	1.725v	1001110	2.800v	1111001	3.875v
0100100	1.750v	1001111	2.825v	1111010	3.900v
0100101	1.775v	1010000	2.850v	1111011	3.925v
0100110	1.800v	1010001	2.875v	1111100	3.950v
0100111	1.825v	1010010	2.900v	1111101	3.975v
0101000	1.850v	1010011	2.925v	1111110	4.000v
0101001	1.875v	1010100	2.950v	1111111	4.025v
0101010	1.900v	1010101	2.975v		

Table 88 DC-DC Converter Output Voltage

During Start-Up, the output voltage of the DC-DC Converters and LDO1 and LDO2 Regulators may be set in hardware using the DC1VSEL, DC2VSEL, LDO1VSEL and LDO2VSEL pins respectively. Hardware control of the output voltage is implemented by setting these pins to a logic level or by connecting the voltage select pin to a potential divider on the output of the corresponding converter or regulator. (In the case of the DC-DC Converters, the 'Output' is the DC1FB or DC2FB pin.)

The hardware voltage select pins are checked during Start-Up, and the applicable voltage select registers are set to the equivalent values by the WM8400. On completion of Start-Up, and once PWRGOOD has been asserted, the voltage select pins have no further effect, and control is passed to the software controlled registers only.

The hardware configurations are illustrated in Table 89.

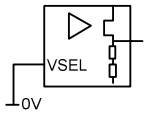
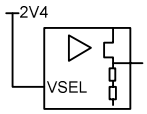
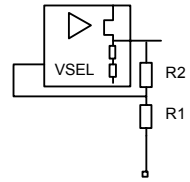
	DC1	DC2	LDO1	LDO2
	DC1VSEL connected to 0v Output voltage = 1.2v	DC2VSEL connected to 0v Output voltage = 2.8v	LDO1VSEL connected to 0v Output voltage = 1.2v	LDO2VSEL connected to 0v Output voltage = 1.8v
	DC1VSEL connected to 2.4v Output voltage = 1.35v	DC2VSEL connected to 2.4v Output voltage = 3.3v	LDO1VSEL connected to 2.4v Output voltage = 1.35v	LDO2VSEL connected to 2.4v Output voltage = 3.3v
	DC1VSEL connected to Output * (R1 / (R1+R2)) Output voltage = 0.625 * (R1+R2) / R1	DC2VSEL connected to Output * (R1 / (R1+R2)) Output voltage = 0.625 * (R1+R2) / R1	LDO1VSEL connected to Output * (R1 / (R1+R2)) Output voltage = 0.625 * (R1+R2) / R1	LDO2VSEL connected to Output * (R1 / (R1+R2)) Output voltage = 0.625 * (R1+R2) / R1

Table 89 DC-DC Converter and LDO Regulator Voltage Setting (Hardware)

For best accuracy, the fixed default voltages should be used if possible. These default settings (selected by connecting VSEL pins to 0V or to 2.4V) are intended to meet the requirements of the most likely usage scenarios. In this configuration, the resistance of the VSEL connection to 0V or 2.4V should be as low as possible, and must be less than 50kΩ.

If the programmable start-up voltage method is used (ie. connecting VSEL to a resistive divider), the resistors should be selected as described in Table 89. It is also an important requirement that the parallel combination of resistors R1 and R2 must equate to at least 100kΩ.

The parallel combination of resistors R1 and R2 is calculated using the equation below. If the parallel resistance is too small, then R1 and R2 should be scaled in order to achieve a suitable value.

$$\text{Parallel Resistance R1,R2} = \frac{1}{\left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Some limitations of the programmable start-up voltage method should be noted. In start-up, the WM8400 initially selects the lowest valid output voltage for each applicable LDO or DC-DC Converter. The control circuit then steps incrementally through the available voltage selections (listed in Table 87 and Table 88) until the desired output voltage is reached. The control circuit detects the desired output voltage using a comparator connected to the VSEL pin. The comparator reference is 0.625V.

If the LDO or DC-DC Converter is loaded during start-up, this may result in the selection of a slightly higher output voltage setting than the value set by R1 and R2. The voltage drop caused by the load causes the VSEL voltage to be reduced also. In this case, the control circuit continues to increment the LDO or DC-DC Converter output voltage until the correct voltage is sensed at VSEL. When this has been achieved, the output voltage of the converter may be slightly higher than under ideal conditions. The magnitude of the error may be larger in the case of the LDOs, as the voltage control steps are larger. The voltage error is more likely to arise under high load conditions.

An important consequence of this behaviour is that the maximum LDO or DC-DC Converter output voltages cannot be selected in start-up. This is because, in attempting to achieve the required voltage on VSEL, the control circuit may attempt to select an output voltage higher than the maximum, which can lead to an unstable condition.

The maximum recommended start-up output voltage selected by R1 and R2 is 3.1V (for LDO1 and LDO2) and 3.975V (for DC1 and DC2). (As noted earlier, the performance figures in the Electrical Characteristics are valid for DC-DC output voltages of up to 3.4V only.)

The limitations described above are only applicable during the start-up phase of the WM8400. It is recommended that the voltage select registers (see Table 87 and Table 88) should be set in software at the earliest opportunity after start-up in order to ensure accurate output voltage regulation for normal running conditions. Note that, after start-up, the VSEL pins are no longer used.

DC-DC CONVERTER CURRENT LIMIT

In Active mode, the DC-DC Converters are primarily designed to operate up to 600mA. However, it is possible to run the device for short periods of time with loads up to 1000mA. This feature is controlled through register bits DC1_ACT_LIM and DC2_ACT_LIM.

It is important to note that currents in excess of 600mA may give rise to excessive temperatures within the device. Care must be taken to ensure that the maximum junction temperature is not exceeded - see “Thermal Characteristics”. It is recommended that the Current Limit register field be returned to the 600mA setting when the device is not required to support exceptional load currents.

In DC-DC Converter Standby/Hysteretic mode, a different current limit is applied to the DC-DC Converters. This limit is set by the DC1_STBY_LIM and DC2_STBY_LIM fields, in conjunction with DC1_ACT_LIM and DC2_ACT_LIM. These fields are described in Table 90.

Note that, in Hibernate mode, the current limit is not programmable.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R71 (47h)	9:8	DC1_STBY_LIM [1:0]	00b	DC1 Standby Mode current limit If DC1_ACT_LIM = 0: 00 = 70mA 01 = 150mA 10 = 300mA 11 = 600mA If DC1_ACT_LIM = 1: 00 = 110mA 01 = 220mA 10 = 450mA 11 = 900mA
	7	DC1_ACT_LIM	0b	DC1 Active Mode current limit 0 = 600mA 1 = 1000mA
R73 (49h)	9:8	DC2_STBY_LIM [1:0]	00b	DC2 Standby Mode current limit If DC2_ACT_LIM = 0: 00 = 70mA 01 = 150mA 10 = 300mA 11 = 600mA If DC2_ACT_LIM = 1: 00 = 110mA 01 = 220mA 10 = 450mA 11 = 900mA
	7	DC2_ACT_LIM	0b	DC2 Active Mode current limit 0 = 600mA 1 = 1000mA

Table 90 DC-DC Converter Current Limit

HIBERNATE MODE CONFIGURATION

The DC-DC Converters and LDO Regulators are placed in Hibernate Mode when the WM8400 is in Deep Sleep mode. The DC-DC Converters can also be individually placed in Hibernate Mode using the DC1_SLEEP and DC2_SLEEP register bits.

The behaviour of the DC-DC Converters and LDO Regulators in Hibernate Mode may be set in software. Each of the Converters and Regulators can be selected to switch off in Hibernate Mode, or else to adopt a low power operating state and an 'image' voltage output. The applicable register fields are described in Table 91.

When a DC-DC Converter is enabled in Hibernate mode, it operates as a low power LDO converter, and not as a buck converter. Note that the DC-DC Converters and LDO Regulators must also be enabled in hardware or software as described earlier.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (41h)	10	LDO1_HIB_MODE	0b	LDO1 Hibernate Mode 0 = LDO1 disabled in Hibernate 1 = LDO1 enabled in Hibernate
	9:5	LDO1_VIMG [4:0]	00000b	LDO1 Hibernate Mode output voltage 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details.
R66 (42h)	10	LDO2_HIB_MODE	0b	LDO2 Hibernate Mode 0 = LDO2 disabled in Hibernate 1 = LDO2 enabled in Hibernate
	9:5	LDO2_VIMG [4:0]	00000b	LDO2 Hibernate Mode output voltage 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details.
R67 (43h)	10	LDO3_HIB_MODE	0b	LDO3 Hibernate Mode 0 = LDO3 disabled in Hibernate 1 = LDO3 enabled in Hibernate
	9:5	LDO3_VIMG [4:0]	00000b	LDO3 Hibernate Mode output voltage 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details.
R68 (44h)	10	LDO4_HIB_MODE	0b	LDO4 Hibernate Mode 0 = LDO4 disabled in Hibernate 1 = LDO4 enabled in Hibernate
	9:5	LDO4_VIMG [4:0]	00000b	LDO4 Hibernate Mode output voltage 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details.
R70 (46h)	10	DC1_HIB_MODE	1b	DC1 Hibernate Mode 0 = DC1 disabled in Hibernate 1 = DC1 enabled (LDO mode) in Hibernate
R71 (47h)	6:0	DC1_VIMG [6:0]	0000000b	DC1 Hibernate Mode output voltage 0.85v to 4.025v in 0.025v steps See Table 88 for details
R72 (48h)	10	DC2_HIB_MODE	1b	DC2 Hibernate Mode 0 = DC2 disabled in Hibernate 1 = DC2 enabled (LDO mode) in Hibernate
R73 (49h)	6:0	DC2_VIMG [6:0]	0000000b	DC2 Hibernate Mode output voltage 0.85v to 4.025v in 0.025v steps See Table 88 for details

Table 91 Hibernate Mode Configuration

DC-DC CONVERTER SOFT START

A soft start feature may be enabled on either of the DC-DC Converters, in order to limit the in-rush current when they are enabled. When a converter is enabled with soft-start selected, a current limit will initially be applied to the DC-DC Converter output. This current limit will be increased up to the maximum current in three stages. The register fields in Table 92 control the duration of the three stages. Therefore, when soft-start is enabled, the full start-up time for that DC-DC Converter will be 3 x Soft Start time.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R70 (46h)	9:8	DC1_SOFTST [1:0]	00b	DC1 Soft Start 00 = No soft start 01 = 400us steps 10 = 4ms steps 11 = 40ms steps
R72 (48h)	9:8	DC2_SOFTST [1:0]	00b	DC2 Soft Start 00 = No soft start 01 = 400us steps 10 = 4ms steps 11 = 40ms steps

Table 92 DC-DC Converter Soft Start

UNDERVOLTAGE DETECTION

Each DC-DC Converter and LDO Regulator is monitored for voltage accuracy. An Undervoltage condition is set if the voltage falls below 95% of the required level. The action taken in response to an Undervoltage condition can be set independently for each DC-DC Converter and each LDO Regulator, as described in Table 93.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (41h)	11	LDO1_ERRACT	0b	LDO1 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
R66 (42h)	11	LDO2_ERRACT	0b	LDO2 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
R67 (43h)	11	LDO3_ERRACT	0b	LDO3 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
R68 (44h)	11	LDO4_ERRACT	0b	LDO4 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
R70 (46h)	11	DC1_ERRACT	0b	DC1 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
R72 (48h)	11	DC2_ERRACT	0b	DC2 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device

Table 93 Undervoltage Detection Control

OVERVOLTAGE PROTECTION

When inductive components are connected to the Converters or Regulators, it is possible that voltage overshoot can occur during load or line transitions. The WM8400 provides overvoltage protection circuitry on the DC-DC Converters which minimizes these effects. When enabled, the overvoltage protection aims to limit the transient voltage at 50mv above the selected level. This feature is enabled using the register bits described in Table 94.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R70 (46h)	7	DC1_OV_PROT	0b	DC1 Overvoltage Protection 0 = Disabled 1 = Enabled
R72 (48h)	7	DC2_OV_PROT	0b	DC2 Overvoltage Protection 0 = Disabled 1 = Enabled

Table 94 DC-DC Converter Overvoltage Control

DC-DC CONVERTER OPERATION

The WM8400 provides two DC-DC switching Buck Converters. These are versatile, step-down, PWM controlled converters, designed to deliver high efficiency across all load conditions up to 600mA.

They are typically suitable for powering Digital Core and I/O functions. Their principal characteristics are summarised in Table 95.

PARAMETER	VALUE
Converter Type	Buck Converter
Input Voltage Range	2.7V to 5.5V
Output Voltage Range	0.85V to 4.025V (performance only measured to 3.4V)
Maximum Load Current	600mA (short term output up to 1000mA is possible)
Switching frequency	2.048MHz

Table 95 DC-DC Converter Characteristics

The connections to the Converter DC1 are illustrated in Figure 85. The equivalent circuit applies to DC Converter 2 also.

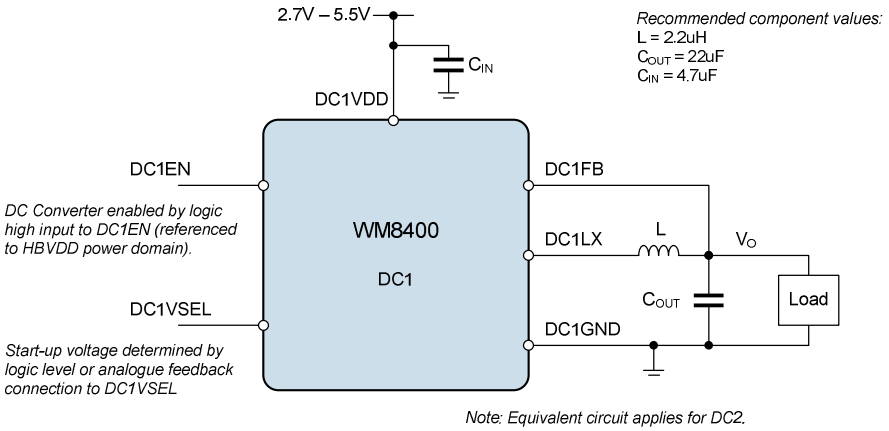


Figure 85 DC-DC Converter Connections

The external components at the converter output are required by the DC-DC Converter integral loop compensation circuit. Note that the recommended output capacitor Cout varies according to the required transient response on each DC-DC Converter. See “Applications Information” for details of the recommended external components.

LDO REGULATOR OPERATION

The WM8400 provides four LDO Regulators. All of these are dynamically programmable in software; LDO1 and LDO2 may also be enabled and configured in hardware.

In a typical application, LDO3 and LDO4 are suitable for powering the CODEC circuits. In such a case, LDO3 could supply 3.0V to AVDD/HPVDD and LDO4 could supply 1.8V to DCVDD.

The principal characteristics of the LDOs are summarised in Table 96.

PARAMETER	VALUE
Converter Type	Low Drop-Out Regulator (LDO)
Input Voltage Range	2.5V to 5.5V
Output Voltage Range	0.9V to 3.3V
Maximum Load Current	150mA (short term output up to 250mA is possible)
Drop-Out Voltage (Vout < 1.8V)	700mV (typical)
Drop-Out Voltage (Vout > 1.8V)	200mV (typical)

Table 96 LDO Regulator Characteristics

The connections to the LDO Regulator 1 are illustrated in Figure 86. The equivalent circuit applies to LDO2, LDO3 and LDO4 also.

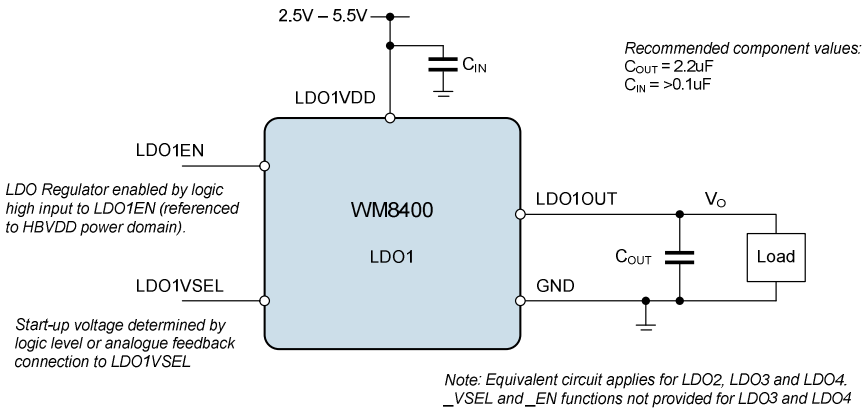


Figure 86 LDO Regulator Connections

An input and output capacitor are recommended for each LDO Regulator, as illustrated above. See "Applications Information" for details of these external components.

CURRENT REFERENCE

The Power Management functions on the WM8400 use an integrated current reference circuit. This circuit requires the connection of an external resistor to the RIREF pin. A 100kΩ resistor is recommended - see "Applications Information".

BATTERY MONITORING AND UNDERVOLTAGE LOCK-OUT (UVLO)

The WM8400 incorporates a Battery Comparator Supervisory function, which monitors the voltage on the LINE supply pin and compares it with programmable thresholds. This feature can be used to ensure that a suitable supply is available before enabling any dependent peripherals and also enables the WM8400 to respond to any drops in Battery voltage. Note that a different threshold is provided for increasing LINE voltage and for decreasing LINE voltage. The device behaviour when the LINE voltage falls below the threshold LINE_CMP_VTHD is set using register bit LINE_CMP_ERRACT. When the LINE voltage falls below LINE_CMP_VTHD, the associated Interrupt Level bit LINE_CMP_LVL will be set. Unless specifically masked, this condition will also trigger an Interrupt (IRQ) Event (see "Interrupt Events"). The LINE_CMP_LVL bit will be reset once the LINE voltage has risen above the threshold LINE_CMP_VTHI.

It is recommended that the thresholds are set during the initial set-up programming stages

The Undervoltage Lock-Out (UVLO) circuit monitors the voltage on the LINE supply pin. An Undervoltage condition is detected if this voltage drops below a threshold of 2.7v ±0.1v. Under this condition, the accuracy and regulation of all the DC-DC Converters and LDO Regulators is likely to be degraded. The device behaviour under this condition can be set using register bit UVLO_ERRACT, as detailed in Table 97.

If an IRQ event arises from these functions, this causes the NIRQ pin to output a logic low level (referenced to the MBVDD power domain).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R78 (4Eh)	7	LINE_CMP_ERRACT	1b	Battery Comparator Action 0 = Battery failure condition generates IRQ only 1 = Battery failure condition generates IRQ and initiates device shutdown
	6	UVLO_ERRACT	1b	Undervoltage Lock-Out Action 0 = UVLO generates IRQ only 1 = UVLO generates IRQ and initiates device shutdown
R84 (54h)	7:4	LINE_CMP_VTHI [3:0]	0111b	Rising Threshold for LINE comparator 2.70v to 3.45v in 50mv steps See Table 98 for details
	3:0	LINE_CMP_VTHD [3:0]	0100b	Falling Threshold for LINE comparator 2.70v to 3.45v in 50mv steps See Table 98 for details

Table 97 Battery Comparator and Undervoltage Lock-Out Control

The coding for the Battery Comparator threshold voltage select fields is detailed in Table 98.

LINE_CMP_VTHI, LINE_CMP_VTHD	BATTERY COMPARATOR THRESHOLD	LINE_CMP_VTHI, LINE_CMP_VTHD	BATTERY COMPARATOR THRESHOLD
0000	2.70	1000	3.10
0001	2.75	1001	3.15
0010	2.80	1010	3.20
0011	2.85	1011	3.25
0100	2.90	1100	3.30
0101	2.95	1101	3.35
0110	3.00	1110	3.40
0111	3.05	1111	3.45

Table 98 Battery Comparator Threshold Voltage Control

INTERRUPT EVENTS

The WM8400 continuously monitors its input and output voltages, device temperature and other events. The NIRQ output pin can be used to signal events or abnormal conditions associated with these monitoring functions. Register fields also provide the ability to read the status of these event detection features. The debounced status of these fields is available in Register 81 (51h).

By default, each of these fields will trigger an Interrupt (IRQ) event, resulting in the corresponding bit in Register 79 (4Fh) being set. Individual Mask bits in Register 80 (50h) can be used to prevent an Interrupt being generated by a specific event.

In the case of MIC Current detect, MIC Short Circuit detect, Jack detect (Left) and Jack detect (Right), an Interrupt event is triggered on rising and falling edges of the event. All other Interrupt events occur only on the rising edge of the event (eg. when a temperature threshold is exceeded, or an LDO goes undervoltage).

The unmasked Interrupt events are latched in Register 79 (4Fh) until a Register Read is scheduled at that address. When any Interrupt event is latched in Register 79 (4Fh), the NIRQ pin is set logic low (referenced to the MBVDD power domain). The NIRQ will return to its normal logic high level after the Interrupt Status Register (R79) has been read.

The Register fields associated with the Interrupt events are described in Table 99.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R79 (4Fh)	15	MICD_CINT	0b	MIC Current Detect IRQ status 0 = MIC Current IRQ not set 1 = MIC Current IRQ set
	14	MICSCD_CINT	0b	MIC Short Circuit IRQ status 0 = MIC Short Circuit IRQ not set 1 = MIC Short Circuit IRQ set
	13	JDL_CINT	0b	Jack Detect (Left) IRQ status 0 = Jack Detect (Left) IRQ not set 1 = Jack Detect (Left) IRQ set
	12	JDR_CINT	0b	Jack Detect (Right) IRQ status 0 = Jack Detect (Right) IRQ not set 1 = Jack Detect (Right) IRQ set
	11	CODEC_SEQ_END_EINT	0b	CODEC softstart or shutdown status 0 = CODEC sequence normal 1 = CODEC softstart or shutdown sequence completed
	10	CDEL_TO_EINT	0b	CDELAY IRQ status 0 = CDELAY normal 1 = Reset Delay Timer was triggered by 500ms timeout OR invalid CDELAY capacitance caused CDELAY error.
	9	CHIP_GT150_EINT	0b	Temperature Level 2 IRQ status 0 = 150°C threshold not exceeded 1 = 150°C threshold exceeded
	8	CHIP_GT115_EINT	0b	Temperature Level 1 IRQ status 0 = 115°C threshold not exceeded 1 = 115°C threshold exceeded
	7	LINE_CMP_EINT	0b	Battery Comparator IRQ status 0 = Battery Comparator normal 1 = Battery Comparator undervoltage
	6	UVLO_EINT	0b	UVLO IRQ status 0 = UVLO disabled 1 = UVLO enabled
	5	DC2_UV_EINT	0b	DC2 Converter IRQ status 0 = DC2 voltage normal 1 = DC2 undervoltage detected

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4	DC1_UV_EINT	0b	DC1 Converter IRQ status 0 = DC1 voltage normal 1 = DC1 undervoltage detected
	3	LDO4_UV_EINT	0b	LDO4 Regulator IRQ status 0 = LDO4 voltage normal 1 = LDO4 undervoltage detected
	2	LDO3_UV_EINT	0b	LDO3 Regulator IRQ status 0 = LDO3 voltage normal 1 = LDO3 undervoltage detected
	1	LDO2_UV_EINT	0b	LDO2 Regulator IRQ status 0 = LDO2 voltage normal 1 = LDO2 undervoltage detected
	0	LDO1_UV_EINT	0b	LDO1 Regulator IRQ status 0 = LDO1 voltage normal 1 = LDO1 undervoltage detected
R80 (50h)	15	IM_MICD_CINT	0b	MIC Current Detect IRQ enable 0 = Not masked 1 = Masked
	14	IM_MICSCD_CINT	0b	MIC Short Circuit IRQ enable 0 = Not masked 1 = Masked
	13	IM_JDL_CINT	0b	Jack Detect (Left) IRQ enable 0 = Not masked 1 = Masked
	12	IM_JDR_CINT	0b	Jack Detect (Right) IRQ enable 0 = Not masked 1 = Masked
	11	IM_CODEC_SEQ_END_EINT	0b	CODEC softstart or shutdown IRQ enable 0 = Not masked 1 = Masked
	10	IM_CDEL_TO_EINT	0b	CDELAY IRQ enable 0 = Not masked 1 = Masked
	9	IM_CHIP_GT150_EINT	0b	Temperature Level 2 IRQ enable 0 = Not masked 1 = Masked
	8	IM_CHIP_GT115_EINT	0b	Temperature Level 1 IRQ enable 0 = Not masked 1 = Masked
	7	IM_LINE_CMP_EINT	0b	Battery Comparator IRQ enable 0 = Not masked 1 = Masked
	6	IM_UVLO_EINT	0b	UVLO IRQ enable 0 = Not masked 1 = Masked
	5	IM_DC2_UV_EINT	0b	DC2 Converter IRQ enable 0 = Not masked 1 = Masked
	4	IM_DC1_UV_EINT	0b	DC1 Converter IRQ enable 0 = Not masked 1 = Masked

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	IM_LDO4_UV_EINT	0b	LDO4 Regulator IRQ enable 0 = Not masked 1 = Masked
	2	IM_LDO3_UV_EINT	0b	LDO3 Regulator IRQ enable 0 = Not masked 1 = Masked
	1	IM_LDO2_UV_EINT	0b	LDO2 Regulator IRQ enable 0 = Not masked 1 = Masked
	0	IM_LDO1_UV_EINT	0b	LDO1 Regulator IRQ enable 0 = Not masked 1 = Masked
R81 (51h)	15	MICD_LVL	0b	MIC Current Detect IRQ level 0 = MIC Current not detected 1 = MIC Current detected
	14	MICSCD_LVL	0b	MIC Short Circuit IRQ level 0 = MIC Short Circuit not detected 1 = MIC Short Circuit detected
	13	JDL_LVL	0b	Jack Detect (Left) IRQ level 0 = Jack Detect (Left) not detected 1 = Jack Detect (Left) detected
	12	JDR_LVL	0b	Jack Detect (Right) IRQ level 0 = Jack Detect (Right) not detected 1 = Jack Detect (Right) detected
	11	CODEC_SEQ_END_LVL	0b	CODEC softstart or shutdown IRQ level 0 = CODEC sequence normal 1 = CODEC softstart or shutdown sequence completed
	9	CHIP_GT150_LVL	0b	Temperature Level 2 IRQ level 0 = 150°C threshold not exceeded 1 = 150°C threshold exceeded
	8	CHIP_GT115_LVL	0b	Temperature Level 1 IRQ level 0 = 115°C threshold not exceeded 1 = 115°C threshold exceeded
	7	LINE_CMP_LVL	0b	Battery Comparator IRQ level 0 = Battery Comparator normal 1 = Battery Comparator undervoltage
	6	UVLO_LVL	0b	UVLO IRQ level 0 = UVLO disabled 1 = UVLO enabled
	5	DC2_UV_LVL	0b	DC2 Converter IRQ level 0 = DC2 voltage normal 1 = DC2 undervoltage detected
	4	DC1_UV_LVL	0b	DC1 Converter IRQ level 0 = DC1 voltage normal 1 = DC1 undervoltage detected
	3	LDO4_UV_LVL	0b	LDO4 Regulator IRQ level 0 = LDO4 voltage normal 1 = LDO4 undervoltage detected
	2	LDO3_UV_LVL	0b	LDO3 Regulator IRQ level 0 = LDO3 voltage normal 1 = LDO3 undervoltage detected
	1	LDO2_UV_LVL	0b	LDO2 Regulator IRQ level

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				0 = LDO2 voltage normal 1 = LDO2 undervoltage detected
	0	LDO1_UV_LVL	0b	LDO1 Regulator IRQ level 0 = LDO1 voltage normal 1 = LDO1 undervoltage detected

Table 99 Interrupt Event Control

TEMPERATURE SENSING

The WM8400 incorporates a thermal sensor which can be used to prevent damage or hazards in the event of safe operating temperatures being exceeded. The register fields CHIP_GT115_ERRACT and CHIP_GT150_ERRACT determine what action is taken at the temperature thresholds 115°C and 150°C respectively. The available options are to signal an Interrupt (IRQ) event only, or to additionally initiate device shutdown. It is recommended to shut down the WM8400 as soon as possible if the upper threshold is reached.

If an IRQ event arises from these functions, this causes the NIRQ pin to output a logic low level (referenced to the MBVDD power domain).

The thermal protection of the audio components of the WM8400 may be controlled independently. If the device temperature reaches approximately 150ºC and the thermal shutdown circuit is enabled (TSHUT_ENA = 1; TSHUT_OPDIS = 1) the speaker and headphone amplifiers (LOUT, ROUT, SPKP, SPKN, OUT3 and OUT4) will be disabled.

Note that TSHUT_ENA must be set to 1 to enable the temperature sensor when using the TSHUT_OPDIS thermal shutdown function. The output of this temperature sensor can also be output to the GPIO pins.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h)	14	TSHUT_ENA (rw)	1b	Audio Components Thermal Sensor Enable 0 = Thermal sensor disabled 1 = Thermal sensor enabled
	13	TSHUT_OPDIS (rw)	1b	Audio Components Thermal Shutdown Enable (Requires thermal sensor to be enabled) 0 = Thermal shutdown disabled 1 = Thermal shutdown enabled
R78 (4Eh)	9	CHIP_GT150_ERRACT	1b	Device Overtemperature 2 Action 0 = UVLO generates IRQ only 1 = UVLO generates IRQ and initiates device shutdown
	8	CHIP_GT115_ERRACT	0b	Device Overtemperature 1 Action 0 = UVLO generates IRQ only 1 = UVLO generates IRQ and initiates device shutdown

Table 100 Thermal Shutdown

When the speaker driver is operating in class AB mode the internal power dissipation of the WM8400 is likely to be significantly higher than when operating in class D mode.

Note: To prevent potential pops and clicks THSUT_ENA and TSHUT_OPDIS need to be configured while the speaker and headphone outputs are off, i.e. LOUT_ENA, ROUT_ENA, OUT3_ENA, OUT4_ENA and SPK_ENA are 0 (see also Table 77).

DEVICE SHUTDOWN

The WM8400 can be programmed to initiate a device shutdown in response to selected overtemperature or undervoltage conditions. These conditions are referenced in Table 93, Table 97 and Table 100. Setting the applicable _ERRACT register bits detailed in these tables will cause a device shutdown to be initiated if the corresponding condition occurs.

A device shutdown is performed in the event of a CDELAY error condition (see "Power Sequencing and Control"). A CDELAY error condition will occur if the CDELAY pin is shorted to GND or if an unsuitable CDELAY capacitor is connected. Suitable CDELAY components are detailed in the "Applications Information" section.

The WM8400 will also initiate a device shutdown in response to a logic low level on the NPDN pin (referenced to the HBVDD power domain) or by setting the Register bit CHIP_SOFTSD. Either of these events will command the WM8400 to execute a 'soft shutdown', where the CODEC and Power Management functions are disabled in a controlled manner, avoiding audio pops and other undesirable effects. The definition of CHIP_SOFTSD is provided in Table 101.

Following a Shutdown caused by setting CHIP_SOFTSD, the chip will ignore the status of the NPDN pin until it has been restored to a logic low level. Therefore, re-starting the chip following a CHIP_SOFTST requires NPDN to be toggled low and then high again.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R76 (4Ch)	13	CHIP_SOFTSD	0b	Chip Soft Shutdown Sequence 0 = Disabled 1 = Enabled

Table 101 Chip Soft Shutdown

When a Shutdown has been initiated, the cause of this shutdown can be read from Register R82 (52h), as described in Table 102. Note that register read/write operations are still supported following shutdown, provided that NPDN remains asserted.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R82 (52h)	13	SDR_CHIP_SOFTSD	0b	CHIP_SOFTSD shutdown status 0 = Disabled 1 = Enabled
	11	SDR_NPDN	0b	NPDN shutdown status 0 = Disabled 1 = Enabled
	10	SDR_CDEL_TO	0b	CDELAY time shutdown status 0 = Disabled 1 = Enabled
	9	SDR_CHIP_GT150	0b	Temperature Level 2 shutdown status 0 = Disabled 1 = Enabled
	8	SDR_CHIP_GT115	0b	Temperature Level 1 shutdown status 0 = Disabled 1 = Enabled
	7	SDR_LINE_CMP	0b	Battery Comparator shutdown status 0 = Disabled 1 = Enabled
	6	SDR_UVLO	0b	UVLO shutdown status 0 = Disabled 1 = Enabled
	5	SDR_DC2_UV	0b	DC2 Undervoltage shutdown status 0 = Disabled 1 = Enabled
	4	SDR_DC1_UV	0b	DC1 Undervoltage shutdown status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				0 = Disabled 1 = Enabled
	3	SDR_LDO4_UV	0b	LDO4 Undervoltage shutdown status 0 = Disabled 1 = Enabled
	2	SDR_LDO3_UV	0b	LDO3 Undervoltage shutdown status 0 = Disabled 1 = Enabled
	1	SDR_LDO2_UV	0b	LDO2 Undervoltage shutdown status 0 = Disabled 1 = Enabled
	0	SDR_LDO1_UV	0b	LDO1 Undervoltage shutdown status 0 = Disabled 1 = Enabled

Table 102 Shutdown Register

CHIP RESET

HARDWARE RESET

A full hardware reset of the WM8400 can be implemented by powering down the device. Setting a logic low level on NPDN (referenced to the HBVDD power domain) will initiate 'soft shutdown' sequence, where the CODEC and Power Management functions are disabled in a controlled manner, avoiding audio pops and other undesirable effects. Following this reset, the device may be re-started by asserting NPDN - see "Enabling the Device".

SOFTWARE RESET

CHIP RESET AND ID

The Device ID can be read back from Register 0. Writing to this register will reset the device. Resetting the device will result in all DC-DC Converters and LDO Regulators being switched off and will reset the NRST output to logic low level. Register read/wire operations are supported following a software reset, but a complete re-starting of the device requires NPDN to be toggled.

Register 1 contains the Chip Revision ID

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Reset / ID	15:0	SW_RESET/CHIP_ID [15:0] (rr)	6172h	Writing to this register resets all registers to their default state. Reading from this register will indicate Device ID 6172h.
R1 (01h) ID	14:12	CHIP_REV [2:0] (rr)	000b	Reading from this register will indicate the Revision ID.

Table 103 Chip Reset and ID

REGISTER MAP

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	00h	Reset/ID (SC)	SW_RESET/CHIP_ID[15:0]															
1	01h	ID	0	CHIP_REV[2:0]			0	0	0	0	CUST_ID[7:0]							
2	02h	Power Management (1)	CODEC_ENA	SYSCLK_ENA	SPK_MIX_ENA	SPK_ENA	OUT3_ENA	OUT4_ENA	LOUT_ENA	ROUT_ENA	0	0	0	MIC1BIAS_ENA	0	VMID_MODE[1:0]		VREF_ENA
3	03h	Power Management (2)	FLL_ENA	TSHUT_ENA	TSHUT_OPDIS	0	OPCLK_ENA	0	AINL_ENA	AINR_ENA	LIN34_ENA	LIN12_ENA	RIN34_ENA	RIN12_ENA	0	0	ADCL_ENA	ADCR_ENA
4	04h	Power Management (3)	0	0	LON_ENA	LOP_ENA	RON_ENA	ROP_ENA	0	0	LOPGA_ENA	ROPGA_ENA	LOMIX_ENA	ROMIX_ENA	0	0	DACL_ENA	DACR_ENA
5	05h	Audio Interface (1)	AIFADCL_SRC	AIFADCR_SRC	AIFADC_TDM	AIFADC_TDM_CHAN	0	0	0	AIF_BCLK_INV	AIF_LRCLK_INV	AIF_WL[1:0]		AIF_FMT[1:0]		0	0	0
6	06h	Audio Interface (2)	DACL_SRC	DACR_SRC	AIFDAC_TDM	AIFDAC_TDM_CHAN	DAC_BOOST[1:0]		0	0	0	0	0	DAC_COMP	DAC_COMPMODE	ADC_COMP	ADC_COMPMODE	LOOPBACK
7	07h	Clocking (1)	TOCLK_RATE	TOCLK_ENA	0	OPCLKDIV[3:0]				DCLKDIV[2:0]			0	BCLK_DIV[3:0]				0
8	08h	Clocking (2)	MCLK_SRC	SYSCLK_SRC	CLK_FORCE	MCLK_DIV[1:0]		MCLK_INV	0	0	ADC_CLKDIV[2:0]			DAC_CLKDIV[2:0]			0	0
9	09h	Audio Interface (3)	AIF_MSTR1	AIF_MSTR2	AIF_SEL	0	ADCLRC_DIR	ADCLRC_RATE[10:0]										
10	0Ah	Audio Interface (4)	ALRCGPIO1	ALRCBGPIO6	AIF_TRIS	0	DACLRC_DIR	DACLRC_RATE[10:0]										
11	0Bh	DAC CTRL	0	0	DAC_SDMCLK_RATE	0	0	AIF_LRCLKRATE	DAC_MONO	DAC_SB_FILT	DAC_MUTERATE	DAC_MUTEMODE	DEEMP[1:0]		0	DAC_MUTE	DACL_DATINV	DACR_DATINV
12	0Ch	Left DAC Digital Volume	0	0	0	0	0	0	0	DAC_VU	DACL_VOL[7:0]							
13	0Dh	Right DAC Digital Volume	0	0	0	0	0	0	0	DAC_VU	DACR_VOL[7:0]							
14	0eH	Digital Side Tone	0	0	0	ADCL_DAC_SVOL[3:0]				ADCR_DAC_SVOL[3:0]				0	ADC_TO_DACL[1:0]		ADC_TO_DACR[1:0]	
15	0Fh	ADC CTRL	0	0	0	0	0	0	0	ADC_HPF_ENA	0	ADC_HPF_CUT[1:0]		0	0	0	ADCL_DATINV	ADCR_DATINV
16	10h	Left ADC Digital Volume	0	0	0	0	0	0	0	ADC_VU	ADCL_VOL[7:0]							
17	11h	Right ADC Digital Volume	0	0	0	0	0	0	0	ADC_VU	ADCR_VOL[7:0]							
18	12h	GPIO CTRL 1	0	0	0	IRQ	TEMPOK	MIC1SHRT	MIC1DET	FLL_LCK	GPIO_STATUS[7:0]							
19	13h	GPIO1 & GPIO2	GPIO2_DEB_ENA	GPIO2_IRQ_ENA	GPIO2_PU	GPIO2_PD	GPIO2_SEL[3:0]				GPIO1_DEB_ENA	GPIO1_IRQ_ENA	GPIO1_PU	GPIO1_PD	GPIO1_SEL[3:0]			
20	14h	GPIO3 & GPIO4	GPIO4_DEB_ENA	GPIO4_IRQ_ENA	GPIO4_PU	GPIO4_PD	GPIO4_SEL[3:0]				GPIO3_DEB_ENA	GPIO3_IRQ_ENA	GPIO3_PU	GPIO3_PD	GPIO3_SEL[3:0]			
21	15h	GPIO5 & GPIO6	GPIO6_DEB_ENA	GPIO6_IRQ_ENA	GPIO6_PU	GPIO6_PD	GPIO6_SEL[3:0]				GPIO5_DEB_ENA	GPIO5_IRQ_ENA	GPIO5_PU	GPIO5_PD	GPIO5_SEL[3:0]			
22	16h	GPIOCTRL 2	1	0	0	0	TEMPOK_IRQ_ENA	MIC1SHRT_IRQ_ENA	MIC1DET_IRQ_ENA	FLL_LCK_IRQ_ENA	GPI8_DEB_ENA	GPI8_IRQ_ENA	0	GPI8_ENA	GPI7_DEB_ENA	GPI7_IRQ_ENA	0	GPI7_ENA
23	17h	GPIO_POL	0	0	0	IRQ_INV	TEMPOK_POL	MIC1SHRT_POL	MIC1DET_POL	FLL_LCK_POL	GPIO_POL[7:0]							
24	18h	Left Line Input 1&2 Volume	0	0	0	0	0	0	0	IPVU[0]	LI12MUTE	LI12ZC	0	LIN12VOL[4:0]				
25	19h	Left Line Input 3&4 Volume	0	0	0	0	0	0	0	IPVU[1]	LI34MUTE	LI34ZC	0	LIN34VOL[4:0]				
26	1Ah	Right Line Input 1&2 Volume	0	0	0	0	0	0	0	IPVU[2]	RI12MUTE	RI12ZC	0	RIN12VOL[4:0]				
27	1Bh	Right Line Input 3&4 Volume	0	0	0	0	0	0	0	IPVU[3]	RI34MUTE	RI34ZC	0	RIN34VOL[4:0]				
28	1Ch	Left Output Volume	0	0	0	0	0	0	0	OPVU[0]	LOZC	LOUTVOL[6:0]						
29	1Dh	Right Output Volume	0	0	0	0	0	0	0	OPVU[1]	ROZC	ROUTVOL[6:0]						

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
30	1Eh	Line Outputs Volume	0	0	0	0	0	0	0	0	0	LONMUTE	LOPMUTE	LOATTN	0	RONMUTE	ROPMUTE	ROATTN
31	1Fh	Out3/4 Volume	0	0	0	0	0	0	0	0	0	0	OUT3MUTE	OUT3ATTN	0	0	OUT4MUTE	OUT4ATTN
32	20h	Left OPGA Volume	0	0	0	0	0	0	0	OPVU[2]	LOPGAZC	LOPGAVOL[6:0]						
33	21h	Right OPGA Volume	0	0	0	0	0	0	0	OPVU[3]	ROPGAZC	ROPGAVOL[6:0]						
34	22h	Speaker Volume	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SPKATTN[1:0]	
35	23h	ClassD1	0	0	0	0	0	0	0	CDMODE	CLASSD_CLK_SEL	0	0	0	0	0	1	1
36	24h	ClassD2	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
37	25h	ClassD3	0	0	0	0	0	0	0	1	0	0	DCGAIN[2:0]			ACGAIN[2:0]		
38	26h	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
39	27h	Input Mixer1	0	0	0	0	0	0	0	0	0	0	0	0	AINLMODE[1:0]		AINRMODE[1:0]	
40	28h	Input Mixer2	0	0	0	0	0	0	0	0	LMP4	LMN3	LMP2	LMN1	RMP4	RMN3	RMP2	RMN1
41	29h	Input Mixer3	0	0	0	0	0	0	0	L34MNB	L34MNBST	0	L12MNB	L12MNBST	0	LDBVOL[2:0]		
42	2Ah	Input Mixer4	0	0	0	0	0	0	0	R34MNB	R34MNBST	0	R12MNB	R12MNBST	0	RDBVOL[2:0]		
43	2Bh	Input Mixer5	0	0	0	0	0	0	0	LI2BVOL[2:0]			LR4BVOL[2:0]			LL4BVOL[2:0]		
44	2Ch	Input Mixer6	0	0	0	0	0	0	0	RI2BVOL[2:0]			RL4BVOL[2:0]			RR4BVOL[2:0]		
45	2Dh	Output Mixer1	0	0	0	0	0	0	0	0	LRBLO	LLBLO	LRI3LO	LLI3LO	LR12LO	LL12LO	0	LDLO
46	2Eh	Output Mixer2	0	0	0	0	0	0	0	0	RLBRO	RRBRO	RLI3RO	RRI3RO	RL12RO	RR12RO	0	RDRO
47	2Fh	Output Mixer3	0	0	0	0	0	0	0	LLI3LOVOL[2:0]			LR12LOVOL[2:0]			LL12LOVOL[2:0]		
48	30h	Output Mixer4	0	0	0	0	0	0	0	RRI3ROVOL[2:0]			RL12ROVOL[2:0]			RR12ROVOL[2:0]		
49	31h	Output Mixer5	0	0	0	0	0	0	0	LRI3LOVOL[2:0]			LRBLOVOL[2:0]			LLBLOVOL[2:0]		
50	32h	Output Mixer6	0	0	0	0	0	0	0	RLI3ROVOL[2:0]			RLBROVOL[2:0]			RRBROVOL[2:0]		
51	33h	Out3/4 Mixer	0	0	0	0	0	0	0	VSEL[1:0]		0	LI4O3	LPGAO3	0	0	RI4O4	RPGAO4
52	34h	Line Mixer1	0	0	0	0	0	0	0	0	0	LLOPGALON	LROPGALON	LOPLON	0	LR12LOP	LL12LOP	LLOPGALOP
53	35h	Line Mixer2	0	0	0	0	0	0	0	0	0	RROPGARON	RLOPGARON	ROPRON	0	RL12ROP	RR12ROP	RROPGAROP
54	36h	Speaker Mixer	0	0	0	0	0	0	0	0	LB2SPK	RB2SPK	LI2SPK	RI2SPK	LOPGASPK	ROPGASPK	LDSPK	RDSPK
55	37h	Additional Control	0	0	0	0	0	0	0	0	0	0	0	SPARE2[3:0]				VROI
56	38h	AntiPOP1	0	0	0	0	0	0	0	0	0	0	DIS_LLINE	DIS_RLINE	DIS_OUT3	DIS_OUT4	DIS_LOUT	DIS_ROUT
57	39h	AntiPOP2	0	0	0	0	0	0	0	0	0	SOFTST	SOFTSLEEPEN	QUARTEBIASEN	BUFIOEN	BUFDCOPEN	POBCTRL	VMIDTOG
58	3Ah	MICBIAS	0	0	0	0	0	0	0	0	MCDSCTH[1:0]		MCDTHR[2:0]			MCD	0	MBSEL
59	3Bh	CODEC Spare	SPARE_REG[15:0]															

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
60	3C	FLL Control 1	0	0	0	FLL_REF_FREQ	FLL_CLK_SRC[1:0]		FLL_FRAC	FLL_OSC_ENA	FLL_CTRL_RATE[2:0]			FLL_FRATIO[4:0]				
61	3D	FLL Control 2	FLL_K[15:0]															
62	3E	FLL Control 3	0	0	0	0	0	0	FLL_N[9:0]									
63	3F	FLL Control 4	0	0	0	0	0	0	0	0	0	FLL_TRK_GAIN[3:0]				FLL_OUTDIV[2:0]		
64	40	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
65	41	LDO 1 Control	LDO1_ENA	LDO1_SWI	0	LDO1_OPFLT	LDO1_ERRACT	LDO1_HIB_MODE	LDO1_VIMG[4:0]					LDO1_VSEL[4:0]				
66	42	LDO 2 Control	LDO2_ENA	LDO2_SWI	0	LDO2_OPFLT	LDO2_ERRACT	LDO2_HIB_MODE	LDO2_VIMG[4:0]					LDO2_VSEL[4:0]				
67	43	LDO 3 Control	LDO3_ENA	LDO3_SWI	0	LDO3_OPFLT	LDO3_ERRACT	LDO3_HIB_MODE	LDO3_VIMG[4:0]					LDO3_VSEL[4:0]				
68	44	LDO 4 Control	LDO4_ENA	LDO4_SWI	0	LDO4_OPFLT	LDO4_ERRACT	LDO4_HIB_MODE	LDO4_VIMG[4:0]					LDO4_VSEL[4:0]				
69	45	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
70	46	DCDC1 Control 1	DC1_ENA	DC1_ACTIVE	DC1_SLEEP	DC1_OPFLT	DC1_ERRACT	DC1_HIB_MODE	DC1_SOFTST[1:0]		DC1_OV_PROT	DC1_VSEL[6:0]						
71	47	DCDC1 Control 2	DC1_CAP[1:0]		DC1_FRC_PWM	0	0	0	DC1_STBY_LIM[1:0]		DC1_ACT_LIM	DC1_VIMG[6:0]						
72	48	DCDC2 Control 1	DC2_ENA	DC2_ACTIVE	DC2_SLEEP	DC2_OPFLT	DC2_ERRACT	DC2_HIB_MODE	DC2_SOFTST[1:0]		DC2_OV_PROT	DC2_VSEL[6:0]						
73	49	DCDC2 Control 2	DC2_CAP[1:0]		DC2_FRC_PWM	0	0	0	DC2_STBY_LIM[1:0]		DC2_ACT_LIM	DC2_VIMG[6:0]						
74	4A	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
75	4B	Interface	0	0	0	0	0	0	0	0	0	0	0	0	AUTOINC	ARA_ENA	SPI_CFG	0
76	4C	PM GENERAL	CODEC_SOFTST	CODEC_SOFTSD	CHIP_SOFTSD	0	0	0	0	0	0	0	0	0	DSLEEP1_POL	DSLEEP2_POL	PWR_STATE[1:0]	
77	4D	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
78	4E	PM Shutdown Control	0	0	0	0	0	0	CHIP_GT150_ERRACT	CHIP_GT115_ERRACT	LINE_CMP_ERRACT	UVLO_ERRACT	0	0	0	0	0	0
79	4F	Interrupt Status 1	MICD_CINT	MICSCD_CINT	JDL_CINT	JDR_CINT	CODEC_SEQ_END_EINT	CDEL_TO_EINT	CHIP_GT150_EINT	CHIP_GT115_EINT	LINE_CMP_EINT	UVLO_EINT	DC2_UV_EINT	DC1_UV_EINT	LDO4_UV_EINT	LDO3_UV_EINT	LDO2_UV_EINT	LDO1_UV_EINT
80	50	Interrupt Status 1 Mask	IM_MICD_CINT	IM_MICSCD_CINT	IM_JDL_CINT	IM_JDR_CINT	IM_CODEC_SEQ_END_EINT	IM_CDEL_TO_EINT	IM_CHIP_GT150_EINT	IM_CHIP_GT115_EINT	IM_LINE_CMP_EINT	IM_UVLO_EINT	IM_DC2_UV_EINT	IM_DC1_UV_EINT	IM_LDO4_UV_EINT	IM_LDO3_UV_EINT	IM_LDO2_UV_EINT	IM_LDO1_UV_EINT
81	51	Interrupt Levels	MICD_LVL	MICSCD_LVL	JDL_LVL	JDR_LVL	CODEC_SEQ_END_LVL	0	CHIP_GT150_LVL	CHIP_GT115_LVL	LINE_CMP_LVL	UVLO_LVL	DC2_UV_LVL	DC1_UV_LVL	LDO4_UV_LVL	LDO3_UV_LVL	LDO2_UV_LVL	LDO1_UV_LVL
82	52	Shutdown Reason	0	0	SDR_CHIP_SOFTSD	0	SDR_NPDN	SDR_CDEL_TO	SDR_CHIP_GT150	SDR_CHIP_GT115	SDR_LINE_CMP	SDR_UVLO	SDR_DC2_UV	SDR_DC1_UV	SDR_LDO4_UV	SDR_LDO3_UV	SDR_LDO2_UV	SDR_LDO1_UV
83	53	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
84	54	Line Circuits	0	0	0	0	0	0	0	0	LINE_CMP_VTHI[3:0]				LINE_CMP_VTHD[3:0]			

REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Reset / ID	15:0	SW_RESET_CHIP_ID [15:0] (rr)	6172h	Writing to this register resets all registers to their default state. Reading from this register will indicate Device ID 6172h.
R1 (01h) ID	15		0b	Reserved - Do Not Change
	14:12	CHIP_REV [2:0] (rr)	000b	Reading from this register will indicate the Revision ID.
	11:0		000h	Reserved - Do Not Change
R2 (02h) Power Management (1)	15	CODEC_ENA (rw)	0b	Master CODEC enable bit. 0 = CODEC registers held in reset 1 = CODEC registers operate normally
	14	SYSCLK_ENA (rw)	0b	SYSCLK enable 0 = disabled 1 = enabled
	13	SPK_MIX_ENA (rw)	0b	Speaker Mixer Enable 0 = disabled 1 = enabled
	12	SPK_ENA (rw)	0b	Speaker Output Enable 0 = disabled 1 = enabled
	11	OUT3_ENA (rw)	0b	OUT3 and OUT3MIX Enable 0 = disabled 1 = enabled
	10	OUT4_ENA (rw)	0b	OUT4 and OUT4MIX Enable 0 = disabled 1 = enabled
	9	LOUT_ENA (rw)	0b	LOUT (Left Headphone Output) Enable 0 = disabled 1 = enabled
	8	ROUT_ENA (rw)	0b	ROUT (Right Headphone Output) Enable 0 = disabled 1 = enabled
	7:5		000b	Reserved - Do Not Change
	4	MIC1BIAS_ENA (rw)	0b	MICBIAS Enable 0 = OFF (high impedance output) 1 = ON
	3		0b	Reserved - Do Not Change
	2:1	VMID_MODE [1:0] (rw)	00b	Vmid Divider Enable and Select 00 = Vmid disabled (for OFF mode) 01 = 2 x 50kΩ divider (Normal mode) 10 = 2 x 300kΩ divider (Standby mode) 11 = 2 x 6.8kΩ divider (for fast start-up)
	0	VREF_ENA (rw)	0b	VREF Enable (Bias for all analogue functions) 0 = VREF bias disabled 1 = VREF bias enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R03 (03h) Power Management (2)	15	FLL_ENA (rw)	0b	FLL Enable 0 = disabled 1 = enabled
	14	TSHUT_ENA (rw)	1b	Audio Components Thermal Sensor Enable 0 = Thermal sensor disabled 1 = Thermal sensor enabled
	13	TSHUT_OPDIS (rw)	1b	Audio Components Thermal Shutdown Enable (Requires thermal sensor to be enabled) 0 = Thermal shutdown disabled 1 = Thermal shutdown enabled
	12		0b	Reserved - Do Not Change
	11	OPCLK_ENA (rw)	0b	GPIO Clock Output Enable 0 = disabled 1 = enabled
	10		0b	Reserved - Do Not Change
	9	AINL_ENA (rw)	0b	Left Input Path Enable (Enables AINLMUX, INMIXL, DIFFINL and RXVOICE input to AINLMUX) 0 = disabled 1 = enabled
	8	AINR_ENA (rw)	0b	Right Input Path Enable (Enables AINRMUX, INMIXR, DIFFINR and RXVOICE input to AINRMUX) 0 = disabled 1 = enabled
	7	LIN34_ENA (rw)	0b	LIN34 Input PGA Enable 0 = disabled 1 = enabled
	6	LIN12_ENA (rw)	0b	LIN12 Input PGA Enable 0 = disabled 1 = enabled
	5	RIN34_ENA (rw)	0b	RIN34 Input PGA Enable 0 = disabled 1 = enabled
	4	RIN12_ENA (rw)	0b	RIN12 Input PGA Enable 0 = disabled 1 = enabled
	3:2		00b	Reserved - Do Not Change
	1	ADCL_ENA (rw)	0b	Left ADC Enable 0 = disabled 1 = enabled
	0	ADCR_ENA (rw)	0b	Right ADC Enable 0 = disabled 1 = enabled
R04 (04h) Power Management (3)	15:14		00b	Reserved - Do Not Change
	13	LON_ENA (rw)	0b	LON Line Out and LONMIX Enable 0 = disabled 1 = enabled
	12	LOP_ENA (rw)	0b	LOP Line Out and LOPMIX Enable 0 = disabled 1 = enabled
	11	RON_ENA (rw)	0b	RON Line Out and RONMIX Enable 0 = disabled 1 = enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10	ROP_ENA (rw)	0b	ROP Line Out and ROPMIX Enable 0 = disabled 1 = enabled
	9:8		00b	Reserved - Do Not Change
	7	LOPGA_ENA (rw)	0b	LOPGA Left Volume Control Enable 0 = disabled 1 = enabled
	6	ROPGA_ENA (rw)	0b	ROPGA Right Volume Control Enable 0 = disabled 1 = enabled
	5	LOMIX_ENA (rw)	0b	LOMIX Left Output Mixer Enable 0 = disabled 1 = enabled
	4	ROMIX_ENA (rw)	0b	ROMIX Right Output Mixer Enable 0 = disabled 1 = enabled
	3:2		00b	Reserved - Do Not Change
	1	DACL_ENA (rw)	0b	Left DAC Enable 0 = disabled 1 = enabled
	0	DACR_ENA (rw)	0b	Right DAC Enable 0 = disabled 1 = enabled
R05 (05h) Audio Interface (1)	15	AIFADCL_SRC	0b	Left Digital Audio channel source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel
	14	AIFADCR_SRC	1b	Right Digital Audio channel source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
	13	AIFADC_TDM	0b	ADC TDM Enable 0 = Normal ADCDAT operation 1 = TDM enabled on ADCDAT
	12	AIFADC_TDM_CHAN	0b	ADCDAT TDM Channel Select 0 = ADCDAT outputs data on slot 0 1 = ADCDAT output data on slot 1
	11:9		0b	Reserved - Do Not Change
	8	AIF_BCLK_INV	0b	BCLK Invert 0 = BCLK not inverted 1 = BCLK inverted
	7	AIF_LRCLK_INV	0b	Right, left and I^2S modes – LRCLK polarity 0 = normal LRCLK polarity 1 = invert LRCLK polarity
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)
	6:5	AIF_WL [1:0]	10b	Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits Note - see “Companding” for the selection of 8-bit mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4:3	AIF_FMT [1:0]	10b	Digital Audio Interface Format 00 = Right justified 01 = Left justified 10 = I^2S Format 11 = DSP Mode
	2:0		0b	Reserved - Do Not Change
R06 (06h) Audio Interface (2)	15	DACL_SRC	0b	Left DAC Data Source Select 0 = Left DAC outputs left channel data 1 = Left DAC outputs right channel data
	14	DACR_SRC	1b	Right DAC Data Source Select 0 = Right DAC outputs left channel data 1 = Right DAC outputs right channel data
	13	AIFDAC_TDM	0b	DAC TDM Enable 0 = Normal DACDAT operation 1 = TDM enabled on DACDAT
	12	AIFDAC_TDM_CHAN	0b	DACDAT TDM Channel Select 0 = DACDAT data input on slot 0 1 = DACDAT data input on slot 1
	11:10	DAC_BOOST [1:0]	00b	DAC Input Volume Boost 00 = 0dB 01 = +6dB (Input data must not exceed -6dBFS) 10 = +12dB (Input data must not exceed -12dBFS) 11 = +18dB (Input data must not exceed -18dBFS)
	9:5			Reserved - Do Not Change
	4	DAC_COMP	0b	DAC Companding Enable 0 = disabled 1 = enabled
	3	DAC_COMPMODE	0b	DAC Companding Type 0 = µ-law 1 = A-law
	2	ADC_COMP	0b	ADC Companding Enable 0 = disabled 1 = enabled
	1	ADC_COMPMODE	0b	ADC Companding Type 0 = µ-law 1 = A-law
	0	LOOPBACK	0b	Digital Loopback Function 0 = No loopback 1 = Loopback enabled (ADC data output is directly input to DAC data input). Note: ADC and DAC left/right clocks must be set to the same pin when using LOOPBACK function (ALRCGPIO1=1)
R07 (07h) Clocking (1)	15	TOCLK_RATE	0b	Timeout Clock Rate (Selects clock to be used for volume update timeout and GPIO input de-bounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)
	14	TOCLK_ENA	0b	Timeout Clock Enable (This clock is required for volume update timeout and GPIO input de-bounce) 0 = disabled 1 = enabled
	13			Reserved - Do Not Change

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	12:9	OPCLKDIV [3:0]	0000b	GPIO Output Clock Divider 0000 = SYSCLK 0001 = SYSCLK / 2 0010 = SYSCLK / 3 0011 = SYSCLK / 4 0100 = SYSCLK / 5.5 0101 = SYSCLK / 6 0110 = SYSCLK / 8 0111 = SYSCLK / 12 1000 = SYSCLK / 16 1001 to 1111 = Reserved
	8:6	DCLKDIV [2:0]	111b	Class D Clock Divider 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16
	5		0b	Reserved - Do Not Change
	4:1	BCLK_DIV [3:0]	0100b	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 = SYSCLK / 32 1110 = SYSCLK / 44 1111 = SYSCLK / 48
	0		0b	Reserved - Do Not Change
R08 (08h) Clocking (2)	15	MCLK_SRC	0b	MCLK Source Select 0 = MCLK pin 1 = GPIO2/MCLK2 pin
	14	SYSCLK_SRC	0b	SYSCLK Source Select 0 = MCLK (or MCLK2 if MCLK_SRC=1) 1 = FLL output
	13	CLK_FORCE	0b	Forces Clock Source Selection 0 = Existing SYSCLK source (MCLK, MCLK2 or FLL output) must be active when changing to a new clock source. 1 = Allows existing MCLK source to be disabled before changing to a new clock source.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	12:11	MCLK_DIV [1:0]	00b	SYSCLK Pre-divider. Clock source (MCLK, MCLK2 or FLL output) will be divided by this value to generate SYSCLK. 00 = Divide SYSCLK by 1 01 = Reserved 10 = Divide SYSCLK by 2 11 = Reserved
	10	MCLK_INV	0b	MCLK Invert 0 = Master clock (MCLK or MCLK2) not inverted 1 = Master clock (MCLK or MCLK2) inverted
	9:8		00b	Reserved - Do Not Change
	7:5	ADC_CLKDIV [2:0]	000b	ADC Sample Rate Divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2.0 011 = SYSCLK / 3.0 100 = SYSCLK / 4.0 101 = SYSCLK / 5.5 110 = SYSCLK / 6.0 111= Reserved
	4:2	DAC_CLKDIV [2:0]	000b	DAC Sample Rate Divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2.0 011 = SYSCLK / 3.0 100 = SYSCLK / 4.0 101 = SYSCLK / 5.5 110 = SYSCLK / 6.0 111= Reserved
	1:0		00b	Reserved - Do Not Change
R09 (09h) Audio Interface (3)	15	AIF_MSTR1	0b	Audio Interface 1 Master Mode Select 0 = Slave mode 1 = Master mode
	14	AIF_MSTR2	0b	Audio Interface 2 Master Mode Select 0 = Slave mode 1 = Master mode
	13	AIF_SEL	0b	Audio Interface Select 0 = Audio interface 1 1 = Audio interface 2 (GPIO3/BCLK2, GPIO4/DACLRC2, GPIO5/DACDAT2)
	12		0b	Reserved - Do Not Change
	11	ADCLRC_DIR	0b	ADCLRC Direction (Forces ADCLRC clock to be output in slave mode) 0 = ADCLRC normal operation 1 = ADCLRC clock output enabled
	10:0	ADCLRC_RATE [10:0]	040h	ADCLRC Rate ADCLRC clock output = BCLK / ADCLRC_RATE Integer (LSB = 1) Valid from 8..2047

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) Audio Interface (4)	15	ALRCGPIO1	0b	ADCLRC/GPIO1 Pin Function Select 0 = ADCLRC pin 1 = GPIO1 pin (ADCLRC connected to DACLRC internally)
	14	ALRCBGPIO6	0b	GPIO6/ADCLRCB Pin Function Select 0 = GPIO6 pin 1 = Inverted ADCLRC clock output
	13	AIF_TRIS	0b	Audio Interface and GPIO Tristate 0 = Audio interface and GPIO pins operate normally 1 = Tristate all audio interface and GPIO pins
	12		0b	Reserved - Do Not Change
	11	DACLRC_DIR	0b	DACLRC Direction (Forces DACLRC clock to be output in slave mode) 0 = DACLRC normal operation 1 = DACLRC clock output enabled
	10:0	DACLRC_RATE [10:0]	040h	DACLRC Rate DACLRC clock output = BCLK / DACLRC_RATE Integer (LSB = 1) Valid from 8..2047
R11 (0Bh) DAC Control	15:14		00b	Reserved - Do Not Change
	13	DAC_SDMCLK_RATE	0b	DAC clocking rate 0 = Normal operation (64fs) 1 = SYSCLK/4
	12:11		00b	Reserved - Do Not Change
	10	AIF_LRCLKRATE	0b	LRCLK Rate 0 = Normal mode (256 * fs) 1 = USB mode (272 * fs)
	9	DAC_MONO	0b	DAC Mono Mix 0 = Stereo 1 = Mono (Mono mix output on enabled DACs)
	8	DAC_SB_FILT	0b	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband mode
	7	DAC_MUTERATE	0b	DAC Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k)
	6	DAC_MUTEMODE	0b	DAC Soft Mute Mode 0 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to change immediately to DACL_VOL and DACR_VOL settings 1 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to ramp up gradually to the DACL_VOL and DACR_VOL settings
	5:4	DEEMP	00b	DAC De-Emphasis Control 00 = De-emphasis disabled 01 = De-emphasis enabled (Optimised for fs=32kHz) 10 = De-emphasis enabled (Optimised for fs=44.1kHz) 11 = De-emphasis enabled (Optimised for fs=48kHz)
	3		0b	Reserved - Do Not Change
	2	DAC_MUTE	1b	DAC Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	DACL_DATINV	0b	Left DAC Invert 0 = Left DAC output not inverted 1 = Left DAC output inverted
	0	DACR_DATINV	0b	Right DAC Invert 0 = Right DAC output not inverted 1 = Right DAC output inverted
R12 (0Ch) Left DAC Digital Volume	15:9		00h	Reserved - Do Not Change
	8	DAC_VU	N/A	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously
	7:0	DACL_VOL [7:0]	1100_0000b (0dB)	Left DAC Digital Volume (See Table 43 for volume settings)
R13 (0Dh) Right DAC Digital Volume	15:9		00h	Reserved - Do Not Change
	8	DAC_VU	N/A	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously
	7:0	DACR_VOL [7:0]	1100_0000b (0dB)	Right DAC Digital Volume (See Table 43 for volume settings)
R14 (0Eh) Digital Sidetone	15:13		000b	Reserved - Do Not Change
	12:9	ADCL_DAC_SVOL [3:0]	0000b	Left Channel Digital Sidetone Volume (See Table 40 for volume range)
	8:5	ADCR_DAC_SVOL [3:0]	0000b	Right Channel Digital Sidetone Volume (See Table 40 for volume range)
	4		0b	Reserved - Do Not Change
	3:2	ADC_TO_DACL [1:0]	00b	Left DAC Digital Sidetone Source 00 = No sidetone 01 = Left ADC 10 = Right ADC 11 = Reserved
	1:0	ADC_TO_DACR [1:0]	00b	Right DAC Digital Sidetone Source 00 = No sidetone 01 = Left ADC 10 = Right ADC 11 = Reserved
R15 (0Fh) ADC Control	15:9		00h	Reserved - Do Not Change
	8	ADC_HPF_ENA	1b	ADC Digital High Pass Filter Enable 0 = disabled 1 = enabled
	7		0b	Reserved - Do Not Change
	6:5	ADC_HPF_CUT [1:0]	00b	ADC Digital High Pass Filter Cut-Off Frequency (fc) 00 = Hi-fi mode (fc=4Hz at fs=48kHz) 01 = Voice mode 1 (fc=127Hz at fs=16kHz) 10 = Voice mode 2 (fc=130Hz at fs=8kHz) 11 = Voice mode 3 (fc=267Hz at fs=8kHz) (Note: fc scales with sample rate. See Table 36 for cut-off frequencies at all supported sample rates)
	4:2		000b	Reserved - Do Not Change
	1	ADCL_DATINV	0b	Left ADC Invert 0 = Left ADC output not inverted 1 = Left ADC output inverted

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	ADCR_DATINV	0b	Right ADC Invert 0 = Right ADC output not inverted 1 = Right ADC output inverted
R16 (10h) Left ADC Digital Volume	15:9		00h	Reserved - Do Not Change
	8	ADC_VU	N/A	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCL_VOL [7:0]	1100_0000b (0dB)	Left ADC Digital Volume (See Table 34 for volume range)
R17 (11h) Right ADC Digital Volume	15:9		00h	Reserved - Do Not Change
	8	ADC_VU	N/A	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volume to be updated simultaneously
	7:0	ADCR_VOL [7:0]	1100_0000b (0dB)	Right ADC Digital Volume (See Table 34 for volume range)
R18 (12h) GPIO Control (1)	15:13		0dB	Reserved - Do Not Change
	12	IRQ (ro)	Read Only	IRQ Readback (Allows polling of IRQ status)
	11	TEMPOK (rr)	Read or Reset	Temperature OK CODEC interrupt 0 = interrupt not set 1 = interrupt is set This bit is latched once set. The TEMPOK_POL bit determines the polarity of the input event to set this bit. It is cleared when a '1' is written.
	10	MIC1SHRT (rr)	Read or Reset	MICBIAS Short Circuit CODEC interrupt 0 = interrupt not set 1 = interrupt is set This bit is latched once set. The MIC1SHRT_POL bit determines the polarity of the input event to set this bit. It is cleared when a '1' is written.
	9	MIC1DET (rr)	Read or Reset	MICBIAS Current Detect CODEC interrupt 0 = interrupt not set 1 = interrupt is set This bit is latched once set. The MIC1DET_POL bit determines the polarity of the input event to set this bit. It is cleared when a '1' is written.
	8	FLL_LCK (rr)	Read or Reset	FLL Lock CODEC interrupt 0 = interrupt not set 1 = interrupt is set This bit is latched once set. The FLL_LCK_POL bit determines the polarity of the input event to set this bit. It is cleared when a '1' is written.
	7:0	GPIO_STATUS [7:0] (rr)	Read or Reset	GPIO and GPI Input Pin Status GPIO_STATUS[7] = GPI8 pin status GPIO_STATUS[6] = GPI7 pin status GPIO_STATUS[5] = GPIO6 pin status GPIO_STATUS[4] = GPIO5 pin status GPIO_STATUS[3] = GPIO4 pin status GPIO_STATUS[2] = GPIO3 pin status GPIO_STATUS[1] = GPIO2 pin status GPIO_STATUS[0] = GPIO1 pin status These bits are latched once set. The GPIO_POL bits determine the polarity of the input event to set these bits. They are cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 (13h) GPIO1 and GPIO2	15	GPIO2_DEB_ENA	0b	GPIO2 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	14	GPIO2_IRQ_ENA	0b	GPIO2 IRQ Enable 0 = disabled 1 = enabled (GPIO2 input will generate IRQ)
	13	GPIO2_PU	0b	GPIO2 Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	12	GPIO2_PD	1b	GPIO2 Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)
	11:8	GPIO2_SEL [3:0]	0000b	GPIO2 Function Select 0000 = Input pin 0001 = Clock output (f=SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = FLL Lock output 0101 = Temperature OK output 0110 = Reserved 0111 = CODEC IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 = MIC Detect 1011 = MIC Short Circuit Detect 1100 to 1111 = Reserved
	7	GPIO1_DEB_ENA	0b	GPIO1 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	6	GPIO1_IRQ_ENA	0b	GPIO1 IRQ Enable 0 = disabled 1 = enabled (GPIO1 input will generate IRQ)
	5	GPIO1_PU	0b	GPIO1 Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	4	GPIO1_PD	0b	GPIO1 Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)
	3:0	GPIO1_SEL [3:0]	0000b	GPIO1 Function Select 0000 = Input pin 0001 = Clock output (f=SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = FLL Lock output 0101 = Temperature OK output 0110 = Reserved 0111 = CODEC IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 = MIC Detect 1011 = MIC Short Circuit Detect 1100 to 1111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) GPIO3 and GPIO4	15	GPIO4_DEB_ENA	0b	GPIO4 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	14	GPIO4_IRQ_ENA	0b	GPIO4 IRQ Enable 0 = disabled 1 = enabled (GPIO4 input will generate IRQ)
	13	GPIO4_PU	0b	GPIO4 Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	12	GPIO4_PD	1b	GPIO4 Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)
	11:8	GPIO4_SEL [3:0]	0000b	GPIO4 Function Select 0000 = Input pin 0001 = Clock output (f=SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = FLL Lock output 0101 = Temperature OK output 0110 = Reserved 0111 = CODEC IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 = MIC Detect 1011 = MIC Short Circuit Detect 1100 to 1111 = Reserved
	7	GPIO3_DEB_ENA	0b	GPIO3 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	6	GPIO3_IRQ_ENA	0b	GPIO3 IRQ Enable 0 = disabled 1 = enabled (GPIO3 input will generate IRQ)
	5	GPIO3_PU	0b	GPIO3 Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	4	GPIO3_PD	1b	GPIO3 Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)
	3:0	GPIO3_SEL [3:0]	0000b	GPIO3 Function Select 0000 = Input pin 0001 = Clock output (f=SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = FLL Lock output 0101 = Temperature OK output 0110 = Reserved 0111 = CODEC IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 = MIC Detect 1011 = MIC Short Circuit Detect 1100 to 1111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) GPIO5 and GPIO6	15	GPIO6_DEB_ENA	0b	GPIO6 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	14	GPIO6_IRQ_ENA	0b	GPIO6 IRQ Enable 0 = disabled 1 = enabled (GPIO6 input will generate IRQ)
	13	GPIO6_PU	0b	GPIO6 Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	12	GPIO6_PD	1b	GPIO6 Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)
	11:8	GPIO6_SEL [3:0]	0000b	GPIO6 Function Select 0000 = Input pin 0001 = Clock output (f=SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = FLL Lock output 0101 = Temperature OK output 0110 = Reserved 0111 = CODEC IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 = MIC Detect 1011 = MIC Short Circuit Detect 1100 to 1111 = Reserved
	7	GPIO5_DEB_ENA	0b	GPIO5 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	6	GPIO5_IRQ_ENA	0b	GPIO5 IRQ Enable 0 = disabled 1 = enabled (GPIO5 input will generate IRQ)
	5	GPIO5_PU	0b	GPIO5 Pull-Up Resistor Enable 0 = Pull-up disabled 1 = Pull-up enabled (Approx 150kΩ)
	4	GPIO5_PD	1b	GPIO5 Pull-Down Resistor Enable 0 = Pull-down disabled 1 = Pull-down enabled (Approx 150kΩ)
	3:0	GPIO5_SEL [3:0]	0000b	GPIO5 Function Select 0000 = Input pin 0001 = Clock output (f=SYSCLK/OPCLKDIV) 0010 = Logic '0' 0011 = Logic '1' 0100 = FLL Lock output 0101 = Temperature OK output 0110 = Reserved 0111 = CODEC IRQ output 1000 = MIC Detect 1001 = MIC Short Circuit Detect 1010 = MIC Detect 1011 = MIC Short Circuit Detect 1100 to 1111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h) GPI7 and GPI8	15:12		1000b	Reserved - Do Not Change
	11	TEMPOK_IRQ_ENA	0b	Temperature Sensor CODEC IRQ Enable 0 = disabled 1 = enabled
	10	MIC1SHRT_IRQ_ENA	0b	MICBIAS short circuit detect CODEC IRQ Enable 0 = disabled 1 = enabled
	9	MIC1DET_IRQ_ENA	0b	MICBIAS current detect CODEC IRQ Enable 0 = disabled 1 = enabled
	8	FLL_LCK_IRQ_ENA	0b	FLL Lock CODEC IRQ Enable 0 = disabled 1 = enabled
	7	GPI8_DEB_ENA	0b	GPI8 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	6	GPI8_IRQ_ENA	0b	GPI8 IRQ Enable 0 = disabled 1 = enabled (GPI8 input will generate IRQ)
	5		0b	Reserved - Do Not Change
	4	GPI8_ENA	0b	GPI8 Input Pin Enable 0 = RIN3/GPI8 pin disabled as GPI8 input 1 = RIN3/GPI8 pin enabled as GPI8 input
	3	GPI7_DEB_ENA	0b	GPI7 Input De-Bounce 0 = disabled (Not de-bounced) 1 = enabled (Requires MCLK input and TOCLK_ENA=1)
	2	GPI7_IRQ_ENA	0b	GPI7 IRQ Enable 0 = disabled 1 = enabled (GPI7 input will generate IRQ)
	1		0b	Reserved - Do Not Change
	0	GPI7_ENA	0b	GPI7 Input Pin Enable 0 = LIN3/GPI7 pin disabled as GPI7 input 1 = LIN3/GPI7 pin enabled as GPI7 input
R23 (17h) GPIO Control (2)	15:13		0000b	Reserved - Do Not Change
	12	IRQ_INV (rw)	0b	IRQ Invert 0 = IRQ output active high 1 = IRQ output active low
	11	TEMPOK_POL (rw)	1b	Temperature Sensor polarity 0 = Non-inverted 1 = Inverted
	10	MIC1SHRT_POL (rw)	0b	MICBIAS short circuit detect polarity 0 = Non-inverted 1 = Inverted
	9	MIC1DET_POL (rw)	0b	MICBIAS current detect polarity 0 = Non-inverted 1 = Inverted
	8	FLL_LCK_POL (rw)	0b	FLL Lock Polarity 0 = Non-inverted 1 = Inverted

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	GPIO_POL[7:0] (rw)	00h	GPIOn Input Polarity 0 = Non-inverted 1 = Inverted GPIO_POL[7]: GPI8 polarity GPIO_POL[6]: GPI7 polarity GPIO_POL[5]: GPIO6 polarity GPIO_POL[4]: GPIO5 polarity GPIO_POL[3]: GPIO4 polarity GPIO_POL[2]: GPIO3 polarity GPIO_POL[1]: GPIO2 polarity GPIO_POL[0]: GPIO1 polarity
R24 (18h) LIN12 Input PGA Volume	15:9		00h	Reserved - Do Not Change
	8	IPVU[0]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	LI12MUTE	1b	LIN12 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	LI12ZC	0b	LIN12 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	5		0b	Reserved - Do Not Change
	4:0	LIN12VOL [4:0]	01011b	LIN12 Volume (See Table 24 for PGA volume range)
R25 (19h) LIN34 Input PGA Volume	15:9		00h	Reserved - Do Not Change
	8	IPVU[1]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	LI34MUTE	1b	LIN34 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	LI34ZC	0b	LIN34 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	5		0b	Reserved - Do Not Change
	4:0	LIN34VOL [4:0]	01011b	LIN34 Volume (See Table 24 for PGA volume range)
R26 (1Ah) RIN12 Input PGA Volume	15:9		00h	Reserved - Do Not Change
	8	IPVU[2]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	RI12MUTE	1b	RIN12 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	RI12ZC	0b	RIN12 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	5		0b	Reserved - Do Not Change
	4:0	RIN12VOL [4:0]	01011b	RIN12 Volume (See Table 24 for PGA volume range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) RIN34 Input PGA Volume	15:9		00h	Reserved - Do Not Change
	8	IPVU[3]	N/A	Input PGA Volume Update Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)
	7	RI34MUTE	1b	RIN34 PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	RI34ZC	0b	RIN34 PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	5		0b	Reserved - Do Not Change
	4:0	RIN34VOL [4:0]	01011b	RIN34 Volume (See Table 24 for PGA volume range)
R28 (1Ch) Left Headphone Output Volume	15:9		00h	Reserved - Do Not Change
	8	OPVU[0]	N/A	Output PGA Volume Update Writing a 1 to this bit will update LOPGA, ROPGA, LOUTVOL and ROUTVOL volumes simultaneously.
	7	LOZC	0b	Left Headphone Output Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6:0	LOUTVOL [6:0]	00h (mute)	Left Headphone Output Volume (See Table 53 for output PGA volume control range)
R29 (1Dh) Right Headphone Output Volume	15:9		00h	Reserved - Do Not Change
	8	OPVU[1]	N/A	Output PGA Volume Update Writing a 1 to this bit will update LOPGA, ROPGA, LOUTVOL and ROUTVOL volumes simultaneously.
	7	ROZC	0b	Right Headphone Output Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6:0	ROUTVOL [6:0]	00h (mute)	Right Headphone Output Volume (See Table 53 for output PGA volume control range)
R30 (1Eh) Line Output Volume	15:7		000h	Reserved - Do Not Change
	6	LONMUTE	1b	LON Line Output Mute 0 = Un-mute 1 = Mute
	5	LOPMUTE	1b	LOP Line Output Mute 0 = Un-mute 1 = Mute
	4	LOATTN	0b	LOP Attenuation 0 = 0dB 1 = -6dB
	3		0b	Reserved - Do Not Change
	2	RONMUTE	1b	RON Line Output Mute 0 = Un-mute 1 = Mute
	1	ROPMUTE	1b	ROP Line Output Mute 0 = Un-mute 1 = Mute
	0	ROATTN	0b	ROP Attenuation 0 = 0dB 1 = -6dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) OUT3 and OUT4 Volume	15:6		00000000 00b	Reserved - Do Not Change
	5	OUT3MUTE	1b	OUT3 Mute 0 = Un-mute 1 = Mute
	4	OUT3ATTN	0b	OUT3 Attenuation 0 = 0dB 1 = -6dB
	3:2		00b	Reserved - Do Not Change
	1	OUT4MUTE	1b	OUT4 Mute 0 = Un-mute 1 = Mute
	0	OUT4ATTN	0b	OUT4 Attenuation 0 = 0dB 1 = -6dB
R32 (20h) LOPGA Volume	15:9		00h	Reserved - Do Not Change
	8	OPVU[2]	N/A	Output PGA Volume Update Writing a 1 to this bit will update LOPGA, ROPGA, LOUTVOL and ROUTVOL volumes simultaneously.
	7	LOPGAZC	0b	LOPGA Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6:0	LOPGAVOL [6:0]	79h (0dB)	LOPGA Volume (See Table 53 for output PGA volume control range)
R33 (21h) ROPGA Volume	15:9		00h	Reserved - Do Not Change
	8	OPVU[3]	N/A	Output PGA Volume Update Writing a 1 to this bit will update LOPGA, ROPGA, LOUTVOL and ROUTVOL volumes simultaneously.
	7	ROPGAZC	0b	ROPGA Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6:0	ROPGAVOL [6:0]	79h (0dB)	ROPGA Volume (See Table 53 for output PGA volume control range)
R34 (22h) Speaker Volume	15:2		0000h	Reserved - Do Not Change
	1:0	SPKATTN [1:0]	11b	Speaker Output Attenuation (SPKN and SPKP) 00 = 0dB 01 = -6dB 10 = -12dB 11 = mute
R35 (23h) Class D (1)	15:9		00h	Reserved - Do Not Change
	8	CDMODE	0b	Speaker Class D Mode Enable 0 = Class D mode 1 = Class AB mode
	7	CLASSD_CLK_SEL	0b	Class D Clock Source 0 = Derived from SYSCLK (via DCLKDIV) 1 = 600kHz oscillator
	6:0		0000011b	Reserved - Do Not Change
R36 (24h) Class D (2)	15:0		0057h	Reserved - Do Not Change
R37 (25h) Class D (3)	15:6		00000000 100b	Reserved - Do Not Change

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5:3	DCGAIN [2:0]	000b	DC Speaker Boost 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 to 111 = Reserved
	2:0	ACGAIN [2:0]	000b	AC Speaker Boost 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 to 111 = Reserved
R38 (26h)	15:0		0000h	Reserved - Do Not Change
R39 (27h) Input Mixers (1)	15:4		000h	Reserved - Do Not Change
	3:2	AINLMODE [1:0]	00b	AINLMUX Input Source 00 = INMIXL (Left Input Mixer) 01 = RXVOICE (RXP - RXN) 10 = DIFFINL (LIN12 PGA - LIN34 PGA) 11 = (Reserved)
	1:0	AINRMODE [1:0]	00b	AINRMUX Input Source 00 = INMIXR (Right Input Mixer) 01 = RXVOICE (RXP - RXN) 10 = DIFFINR (RIN12 PGA - RIN34 PGA) 11 = (Reserved)
R40 (28h) Input Mixers (2)	15:8		00h	Reserved - Do Not Change
	7	LMP4	0b	LIN34 PGA Non-Inverting Input Select 0 = LIN4 not connected to PGA 1 = LIN4 connected to PGA
	6	LMN3	0b	LIN34 PGA Inverting Input Select 0 = LIN3 not connected to PGA 1 = LIN3 connected to PGA
	5	LMP2	0b	LIN12 PGA Non-Inverting Input Select 0 = LIN2 not connected to PGA 1 = LIN2 connected to PGA
	4	LMN1	0b	LIN12 PGA Inverting Input Select 0 = LIN1 not connected to PGA 1 = LIN1 connected to PGA
	3	RMP4	0b	RIN34 PGA Non-Inverting Input Select 0 = RIN4 not connected to PGA 1 = RIN4 connected to PGA
	2	RMN3	0b	RIN34 PGA Inverting Input Select 0 = RIN3 not connected to PGA 1 = RIN3 connected to PGA
	1	RMP2	0b	RIN12 PGA Non-Inverting Input Select 0 = RIN2 not connected to PGA 1 = RIN2 connected to PGA
	0	RMN1	0b	RIN12 PGA Inverting Input Select 0 = RIN1 not connected to PGA 1 = RIN1 connected to PGA

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R41 (29h) Input Mixers (3)	15:9		00h	Reserved - Do Not Change
	8	L34MNB	0b	LIN34 PGA Output to INMIXL Mute 0 = Mute 1 = Un-Mute
	7	L34MNBST	0b	LIN34 PGA Output to INMIXL Gain 0 = 0dB 1 = +30dB
	6		0b	Reserved - Do Not Change
	5	L12MNB	0b	LIN12 PGA Output to INMIXL Mute 0 = Mute 1 = Un-Mute
	4	L12MNBST	0b	LIN12 PGA Output to INMIXL Gain 0 = 0dB 1 = +30dB
	3		0b	Reserved - Do Not Change
	2:0	LDBVOL [2:0]	000b	LOMIX to INMIXL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
R42 (2Ah) Input Mixers (4)	15:9		00h	Reserved - Do Not Change
	8	R34MNB	0b	RIN34 PGA Output to INMIXR Mute 0 = Mute 1 = Un-Mute
	7	R34MNBST	0b	RIN34 PGA Output to INMIXR Gain 0 = 0dB 1 = +30dB
	6		0b	Reserved - Do Not Change
	5	R12MNB	0b	RIN12 PGA Output to INMIXR Mute 0 = Mute 1 = Un-Mute
	4	R12MNBST	0b	RIN12 PGA Output to INMIXR Gain 0 = 0dB 1 = +30dB
	3		0b	Reserved - Do Not Change
	2:0	RDBVOL [2:0]	000b	ROMIX to INMIXR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R43 (2Bh) Input Mixers (5)	15:9		00h	Reserved - Do Not Change
	8:6	LI2BVOL [2:0]	000b	LIN2 Pin to INMIXL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	5:3	LR4BVOL [2:0]	000b	RXVOICE to AINLMUX Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	2:0	LL4BVOL [2:0]	000b	LIN4/RXN Pin to INMIXL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
R44 (2Ch) Input Mixers (6)	15:9		00h	Reserved - Do Not Change
	8:6	RI2BVOL [2:0]	000b	RIN2 Pin to INMIXR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	5:3	RL4BVOL [2:0]	000b	RXVOICE to AINRMUX Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:0	RR4BVOL [2:0]	000b	RIN4/RXP Pin to INMIXR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
R45 (2Dh) Output Mixers (1)	15:8		00h	Reserved - Do Not Change
	7	LRBLO	0b	AINRMUX Output (Right ADC bypass) to LOMIX Mute 0 = Mute 1 = Un-mute
	6	LLBLO	0b	AINLMUX Output (Left ADC bypass) to LOMIX Mute 0 = Mute 1 = Un-mute
	5	LRI3LO	0b	RIN3 to LOMIX Mute 0 = Mute 1 = Un-mute
	4	LLI3LO	0b	LIN3 to LOMIX Mute 0 = Mute 1 = Un-mute
	3	LR12LO	0b	RIN12 PGA Output to LOMIX Mute 0 = Mute 1 = Un-mute
	2	LL12LO	0b	LIN12 PGA Output to LOMIX Mute 0 = Mute 1 = Un-mute
	1		0b	Reserved - Do Not Change
	0	LDLO	0b	Left DAC to LOMIX Mute 0 = Mute 1 = Un-mute Note: LDLO must be muted when LDSPK=1
R46 (2Eh) Output Mixers (2)	15:8		00h	Reserved - Do Not Change
	7	RLBRO	0b	AINLMUX Output (Left ADC bypass) to ROMIX Mute 0 = Mute 1 = Un-mute
	6	RRBRO	0b	AINRMUX Output (Right ADC bypass) to ROMIX 0 = Mute 1 = Un-mute
	5	RLI3RO	0b	LIN3 to ROMIX Mute 0 = Mute 1 = Un-mute
	4	RRI3RO	0b	RIN3 to ROMIX Mute 0 = Mute 1 = Un-mute
	3	RL12RO	0b	LIN12 PGA Output to ROMIX Mute 0 = Mute 1 = Un-mute
	2	RR12RO	0b	RIN12 PGA Output to ROMIX Mute 0 = Mute 1 = Un-mute
	1		0b	Reserved - Do Not Change

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	RDRO	0b	Right DAC to ROMIX Mute 0 = Mute 1 = Un-mute Note: RDRO must be muted when RDSPK=1
R47 (2Fh) Output Mixers (3)	15:9		00h	Reserved - Do Not Change
	8:6	LLI3LOVOL [2:0]	000b	LIN3 Pin to LOMIX Volume (See Table 51 for Volume Range)
	5:3	LR12LOVOL [2:0]	000b	RIN12 PGA Output to LOMIX Volume (See Table 51 for Volume Range)
	2:0	LL12LOVOL [2:0]	000b	LIN12 PGA Output to LOMIX Volume (See Table 51 for Volume Range)
R48 (30h) Output Mixers (4)	15:9		00h	Reserved - Do Not Change
	8:6	RRI3ROVOL [2:0]	000b	RIN3 to ROMIX Volume (See Table 51 for Volume Range)
	5:3	RL12ROVOL [2:0]	000b	LIN12 PGA Output to ROMIX Volume (See Table 51 for Volume Range)
	2:0	RR12ROVOL [2:0]	000b	RIN12 PGA Output to ROMIX Volume (See Table 51 for Volume Range)
R49 (31h) Output Mixers (5)	15:9		00h	Reserved - Do Not Change
	8:6	LRI3LOVOL [2:0]	000b	RIN3 to LOMIX Volume (See Table 51 for Volume Range)
	5:3	LRBLOVOL [2:0]	000b	AINRMUX Output (Right ADC bypass) to LOMIX Volume (See Table 51 for Volume Range)
	2:0	LLBLOVOL [2:0]	000b	AINLMUX Output (Left ADC bypass) to LOMIX Volume (See Table 51 for Volume Range)
R50 (32h) Output Mixers (6)	15:9		00h	Reserved - Do Not Change
	8:6	RLI3ROVOL [2:0]	000b	LIN3 to ROMIX Volume (See Table 51 for Volume Range)
	5:3	RLBROVOL [2:0]	000b	AINLMUX Output (Left ADC bypass) to ROMIX Volume (See Table 51 for Volume Range)
	2:0	RRBROVOL [2:0]	000b	AINRMUX Output (Right ADC bypass) to ROMIX Volume (See Table 51 for Volume Range)
R51 (33h) OUT3 and OUT4 Mixers	15:9		00h	Reserved - Do Not Change
	8:7	VSEL [1:0]	11b	Analogue Bias Optimisation 00 = Reserved 01 = Bias current optimized for AVDD=2.7V 1X = Lowest bias current, optimized for AVDD=3.3V
	6		0b	Reserved - Do Not Change
	5	LI4O3	0b	LIN4/RXN Pin to OUT3MIX 0 = Mute 1 = Un-mute
	4	LPGAO3	0b	LOPGA to OUT3MIX 0 = Mute 1 = Un-mute
	3:2		00b	Reserved - Do Not Change
	1	RI4O4	0b	RIN4/RXP Pin to OUT4MIX 0 = Mute 1 = Un-mute
	0	RPGAO4	0b	ROPGA to OUT4MIX 0 = Mute 1 = Un-mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R52 (34h) Line Output Mixers (1)	15:7		000h	Reserved - Do Not Change
	6	LLOPGALON	0b	LOPGA to LONMIX 0 = Mute 1 = Un-mute
	5	LROPGALON	0b	ROPGA to LONMIX 0 = Mute 1 = Un-mute
	4	LOPLON	0b	Inverted LOP Output to LONMIX 0 = Mute 1 = Un-mute
	3		0b	Reserved - Do Not Change
	2	LR12LOP	0b	RIN12 PGA Output to LOPMIX 0 = Mute 1 = Un-mute
	1	LL12LOP	0b	LIN12 PGA Output to LOPMIX 0 = Mute 1 = Un-mute
	0	LLOPGALOP	0b	LOPGA to LOPMIX 0 = Mute 1 = Un-mute
R53 (35h) Line Output Mixers (2)	15:7		000h	Reserved - Do Not Change
	6	RROPGARON	0b	ROPGA to RONMIX 0 = Mute 1 = Un-mute
	5	RLOPGARON	0b	LOPGA to RONMIX 0 = Mute 1 = Un-mute
	4	ROPRON	0b	Inverted ROP Output to RONMIX 0 = Mute 1 = Un-mute
	3		0b	Reserved - Do Not Change
	2	RL12ROP	0b	LIN12 PGA Output to ROPMIX 0 = Mute 1 = Un-mute
	1	RR12ROP	0b	RIN12 PGA Output to ROPMIX 0 = Mute 1 = Un-mute
	0	RROPGAROP	0b	ROPGA to ROPMIX 0 = Mute 1 = Un-mute
R54 (36h) Speaker Output Mixer	15:8		000h	Reserved - Do Not Change
	7	LB2SPK	0b	AINLMUX Output to SPKMIX 0 = Mute 1 = Un-mute
	6	RB2SPK	0b	AINRMUX Output to SPKMIX 0 = Mute 1 = Un-mute
	5	LI2SPK	0b	LIN2 to SPKMIX 0 = Mute 1 = Un-mute
	4	RI2SPK	0b	RIN2 to SPKMIX 0 = Mute 1 = Un-mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	LOPGASPK	0b	LOPGA to SPKMIX 0 = Mute 1 = Un-mute
	2	ROPGASPK	0b	ROPGA to SPKMIX 0 = Mute 1 = Un-mute
	1	LDSPK	0b	Left DAC to SPKMIX 0 = Mute 1 = Un-mute Note: LDSPK must be muted when LDLO=1
	0	RDSPK	0b	Right DAC to SPKMIX 0 = Mute 1 = Un-mute Note: RDSPK must be muted when RDRO=1
R55 (37h) Additional Control	15:1		0000h	Reserved - Do Not Change
	0	VROI	0b	VREF to Analogue Output Resistance (Disabled Outputs) 0 = 20kΩ (Headphone) or 10kΩ (Line Out) from buffered VMID to output 1 = 500Ω from buffered VMID to output
R56 (38h) Anti-Pop (1)	15:6		000h	Reserved - Do Not Change
	5	DIS_LLINE	0b	Discharges LOP and LON outputs via approx 500Ω resistor 0 = Not active 1 = Actively discharging LOP and LON
	4	DIS_RLINE	0b	Discharges ROP and RON outputs via approx 500Ω resistor 0 = Not active 1 = Actively discharging ROP and RON
	3	DIS_OUT3	0b	Discharges OUT3 output via approx 500Ω resistor 0 = Not active 1 = Actively discharging OUT3
	2	DIS_OUT4	0b	Discharges OUT4 output via approx 500Ω resistor 0 = Not active 1 = Actively discharging OUT4
	1	DIS_LOUT	0b	Discharges LOUT output via approx 500Ω resistor 0 = Not active 1 = Actively discharging LOUT
	0	DIS_ROUT	0b	Discharges ROUT output via approx 500Ω resistor 0 = Not active 1 = Actively discharging ROUT
R57 (39h) Anti-Pop (2)	15:7		0000_0000_0b	Reserved - Do Not Change
	6	SOFTST	0b	Enables VMID soft start 0 = Disabled 1 = Enabled
	5:4		00b	Reserved - Do Not Change
	3	BUFIOEN	0b	Enables the VGS / R current generator and the analogue input and output bias 0 = Disabled 1 = Enabled
	2	BUFDCOPEN	0b	Enables the VGS / R current generator 0 = Disabled 1 = Enabled
	1	POBCTRL	0b	Selects the bias current source for output amplifiers and VMID buffer 0 = VMID / R bias 1 = VGS / R bias

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	VMIDTOG	0b	Connects VMID to ground 0 = Disabled 1 = Enabled
R58 (3Ah) Microphone Bias	15:8		0000_0000b	Reserved - Do Not Change
	7:6	MCDSCTH [1:0]	00b	MICBIAS Short Circuit Detect Threshold 00 = 450uA 01 = 850uA 10 = 1250uA 11 = 1650uA These values are for AVDD=3.0V
	5:3	MDCTHR [2:0]	000b	MICBIAS Current Detect Threshold 000 = 220uA 001 = 330uA 010 = 440uA 011 = 550uA 100 = 660uA 101 = 770uA 110 = 880uA 111 = 990uA These values are for AVDD=3.0V
	2	MCD	0b	MICBIAS Current and Short Circuit Detect Enable 0 = disabled 1 = enabled
	1		0b	Reserved - Do Not Change
	0	MBSEL	0b	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD
R59 (3Bh) Reserved	15:0		0000h	Reserved - Do Not Change
R60 (3Ch) FLL Control 1	15:13		0h	Reserved - Do Not Change
	12	FLL_REF_FREQ	1	Low frequency reference locking 0 = Lock achieved after 509 ref clks (Recommended for Reference clock > 48kHz) 1 = Lock achieved after 49 ref clks (Recommended for Reference clock <= 48kHz)
	11:10	FLL_CLK_SRC		FLL Clock source 00 = MCLK 01 = DAC LRCLK 10 = ADC LRCLK 11 = GPIO6
	9	FLL_FRAC	0b	Fractional enable 0 = Integer Mode 1 = Fractional Mode 1 recommended in all cases
	8	FLL_OSC_ENA	0b	FLL Analogue enable 0 = FLL disabled 1 = FLL enabled FLL_OSC_ENA must be enabled before enabling FLL_ENA. The order is important.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:5	FLL_CTRL_RATE [2:0]	0h	Frequency of the FLL control block 000 = F_{VCO} / 1 (Recommended value) 001 = F_{VCO} / 2 010 = F_{VCO} / 4 011 = F_{VCO} / 8 100 = F_{VCO} / 16 101 = F_{VCO} / 32 Recommended that these are not changed from default.
	4:0	FLL_FRATIO [4:0]	8	CLK_VCO is divided by this integer, valid from 1 .. 31. 1 recommended for high freq reference 8 recommended for low freq reference
R61 (3Dh) FLL Control 2	15:0	FLL_K[15:0]	0h	Fractional multiply for CLK_REF
R62 (3Eh) FLL Control 3	15:10		00h	Reserved - Do Not Change
	9:0	FLL_N[9:0]	0h	Integer multiply for CLK_REF
R63 (3Fh) FLL Control 4	15:7		000h	Reserved - Do Not Change
	6:3	FLL_TRK_GAIN [3:0]	0h	Gain applied to error 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that these are not changed from default.
	2:0	FLL_OUTDIV [2:0]	3h	F_{OUT} clock divider 000 = F_{VCO} / 2 001 = F_{VCO} / 4 010 = F_{VCO} / 8 (best performance) 011 = F_{VCO} / 16 100 = F_{VCO} / 32 101 = Reserved 110 = Reserved 111 = Reserved
R65 (41h) LDO1 Control	15	LDO1_ENA	0b	LDO1 Software enable 0 = Disabled 1 = Enabled
	14	LDO1_SWI	0b	LDO1 function select 0 = LDO Regulator 1 = Current Limited switch
	13:12		00b	Reserved - Do Not Change
	11	LDO1_ERRACT	0b	LDO1 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
	10	LDO1_HIB_MODE	0b	LDO1 Hibernate Mode 0 = LDO1 disabled in Hibernate 1 = LDO1 enabled in Hibernate

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	9:5	LDO1_VIMG [4:0]	00000b	LDO1 Hibernate Mode output voltage 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details.
	4:0	LDO1_VSEL [4:0]	00000b	LDO1 voltage select 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details
R66 (42h) LDO2 Control	15	LDO2_ENA	0b	LDO2 Software enable 0 = Disabled 1 = Enabled
	14	LDO2_SWI	0b	LDO2 Software enable 0 = LDO Regulator 1 = Current Limited switch
	13:12		00b	Reserved - Do Not Change
	11	LDO2_ERRACT	0b	LDO2 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
	10	LDO2_HIB_MODE	0b	LDO2 Hibernate Mode 0 = LDO2 disabled in Hibernate 1 = LDO2 enabled in Hibernate
	9:5	LDO2_VIMG [4:0]	00000b	LDO2 Hibernate Mode output voltage 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details.
	4:0	LDO2_VSEL [4:0]	00000b	LDO2 voltage select 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details
R67 (43h) LDO3 Control	15	LDO3_ENA	0b	LDO3 Software enable 0 = Disabled 1 = Enabled
	14	LDO3_SWI	0b	LDO3 Software enable 0 = LDO Regulator 1 = Current Limited switch
	13:12		00b	Reserved - Do Not Change
	11	LDO3_ERRACT	0b	LDO3 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
	10	LDO3_HIB_MODE	0b	LDO3 Hibernate Mode 0 = LDO3 disabled in Hibernate 1 = LDO3 enabled in Hibernate
	9:5	LDO3_VIMG [4:0]	00000b	LDO3 Hibernate Mode output voltage 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details.
	4:0	LDO3_VSEL [4:0]	00000b	LDO3 voltage select 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R68 (44h) LDO4 Control	15	LDO4_ENA	0b	LDO4 Software enable 0 = Disabled 1 = Enabled
	14	LDO4_SWI	0b	LDO4 Software enable 0 = LDO Regulator 1 = Current Limited switch
	13:12		00b	Reserved - Do Not Change
	11	LDO4_ERRACT	0b	LDO4 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
	10	LDO4_HIB_MODE	0b	LDO4 Hibernate Mode 0 = LDO4 disabled in Hibernate 1 = LDO4 enabled in Hibernate
	9:5	LDO4_VIMG [4:0]	00000b	LDO4 Hibernate Mode output voltage 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details.
	4:0	LDO4_VSEL [4:0]	00000b	LDO4 voltage select 0.9v to 1.6v in 0.05v steps, 1.7 to 3.3v in 0.10v steps See Table 87 for details
R69 (45h) Reserved	15:0		0000h	Reserved - Do Not Change
R70 (46h) DCDC1 Control 1	15	DC1_ENA	0b	DC1 Software enable 0 = Disabled 1 = Enabled
	14	DC1_ACTIVE	1b	DC1 Active Mode select 0 = Standby/Hysteretic Mode selected 1 = Active Mode selected
	13	DC1_SLEEP	0b	DC1 Sleep Mode select 0 = Not selected 1 = Selected
	12		0b	Reserved - Do Not Change
	11	DC1_ERRACT	0b	DC1 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
	10	DC1_HIB_MODE	1b	DC1 Hibernate Mode 0 = DC1 disabled in Hibernate 1 = DC1 enabled (LDO mode) in Hibernate
	9:8	DC1_SOFTST [1:0]	00b	DC1 Soft Start 00 = No soft start 01 = 400us steps 10 = 4ms steps 11 = 40ms steps
	7	DC1_OV_PROT	0b	DC1 Overvoltage Protection 0 = Disabled 1 = Enabled
	6:0	DC1_VSEL [6:0]	0000000b	DC1 voltage select 0.85v to 4.025v in 0.025v steps See Table 88 for details

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R71 (47h) DCDC1 Control 2	15:14	DC1_CAP	01	DC-DC1 Output Capacitor 00 = Reserved 01 = 10µF 10 = 22µF 11 = 47µF
	13	DC1_FRC_PWM	0b	DC1 Force PWM operation 0 = Not selected 1 = PWM operation forced
	12:10		000b	Reserved - Do Not Change
	9:8	DC1_STBY_LIM [1:0]	00b	DC1 Standby Mode current limit If DC1_ACT_LIM = 0: 00 = 70mA 01 = 150mA 10 = 300mA 11 = 600mA If DC1_ACT_LIM = 1: 00 = 110mA 01 = 220mA 10 = 450mA 11 = 900mA
	7	DC1_ACT_LIM	0b	DC1 Active Mode current limit 0 = 600mA 1 = 1000mA
	6:0	DC1_VIMG [6:0]	0000000b	DC1 Hibernate Mode output voltage 0.85v to 4.025v in 0.025v steps See Table 88 for details
R72 (48h) DCDC2 Control 1	15	DC2_ENA	0b	DC2 Software enable 0 = Disabled 1 = Enabled
	14	DC2_ACTIVE	1b	DC2 Active Mode select 0 = Standby/Hysteretic Mode selected 1 = Active Mode selected
	13	DC2_SLEEP	0b	DC2 Sleep Mode select 0 = Not selected 1 = Selected
	12		0b	Reserved - Do Not Change
	11	DC2_ERRACT	0b	DC2 Undervoltage Error Action 0 = Generate IRQ only 1 = Generate IRQ, Assert NRST, De-assert PWRGOOD, Shutdown device
	10	DC2_HIB_MODE	1b	DC2 Hibernate Mode 0 = DC2 disabled in Hibernate 1 = DC2 enabled (LDO mode) in Hibernate
	9:8	DC2_SOFTST [1:0]	00b	DC2 Soft Start 00 = No soft start 01 = 400us steps 10 = 4ms steps 11 = 40ms steps
	7	DC2_OV_PROT	0b	DC2 Overvoltage Protection 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:0	DC2_VSEL [6:0]	0000000b	DC2 voltage select 0.85v to 4.025v in 0.025v steps See Table 88 for details
R73 (49h) DCDC2 Control 2	15:14	DC1_CAP	01	DC-DC2 Output Capacitor 00 = Reserved 01 = 10µF 10 = 22µF 11 = 47µF
	13	DC2_FRC_PWM	0b	DC2 Force PWM operation 0 = Not selected 1 = PWM operation forced
	12:10		000b	Reserved - Do Not Change
	9:8	DC2_STBY_LIM [1:0]	00b	DC2 Standby Mode current limit If DC2_ACT_LIM = 0: 00 = 70mA 01 = 150mA 10 = 300mA 11 = 600mA If DC2_ACT_LIM = 1: 00 = 110mA 01 = 220mA 10 = 450mA 11 = 900mA
	7	DC2_ACT_LIM	0b	DC2 Active Mode current limit 0 = 600mA 1 = 1000mA
	6:0	DC2_VIMG [6:0]	0000000b	DC2 Hibernate Mode output voltage 0.85v to 4.025v in 0.025v steps See Table 88 for details
R74 (4Ah) Reserved	15:0		0000h	Reserved - Do Not Change
R75 (4Bh) Interface	15:4		000h	Reserved - Do Not Change
	3	AUTOINC	1b	Enable Auto-Increment function (2-wire I2C mode) 0 = Disabled 1 = Enabled
	2	ARA_ENA	0b	Enable Alert Response Address function (2-wire I2C mode) 0 = Disabled 1 = Enabled
	1	SPI_CFG	0b	3-wire Read mode configuration 0 = CMOS output 1 = Open-drain
	0		0b	Reserved - Do Not Change
R76 (4Ch) PM General	15	CODEC_SOFTST	0b	CODEC Soft Start Sequence 0 = Disabled 1 = Enabled
	14	CODEC_SOFTSD	0b	CODEC Soft Shutdown Sequence 0 = Disabled 1 = Enabled
	13	CHIP_SOFTSD	0b	Chip Soft Shutdown Sequence 0 = Disabled 1 = Enabled
	12:4		000h	Reserved - Do Not Change

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	DSLEEP1_POL	0	MSLEEP control 0 = Active high 1 = Active low
	2	DSLEEP2_POL	0	HSLEEP control 0 = Active high 1 = Active low
	1:0	PWR_STATE	00	Power State software control 00 = Active 01 = Soft Sleep 10 = Deep Sleep 11 = Reserved
R77 (4Dh) Reserved	15:0		0b	Reserved - Do Not Change
R78 (4Eh) PM Shutdown Control	15:10		00000b	Reserved - Do Not Change
	9	CHIP_GT150_ERR ACT	1b	Device Overtemperature 2 Action 0 = UVLO generates IRQ only 1 = UVLO generates IRQ and initiates device shutdown
	8	CHIP_GT115_ERR ACT	0b	Device Overtemperature 1 Action 0 = UVLO generates IRQ only 1 = UVLO generates IRQ and initiates device shutdown
	7	LINE_CMP_ERRAC T	1b	Battery Comparator Action 0 = Battery failure condition generates IRQ only 1 = Battery failure condition generates IRQ and initiates device shutdown
	6	UVLO_ERRACT	1b	Undervoltage Lock-Out Action 0 = UVLO generates IRQ only 1 = UVLO generates IRQ and initiates device shutdown
	5:0		000000b	Reserved - Do Not Change
R79 (4Fh) Interrupt Status 1	15	MICD_CINT	0b	MIC Current Detect IRQ status 0 = MIC Current IRQ not set 1 = MIC Current IRQ set
	14	MICSCD_CINT	0b	MIC Short Circuit IRQ status 0 = MIC Short Circuit IRQ not set 1 = MIC Short Circuit IRQ set
	13	JDL_CINT	0b	Jack Detect (Left) IRQ status 0 = Jack Detect (Left) IRQ not set 1 = Jack Detect (Left) IRQ set
	12	JDR_CINT	0b	Jack Detect (Right) IRQ status 0 = Jack Detect (Right) IRQ not set 1 = Jack Detect (Right) IRQ set
	11	CODEC_SEQ_END _EINT	0b	CODEC softstart or shutdown status 0 = CODEC sequence normal 1 = CODEC softstart or shutdown sequence completed
	10	CDEL_TO_EINT	0b	CDELAY IRQ status 0 = CDELAY normal 1 = Reset Delay Timer was triggered by 500ms timeout OR invalid CDELAY capacitance caused CDELAY error.
	9	CHIP_GT150_EINT	0b	Temperature Level 2 IRQ status 0 = 150°C threshold not exceeded 1 = 150°C threshold exceeded
	8	CHIP_GT115_EINT	0b	Temperature Level 1 IRQ status 0 = 115°C threshold not exceeded 1 = 115°C threshold exceeded

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7	LINE_CMP_EINT	0b	Battery Comparator IRQ status 0 = Battery Comparator normal 1 = Battery Comparator undervoltage
	6	UVLO_EINT	0b	UVLO IRQ status 0 = UVLO disabled 1 = UVLO enabled
	5	DC2_UV_EINT	0b	DC2 Converter IRQ status 0 = DC2 voltage normal 1 = DC2 undervoltage detected
	4	DC1_UV_EINT	0b	DC1 Converter IRQ status 0 = DC1 voltage normal 1 = DC1 undervoltage detected
	3	LDO4_UV_EINT	0b	LDO4 Regulator IRQ status 0 = LDO4 voltage normal 1 = LDO4 undervoltage detected
	2	LDO3_UV_EINT	0b	LDO3 Regulator IRQ status 0 = LDO3 voltage normal 1 = LDO3 undervoltage detected
	1	LDO2_UV_EINT	0b	LDO2 Regulator IRQ status 0 = LDO2 voltage normal 1 = LDO2 undervoltage detected
	0	LDO1_UV_EINT	0b	LDO1 Regulator IRQ status 0 = LDO1 voltage normal 1 = LDO1 undervoltage detected
R80 (50h) Interrupt Status 1 Mask	15	IM_MICD_CINT	0b	MIC Current Detect IRQ enable 0 = Not masked 1 = Masked
	14	IM_MICSCD_CINT	0b	MIC Short Circuit IRQ enable 0 = Not masked 1 = Masked
	13	IM_JDL_CINT	0b	Jack Detect (Left) IRQ enable 0 = Not masked 1 = Masked
	12	IM_JDR_CINT	0b	Jack Detect (Right) IRQ enable 0 = Not masked 1 = Masked
	11	IM_CODEC_SEQ_END_EINT	0b	CODEC softstart or shutdown IRQ enable 0 = Not masked 1 = Masked
	10	IM_CDEL_TO_EINT	0b	CDELAY IRQ enable 0 = Not masked 1 = Masked
	9	IM_CHIP_GT150_EINT	0b	Temperature Level 2 IRQ enable 0 = Not masked 1 = Masked
	8	IM_CHIP_GT115_EINT	0b	Temperature Level 1 IRQ enable 0 = Not masked 1 = Masked
	7	IM_LINE_CMP_EINT	0b	Battery Comparator IRQ enable 0 = Not masked 1 = Masked
	6	IM_UVLO_EINT	0b	UVLO IRQ enable 0 = Not masked 1 = Masked

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5	IM_DC2_UV_EINT	0b	DC2 Converter IRQ enable 0 = Not masked 1 = Masked
	4	IM_DC1_UV_EINT	0b	DC1 Converter IRQ enable 0 = Not masked 1 = Masked
	3	IM_LDO4_UV_EINT	0b	LDO4 Regulator IRQ enable 0 = Not masked 1 = Masked
	2	IM_LDO3_UV_EINT	0b	LDO3 Regulator IRQ enable 0 = Not masked 1 = Masked
	1	IM_LDO2_UV_EINT	0b	LDO2 Regulator IRQ enable 0 = Not masked 1 = Masked
	0	IM_LDO1_UV_EINT	0b	LDO1 Regulator IRQ enable 0 = Not masked 1 = Masked
R81 (51h) Interrupt Levels	15	MICD_LVL	0b	MIC Current Detect IRQ level 0 = MIC Current not detected 1 = MIC Current detected
	14	MICSCD_LVL	0b	MIC Short Circuit IRQ level 0 = MIC Short Circuit not detected 1 = MIC Short Circuit detected
	13	JDL_LVL	0b	Jack Detect (Left) IRQ level 0 = Jack Detect (Left) not detected 1 = Jack Detect (Left) detected
	12	JDR_LVL	0b	Jack Detect (Right) IRQ level 0 = Jack Detect (Right) not detected 1 = Jack Detect (Right) detected
	11	CODEC_SEQ_END_LVL	0b	CODEC softstart or shutdown IRQ level 0 = CODEC sequence normal 1 = CODEC softstart or shutdown sequence completed
	9	CHIP_GT150_LVL	0b	Temperature Level 2 IRQ level 0 = 150°C threshold not exceeded 1 = 150°C threshold exceeded
	8	CHIP_GT115_LVL	0b	Temperature Level 1 IRQ level 0 = 115°C threshold not exceeded 1 = 115°C threshold exceeded
	7	LINE_CMP_LVL	0b	Battery Comparator IRQ level 0 = Battery Comparator normal 1 = Battery Comparator undervoltage
	6	UVLO_LVL	0b	UVLO IRQ level 0 = UVLO disabled 1 = UVLO enabled
	5	DC2_UV_LVL	0b	DC2 Converter IRQ level 0 = DC2 voltage normal 1 = DC2 undervoltage detected
	4	DC1_UV_LVL	0b	DC1 Converter IRQ level 0 = DC1 voltage normal 1 = DC1 undervoltage detected
	3	LDO4_UV_LVL	0b	LDO4 Regulator IRQ level 0 = LDO4 voltage normal 1 = LDO4 undervoltage detected

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2	LDO3_UV_LVL	0b	LDO3 Regulator IRQ level 0 = LDO3 voltage normal 1 = LDO3 undervoltage detected
	1	LDO2_UV_LVL	0b	LDO2 Regulator IRQ level 0 = LDO2 voltage normal 1 = LDO2 undervoltage detected
	0	LDO1_UV_LVL	0b	LDO1 Regulator IRQ level 0 = LDO1 voltage normal 1 = LDO1 undervoltage detected
R82 (52h) Shutdown Reason	15:14		00b	Reserved - Do Not Change
	13	SDR_CHIP_SOFTSD	0b	CHIP_SOFTSD shutdown status 0 = Disabled 1 = Enabled
	12		0b	Reserved - Do Not Change
	11	SDR_NPDN	0b	NPDN shutdown status 0 = Disabled 1 = Enabled
	10		0b	Reserved - Do Not Change
	9	SDR_CHIP_GT150	0b	Temperature Level 2 shutdown status 0 = Disabled 1 = Enabled
	8	SDR_CHIP_GT115	0b	Temperature Level 1 shutdown status 0 = Disabled 1 = Enabled
	7	SDR_LINE_CMP	0b	Battery Comparator shutdown status 0 = Disabled 1 = Enabled
	6	SDR_UVLO	0b	UVLO shutdown status 0 = Disabled 1 = Enabled
	5	SDR_DC2_UV	0b	DC2 Undervoltage shutdown status 0 = Disabled 1 = Enabled
	4	SDR_DC1_UV	0b	DC1 Undervoltage shutdown status 0 = Disabled 1 = Enabled
	3	SDR_LDO4_UV	0b	LDO4 Undervoltage shutdown status 0 = Disabled 1 = Enabled
	2	SDR_LDO3_UV	0b	LDO3 Undervoltage shutdown status 0 = Disabled 1 = Enabled
	1	SDR_LDO2_UV	0b	LDO2 Undervoltage shutdown status 0 = Disabled 1 = Enabled
	0	SDR_LDO1_UV	0b	LDO1 Undervoltage shutdown status 0 = Disabled 1 = Enabled
R83 (53h) Reserved	15:0		0000h	Reserved - Do Not Change
R84 (54h) Line Circuits	15:8		00h	Reserved - Do Not Change
	7:4	LINE_CMP_VTHI [3:0]	0111b	Rising Threshold for LINE comparator 2.70v to 3.45v in 50mv steps See Table 98 for details

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	LINE_CMP_VTHD [3:0]	0100b	Falling Threshold for LINE comparator 2.70v to 3.45v in 50mv steps See Table 98 for details
R85 (55h) to R127 (7Fh)	Reserved - Do Not Change			

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.05dB	0		0.454 fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.546s			
Stopband Attenuation	f > 0.546 fs	-60			dB
DAC Normal Filter					
Passband	+/- 0.03dB	0		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.454 fs			+/- 0.03	dB
Stopband		0.546 fs			
Stopband Attenuation	F > 0.546 fs	-50			dB
DAC Sloping Stopband Filter					
Passband	+/- 0.03dB	0		0.25 fs	
	+/- 1dB	0.25 fs		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.25 fs			+/- 0.03	dB
Stopband 1		0.546 fs		0.7 fs	
Stopband 1 Attenuation	f > 0.546 fs	-60			dB
Stopband 2		0.7 fs		1.4 fs	
Stopband 2 Attenuation	f > 0.7 fs	-85			dB
Stopband 3		1.4 fs			
Stopband 3 Attenuation	F > 1.4 fs	-55			dB

DAC FILTERS		ADC FILTERS	
Mode	**Group Delay**	**Mode**	**Group Delay**
Normal	18 / fs	Normal	18 / fs
Sloping Stopband	18 / fs		

ADC FILTER RESPONSES

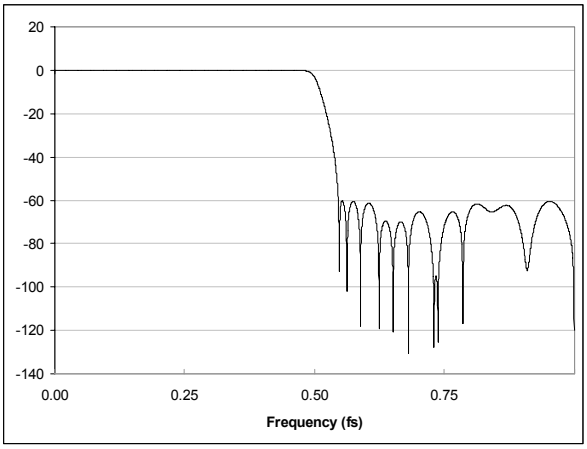


Figure 87 ADC Digital Filter Frequency Response

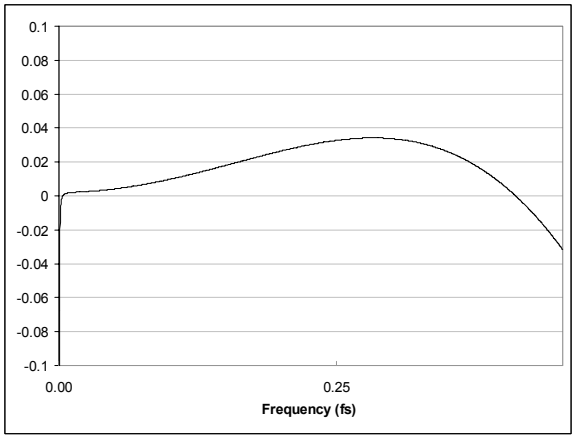


Figure 88 ADC Digital Filter Ripple

ADC HIGH PASS FILTER RESPONSES

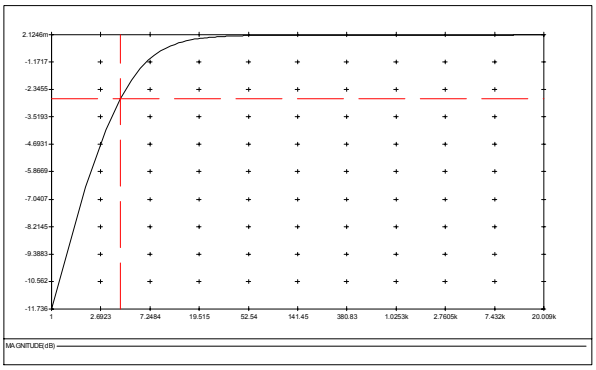


Figure 89 ADC Digital High Pass Filter Frequency Response (48kHz, Hi-Fi Mode, ADC_HPF_CUT[1:0]=00)

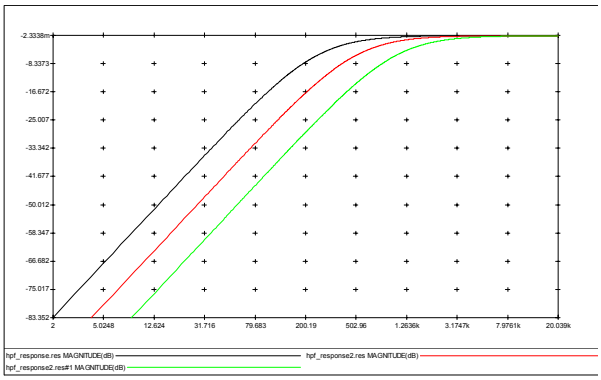


Figure 90 ADC Digital High Pass Filter Ripple (48kHz, Voice Mode, ADC_HPF_CUT=01, 10 and 11)

DAC FILTER RESPONSES

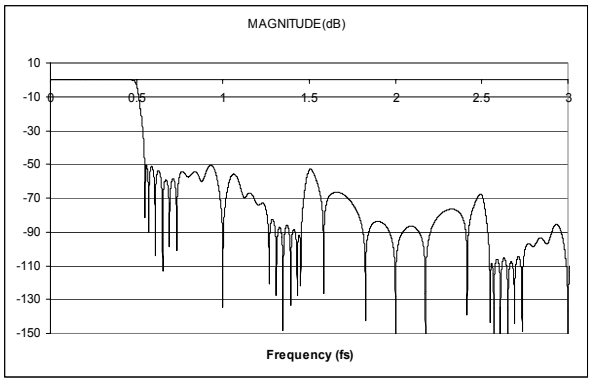


Figure 91 DAC Digital Filter Frequency Response (Normal Mode)

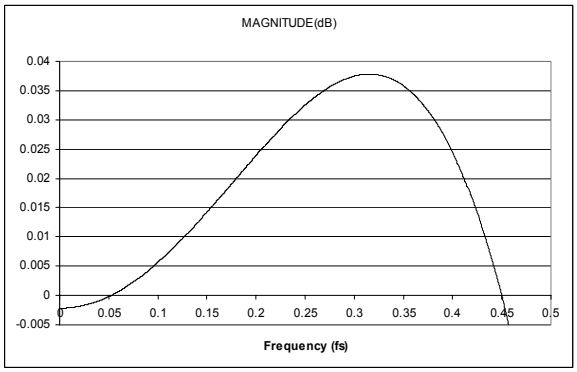


Figure 92 DAC Digital Filter Ripple (Normal Mode)

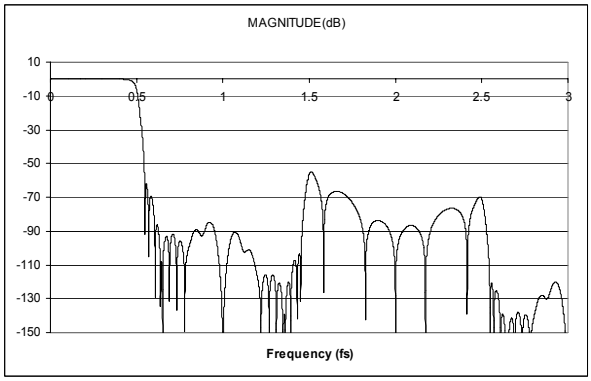


Figure 93 DAC Digital Filter Frequency Response (Sloping Stopband Mode)

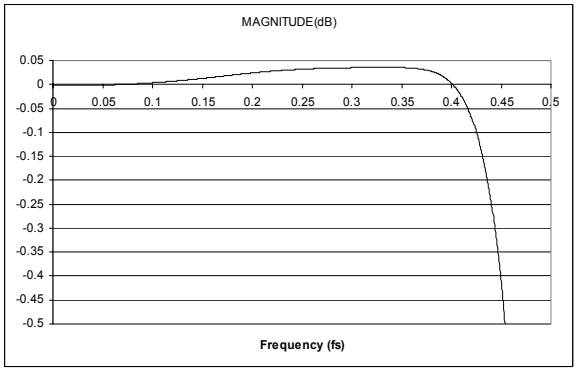


Figure 94 DAC Digital Filter Ripple (Sloping Stopband Mode)

DE-EMPHASIS FILTER RESPONSES

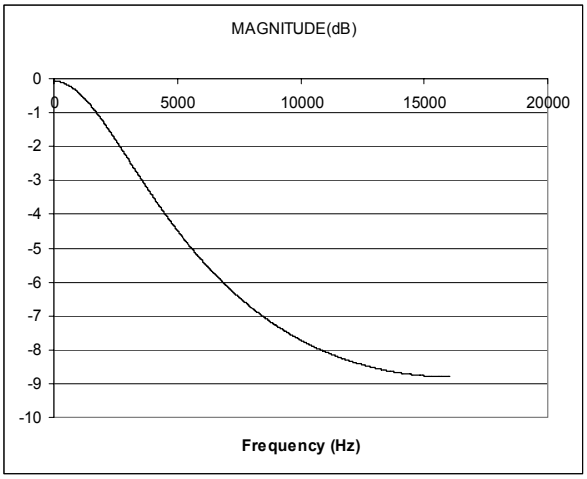


Figure 95 De-Emphasis Digital Filter Response (32kHz)

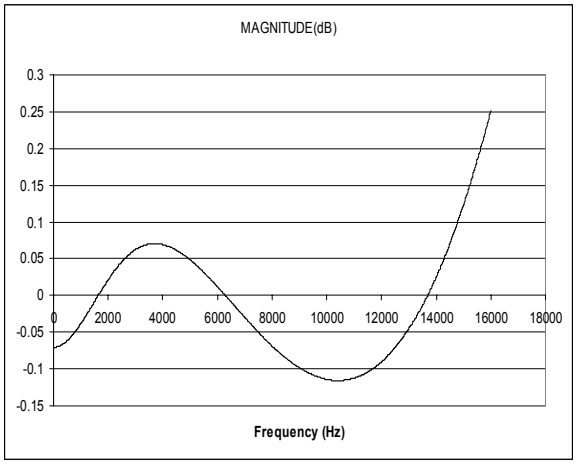


Figure 96 De-Emphasis Error (32kHz)

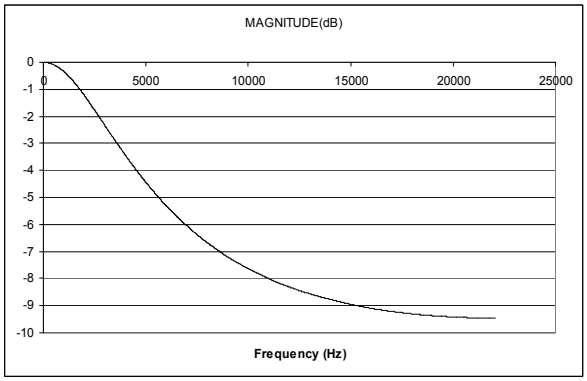


Figure 97 De-Emphasis Digital Filter Response (44.1kHz)

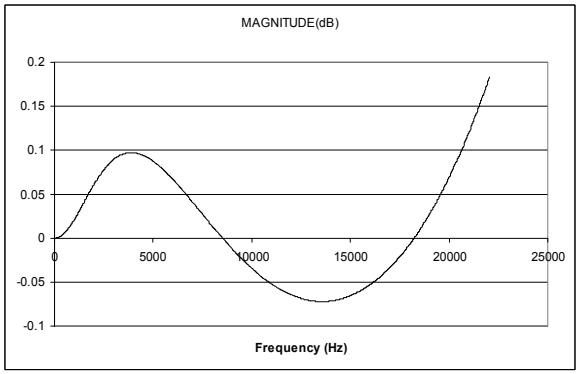


Figure 98 De-Emphasis Error (44.1kHz)

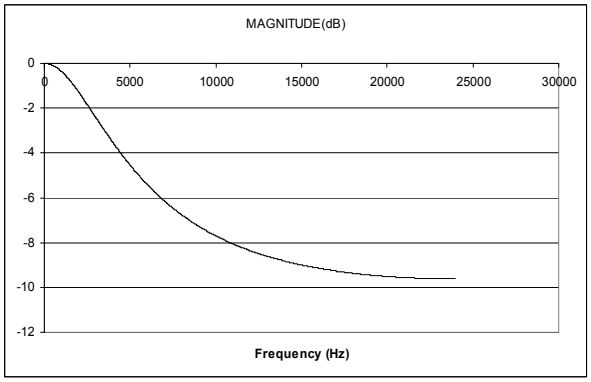


Figure 99 De-Emphasis Digital Filter Response (48kHz)

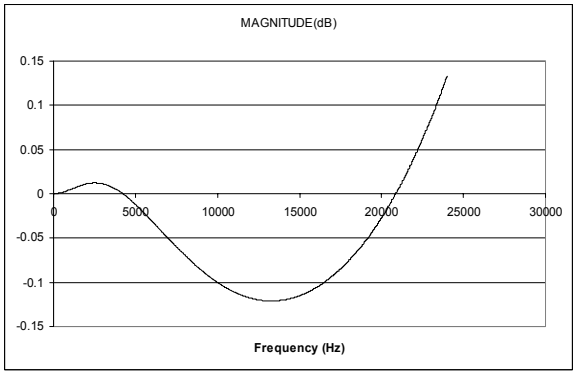


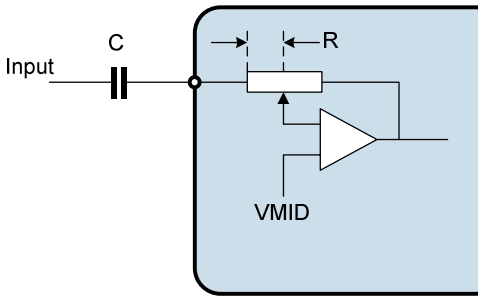
Figure 100 De-Emphasis Error (48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

AUDIO INPUT PATHS

The WM8400 provides 4 stereo pairs of analogue audio inputs. Each of these inputs is referenced to the internal DC reference, VMID. A DC blocking capacitor is required for each input pin used in the target application. The choice of capacitor is determined by the filter that is formed between that capacitor and the input impedance of the input pin. The circuit is illustrated in Figure 101.



$$Fc = \frac{1}{2\pi RC}$$

Fc = high pass 3dB cut-off frequency

Figure 101 Audio Input Path DC Blocking

Using a large capacitance will result in a lower filter cut-off frequency, with no attenuation of the audio frequencies of interest. However, a large capacitance is undesirable in a portable application due to its large physical size. A small capacitance will raise the cut-off frequency, which may result in some of the audio bandwidth being compromised. A judgement needs to be made regarding what frequencies require to be passed by the filter. For hi-fi audio applications, typical circuits aim to provide a cut-off frequency at 20Hz.

If the input impedance is known, and the cut-off frequency is known, then the minimum capacitor value may be derived easily. However, it can be seen from the representation in Figure 101 that the input impedance is not fixed in all applications but can vary with gain and boost amplifier settings. The choice of capacitor for a 20Hz cut-off frequency is shown in Table 105 for different input impedance conditions. The applicable input impedance can be found in the "Electrical Characteristics" section of this datasheet.

IMPEDANCE	MINIMUM CAPACITANCE FOR 20HZ PASS BAND
2kΩ	4 µF
15kΩ	0.5 µF
30kΩ	0.27 µF
60kΩ	0.13 µF

Table 104 Audio Input DC Blocking Capacitors

Using the figures in Table 105, it follows that a 1µF capacitance for all input connections will give good results in most cases. Tantalum electrolytic capacitors are particularly suitable as they offer high stability in a small package size.

Ceramic equivalents are a cost effective alternative to the superior tantalum packages, but care must be taken to ensure the desired capacitance is maintained at the AVDD operating voltage. Also, ceramic capacitors may show microphonic effects, where vibrations and mechanical conditions give rise to electrical signals. This is particularly problematic for microphone input paths where a large signal gain is required.

A single capacitor is required for a line input or single-ended microphone connection. In the case of a differential microphone connection, a DC blocking capacitor is required on both input pins.

AUDIO OUTPUT PATHS

The WM8400 provides 4 line outputs (LOP, LON, ROP, RON) and 4 headphone outputs (LOUT, ROUT, OUT3, OUT4). Each of these outputs is referenced to the internal DC reference, VMID. These outputs may be connected in a number of different ways, including differential and capless options (see "Analogue Output Paths").

In the case of any line output or headphone output used in a single-ended configuration (i.e. referenced to AGND), a DC blocking capacitor will be required in order to remove the VMID bias. In the case of capless outputs (using a disabled or muted output as a 'virtual ground') or a pair of outputs that are configured as a differential pair, then the DC blocking capacitor should be omitted.

The choice of capacitor is determined from the filter that is formed between the capacitor and the load impedance. The line outputs are intended to drive a typical line load of 10kΩ or 47kΩ impedance. The headphone outputs would typically be connected to a load of 16Ω or 32Ω per left/right channel. Similar to the choice of audio input capacitor, a judgement needs to be made regarding what frequencies require to be passed, and what the anticipated load impedance will be. The choice of capacitor for a 20Hz cut-off frequency is shown in Table 105 for different impedance conditions.

IMPEDANCE	MINIMUM CAPACITANCE FOR 20HZ PASS BAND
16Ω	498 µF
32Ω	248 µF
10kΩ	0.8 µF
47kΩ	0.17 µF

Table 105 Line Output Frequency Cut-Off

Using the figures in Table 105, it follows that a 220µF capacitance would be a suitable choice for a 32Ω headphone load and that a 1µF capacitance would be a suitable choice for a line load. Tantalum electrolytic capacitors are particularly suitable as they offer high stability in a small package size. Ceramic equivalents are a cost effective alternative to the superior tantalum packages, but care must be taken to ensure the desired capacitance is maintained at the AVDD operating voltage.

For best audio performance, it is recommended to connect a zobel network to the audio output pins. This network should comprise a 50Ω resistor and 22nF capacitor in series with each other. These components have the effect of dampening high frequency oscillations or instabilities that can arise outside the audio band under certain conditions. Possible sources of these instabilities include the inductive load of a headphone coil or an active load in the form of an external line amplifier.

For best pop suppression performance, it is recommended to connect a 47kΩ resistor between the load and AGND. This will ensure that the output capacitor does not become charged as a result of unpredictable behaviour in the load, or as a result of memory effects in the capacitor. The inclusion of this resistor ensures best compatibility with the WM8400 pop & click suppression circuits.

The complete set of recommended components for single-ended headphone and line outputs is illustrated in Figure 102. Note that, as described above, not all of these components will be required in all circumstances.

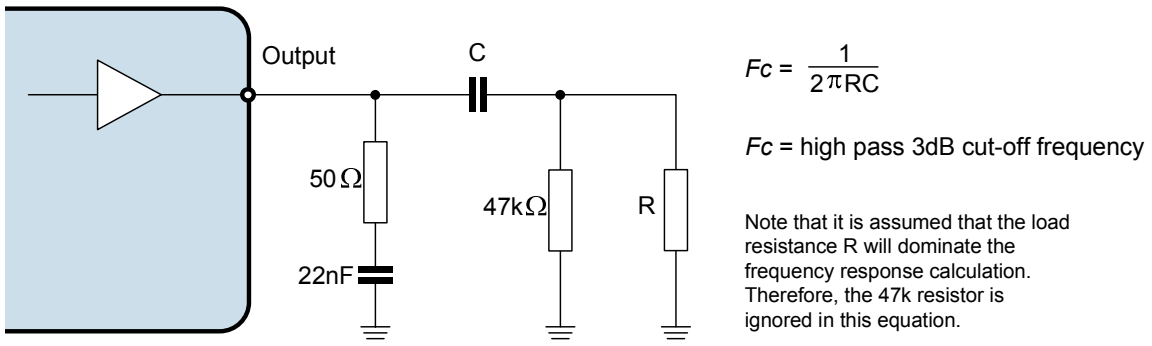


Figure 102 Audio Output Path Components

POWER SUPPLY DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations (or 'spikes') in the power supply voltage can cause malfunctions and unintentional behaviour in other components. A decoupling (or 'bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the WM8400, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling (or 'bypass') capacitor can be used to filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail. The best protection is achieved by placing the capacitor as close as possible to the circuit to be decoupled. This is because lengthy interconnect tracks can result in inductance which will reduce the effectiveness of the capacitor. The decoupling capacitors should therefore be placed as close as possible to the WM8400.

For the purposes of decoupling from high frequency effects on the power supply rails, the size of the decoupling/bypass capacitor is dependent upon the frequencies at which decoupling is required. The higher the frequency of the switching effects, the smaller capacitance that is required to shunt them. In the case of lower frequencies or for higher current loads, a larger capacitance will be required for adequate decoupling.

The recommended power supply decoupling capacitors are listed below in Table 106.

POWER SUPPLY	DECOUPLING CAPACITOR
FLLVDD, DCVDD, I2CVDD, I2S1VDD, I2S2VDD, MBVDD, HBVDD	0.1μF ceramic
AVDD, HPVDD	4.7μF ceramic
VMID	4.7μF ceramic
VINT	1uF ceramic

Table 106 Power Supply Decoupling Capacitors

A small capacitance is recommended for many of the supplies listed above, as appropriate for the high frequency switching of the ADCs, DACs and digital core.

A larger capacitance is recommended for AVDD and HPVDD decoupling. In many applications, a smaller capacitor (eg. 1μF) will be sufficient for the AVDD connection, as the low power design of the WM8400 results in very low AVDD current. The recommended 4.7μF capacitance will provide a greater level of immunity to electrical noise on the AVDD and HPVDD power rails.

As noted above, all decoupling capacitors should be as close as possible to the WM8400 device. The connection between AGND, the AVDD decoupling capacitor and the main system ground should be made at a single point as close as possible to the AGND ball of the WM8400. Similarly, the connection between HPGND, the HPVDD decoupling capacitor and the main system ground should be a single point that is as close as possible to the HPGND ball of the WM8400.

The VMID capacitor is not, technically, a decoupling capacitor. However, it does serve a similar purpose in filtering noise on the VMID bias voltage to which the microphone and line inputs are referenced. Using a smaller capacitance is not recommended here as it may lead to an increased noise level throughout the analogue signal chain.

Similarly, the VINT capacitor is not, technically, a decoupling capacitor. VINT is the output of an internal linear regulator, therefore the VINT capacitor both acts as a filter for noise and also as the energy storage device for the regulator.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application.

MICROPHONE BIAS CIRCUIT

The WM8400 is designed to interface easily with up to four electret condenser microphones. These may be connected in single-ended or pseudo-differential configurations. The single-ended method allows greater capability for the connection of multiple audio sources simultaneously, whilst the pseudo-differential method provides better performance due to its rejection of common-mode noise.

In either configuration, the electret microphone requires a bias current, which is provided via the MICBIAS connection of the WM8400. The bias current is generated by an output-compensated amplifier, which requires an external capacitor in order to ensure accuracy and stability. The recommended capacitance is 4.7µF. A ceramic type is a suitable choice here, providing that care is taken to choose a component that exhibits this capacitance at the intended MICBIAS voltage.

A current-limiting resistor is also required for the electret condenser microphone. The resistance should be chosen according to the recommended operating voltage of the microphone and the maximum bias current of the WM8400. The operating voltage of a typical electret microphone for portable applications is around 1.3v. The recommended 2.2kΩ current limiting resistor is suggested as it provides compatibility with a wide range of microphone models.

Note that the MICBIAS voltage may be adjusted using register control to suit the requirements of the microphone. Also note the WM8400 supports a maximum MICBIAS current of 3mA in total; if more than one microphone interface is connected, the combined current of these interfaces must not exceed 3mA.

Figure 103 illustrates the recommended single-ended and pseudo-differential microphone connections for the WM8400.

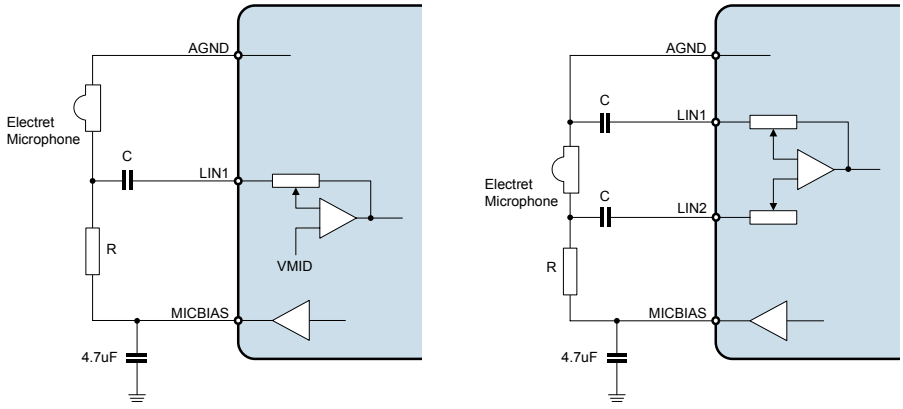


Figure 103 Single-Ended and Pseudo-Differential Microphone Connections

CLASS D SPEAKER CONNECTIONS

The WM8400 incorporates a Class D/AB 1W speaker driver. By default, the device operates in Class D mode, which offers high amplifier efficiency at large signal levels. As the Class D output is a pulse width modulated signal, the choice of speakers and tracking of signals is critical for ensuring good performance and reducing EMI in this mode.

The Class D output requires external filtering in order to recreate the audio signal. This may be implemented using an LC or RC filter or else may be achieved by using a loudspeaker whose internal inductance provides the required filter response. An LC or RC filter should be used if the loudspeaker characteristics are unknown or unsuitable, or if the length of the loudspeaker connection is likely to lead to EMI problems.

In applications where it is necessary to provide Class D filter components, an LC filter is the recommended solution, in order to minimise the power dissipated in the filter. A suitable implementation is illustrated in Figure 104.

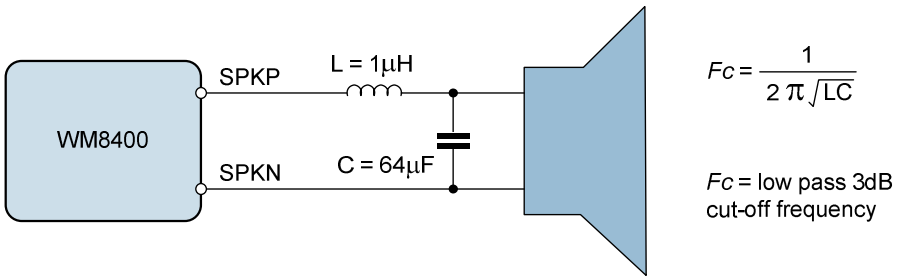


Figure 104 Class D Output Filter Components

A simple equivalent circuit of a loudspeaker consists of a serially connected resistor and inductor, as shown in Figure 105. This circuit provides a low pass filter for the speaker output. If the loudspeaker characteristics are suitable, then the loudspeaker itself can be used in place of the filter components described earlier. This is known as 'filterless operation'.

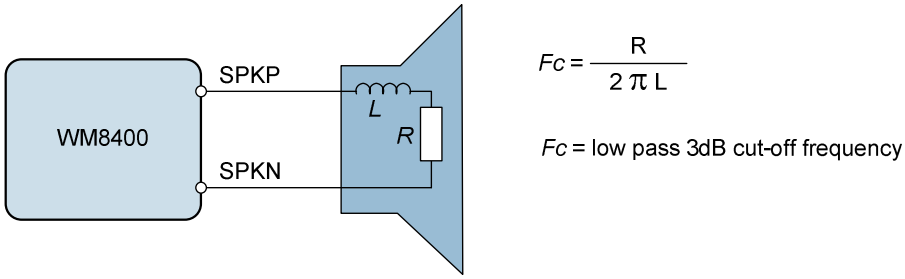


Figure 105 Speaker Equivalent Circuit for Filterless Operation

For filterless Class D operation, it is important to ensure that a speaker with suitable inductance is chosen. For example, if we know the speaker impedance is 8Ω and the desired cut-off frequency is 20kHz, then the optimum speaker inductance may be calculated as:

$$L = \frac{R}{2\pi Fc} = \frac{8\Omega}{2\pi * 20kHz} = 64\mu H$$

It should be noted, however, that a loudspeaker inductance will not be constant across the relevant frequencies for Class D operation (up to and beyond the Class D switching frequency). Care should be taken to ensure that the cut-off frequency of the loudspeaker's filtering is low enough to suppress the high frequency energy of the Class D switching and, in so doing, to prevent speaker damage. The Class D outputs of the WM8400 operate at much higher frequencies than is recommended for most speakers, and it must be ensured that the cut-off frequency is low enough to protect the speaker.

DC-DC CONVERTER COMPONENT SELECTION

The DC-DC Converters use an integral loop compensation circuit, requiring external components to be connected. The recommended external component connections are illustrated in Figure 106.

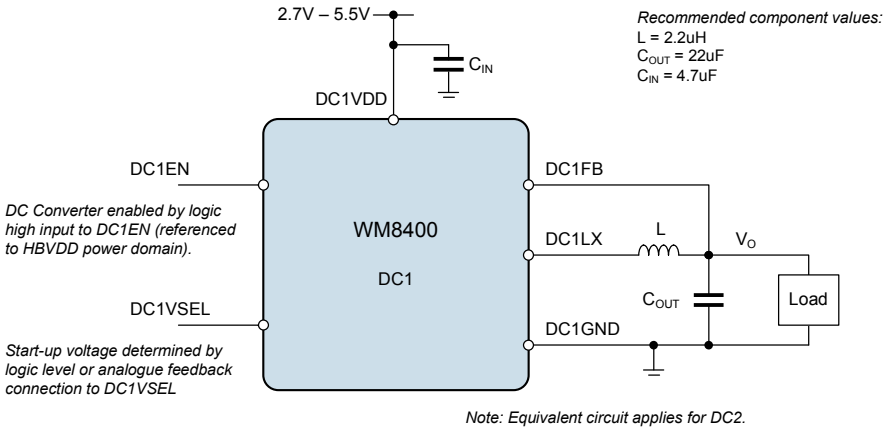


Figure 106 DC-DC Converter External Components

When selecting suitable capacitors, is it imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. It should be noted that some components' capacitance changes significantly depending on the DC voltage applied. Ceramic X7R or X5R types are recommended.

The choice of output capacitor for DC-DC1 and DC-DC2 varies depending on the required transient response. A value of 22µF is recommended in the first instance. Larger values (up to 47µF) may be required for optimum performance under large load transient conditions. Smaller values (down to 10µF) may be sufficient for a steady load in some applications.

For layout and size reasons, users may choose to implement large values of output capacitance by connecting two or more capacitors in parallel.

To ensure stable operation, the register fields DC1_CAP and DC2_CAP must be set according to the output capacitance, as detailed in Table 107.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R71 (47h) DCDC1 Control 2	15:14	DC1_CAP	01	DC-DC1 Output Capacitor 00 = Reserved 01 = 10µF 10 = 22µF 11 = 47µF
R73 (49h) DCDC2 Control 2	15:14	DC2_CAP	01	DC-DC2 Output Capacitor 00 = Reserved 01 = 10µF 10 = 22µF 11 = 47µF

Table 107 Register Control for DC-DC1 and DC-DC2 Output Capacitor

When selecting a suitable output inductor, the inductance value and the saturation current must be compatible with the operating conditions of the converter.

The magnitude of the inductor current ripple is dependant on the inductor value and can be determined by the following equation:

$$\triangle I_L = \frac{V_{OUT} \cdot (1 - (V_{OUT} / V_{IN}))}{L \cdot F_{SW}}$$

$\triangle I_L$ = Inductor ripple current
V_{OUT} = Output voltage
V_{IN} = Input voltage
L = Inductance
F_{SW} = Switching frequency (2MHz)

As a minimum requirement, the DC current rating should be equal to the maximum load current plus one half of the inductor current ripple:

$$I_{Lpeak} = I_{OUTmax} + (\triangle I_L / 2)$$

I_{Lpeak} = Inductor peak current
I_{OUTmax} = Maximum load current
$\triangle I_L$ = Inductor ripple current

To be suitable for the application, the chosen inductor must have a saturation current that is higher than the peak inductor current given by the above equation. To maximise the converter efficiency, the inductor should also have a low DC Resistance (DCR), resulting in minimum conduction losses. Care should also be taken to ensure that the inductor is effective at the applicable operating temperature.

Wolfson recommends the following external components for use with DC-DC Converters 1 and 2. Note that the choice of output capacitor should be determined as described above.

COMPONENT	VALUE	PART NUMBER	SIZE
L	2.2µH	Murata LQM31PN2R2M00 (0.9A)	1206
C_{OUT}	22µF	Murata GRM21BR60J226M	0805
C_{IN}	4.7µF	Murata GRM188R60J475KE19D	0603

Table 108 Recommended External Components - DC-DC1 and DC-DC2

LDO REGULATOR COMPONENT SELECTION

An input and output capacitor are recommended for each LDO Regulator. The recommended connections are illustrated in Figure 107.

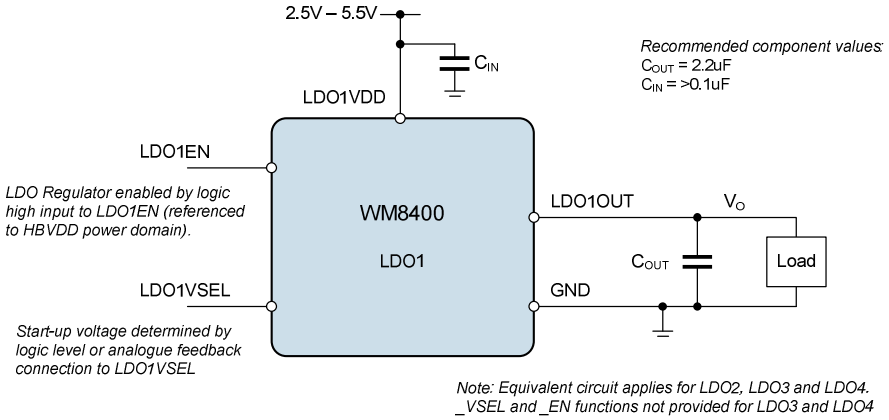


Figure 107 LDO Regulator External Components

When selecting suitable capacitors, is it imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. Ceramic X7R or X5R types are recommended.

Wolfson recommends the following external components for use with LDO Regulators 1, 2, 3 and 4. Note that larger capacitors will improve load transient response and power supply rejection. A maximum of 10µF is possible at the output; a maximum of 1µF is possible at the input.

COMPONENT	VALUE	PART NUMBER	SIZE
C_{OUT}	4.7µF	Murata GRM188R60J47KE19D	0603
C_{IN}	1µF	Murata GRM155R60J105KE19D	0402

Table 109 Recommended External Components - LDO1, LDO2, LDO3 and LDO4

CDELAY COMPONENT SELECTION

A capacitor between CDELAY and GND determines the Reset Timer duration. This timer sets the delay between the RSTTRIG input being set high and the NRST output being set high.

The minimum capacitance 10nF results in a Reset Timer duration of 240µs.

The maximum capacitance 10µF results in a Reset Timer duration of 240ms.

When selecting a suitable CDELAY capacitor, this should be compatible with the typical charging current of 50µA.

The ground connection for the capacitor should be returned directly to the main system ground (GND).

RIREF COMPONENT SELECTION

A 100kΩ resistor is required between RIREF and AGND. The value of this component impacts on the device power consumption and also on the internal oscillator operation and CDELAY time. It is recommended that only a 100kΩ resistor is used.

PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the WM8400 device as possible, with current loop areas kept as small as possible. Specific factors relating to Class D loudspeaker connection and the Power Management (DC-DC Converters and LDO Regulators) are detailed below.

CLASS D LOUDSPEAKER CONNECTION

Long, exposed PCB tracks or connection wires will emit EMI. The distance between the WM8400 and the loudspeaker should therefore be kept as short as possible. Where speakers are connected to the PCB via a cable form, it is recommended that a shielded twisted pair cable is used, with a minimum of 90% shield coverage. The shield should be connected to the main system, with care taken to ensure ground loops are avoided.

Further reduction in EMI can be achieved using PCB ground (or VDD) planes and also by using passive LC components to filter the Class D switching waveform. When passive filtering is used, low ESR components should be chosen in order to minimise the series resistance between the WM8400 and the speaker, maximising the power efficiency.

LC passive filtering will usually be effective at reducing EMI at frequencies up to around 30MHz. To reduce emissions at higher frequencies, ferrite beads can also be used. These should be positioned as close to the device as possible.

These techniques for EMI reduction are illustrated in Figure 108.

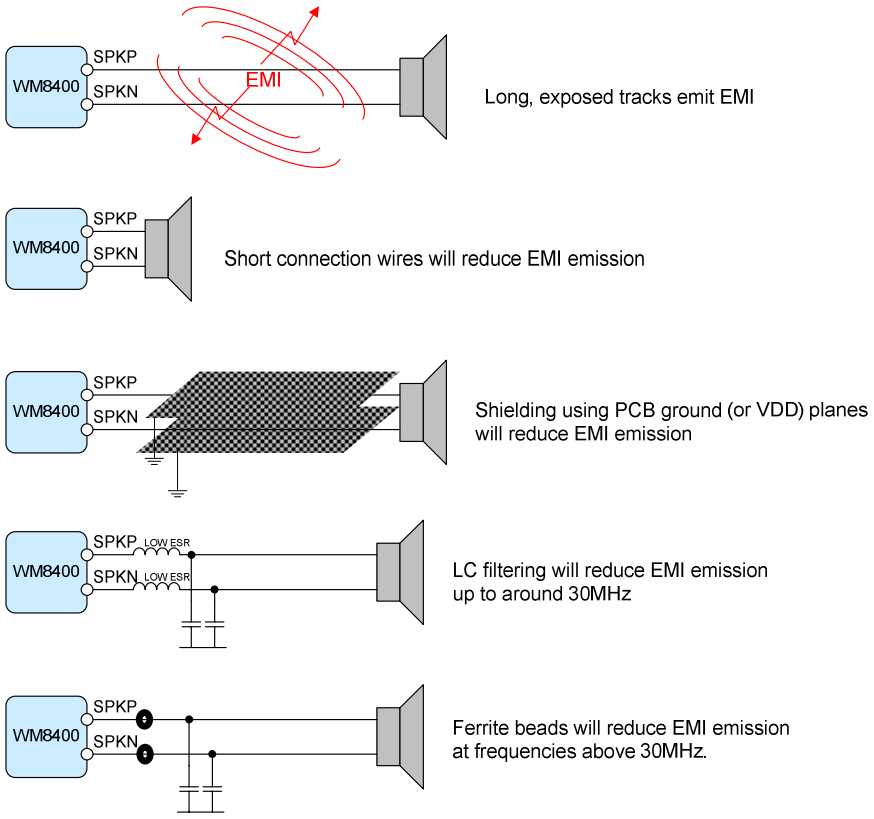


Figure 108 EMI Reduction Techniques

POWER MANAGEMENT (DC-DC / LDO CONNECTIONS)

The tracking and component layout associated with the DC Converters and LDO Regulators is particularly important, as the ripple currents in these circuits can be prone to coupling into other circuits.

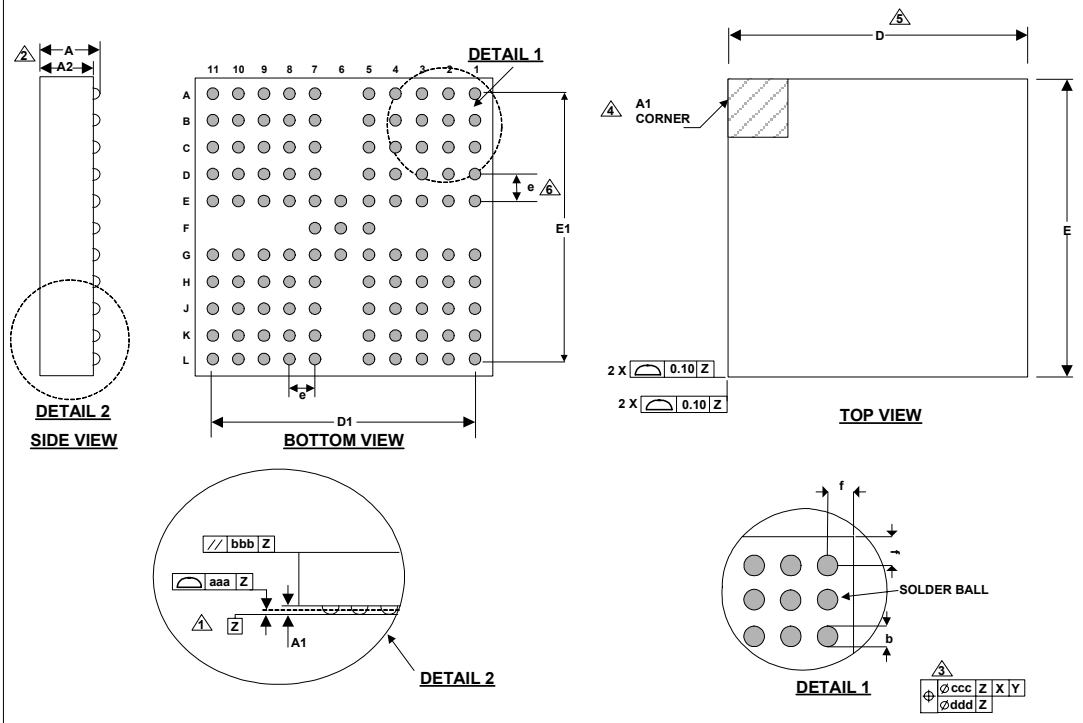
Ripple current can flow from a DC-DC converter input capacitor, through the WM8400 to the output capacitor and back to the input through the ground trace. It is therefore advisable to keep all such tracking loops as small as possible.

A single load connection point should be used at the output of each DC Converter or LDO Regulator. A 'star' connection point should be provided for the ground connection to each DC Converter or LDO Regulator; these should connect to the main system ground as close to the chip as possible.

High current PCB tracks for the Power Management circuits should be short and wide, as far as possible. All Power Management tracks should be kept on the component side of the PCB in order to avoid impedance through vias.

PACKAGE DIMENSIONS

B: 105 BALL BGA PLASTIC PACKAGE 6 x 6 x 0.94 mm BODY, 0.50 mm BALL PITCH **DM055.B**



Symbols		Dimensions (mm)		
	MIN	NOM	MAX	NOTE
A	0.83	0.94	1.05	
A1	0.20	0.24	0.28	
A2	0.63	0.70	0.77	
b	0.25	0.30	0.35	
D	5.90	6.00	6.10	
D1		5.00 BSC		
E	5.90	6.00	6.10	
E1		5.00 BSC		
e		0.50 BSC		6
f	0.40	0.50	0.60	
Tolerances of Form and Position				
aaa		0.08		
bbb		0.10		
ccc		0.15		
ddd		0.05		
REF:		JEDEC, MO-195		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. DIMENSION 'b' IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -Z-.
4. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
6. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
8. FALLS WITHIN JEDEC, MO-195

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