WM8351

Wolfson AudioPlus™ Stereo CODEC with Power Management

DESCRIPTION

The WM8351 is an integrated audio and power management subsystem which provides a cost effective, single-chip solution for portable audio and multimedia systems.

The integrated audio CODEC provides all the necessary functions for high-quality stereo recording and playback. Programmable on-chip amplifiers allow for the direct connection of headphones and microphones with a minimum of external components. A programmable low-noise bias voltage is available to feed one or more electret microphones. Additional audio features include programmable high-pass filter in the ADC input path.

The WM8351 includes four programmable DC-DC converters, four low-dropout (LDO) regulators and a current limit switch to generate suitable supply voltages for each part of the system, including the integrated audio CODEC as well as off-chip components such as a digital core and I/O supplies, and LED lighting. An additional on-chip regulator maintains the backup power for always-on functions. The WM8351 can be powered by a lithium battery, by a wall adaptor or USB.

An on-chip battery charger supports both trickle charging and fast (constant current, constant voltage) charging of single-cell lithium batteries. The charge current, termination voltage, and charger time-out are programmable to suit different types of batteries.

Internal power management circuitry controls the start-up and shutdown sequencing of clocks and supply voltages. It also detects and handles conditions such as under-voltage, extreme temperatures, and deeply discharged or defective batteries, with a minimum of software involvement.

A programmable constant-current sink is available for driving LED strings, e.g. for display backlights or photo-flash applications, in a highly power-efficient way. Additional RGB LEDs can be driven through GPIO pins.

The WM8351 includes a 32.768kHz crystal oscillator, an internal RC oscillator, a real-time clock (RTC) and an alarm function capable of waking up the system. Internal circuitry can generate all clock signals required to start up the device.

The master clock for the audio CODEC can be input directly, or may be generated internally using an integrated, low power Frequency Locked Loop (FLL).

To extend battery life, fine-grained power management enables each function in the WM8351 to be independently powered down through the control interface. The WM8351 forms part of the Wolfson AudioPlus™ series of audio and power management solutions.

FEATURES

Stereo Hi-Fi CODEC

- DAC SNR 95dB ('A' weighted @ 48kHz), THD –81dB
- ADC SNR 95dB ('A' weighted @ 48kHz), THD –83dB
- 40mW on-chip headphone driver with 'capless' option
- 16Ω headphone load: THD -72dB, Po = 20mW
- 2 differential microphone inputs with low-noise bias voltage and programmable preamps
- Programmable high-pass filter for ADC
- Microphone and Headphone detection
- Auxiliary inputs for analogue signals
- Sample rates: 8, 11.025, 16, 22.05, 24, 32, 44.1 or 48kHz

System Control

- Support for 2-wire or 3-/4-wire Control Interface
- Handles power sequencing, reset signals and fault conditions
- Autonomous power source selection (battery, wall adaptor or USB bus)
- Total current drawn from USB bus is limited to comply with USB 2.0 standard and USB OTG supplement

Supply Generation

- 1 x DC-DC Buck Converter (0.85V - 3.4V, Up to 1A)
- 2 x DC-DC Buck Converters (0.85V - 3.4V, Up to 500mA)
- 1 x DC-DC Boost Converter (5V - 20V, 40 to 200mA)
- 4 x LDO voltage regulators (0.9V - 3.3V, 150mA)

LED Drivers

- Programmable constant-current sink, suitable for screen backlight or white LED photo flash
- 3 open-drain outputs for RGB LEDs

Battery Charger

- Single-cell Li-Ion / Li-Pol battery charger
- Thermal protection for charge control; temperature monitoring available for thermal regulation
- LED outputs to indicate charge status and fault conditions

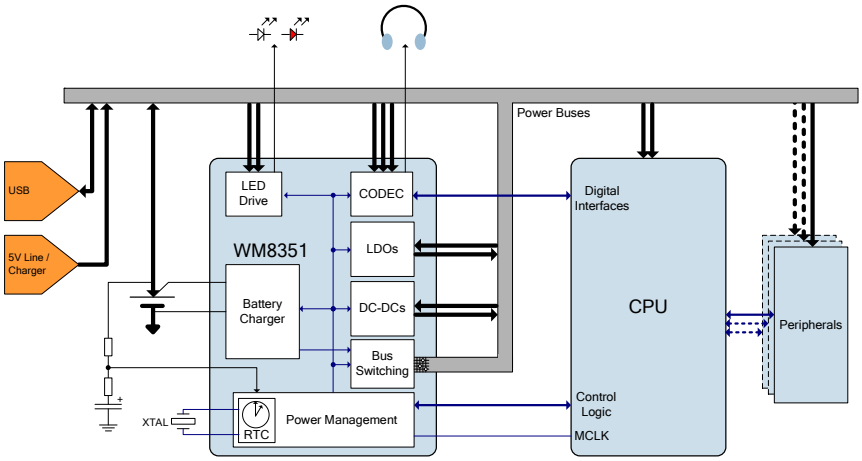
Additional Features

- "Always on" RTC with wake-up alarm
- Watchdog timer
- Up to 13 configurable GPIO pins
- On-chip crystal oscillator and internal RC oscillator
- Low power FLL supporting wide range of input clocks
- 7x7mm, 129 BGA package, 0.5mm ball pitch

APPLICATIONS

- Portable Audio and Media players
- Portable Navigation Devices
- Portable systems powered by single-cell lithium batteries

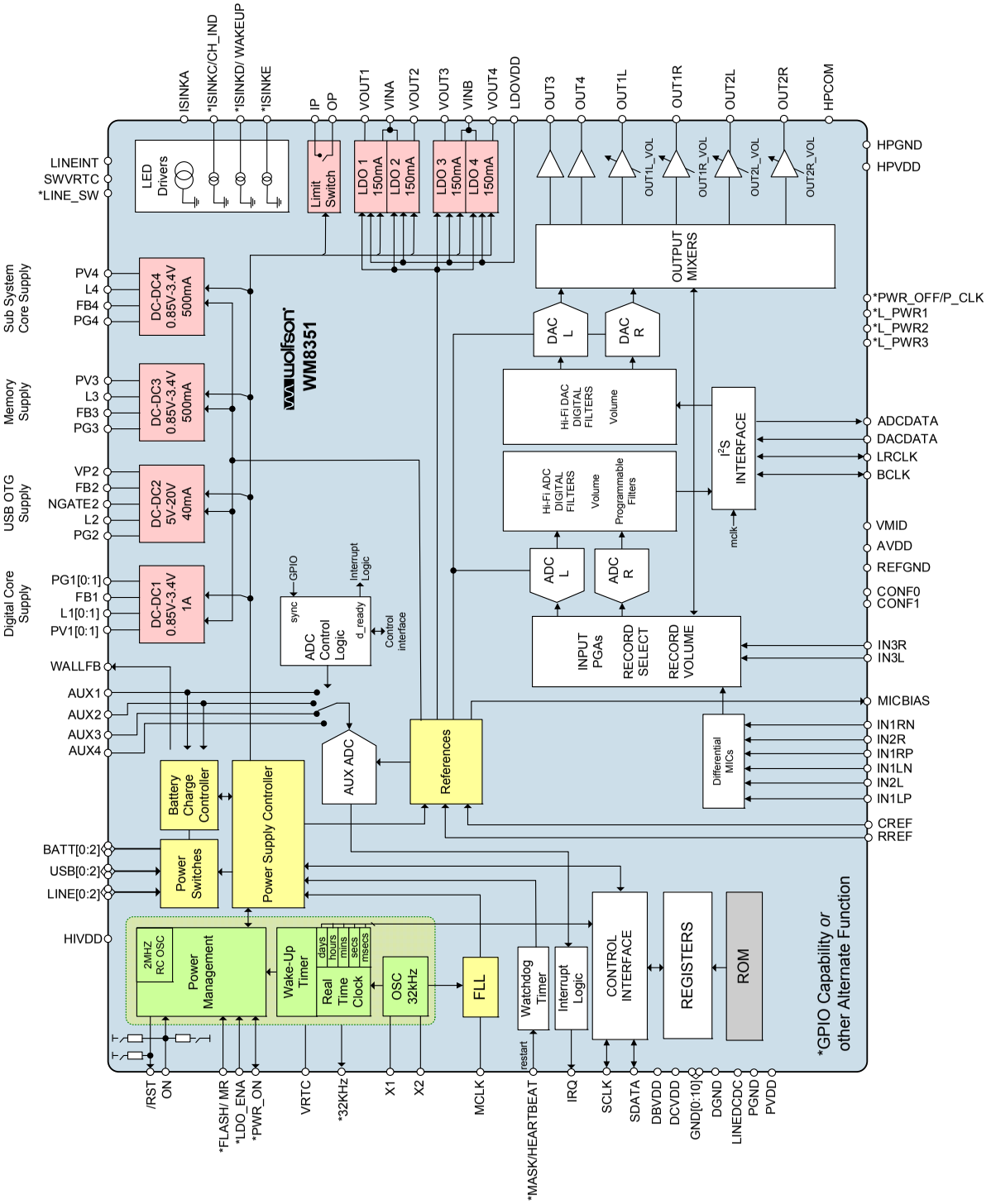
TYPICAL APPLICATIONS



The WM8351 is a complete audio and power management solution for portable media devices. The device incorporates three programmable step-down switching regulators, a step-up switching regulator, a full-featured battery charger, four Low Drop-Out (LDO) voltage regulators which can also serve as hot-swap outputs, a backup supply regulator, a programmable white LED driver, a Real-Time Clock (RTC) alongside a 32.768kHz (32kHz) oscillator capable of operating from a backup battery, a 12-bit auxiliary ADC for precise measurements, a ROM-programmable power management state machine and numerous protection features all in a single 7x7mm BGA package. When only battery power is available, a battery switch provides power to all switching regulators (and some other internal modules). When external power is applied (eg. from USB or Wall adapter), the WM8351 seamlessly transitions from battery power (a single-cell Lithium battery) to the applicable external supply. The battery charger is then activated, all internal power for the device is drawn from the appropriate external power source and the battery is disconnected from the load. Maximum battery charge current and charge time are programmable. The USB power manager provides accurate current limiting for the USB pin under all conditions. The hot-swap outputs (LDOs in current-limited 'Switch Mode' operation) are ideal for powering memory cards and other devices that can be inserted while the system is fully powered.

The integrated Hi-Fi stereo CODEC incorporates preamps and a low-noise bias voltage for differential microphones, and flexible pseudo-differential drivers for headphone and differential/single-ended line outputs. External component requirements are reduced as no separate microphone or headphone amplifiers are required. Digital filter options are available in the ADC and DAC paths, to cater for application filtering. The WM8351 is capable of operating without any external clock, as it can derive all required clocks from its internal crystal oscillator, RC clock, and Frequency Locked Loop. An external low jitter clock may be required in some applications for high performance audio.

BLOCK DIAGRAM



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1 PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	DNC	DNC	OP	PV1	L1	PG1	DNC	DNC	DNC	DNC	GPIO12	FB2	PG2
B	DNC	DNC	IP	PV1	L1	PG1	DNC	DNC	DNC	PVDD	GPIO10	NGATE2	VP2
C	L4	PG4	FB4	DNC	LINEDCDC	FB1	GND	GND	AUX4	GPIO11	PGND	PG3	L2
D	PV4	BATT	HIVDD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	FB3	PV3	L3
E	BATT	BATT	WALLFB	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ISINKA	DNC	SINKGND
F	LINE	LINE	LINE	N/A	N/A	GND	GND	GND	N/A	N/A	VOUT4	LDOVDD	VINB
G	USB	USB	USB	N/A	N/A	GND	GND	GND	N/A	N/A	VOUT2	VOUT3	VINA
H	VRTC	LINEINT	CREF	N/A	N/A	GND	GND	GND	N/A	N/A	AUX1	VOUT1	AUX3
J	CONF0	X1	RREF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	OUT1R	HPCOM	AUX2
K	CONF1	ON	X2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	OUT1L	OUT4	HPVDD
L	GPIO0	/RST	SWVRTC	IRQ	GPIO5	GPIO8	GPIO9	BCLK	LRCLK	IN3L	IN1LN	OUT3	HPGND
M	GPIO2	GPIO1	SDA	GPIO6	DGND	MCLK	ADCDATA	AVDD	IN3R	INL2	MICBIAS	OUT2R	OUT2L
N	GPIO3	SCL	GPIO4	GPIO7	DCVDD	DBVDD	DACDATA	REFGND	VMID	IN1LP	INR2	IN1RP	IN1RN

7mm x 7mm BGA

Notes: Pin names beginning with a lower-case "n" indicate that the pin is active low.
Colour coding indicates function of pins in typical usage:

- DC-DC converters
- LDO voltage regulators
- Power management functions
- Analogue pins for audio codec
- Digital pins for audio codec
- Quiet ground
- Others

2 ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8351CGEB/V	-25°C to +85°C	129-ball BGA (7 x 7 mm) (Pb-free)	MSL3	260°C
WM8351CGEB/RV	-25°C to +85°C	129-ball BGA (7 x 7 mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 2,200

3 PIN DESCRIPTION

Notes:

Pins are listed in alphabetical order by name.

NAME	LOCATION(S)	TYPE	POWER DOMAIN	DESCRIPTION
ADCDATA	M7	Digital Output	DBVDD	Digital audio output (typically from on-chip audio ADC to external IC)
AUX1	H11	Analogue Input	LINE	Auxiliary ADC input AUX1 (Special function for connection to temperature-sensing NTC resistor in battery pack)
AUX2	J13	Analogue Input	LINE	Auxiliary ADC input AUX2
AUX3	H13	Analogue Input	LINE	Auxiliary ADC input AUX3
AUX4	C9	Analogue Input	LINE	Auxiliary ADC input AUX4
AVDD	M8	Supply		Analogue supply for audio CODEC
BATT	E1, E2, D2	Analogue I/O		Main battery power connection (can draw power or charge battery)
BCLK	L8	Digital I/O	DBVDD	Bit clock signal for digital audio interface
CREF	H3	Analogue Output	VRTC	Decoupling for VREF reference voltage (connect capacitor here)
CONF0	J1	Digital Input	VRTC	Start-up configuration pin 0
CONF1	K1	Digital Input	VRTC	Start-up configuration pin 1
DACDATA	N7	Digital Input	DBVDD	Digital audio input (typically from external IC to on-chip audio DAC)
DCVDD	N5	Supply		Digital core supply; powers digital core of audio CODEC
DBVDD	N6	Supply		Digital I/O buffer supply; powers digital audio interface, control interface and pins GPIO4 to GPIO9
DGND	M5	Supply		Digital ground; return path for DCVDD and DBVDD supplies
FB1	C6	Analogue Input	PV1	DC-DC1 feedback pin
FB2	A12	Analogue Input	VP2	DC-DC2 feedback pin
FB3	D11	Analogue Input	PV3	DC-DC3 feedback pin
FB4	C3	Analogue Input	PV4	DC-DC4 feedback pin
GND	F6, F7, F8, G6, G7, G8, H6, H7 H8, C7, C8	Supply		Quiet ground connection for audio CODEC. Note that DC-DC Converters use a separate ground connection.
GPIO0	L1	Digital I/O	VRTC	General Purpose Input/Output pin 0
GPIO1	M2	Digital I/O	VRTC	General Purpose Input/Output pin 1
GPIO2	M1	Digital I/O	VRTC	General Purpose Input/Output pin 2
GPIO3	N1	Digital I/O	VRTC	General Purpose Input/Output pin 3
GPIO4	N3	Digital I/O	DBVDD	General Purpose Input/Output pin 4
GPIO5	L5	Digital I/O	DBVDD	General Purpose Input/Output pin 5
GPIO6	M4	Digital I/O	DBVDD	General Purpose Input/Output pin 6
GPIO7	N4	Digital I/O	DBVDD	General Purpose Input/Output pin 7
GPIO8	L6	Digital I/O	DBVDD	General Purpose Input/Output pin 8
GPIO9	L7	Digital I/O	DBVDD	General Purpose Input/Output pin 9
GPIO10	B11	Digital I/O	LINE	General Purpose Input/Output pin 10
GPIO11	C10	Digital I/O	LINE	General Purpose Input/Output pin 11
GPIO12	A11	Digital I/O	LINE	General Purpose Input/ Output pin 12
HIVDD	D3	Analogue Output		Analogue output from power management unit which determines highest supply from Line, Battery or USB.
HPCOM	J12	Analogue Input	HPVDD	Headphone output amplifier noise compensation input
HPGND	L13	Supply	HPVDD	Headphone ground; return path for HPVDD supply
HPVDD	K13	Supply		Headphone supply – powers the analogue outputs OUT1L, OUT1R, OUT2L, OUT2R, OUT3 and OUT4
IN1LN	L11	Analogue Input	AVDD	Inverting input for left microphone channel

NAME	LOCATION(S)	TYPE	POWER DOMAIN	DESCRIPTION
IN1LP	N10	Analogue Input	AVDD	Non-inverting input 1 for left microphone channel
IN1RN	N13	Analogue Input	AVDD	Inverting input for right microphone channel
IN1RP	N12	Analogue Input	AVDD	Non-inverting input 1 for right microphone channel
IN2L	M10	Analogue Input	AVDD	Non-inverting input 2 for left microphone channel
IN2R	N11	Analogue Input	AVDD	Non-inverting input 2 for right microphone channel
IN3L	L10	Analogue Input	AVDD	Auxiliary input for analogue audio signals (left channel)
IN3R	M9	Analogue Input	AVDD	Auxiliary input for analogue audio signals (right channel)
IP	B3	Analogue Input		Power input to current limit switch
ISINKA	E11	Analogue Output	LDOVDD	Constant-current LED driver A
L1	A5, B5	Analogue I/O	PV1	DC-DC1 inductor connection
L2	C13	Analogue I/O	VP2	DC-DC2 inductor connection
L3	D13	Analogue I/O	PV3	DC-DC3 inductor connection
L4	C1	Analogue I/O	PV4	DC-DC4 inductor connection
LDOVDD	F12	Supply		LDO amplifier supply voltage
LINEDCDC	C5	Supply		Supply connection for DC-DC 1 and 4 control circuits
LINEINT	H2	Supply		Supply connection for Internal Reference circuits
LINE	F1, F2, F3	Supply		LINE supply connection
LRCLK	L9	Digital I/O	DBVDD	Word clock (left/right clock) signal for digital audio interface
MCLK	M6	Digital I/O	DBVDD	Master Clock (may be generated internally or externally)
MICBIAS	M11	Analogue Output	AVDD	Low-noise bias voltage for condenser microphones (connect decoupling capacitor here)
NGATE2	B12	Analogue Output	VP2	DC-DC2 connection to gate of external power FET
IRQ	L4	Digital Output open-drain	DBVDD	Interrupt signal from WM8351 to host processor
ON	K2	Digital Input	VRTC	Connection for power-on switch
/RST	L2	Digital Output open-drain	DBVDD	System Reset Signal (active low)
OP	A3	Analogue Output		Power output from current limit switch
OUT1L	K11	Analogue Output	AVDD	Left channel analogue audio output 1
OUT2L	M13	Analogue Output	AVDD	Left channel analogue audio output 2
OUT1R	J11	Analogue Output	AVDD	Right channel analogue audio output 1
OUT2R	M12	Analogue Output	AVDD	Right channel analogue audio output 2
OUT3	L12	Analogue Output	AVDD	Analogue audio output 3 (or pseudo-ground output for capacitor-less headphone outputs)
OUT4	K12	Analogue Output	AVDD	Analogue audio output 4
PG1	A6, B6	Supply		DC-DC1 power ground
PG2	A13	Supply		DC-DC2 power ground
PG3	C12	Supply		DC-DC3 power ground
PG4	C2	Supply		DC-DC4 power ground
PGND	C11	Supply		Ground connection
PV1	A4, B4,	Supply		DC-DC1 line or battery power input
PV3	D12	Supply		DC-DC3 line or battery power input
PV4	D1	Supply		DC-DC4 line or battery power input
PVDD	B10	Supply		Supply connection for DC-DC 2 and 3 control circuits
REFGND	N8	Supply		Reference ground for audio ADC and DAC
RREF	J3	Analogue Output		Connection for external 100kΩ current reference resistor
SCLK	N2	Digital Input	DBVDD	Clock signal for 2-wire serial control interface (5V Tolerant)
SDATA	M3	Digital I/O	DBVDD	Data line for 2-wire serial control interface (5V Tolerant)
SINKGND	E13	Supply		Ground connection for ISINKA

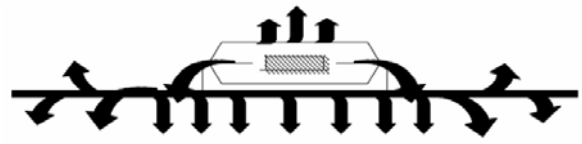
NAME	LOCATION(S)	TYPE	POWER DOMAIN	DESCRIPTION
SWVRTC	L3	Analogue Output	VRTC	Switchable VRTC output. Typically used for battery temperature monitoring
USB	G1, G2, G3	Supply		Connection to USB power rail
VINA	G13	Supply		Input to voltage regulators LDO1 and LDO2
VINB	F13	Supply		Input to voltage regulators LDO3 and LDO4
VMID	N9	Analogue I/O	AVDD	Reference voltage (normally AVDD/2) for audio CODEC (connect capacitor here)
VOUT1	H12	Analogue Output	VINA	Output of voltage regulator LDO1
VOUT2	G11	Analogue Output	VINA	Output of voltage regulator LDO2
VOUT3	G12	Analogue Output	VINB	Output of voltage regulator LDO3
VOUT4	F11	Analogue Output	VINB	Output of voltage regulator LDO4
VP2	B13	Supply		DC-DC2 power input
VRTC	H1	Supply		Backup power connection (WM8351 can draw power from this pin or re-charge the backup power source)
WALLFB	E3	Analogue Input	LINE	Connection to Wall feedback
X1	J2	Analogue Input	VRTC	Connection for 32.768kHz crystal (input to oscillator from crystal) or 32.768kHz external clock input (when not using crystal)
X2	K3	Analogue Output	VRTC	Connection for 32.768kHz crystal (output from oscillator to crystal)
DNC	A1, A2, A7, A8, A9, A10, B1, B2, B7, B8, B9, C4, E12			Do Not Connect

4 THERMAL CHARACTERISTICS

Thermal analysis must be performed in the intended application to prevent the WM8351 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the nine central GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package leads to PCB (conduction).



The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated by the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air.
- For WM8351, Θ_{JA} = 32°C/W

The junction temperature T_J is given by $T_J = T_A + T_R$

1. T_A, is the ambient temperature.

The worst case conditions are when the WM8351 is operating in a high ambient temperature, with low supply voltage, high duty cycle and high output current. Under such conditions, it is possible that the heat dissipated could exceed the maximum junction temperature of the device. Care must be taken to avoid this situation. An example calculation of the junction temperature is given below.

- P_D = 1W (example figure)
- Θ_{JA} = 32°C/W
- $T_R = P_D * \Theta_{JA}$ = 32°C
- T_A = 85°C (example figure)
- $T_J = T_A + T_R$ = 117°C

The minimum and maximum operating junction temperatures for the WM8351 are quoted in Section 5. The maximum junction temperature is 125°C. Therefore, the junction temperature in the above example is within the operating limits of the WM8351.

5 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8351 has been classified as MSL3.

CONDITION	MIN	MAX
BATT, LINE and USB voltage	-0.3V	+7V
Input voltage for LDO regulators (pins VINA, VINB)	-0.3V	+7V
Analogue supply voltages (AVDD, HPVDD)	-0.3V	+4.5V
Digital supply voltages (DCVDD, DBVDD)	-0.3V	+4.5V
Voltage range for CODEC analogue inputs	-0.3V	AVDD + 0.3V
Voltage range for digital inputs	-0.3V	DBVDD + 0.3V
Master Clock Frequency (When MCLK_DIV set to divide by 2)		37MHz
Operating Temperature Range, T_A	-25°C	+85°C
Junction Temperature, T_J	-20°C	+125°C
Thermal Impedance Junction to Ambient, θ_{JA}		32°C/W
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-65°C	+150°C
Soldering temperature (10 seconds)		+260°C
Note: These ratings assume that all ground pins are at 0V.		

6 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Digital Supply Range (Core)	DCVDD	1.71		3.6	V
Digital Supply Range (Buffer)	DBVDD	1.71		3.6	V
Headphone Supply Range	HPVDD	2.5		3.6	V
Analogue Supply Range	AVDD	2.5		3.6	V
Line Input Source	LINE	2.95		5.5	V
Battery Input Source	BATT	2.95		4.2	V
USB Input Source	USB	4.75		5.25	V
LDO Input Source	VINA, VINB	0		5.5	V
Ground	GND, PGND, DGND, HPGND, REFGND, PG1, PG2, PG3, PG4		0		V

7 ELECTRICAL CHARACTERISTICS

7.1 HI-FI AUDIO CODEC

Test Conditions

DCVDD = 1.8V, AVDD = HPVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Preamp Inputs (IN1LP, IN1LN, IN1RP, IN1RN)						
Full-scale Input Signal Level (0dB) – note this changes with AVDD	V_{INFS}			1 0		V rms dBV
Mic preamp equivalent input noise	At 35.25dB gain			150		µV
Input resistance	R_{MICIN}	Gain set to 35.25dB		2.3		kΩ
Input resistance	R_{MICIN}	Gain set to 0dB		64		kΩ
Input resistance	R_{MICIN}	Gain set to -12dB		101		kΩ
Input Capacitance	C_{MICIN}			2		pF
Recommended decoupling cap	C_{DECOUP}			0.33		µF
MIC Programmable Gain Amplifier (PGA)						
Programmable Gain			-12		35.25	dB
Programmable Gain Step Size		Monotonic		0.75		dB
Mute Attenuation				-90		dB
Selectable Input Gain Boost (0/+20dB)						
Gain Boost			0		20	dB
Auxiliary Analogue Inputs (IN3L, IN3R)						
Full-scale Input Signal Level (0dB) – note this changes with AVDD	V_{INFS}			1.0 0		Vrms dBV
PGA gain range to summer			-12		+6	dB
PGA step size to summer				3		dB
Input Resistance	R_{AUXIN}			32		kΩ
Input Capacitance	C_{AUXIN}			10		pF
Analogue to Digital Converter (ADC)						
Signal to Noise Ratio (Note 1, 2)		A-weighted, 0dB gain	86	95		dB
Total Harmonic Distortion (Note 4)		-2dBV Input	-75	-83		dB
Digital to Analogue Converter (DAC) to Line-Out (OUT1L, OUT1R with 10kΩ / 50pF load)						
Full-scale output		PGA gains set to 0dB		HPVDD/3.3		Vrms
Signal to Noise Ratio (Note 1, 2)	SNR	A-weighted	90	95		dB
Total Harmonic Distortion (Note 3)	THD+N	R_L = 10kΩ full-scale signal	-75	-81		dB
Channel Separation (Note 4)		1kHz signal		89		dB
Output Mixers						
PGA gain range into mixer			-15	0	+6	dB
PGA gain step into mixer				3		dB
Analogue Output PGAs (OUT1L, OUT1R, OUT2L, OUT2R)						
Programmable Gain range			-57	0	+6	dB
Programmable Gain step size		Monotonic		1		dB
Mute attenuation		1kHz, full scale signal		78		dB

Test Conditions

DCVDD = 1.8V, AVDD = HPVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Headphone Output (OUT1L, OUT1R, OUT2L, OUT2R)						
0dB full scale output voltage				HPVDD/3.3		Vrms
Signal to Noise Ratio	SNR	A-weighted	87	96		dB
Total Harmonic Distortion (Note 3)	THD+N	R_L = 16Ω, Po=20mW HPVDD=3.3V	-65	-72		dB
		R_L = 32Ω, Po=20mW HPVDD=3.3V		-71		dB
OUT3/OUT4 outputs (with 10kΩ / 50pF load)						
Full-scale output				HPVDD/3.3		Vrms
Signal to Noise Ratio (Note 1, 2)	SNR	A-weighted	90	97		dB
Total Harmonic Distortion (Note 3)	THD	R_L = 10kΩ full-scale signal	-77	-83		dB
Channel Separation (Note 4)		5kHz signal		80		dB
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	MBVSEL=0		0.9*AVDD		V
		MBVSEL=1		0.75*AVDD		V
Bias Current Source	$I_{MICBIAS}$			3		mA
Output Noise Voltage	Vn	1kHz to 20kHz		24		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OH}-1mA			0.1xDBVDD	V
Frequency Locked Loop (FLL)						
Reference clock frequency	F_{REF}		0.032		22	MHz
Jack Detect						
Detection switch threshold	V_{IH}		0.7xAVDD			V
	V_{IL}				0.3xAVDD	V
HPCOM						
Ground noise rejection	V_{IH}			40		dB
	V_{IL}			40		dB

TERMINOLOGY

1. Signal-to-noise ratio (dB) = SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) = DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (E.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) = THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) = Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

7.2 DC-DC STEP UP CONVERTER ELECTRICAL CHARACTERISTICS

Test Conditions
T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC-DC2						
Input voltage range	V_{IN}	when used as converter	2.7	3.7	5.5	V
		when used as switch	1.2			
Output voltage range	V_{OUT}	by default (needs external component configuration)	V_{IN}		20 (30)	V
USB OTG output voltage	$V_{OUT,USB}$	V_{IN}<4.5V; I_{OUT}<100mA; DC2_FBSRC [1:0]=11		5.0		V
Output current	I_{OUT}	V_{OUT}=30V	0		25	mA
		V_{OUT}=20V (DC2_ILIM_=1)			40 (18)	
		V_{OUT}=5.0V (DC2_ILIM_=1)			170 (100)	
Switch resistance	R_{ON}	V_{IN}=3.3V; V_{OUT}=3.2V; +25°C		0.26		Ω
		V_{IN}=1.8V; V_{OUT}=1.7V; +25°C		0.41		
		V_{IN}=1.2V; V_{OUT}=1.1V; +25°C		0.84		
Maximum switch current	$I_{SW,MAX}$				700	mA
Switching frequency	f_{CLK}			1.0		MHz
Maximum duty cycle	D_{MAX}	V_{IN}=3V; f_{CLK}=1.0MHz		90		%
Efficiency	H	V_{IN}=3.8V; V_{OUT}=20V; I_{OUT}=20mA		75		%
		V_{IN}=3.8V; V_{OUT}=5.0V; I_{OUT}=100mA		88		
Quiescent current	I_{DD}	Shutdown or switch configuration		0.1		uA
		active; no switching		260		
		active; pulse skipping		260		
Regulated feedback voltage	V_{FB}	DC2_FBSRC [1:0] = 00		0.5		V
	V_{CURR}	DC2_FBSRC [1:0] = 01 or 10		0.5		
Undervoltage detect	$V_{FB,UV}$	below feedback voltage		12		%
	$V_{USB,UV}$	DC2_FBSRC [1:0] = 11		4.6		V
Overvoltage detect	$V_{FB,OV}$	above feedback voltage		8		%
	$V_{USB,OV}$	DC2_FBSRC [1:0] = 11		5.4		V
Peak inductor current limit	I_{PK}	V_{IN}=3V; V_{OUT}=90%;		700		mA
		DC2_ILIM_=1		450		
On resistance of NGATE driver	R_{NGATE}	P-Channel FET (I_{PFET}=100mA)		4.6		Ω
		N-Channel FET (I_{NFET}=100mA)		4.9		
Input capacitor	C_{IN}	X5R/X7R dielectric	1.0	2.2		µF
Inductor	L_F		-30%	10	+30%	µH
Inductor current rating	$I_{SAT,Lf}$		500			mA
		DC2_ILIM_=1	320			
Output capacitor	C_{OUT}	DC2_FBSRC [1:0]= 00 or 11; V_{OUT}=5V	3.7	10	22	µF
		DC2_FBSRC [1:0]= 00; V_{OUT}=10V	0.84	2.2	4.7	
		DC2_FBSRC [1:0]= 00; V_{OUT}=20V	0.18	0.47	1.0	
		DC2_FBSRC [1:0]= 01 or 10; V_{OUT}=10V	2.0	4.7	10	
		DC2_FBSRC [1:0]= 01 or 10; V_{OUT}=15V	1.5	2.2	10	
		DC2_FBSRC [1:0]= 01 or 10; V_{OUT}=20V	0.9	1.5	4.7	

7.3 DC-DC STEP DOWN CONVERTER ELECTRICAL CHARACTERISTICS

Test Conditions
V_{IN} = 3.7, V_{OUT} = 1.8V, T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
DC-DC1								
Input Voltage	V_{IN}				2.7	3.7	5.5	V
Output Voltage	V_{OUT}				0.85		3.4	V
VOUT Accuracy	V_{OUT}	V_{IN} = 3.7V V_{OUT} = 0.85V / 1.8V / 3.4V	I_{OUT} = 0.5A	Active		+/- 3.0		%
			I_{OUT} = 0.005A	Sleep		-1.5 +4.5		
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = 2.7V to 5.5V V_{OUT} = 1.8V	I_{OUT} = 0.5A	Active		+/- 0.5		%
			I_{OUT} = 0.1A	Standby		+/- 0.25		
			I_{OUT} = 0.005A	Sleep		+/- 0.4	+/- 0.5	
Load Regulation	$V_{OUT\ LOAD}$	I_{OUT} = 0.001A to 1A		Active		+/- 0.2		%
		I_{OUT} = 0A to 0.1A		Standby		+/- 0.2		
		I_{OUT} = 0A to 0.01A		Sleep		+/- 0.3	+/- 0.5	
Quiescent Current	$I_{Q\ ACTIVE}$	Active (excluding switching losses)				265		µA
	$I_{Q\ STANDBY}$	Standby (excluding switching losses)				115		
	I_{QSLEEP}	Sleep				25		
Shutdown current	I_{SD}					0.01		µA
P-channel On Resistance	R_{DSP}	V_{IN} = 3.7V, $I_{L(n)}$ = 100mA				0.09		Ω
N-channel On Resistance	R_{DSN}	V_{IN} = 3.7V, $I_{L(n)}$ = 100mA				0.167		Ω
P-channel leakage current	I_{LXP}	V_{IN} = 3.7V, L(n) = GND				0.01		µA
N-channel leakage current	I_{LXN}	V_{IN} = 3.7V, L(n) = 3.7V				2.8		µA
Switching Frequency	f_{SW}					2.0		MHz

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
DC-DC3 and DC-DC4								
Input Voltage	V_{IN}				2.7	3.7	5.5	V
Output Voltage	V_{OUT}				0.85		3.4	V
VOUT Accuracy	V_{OUT}	V_{IN} = 3.7V V_{OUT} = 0.85V / 1.8V / 3.4V	I_{OUT} = 0.5A	Active		+/- 3.0		%
			I_{OUT} = 0.005A	Sleep		-1.5 +4.5		
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = 2.7V to 5.5V V_{OUT} = 1.8V	I_{OUT} = 0.25A	Active		+/- 0.4		%
			I_{OUT} = 0.025A (100mA lim)	Standby		+/- 0.18		
			I_{OUT} = 0.005A	Sleep		+/- 0.4	+/- 0.5	
Load Regulation	$V_{OUT\ LOAD}$	I_{OUT} = 1mA to 500mA		Active		+/- 0.5		%
		I_{OUT} = 0A to 0.05A		Standby		+/- 0.2		
		I_{OUT} = 0A to 0.010A		Sleep		+/- 0.3	+/- 0.5	
Quiescent Current	$I_{Q\ ACTIVE}$	Active (excluding switching losses)				318		µA
	$I_{Q\ STANDBY}$	Standby (excluding switching losses)				120		
	$I_{Q\ SLEEP}$	Sleep				25		
Shutdown current	I_{SD}					0.01		µA
P-channel On Resistance	R_{DSP}	V_{IN} = 3.7V, $I_{L(n)}$ = 100mA				0.29		Ω
N-channel On Resistance	R_{DSN}	V_{IN} = 3.7V, $I_{L(n)}$ = 100mA				0.2		Ω
P-channel leakage current	I_{LXP}	V_{IN} = 3.7V, L(n) = GND				0.02		µA
N-channel leakage current	I_{LXN}	V_{IN} = 3.7V, L(n) = 3.7V				1.4		µA
Switching Frequency	f_{SW}					2.0		MHz

7.4 LDO REGULATOR ELECTRICAL CHARACTERISTICS

Test Conditions

V_{IN} = 3.7, V_{OUT} = 1.8V, T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO1 to LDO4 (WM8351 in ACTIVE State)						
Input Voltage	VIN	After start-up	1.6	3.7	5.5	V
Output voltage	VOUT*n*		0.9		3.3	V
Regulation Accuracy				+/-3.3%		%
Dropout Voltage		100mA, V_{IN} < 1.8V		200		mV
		100mA, V_{IN} <2.7V		700		
Load current				100	150	mA
Quiescent Current			27		1% of load	µA
Leakage Current				<2.5		µA
Power Supply Rejection Ratio	PSRR	1kHz, V_{OUT} =1.8V, 25mA load		-50		dB
		100Hz				
ON Resistance in switch mode	R_{ON}	LDOn_SWI = 1		2	3.5	Ω
LDO1 (WM8351 in OFF State)						
Output Voltage	VOUT1			0.95 × VOUT1 in ACTIVE		V

7.5 BATTERY CHARGER

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
Wall adaptor voltage	LINE	When charging from wall adaptor	4.0		5.5	V
USB voltage	USB	When charging from USB power rail	4.0		5.5	V
Target voltage		CHG_VSEL=00	4.0	4.05	4.1	V
		CHG_VSEL=01	4.05	4.1	4.15	
		CHG_VSEL=10	4.1	4.15	4.2	
		CHG_VSEL=11	4.15	4.2	4.25	
Defective battery threshold				2.85		V
End of Charge Current	EOC	Programmable in register R168 CHG_EOC_SEL bits		20 to 90		mA
Trickle Charging						
Trickle charge initiation threshold (WM8351 starts trickle charging when battery is below this threshold)				CHG_VSEL - 100mV		V
50mA trickle charge current		CHG_TRICKLE_SEL = 0 (default)		35.9		mA
100mA trickle charge current		CHG_TRICKLE_SEL = 1		78.6		mA
Fast Charging						
Fast charge threshold (WM8351 can only fast-charge if battery is above this threshold)				3.1		V
Maximum fast-charge current	I_{MAX}			750		mA
Backup Battery (VRTC)						
Backup battery charger output. (Note that this backup charger voltage also determines the UVLO threshold.)			2.5	2.7	2.9	V

7.6 CURRENT LIMIT SWITCH

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Maximum input voltage		2.7		LINE	V
On resistance (at 3.3V)			2.0		Ω
Current limit flag threshold			180		mA
Current limit			215		mA
Quiescent current (EN but not ON)			7		µA
Quiescent current (EN and ON)					µA

7.7 LED DRIVERS

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISINKA						
Sink Current		duty cycle = 20%			200	mA
		continuous			40	
ISINKC, ISINKD, ISINKE						
Sink Current					20	mA
Output voltage drop		10mA load		0.8		V

7.8 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO0 to GPIO3						
Input HIGH Level	V_{IH}		0.7×VRTC			V
Input LOW Level	V_{IL}				0.3×VRTC	V
Output HIGH Level	V_{OH}	sinking 2 mA	0.9×VRTC			V
Output LOW Level	V_{OL}	sourcing 2 mA			0.1×VRTC	V
Sink / source current						mA
Pull-up resistance to VRTC	R_{PU}	GPn_PU = 1		310		kΩ
Pull-down resistance	R_{PD}	GPn_PD = 1		225		kΩ
GPIO4 to GPIO9						
Logic levels	See Section 7.9					
Sink / source current						mA
Pull-up resistance to DBVDD	R_{PU}	GPn_PU= 1		220		kΩ
Pull-down resistance	R_{PD}	GPn_PD = 1		144		kΩ
GPIO10 to GPIO12						
Input HIGH Level	V_{IH}		2.0			V
Input LOW Level	V_{IL}				0.9	V
Output HIGH Level	V_{OH}	sinking 2 mA	0.9× LINE			V
Output LOW Level	V_{OL}	sourcing 2 mA			0.1× GPIO_VDD	V
Sink / source current						mA
Pull-up resistance to LINE	R_{PU}	GPn_PU = 1		250		kΩ
Pull-down resistance	R_{PD}	GPn_PD = 1		135		kΩ

7.9 DIGITAL INTERFACES

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA, SCLK, MCLK, BCLK, LRCLK, ADCDATA, DACDATA, GPIO4 to GPIO9						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	sinking 1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	sourcing 1mA			0.1xDBVDD	V

7.10 AUXILIARY ADC

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Input resistance (AUX1,2,3,4, USB, LINE, BATT and CHIPTEMP)	AUXADC_SCALEn [1:0] = 00		∞	∞	∞	Ω
	AUXADC_SCALEn [1:0] = 01			2.2		kΩ
	AUXADC_SCALEn [1:0]= 10		330		660	kΩ
	AUXADC_SCALEn [1:0] = 11		330		440	kΩ
Input Voltage range. AUX1,2,3,4,USB,LINE,BATT and CHIPTEMP (V_{RTC} = 2.7V & V_{LINE} (max)= 5.5V, V_{BG}=1.25V)	AUXADC_SCALEn [1:0] = 01 AUXADC_REF = 0				V_{BG}	V
	AUXADC_SCALEn [1:0] = 01 AUXADC_REF = 1				V_{RTC}	V
	AUXADC_SCALEn [1:0] = 10 AUXADC_REF = 0				2 x V_{BG}	V
	AUXADC_SCALEn [1:0] = 10 AUXADC_REF = 1				2 x V_{RTC}	V
	AUXADC_SCALEn [1:0] = 11 AUXADC_REF = 0				V_{LINE}	V
	AUXADC_SCALEn [1:0] = 11 AUXADC_REF = 1				4 x V_{BG}	V
Input capacitance (AUX1,2,3,4, USB, LINE, BATT and CHIPTEMP)	Input is selected (INPUT_SELECT) and AUXADC_SCALEn [1:0] not = 00			2.08		pF
VRTC quiescent current	AUX_RBMODE = 0, AUXADC_ENA = 1			140		µA
VRTC quiescent current	AUX_RBMODE = 1 AUXADC_ENA = 1			151		µA
LINE_INT quiescent current					<<1	mA
ADCCLK frequency		f_{AUXCLK}	400	470/512	800	kHz
ADC Resolution				12		bits
ADC Conversion Time				13		CLK periods
Aux ADC accuracy	Non-calibrated (calibration possible using the VBG input on AUX3). 1% of this variation due to BG variation over temperature.			2.2		%

8 TYPICAL POWER CONSUMPTION

ADC Master Mode

48kHz

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	3.6	0.000014	0.55	2.3	13.87
3.3	3.3	3.3	1.8	4.46	0.00003	1.085	2.4	22.62
3.6	3.6	3.6	3.6	4.79	0.000028	1.18	5.67	41.90

ADC Master Mode

1kHz Tone 100mVpk-pk

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	3.6	0.00009	0.5	2.14	13.51
3.3	3.3	3.3	1.8	4.4	0.00016	1.02	2.3	22.03
3.6	5.5	3.6	3.6	4.8	0.00008	1.12	5.3	40.39

ADC Master Mode

Pink Noise

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	3.58	0.000004	0.51	2.1	13.41
3.3	3.3	3.3	1.8	4.43	0.00026	1	2.2	21.88
3.6	5.5	3.6	3.6	4.8	0.000085	1.1	5.2	39.96

ADC Slave Mode

44.1kHz

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	3.4	0.00002	0.02	2.2	12.30
3.3	3.3	3.3	1.8	4.2	0.00041	0.05	2.3	18.17
3.6	3.6	3.6	3.6	4.4	0.0004	0.05	5.33	35.21

DAC OUT1 Master Mode

44.1kHz, 10kΩ Load

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	2.97	0.299	0.193	1.69	11.39
3.3	3.3	3.3	1.8	4.14	0.432	0.39	1.78	19.58
3.6	3.6	3.6	3.6	4.54	0.486	0.461	4.28	35.16

48kHz,10kΩ Load

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	2.82	0.3	0.2	2	11.56
3.3	3.3	3.3	1.8	3.94	0.45	0.42	2.12	19.69
3.6	3.6	3.6	3.6	4.33	0.51	0.46	4.9	36.72

DAC OUT1 Master Mode

Pink Noise

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	2.97	2	0.192	2.2	16.52
3.3	3.3	3.3	1.8	4.13	2.6	0.39	2.3	27.64
3.6	5.5	3.6	3.6	4.5	2.9	0.45	5.5	53.57

DAC OUT1 Master Mode

1kHz Tone, 16Ω Load

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	2.9	2.97	0.19	2.2	18.76
3.3	3.3	3.3	1.8	4.1	3.8	0.4	2.3	31.53
3.6	5.5	3.6	3.6	4.5	4.1	0.44	5.4	59.77

1kHz Tone, 10kΩ Load

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	2.97	0.3	0.2	2.17	12.23
3.3	3.3	3.3	1.8	4.14	0.43	0.4	2.3	20.54
3.6	3.6	3.6	3.6	4.5	0.5	0.46	5.4	39.10

DAC OUT1 Slave Mode

44.1 kHz, 10kΩ Load

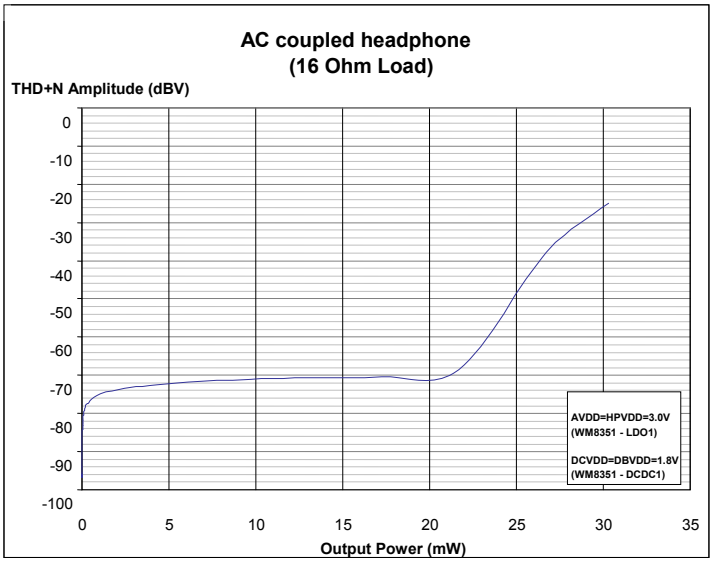
AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	2.8	0.27	0.009	2.1	11.28
3.3	3.3	3.3	1.8	3.6	0.38	0.02	2.3	17.34
3.6	3.6	3.6	3.6	4.1	0.43	0.02	5.2	35.10

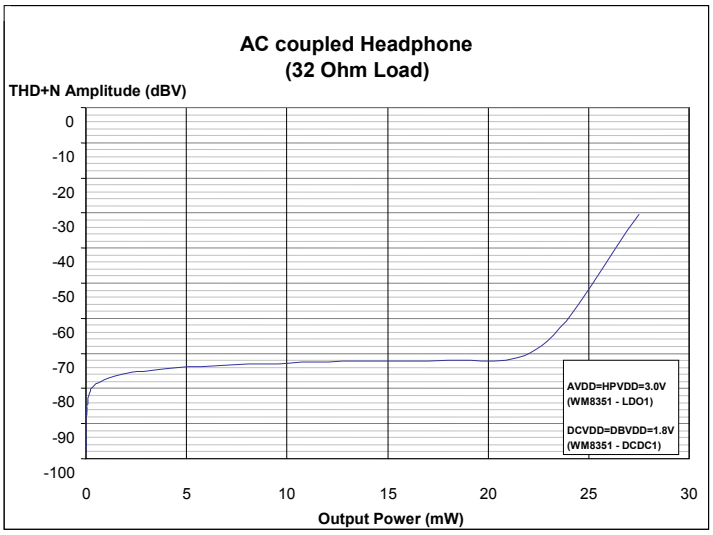
9 TYPICAL PERFORMANCE DATA

9.1 AUDIO CODEC

Typical THD+N performance of the Headphone Drivers is shown below for 16Ω and 32Ω headphone loads. These graphs are derived whilst using the WM8351 Power Management to generate the power supply rails for the audio CODEC. The supply conditions are as follows:

- AVDD = HPVDD = 3.0V, generated by WM8351 LDO1
- DCVDD = DBVDD = 1.8V, generated by WM8351 DC-DC1





9.2 DC-DC CONVERTERS

9.2.1 POWER EFFICIENCY

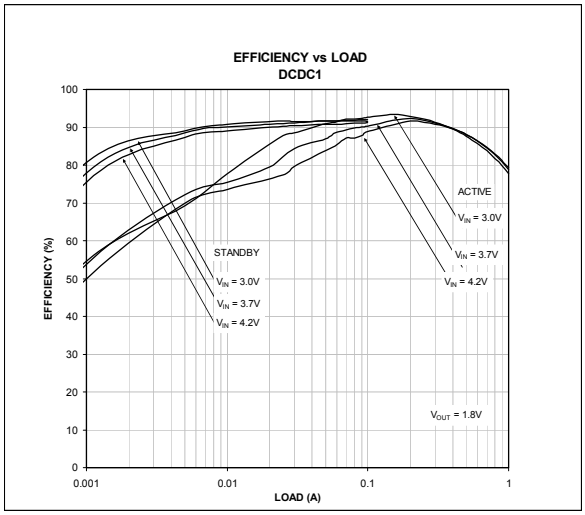


Figure 1 DC-DC1 Efficiency Vs Load Current Vo=1.8V

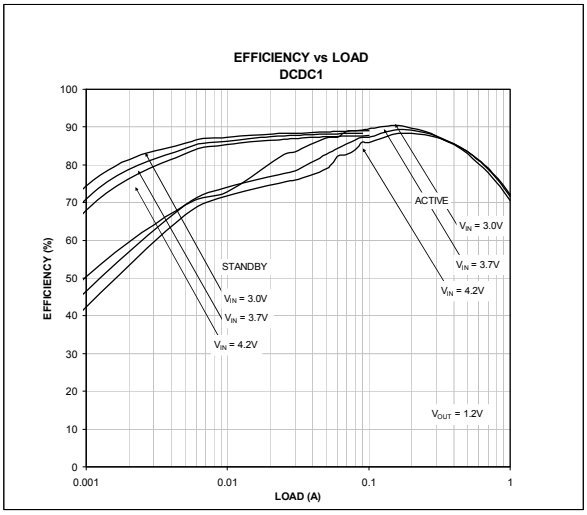


Figure 2 DC-DC1 Efficiency Vs Load Current Vo=1.2V

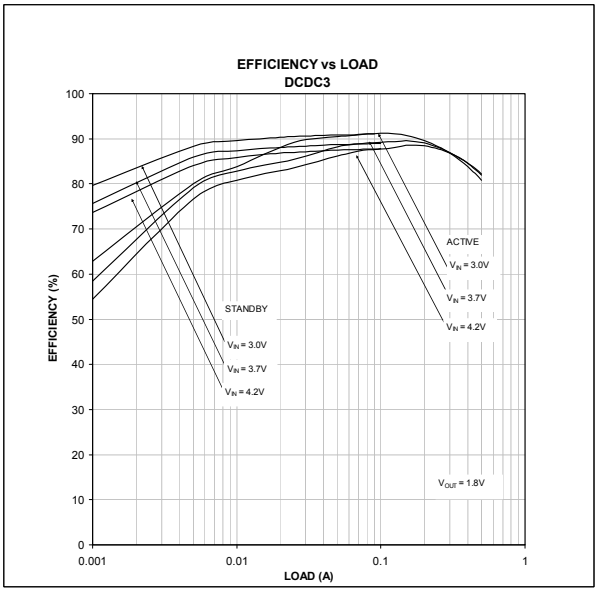


Figure 3 DC-DC3 Efficiency Vs Load Current Vo=1.8V

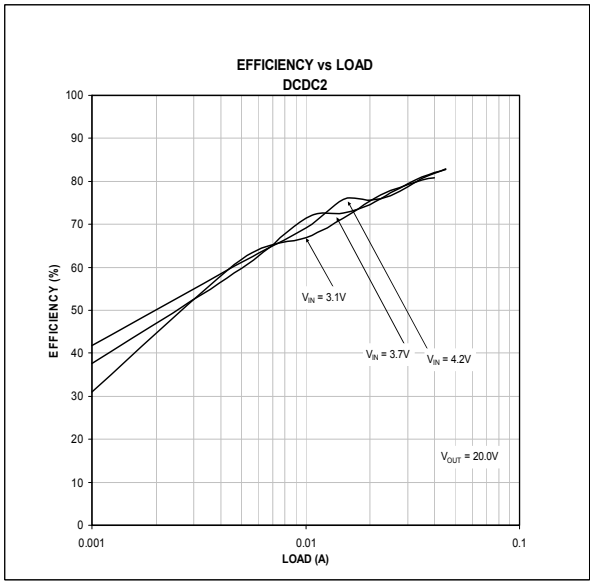


Figure 4 DC-DC2 Efficiency Vs Load Current Vo=20V

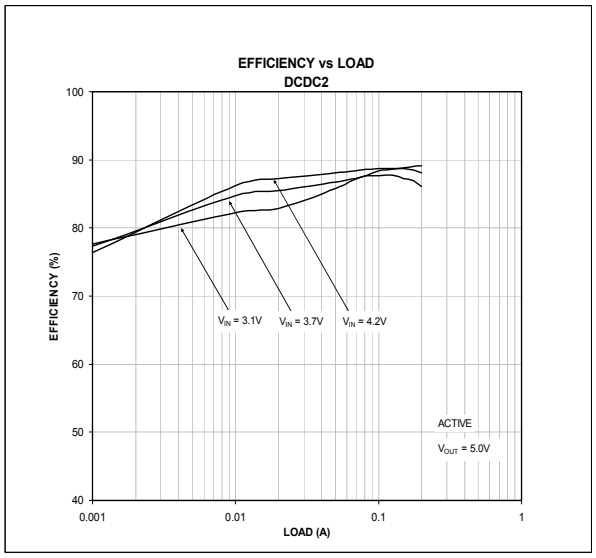


Figure 5 DC-DC2 Efficiency Vs Load Current Vo=5V

9.2.2 OUTPUT VOLTAGE REGULATION

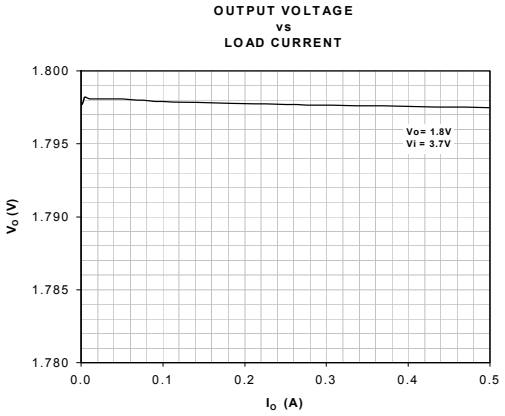


Figure 6 DC-DC1 Output Voltage Vs Output Current

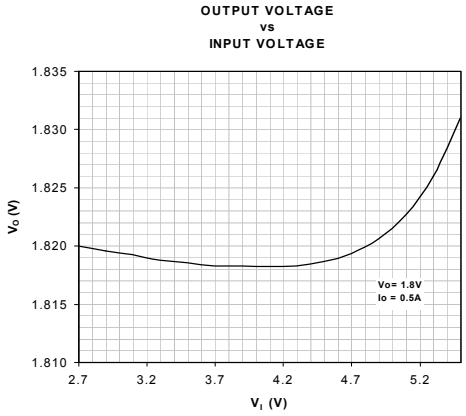


Figure 7 DC-DC1 Output Voltage Vs Input Voltage

9.2.3 DYNAMIC OUTPUT VOLTAGE

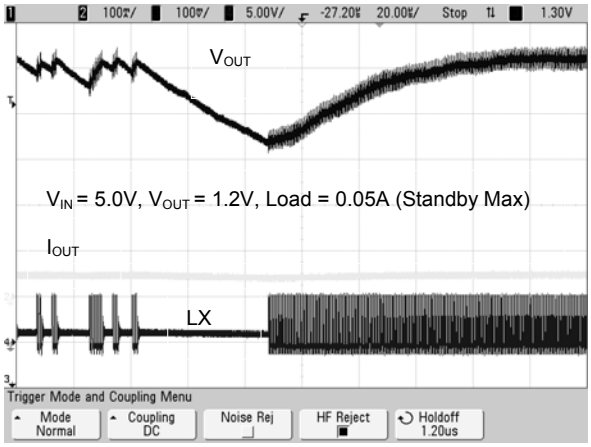


Figure 8 DC-DC1 STANDBY to ACTIVE Handover at Maximum Standby Current

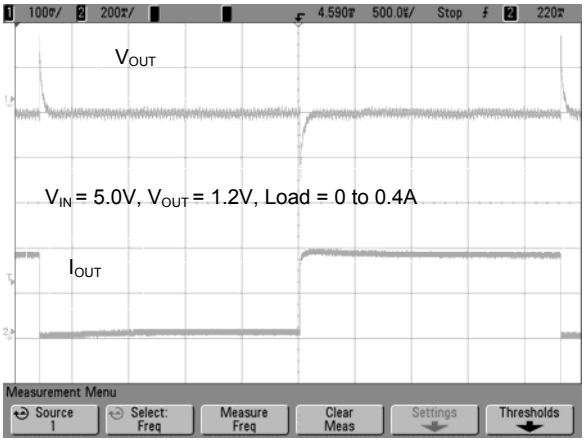


Figure 9 DC-DC1 Transient Load

9.3 LDO REGULATORS

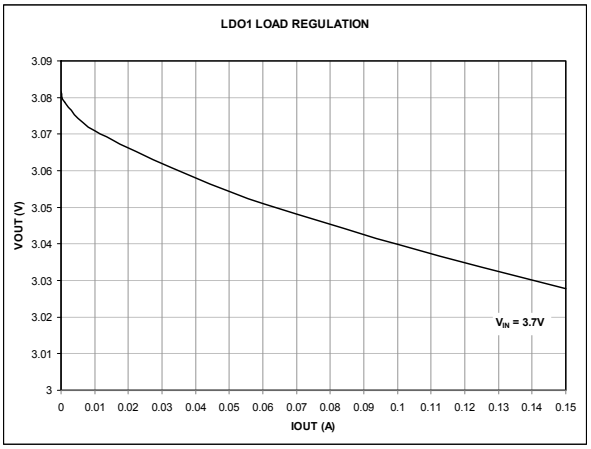


Figure 10 LDO1 Output Voltage Versus Output Current

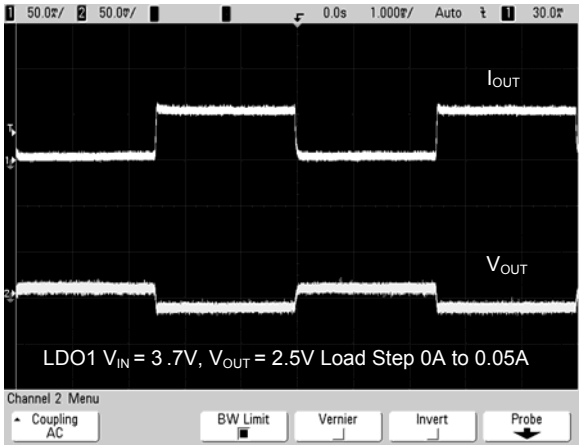


Figure 11 LDO1 Load Transient Response

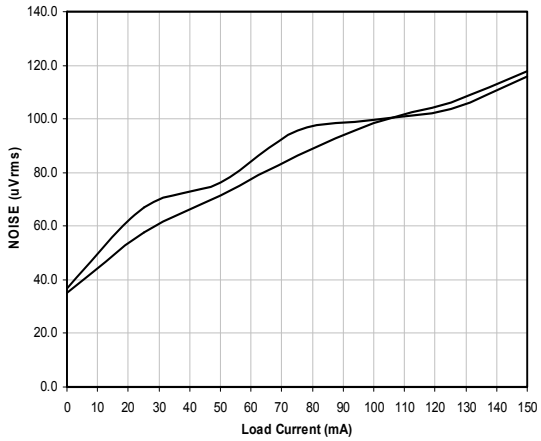


Figure 12 LDO1 Output Noise versus Output Current

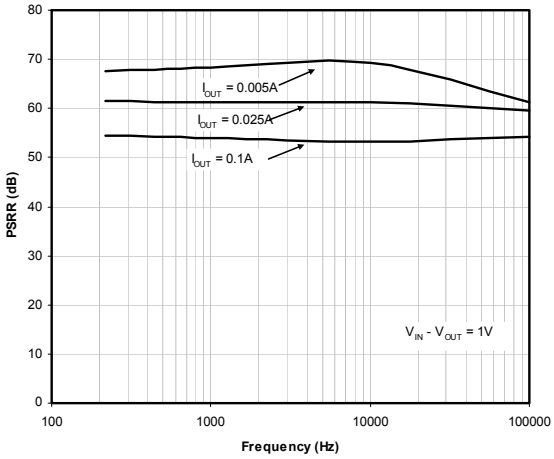


Figure 13 Power Supply Ripple Rejection versus Frequency 217Hz GSM to 100kHz

10 SIGNAL TIMING REQUIREMENTS

10.1 SYSTEM CLOCK TIMING

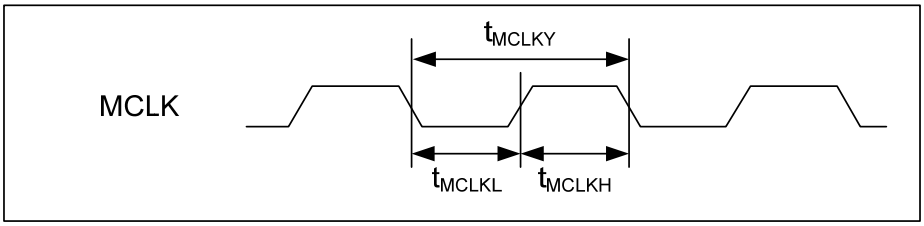


Figure 14 Master Clock Timing

Master Clock Timing						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
MCLK cycle time	T_{MCLKY}		40			ns
MCLK duty cycle		= high time / low time	60:40		40:60	

10.2 AUDIO INTERFACE TIMING - MASTER MODE

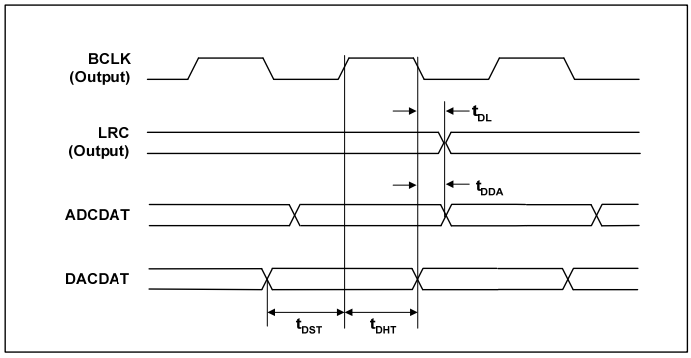


Figure 15 Digital Audio Data Timing – Master Mode

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BCLK rise time (10pF load)	t_{BCLKR}			3	ns
BCLK fall time (10pF load)	t_{BCLKF}			3	ns
BCLK duty cycle	t_{BCLKDS}	60:40		40:60	
LRC propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			10	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

10.3 AUDIO INTERFACE TIMING - SLAVE MODE

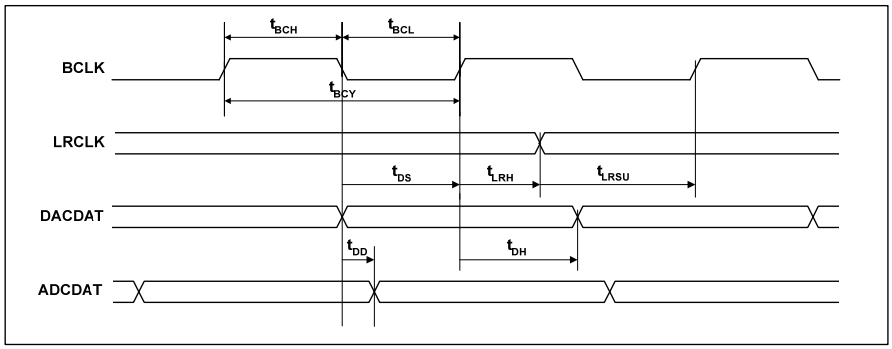


Figure 16 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	10			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
DACDAT set-up time to BCLK rising edge	t_{DS}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			10	ns

10.4 AUDIO INTERFACE TIMING - TDM MODE

In TDM mode, it is important that two ADC devices to not attempt to drive the ADCDAT pin simultaneously. The timing of the WM8351 ADCDAT tri-stating at the start and end of the data transmission is described in Figure 17 and the table below.

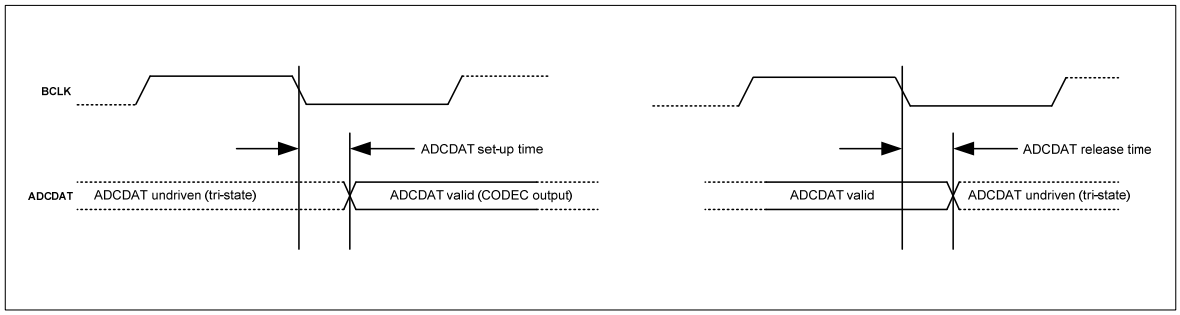


Figure 17 Digital Audio Data Timing - TDM Mode

Test Conditions

DBVDD = 3.3V, DGND = 0V, T_A=+25°C, Master Mode, fs=48kHz, 24-bit data, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
ADCDAT setup time from BCLK falling edge	DCVDD = 3.6V		5		ns
	DCVDD = 1.8V		15		ns
ADCDAT release time from BCLK falling edge	DCVDD = 3.6V		5		ns
	DCVDD = 1.8V		15		ns

10.5 CONTROL INTERFACE TIMING

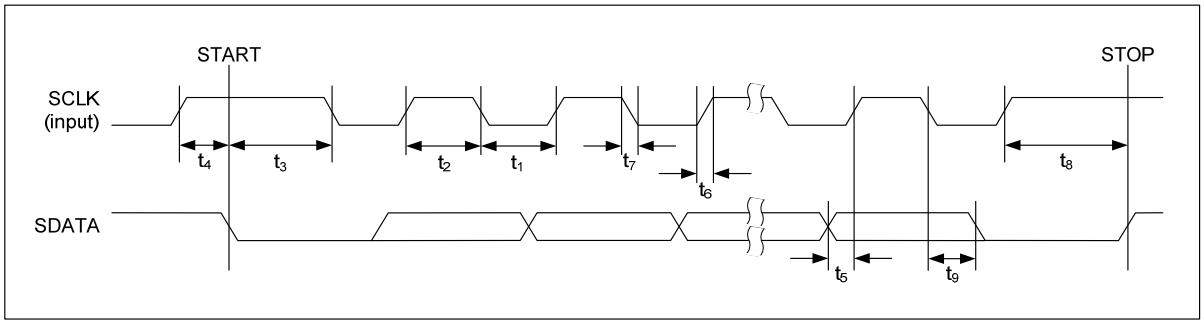


Figure 18 Control Interface Timing - 2-wire Control Mode

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDATA, SCLK Rise Time	t_6			300	ns
SDATA, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

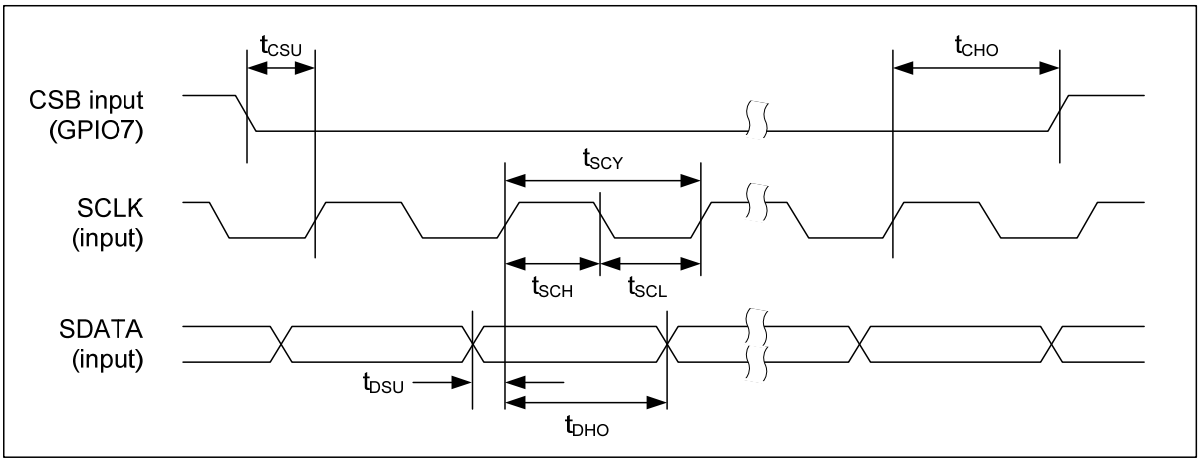


Figure 19 Control Interface Timing - 3-wire Control Mode (Write Cycle)

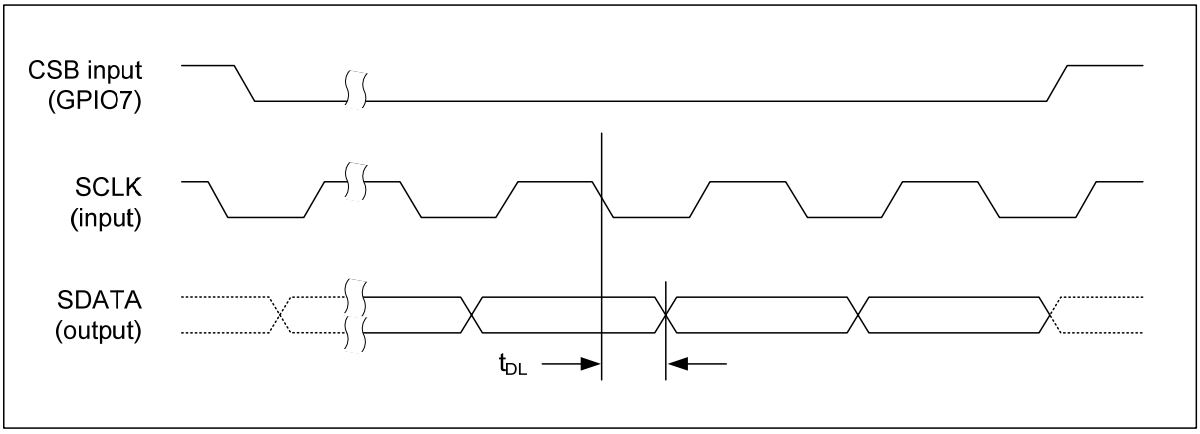


Figure 20 Control Interface Timing - 3-wire Control Mode (Read Cycle)

Test Conditions

DBVDD = 3.3V, DGND = 0V, T_A = +25°C, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CSB falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK rising edge to CSB rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDATA to SCLK set-up time	t_{DSU}	40			ns
SDATA to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDATA output transition	t_{DL}			40	ns

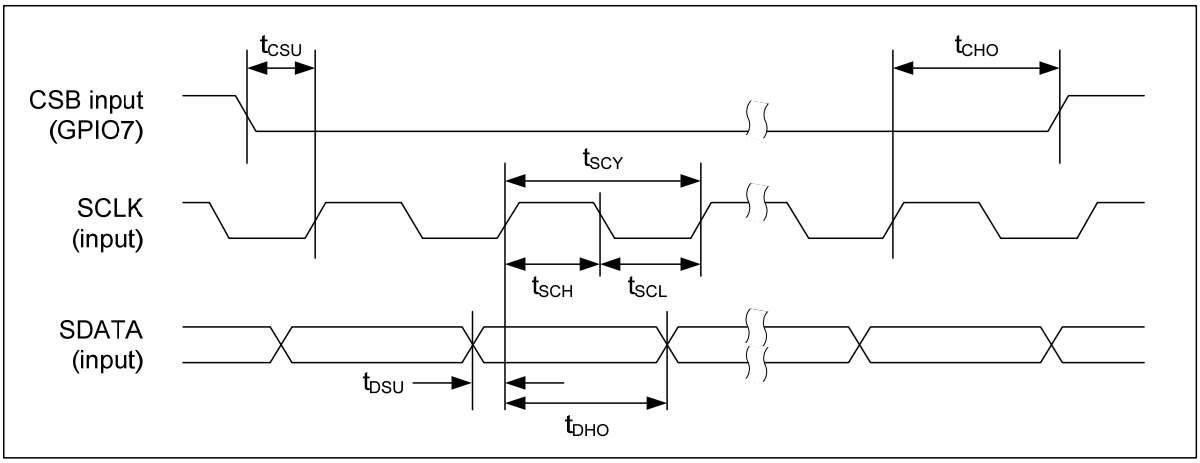


Figure 21 Control Interface Timing - 4-wire Control Mode (Write Cycle)

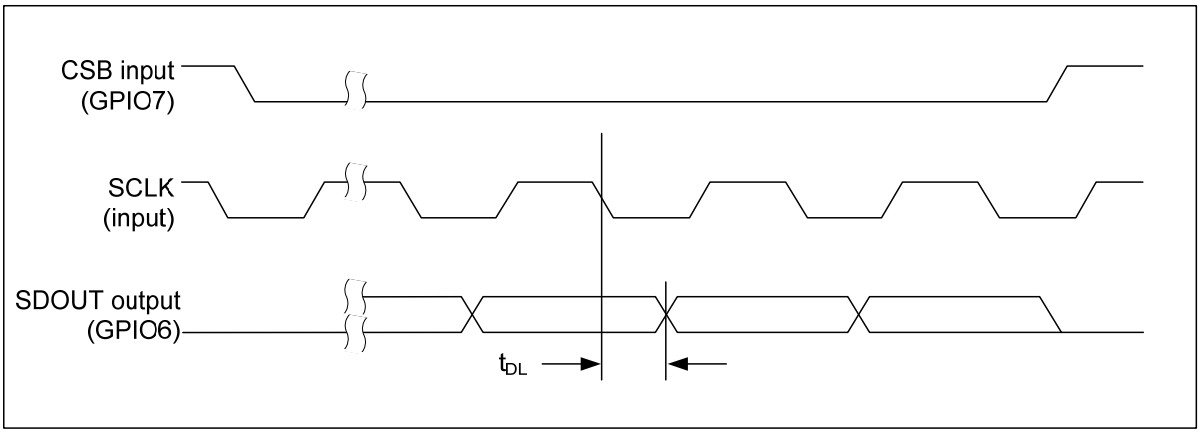


Figure 22 Control Interface Timing - 4-wire Control Mode (Read Cycle)

Test Conditions

DBVDD = 3.3V, DGND = 0V, T_A = +25°C, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CSB falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK rising edge to CSB rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDATA to SCLK set-up time	t_{DSU}	40			ns
SDATA to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

11 CONTROL INTERFACE

11.1 GENERAL DESCRIPTION

The WM8351 is controlled by writing to its control registers. Readback is available for most registers. Most aspects of the WM8351 operation can be controlled via this interface. The control interface can operate as either a 2-, 3- or 4-wire control interface:

2-wire mode uses pins SCLK and SDATA.

3-wire mode uses pins CSB, SCLK and SDATA.

4-wire mode uses pins CSB, SCLK, SDATA and SDOUT.

GPIO7 is automatically enabled as CSB in 3-wire and 4-wire control modes. GPIO6 is automatically enabled as SDOUT in 4-wire control mode. Register readback is provided on the bi-directional pin SDATA in 2-/3-wire modes and on SDOUT (GPIO6) in 4-wire mode.

In 2-wire mode, the control interface supports single register access as well as multiple access with or without address auto-increment.

In Development Mode (see Section 14.4), the WM8351 initially selects the secondary 2-wire control interface, using pins GPIO10 and GPIO11. This enables configuration of the WM8351 via a separate interface prior to selecting the normal system operation. Note that, in Custom modes, the secondary interface is not supported.

11.2 CONTROL INTERFACE MODES

The WM8351 control interface can be configured for 2-, 3- or 4-wire operation using the following register bits:

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Interface Control	3	SPI_CFG	0	Controls the SDOUT (GPIO6) pin operation in 4 wire mode 0 = SDOUT output is CMOS 1 = SDOUT output is open drain Note: SPI_4WIRE must be set for this to take effect.
	2	SPI_4WIRE	0	Selects 3-wire or 4-wire SPI mode 0 = 3 wire mode using bi-directional SDATA pin 1 = 4 wire mode using SDOUT (GPIO6) Note: SPI_3WIRE must be set for this to take effect.
	1	SPI_3WIRE	0	Selects 2- or 3-/4-wire mode. 0 = 2-wire mode 1 = 3-/4-wire mode

Table 1 Control Interface Modes

11.3 2-WIRE SERIAL CONTROL MODE

The 2-wire control interface normally uses the SCLK and SDATA pins, which are referenced to the digital buffer supply, DBVDD. (In Development mode, the interface is initially redirected, with GPIO10 and GPIO11 effectively replacing SCLK and SDATA - see Section 14.4.1).

2-wire control mode is selected by setting SPI_3WIRE = 0. This is the default setting for this field.

In 2-wire mode, the WM8351 is a slave device on the control interface; SCLK (or GPIO10) is a clock input, while SDATA (or GPIO11) is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8351 transmits logic 1 by tri-stating the SDATA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDATA line high so that the logic 1 can be recognised by the master.

Many devices can be controlled by the same bus, and each device has a unique 7-bit device ID (this is not the same as the 8-bit address of each register in the WM8351). The default device ID is 0011 0100 (0x34h). The LSB of the device ID is the Read/Write bit; this bit is set to logic 1 for “Read” and logic 0 for “Write”. In Development Mode, the device ID may be changed to other values.

The controller indicates the start of data transfer with a high to low transition on SDATA while SCLK remains high. This indicates that a device ID, register address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDATA (7-bit device ID + Read/Write bit, MSB first). If the device ID received matches the device ID of the WM8351, then the WM8351 responds by pulling SDATA low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is ‘1’ when operating in write only mode, the WM8351 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM8351, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDATA while SCKL remains high. After receiving a complete address and data sequence the WM8351 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDATA changes while SCLK is high), the device returns to the idle condition.

The WM8351 supports the following read and write operations:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

The sequence of signals associated with a single register write operation is illustrated in Figure 23.

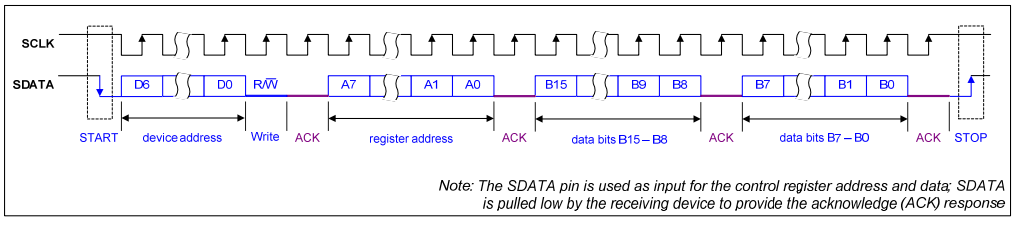


Figure 23 Control Interface 2-wire Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 24.

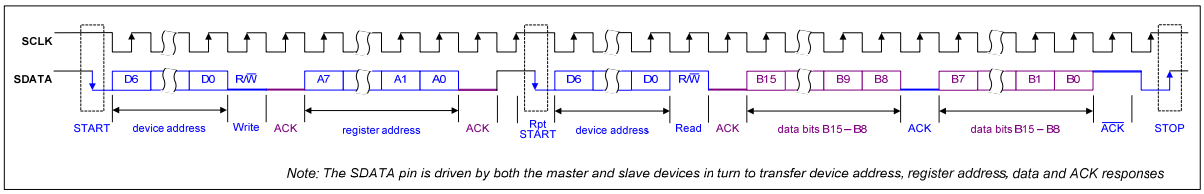


Figure 24 Control Interface 2-wire Register Read

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 2.

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge	
P	Stop Condition	
R/$\overline{W}$	ReadNotWrite	0 = Write 1 = Read
[White field]	Data flow from bus master to WM8351	
[Grey field]	Data flow from WM8351 to bus master	

Table 2 Control Interface Terminology

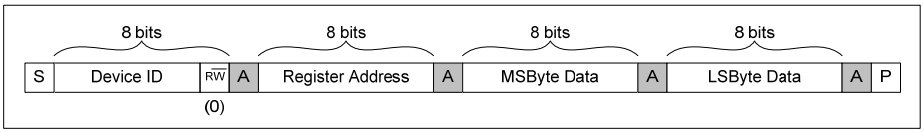


Figure 25 Single Register Write to Specified Address

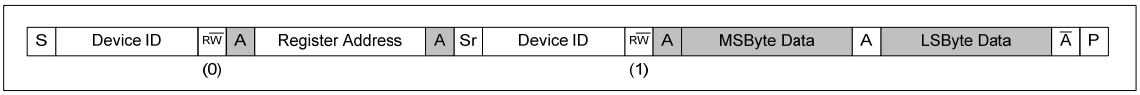


Figure 26 Single Register Read from Specified Address

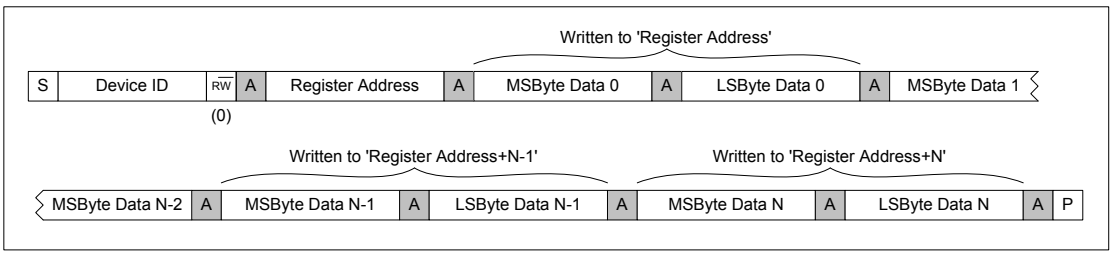


Figure 27 Multiple Register Write to Specified Address using Auto-increment

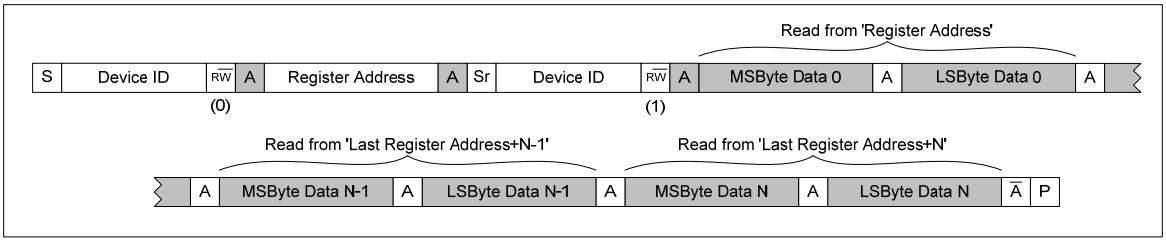


Figure 28 Multiple Register Read from Specified Address using Auto-increment

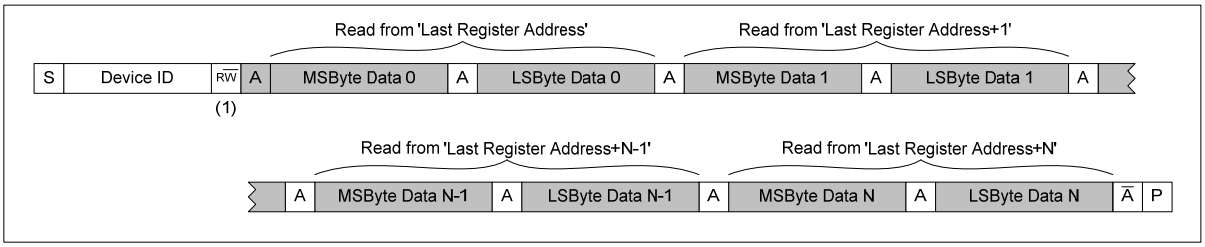


Figure 29 Multiple Register Read from Last Address using Auto-increment

Multiple Write and Multiple Read operations enable the host processor to access sequential blocks of the data in the WM8351 register map faster than is possible with single register operations. The Auto-Increment function is enabled by default; this is controlled by the AUTOINC register bit as described in Table 3.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Interface Control	9	AUTOINC	1	Enables address auto-increment 0 = disabled 1 = enabled

Table 3 Enabling Address Auto-Increment

11.4 3-WIRE SERIAL CONTROL MODE

The 3-wire control interface uses the CSB, SCLK and SDATA pins, which are referenced to the digital buffer supply, DBVDD. (In 3-wire mode, CSB is provided on GPIO7.)

3-wire control mode is selected by setting SPI_3WIRE = 1 and SPI_4WIRE = 0.

In 3-wire control mode, a control word consists of 24 bits. The first bit is the read/write bit (R/W), which is followed by 7 address bits (A6 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDATA pin. A rising edge on CSB latches in a complete control word consisting of the last 24 bits.

In Write operations (R/W=0), all SDATA bits are driven by the controlling device.

In Read operations (R/W=1), the SDATA pin is driven by the controlling device to clock in the register address, after which the WM8351 drives the SDATA pin to output the applicable data bits.

Similarly to 2-wire control mode, the WM8351 transmits logic 1 by tri-stating the SDATA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDATA line high so that the logic 1 can be recognised by the master.

The 3-wire control mode timing is illustrated in Figure 30.

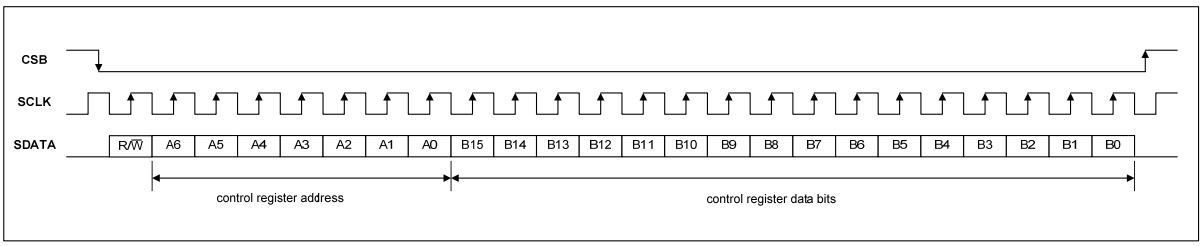


Figure 30 3-Wire Serial Control Interface

11.5 4-WIRE SERIAL CONTROL MODE

The 4-wire control interface uses the CSB, SCLK, SDATA and SDOUT pins, which are referenced to the digital buffer supply, DBVDD. (In 4-wire mode, SDOUT is provided on GPIO6; CSB is provided on GPIO7.)

4-wire control mode is selected by setting SPI_3WIRE = 1 and SPI_4WIRE = 1.

The Data Output pin, SDOUT, can be configured as CMOS or Open Drain, as described in Table 1. In CMOS mode, SDOUT is driven low when not outputting register data bits. In Open Drain mode, SDOUT is undriven when not outputting register data bits.

In Write operations (R/W=0), this mode is the same as 3-wire mode described above.

In Read operations (R/W=1), the SDATA pin is ignored following receipt of the valid register address. SDOUT is driven by the WM8351.

The 4-wire control mode timing is illustrated in Figure 31 and Figure 32.

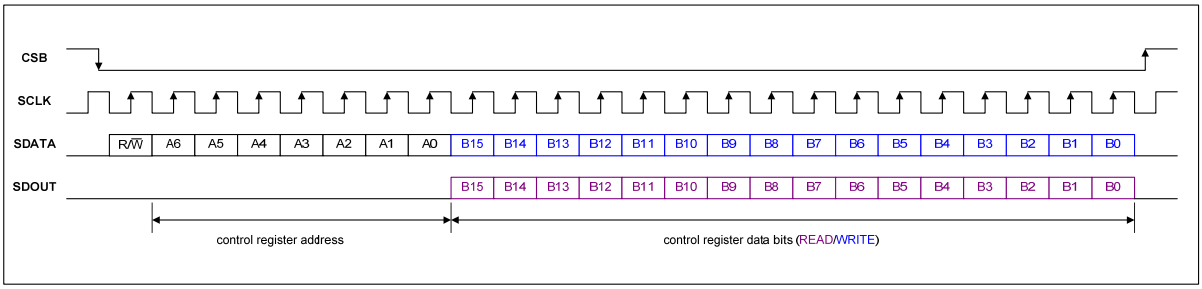


Figure 31 4-Wire Readback (CMOS)

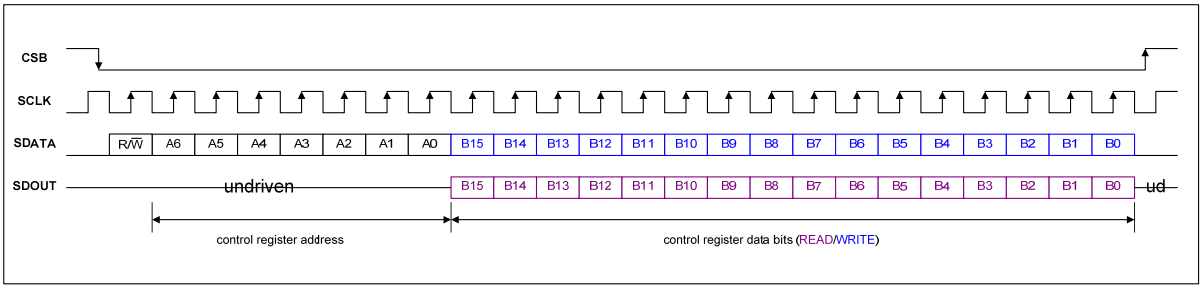


Figure 32 4-Wire Readback (Open Drain)

11.6 REGISTER LOCKING

Certain control fields are protected against accidental overwriting. This includes:

- Watchdog timer and system control settings in Registers R3, R4, R6 and R12 (03h, 04h, 06h and 0Ch).
- Battery charger control fields in Registers R168, R169 and R170 (A8h, A9h and AAh).

By default, these registers are locked, i.e. writing to them has no effect. However, they can be unlocked by writing a value of 0013h to Register R219 (DBh).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R219 (DBh) Security	15:0	SECURITY [15:0]	0000h	The value 0013h needs to be set in this register to allow write access to the security locked registers.

Table 4 Locking and Unlocking Protected Registers

It is recommended to re-lock the protected registers immediately after writing to them. This helps protect the system against accidental overwriting of register values.

It is recommended to contact Wolfson Applications support for guidance on features that are affected by Register Locking.

11.7 SPECIAL REGISTERS

11.7.1 CHIP ID

A read instruction from register 0 can be used to confirm that the chip is a WM8351.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Chip ID	15:0	CHIP_ID [15:0]	6143h	Reading this register returns 6143h.

Table 5 Chip ID

11.7.2 DEVICE INFORMATION

The read-only register 1 provides additional information about the WM8351 device.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) ID	15:12	CHIP_REV [3:0]		The functional silicon revision - this tracks changes in functionality which are separate from ROM mask settings
	11:10	CONF_STS [1:0]		The state of the configuration pins. This selects what register defaults should be.
	7:0	CUST_ID [7:0]		The chip revision number
R2 (02h) Revision	7:0	MASK_REV [7:0]		The ROM mask ID

Table 6 Reading Device Information

12 CLOCKING, TIMING AND SAMPLE RATES

12.1 GENERAL DESCRIPTION

The WM8351 includes clocking circuitry for the on-chip audio CODEC, the DC-DC converters and the auxiliary ADC. It provides the following capabilities:

The WM8351 has two internal clock generators: a 2MHz RC oscillator and a 32kHz crystal oscillator. Clocks are required for system start-up and also for the DC-DC converter clocks; these are derived from the internal 2MHz RC oscillator. The 32kHz crystal oscillator (or external 32kHz source) is used to drive the internal Real Time Clock (RTC), and may also be used as a reference source for the CODEC clock generators.

The CODEC clocks may be derived either directly from MCLK, or else via an on-chip Frequency Locked Loop (FLL) to generate the required clocking from a wide range of reference inputs. The FLL can take as input the external MCLK, or ADCLRCLK / DACLRCLK (in Slave modes), or the 32kHz crystal oscillator (or external 32kHz source), and generates (typically) a 12.288MHz clock for the CODEC.

The flexible clocking arrangements are illustrated in Figure 33.

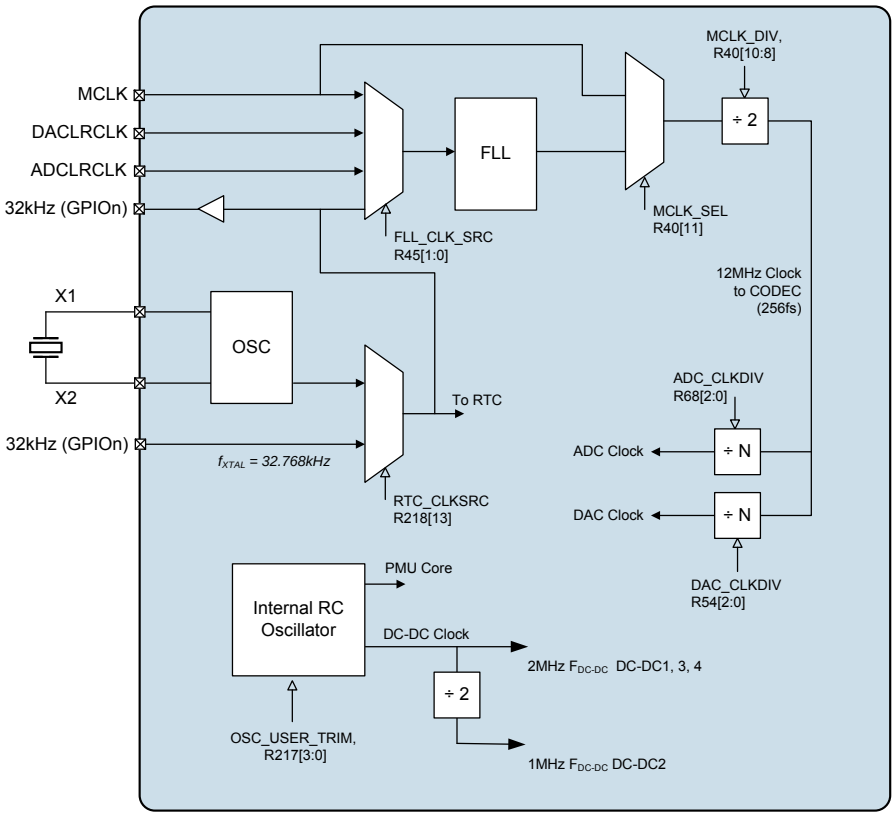


Figure 33 Clock Generation and Distribution Scheme

12.1.1 CLOCKING THE AUDIO CODEC

The WM8351 audio CODEC core requires an accurate, low-jitter clock. Clocks for the ADCs, DACs, DSP core functions, and the digital audio interface are all derived from a common internal clock source, SYSCLK. This clock may be derived directly from MCLK, or may be generated from an FLL using MCLK or alternate sources as an external reference. The SYSCLK source is selected by MCLK_SEL. Many commonly-used audio sample rates can be derived directly from typical MCLK frequencies.

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, using ADC_CLKDIV and DAC_CLKDIV. Refer to Section 12.3 for more details

12.1.2 CLOCKING THE DC-DC CONVERTERS

During a system start-up, no external clock signals are available. The WM8351 therefore generates all internal clocks required for the DC-DC converters, system control and housekeeping functions. These clocks are derived from the on-chip RC oscillator. The DC-DC converters' nominal switching rate is 2.0MHz and 1.0MHz.

12.1.3 INTERNAL RC OSCILLATOR

The internal RC Oscillator generates the system clock 2.0MHz as well as the clock for the DCDC converters. The period of the generated clock is defined by the time needed for a fixed value capacitor to be charged up to the reference voltage by a constant current source.

12.2 CRYSTAL OSCILLATOR

The on-chip crystal oscillator generates a 32.768kHz reference clock, which can be used to provide reference clock for the Real Time Clock (RTC) in the WM8351. It may also be used as a reference input to the FLL, for the purpose of generating the CODEC clocks. The oscillator is powered from VRTC, so that it can keep running when no other power source is available. It requires an external crystal on the X1 and X2 pins, as well as two capacitors and a resistor, connected as shown in Figure 34.

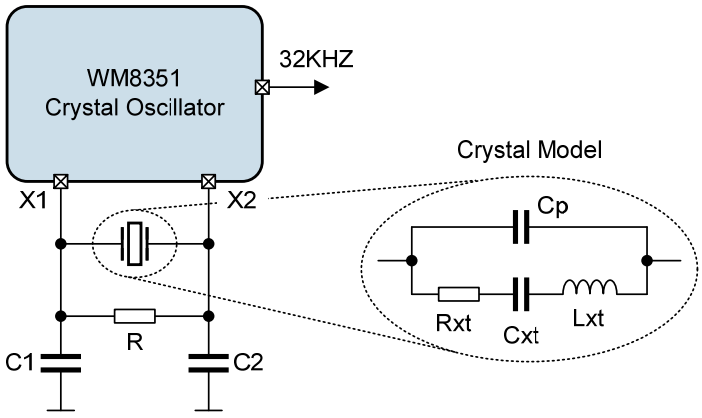


Figure 34 WM8351 Crystal Oscillator

The oscillator is enabled by the OSC32K_ENA field, as described in Table 7. It is enabled by default and remains enabled when the WM8351 is in the OFF or BACKUP state.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) Power Mgmt (5)	10	OSC32K_ENA	1	32kHz crystal oscillator control 0 = 32kHz OSC is disabled 1 = 32kHz OSC is enabled
R218 (DAh) RTC Tick Control	12			
Note: OSC32K_ENA can be accessed through R12 or through R218. Reading from or writing to either register location has the same effect.				

Table 7 Enabling the 32kHz Oscillator

If a suitable 32.768kHz clock is already present elsewhere in the system, then it is possible for the WM8351 to use this clock instead. An external clock can be provided to the WM8351 on pin X1 (with pin X2 left floating) or else on a GPIO pin configured as a 32kHz input (see Section 20).

In addition to driving the RTC, the 32kHz oscillator signal can be output to a GPIO pin configured as a 32kHz output; this is possible on GPIO pins 2, 3, 5 and 12 (see Section 20.2).

12.3 CLOCKING AND SAMPLE RATES

Clocks for the ADCs, DACs, DSP core functions, and the digital audio interface are all derived from a common internal clock source, SYSCLK.

SYSCLK can either be derived directly from MCLK (with a selectable divide by two option, controlled by MCLK_DIV), or may be generated by the FLL using MCLK or alternate sources as an external reference. The SYSCLK source is selected by MCLK_SEL. Many commonly-used audio sample rates can be derived directly from typical MCLK frequencies.

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, using ADC_CLKDIV and DAC_CLKDIV. These fields must be set according to the required sampling frequency and depending upon the selected clocking mode. Two clocking modes are provided as follows. Normal mode allows selection of the commonly used sample rates from typical audio system clocking frequencies (eg. 12.288MHz); USB mode allows many of these sample rates to be generated from a 12MHz USB clock. Depending on the available clock sources, USB mode may be used to save power by supporting 44.1kHz operation.

In Normal mode,

- ADC_SYSCLK = 256 x ADC Sampling Frequency
- DAC_SYSCLK = 256 x DAC Sampling Frequency

In USB mode,

- ADC_SYSCLK = 272 x ADC Sampling Frequency
- DAC_SYSCLK = 272 x DAC Sampling Frequency

The above equations determine the required values for ADC_CLKDIV and DAC_CLKDIV. The clocking mode is selected via the AIF_LRCLKRATE field.

In master mode, BCLK is also derived from SYSCLK via a programmable division set by BCLK_DIV. In the case where the ADCs and DACs are operating at different sample rates, BCLK must be set according to whichever is the faster rate. In Master Mode, internal clock divide and phase control mechanisms ensure that the BCLK, ADCLRCLK and DACLRCLK edges will occur in a predictable and repeatable position relative to each other and to the data for a given combination of ADC/DAC sample rates and BCLK settings. In Slave Mode, the host processor must ensure that BCLK, ADCLRCLK and DACLRCLK are fully synchronised; if these inputs are not synchronised, unpredictable pops and noise may result.

When the GPIO5 pin is configured as CODEC_OPCLK, a clock derived from SYSCLK may be output on this pin to provide clocking for other parts of the system. The frequency of this signal is set by OPCLK_DIV.

Alternate GPIO pins can be used to provide ADCLRCLK and ADCBCLK as described in Section 20. An inverted L/R clock signal ADCLRCLKB can also be generated. When this feature is used, the LRCLK and BCLK pins support the DAC only, and the alternate GPIO pins support the ADC only. Limited capability can be provided to support mixed sample rates by this method. (The selection of USB mode and the supported values of the various SYSCLK dividers impose restrictions on what combinations of clocking and sample rates may be configured.)

A slow clock derived from SYSCLK may be used to provide de-bouncing of the headphone detect function, and to set the timeout period for volume updates when zero-cross functions are used. This clock is enabled by TOCLK_ENA and its frequency is set by TOCLK_RATE.

The overall CODEC clocking scheme is illustrated in Figure 35.

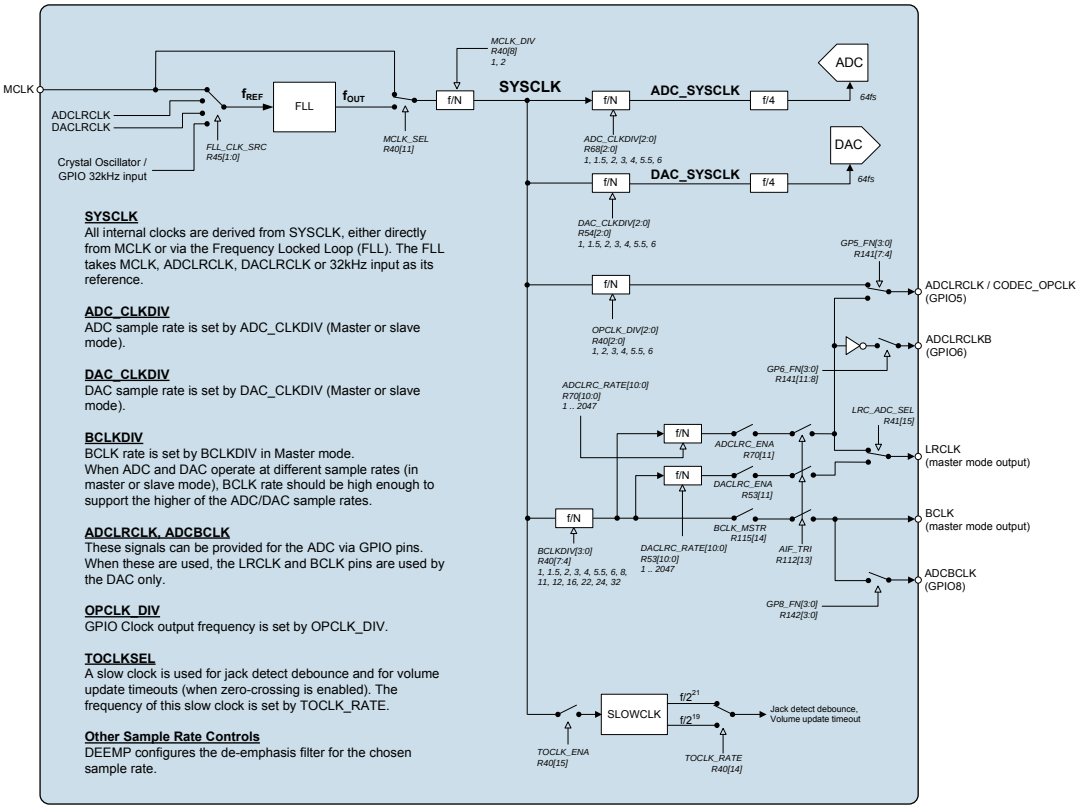


Figure 35 Audio CODEC Clocking

12.3.1 SYSCLK CONTROL

The MCLK_SEL bit is used to select the source for SYSCLK. The source may be either directly from the MCLK input or may be from the output of the FLL. If required, the selected source may be divided by two, as determined by MCLK_DIV, as described in Table 8. For further details of the FLL, see Section 12.4.

When the internal clock source is switched from one value to another using MCLK_SEL, the change of source will only occur following a falling edge of the source signal that was originally selected. In the case where the clock source is switched from FLL to MCLK, a suitable falling edge can be ensured by disabling the FLL after selection of MCLK as the source.

The recommended sequence of actions to switch from FLL to MCLK source is as follows:

- Select MCLK as source (MCLK_SEL = 0)
- Disable FLL (FLL_ENA = 0)
- Disable FLL oscillator (FLL_OSC_ENA = 0)

Note that, as an alternative to the above sequence, a software reset may be used to re-select MCLK as the default SYSCLK source.

The recommended sequence of actions to switch from MCLK to FLL source is as follows:

- Enable FLL oscillator (FLL_OSC_ENA = 1)
- Enable FLL (FLL_ENA = 1)
- Select FLL as source (MCLK_SEL = 1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) Clock Control 1	11	MCLK_SEL	0	Selects source for SYSCLK to CODEC 0 = MCLK pin 1 = FLL
	8	MCLK_DIV	0	Selects MCLK division in slave (MCLK input) mode: 0 = divide MCLK by 1 1 = divide MCLK by 2

Table 8 SYSCLK Control

12.3.2 ADC / DAC SAMPLE RATES

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, by setting the register fields ADC_CLKDIV and DAC_CLKDIV. These fields must be set according to the SYSCLK frequency, and according to the selected mode of operation (Normal or USB). The applicable fields are described in Table 9.

Selection of USB mode enables a 12MHz USB clock to be used to generate the required internal clock signals. Table 10 describes the available sample rates using four different common MCLK frequencies. The AIF_LRCLKRATE field must be set as described in Table 9.

In Normal mode, the programmable division set by ADC_CLKDIV must ensure that ADC_SYSCLK is 256 * ADC Sampling Frequency. DAC_CLKDIV must ensure that DAC_SYSCLK is 256 * DAC Sampling Frequency.

In USB mode, ADC_CLKDIV must ensure that ADC_SYSCLK is 272 * ADC Sampling Frequency. DAC_CLKDIV must ensure that DAC_SYSCLK is 272 * DAC Sampling Frequency.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (30h) DAC Control	12	AIF_LRCLKRATE	0	Mode Select 1 = USB mode (272 * Fs) 0 = Normal mode (256 * Fs)
R68 (44h) ADC Clock Control	2:0	ADC_CLKDIV [2:0]	000	ADC Sample rate divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2 011 = SYSCLK / 3 100 = SYSCLK / 4 101 = SYSCLK / 5.5 110 = SYSCLK / 6 111 = Reserved
R54 (36h) DAC Clock Control	2:0	DAC_CLKDIV [2:0]	000	DAC Sample rate divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2 011 = SYSCLK / 3 100 = SYSCLK / 4 101 = SYSCLK / 5.5 110 = SYSCLK / 6 111 = Reserved

Table 9 ADC / DAC Sample Rate Control

SYSCLK	ADC / DAC SAMPLE RATE DIVIDER	CLOCKING MODE	ADC / DAC SAMPLE RATE
12.2880 MHz	000 = SYSCLK / 1	Normal (256 * Fs)	48 kHz
	001 = SYSCLK / 1.5		32 kHz
	010 = SYSCLK / 2		24 kHz
	011 = SYSCLK / 3		16 kHz
	100 = SYSCLK / 4		12 kHz
	101 = SYSCLK / 5.5		Not used
	110 = SYSCLK / 6		8 kHz
	111 = Reserved		Reserved
11.2896 MHz	000 = SYSCLK / 1	Normal (256 * Fs)	44.1 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		22.05 kHz
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		11.025 kHz
	101 = SYSCLK / 5.5		8.018 kHz
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved
12.0000 MHz	000 = SYSCLK / 1	USB (272 * Fs)	44.118 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		22.059 kHz
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		11.029 kHz
	101 = SYSCLK / 5.5		8.021 kHz
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved
2.0480 MHz	000 = SYSCLK / 1	Normal (256 * Fs)	8 kHz
	001 = SYSCLK / 1.5		Not used
	010 = SYSCLK / 2		Not used
	011 = SYSCLK / 3		Not used
	100 = SYSCLK / 4		Not used
	101 = SYSCLK / 5.5		Not used
	110 = SYSCLK / 6		Not used
	111 = Reserved		Reserved

Table 10 Derivation of Sample Rates in Normal / USB Modes

Note that, in USB mode, the ADC / DAC sample rates do not match exactly with the commonly used sample rates (eg. 44.118 kHz instead of 44.100 kHz). At most, the difference is less than 0.5%, which is within normal accepted tolerances. Data recorded at 44.100 kHz sample rate and replayed at 44.118 kHz will experience a slight (sub 0.5%) pitch shift as a result of this difference.

Note: USB mode cannot be used to generate a 48kHz samples rate from a 12MHz MCLK; the FLL should be used in this case.

The user must ensure correct synchronisation of data across the digital interfaces. This is particularly important when different sample rates are used, as described above.

12.3.3 BCLK CONTROL

In Master Mode, BCLK is derived from SYSCLK via a programmable division set by BCLK_DIV, as described in Table 11. BCLK_DIV must be set to an appropriate value to ensure that there are sufficient BCLK cycles to transfer the complete data words from the ADCs and to the DACs. When the GPIO8 pin is used to provide ADCBCLK in Master mode, the clock rate on this pin is also controlled by BCLK_DIV.

In Slave Mode, BCLK is generated externally and appears as an input to the CODEC. The host device must provide sufficient BCLK cycles to transfer complete data words to the ADCs and DACs.

Note that, although the ADC and DAC can run at different sample rates, they share the same bit clock BCLK in Master Mode. In the case where different ADC / DAC sample rates are used, the BCLK frequency should be set according to the higher of the ADC / DAC bit rates. When the GPIO8 pin is used to provide ADCBCLK, and either the ADC or DAC is in Slave mode, then this restriction does not apply.

Master/Slave operation for BCLK is controlled by the BCLK_MSTR register field.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) Clock Control 1	7:4	BCLK_DIV [3:0]	0000	Sets BCLK rate for Master mode 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0101 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 = SYSCLK / 32 1110 = SYSCLK / 32 1111 = SYSCLK / 32
R115 (73h) Audio I/F DAC Control	14	BCLK_MSTR	0	Enables the Audio Interface BCLK generation and enables the BCLK pin for Master mode 0 = BCLK Slave Mode 1 = BCLK Master Mode

Table 11 BCLK Control

Table 12 shows the maximum word lengths supported for a given SYSCLK and BCLK_DIV, assuming that one or both the ADCs and DACs are running at maximum rate.

SYSCLK	BCLK DIVIDER BCLK_DIV	BCLK RATE (MASTER MODE) (MHZ)	MAXIMUM WORD LENGTH
12.288 MHz	0000 = SYSCLK / 1	12.288	32
	0001 = SYSCLK / 1.5	8.192	32
	0010 = SYSCLK / 2	6.144	32
	0011 = SYSCLK / 3	4.096	32
	0100 = SYSCLK / 4	3.072	32
	0101 = SYSCLK / 5.5	2.2341818	20
	0110 = SYSCLK / 6	2.048	20
	0111 = SYSCLK / 8	1.536	16
	1000 = SYSCLK / 11	1.117091	8
	1001 = SYSCLK / 12	1.024	8
	1010 = SYSCLK / 16	0.768	8
	1011 = SYSCLK / 22	0.558545	N/A
	1100 = SYSCLK / 24	0.512	N/A
	1101 = SYSCLK / 32	0.384	N/A
	1110 = SYSCLK / 32	0.384	N/A
	1111 = SYSCLK / 32	0.384	N/A
11.2896 MHz	0000 = SYSCLK / 1	11.2896	32
	0001 = SYSCLK / 1.5	7.5264	32
	0010 = SYSCLK / 2	5.6448	32
	0011 = SYSCLK / 3	3.7632	32
	0100 = SYSCLK / 4	2.8224	32
	0101 = SYSCLK / 5.5	2.052655	20
	0110 = SYSCLK / 6	1.8816	20
	0111 = SYSCLK / 8	1.4112	16
	1000 = SYSCLK / 11	1.026327	8
	1001 = SYSCLK / 12	0.9408	8
	1010 = SYSCLK / 16	0.7056	8
	1011 = SYSCLK / 22	0.513164	N/A
	1100 = SYSCLK / 24	0.4704	N/A
	1101 = SYSCLK / 32	0.3528	N/A
	1110 = SYSCLK / 32	0.3528	N/A
	1111 = SYSCLK / 32	0.3528	N/A

Table 12 BCLK Divider in Master Mode

12.3.4 ADCLRCLK / DACLRCLK CONTROL

In Master Mode, ADCLRCLK and DACLRCLK are derived from BCLK via programmable dividers set by ADCLRC_RATE and DACLRC_RATE. The BCLK frequency is derived from SYSCLK according to BCLK_DIV, as described earlier in Table 11.

In Slave Mode, ADCLRCLK and DACLRCLK are generated externally and are input to the CODEC.

By default, the LRCLK pin provides the L/R Clock signal for the ADC and the DAC. If a separate L/R Clock is required for the ADC and the DAC, then a GPIO pin must be configured as ADCLRCLK (or ADCLRCB) as described in Section 20. The LRCLK pin can be driven by either ADCLRCLK or by DACLRCLK in Master Mode; this is selected by the LRC_ADC_SEL bit as described in Table 13.

Master/Slave operation for ADCLRCLK is controlled by the ADCLRC_ENA register field.

Master/Slave operation for DACLRCLK is controlled by the DACLRC_ENA register field.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R70 (46h) ADC LRC Rate	11	ADCLRC_ENA	0	Enables the LRC generation for the ADC 0 = disabled 1 = enabled
	10:0	ADCLRC_RATE [10:0]	040h (64 BCLK/LRC)	Determines the number of bit clocks per LRC phase (when enabled) 00000000000 = invalid ... 00000000111 = invalid 00000001000 = 8 BCPS … 11111111111 = 2047 BCPS
R53 (35h) DAC LRC Rate	11	DACLRC_ENA	0	Enables DAC LRC generation in Master mode 0 = disabled 1 = enabled
	10:0	DACLRC_RATE [10:0]	040h (64 BCLK/LRC)	Determines the number of bit clocks per LRC phase (when enabled) 00000000000 = invalid ... 00000000111 = invalid 00000001000 = 8 BCPS … 11111111111 = 2047 BCPS
R41 (29h) Clock Control 2	15	LRC_ADC_SEL	0	Selects either ADCLRCLK or DACLRCLK to drive LRCLK pin in Master Mode 0 = DACLRCLK 1 = ADCLRCLK

Table 13 ADCLRCLK / DACLRCLK Control

12.3.5 OPCLK CONTROL

When the GPIO5 pin is configured as CODEC_OPCLK, a clock derived from SYSCLK may be output on this pin to provide clocking for other parts of the system. The frequency of this signal is derived from SYSCLK and determined by OPCLK_DIV, as described in Table 14.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) Clock Control 1	2:0	OPCLK_DIV [2:0]	000	OPCLK Frequency (GPIO function) 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 5.5 101 = SYSCLK / 6 110 = Reserved 111 = Reserved

Table 14 OPCLK Control

12.3.6 SLOWCLK CONTROL

A slow clock derived from SYSCLK may be generated for de-bouncing of the Headphone Jack Detect function or to set the timeout period for volume updates when zero-cross functions are used. This clock is enabled by TOCLK_ENA and its frequency is set by TOCLK_RATE, as described in Table 15.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh) Power Mgmt 4	8	TOCLK_ENA	0	Slow clock enable. Used for both the jack insert detect debounce circuit and the zero cross timeout. 0 = slow clock disabled 1 = slow clock enabled
R40 (28h) Clock Control 1	15			
	14	TOCLK_RATE	0	Slow Clock Selection (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)
Note: TOCLK_ENA can be accessed through R11 or through R40. Reading from or writing to either register location has the same effect.				

Table 15 SLOWCLK Control

12.4 FLL

The integrated FLL can be used to generate SYSCLK from a wide variety of different reference sources and frequencies. The FLL can accept a wide range of reference frequencies, which may be high frequency (eg. 12.288MHz) or low frequency (eg. 32.768kHz). The FLL is tolerant of jitter and may be used to generate a stable SYSCLK from a less stable input signal.

The FLL can take as input the external MCLK, or ADCLRCLK / DACLRCLK (in Slave modes), or the 32kHz crystal oscillator (or external 32kHz source). The FLL input reference source is selected using the FLL_CLK_SRC, as described in Table 17. Choosing the 32kHz source as an input selects either the 32kHz GPIO input or the internal 32kHz oscillator, as illustrated in Figure 33. For best audio performance, it is recommended that a high frequency input clock (above 1MHz) is used.

The analogue and digital portions of the FLL may be enabled independently via FLL_OSC_ENA and FLL_ENA. When initialising the FLL, the analogue circuit must be enabled first by setting FLL_OSC_ENA. The digital circuit may then be enabled on the next register write or later. When changing FLL settings, it is recommended that the digital circuit be disabled via FLL_ENA and then re-enabled after the other register settings have been updated. When changing the input reference frequency F_{REF}, it is recommended that the FLL be reset by setting FLL_ENA to 0.

The field FLL_RATE controls internal functions within the FLL; it is recommended that only the default setting be used for this parameter. FLL_RSP_RATE controls the internal loop gain and should be set to the recommended value.

The FLL output frequency is directly determined from FLL_RATIO, FLL_OUTDIV and the real number represented by FLL_N and FLL_K. The field FLL_N is an integer (LSB = 1); FLL_K is the fractional portion of the number (MSB = 0.5). The fractional portion is only valid when enabled by the field FLL_FRAC. It is recommended that FLL_FRAC is enabled at all times.

The FLL frequency is determined according to the following equation:

$$F_{OUT} = (F_{VCO} / FLL\_OUTDIV)$$

$$F_{VCO} = (F_{REF} \times N.K \times FLL\_RATIO)$$

F_{VCO} must be in the range 90-100 MHz. The value of FLL_OUTDIV should be selected as follows according to the desired output F_{OUT}.

OUTPUT FREQUENCY F_{OUT}	FLL_OUTDIV
2.8125 MHz - 3.125 MHz	4h (divide by 32)
5.625 MHz - 6.25 MHz	3h (divide by 16)
11.25 MHz - 12.5 MHz	2h (divide by 8)
22.5 MHz - 25 MHz	1h (divide by 4)

Table 16 Choice of FLL_OUTDIV

Note that the output frequencies that do not lie within the ranges quoted above cannot be guaranteed across the full range of device operating temperatures.

Once F_{VCO} has been determined, the value of FLL_RATIO should be selected in accordance with the recommendations in Table 17. The value of N.K can then be determined using the equation above. FLL_REF_FREQ should be set as described in Table 17.

For best performance, FLL Fractional Mode should always be used. Therefore, if the calculations yield an integer value of N.K, then it is recommended to adjust FLL_RATIO in order to obtain a non-integer value of N.K.

The register fields that control the FLL are described in Table 17. Example settings for a variety of reference frequencies and output frequencies are shown in Table 18.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2Ah) FLL Control 1	15	FLL_ENA	0	Digital Enable for FLL 0 = disabled 1 = enabled Note that FLL_OSC_ENA must be enabled before enabling FLL_ENA.
	14	FLL_OSC_ENA	0	Analogue Enable for FLL 0 = FLL disabled 1 = FLL enabled Note that FLL_OSC_ENA must be enabled before enabling FLL_ENA.
	10:8	FLL_OUTDIV [2:0]	010	F_{OUT} clock divider 000 = F_{VCO} / 2 001 = F_{VCO} / 4 010 = F_{VCO} / 8 011 = F_{VCO} / 16 100 = F_{VCO} / 32 101 = Reserved 110 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				111 = Reserved
	7:4	FLL_RSP_RATE	0000	FLL Loop Gain 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that these are not changed from default.
	2:0	FLL_RATE [2:0]	000	Frequency of the FLL control block 000 = F_{VCO} / 1 (Recommended value) 001 = F_{VCO} / 2 010 = F_{VCO} / 4 011 = F_{VCO} / 8 100 = F_{VCO} / 16 101 = F_{VCO} / 32 Recommended that these are not changed from default.
R43 (2Bh) FLL Control 2	15:11	FLL_RATIO [4:0]	14 (0Eh)	CLK_VCO is divided by this integer, valid from 1 .. 31. 1 recommended for high freq reference 8 recommended for low freq reference
	9:0	FLL_N [9:0]	086h	FLL integer multiplier N for CLK_REF
R44 (2Ch) FLL Control 3	15:0	FLL_K [15:0]	C226h	FLL fractional multiplier K for CLK_REF. This is only used if FLL_FRAC is set.
R45 (2Dh) FLL Control 4	7	FLL_REF_FREQ	0	Low frequency reference locking 0 = High frequency reference locking (recommended for reference clock > 48kHz) 1 = Lock frequency reference locking (recommended for reference clock <= 48kHz)
	5	FLL_FRAC	0	Fractional enable 0 = Integer Mode 1 = Fractional Mode 1 recommended in all cases
	1:0	FLL_CLK_SRC [1:0]	00	Select FLL input clock Source 00 = MCLK 01 = DACLRCLK 10 = ADCLRCLK 11 = CLK_32K_REF

Table 17 FLL Control Registers

12.4.1 EXAMPLE FLL CALCULATION

To generate 12.288 MHz output (F_{OUT}) from a 12.000 MHz reference clock (F_{REF}):

- Determine FLL_OUTDIV for the required output frequency as given by Table 16:
  For F_{OUT} = 12.288 MHz, FLL_OUTDIV = 2h (divide by 8)
- Calculate F_{VCO} for the given FLL_OUTDIV:
  $F_{VCO} = F_{OUT}$ * FLL_OUTDIV = 12.288 MHz * 8 = 98.304 MHz
- Calculate the required N.K x FLL_RATIO for the given F_{REF} and F_{VCO}.:
  N.K x FLL_RATIO = F_{VCO} / F_{REF} = 8.192
- Determine FLL_REF_FREQ for the given F_{REF} as given by Table 17:
  For F_{REF} = 12MHz, FLL_REF_FREQ = 0
- Determine FLL_RATIO as given by Table 17:
  For High Frequency Reference, FLL_RATIO = 1
- Calculate N.K for the given FLL_RATIO:
  N.K = 8.192 / 1 = 8.192
- Determine FLL_N and FLL_K from the integer and fractional portions of N.K:
  FLL_N is 8. FLL_K is 0.192
- Set FLL_FRAC according to whether fractional mode is required:
  FLL_K is 0.192, so fractional mode is required; FLL_FRAC = 1

Note that, for best performance, FLL Fractional Mode should always be used. If the calculations yield an integer value of N.K, then it is recommended to adjust FLL_RATIO in order to obtain a non-integer value of N.K.

12.4.2 EXAMPLE FLL SETTINGS

Table 18 provides example FLL settings for generating common SYSCLK frequencies from a variety of low and high frequency reference inputs.

F_{REF}	F_{OUT}	F_{VCO}	FLL_N	FLL_K	FLL_ RATIO	FLL_ OUTDIV	FLL_FRAC	FLL_REF_ FREQ
32.000 kHz	12.288 MHz	98.304 MHz	438 (1B6h)	0.857143 (DB6Eh)	7	2h (divide by 8)	1	1
32.000 kHz	11.2896 MHz	90.3168 MHz	352 (160h)	0.8 (CCCCh)	8	2h (divide by 8)	1	1
32.768 kHz	12.288 MHz	98.304 MHz	428 (1ACh)	0.571429 (9249 h)	7	2h (divide by 8)	1	1
32.768 kHz	11.288576 MHz	90.308608 MHz	344 (158h)	0.500000 (8000 h)	8	2h (divide by 8)	1	1
32.768 kHz	11.2896 MHz	90.3168 MHz	344 (158h)	0.53125 (8800h)	8	2h (divide by 8)	1	1
48 kHz	12.288 MHz	98.304 MHz	292 (124h)	0.571429 (9249 h)	7	2h (divide by 8)	1	1
11.3636 MHz	12.368544 MHz	98.948354 MHz	8 (008h)	0.707483 (B51Dh)	1	2h (divide by 8)	1	0
12.000 MHz	12.288 MHz	98.3040 MHz	8 (008h)	0.192 (3127h)	1	2h (divide by 8)	1	0
12.000 MHz	11.289597 MHz	90.3168 MHz	7 (007h)	0.526398 (86C2h)	1	2h (divide by 8)	1	0
12.288 MHz	12.288 MHz	98.304 MHz	2 (002h)	0.666667 (AAABh)	3	2h (divide by 8)	1	0
12.288 MHz	11.2896 MHz	90.3168 MHz	7 (007h)	0.35 (599Ah)	1	2h (divide by 8)	1	0
13.000 MHz	12.287990 MHz	98.3040 MHz	7 (007h)	0.56184 (8FD5h)	1	2h (divide by 8)	1	0
13.000 MHz	11.289606 MHz	90.3168 MHz	6 (006h)	0.94745 (F28Ch)	1	2h (divide by 8)	1	0
19.200 MHz	12.287988 MHz	98.3040 MHz	5 (005h)	0.119995 (1EB8h)	1	2h (divide by 8)	1	0
19.200 MHz	11.289588 MHz	90.3168 MHz	4 (004h)	0.703995 (B439h)	1	2h (divide by 8)	1	0

Table 18 Example FLL Settings

13 AUDIO CODEC SUBSYSTEM

13.1 GENERAL DESCRIPTION

The WM8351 includes a high-performance stereo CODEC. Analogue output buffers and input amplifiers are integrated on-chip, enabling the WM8351 to connect directly to headphones and microphones as well as line-in and line-out sockets.

The CODEC handles analogue-to-digital and digital-to-analogue conversion for audio signals, and integrates programmable filtering. Analogue mixing capabilities are also provided.

Digital audio data is transferred to and from the audio CODEC through a dedicated audio interface that supports a number of industry-standard data formats.

Electrical power is provided to the CODEC through the following pins:

- DBVDD and DGND – for the CODEC's audio interface
- DCVDD and DGND – for the CODEC's digital core
- HPVDD and HPGND – for the analogue outputs
- AVDD and REF_GND – for ADC and DAC references
- AVDD and GND – for all other analogue functions (including input amplifiers and buffers, ADC, DAC, and analogue mixers)

13.2 AUDIO PATHS

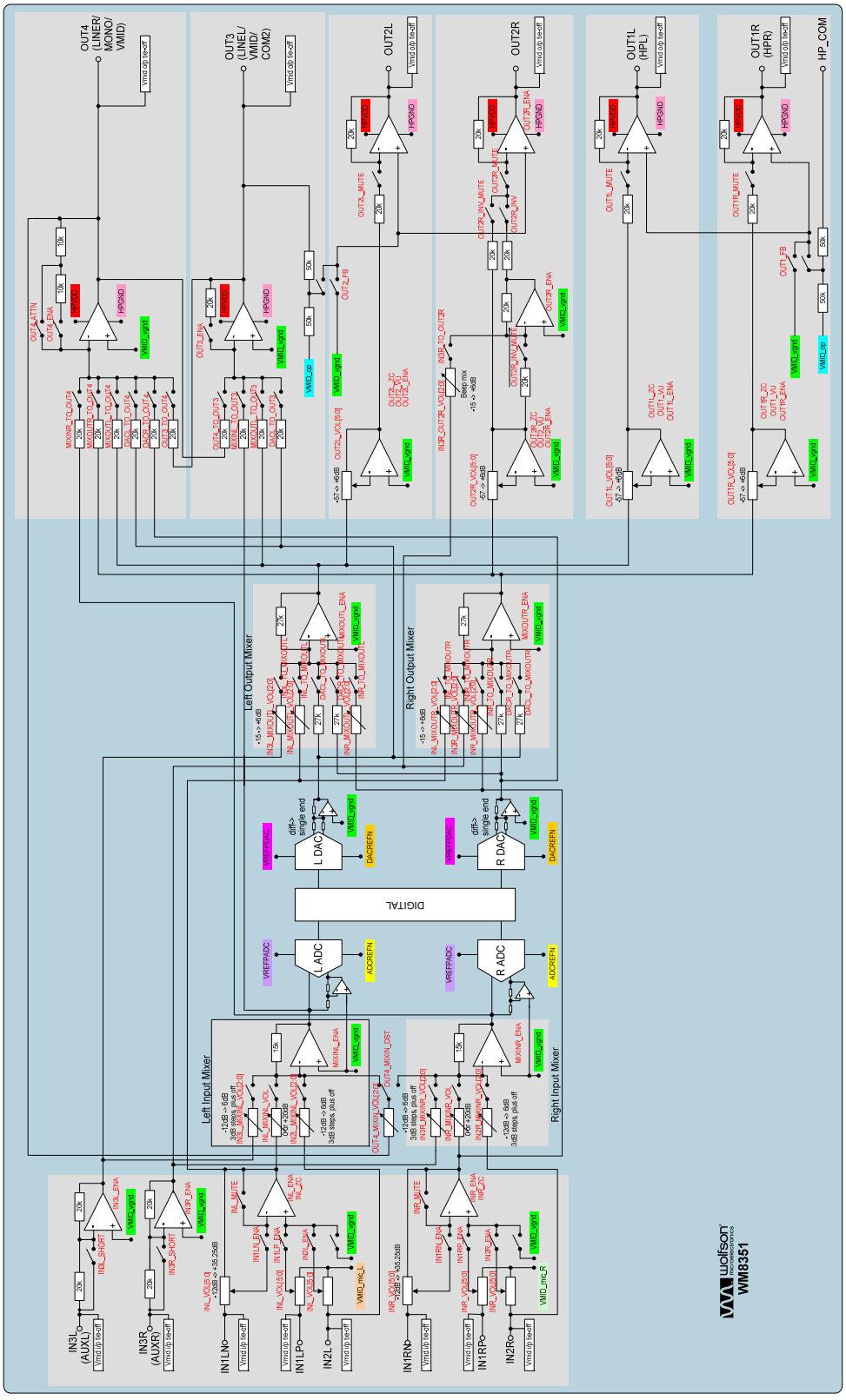


Figure 36 WM8351 Audio Path Diagram

13.3 ENABLING THE AUDIO CODEC

Before the audio CODEC can be used, it must be enabled by writing to the CODEC_ENA, SYSCLK_ENA and BIAS_ENA register bits.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) Power Mgmt 5	12	CODEC_ENA	0	Master codec enable bit. Until this bit is set, all codec registers are held in reset. 0 = All codec registers held in reset 1 = Codec registers operate normally.
R11 (0Bh) Power Mgmt 4	14	SYSCLK_ENA	0	CODEC SYSCLK enable 0 = disabled 1 = enabled
R8 (08h) Power Mgmt 1	5	BIAS_ENA	0	Enables bias to analogue audio CODEC circuitry 0 = disabled 1 = enabled

Table 19 Enabling the Audio CODEC

Each individual part of the audio CODEC (e.g. left/right ADC, left/right DAC, each analogue output pin, mic bias etc.) also has its own enable bit, which must be set before that part of the CODEC can be used. These enable bits are described in the sections that follow.

In order to minimize output pop and click noise, it is recommended that the WM8351 device is powered up and down under control using the following sequences:

Power Up:

1. Ensure the CODEC power supplies are available before the CODEC is enabled R12[CODEC_ENA]=1 . The order in which this is done should be DCVDD, DBVDD then HPAVVD And/Or AVDD
2. Mute all outputs
3. Enable the anti-pop circuits by setting ANTI_POP. There are three Anti-pop setting options. Recommended value is ANTI_POP = 01.
4. Ensure external capacitors are full discharged on all outputs that are used by delaying 250ms
5. Set the mixers and DAC volume to required settings
6. Enable VMID by setting VMID_ENA = 1. VMID should raise in a controlled fashion and charge the output capacitors
7. Wait approx 500ms to allow VMID to charge.
8. Disable the anti-pop circuits by setting ANTI_POP = 00.
9. Un-mute all outputs

Power Down:

1. Mute all outputs
2. Enable anti-pop circuits by setting ANTI_POP to the appropriate value.
3. Disable circuits down-stream on outputs
4. Disable VMID by setting VMID_ENA = 0
5. Wait for VMID to discharge (typically 500ms)
6. Disable the anti-pop circuits by setting ANTI_POP = 00
7. Disable all outputs

13.4 INPUT SIGNAL PATH

The WM8351 has multiple analogue inputs. There are two input channels, Left and Right, each of which consists of an input PGA stage followed by a boost/mix stage switch into the hi-fi ADC. Each input PGA path has three input pins which can be configured in a variety of ways to accommodate single-ended, differential or dual differential microphones. There are two auxiliary input pins which can be fed into to the input boost/mix stage as well as driving into the output path. A bypass path exists from the output of the boost/mix stage into the output left/right mixers.

13.4.1 MICROPHONE INPUTS

The microphone inputs of the WM8351 are designed to accommodate electret condenser microphones or analogue line-in signals. They comprise the following pins:

- IN1LP: first non-inverting input, left channel
- IN2L: second non-inverting input, left channel
- IN1LN: inverting input, left channel
- IN1RP: first non-inverting input, right channel
- IN2R: second non-inverting input, right channel
- IN1RN: inverting input, right channel

The non-inverting inputs have constant input impedance to VMID, whereas the inverting input's impedance varies with the pre-amplifier's gain. (Note: the terms "inverting" and "non-inverting" refer to the microphone pre-amplifiers only. For overall behaviour, the inverting record mixer and the ADC, whose output can optionally be inverted in the digital domain, must also be taken into account.)

Each channel has a programmable pre-amplifier, which supports single-ended or pseudo-differentially connected microphones. The amplified signal for each channel can be digitised in the audio ADC and/or mixed into the output signal path.

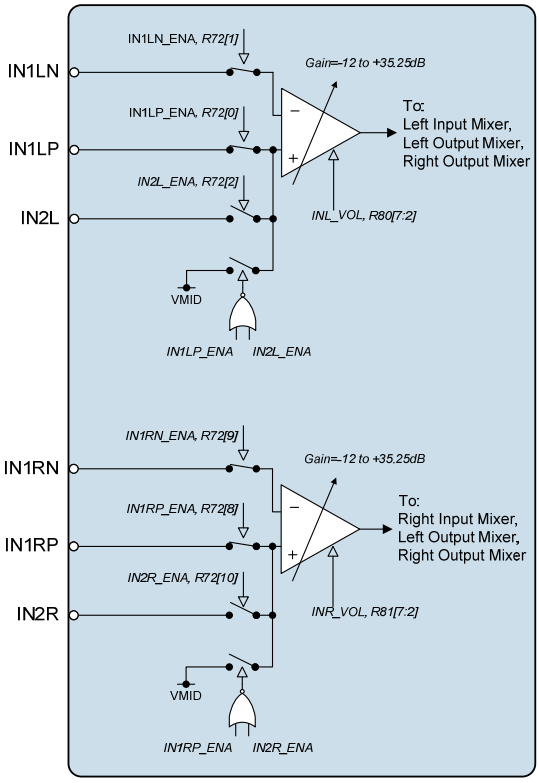


Figure 37 Microphone Inputs and Pre-amplifiers

13.4.2 ENABLING THE PRE-AMPLIFIERS

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) Power Mgmt 2	8	INL_ENA	0	Left input PGA enable 0 = disabled 1 = enabled
	9	INR_ENA	0	Right input PGA enable 0 = disabled 1 = enabled
R80 (50h) Left Input Volume	15	INL_ENA	0	Left input PGA enable 0 = disabled 1 = enabled
R81 (51h) Right Input Volume	15	INR_ENA	0	Right input PGA enable 0 = disabled 1 = enabled
Note: These bits can be accessed through R9 or through R80/R81. Reading from or writing to either register location has the same effect.				

Table 20 Enabling the Microphone Pre-amplifiers

13.4.3 SELECTING INPUT SIGNALS

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R72 (48h) Mic Input Control	0	IN1LP_ENA	1	Connect IN1LP pin to left channel input PGA amplifier positive terminal. 0 = IN1LP not connected to input PGA 1 = input PGA amplifier positive terminal connected to IN1LP (constant input impedance)
	1	IN1LN_ENA	1	Connect IN1LN pin to left channel input PGA negative terminal. 0 = IN1LN not connected to input PGA 1 = IN1LN connected to input PGA amplifier negative terminal.
	2	IN2L_ENA	0	Connect IN2L pin to left channel input PGA amplifier 0 = IN2L not connected to input PGA amplifier 1 = IN2L connected to input PGA amplifier
	8	IN1RP_ENA	1	Connect IN1RP pin to right channel input PGA amplifier positive terminal. 0 = IN1RP not connected to input PGA 1 = right channel input PGA amplifier positive terminal connected to IN1RP (constant input impedance)
	9	IN1RN_ENA	1	Connect IN1RN pin to right channel input PGA negative terminal. 0 = IN1RN not connected to input PGA 1 = IN1RN connected to right channel input PGA amplifier negative terminal.
	10	IN2R_ENA	0	Connect IN2R pin to right channel input PGA 0 = IN2R not connected to input PGA amplifier 1 = IN2R connected to input PGA amplifier

Table 21 Selecting Input Pins for the Microphone Pre-amplifiers

13.4.4 CONTROLLING THE PRE-AMPLIFIER GAINS

The gain of each microphone pre-amplifier is controlled by writing to the appropriate control registers. The gain of each pre-amplifier applies to all three inputs associated with that pre-amplifier, whether inverting or non-inverting. Although the gain settings for each pre-amplifier are in two separate registers, both gains can be changed simultaneously using the IN_VU bit (see Table 22). Additionally, it is also possible to control the gain updates to occur when the respective signal crosses through zero. This feature reduces clicking noise caused by gain changes.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R80 (50h) Left Input Volume	14	INL_MUTE	0	Mute control for left channel input PGA: 0 = Input PGA not muted, normal operation 1 = Input PGA muted (and disconnected from the following input record mixer).
	13	INL_ZC	0	Left channel input PGA zero cross enable: 0 = Update gain when gain register changes 1 = Update gain on 1st zero cross after gain register write.
	8	IN_VU	0	Input left PGA and input right PGA volume do not update until a 1 is written either IN_VU register bit.
	7:2	INL_VOL [5:0]	01_0000	Left channel input PGA volume 000000 = -12dB 000001 = -11.25db . 010000 = 0dB . 111111 = 35.25dB
R81 (51h) Right Input Volume	14	INR_MUTE	0	Mute control for right channel input PGA: 0 = Input PGA not muted, normal operation 1 = Input PGA muted (and disconnected from the following input record mixer).
	13	INR_ZC	0	Right channel input PGA zero cross enable: 0 = Update gain when gain register changes 1 = Update gain on 1st zero cross after gain register write.
	8	IN_VU	0	Input left PGA and input right PGA volume do not update until a 1 is written either IN_VU register bit.
	7:2	INR_VOL [5:0]	01_0000	Right channel input PGA volume 000000 = -12dB 000001 = -11.25db . 010000 = 0dB . 111111 = 35.25dB

Table 22 Controlling the Microphone Pre-amplifier Gain

13.4.5 MICROPHONE BIASING

The WM8351 provides a programmable, low-noise bias voltage for condenser electret microphones on the MICBIAS pin.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Power Mgmt 1	4	MICB_ENA	0	Microphone bias enable 0 = OFF (high impedance output) 1 = ON This bit can be accessed through R8 or through R74. Reading from or writing to either register location has the same effect.
R74 (4Ah) Mic Bias Control	15	MICB_ENA		
	14	MICB_SEL	0	Microphone bias voltage control: 0 = 0.9 * AVDD 1 = 0.75 * AVDD
Note: MICB_ENA can be accessed through R8 or through R74. Reading from or writing to either register location has the same effect.				

Table 23 Controlling the Microphone Bias Voltage

13.4.6 AUXILIARY INPUTS (IN3L AND IN3R)

The WM8351 provides two additional analogue input pins, IN3L and IN3R, for line-level audio or "beep" signals. Each pin has a simple input buffer whose output signal can be digitised in the audio ADC and/or mixed into the output signal path. The Right input IN3R may also be connected to the Output Beep Mixer, for output on OUT2R (see Table 43). The input buffers have a nominal default gain of -1 (0dB).

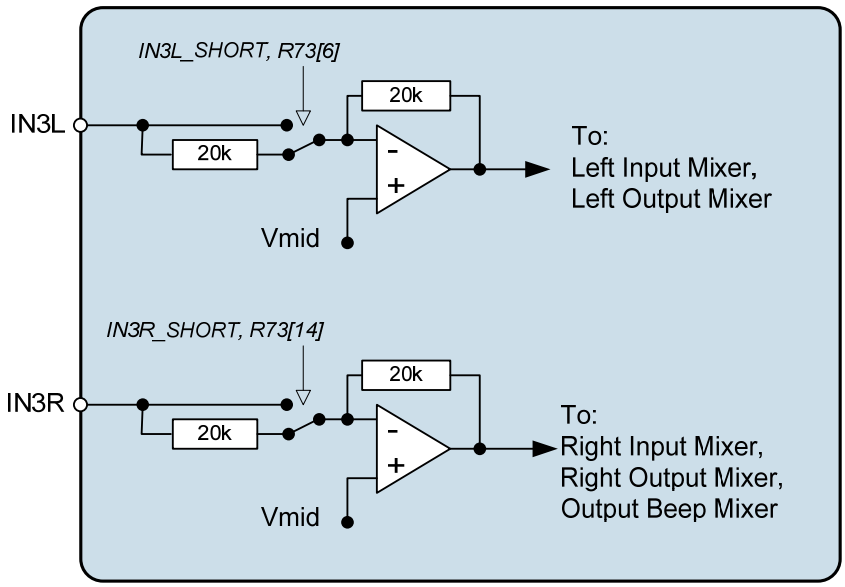


Figure 38 Auxiliary Input Buffers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) Power Mgmt 2	10	IN3L_ENA	0	IN3L Amplifier enable 0 = disabled 1 = enabled
	11	IN3R_ENA	0	IN3R Amplifier enable 0 = disabled 1 = enabled
R73 (49h) IN3 Input Control	7	IN3L_ENA	0	IN3L Amplifier enable 0 = disabled 1 = enabled
	15	IN3R_ENA	0	IN3R Amplifier enable 0 = disabled 1 = enabled
	6	IN3L_SHORT	0	Short circuit internal input resistor for IN3L amplifier. 0 = Internal resistor in circuit 1 = Internal resistor shorted
	14	IN3R_SHORT	0	Short circuit internal input resistor for IN3R amplifier. 0 = Internal resistor in circuit 1 = Internal resistor shorted
Note: IN3L_ENA and IN3R_ENA can be accessed through R9 or through R73. Reading from or writing to either register location has the same effect.				

Table 24 Controlling the Auxiliary Input Buffers

13.4.7 INPUT MIXERS

The WM8351 has mixers in the input signal paths. This allows each ADC to record either a single input signal or a mix of several signals, as desired. The gain for the different input signals can also be adjusted. Each record mixer has four inputs:

- the output of the respective (left/right) microphone pre-amplifier
- the IN2L and IN2R pins (used as a line input, bypassing the microphone pre-amplifiers)
- the output of the respective (left/right) auxiliary input buffer (ie. inputs IN3L or IN3R)
- the output of the OUT4 amplifier (only one input mixer at a time can take this signal)

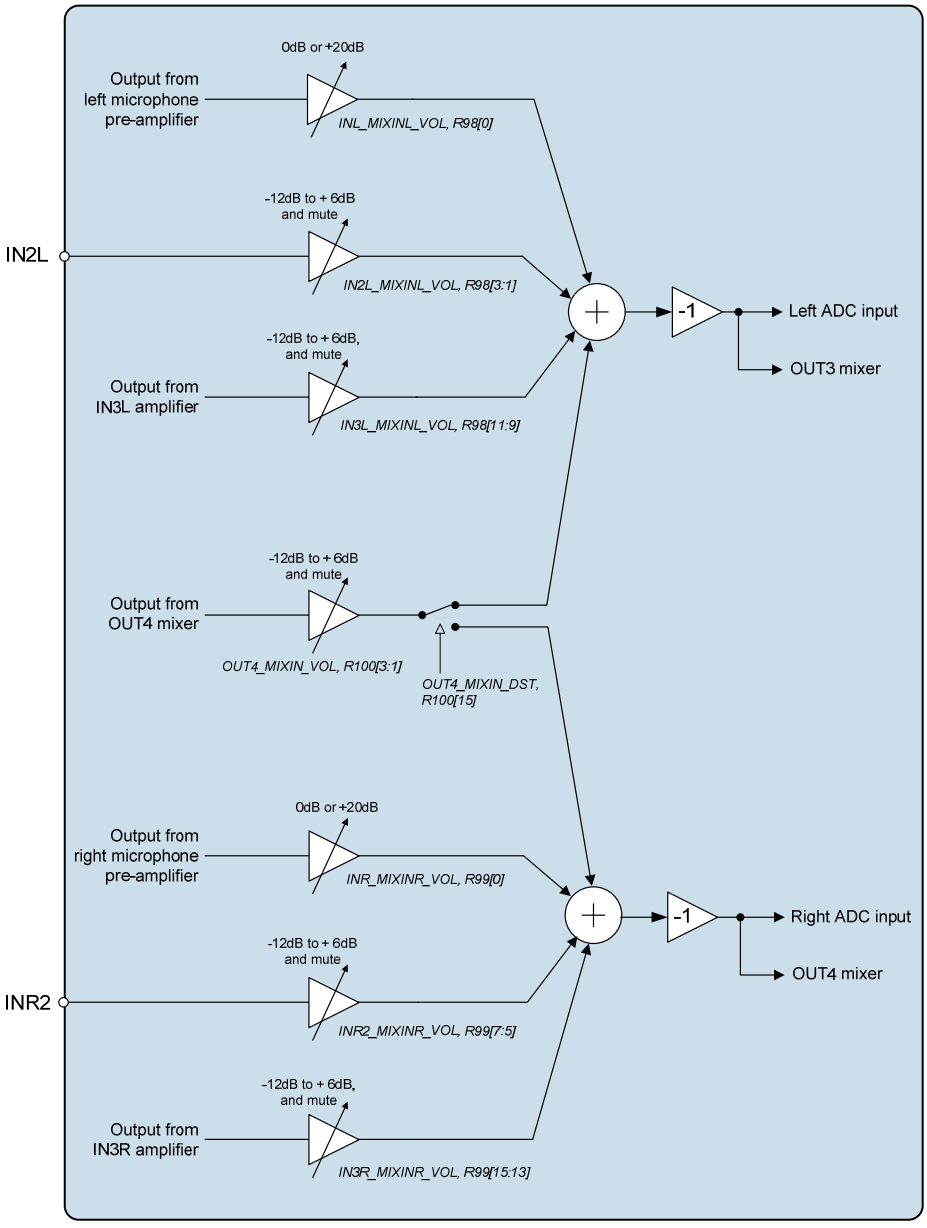


Figure 39 Input Mixers

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) Power Mgmt 2	7	MIXINR_ENA	0	Right input mixer enable 0 = disabled 1 = enabled
	6	MIXINL_ENA	0	Left input mixer enable 0 = disabled 1 = enabled
R98 (62h) Input mixer volume for left channel	0	INL_MIXINL_VOL	0	Boost enable for left channel input PGA: 0 = PGA output has +0dB gain through input record mixer. 1 = PGA output has +20dB gain through input record mixer.
	3:1	IN2L_MIXINL_VOL [2:0]	000	IN2L amplifier volume control to right input mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer
	11:9	IN3L_MIXINL_VOL	000	IN3L amplifier volume control to right input mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer
R99 (63h) Input mixer volume for right channel	0	INR_MIXINR_VOL	1	Boost enable for right channel input PGA: 0 = PGA output has +0dB gain through input record mixer. 1 = PGA output has +20dB gain through input record mixer.
	7:5	IN2R_MIXINR_VOL [2:0]	000	IN2R amplifier volume control to right input mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer
	15:13	IN3R_MIXINR_VOL [2:0]	000	IN3R amplifier volume control to right input mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer
R100 (64h) OUT4 Mixer Control	15	OUT4_MIXIN_DST	0	Select routing of OUT4 to input mixers. 0 = OUT4 to left input mixer. 1 = OUT4 to right input mixer.
	3:1	OUT4_MIXIN_VOL [2:0]	000	Controls the gain of OUT4 to left and right input mixers: 000 = Path disabled (left and right mute) 001 = -12dB gain through boost stages 010 = -9dB gain through boost stages …. 111 = +6dB gain through boost stages

Table 25 Input Mixer Control

13.5 ANALOGUE TO DIGITAL CONVERTER (ADC)

The high-performance stereo ADC within the WM8351 converts analogue input signals to the digital domain. It uses a multi-bit, over-sampled sigma-delta architecture. The ADC's over-sampling rate is selectable to control the trade-off between best audio performance and lowest power consumption. A variety of digital filtering stages process the ADC's digital output signal before it is sent to the WM8351 audio interface. These include:

- digital decimation and filtering needed for the ADC
- digital volume control
- A programmable high-pass filter

The audio ADC supports all commonly used audio sampling rates between 8kHz and 48kHz (see Figure 40).

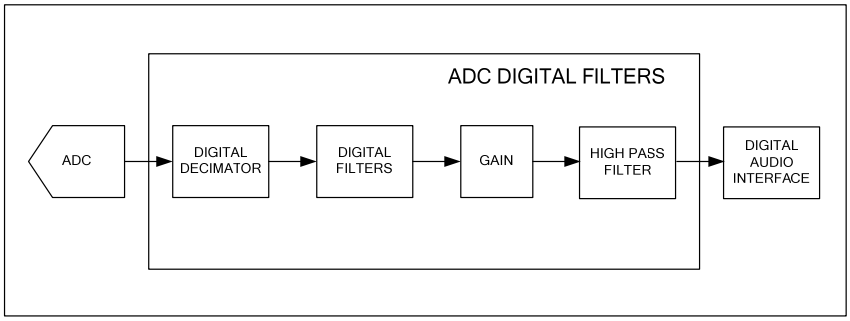


Figure 40 ADC Digital Filter Path

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh) Power Mgmt 4	2	ADCL_ENA	0	Left ADC enable 0 = disabled 1 = enabled When ADCR and ADCL are used together as a stereo pair, then both ADCs must be enabled together using a single register write to Register R11 (0Bh).
R66 (42h) ADC Digital Volume L	15			
R11 (0Bh) Power Mgmt 4	3	ADCR_ENA	0	Right ADC enable 0 = disabled 1 = enabled When ADCR and ADCL are used together as a stereo pair, then both ADCs must be enabled together using a single register write to Register R11 (0Bh).
R67 (43h) ADC Digital Volume R	15			
R64 (40h) ADC Control	1	ADCL_DATINV	0	ADC Left channel polarity: 0 = Normal 1 = Inverted
	0	ADCR_DATINV	0	ADC Right Channel Polarity 0 = Normal 1 = Inverted
Note: ADCL_ENA and ADCR_ENA can be accessed through R11 or through R66/R67. Reading from or writing to either register location has the same effect.				

Table 26 Enabling the ADC Left and Right Channels

When ADCR and ADCL are used together as a stereo pair, then it is important that ADCR_ENA and ADCL_ENA are enabled at the same time using a single register write. This must be implemented by writing to the bits in Register R11 (0Bh). This ensures that the system starts up both channels in a synchronous manner.

13.5.1 ADC VOLUME CONTROL

Programmable digital volume control is provided to attenuate the ADC's output signal.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R66 (42h) ADC Digital Volume L	8	ADC_VU	0	ADC left and ADC right volume do not update until a 1 is written to either ADC_VU register bit.
	7:0	ADCL_VOL [7:0]	1100_0000	Left ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -71.625dB 0000 0010 = -71.25dB ... 0.375dB steps up to 1110 1111 = +17.625dB
R67 (43h) ADC Digital Volume R	8	ADC_VU	0	ADC left and ADC right volume do not update until a 1 is written to either ADC_VU register bit.
	7:0	ADCR_VOL [7:0]	1100_0000	Right ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -71.625dB 0000 0010 = -71.25dB ... 0.375dB steps up to 1110 1111 = +17.625dB

Table 27 ADC Volume Control

13.5.2 ADC HIGH-PASS FILTER

A digital high-pass filter is provided to remove DC offsets from the ADC signal.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh) Power Mgmt 4	13	ADC_HPF_ENA	0	High Pass Filter enable 0 = disabled 1 = enabled This bit can be accessed through R11 or through R64. Reading from or writing to either register location has the same effect.
R64 (40h) ADC Control	15			
	9:8	ADC_HPF_CUT [1:0]	00	Select cut-off frequency for high-pass filter 00 = 2^-11 (first order) = 3.7Hz @ fs=44.1kHz 01 = 2^-5 (2nd order) = ~250Hz @ fs=8kHz 10 = 2^-4 (2nd order) = ~250Hz @ fs=16kHz 11 = 2^-3 (2nd order) = ~250Hz @ fs=32kHz
Note: ADC_HPF_ENA can be accessed through R11 or through R64. Reading from or writing to either register location has the same effect.				

Table 28 Controlling the ADC High-pass Filter

13.6 DIGITAL MIXING

13.6.1 DIGITAL SIDETONE

A digital sidetone is available when ADCs and DACs are operating at the same sample rate. Digital data from either left or right ADC can be mixed with the audio interface data on the left and right DAC channels. Sidetone data is taken from the ADC high pass filter output, to reduce low frequency noise in the sidetone (e.g. wind noise or mechanical vibration).

The digital sidetone will not function when ADCs and DACs are operating at different sample rates.

When using the digital sidetone, it is recommended that the ADCs are enabled before un-muting the DACs to prevent pop noise. The DAC volumes and sidetone volumes should be set to an appropriate level to avoid clipping at the DAC input.

The digital sidetone is controlled as shown Table 29.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R68 (44h) ADC Divider	11:8	ADCL_DAC_SVOL [3:0]	0000	Left Digital Side tone Volume in dB (See Table 30 for volume range)
	7:4	ADCR_DAC_SVOL [3:0]	0000	Right Digital Side tone Volume in dB (See Table 30 for volume range)
R60 (3Ch) Digital Side Tone Control	13:12	ADC_TO_DACL [1:0]	00	DAC Left Side-tone Control 11 = Unused 10 = Mix ADCR into DACL 01 = Mix ADCL into DACL 00 = No Side-tone mix into DACL
	11:10	ADC_TO_DACR [1:0]	00	DAC Right Side-tone Control 11 = Unused 10 = Mix ADCR into DACR 01 = Mix ADCL into DACR 00 = No Side-tone mix into DACR

Table 29 Digital Side Tone Control

The coding of ADCL_DAC_SVOL and ADCR_DAC_SVOL is described in Table 30.

ADCL_DAC_SVOL or ADCR_DAC_SVOL	SIDETONE VOLUME
0000	-36
0001	-33
0010	-30
0011	-27
0100	-24
0101	-21
0110	-18
0111	-15
1000	-12
1001	-9
1010	-6
1011	-3
1100	0
1101	0
1110	0
1111	0

Table 30 Digital Side Tone Control

13.7 DIGITAL TO ANALOGUE CONVERTER (DAC)

The WM8351 contains a high-performance stereo DAC to convert digital audio signals to the analogue domain. Audio data is passed to the WM8351 via the audio interface, and passes through a variety of digital filtering stages before reaching the DAC. These include:

- Digital volume control
- Digital filtering, interpolation and sigma-delta modulation functions needed for the DAC

The audio DAC supports all commonly used audio sampling rates between 8kHz and 48kHz.

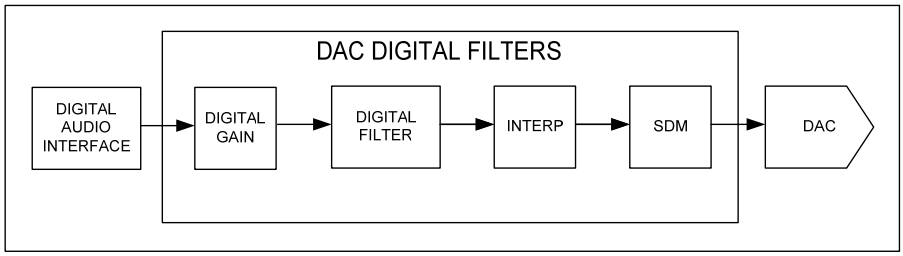


Figure 41 DAC Overview

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh) Power Mgmt 4	4	DACL_ENA	0	Left DAC enable 0 = disabled 1 = enabled
R50 (32h) DAC Digital Volume Left	15			
R11 (0Bh) Power Mgmt 4	5	DACR_ENA	0	Right DAC enable 0 = disabled 1 = enabled
R51 (33h) DAC Digital Volume Right	15			
Note: These bits can be accessed through R11 or through R50/R51. Reading from or writing to either register location has the same effect.				

Table 31 DAC Enable

13.7.1 DAC PLAYBACK VOLUME CONTROL

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R50 (32h) DAC Digital Volume Left	8	DAC_VU	0	DAC left and DAC right volume do not update until a 1 is written to either DAC_VU register bit.
	7:0	DACL_VOL [7:0]	1100_0000	Left DAC digital volume control: 0000_0000 = Digital mute 0000_0001 = -71.625dB 0000_0010 = -71.25dB … (0.375dB steps) 1100_000 = 0dB
R51 (33h) DAC Digital Volume Right	8	DAC_VU	0	DAC left and DAC right volume do not update until a 1 is written to either DAC_VU register bit.
	7:0	DACR_VOL [7:0]	1100_0000	Right DAC digital volume control: 0000_0000 = Digital mute 0000_0001 = -71.625dB 0000_0010 = -71.25dB … (0.375dB steps) 1100_000 = 0dB

Table 32 DAC Volume Control

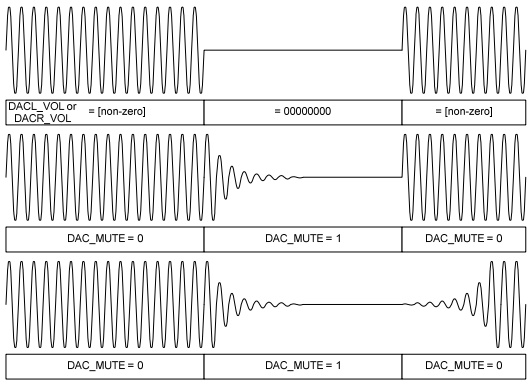
13.7.2 DAC SOFT MUTE AND SOFT UN-MUTE

The WM8351 has a soft mute function which, when enabled, gradually attenuates the volume of the DAC output. When soft mute is disabled, the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DAC_MUTEMODE register bit.

The DAC is soft-muted by default (DAC_MUTE = 1). To play back an audio signal, this function must first be disabled by setting DAC_MUTE to 0.

Soft Mute Mode would typically be enabled (DAC_MUTEMODE = 1) when using DAC_MUTE during playback of audio data so that when DAC_MUTE is subsequently disabled, the sudden volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing during a track).

Soft Mute Mode would typically be disabled (DAC_MUTEMODE = 0) when un-muting at the start of a music file, in order that the first part of the track is not attenuated (e.g. when starting playback of a new track, or resuming playback after pausing between tracks).



DAC muting and un-muting using volume control bits DACL_VOL and DACR_VOL.

DAC muting and un-muting using soft mute bit DAC_MUTE. Soft un-mute not enabled (DAC_MUTEMODE = 0).

DAC muting and un-muting using soft mute bit DAC_MUTE. Soft un-mute enabled (DAC_MUTEMODE = 1).

Figure 42 DAC Mute Control

The volume ramp rate during soft mute and un-mute is controlled by the DAC_MUTERATE bit. Ramp rates of fs/32 and fs/2 are selectable as shown

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R58 (3Ah) DAC Mute	14	DAC_MUTE	1	DAC Mute 0 = disabled 1 = enabled
R59 (3Bh) DAC Mute Volume	14	DAC_MUTEMODE	0	DAC Soft Mute Mode 0 = Disabling soft-mute (DAC_MUTE=0) will cause the volume to change immediately to the DACL_VOL / DACR_VOL settings 1 = Disabling soft-mute (DAC_MUTE=0) will cause the volume to ramp up gradually to the DACL_VOL / DACR_VOL settings
	13	DAC_MUTERATE	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (24kHz at fs=48k, providing maximum delay of 10.7ms) 1 = Slow ramp (1.5kHz at fs=48k, providing maximum delay of 171ms)

Table 33 DAC Soft-Mute Control

13.7.3 DAC DE-EMPHASIS

Digital de-emphasis can be applied to the DAC playback data (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (30h) DAC Control	5:4	DEEMP [1:0]	00	De-Emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No de-emphasis

Table 34 DAC De-Emphasis Control

13.7.4 DAC OUTPUT PHASE AND MONO MIXING

The digital audio data is converted to oversampled bit streams in the on-chip 24-bit digital interpolation filters. The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

In normal operation, the left and right channel digital audio data is converted to analogue in two separate DACs. It is also possible for the DACs to output a mono mix of left and right channels, using DAC_MONO. Both DACs must be enabled for this mono mix to function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (30h) DAC Control	13	DAC_MONO	0	Adds left and right channel and halves the resulting output to create a mono output
	1	DACL_DATINV	0	DAC data left channel polarity 0 = Normal 1 = Inverted
	0	DACR_DATINV	0	DAC data right channel polarity 0 = Normal 1 = Inverted

Table 35 DAC Mono Mix and Phase Invert Select

13.7.5 DAC STOPBAND ATTENUATION

The DAC digital filter type is selected by the DAC_SB_FILT register bit as shown in Table 36.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R59 (3Bh) DAC Digital Control	12	DAC_SB_FILT	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband mode

Table 36 DAC Filter Selection

13.8 OUTPUT SIGNAL PATH

The analogue output pins produce audio signals to drive headphones, line-out connections and/or external loudspeaker amplifiers. These pins include:

- OUT1L and OUT1R
- OUT2L and OUT2R
- OUT3 and OUT4

OUT1L, OUT1R, OUT2L and OUT2R have individual analogue volume PGAs with -57dB to +6dB ranges. AC-coupled and Capless headphone drive modes are available. Common mode noise rejection is possible using the HPCOM connection.

OUT3 and OUT4 can be configured as a stereo line out (OUT3 is left output and OUT4 is right output). OUT3 and OUT4 can also be used as a Vmid buffer to provide a "ground" reference for headphone outputs, eliminating the need for DC blocking capacitors.

Alternatively, OUT4 can be used to provide a mono mix of left and right channels.

All analogue output pins are powered through the HPVDD and HPGND pins.

Each output can drive a headphone load down to 16Ω.

There are four output mixers in the output signal path: the left and right channel mixers which control the signals to headphone (and optionally the line outputs) and also dedicated OUT3 and OUT4 mixers.

13.8.1 ENABLING THE ANALOGUE OUTPUTS

Each output can be individually enabled or disabled via dedicated control bits.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah)	0	OUT1L_ENA	0	OUT1L enable
R104 (68h)	15			0 = disabled 1 = enabled
R10 (0Ah)	1	OUT1R_ENA	0	OUT1R enable
R105 (69h)	15			0 = disabled 1 = enabled
R10 (0Ah)	2	OUT2L_ENA	0	OUT2L enable
R106 (70h)	15			0 = disabled 1 = enabled
R10 (0Ah)	3	OUT2R_ENA	0	OUT2R enable
R107 (71h)	15			0 = disabled 1 = enabled
R9 (09h)	4	OUT3_ENA	0	OUT3 enable
R92 (5Ch)	15			0 = disabled 1 = enabled
R9 (09h)	5	OUT4_ENA	0	OUT4 enable
R93 (5Dh)	15			0 = disabled 1 = enabled
Note: Each bit can be accessed through two separate control registers. Reading from or writing to either register location has the same effect.				

Table 37 Enabling the Analogue Outputs

13.8.2 OUTPUT MIXERS

The left and right output channel mixers are shown in Figure 43. These mixers allow the AUX inputs, the ADC bypass and the DAC left and right channels to be combined as desired. This allows a mono mix of the DAC channels to be done as well as mixing in external line-in from the IN3.

The IN3L/IN3R and PGA inputs have individual volume control from -15dB to +6dB. The DAC channel volumes can be adjusted in the digital domain if required. The outputs of these mixers are routed to OUT1L/OUT1R or OUT2L/OUT2R. They can also optionally be routed to the OUT3 and OUT4 mixers.

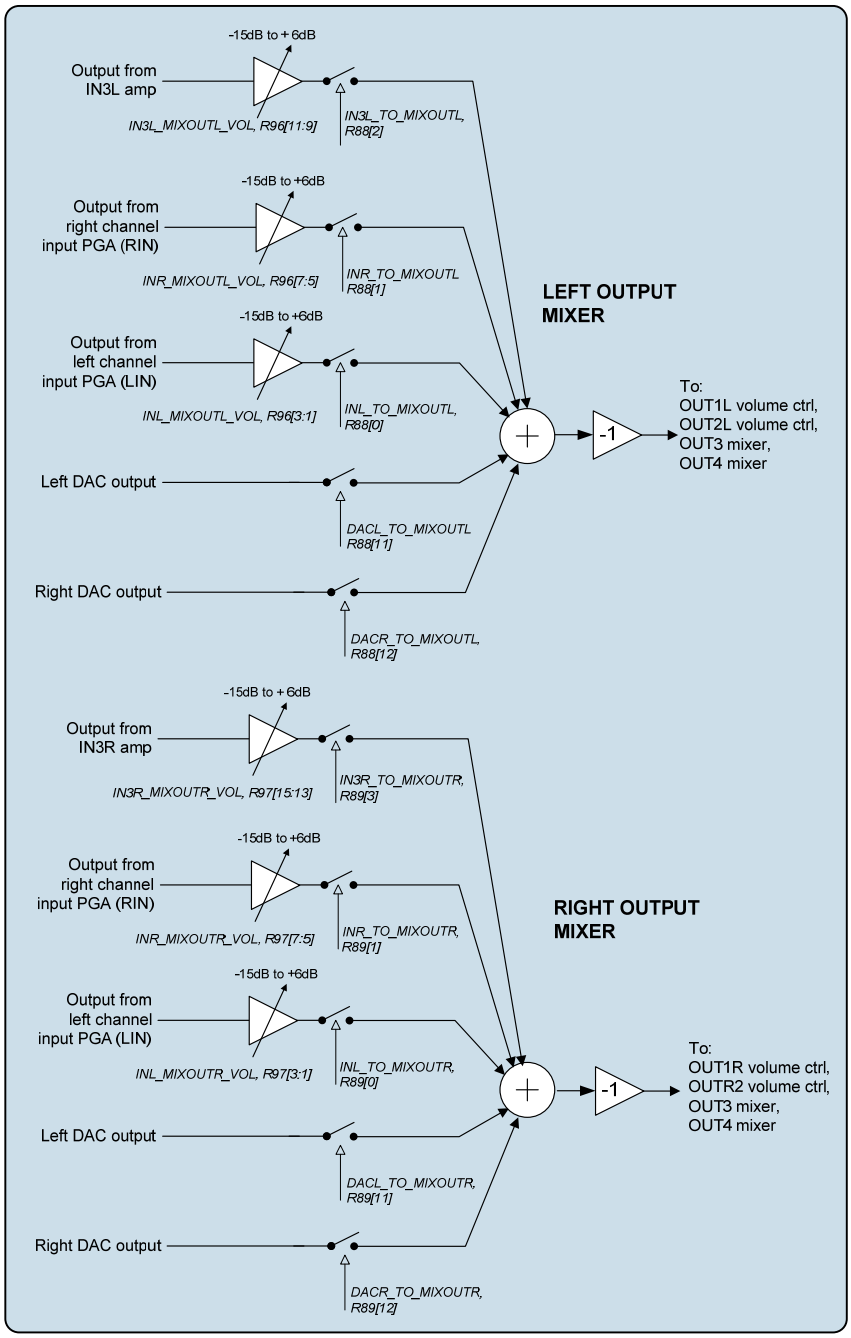


Figure 43 Output Mixers

Each output mixer can be enabled or disabled by writing either to the power management control register or to the respective mixer's own control register. Each analogue signal going into the output mixers can be independently enabled or muted for each mixer.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R88 (58h) Left Mixer Control	0	INL_TO_MIXOUTL	0	Left input PGA output to left output mixer 0 = not selected 1 = selected
	1	INR_TO_MIXOUTL	0	Right input PGA output to left output mixer 0 = not selected 1 = selected
	2	IN3L_TO_MIXOUTL	0	IN3L amplifier output to left channel output mixer: 0 = not selected 1 = selected
	11	DACL_TO_MIXOUTL	0	Left DAC output to left output mixer 0 = not selected 1 = selected
	12	DACR_TO_MIXOUTL	0	Right DAC output to left output mixer 0 = not selected 1 = selected
	15	MIXOUTL_ENA	0	Left output channel mixer enable 0 = disabled 1 = enabled
R9 (09h) Power Mgmt 2	0			
R89 (59h) Right Mixer Control	0	INL_TO_MIXOUTR	0	Left input PGA output to right output mixer 0 = not selected 1 = selected
	1	INR_TO_MIXOUTR	0	Right input PGA output to right output mixer 0 = not selected 1 = selected
	3	IN3L_TO_MIXOUTR	0	IN3L amplifier output to left channel output mixer: 0 = not selected 1 = selected
	11	DACL_TO_MIXOUTR	0	Left DAC output to right output mixer 0 = not selected 1 = selected
	12	DACR_TO_MIXOUTR	0	Right DAC output to right output mixer 0 = not selected 1 = selected
	15	MIXOUTR_ENA	0	Right Output Mixer Enable 0 = disabled 1 = enabled
R9 (09h) Power Mgmt 2	1			
Note: MIXOUTL_ENA and MIXOUTR_ENA can be accessed through two separate control registers. Reading from or writing to either register location has the same effect.				

Table 38 Selecting Signals into the Output Mixers

The gain for microphone pre-amp and auxiliary input (IN3L/IN3R) signals can be independently adjusted for each output mixer. This does not affect the volume of the same signals going into the separate record mixer. The level of the DAC output signals can be adjusted using the DAC's digital volume control function (see Table 32).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R96 (60h) Output Left Mixer Volume	3:1	INL_MIXOUTL_VOL [2:0]	000	Left input PGA volume control to left output mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer
	7:5	INR_MIXOUTL_VOL [2:0]	000	Right input PGA volume control to left output mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer
	11:9	IN3L_MIXOUTL_VOL [2:0]	000	IN3L amplifier volume control to left output mixer 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer
R97 (61h) Output Right Mixer Volume	3:1	INL_MIXOUTR_VOL [2:0]	000	Left input PGA volume control to right output mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer
	7:5	INR_MIXOUTR_VOL [2:0]	000	Right input PGA volume control to right output mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer
	15:13	IN3R_MIXOUTR_VOL [2:0]	000	IN3R amplifier volume control to right output mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer

Table 39 Controlling the Gain of Signals Going into the Output Mixers

13.9 ANALOGUE OUTPUTS

13.9.1 OUT1L AND OUT1R

The headphone outputs, OUT1L and OUT1R can drive a 16Ω or 32Ω headphone load, either through DC blocking capacitors, or DC coupled without any capacitor. Each output has an analogue volume control PGA with a gain range of -57dB to +6dB as shown in Figure 44.

Common mode noise rejection is also possible on the OUT1L and OUT1R outputs, using HPCOM as the return path. The HPCOM feature must be enabled via the OUT1_FB register field and the HPCOM connection must be AC coupled to the headphone output. A 4.7uF coupling capacitor is required between the noisy ground connection the HPCOM pin.

The control register fields for the OUT1L and OUT1R outputs are described in Table 40. The available output configurations are shown in Section 13.9.3.

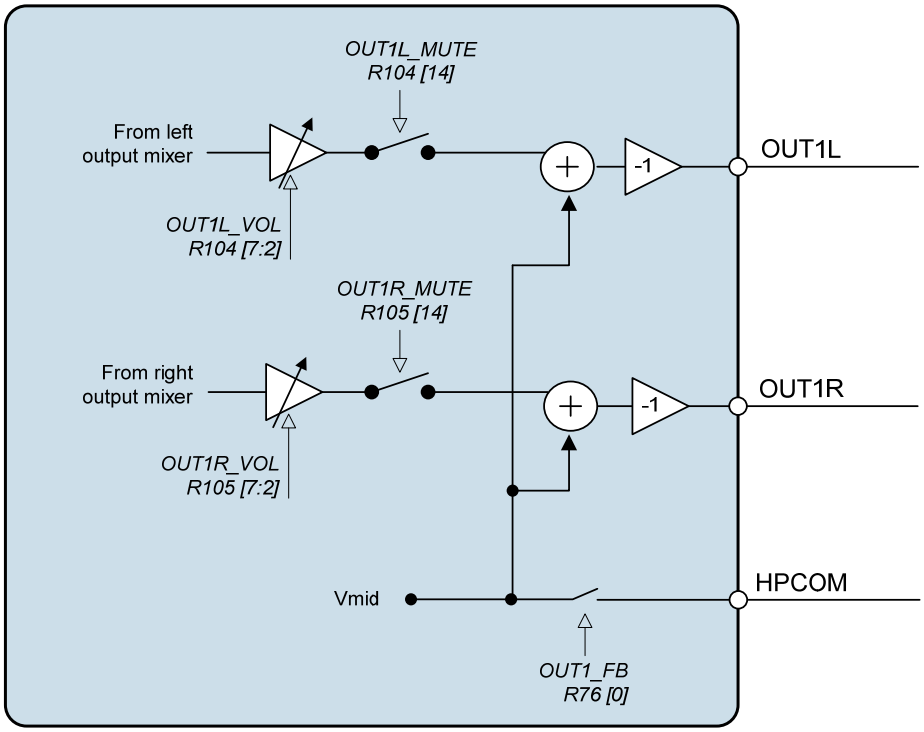


Figure 44 Headphone Outputs OUT1L and OUT1R

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R104 (68h) OUT1L Volume	14	OUT1L_MUTE	0	OUT1L mute: 0 = normal operation 1 = mute
	13	OUT1L_ZC	0	OUT1L volume zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	8	OUT1_VU	0	OUT1L and OUT1R volumes do not update until a 1 is written to either OUT1_VU.
	7:2	OUT1L_VOL [5:0]	11_1001	OUT1L volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB
R105 (69h) OUT1R Volume	14	OUT1R_MUTE	0	OUT1R mute: 0 = normal operation 1 = mute
	13	OUT1R_ZC	0	OUT1R volume zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	8	OUT1_VU	0	OUT1L and OUT1R volumes do not update until a 1 is written to either OUT1_VU.
	7:2	OUT1R_VOL [5:0]	11_1001	OUT1R volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB
R76 (4Ch) Output Control	0	OUT1_FB	0	Enable Headphone common mode ground feedback for OUT1 0 = disabled (HPCOM unused) 1 = enabled (common mode feedback through HPCOM)

Table 40 Controlling OUT1L and OUT1R

13.9.2 OUT2L AND OUT2R

OUT2L and OUT2R are designed as a stereo pair and can drive a headphone, a line load or a loudspeaker amplifier. Each output has an analogue volume control PGA with a gain range of -57dB to +6dB as shown in Figure 45.

Common mode noise rejection is also possible on the OUT2L and OUT2R outputs, using HPCOM as the return path. The HPCOM feature must be enabled via the OUT2_FB register field and the HPCOM connection must be AC coupled to the headphone output. A 4.7uF coupling capacitor is required between the noisy ground connection the HPCOM pin.

The signal path from the right output mixer to OUT2R can be inverted, using the OUT2R_INV and OUT2R_INV_MUTE register bits. Table 41 describes the required settings of these register bits for inverted and non-inverted configurations. Note that the OUT2R_MUTE mutes the OUT2R signal path in both cases.

OUT2R_INV	OUT2R_INV_MUTE	DESCRIPTION
0	1	Non-inverting path from MIXOUTR to OUT2R
1	0	Inverting path from MIXOUTR to OUT2R

Table 41 OUT2R Signal Path Polarity

The control register fields for the OUT2L and OUT2R outputs are described in Table 42. The available output configurations are shown in Section 13.9.3.

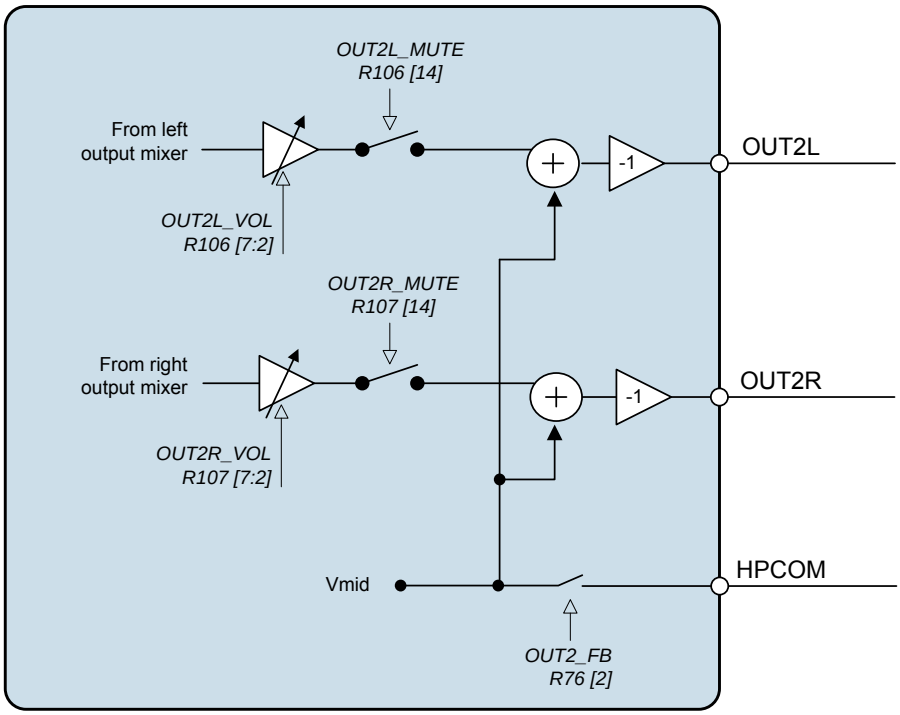


Figure 45 Headphone Outputs OUT2L and OUT2R

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R106 (6Ah) for OUT2L Volume	14	OUT2L_MUTE	0	OUT2L mute: 0 = normal operation 1 = mute
	13	OUT2L_ZC	0	OUT2L volume zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	8	OUT2_VU	0	OUT2L and OUT2R volumes do not update until a 1 is written to either OUT2_VU register bits.
	7:2	OUT2L_VOL [5:0]	11_1001	OUT2L volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB
R107 (6Bh) for OUT2R	14	OUT2R_MUTE	0	OUT2R mute: 0 = normal operation 1 = mute
	13	OUT2R_ZC	0	OUT2R volume zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	10	OUT2R_INV	0	Enable OUT2R inverting amplifier 0 = disabled 1 = enabled This register must be set to 0 when using the non-inverting MIXOUT2R to OUT2R path. This register must be set to 1 when using the inverting MIXOUT2R to OUT2R path.
	9	OUT2R_INV_MUTE	1	Mute output of PGA to inverting amplifier. 0 = PGA output goes to inverting amplifier 1 = PGA output goes to output driver This register must be set to 0 when using the inverting MIXOUT2R to OUT2R path. This register must be set to 1 when using the non-inverting MIXOUT2R to OUT2R path.
	8	OUT2_VU	0	OUT2L and OUT2R volumes do not update until a 1 is written to either OUT2_VU register bits.
	7:2	OUT2R_VOL [5:0]	11_1001	OUT2R volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB
R76 (4Ch) Output Control	2	OUT2_FB	0	Enable Headphone common mode ground feedback for OUT2 0 = disabled (HPCOM unused) 1 = enabled (common mode feedback through HPCOM)

Table 42 Controlling OUT2L and OUT2R

A beep signal on the IN3R pin (see Table 43) can be mixed into OUT2R independently of the right output mixer (i.e. without mixing the same beep signal into OUT1R).

Note that this feature is only possible when the inverting path configuration (MIXOUTR to OUT2R) is selected. See Table 41 for the required register settings.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R111 (6Fh) Beep Volume	15	IN3R_TO_OUT2R	0	Beep mixer enable 0 = disabled 1 = enabled
	7:5	IN3R_OUT2R_VOL [2:0]	000	Beep mixer volume: 000 = -15dB … in +3dB steps 111 = +6dB

Table 43 Controlling the "Beep" Path (IN3R to OUT2R)

13.9.3 HEADPHONE OUTPUTS EXTERNAL CONNECTIONS

Some example headphone output configurations are shown below.

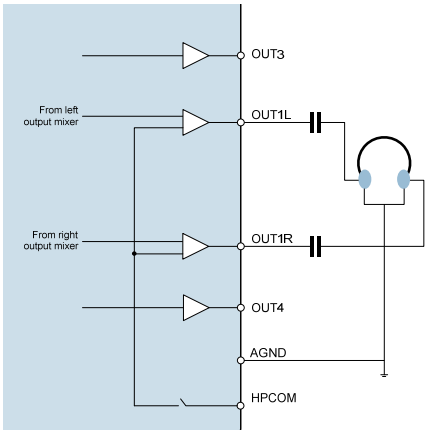


Figure 46 AC-Coupled Headphone Drive

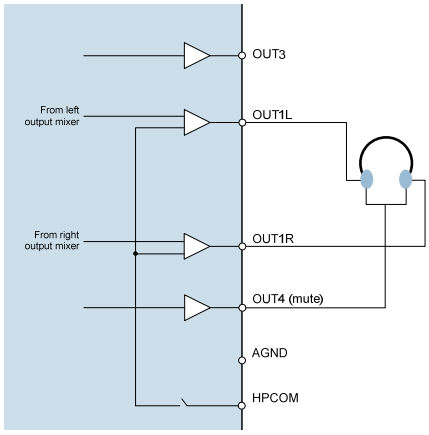


Figure 47 DC-Coupled (Capless) Mode Headphone Drive

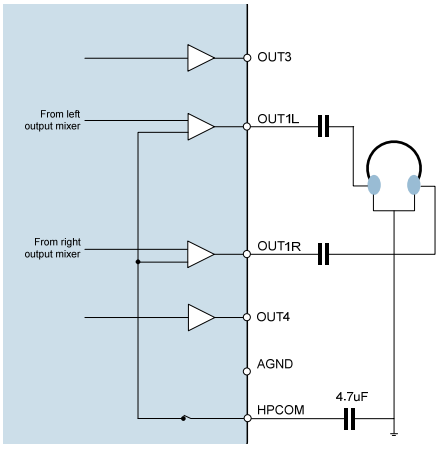


Figure 48 AC-Coupled Headphone Drive with Common Mode Noise Rejection

Notes:

1. The above figures illustrate the headphone connections to outputs OUT1L and OUT1R. The equivalent configurations apply equally to OUT2L and OUT2R.
2. The DC-coupled configuration illustrated in Figure 47 shows OUT4 (muted) being used as the Ground Return connection. The same capability may alternatively be provided using OUT3.
3. Twin headphone output (OUT1L, OUT1R, OUT2L and OUT2R) is possible, using a shared Ground Return connection via any of OUT3, OUT4, HPCOM or AGND.
4. Capless operation is not possible when using the HPCOM feature.

When DC blocking capacitors are used their capacitance and the load resistance together determine the lower cut-off frequency, f_c. Increasing the capacitance lowers f_c, improving the bass response. Smaller capacitance values will diminish the bass response. For a 16Ω load and a capacitance of 220μF, the following derivation of cut-off frequency applies:

$f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 16\Omega \times 220\mu F) = 45$ Hz

In the DC coupled configuration, the headphone "ground" is connected to VMID. The OUT3 or OUT4 pins can be configured as DC output drivers by de-selecting all inputs to the OUT3 or OUT4 mixers. The DC voltage on VMID in this configuration is equal to the DC offset on the OUT1L and OUT2L pins therefore no DC blocking capacitors are required. This saves space and material cost in portable applications.

It is recommended to only use the DC coupled configuration to drive headphones, and not to use this configuration to drive the line input of another device.

13.9.4 OUT3 AND OUT4

The additional analogue outputs OUT3 and OUT4 have independent mixers and can be used in a number of different ways:

- OUT3 and OUT4 as a stereo pair (OUT3 = left, OUT4 = right) to drive a headphone or line load
- OUT3 or OUT4 as pseudo-ground outputs for headphones connected directly (without DC blocking capacitors) to OUT1L/OUT1R or OUT2L/OUT2R
- OUT4 as a mono mix of left and right signals

The OUT3 and OUT4 output stages are powered from HPVDD and HPGND.

If OUT4 is providing a mono mix, it is recommended to reduce the level of OUT4 by 6dB to avoid clipping in the event of 2 full-scale signals being combined. This is implemented via the OUT4_ATT register field. When OUT4_ATT is asserted, then OUT4 = (L+R) / 2.

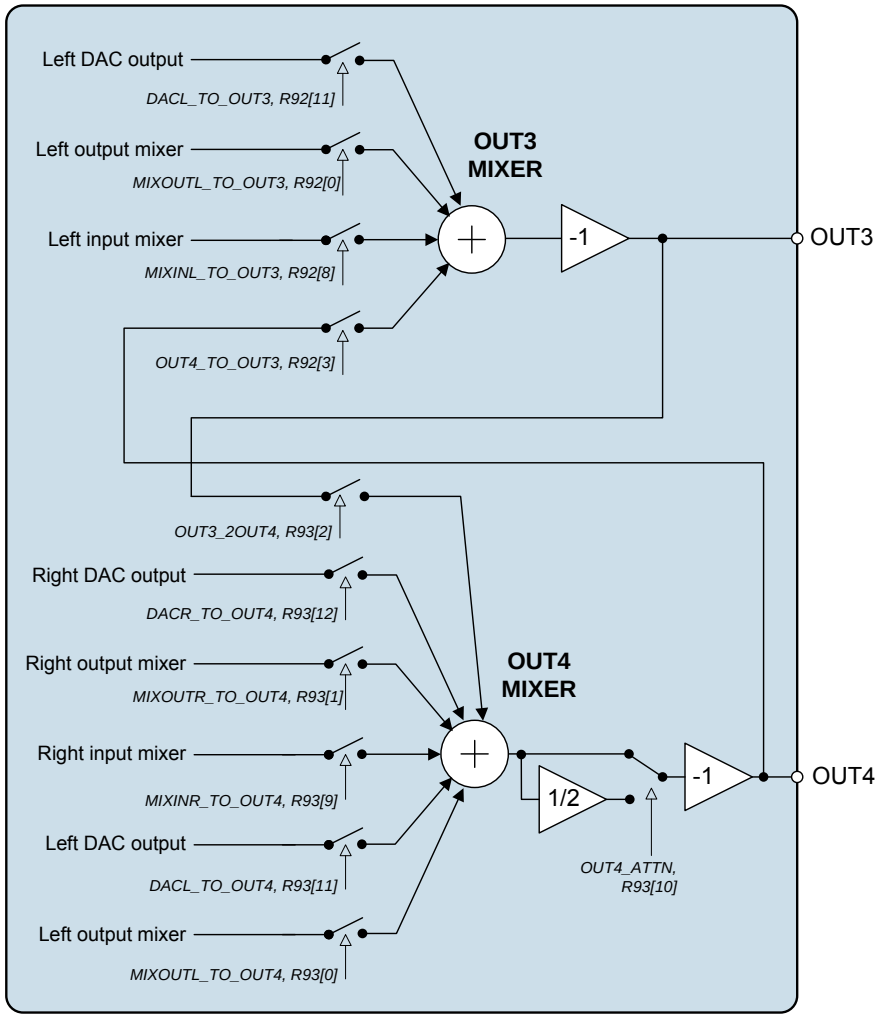


Figure 49 OUT 3 and OUT4 Mixers

OUT3 can provide a buffered midrail headphone pseudo-ground, or a left line output. It can also be a common mode input for OUT2L/OUT2R. OUT4 can provide a buffered midrail headphone pseudo-ground, a right line output, or a mono mix output. It can also be mixed into the input boost mixer for recording.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R92 (5Ch) OUT3 Mixer	11	DACL_TO_OUT3	0	Left DAC output to OUT3 0 = disabled 1 = enabled
	8	MIXINL_TO_OUT3	0	Left input mixer to OUT3 0 = disabled 1 = enabled
	3	OUT4_TO_OUT3	0	OUT4 mixer to OUT3 0 = disabled 1 = enabled
	0	MIXOUTL_TO_OUT 3	0	Left output mixer to OUT3 0 = disabled 1 = enabled
R92 (5Ch) OUT3 Mixer	15	OUT3_ENA	0	OUT3 enable 0 = disabled 1 = enabled
R9 (09h) Power Mgmt 2	4			
Note: OUT3_ENA can be accessed through R92 or R9. Reading from or writing to either register location has the same effect.				

Table 44 Controlling the OUT3 Mixer

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R93 (5Dh) OUT4 Mixer	12	DACR_TO_OUT4	0	Right DAC output to OUT4 0 = disabled 1 = enabled
	11	DACL_TO_OUT4	0	Left DAC output to OUT4 0 = Disabled 1 = Enabled
	10	OUT4_ATT	0	Reduce OUT4 output by 6dB 0 = Output at normal level 1 = Output reduced by 6dB
	9	MIXINR_TO_OUT4	0	Right input mixer to OUT4 0 = disabled 1 = enabled
	2	OUT3_TO_OUT4	0	OUT3 mixer to OUT4 This function is not supported
	1	MIXOUTR_TO OUT4	0	Right output mixer to OUT4 0 = Disabled 1 = Enabled
	0	MIXOUTL_TO_OUT4	0	Left output mixer to OUT4 0 = disabled 1 = enabled
R93 (5Dh) OUT4 Mixer	15	OUT4_ENA	0	OUT4 enable 0 = disabled 1 = enabled
R9 (09h) Power Mgmt 2	5			
Note: OUT4_ENA can be accessed through R93 or R9. Reading from or writing to either register location has the same effect.				

Table 45 Controlling the OUT4 Mixer

13.10 DIGITAL AUDIO INTERFACE

The audio interface enables the WM8351 to exchange audio data with other system components. It is separate from the control interface and has four dedicated pins:

- ADCDAT: Output pin for data coming from the audio ADC
- DACDAT: Input pin for audio data going to the audio DAC
- LRCLK: Data Left/Right alignment clock (also known as "word clock")
- BCLK: Bit clock, for synchronisation

The LRCLK and BCLK pins are outputs when the WM8351 operates as a master device and are inputs when it is a slave device.

In order to allow the ADC and DAC to run at different sampling rates, separate ADCLRCLK and ADCBCLK signals are both available through GPIO pins: GPIO5 (ADCLRCLK) and GPIO6 or GPIO8 (ADCBCLK). This feature also allows mixed Master/Slave operation between the ADC and DAC.

13.10.1 AUDIO DATA FORMATS

The audio interface supports six different audio data formats:

- Left justified
- Right justified
- I^2S
- DSP mode A
- DSP mode B
- TDM Mode

In all of these formats, the MSB (most significant bit) of each data sample is transferred first and the LSB (least significant bit) last.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R112 (70h) Audio Interface	15	AIF_BCLK_INV	0	BCLK polarity 0 = normal 1 = inverted
	13	AIF_TRI	0	Sets Output enables for LRCLK and BCLK and ADCDAT to inactive state 0 = normal 1 = forces pins to Hi-Z
	12	AIF_LRCLK_INV	0	LRCLK clock polarity 0 = normal 1 = inverted DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRCLK rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRCLK rising edge (mode B)
	11:10	AIF_WL [1:0]	10 (24 bits)	Data word length 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits Note: When using the Right-Justified data format (AIF_FMT=00), the maximum word length is 24 bits.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8:9	AIF_FMT [1:0]	10 (I^2S)	Data format 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP / PCM mode Note - see Section 13.11 for the selection of 8-bit mode.
R114 (72h) Audio Interface ADC Control	7	AIFADC_PD	0	Enables a pull down on ADC data pin 0 = disabled 1 = enabled
	6	AIFADCL_SRC	0	Selects Left channel ADC output. 0 = ADC Left channel 1 = ADC Right channel
	5	AIFADCR_SRC	1	Selects Right channel ADC output. 0 = ADC Left channel 1 = ADC Right channel
	4	AIFADC_TDM_ CHAN	0	ADCDAT TDM Channel Select 0 = ADCDAT outputs data on slot 0 1 = ADCDAT output data on slot 1
	3	AIFADC_TDM	0	ADC TDM Enable 0 = Normal ADCDAT operation 1 = TDM enabled on ADCDAT
R115 (73h) Audio Interface DAC Control	7	AIFDAC_PD	0	Enables a pull down on DAC data pin 0 = disabled 1 = enabled
	6	DACL_SRC	0	Selects Left channel DAC input. 0 = DAC Left channel 1 = DAC Right channel
	5	DACR_SRC	1	Selects Right channel DAC input. 0 = DAC Left channel 1 = DAC Right channel
	4	AIFDAC_TDM_ CHAN	0	DACDAT TDM Channel Select 0 = DACDAT outputs data on slot 0 1 = DACDAT output data on slot 1
	3	AIFDAC_TDM	0	DAC TDM Enable 0 = Normal DACDAT operation 1 = TDM enabled on DACDAT

Table 46 Selecting the Audio Data Format

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

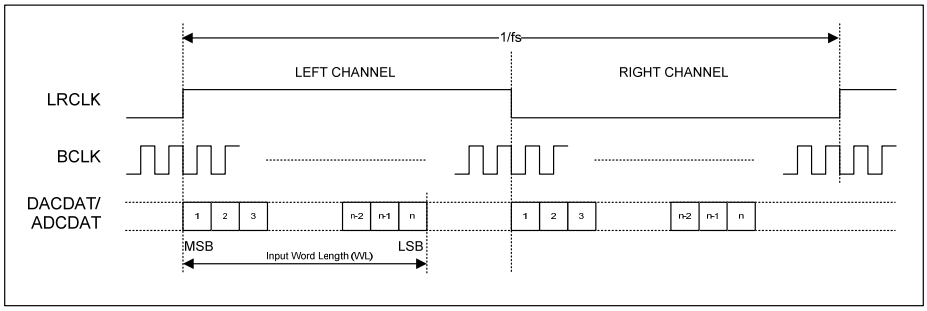


Figure 50 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

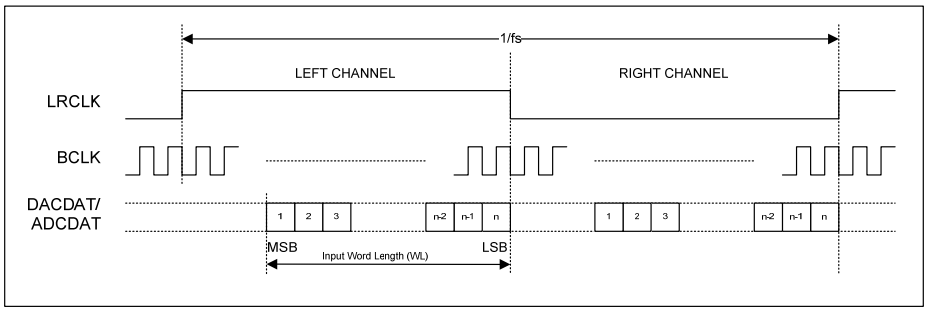


Figure 51 Right Justified Audio Interface (assuming n-bit word length)

In I2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

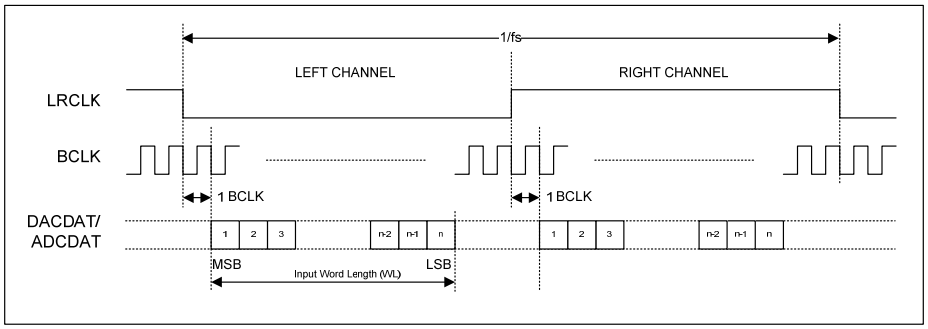


Figure 52 I2S Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by AIF_LRCLK_INV) following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

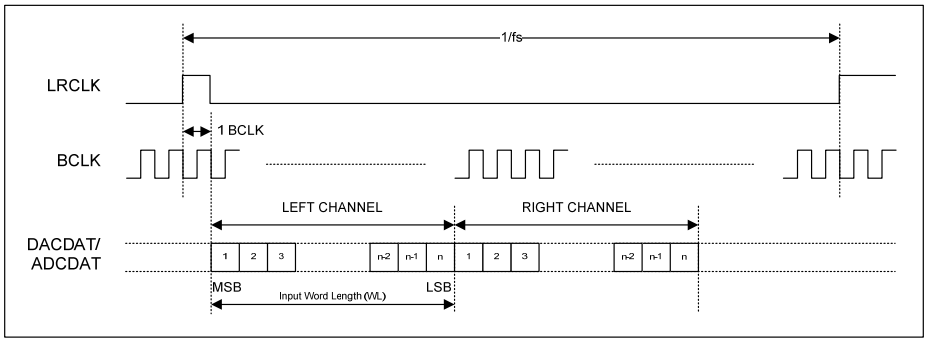


Figure 53 DSP/PCM Mode Audio Interface (mode A, AIF_LRCLK_INV=0)

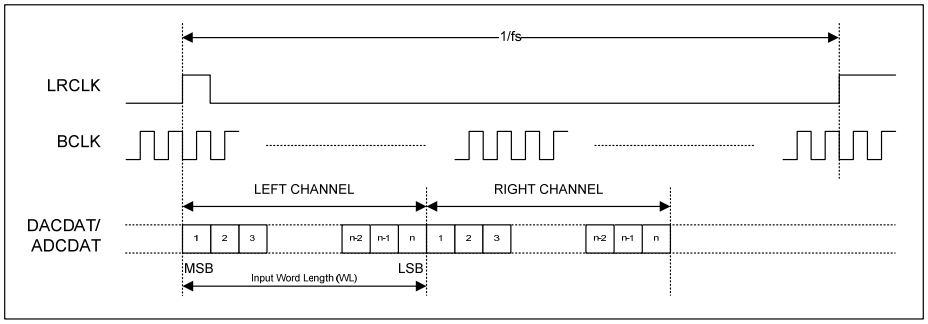


Figure 54 DSP/PCM Mode Audio Interface (mode B, AIF_LRCLK_INV=1)

13.10.2 AUDIO INTERFACE TDM MODE

The digital audio interface on WM8351 has the facility of tri-stating the ADCDAT pin to allow multiple data sources to operate on the same bus. Time division multiplexing (TDM) is also supported, allowing audio output data to be transferred simultaneously from two different sources.

TDM mode is enabled for the ADC and DAC by register bits AIFADC_TDM and AIFDAC_TDM respectively. TDM slot selection for the WM8351 is set for the ADC and DAC by register bits AIFADC_TDM_CHAN and AIFDAC_TDM_CHAN respectively, as defined in Table 46. When not actively transmitting data, the ADCDAT pin will be tristated in TDM mode, to allow other devices to transmit data.

13.10.3 TDM DATA FORMATS

All selectable data formats support TDM. The allocation of time slots is controlled by register bits AIFADC_TDM_CHAN and AIFDAC_TDM_CHAN. Two possible slots (SLOT0 and SLOT1) are available for the ADC and for the DAC.

Timing signals for the various interface formats in TDM mode are shown below for the ADC. Similar slot allocation will exist for the DAC.

Left Justified Mode: SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 to the start of SLOT1 is determined by the selected word length of the interface of the WM8351.

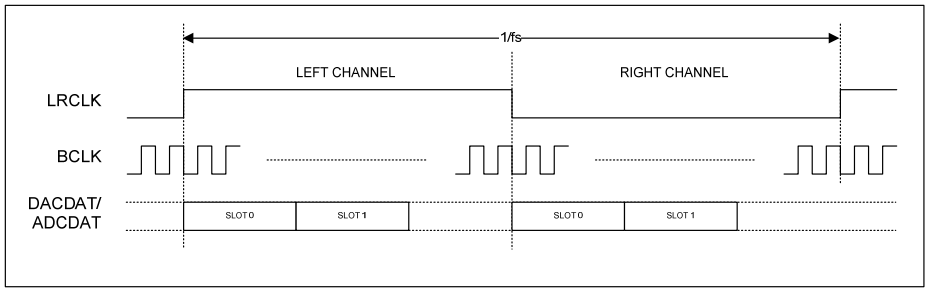


Figure 55 Left Justified Mode with TDM

Right Justified Mode: SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the end of SLOT1 to the end of SLOT0 is determined by the selected word length of the interface of the WM8351.

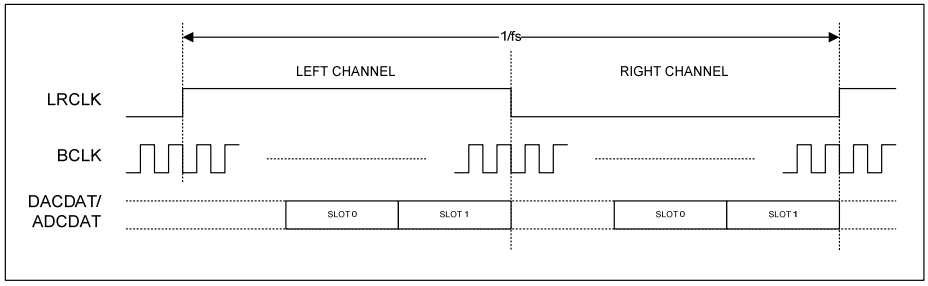


Figure 56 Right Justified Mode with TDM

I2S Mode: SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 to the start of SLOT1 is determined by the selected word length of the interface of the WM8351.

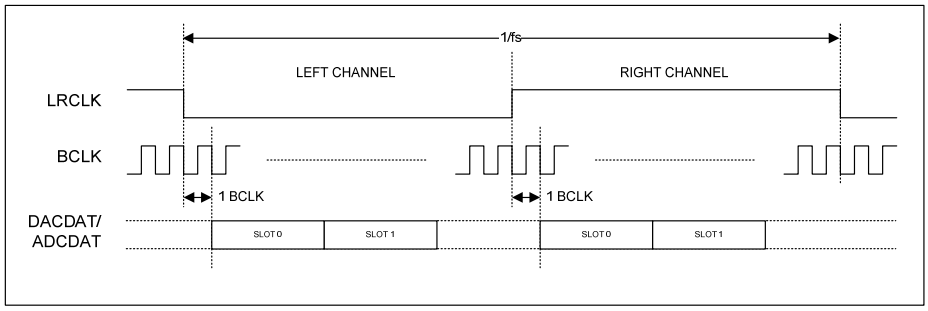


Figure 57 I2S Mode with TDM

DSP/PCM Mode A, Master Mode: SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 (left) to the start of SLOT1 (left) is determined by the selected word length of the interface of the WM8351.

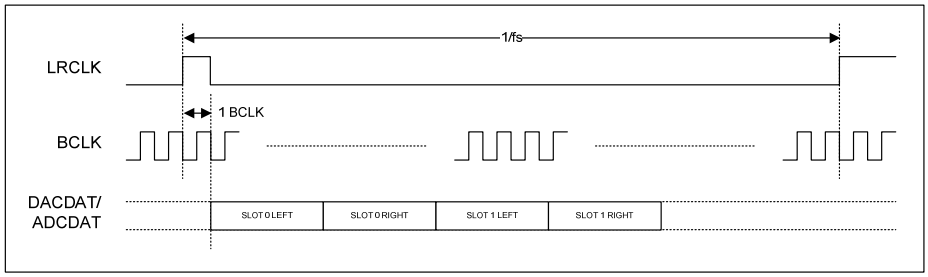


Figure 58 DSP/PCM Mode A, Master Mode with TDM

DSP/PCM Mode B, Master Mode: SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 (left) to the start of SLOT1 (left) is determined by the selected word length of the interface of the WM8351.

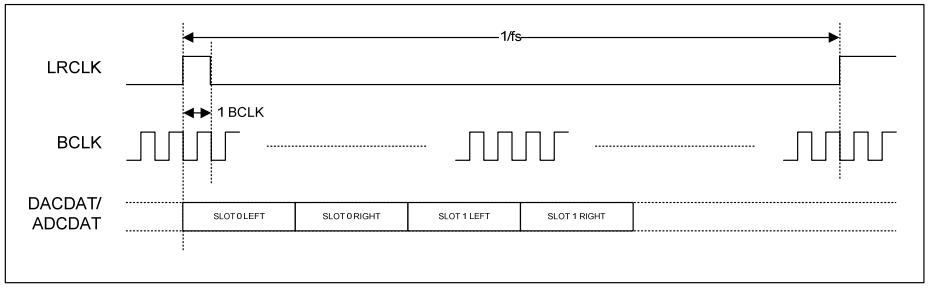


Figure 59 DSP/PCM Mode B, Master Mode, with TDM

DSP/PCM Mode A, Slave Mode: SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 (left) to the start of SLOT1 (left) is determined by the selected word length of the interface of the WM8351.

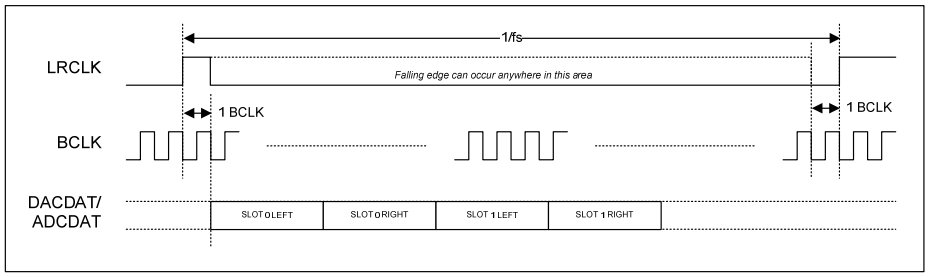


Figure 60 DSP/PCM Mode A, Slave Mode with TDM

DSP/PCM Mode B, Slave Mode: SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 (left) to the start of SLOT1 (left) is determined by the selected word length of the interface of the WM8351.

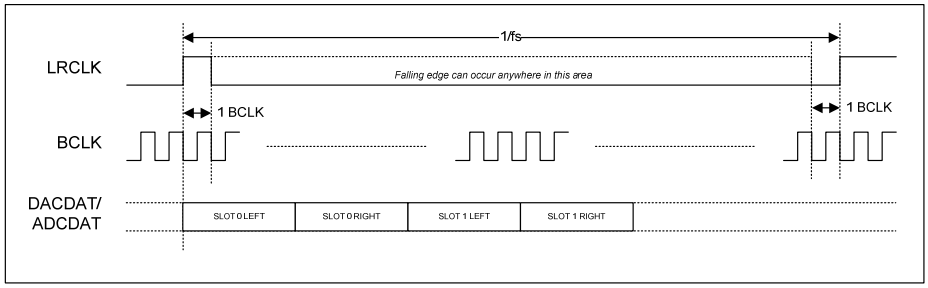


Figure 61 DSP/PCM Mode B, Slave Mode, with TDM

13.10.4 LOOPBACK

When the loopback feature is enabled, the audio ADC's digital output data is looped back to the audio DAC and converted back into an analogue signal. This is often useful for test and evaluation purposes.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R113 (71h) ADC Control	0	LOOPBACK	0	Digital Loopback Function 0 = No loopback. 1 = Loopback enabled, ADC data output is fed directly into DAC data input.

Table 47 Enabling loopback

13.11 COMPANDING

The WM8351 supports A-law and μ-law companding on both transmit (ADC) and receive (DAC) sides. Companding can be enabled on the DAC or ADC audio interfaces by writing the appropriate value to the DAC_COMP or ADC_COMP register bits respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R113 (71h) Companding Control	4	ADC_COMPMODE	0	ADC Companding mode select: 0 = μ-law 1 = A-law (Note: Setting ADC_COMPMODE=1 selects 8-bit mode when DAC_COMP=0 and ADC_COMP=0)
	5	ADC_COMP	0	ADC Companding enable 0 = off 1 = on
	6	DAC_COMPMODE	0	DAC Companding mode select: 0 = μ-law 1 = A-law (Note: Setting DAC_COMPMODE=1 selects 8-bit mode when DAC_COMP=0 and ADC_COMP=0)
	7	DAC_COMP	0	DAC Companding enable 0 = off 1 = on

Table 49 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

μ-law (where μ=255 for the U.S. and Japan):

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu)$ $\quad -1 \le x \le 1$

law (where A=87.6 for Europe):

$F(x) = A|x| / (1 + \ln A)$ } for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ } for $1/A \le x \le 1$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ-law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSBs of data.

Companding converts 13 bits (μ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. This provides greater precision for low amplitude signals than for high amplitude signals, resulting in a greater usable dynamic range than 8 bit linear quantization. The companded signal is an 8-bit word comprising sign (1 bit), exponent (3 bits) and mantissa (4-bits).

8-bit mode is selected whenever DAC_COMP=1 or ADC_COMP=1. The use of 8-bit data allows samples to be passed using as few as 8 BCLK cycles per LRCLK frame. When using DSP mode B, 8-bit data words may be transferred consecutively every 8 BCLK cycles.

8-bit mode (without Companding) may be enabled by setting ADC_COMPMODE=1 when ADC_COMP=0.

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 50 8-bit Companded Word Composition

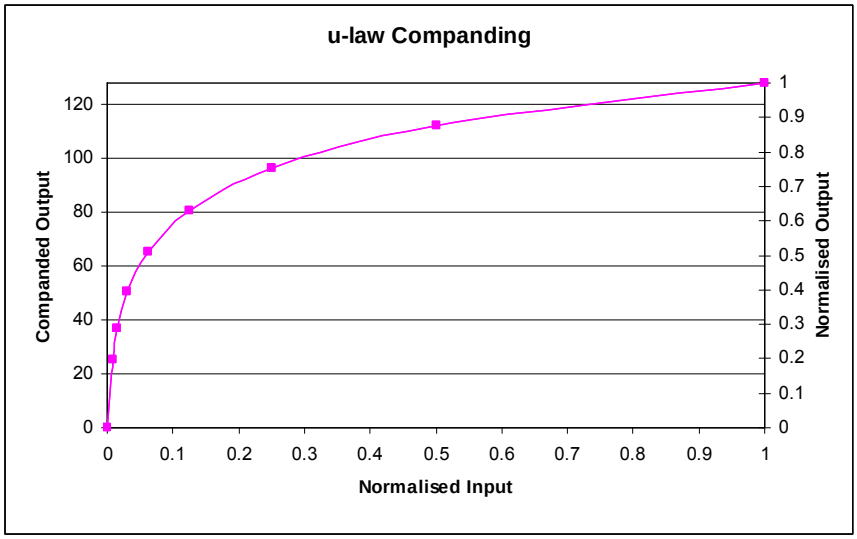


Figure 39 μ-Law Companding

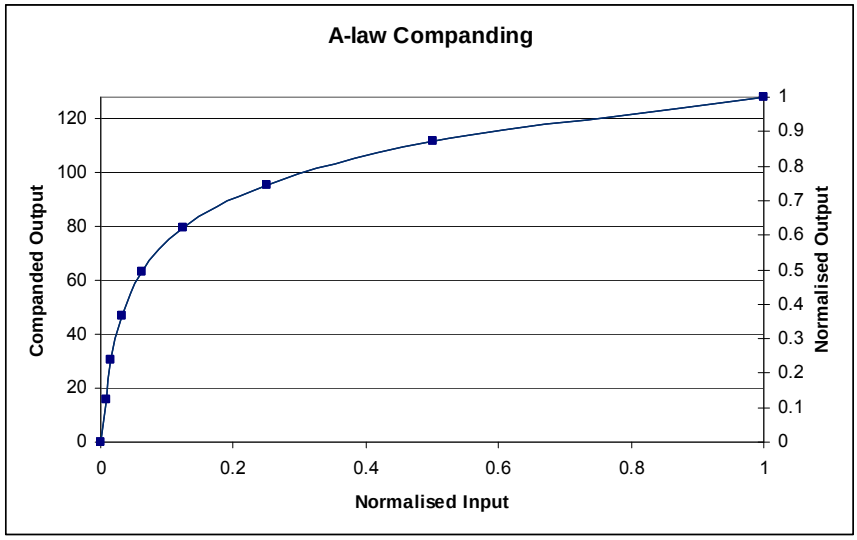


Figure 40 A-Law Companding

13.12 ADDITIONAL CODEC FUNCTIONS

13.12.1 HEADPHONE JACK DETECT

The IN2L and IN2R pins can be selected as headphone jack detect inputs, to enable automatic control of the analogue outputs when a headphone is plugged into a jack socket.

Jack Detection on the IN2L or IN2R pins is enabled by register bits JDL_ENA or JDR_ENA respectively. When Jack Detection is enabled, the associated second level interrupts CODEC_JCK_DET_L_EINT and CODEC_JCK_DET_R_EINT indicate the status of the jack socket. See Section 13.12.7 for further details.

The Headphone Jack Detect function requires the internal slow clock to be enabled - see Section 12.3.6.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R77 (4Dh) Jack Detect	15	JDL_ENA	0	Jack Detect Enable for inputs connected to IN2L 0 = disabled 1 = enabled
	14	JDR_ENA	0	Jack Detect Enable for input connected to IN2R 0 = disabled 1 = enabled

Table 48 Headphone Jack Detect

13.12.2 MICROPHONE DETECTION

The WM8351 can detect when a microphone has been plugged in, and/or when the microphone is short-circuited. It detects these events by comparing the current drawn from the MICBIAS pin against two thresholds. The thresholds for plug-in detection and short-circuit detection are programmable.

A MICBIAS current above the MCDTHR threshold level is used to indicate that a microphone is plugged in, and is associated with the CODEC_MICD_EINT interrupt. If the bias current exceeds the MCDSCTHR limit, this indicates a microphone short-circuit condition, and the WM8351 raises a CODEC_MICSCD_EINT interrupt. See Section 13.12.7 for further details. Note that the MICBIAS current thresholds are subject to a wide tolerance - up to +/-50% of the specified value.

Microphone detection requires the internal slow clock to be enabled - see Section 12.3.6.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Power Mgmt 1	8	MIC_DET_ENA	0	Enable MIC detect: 0 = disabled 1 = enabled
R74 (4Ah) Mic Bias Control	7	MIC_DET_ENA	0	
	4:2	MCDTHR [2:0]	000	Threshold for bias current detection 000 = 160µA 001 = 330µA 010 = 500µA 011 = 680µA 100 = 850µA 101 = 1000µA 110 = 1200µA 111 = 1400µA These threshold currents scale proportionally with AVDD. The values given are for AVDD=3.3V.
	1:0	MCDSCTHR [1:0]	00	Threshold for microphone short-circuit detection 00 = 400µA 01 = 900µA 10 = 1350µA 11 = 1800µA These threshold currents scale proportionally with AVDD. The values given are for AVDD=3.3V.
Note: MIC_DET_ENA can be accessed through R8 or through R74. Reading from or writing to either register location has the same effect.				

Table 49 Controlling Microphone Bias Current Detection

13.12.3 MID-RAIL REFERENCE (VMID)

VMID provides a potential mid-way between AVDD and GND, used in many parts of the audio CODEC. It is generated from AVDD using on-chip potential dividers. Different resistor values can be selected for this purpose. A medium resistance should be used when the CODEC is active. A high resistance option provides a more power-efficient way to maintain the VMID voltage when the CODEC is in "Standby" (i.e. inactive but ready to start immediately, without needing to wait for the VMID capacitor to be charged). For startup and shutdown the VMID generator provides soft VMID ramping to reduce pops and clicks. The speed of this ramp is selectable using the anti-pop controls and can be tuned to the application.

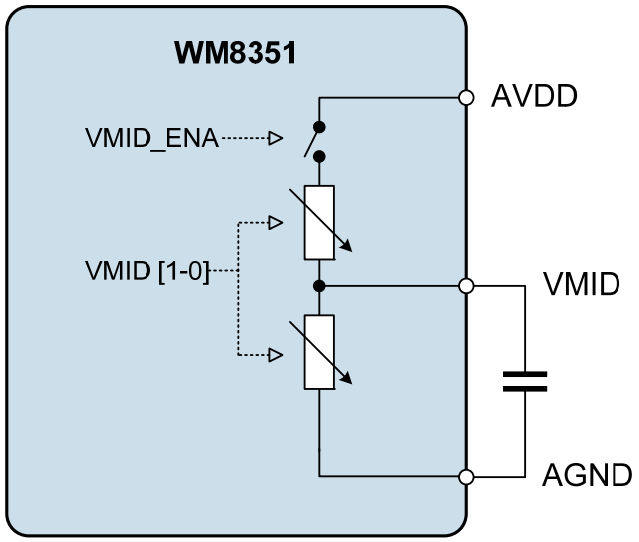


Figure 62 Generating the Mid-rail Reference

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Power Management 1	2	VMID_ENA	0	Enables VMID resistor string 0 = disabled, 1 = enabled
	1:0	VMID [1:0]	00 (off)	Resistor selection for VMID potential divider 00 = off 01 = VMID comes from 300kΩ R-string 10 = VMID comes from 50kΩ R-string 11 = VMID comes from 5kΩ R-string

Table 50 Controlling the Mid-rail Reference

13.12.4 ANTI-POP CONTROL

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R78 (4Eh) Anti pop control	9:8	ANTI_POP [1:0]	00	Reduces pop when VMID is enabled by setting the speed of the S-ramp for VMID. 00 = no S-ramp (will pop) 01 = fastest S-curve 10 = medium S-curve 11 = slowest S-curve
	7:6	DIS_OP_LN4 [1:0]	00	Sets the Discharge rate for OUT4 00 = discharge path OFF 01 = fastest discharge 10 = medium discharge 11 = slowest discharge
	5:4	DIS_OP_LN3 [1:0]	00	Sets the Discharge rate for OUT3 00 = discharge path OFF 01 = fastest discharge 10 = medium discharge 11 = slowest discharge
	3:2	DIS_OP_OUT2 [1:0]	00	Sets the discharge rate for OUT2L and OUT2R 00 = discharge path OFF 01 = fastest discharge 10 = medium discharge 11 = slowest discharge
	1:0	DIS_OP_OUT1 [1:0]	00	Sets the discharge rate for OUT1L and OUT1R 00 = discharge path OFF 01 = fastest discharge 10 = medium discharge 11 = slowest discharge

Table 51 Control Registers for Anti-pop

13.12.5 UNUSED ANALOGUE INPUTS/OUTPUTS

Whenever an analogue input/output is disabled, it remains connected to AVDD/2 through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between the voltage buffer and the output pins can be controlled using the VROI control bits. The default impedance is low, so that any capacitors on the outputs can charge up quickly at start-up. If high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 30kΩ.

There are individual VROI bits for each output or output pair. This allows matching of the rise times of the outputs if they are driving different capacitors. Using the small resistance with a capacitor for headphone outputs (typically 220uF) and the larger resistance with a line load capacitance (10uF for example); will allow both sets of outputs to power up in around the same time, around 200ms.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Power Mgmt 1	13	VBUF_ENA	0	Forces ON the tie-off amplifiers 0 = Disabled 1 = Enabled
R76 (4Ch) Output Control	8	OUT1_VROI	0	VREF (AVDD/2) to OUT1L/OUT1R resistance 0 = approx 500Ω 1 = approx 30 kΩ
	9	OUT2_VROI	0	VREF (AVDD/2) to OUT2L/OUT2R resistance 0 = approx 500Ω 1 = approx 30 kΩ
	10	OUT3_VROI	0	VREF (AVDD/2) to OUT3 resistance 0 = approx 500Ω 1 = approx 30 kΩ
	11	OUT4_VROI	0	VREF (AVDD/2) to OUT4 resistance 0 = approx 500Ω 1 = approx 30 kΩ

Table 52 Disabled Outputs to VREF Resistance

A dedicated buffer is available for tying off unused analogue I/O pins as shown below. This buffer can be enabled using the VBUF_ENA register bit.

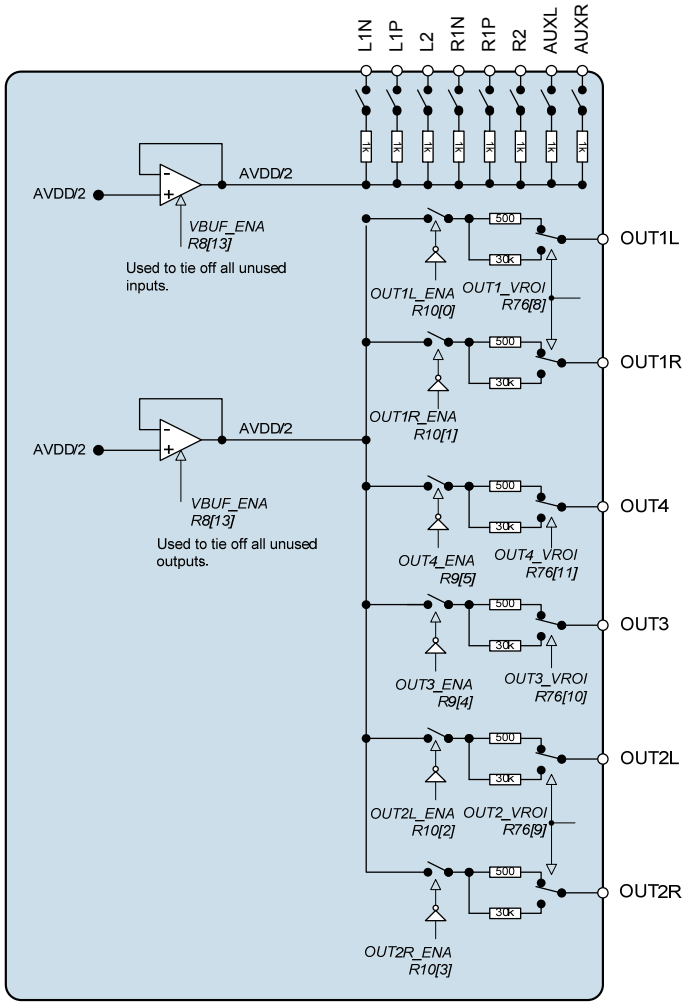


Figure 63 Unused Input/Output Pin Tie-off Buffers

OUT1R/L_ENA/ OUT2R/L_ENA OUT3/4_ENA	VROI	OUTPUT CONFIGURATION
0	0	500Ω tie-off to AVDD/2
0	1	30kΩ tie-off to AVDD/2
1	X	Output enabled (DC level = AVDD/2)
1	X	Output enabled (DC level = 1.5 x AVDD/2)

Table 53 Unused Output Pin Tie-off Options

13.12.6 ZERO CROSS TIMEOUT

A zero-cross timeout function is also provided so that if zero cross is enabled on the input or output PGAs the gain will automatically update after a timeout period if a zero cross has not occurred.

The zero-cross timeout function requires the internal slow clock to be enabled - see Section 12.3.6.

13.12.7 INTERRUPTS AND FAULT PROTECTION

The CODEC has its own first-level interrupt, CODEC_INT (see Section 24). This comprises four second-level interrupts which indicate Jack detect and Microphone current conditions. These interrupts can be individually masked by setting the applicable mask bit(s) as described in Table 54.

ADDRESS	BIT	LABEL	DESCRIPTION
R31 (1Fh) Comparator Interrupt Status	11	CODEC_JCK_DET_L_EINT	Left channel Jack detection interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
	10	CODEC_JCK_DET_R_EINT	Right channel Jack detection interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
	9	CODEC_MICSCD_EINT	Mic short-circuit detect interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
	8	CODEC_MICD_EINT	Mic detect interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
R39 (27h) Comparator Interrupt Status Mask	11:8	"IM_" + name of respective bit in R31	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R39 enables or masks the corresponding bit in R31. The default value for these bits is 0 (unmasked).

Table 54 CODEC Interrupts

14 POWER MANAGEMENT SUBSYSTEM

14.1 GENERAL DESCRIPTION

The WM8351 provides five DC-DC Converters and four LDO Regulators which each deliver high efficiency across a wide range of line and load conditions. These power management components are designed to support application processors and associated peripherals. They are also suitable for providing power to the analogue and digital functions of the on-board CODEC and GPIO features. The output voltage of each of the converters and regulators is programmable in software through control registers.

The WM8351 has a number of operating states which are either selected by software control or are selected autonomously according to the available power supply conditions. A low power active 'Hibernate' state is provided, with programmable characteristics. The 'Backup' and 'Zero' states are selected autonomously when the available supply voltages do not permit full operation of the WM8351.

Four configuration modes are provided, selected by hardware control. Development Mode gives complete control over the configuration and start-up behaviour of the WM8351. Three different Custom Modes each have a defined set of configuration parameters, which determine the start-up timing and output voltage of each of the DC-DC Converters and LDO Regulators. The configuration of each of the GPIO pins is also contained with the configuration modes definitions.

14.2 POWER MANAGEMENT OPERATING STATES

The WM8351 autonomously controls the power-up and power-down sequencing for itself and for other connected devices. It also selects the most appropriate power source available at any given time (see Section 17). The stable states of the WM8351 are:

ACTIVE - All WM8351 functions can be used. The WM8351 enters the ACTIVE state after a valid start-up event (see Section 14.3.1), provided that no fault condition occurred during start-up.

HIBERNATE - This is an alternative active state with programmable characteristics, allowing an optional low power system condition. The internally generated supply voltages can be individually enabled or disabled as desired. The WM8351 enters the HIBERNATE state from ACTIVE by setting the HIBERNATE register bit or when commanded via a GPIO pin configured as a HIBERNATE alternate function.

OFF - All DC-DC converters and regulators LDO2, LDO3 and LDO4 are disabled. LDO1 may remain active (See Section 14.7.4). The VRTC regulator remains active and powers the always-on functions (such as crystal oscillator and RTC.) Register settings are restored to default settings. Trickle charging for the main battery is enabled by default. The WM8351 enters the OFF state from ACTIVE if a shutdown event occurs (see Section 14.3.3), or if the power source falls below the shutdown threshold (see Section 18). The WM8351 enters the OFF state from BACKUP if a power source greater than the UVLO threshold becomes available.

BACKUP - The crystal oscillator and RTC are enabled, powered from the backup power (VRTC) supply. All other functions are disabled. The WM8351 enters the BACKUP state from OFF if the power source falls below the UVLO threshold (see Section 18), and provided that backup power (VRTC) is available (i.e. LINE falls below the UVLO level but VRTC remains above the Power-On Reset threshold).

ZERO - All functions are disabled and all data in registers is lost. The WM8351 goes into this state when no power source is available and VRTC falls below the Power-On Reset threshold.

The Active state can only be entered via the **PRE-ACTIVE** state. In Development Mode, the Pre-Active state is the state in which the WM8351 start-up parameters may be defined, prior to the start-up sequence being triggered. The **ACTIVE** state is only entered on completion of the start-up sequence.

The WM8351 operating states and valid transitions are illustrated in Figure 64.

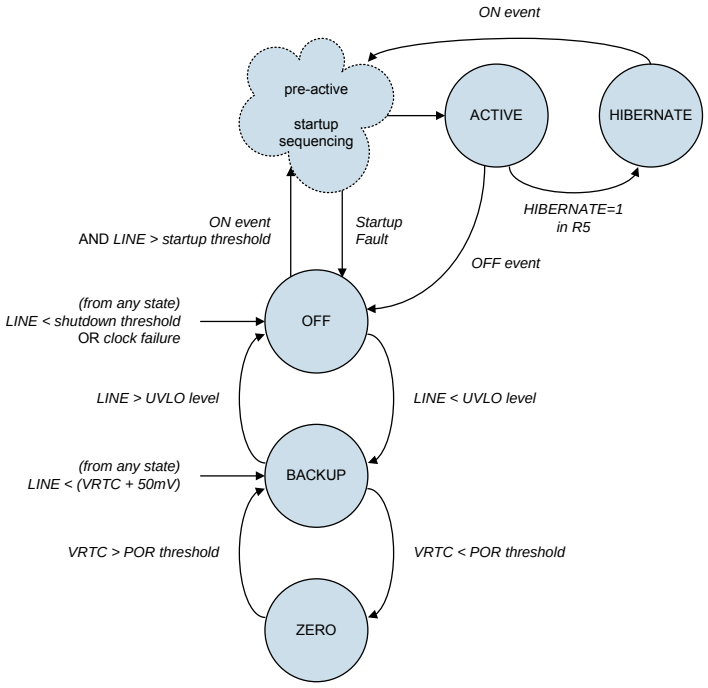


Figure 64 WM8351 Operating State Diagram

14.2.1 HIBERNATE STATE SELECTION

The WM8351 moves from the ACTIVE to the HIBERNATE state when the HIBERNATE register bit is set. It can also move to hibernate using the Hibernate Edge or the Hibernate Level function from the GPIOs.

It returns to the ACTIVE state when the Hibernate Level GPIO function is reset and the HIBERNATE bit is set to 0. It can also return to ACTIVE via the Hibernate Edge function or when a wake-up event (see Section 14.3.1) occurs.

If a fault condition occurs in the HIBERNATE state, the WM8351 moves to the OFF state.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) System Hibernate	15	HIBERNATE	0	Determines what state the chip should operate in. 0 = Active state 1 = Hibernate state The register bit defaults to 0 when a reset happens

Table 55 Invoking HIBERNATE State

The behaviour of the WM8351 in the HIBERNATE state is programmable in terms of supply voltage generation, interrupts and resets. Fast battery charging is disabled in the HIBERNATE state, but trickle charging is possible.

14.3 POWER SEQUENCING AND CONTROL

14.3.1 STARTUP

The WM8351 moves from OFF or HIBERNATE states to the ACTIVE state when a startup event occurs. Startup events include:

- A trigger signal on the ON pin lasting more than 40ms. The active polarity of this input is set by the register field ON_POL.
- A trigger signal on a GPIO pin configured as /WAKEUP lasting more than 40ms. The active polarity of this input is set by GPn_CFG for the applicable GPIO pin (see Section 20).
- A trigger signal on a GPIO pin configured as PWR_ON input lasting more than 40ms. The active polarity of this input is set by GPn_CFG for the applicable GPIO pin (see Section 20).
- Programmed ALARM from RTC module, if enabled (see Section 22).
- Wall adaptor plug-in (WALL_FB rises above 4.0V).
- USB plug-in (USB pin rises above 4.0V).

The start-up events are only valid provided also that the available supply voltage, sensed on the LINE pin, is greater than the start-up threshold set by PCCMP_ON_THR, as defined in Section 18.

Start-Up by Wall adaptor plug-in occurs when the Wall Adapter feedback pin detects a voltage greater than 4.0V. See Section 17.1 for a description of the WALL_FB pin function.

Start-Up by USB plug-in occurs when the USB voltage rises above the LINE voltage. If USB Suspend mode is invoked, then USB plug-in starts the WM8351 on battery power, if available. When USB Suspend Mode is not invoked, this start-up event will lead to starting the WM8351 on USB power, and USB 100mA trickle charging of the battery is enabled.

Note that applying a battery voltage is not a start-up event, i.e. connecting a battery pack does not start the WM8351. The WM8351 starts up on battery power if a startup event occurs and battery power is the only power source available, provided the battery voltage is above the startup threshold. (The start-up threshold is set by PCCMP_ON_THR, as defined in Section 18.)

In the ACTIVE state, the host processor can read the Interrupt status fields in Register R31 in order to determine what action initiated the start-up. These fields indicate, for example, if the start-up was due to a reset caused by an error condition, or if the start-up was caused by a PWR_ON input, or if the start-up was caused by an RTC alarm. The first-level interrupt WKUP_INT is triggered whenever any of the second-level interrupt events described in Table 56 is set. See Section 24 for further details of Interrupt.

ADDRESS	BIT	LABEL	DESCRIPTION
R31 (1Fh) Comparator Interrupt Status	6	WKUP_OFF_STATE_EINT	Indicates that the chip started from the OFF state. (Rising Edge triggered) Note: This bit is cleared once read.
	5	WKUP_HIB_STATE_EINT	Indicated the chip started up from the hibernate state. (Rising Edge triggered) Note: This bit is cleared once read.
	4	WKUP_CONV_FAULT_EINT	Indicates the wakeup was caused by a converter fault leading to the chip being reset. (Rising Edge triggered) Note: This bit is cleared once read.
	3	WKUP_WDOG_RST_EINT	Indicates the wakeup was caused by a watchdog heartbeat being missed, and hence the chip being reset. (Rising Edge triggered) Note: This bit is cleared once read.

ADDRESS	BIT	LABEL	DESCRIPTION
	2	WKUP_GP_PWR_ON_EINT	PWR_ON (Alternate GPIO function) pin has been pressed for longer than specified time. (Rising Edge triggered) Note: This bit is cleared once read.
	1	WKUP_ONKEY_EINT	ON key has been pressed for longer than specified time. (Rising Edge triggered) Note: This bit is cleared once read.
	0	WKUP_GP_WAKEUP_EINT	WAKEUP (Alternate GPIO function) pin has been pressed for longer than specified time. (Rising Edge triggered) Note: This bit is cleared once read.
R39 (27h) Comparator Interrupt Status Mask	6:0	"IM_" + name of respective bit in R31	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R39 enables or masks the corresponding bit in R31. The default value for these bits is 0 (unmasked).

Table 56 Wake-Up Interrupts

14.3.2 POWER-UP SEQUENCING

The WM8351 power supply blocks can be commanded to start up according to a defined sequence when the WM8351 is commanded into the ACTIVE state. This sequence comprises fourteen timeslots, where the enabling of each DC-DC converter, LDO voltage regulator and the current limit switch is associated with one timeslot. In order to minimise supply in-rush current at power-up time, the start-up of these power supply blocks should be staggered in time by the use of this feature.

The WM8351 proceeds from one time slot to the next after a delay of approximately 1.28ms, provided that all power supply blocks started up in the current time slot (if any) have reached 90% of their programmed output voltage. See Section 14.3.4 for details of the WM8351 behaviour if any power supply block fails to achieve 90% of its programmed output voltage.

14.3.3 SHUTDOWN

The WM8351 goes from ACTIVE or HIBERNATE to the OFF state when a shutdown event occurs. Shutdown events include:

- Software shutdown (setting CHIP_ON = 0)
- A trigger signal on a GPIO pin configured as PWR_OFF lasting more than 5ms. The active polarity of this input is set by GPn_CFG for the applicable GPIO pin (see Section 20).
- A trigger signal on the ON pin lasting more than 10 seconds. The active polarity of this input is set by the register field ON_POL. If required, the de-bounce time can be set to 5 seconds using the ON_DEB_T register bit.
- Watchdog time-out (see Section 23) after 7 previous faults.
- Fault conditions programmed to trigger a shutdown (see Section 18).
- Thermal shutdown (see Section 25)

As part of the start-up sequence, the CHIP_ON bit is set to 1. The software shutdown is commanded by writing 0 to the CHIP_ON register field as described in Table 57.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) System Control 1	15	CHIP_ON	0	Indicates whether the system is on or off. Writing 0 to this bit powers down the whole chip. Registers which are affected by state machine reset will get reset. Once the system is turned OFF it can be restarted by any of the valid ON event.
	3	ON_DEB_T	0	ON pin off function debounce time 0 = 10s 1 = 5s
	1	ON_POL	1	ON pin polarity: 0 = Active high (ON) 1 = Active low (/ON)

Table 57 Software Shutdown

As part of the shutdown sequence, the WM8351 asserts the /RST and /MEMRST reset signals, resets its internal control registers, disables most of its functions, resets the CHIP_ON bit to 0 and moves to the OFF state. (Note that /MEMRST is an optional output available on GPIO pins only.)

14.3.4 POWER CYCLING

If an undervoltage fault or a limit switch overcurrent fault is detected (eg. during start-up, or when exiting the HIBERNATE state), the WM8351 will respond according to various configurable options. The Limit Switch and each of the DC Converters and LDO Regulators may be programmed to shutdown the system in the event of a fault condition. In these events (where a system shutdown is selected), the WM8351 will either shut down or will attempt to re-start, depending on the state of the POWERCYCLE register bit.

If POWERCYCLE = 0, then a fault condition will result in the shutdown of the WM8351, reverting to the OFF state. If POWERCYCLE = 1, then the WM8351 will make a maximum of 8 attempts to re-start. Each attempt will be scheduled at 200ms intervals. After 8 consecutive failed attempts, the WM8351 reverts to the OFF state and resets the power cycling counter. Any subsequent start-up event again has a maximum of 8 attempts to start up (provided that POWERCYCLE = 1).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) System Control	13	POWERCYCLE	0	Action to take on a fault (if fault response is set to shutdown system): 0 = Shut down 1 = Shutdown everything then go through startup sequence. ie. Reboot the system.

Table 58 Controlling Power Cycling

14.3.5 REGISTER RESET

The control registers of the WM8351 are reset when it goes into the OFF state. Under default conditions, the control registers are also reset when exiting the HIBERNATE state; this behaviour is selectable using the REG_RESET_HIB_MODE control bit.

In Development mode, the register reset in OFF can be disabled using the RECONFIG_AT_ON register field. See Section 14.4 for a definition of this field.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) System Hibernate	5	REG_RESET_HIB_MODE	0	Action of the internal register reset signal when going from Hibernate to Active. 0 = Do a register reset when leaving the hibernate state. 1 = Do not do a register reset when leaving the hibernate state

Table 59 Register Reset Control

14.3.6 RESET SIGNALS

The WM8351 provides an active-low reset output signal to the host processor on the open-drain /RST pin. The /RST pin is asserted low in the OFF state. The status of the /RST pin in HIBERNATE state is configurable using the RST_HIB_MODE bit.

In start-up, after all enabled power supplies reach 90% of their programmed output voltage, the /RST output is held low for a programmable duration set by RSTB_TO. The /RST pin is then set high. The /RST output is set low during the shutdown sequence.

In Configuration Mode 11 only, the "crystal detect" mode is enabled; this controls the /RST output behaviour. In this mode, the WM8351 monitors the 32kHz crystal oscillator during start-up to verify that the output frequency is valid. The /RST output is held low until this has been achieved.

An additional GPIO output, /RST can be generated, with the same functionality as the /RST pin. A GPIO pin must be configured as /RST in order to output this signal (see Section 20).

The WM8351 can also generate a separate /MEMRST signal for other subsystems such as external memory. This allows resetting some subsystems in the HIBERNATE state, while not resetting others. The /MEMRST feature is provided via a GPIO pin (see Section 20). Note that /MEMRST is not a valid control signal during the start-up as the GPIO pins are not configured at this time. The MEM_VALID field provides an indication of whether the contents of the external memory (under control of /MEMRST) are valid.

The /RST and /MEMRST signals can also be asserted under control of a manual reset input. A GPIO pin (see Section 20) must be configured as /MR to enable this feature. Note that the /MR input has no effect on the WM8351 circuits other than asserting /RST and /MEMRST.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) System Control 1	11:10	RSTB_TO [1:0]	11	Time that the /RST pin and /MEMRST output is held low after the chip reaches the active state. 00 = 15ms 01 = 30ms 10 = 60ms 11 = 120ms
	5	MEM_VALID	0	Indicates that the contents of external memory are still valid. This bit is cleared on startup and whenever /MEMRST is asserted from the main state machine. The system software should set this bit once the external memory has been set up. Controlled in hibernate mode by MEMRST_HIB_MODE 0 = External memory is not valid and needs restoring. 1 = External memory is valid.
R5 (05h) System Hibernate	4	RST_HIB_MODE	0	/RST pin state in hibernate mode: 0 = Asserted (low) 1 = Not asserted (high)
	2	MEMRST_HIB_MODE	0	/MEMRST (Alternative GPIO function) pin state in hibernate mode 0 = Asserted (low) 1 = Not asserted (high)

Table 60 Controlling Reset Signals

The WM8351 can be commanded to assert the /RST and /MEMRST signals by writing a logic '1' to the SYS_RST register bit. In this case, the /RST and /MEMRST outputs are asserted low for the duration specified by RSTB_TO.

Care must be taken if writing to this bit in 2-wire (I2C) Control Interface mode. The WM8351 will act upon the register write operation as soon as it has received the address and data fields; this may happen before the I2C Acknowledge has been clocked by the host processor. If the /RST signal causes the processor to reset before it has clocked the I2C Acknowledge, then the WM8351 will continue to assert the Acknowledge signal (ie. pull the SDA pin low) after the processor has completed its reset. On some processors, it may be necessary to toggle the SCLK pin in order to clear the Acknowledge signal and resume I2C communications.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) System Control 1	14	SYS_RST	0	Allows the processors to reboot itself 0 = Do nothing 1 = Perform a processor reset by asserting the /RST and /MEMRST (GPIO) pins for the programmed duration *Protected by security key.*

Table 61 Software Reset Command

14.4 DEVELOPMENT MODE

The WM8351 can start in different modes depending on the state of the CONF1 and CONF0 pins. Development mode is selected by tying CONF1 and CONF0 to logic 0.

Development mode gives complete control over the configuration and startup behaviour of the WM8351 and allows overriding the default values of selected registers (listed in Table 64). It enables configuration of the WM8351 before startup. This is especially useful for evaluation and debugging.

In low-volume production, an external 'genie' (low-cost, small-size microcontroller) may be used to configure the WM8351 in Development mode. The 'genie' is used to write the required register values to generate the desired supplies and to configure the GPIO pins as required. These register write operations can be achieved via a secondary control interface, which is provided by redirecting the control interface to two GPIO pins as described below.

The configuration mode pins CONF1 and CONF0 should be tied to fixed logic levels. The start-up sequence that they control is initiated on every transition from the OFF to the ACTIVE state.

14.4.1 CONTROL INTERFACE REDIRECTION

In Development mode, the 2-wire control interface is initially redirected from the primary control interface (dedicated SDATA and SCLK pins, which require a DBVDD supply) to the secondary control interface (the GPIO10 and GPIO11 pins, which can run on an externally generated supply provided through the LINE pin). When using GPIO pins for the Control Interface, GPIO11 provides the SDATA functionality, and GPIO10 provides the SCLK functionality.

Use of the secondary interface makes it possible to configure the WM8351 before the DBVDD supply voltage becomes available (e.g. in the OFF and PRE-ACTIVE states). The control interface can be switched back to the primary interface at any time by writing to the USE_DEV_PINS bit. In a typical application, the primary control interface would be selected after the WM8351 is fully configured.

The device address for the secondary control interface is 0x34h, and cannot be changed. In development mode only, the primary interface address can be selected by writing to the DEV_ADDR bits through the secondary interface. Note that this functionality is only available in Development mode.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Interface Control	15	USE_DEV_ PINS	1	Selects which pins to use for the 2-wire control: 0 = Use 2-wire I/F pins as 2-wire interface 1 = Use GPIO 10 and 11 as 2-wire interface, e.g. to download settings from PIC. Only applies when CONFIG pins[1:0] = 00.
	14:13	DEV_ADDR [1:0]	00	Selects device address (only valid when CONF_STS = 00) 00 = 0x34 01 = 0x36 10 = 0x3C 11 = 0x3E
Note: In custom modes (CONF[1:0]≠00), the secondary control interface is never used and the control bits described here have no effect.				

Table 62 Control Interface Switching in Development Mode

14.4.2 STARTING UP IN DEVELOPMENT MODE

In Development mode, the GPIO1 pin is configured as a DO_CONF output (see Section 20), which is asserted high to indicate that the WM8351 is about to start up. This may be used to trigger the 'genie' to configure the WM8351 via the secondary control interface.

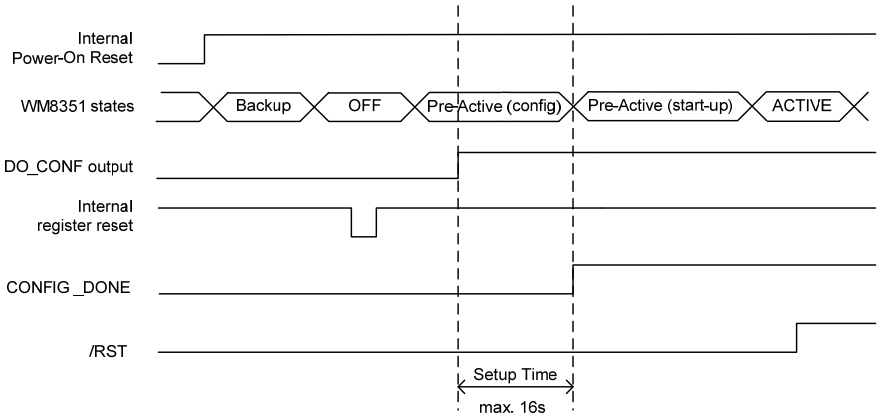


Figure 65 Configuration Timing in Development Mode

On completion of the register configuration, the power-up sequence is initiated by writing a logic 1 to the CONFIG_DONE bit. If the CONFIG_DONE bit is not set before the maximum set-up time has elapsed (see Figure 65), then the WM8351 will revert to the OFF state.

An alternative implementation is to start up the WM8351 by setting CONFIG_DONE to '1' without first programming the converter/LDO settings. By this method, the rising edge of the /RST signal may be used to trigger the WM8351 configuration process after the device has entered the ACTIVE state. In this case, the DC-DC converters and LDOs turn on immediately when they are enabled (time slots are no longer relevant because the WM8351 is already in the ACTIVE state). To reduce in-rush current, any configuration sequence triggered by /RST should therefore include supply staggering in software (i.e. time delays between powering up individual supply domains).

Note that, whether using DO_CONF or /RST to trigger configuration, the on-chip watchdog imposes a time-out for configuration; if the WM8351 watchdog is not serviced, it restarts the system. This can be prevented, if necessary, by disabling the watchdog.

By default, the DO_CONF output will be set low when the WM8351 enters the OFF state and set high on every transition from OFF to ACTIVE, re-triggering the external 'genie'. Also, by default, the internal control registers will be reset when the WM8351 enters the OFF state. This behaviour can be changed using the RECONFIG_AT_ON register bit. If RECONFIG_AT_ON is set to 0, then the control registers will not be reset when going into the OFF state, and the DO_CONF output will remain set high after the first powering up of the chip, regardless of subsequent state transitions.

De-selection of RECONFIG_AT_ON should be used with caution, as this can potentially lead to system failures in some applications. If RECONFIG_AT_ON is set to 0, and an OFF event occurs, then it is possible that control registers will not be set to the intended start-up values when the WM8351 subsequently returns to the ON state. The impact of this will depend upon the hardware and software of the particular target application, and is not necessarily a risk in every instance. Please contact Wolfson Applications support if further guidance is required on this topic.

Note that RECONFIG_AT_ON should never be set to 0 in Custom Modes 01, 10 or 11. Setting this bit to 0 may result in erroneous behaviour and deviation from the custom configuration settings. Under default settings, the control registers are always reset in the OFF state.

The register fields DO_CONF and RECONFIG_AT_ON are defined in Table 63.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Interface Control	12	CONFIG_DONE	0	Tells the system that the PIC micro has completed its programming. 0 = Programming still to be done 1 = Programming complete Only applies when CONFIG pins[1:0] = 00.
	11	RECONFIG_AT_ON	1	Selects whether to reset the registers in the OFF state and whether to reload the device configuration from the PIC when an ON event occurs. 0 = Do not reset registers in the OFF state. Do not load configuration data when an ON event occurs. 1 = Reset registers in the OFF state. Load configuration from the PIC when an ON event occurs. Note that, in development mode, the device configuration from the PIC is always loaded when first powering up the chip. This bit must always be set to default (1) in Custom Modes 01, 10 and 11.

Table 63 Start-Up Control in Development Mode

Note: if the WM8351 enters the BACKUP state as a result of an undervoltage condition (see Section 18), then the control registers will be reset, but DO_CONF will remain high. When the supply voltage rises and device comes out of BACKUP, the DO_CONF output will still be high. If the DO_CONF signal is used to trigger an external 'genie' device, then this may not work, as the DO_CONF has remained high through the BACKUP state transition, and the WM8351 device will become locked in the PRE-ACTIVE state when an ON event occurs.

This problem may be avoided by ensuring that the 'genie' monitors the LINE voltage in order to recognise the undervoltage condition, and that it verifies the I2C Acknowledge signal on the secondary interface (GPIO10 and GPIO11) to determine whether it can execute its programming function.

14.4.3 CONFIGURING THE WM8351 IN DEVELOPMENT MODE

The WM8351 can be configured in Development mode by writing to control bits that determine its startup behaviour. The locations of these register bits are shown in Table 64 below. A typical configuration sequence would include writes to some or all of the registers listed. If none of the highlighted bits in any given register needs to be changed from its default, then no write to that register is recommended.

The configuration bits include:

- Duration control bits for the /RST reset signal (RSTB_TO)
- GPIO pull-up / pull-down settings and debounce times (GP*n*_PD, GP*n*_PU, GP*n*_DB and GP_DBTIME)
- Alternate function and input/output selection for GPIO pins (GP*n*_FN, GP*n*_DIR and GP*n*_CFG)
- Voltage settings for DC-DC converters and LDO regulators (DC*n*_VSEL and LDO*n*_VSEL)
- Time slots for automatic start of all DC-DC converters, all LDO regulators and the Current Limit Switch during startup (DC*n*_ENSLOT, LDO*n*_ENSLOT and LS_ENSLOT). Note that supplies can be programmed to not start up automatically by setting the respective _ENSLOT bits to 0000.

Typically, the final step in the sequence is a write to register R6, in order to:

- Select the WM8351 device address on the primary control interface, using the DEV_ADDR bits.
- Allow the WM8351 to proceed to startup. This is achieved by setting the CONFIG_DONE bit (R6 bit 12) to 1.
- Switch the control interface back to the primary interface (if desired), so that a host processor can communicate with the WM8351. This is achieved by setting USE_DEV_PINS (R6 bit 15) to 0.

REGISTER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Select /RST duration																
R3 (03h)					RSTB_TO											
Unlock protected registers																
R219 (DBh)	0013h															
Alternate function and input/output selection for GPIO pins																
R140 (8Ch)	GP3_FN				GP2_FN				GP1_FN				GP0_FN			
R141 (8Dh)	GP7_FN				GP6_FN				GP5_FN				GP4_FN			
R142 (8Eh)	GP11_FN				GP10_FN				GP9_FN				GP8_FN			
R143 (8Fh)													GP12_FN			
R128 (80h)				GPn_DB (n = 0 to 12)												
R129 (81h)				GPn_PU (n = 0 to 12)												
R130 (82h)				GPn_PD (n = 0 to 12)												
R134 (86h)				GPn_DIR (n = 0 to 12)												
R135 (87h)				GPn_CFG (n = 0 to 12)												
Disable battery charger (only if battery type is not compatible with WM8351 charger)																
R168 (A8h)	0															
Re-lock protected registers																
R219 (DBh)	FFFFh															
Configure supply generation																
R180 (B4h)										DC1_VSEL[6:0]						
R181(B5h)			DC1_ENSLOT[3:0]													
R183 (B7h)			DC2_ENSLOT[3:0]													
R186 (BAh)										DC3_VSEL[6:0]						
R187 (BBh)			DC3_ENSLOT 3:0]													
R189 (BDh)										DC4_VSEL[6:0]						
R190 (BEh)			DC4_ENSLOT[3:0]													
R199 (C7h)			LS_ENSLOT[3:0]													
R200 (C8h)												LDO1_VSEL[4:0]				
R201 (C9h)			LDO1_ENSLOT[3:0]													
R203 (CAh)												LDO2_VSEL[4:0]				
R204 (CBh)			LDO2_ENSLOT[3:0]													
R206 (CEh)												LDO3_VSEL[4:0]				
R207 (CFh)			LDO3_ENSLOT[3:0]													
R209 (D1h)												LDO4_VSEL[4:0]				
R210 (D2h)			LDO4_ENSLOT[3:0]													
Proceed to startup and hand over to host processor																
R6 (06h)	0	DEV_ADDR		1												

Table 64 Suggested Sequence of Register Writes for WM8351 Configuration in Development Mode

Note that configuration only includes registers that are required for starting up correctly. All other register settings should be loaded after the WM8351 has started up.

Most of these control fields are described here within Section 14. See Section 11.6 for details of Register Locking. See Section 20 for details of the GPIO configuration fields. See Section 17.7 for details of the Battery Charger configuration.

When using the /RST signal to trigger configuration, writing to the _ENSLOT and RSTB_TO fields can be omitted (the reset and power-up sequence has already taken place, so the write would have no effect). However, additional writes to R13 or R176 should be added to enable the DC-DC converters and LDO regulators one by one.

14.5 CUSTOM MODES

The WM8351 provides three custom start-up modes. These are selected by setting the CONF1 and CONF0 pins = 01, 10 or 11. The custom mode start-up sequences define the following parameters:

- Polarity of the ON pin (Active low or high)
- Configuration of the USB power source
- Configuration of the Watchdog timer mode
- Configuration of the Control Interface mode
- Configuration of the 32kHz oscillator (enabled or disabled)
- Configuration of the real-time-clock (enabled or disabled)
- Configuration of LDO1
- Selection of crystal oscillator detect mode (see Section 14.3.6)
- Configuration of the voltage settings and start-up timeslots for DC-DC and LDO supplies
- Configuration of GPIO pins

In Development Mode, the RECONFIG_AT_ON register bit (see Section 14.4.2) may be used to control the device configuration behaviour. In Custom Modes 01, 10 or 11, the default setting (RECONFIG_AT_ON = 1) must always be used. Setting this bit to 0 may result in erroneous behaviour and deviation from the custom configuration settings.

The custom modes do not allow configuring the WM8351 in the OFF state. As a result, evaluation and debugging in custom modes is limited.

14.5.1 CONFIGURATION MODE 01

In Configuration Mode 01, the following general default settings apply:

PARAMETER	REGISTER SETTING	DESCRIPTION
ON polarity	ON_POL = 1	ON pin is Active Low
USB power source	USB_SLV_500MA = 1	Selects 500mA limit in USB slave
Watchdog timer	WDOG_MODE [1:0] = 00	Watchdog is disabled
Control Interface	SPI_3WIRE = 0 SPI_4WIRE = 0 SPI_CFG = 0	Control Interface is 2-wire mode
32kHz oscillator	OSC32K_ENA = 1	32kHz Oscillator is enabled
Real Time Clock	RTC_TICK_ENA = 1 RTC_CLKSRC = 0	Real Time Clock is enabled
LDO1	LDO1_PIN_MODE = 1 LDO1_PIN_EN = 0	LDO1 enabled at all times
Crystal detect mode		Crystal detect mode is not enabled.

The default voltages and the power-up sequence for all DC-DCs and LDOs in Configuration Mode 01 are shown below in Table 65 and Figure 66.

The time delay between each time slot is approximately 1.28ms.

Note that the Limit Switch is not enabled automatically in Configuration Mode 01; as a result, the Limit Switch remains open when the WM8351 enters the ACTIVE state.

SUPPLY	REGISTER SETTING	DESCRIPTION
DCDC1	DC1_ENSLOT [3:0] = 0011 DC1_VSEL [6:0] = 000_1110	Third timeslot 1.2V
DCDC2	DC2_ENSLOT [3:0] = 0000	Disabled
DCDC3	DC3_ENSLOT [3:0] = 0001 DC3_VSEL [6:0] = 010_0110	First timeslot 1.8V
DCDC4	DC4_ENSLOT [3:0] = 0010 DC4_VSEL [6:0] = 110_0010	Second timeslot 3.3V
LDO1	LDO1_ENSLOT [3:0] = 0000 LDO1_VSEL [4:0] = 0_0110	(See note below) 1.2V
LDO2	LDO2_ENSLOT [3:0] = 0011 LDO2_VSEL [4:0] = 1_0000	Third timeslot 1.8V
LDO3	LDO3_ENSLOT [3:0] = 0010 LDO3_VSEL [4:0] =1_1111	Second timeslot 3.3V
LDO4	LDO4_ENSLOT [3:0] = 0010 LDO4_VSEL [4:0] = 0_1010	Second timeslot 1.4V

Table 65 Default Supply Voltages / Power-up Sequence for Configuration Mode 01

Note: In this Configuration Mode, LDO1 is enabled at all times. Therefore, the setting of LDO1_ENSLOT has no effect.

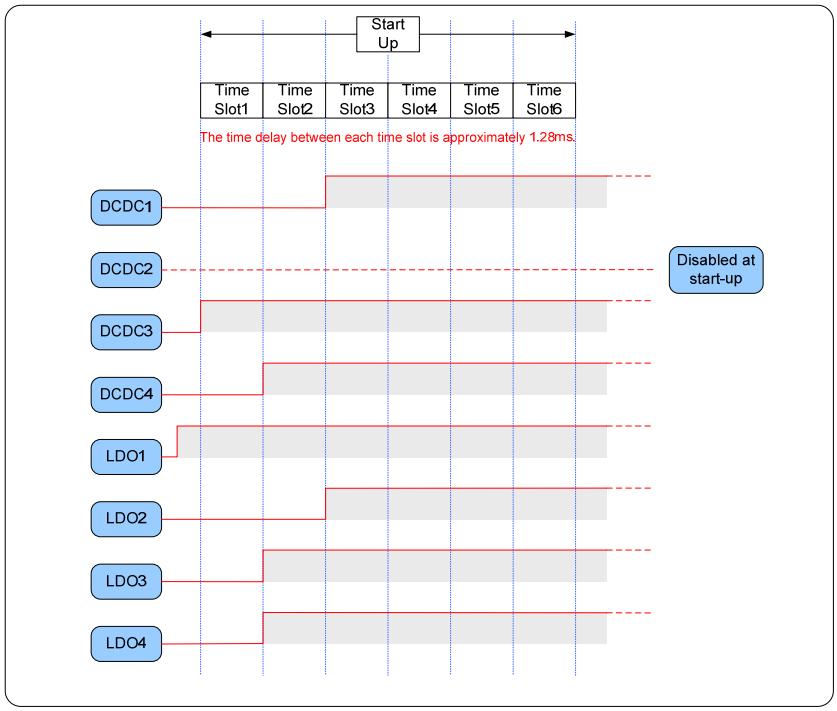


Figure 66 Power-up Sequence - Configuration Mode 01

The default GPIO settings for configuration mode 01 are shown below in Table 66.

GPIO PIN	POWER DOMAIN	DEFAULT GPIO FUNCTION	DEFAULT DIRECTION	DEFAULT PULL-UP / PULL-DOWN	DEFAULT DE-BOUNCE
GPIO0	VRTC	GP0_FN [3:0] = 0000 GPIO	GP0_DIR = 1 GP0_CFG =1 Input, Active High	GP0_PD=0 GP0_PU=0 Normal Mode	GP0_DB = 1 Debounce enabled
GPIO1	VRTC	GP1_FN [3:0] = 0000 GPIO	GP1_DIR = 1 GP1_CFG =1 Input, Active High	GP1_PD=0 GP1_PU=0 Normal Mode	GP1_DB = 1 Debounce enabled
GPIO2	VRTC	GP2_FN [3:0] = 0011 32KHZ	GP2_DIR = 0 GP2_CFG =1 Output, Open Drain	GP2_PD=0 GP2_PU=0 Normal Mode	GP2_DB = 1 Debounce enabled
GPIO3	VRTC	GP3_FN [3:0] = 0000 GPIO	GP3_DIR = 1 GP3_CFG =1 Input, Active High	GP3_PD=0 GP3_PU=0 Normal Mode	GP3_DB = 1 Debounce enabled
GPIO4	DBVDD	GP4_FN [3:0] = 0000 GPIO	GP4_DIR = 1 GP4_CFG =1 Input, Active High	GP4_PD=0 GP4_PU=0 Normal Mode	GP4_DB = 1 Debounce enabled
GPIO5	DBVDD	GP5_FN [3:0] = 0001 L_PWR1	GP5_DIR = 1 GP5_CFG =0 Input, Active Low	GP5_PD=0 GP5_PU=0 Normal Mode	GP5_DB = 1 Debounce enabled
GPIO6	DBVDD	GP6_FN [3:0] = 0001 L_PWR2	GP6_DIR = 1 GP6_CFG =0 Input, Active Low	GP6_PD=0 GP6_PU=0 Normal Mode	GP6_DB = 1 Debounce enabled
GPIO7	DBVDD	GP7_FN [3:0] = 0001 L_PWR3	GP7_DIR = 1 GP7_CFG =0 Input, Active Low	GP7_PD=0 GP7_PU=0 Normal Mode	GP7_DB = 1 Debounce enabled
GPIO8	DBVDD	GP8_FN [3:0] = 0011 /BATT_FAULT	GP8_DIR = 0 GP8_CFG =0 Output, CMOS	GP8_PD=0 GP8_PU=0 Normal Mode	GP8_DB = 1 Debounce enabled
GPIO9	DBVDD	GP9_FN [3:0] = 0001 /VCC_FAULT	GP9_DIR = 0 GP9_CFG =0 Output, CMOS	GP9_PD=0 GP9_PU=0 Normal Mode	GP9_DB = 1 Debounce enabled
GPIO10	LINE	GP10_FN [3:0] = 0000 GPIO	GP10_DIR = 1 GP10_CFG =1 Input, Active High	GP10_PD=0 GP10_PU=0 Normal Mode	GP10_DB = 1 Debounce enabled
GPIO11	LINE	GP11_FN [3:0] = 0000 GPIO	GP11_DIR = 1 GP11_CFG =1 Input, Active High	GP11_PD=0 GP11_PU=0 Normal Mode	GP11_DB = 1 Debounce enabled
GPIO12	LINE	GP12_FN [3:0] = 0011 LINE_SW	GP12_DIR = 0 GP12_CFG =0 Output, CMOS	GP12_PD=0 GP12_PU=0 Normal Mode	GP12_DB = 1 Debounce enabled

Table 66 Default GPIO Settings for Configuration Mode 01

14.5.2 CONFIGURATION MODE 10

In Configuration Mode 10, the following general default settings apply:

PARAMETER	REGISTER SETTING	DESCRIPTION
ON polarity	ON_POL = 1	ON pin is Active Low
USB power source	USB_SLV_500MA = 1	Selects 500mA limit in USB slave
Watchdog timer	WDOG_MODE [1:0] = 01	Watchdog set to Interrupt on Timeout
Control Interface	SPI_3WIRE = 0 SPI_4WIRE = 0 SPI_CFG = 0	Control Interface is 2-wire mode
32kHz oscillator	OSC32K_ENA = 1	32kHz Oscillator is enabled
Real Time Clock	RTC_TICK_ENA = 1 RTC_CLKSRC = 0	Real Time Clock is enabled, driven by the internal 32kHz oscillator
LDO1	LDO1_PIN_MODE = 0 LDO1_PIN_EN = 0	LDO1 controlled as normal via register bits
Crystal detect mode		Crystal detect mode is not enabled.

The default voltages and the power-up sequence for all DC-DCs and LDOs in Configuration Mode 10 are shown below in Table 67 and Figure 67.

The time delay between each time slot is approximately 1.28ms.

Note that the Limit Switch is not enabled automatically in Configuration Mode 10; as a result, the Limit Switch remains open when the WM8351 enters the ACTIVE state.

SUPPLY	REGISTER SETTING	DESCRIPTION
DCDC1	DC1_ENSLOT [3:0] = 0010 DC1_VSEL [6:0] = 001_1010	Second timeslot 1.5V
DCDC2	DC2_ENSLOT [3:0] = 0000	Disabled
DCDC3	DC3_ENSLOT [3:0] = 0001 DC3_VSEL [6:0] = 101_0110	First timeslot 3.0V
DCDC4	DC4_ENSLOT [3:0] = 0011 DC4_VSEL [6:0] = 010_0110	Third timeslot 1.8V
LDO1	LDO1_ENSLOT [3:0] = 0001 LDO1_VSEL [4:0] = 1_1100	First timeslot 3.0V
LDO2	LDO2_ENSLOT [3:0] = 0011 LDO2_VSEL [4:0] = 1_0000	Third timeslot 1.8V
LDO3	LDO3_ENSLOT [3:0] = 0000 LDO3_VSEL [4:0] = 1_0101	Disabled 2.3V
LDO4	LDO4_ENSLOT [3:0] = 0000 LDO4_VSEL [4:0] = 1_1010	Disabled 2.8V

Table 67 Default Supply Voltages / Power-up Sequence for Configuration Mode 10

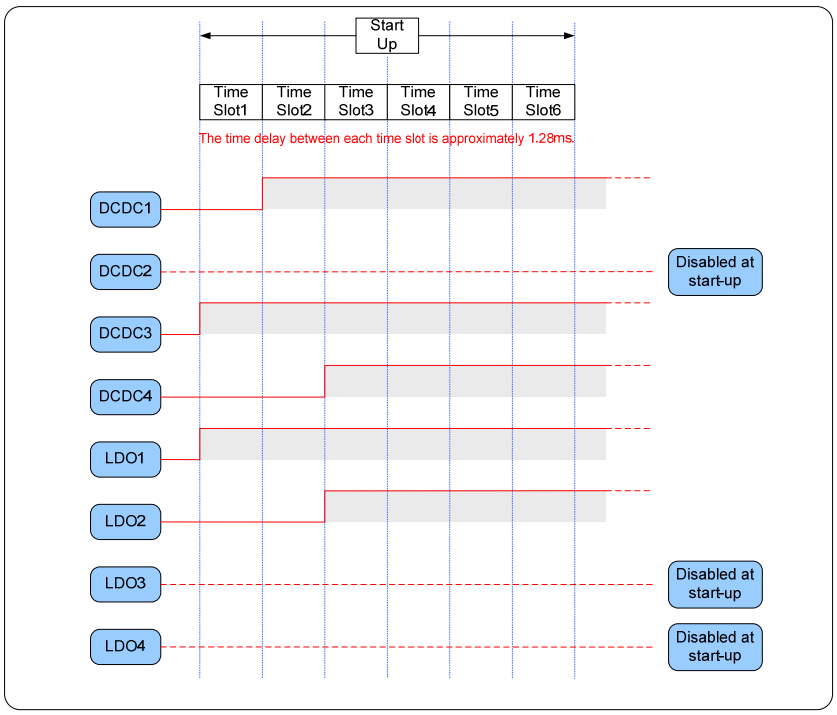


Figure 67 Power-up Sequence - Configuration Mode 10

The default GPIO settings for configuration mode 10 are shown below in Table 68.

GPIO PIN	POWER DOMAIN	DEFAULT GPIO FUNCTION	DEFAULT DIRECTION	DEFAULT PULL-UP / PULL-DOWN	DEFAULT DE-BOUNCE
GPIO0	VRTC	GP0_FN [3:0] = 0000 GPIO	GP0_DIR = 0 GP0_CFG =0 Output, CMOS	GP0_PD=0 GP0_PU=0 Normal Mode	GP0_DB = 1 Debounce enabled
GPIO1	VRTC	GP1_FN [3:0] = 0001 PWR_ON	GP1_DIR = 1 GP1_CFG =1 Input, Active High	GP1_PD=0 GP1_PU=0 Normal Mode	GP1_DB = 1 Debounce enabled
GPIO2	VRTC	GP2_FN [3:0] = 0011 32kHz	GP2_DIR = 0 GP2_CFG =1 Output, Open Drain	GP2_PD=0 GP2_PU=0 Normal Mode	GP2_DB = 1 Debounce enabled
GPIO3	VRTC	GP3_FN [3:0] = 0001 PWR_ON	GP3_DIR = 1 GP3_CFG =0 Input, Active Low	GP3_PD=0 GP3_PU=0 Normal Mode	GP3_DB = 1 Debounce enabled
GPIO4	DBVDD	GP4_FN [3:0] = 0011 HIBERNATE Level	GP4_DIR = 1 GP4_CFG =1 Input, Active High	GP4_PD=1 GP4_PU=0 Pull-down	GP4_DB = 1 Debounce enabled
GPIO5	DBVDD	GP5_FN [3:0] = 0000 GPIO	GP5_DIR = 1 GP5_CFG =1 Input, Active High	GP5_PD=0 GP5_PU=0 Normal Mode	GP5_DB = 1 Debounce enabled
GPIO6	DBVDD	GP6_FN [3:0] = 0000 GPIO	GP6_DIR = 1 GP6_CFG =1 Input, Active High	GP6_PD=0 GP6_PU=0 Normal Mode	GP6_DB = 1 Debounce enabled
GPIO7	DBVDD	GP7_FN [3:0] = 0000 GPIO	GP7_DIR = 1 GP7_CFG =1 Input, Active High	GP7_PD=0 GP7_PU=0 Normal Mode	GP7_DB = 1 Debounce enabled
GPIO8	DBVDD	GP8_FN [3:0] = 0000 GPIO	GP8_DIR = 1 GP8_CFG =1 Input, Active High	GP8_PD=1 GP8_PU=0 Pull-down	GP8_DB = 1 Debounce enabled
GPIO9	DBVDD	GP9_FN [3:0] = 0000 GPIO	GP9_DIR = 0 GP9_CFG =0 Output, CMOS	GP9_PD=0 GP9_PU=0 Normal Mode	GP9_DB = 1 Debounce enabled
GPIO10	LINE	GP10_FN [3:0] = 0000 GPIO	GP10_DIR = 0 GP10_CFG =1 Output, Open Drain	GP10_PD=0 GP10_PU=0 Normal Mode	GP10_DB = 1 Debounce enabled
GPIO11	LINE	GP11_FN [3:0] = 0010 /WAKEUP	GP11_DIR = 1 GP11_CFG =1 (see note)	GP11_PD=0 GP11_PU=0 Normal Mode	GP11_DB = 1 Debounce enabled
GPIO12	LINE	GP12_FN [3:0] = 0000 GPIO	GP12_DIR = 0 GP12_CFG =0 Output, CMOS	GP12_PD=0 GP12_PU=0 Normal Mode	GP12_DB = 1 Debounce enabled
Note: The alternate GPIO functions PWR_ON and /WAKEUP are system wakeup events. The debounce time of these functions are determined by GP_DBTIME[1:0] + 40ms					

Table 68 Default GPIO Settings for Configuration Mode 10

Note that setting GP11_CFG = 1 results in Active Low function for /WAKEUP. In most cases, setting GPn_CFG = 1 results in Active High function, but /MR, /WAKEUP and /LDO_ENA are exceptions to this. See Section 20.

14.5.3 CONFIGURATION MODE 11

In Configuration Mode 11, the following general default settings apply:

PARAMETER	REGISTER SETTING	DESCRIPTION
ON polarity	ON_POL = 1	ON pin is Active Low
USB power source	USB_SLV_500MA = 1	Selects 500mA limit in USB slave
Watchdog timer	WDOG_MODE [1:0] = 00	Watchdog is disabled
Control Interface	SPI_3WIRE = 0 SPI_4WIRE = 0 SPI_CFG = 0	Control Interface is 2-wire mode
32kHz oscillator	OSC32K_ENA = 1	32kHz Oscillator is enabled
Real Time Clock	RTC_TICK_ENA = 1 RTC_CLKSRC = 0	Real Time Clock is enabled, driven by the internal 32kHz oscillator
LDO1	LDO1_PIN_MODE = 0 LDO1_PIN_EN = 0	LDO1 controlled as normal via register bits
Crystal detect mode		Crystal detect mode is enabled. (/RST output is held low until 32kHz oscillator is valid.)

The default voltages and the power-up sequence for all DC-DCs and LDOs in configuration mode 11 are shown below in Table 69 and Figure 68.

The time delay between each time slot is approximately 1.28ms.

Note that the Limit Switch is not enabled automatically in Configuration Mode 11; as a result, the Limit Switch remains open when the WM8351 enters the ACTIVE state.

SUPPLY	REGISTER SETTING	DESCRIPTION
DCDC1	DC1_ENSLOT [3:0] = 0001 DC1_VSEL [6:0] = 000_1110	First timeslot 1.2V
DCDC2	DC2_ENSLOT [3:0] = 0000	Disabled
DCDC3	DC3_ENSLOT [3:0] = 0010 DC3_VSEL [6:0] = 010_0110	Second timeslot 1.8V
DCDC4	DC4_ENSLOT [3:0] = 0101 DC4_VSEL [6:0] = 110_0010	Fifth timeslot 3.3V
LDO1	LDO1_ENSLOT [3:0] = 0011 LDO1_VSEL [4:0] = 0_0110	Third timeslot 1.2V
LDO2	LDO2_ENSLOT [3:0] = 0000 LDO2_VSEL [4:0] = 1_0110	Disabled 2.4V
LDO3	LDO3_ENSLOT [3:0] = 0000 LDO3_VSEL [4:0] = 1_1001	Disabled 2.7V
LDO4	LDO4_ENSLOT [3:0] = 0100 LDO4_VSEL [4:0] = 1_1010	Fourth timeslot 2.8V

Table 69 Default Supply Voltages / Power-up Sequence for Configuration Mode 11

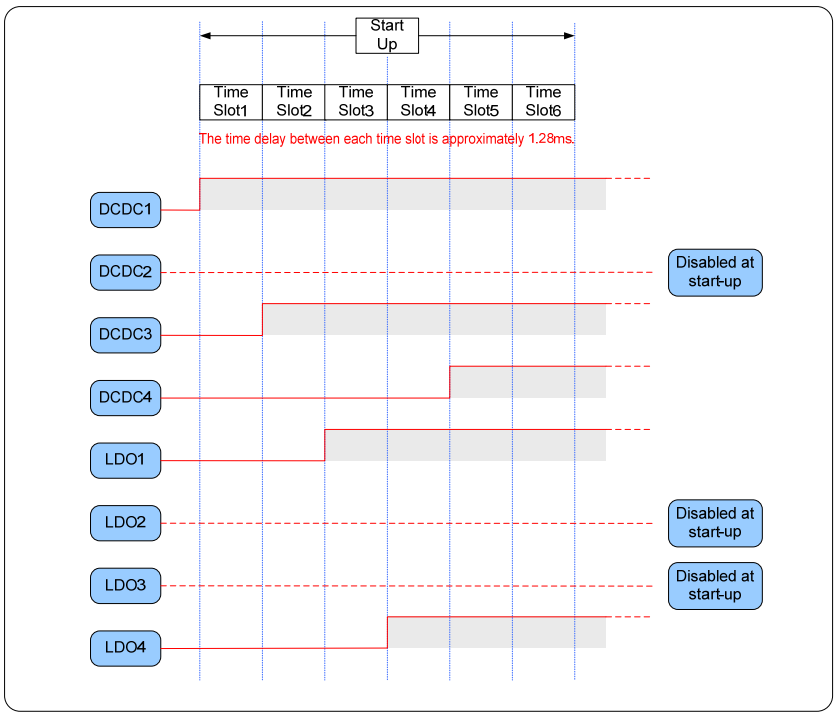


Figure 68 Power-up Sequence - Configuration Mode 11

The default GPIO settings for configuration mode 11 are shown below in Table 70.

GPIO PIN	POWER DOMAIN	DEFAULT GPIO FUNCTION	DEFAULT DIRECTION	DEFAULT PULL-UP / PULL-DOWN	DEFAULT DE-BOUNCE
GPIO0	VRTC	GP0_FN [3:0] = 0000 GPIO	GP0_DIR = 1 GP0_CFG =1 Input, Active High	GP0_PD=0 GP0_PU=0 Normal Mode	GP0_DB = 0 Debounce enabled
GPIO1	VRTC	GP1_FN [3:0] = 0001 PWR_ON	GP1_DIR = 1 GP1_CFG =0 Input, Active Low	GP1_PD=0 GP1_PU=0 Normal Mode	GP1_DB = 1 Debounce enabled
GPIO2	VRTC	GP2_FN [3:0] = 0011 32kHz	GP2_DIR = 0 GP2_CFG =1 Output, Open Drain	GP2_PD=0 GP2_PU=0 Normal Mode	GP2_DB = 1 Debounce enabled
GPIO3	VRTC	GP3_FN [3:0] = 0000 GPIO	GP3_DIR = 1 GP3_CFG =1 Input, Active High	GP3_PD=0 GP3_PU=0 Normal Mode	GP3_DB = 1 Debounce enabled
GPIO4	DBVDD	GP4_FN [3:0] = 0001 /MR	GP4_DIR = 1 GP4_CFG =1 (see note)	GP4_PD=0 GP4_PU=1 Pull-up	GP4_DB = 1 Debounce enabled
GPIO5	DBVDD	GP5_FN [3:0] = 0000 GPIO	GP5_DIR = 1 GP5_CFG =1 Input, Active High	GP5_PD=0 GP5_PU=0 Normal Mode	GP5_DB = 1 Debounce enabled
GPIO6	DBVDD	GP6_FN [3:0] = 0000 GPIO	GP6_DIR = 1 GP6_CFG =1 Input, Active High	GP6_PD=0 GP6_PU=0 Normal Mode	GP6_DB = 1 Debounce enabled
GPIO7	DBVDD	GP7_FN [3:0] = 0000 GPIO	GP7_DIR = 1 GP7_CFG =1 Input, Active High	GP7_PD=0 GP7_PU=0 Normal Mode	GP7_DB = 1 Debounce enabled
GPIO8	DBVDD	GP8_FN [3:0] = 0000 GPIO	GP8_DIR = 1 GP8_CFG =1 Input, Active High	GP8_PD=0 GP8_PU=0 Normal Mode	GP8_DB = 1 Debounce enabled
GPIO9	DBVDD	GP9_FN [3:0] = 0000 GPIO	GP9_DIR = 1 GP9_CFG =1 Input, Active High	GP9_PD=0 GP9_PU=0 Normal Mode	GP9_DB = 1 Debounce enabled
GPIO10	LINE	GP10_FN [3:0] = 0011 CH_IND	GP10_DIR = 0 GP10_CFG =1 Output, Open Drain	GP10_PD=0 GP10_PU=0 Normal Mode	GP10_DB = 1 Debounce enabled
GPIO11	LINE	GP11_FN [3:0] = 0010 /WAKEUP	GP11_DIR = 1 GP11_CFG =1 (see note)	GP11_PD=0 GP11_PU=0 Normal Mode	GP11_DB = 1 Debounce enabled
GPIO12	LINE	GP12_FN [3:0] = 0011 LINE_SW	GP12_DIR = 0 GP12_CFG =0 Output, CMOS	GP12_PD=0 GP12_PU=0 Normal Mode	GP12_DB = 1 Debounce enabled
Note: The alternate GPIO functions PWR_ON and /WAKEUP are system wakeup events. The debounce time of these functions are determined by GP_DBTIME[1:0] + 40ms					

Table 70 Default GPIO Settings for Configuration Mode 11

Note that setting GP4_CFG = 1 results in Active Low function for /MR. Also, setting GP11_CFG = 1 results in Active Low function for /WAKEUP. In most cases, setting GPn_CFG = 1 results in Active High function, but /MR, /WAKEUP and /LDO_ENA are exceptions to this. See Section 20.

14.6 CONFIGURING THE DC-DC CONVERTERS

The configuration of the DC-DC converters is described in the following sections. Some of the control fields form part of the Custom Mode configuration settings and therefore will not require to be set in software in some applications.

14.6.1 DC-DC CONVERTER ENABLE

The DC-DC Converters can be enabled in software using the register fields defined in Table 71. All DC-DC converters include a soft-start feature that helps to reduce the inductor current at start up. In order to further reduce supply in-rush current, individual converters should be programmed to start in different time slots within the start-up sequence.

In the WM8351 ACTIVE state, the DC-DC Converters can be enabled in software using the DC*n*_ENA bits. Setting these bits whilst in the Pre-Active state (see Figure 65) will not immediately enable the corresponding DC-DC converter; these bits will only become effective once the WM8351 has reached the ACTIVE state.

Each Converter may be programmed to switch on in a selected timeslot within the start-up sequence. The WM8351 will set the DC*n*_ENA field for any DC-DC converter that is enabled during the start-up sequence. Note that setting the DC*n*_ENSLOT fields in software is only relevant to the Development Mode, as these fields are assigned preset values in each of the Custom Modes.

Each Converter may be programmed to switch off in a selected timeslot within the shutdown sequence. If a Converter is not allocated to one of the 14 shutdown timeslots, it will be disabled when the WM8351 enters the OFF state.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Note: *n* is a number between 1 and 6 that identifies the individual DC-DC converter				
R13 (0Dh) or R176 (B0h)	0,1,2,3	DC*n*_ENA	Dependant on CONFIG[1:0] settings	DCDC*n* converter enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.
Note: These bits can be accessed through R13 or through R176. Reading from or writing to either register location has the same effect.				
R181 (B5h) for DC-DC1 R184 (B8h) for DC-DC2	13:10	DC*n*_ENSLOT [3:0]	Dependant on CONFIG[1:0] settings	Time slot for DC-DC*n* start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start up on entering ACTIVE
R187 (BBh) for DC-DC3 R190 (BEh) for DC-DC4	9:6	DC*n*_SDSLOT [3:0]	0000	Time slot for DC-DCn shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF
Note: *n* is number between 1 and 4 that identifies the individual DC-DC converter				

Table 71 Enabling and Disabling the DC-DC Converters

14.6.2 CLOCKING

The DC-DC converters are controlled by an internally generated clock signal from the RC Oscillator with a constant frequency of around 2.0MHz for DC-DC 1, 3 and 4, and a constant frequency of around 1.0MHz for DC-DC 2.

14.6.3 DC-DC BUCK (STEP-DOWN) CONVERTER CONTROL

DC-DC Converters 1, 3 and 4 are buck converters which can be configured to operate in different operating modes using the register bits described in Table 72.

In Active mode, the DC-DC Converters operate to their highest level of performance. The DC-DC Converters will automatically select PWM or Pulse-Skipping operation according to the load condition. This enables the power efficiency to be maximised across a wide range of load conditions. It is possible to force the Converters to use the higher performance PWM mode; in this mode, pulse-skipping is disabled and the output voltage is regulated by switching at a constant frequency which improves the transient response at light loads.

In Standby/Hysteretic Mode, the DC-DC Converters disable some of the internal control circuitry in order to reduce power consumption. The load regulation may be degraded in this mode of operation. The efficiency data in Section 9.2.1 shows the conditions under which Standby Mode can offer better efficiency than Active Mode.

In LDO Mode, the DC-DC Converters are reconfigured as low power LDOs.

When DC*n*_SLEEP = 0, the corresponding DC*n*_ACTIVE register bit selects between Active and Standby/Hysteretic modes for the associated DC-DC converter.

The DC*n*_SLEEP register bits control the selection of LDO Mode. Setting DC*n*_SLEEP = 1 selects LDO Mode. This bit takes precedence over the corresponding DC*n*_ACTIVE bit.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R177 (B1h) DC-DC Active Options	0	DC1_ACTIVE	1	DC-DC*n* Active mode 0 = Select Standby mode 1 = Select Active mode
	2	DC3_ACTIVE	1	
	3	DC4_ACTIVE	1	
R178 (B2h) DC-DC Sleep Options	0	DC1_SLEEP	0	DC-DC*n* Sleep Mode 0 = Normal DC-DC operation 1 = Select LDO mode
	2	DC3_SLEEP	0	
	3	DC4_SLEEP	0	
Note: *n* is either 1, 3 or 4 and identifies the individual DC-DC converter				
R248 (F8h) DCDC1 Test Controls	4	DC1_FORCE_PWM	0	Force DC-DC1 PWM mode 0 = Normal DC-DC operation 1 = Force DC-DC PWM mode
R250 (FAh) DCDC3 Test Controls	4	DC3_FORCE_PWM	0	Force DC-DC3 PWM mode 0 = Normal DC-DC operation 1 = Force DC-DC PWM mode
R251 (FBh) DCDC4 Test Controls	4	DC4_FORCE_PWM	0	Force DC-DC4 PWM mode 0 = Normal DC-DC operation 1 = Force DC-DC PWM mode

Table 72 Operating Mode Control for DC-DC Converters 1, 3 and 4

DC-DC Converters 1, 3 and 4 can also be controlled by the device HIBERNATE bit, or by hardware input signals L_PWR1, L_PWR2 and L_PWR3. Several GPIO pins can be assigned as L_PWR pins. Each converter can be assigned to one of these three signals, or else to the device HIBERNATE bit. The signals are active high and each converter's response to the selected signal is programmable as defined in Table 73.

Note that, when a GPIO pin is configured as a Hibernate input pin, and this input is asserted, then all DC-DC Converters will be placed in Hibernate mode.

In order to use GPIO pins as L_PWR pins, they must be configured by setting the respective GP*n*_FN, and GP*n*_DIR bits to the appropriate value (see Section 20).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R182 (B6h) for DC-DC1 R188 (BCh) for DC-DC3 R191 (BFh) for DC-DC4	14:12	DC*n*_HIB_MODE [2:0]	001	DC-DC*n* Hibernate behaviour: 000 = Use current settings (no change) 001 = Select voltage image settings 010 = Force standby mode 011 = Force standby mode and voltage image settings 100 = Force LDO mode 101 = Force LDO mode and voltage image settings 110 = Reserved 111 = Disable output
	9:8	DC*n*_HIB_TRIG [1:0]	00	DC-DC*n* Hibernate signal select 00 = HIBERNATE register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3 Note that Hibernate is also selected when a GPIO Hibernate input is asserted.
Note: *n* is either 1, 3 or 4 and identifies the individual DC-DC converter				

Table 73 Low-Power Mode Control for DC-DC Converters 1, 3 and 4

The default output voltage for DC-DC Converters 1, 3 and 4 is set by writing to the DC*n*_VSEL register bits. The 'image' voltage settings DC*n*_VIMG are alternate values that may be invoked when the HIBERNATE software or hardware control is asserted as described above.

The DC-DC Converters 1, 3 and 4 are dynamically programmable - the output voltage may be adjusted in software at any time. These Converters are buck (step-down) converters; their output voltage can therefore be lower than the input voltage, but cannot be higher.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R180 (B4h) for DC-DC1 R186 (BAh) for DC-DC3 R189 (BDh) for DC-DC4	6:0	DC*n*_VSEL [6:0]	Dependant on CONFIG[1:0] settings	DC-DC*n* Converter output voltage settings in 25mV steps. Maximum output = 3.4V. 110 0110 = 3.4V 110 0010 = 3.3V 101 0110 = 3.0V 100 1110 = 2.8V …… 010 0110 = 1.8V 000 1110 = 1.2V 000 0110 = 1.0V 000 0000 = 0.85V
R182 (B6h) for DC-DC1 R188 (BCh) for DC-DC3 R191 (BFh) for DC-DC4	6:0	DC*n*_VIMG [6:0]	000 0110	DC-DC*n* Converter output image voltage settings in 25mv steps. Maximum output = 3.4V. 110 0110 = 3.4V 110 0010 = 3.3V 101 0110 = 3.0V 100 1110 = 2.8V …… 010 0110 = 1.8V 000 1110 = 1.2V 000 0110 = 1.0V 000 0000 = 0.85V
Note: *n* is either 1, 3 or 4 and identifies the individual DC-DC converter				

Table 74 Output Voltage Control for DC-DC Converters 1, 3 and 4

When the DC-DC Converters 1, 3 and 4 are disabled, the output can be set to float or else the outputs can be actively discharged through internal resistors. This feature is controlled using the register bits described in Table 75.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R180 (B4h) for DC-DC1 R186 (BAh) for DC-DC3 R189 (BDh) for DC-DC4	10	DC*n*_OPFLT	0	Enable discharge of DC-DC*n* outputs when DC-DC*n* is disabled 0 = Enabled - Output to be discharged 1 = Disabled - Output is left floating
Note: *n* is either 1, 3 or 4 and identifies the individual DC-DC converter				

Table 75 Output Float Control for DC-DC Converters 1, 3 and 4

A summary of the Mode Control and Voltage Control for DC-DC Converter 1 is provided in Table 76. Note that "Hibernate" in Table 76 refers to a GPIO Hibernate input or to the applicable Hibernate signal selected by the DC1_HIB_TRIG field.

The equivalent logic applies for DC-DC 3 and 4. Note that the DC-DC Converters must also be enabled as described in Table 71.

HIBERNATE	DC1_HIB_MODE	DC1_SLEEP	DC1_ACTIVE	OPERATING MODE	OUTPUT VOLTAGE
0	X	0	0	Standby/Hysteretic	DC1_VSEL
0	X	0	1	Active	DC1_VSEL
0	X	1	X	LDO Mode	DC1_VSEL
1	000	0	0	Standby/Hysteretic	DC1_VSEL
		0	1	Active	DC1_VSEL
		1	X	LDO Mode	DC1_VSEL
	001	0	0	Standby/Hysteretic	DC1_VIMG
		0	1	Active	DC1_VIMG
		1	X	LDO Mode	DC1_VIMG
	010	X	X	Standby/Hysteretic	DC1_VSEL
	011	X	X	Standby/Hysteretic	DC1_VIMG
	100	X	X	LDO Mode	DC1_VSEL
	101	X	X	LDO Mode	DC1_VIMG
	110	X	X	Disabled	N/A
	111	X	X	Disabled	N/A

Table 76 DC1 Converter Operating Mode Selection

14.6.4 DC-DC BOOST (STEP-UP) CONVERTER CONTROL

DC-DC Converter 2 is a boost converter which can be configured to operate in different operating modes, using the register bits described in Table 77.

In Switch mode, the DC-DC Converter acts as a switch between VP2 and L2. The switch is enabled (closed) by setting DC2_ENA = 1. The switch is disabled (opened) by setting DC2_ENA = 0. Note that the switch voltage source on VP2 must be >1.2V to ensure reliable operation.

In Boost mode, the DC-DC Converter operates as a step-up converter, employing current-mode architecture, capable of powering LED lights. The output voltage can be higher than the input voltage, but cannot be lower. Different configurations of voltage feedback are available in boost mode, to control the output voltage in different ways. The voltage feedback mode is selected by the DC2_FBSRC register field.

When DC2_FBSRC = 00, the converter's output voltage is set by two external resistors connected to FB2. See Section 29 for Applications Information covering the selection of suitable components.

When DC2_FBSRC = 01, the converter uses the ISINKA pin as feedback and adjusts its output voltage in order to achieve the required ISINKA current.

When DC2_FBSRC = 11, the converter's output voltage is set by two internal resistors, resulting in a fixed 5V output, suitable for USB interfaces.

The current-controlled configuration using ISINKA is intended for controlling a string of serially-connected LEDs driven by the DC-DC boost converter. See Table 97 for a definition of the CS1_ISEL register field which determines the required ISINKA current. In this mode, external resistors connected on the FB2 pin determine the maximum output voltage. See Section 29 for Applications Information covering the selection of suitable components.

In all configurations, the input pin VP2 must be externally wired to one of the supply rails, BATT or LINE. Using LINE has the advantage that the converters can operate when the battery is flat, defective or absent. Note that VP2 should not be connected to the USB supply rail.

The DC2_RMPH and DC2_RMPL bits defined in Table 77 should be set according to the desired output voltage in order to optimise the transient response of the converter. Selecting a different value could result in sub-harmonic oscillation of the converter.

The DC2_ILIM bits defined in Table 77 should be set according to the intended output load conditions.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R183 (B7h) DC-DC2 Control	14	DC2_MODE	0	DC-DC2 Converter Mode 0 = boost mode 1 = switch mode
	6	DC2_ILIM	0	DC-DC2 peak current limit select 0 = Higher peak current 1 = Lower peak current
	4:3	DC2_RMPH DC2_RMPL	01	DC-DC2 compensation ramp {DC2_RMPH, DC2_RMPL} 00 = 20V < VOUT ≤ 30V 01 = 10V < VOUT ≤ 20V 10 = 5V < VOUT ≤ 10V 11 = VOUT ≤ 5V (will be chosen automatically if DC2_FBSRC=11)
	1:0	DC2_FBSRC [1:0]	00	DC-DC*n* voltage feedback selection 00 = voltage feedback (using external resistor divider on pin FB*n*) 01 = current sink ISINKA used as feedback 10 = Reserved 11 = voltage feedback (using internal resistor divider on pin USB)

Table 77 Operating Mode Control for DC-DC Converter 2

DC-DC Converter 2 can also be controlled by the device HIBERNATE bit, or by hardware input signals L_PWR1, L_PWR2 and L_PWR3. Several GPIO pins can be assigned as L_PWR pins. The converter can be assigned to one of these three signals, or else to the device HIBERNATE bit. The signals are active high and the converter's response to the selected signal is programmable as defined in Table 78.

Note that, when a GPIO pin is configured as a Hibernate input pin, and this input is asserted, then all DC-DC Converters will be placed in Hibernate mode.

In order to use GPIO pins as L_PWR pins, they must be configured by setting the respective GP*n*_FN, and GP*n*_DIR bits to the appropriate value (see Section 20).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R183 (B7h) DC-DC2 Control	12	DC2_HIB_MODE	0	DC-DC2 Hibernate behaviour: 0 = Continue as in Active state 1 = Disable converter output
	9:8	DC2_HIB_TRIG [1:0]	00	DC-DC2 Hibernate signal select 00 = HIBERNATE register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3 Note that Hibernate is also selected when a GPIO Hibernate input is asserted.

Table 78 Hibernate Mode Control for DC-DC Converter 2

14.6.5 INTERRUPTS AND FAULT PROTECTION

Each DC-DC Converter is monitored for voltage accuracy and fault conditions. An undervoltage condition is set if the voltage falls below 95% of the required level. The action taken in response to a fault condition can be set independently for each DC-DC Converter, as described in Table 79.

The DC*n*_ERRACT fields configure the fault response to disable the respective converter or to shut down the entire system if desired. In addition, DC-DC Converter fault conditions also generate a second-level interrupt (see Section 24).

To prevent false alarms during short current surges, faults are only signalled if the fault condition persists. When a DC-DC Converter is started up, any initial fault condition is ignored until the Converter has been allowed time to settle. The time for which any fault condition is ignored is set by the PUTO register field, as described in Table 79.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R181 (B5h) for DC-DC1 R184 (B8h) for DC-DC2 R187 (BBh) for DC-DC3 R190 (BEh) for DC-DC4	15:14	DC*n*_ERRACT [1:0]	00	Action to take on DC-DC*n* fault (as well as generating an interrupt): 00 = ignore 01 = shut down converter 10 = shut down system 11 = reserved (shut down system)
R177 (B1h) DCDC Active options	13:12	PUTO [1:0]	00	Power up time out value for all converters 00 = 0.5ms 01 = 2ms 10 = 32ms 11 = 256ms
Note: *n* is a number between 1 and 4 that identifies the individual DC-DC converter				

Table 79 Fault Responses for DC-DC Converters

The DC-DC Converters and the LDO Regulators have a first-level interrupt, UV_INT (see Section 24). This comprises second-level interrupts from each of the DC-DC Converters and the LDO Regulators.

Each DC-DC Converter has a dedicated second-level interrupt which indicates an under-voltage condition. These can be masked by setting the applicable mask bit as defined in Table 80.

ADDRESS	BIT	LABEL	DESCRIPTION
R28 (1Ch) Under Voltage Interrupt Status	3	UV_DC4_EINT	DCDC4 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	2	UV_DC3_EINT	DCDC3 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	1	UV_DC2_EINT	DCDC2 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	0	UV_DC1_EINT	DCDC1 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R36 (24h) Under Voltage Interrupt Mask	as in R28	"IM_" + name of respective bit in R28	Mask bits for DC-DC converter under-voltage interrupts Each of these bits masks the respective bit in R28 when it is set to 1 (e.g. UV_DC1_EINT in R28 does not trigger a UV_INT interrupt when IM_UV_DC1_EINT in R36 is set).
Note: there is no over-current fault condition for converter 2.			

Table 80 DC-DC Converter Interrupts

The status of the DC-DC Converters can be indicated and monitored externally via a GPIO pin configured as /VCC_FAULT (see Section 20). When a GPIO pin is configured as /VCC_FAULT output, a logic low level on this pin indicates that there is a fault condition on one of the LDO Regulators, DC-DC Converters, or the Current Limit switch.

The /VCC_FAULT output is configurable by the control fields in Register R215. The fields described in Table 81 determine which of the DC-DCs contribute to the /VCC_FAULT indication. An undervoltage or overvoltage condition on any unmasked DC-DC Converter will cause the /VCC_FAULT output to be set to logic low.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R215 (D7h) VCC_FAULT	3	DC4_FAULT	0	DCDC4 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault
	2	DC3_FAULT	0	DCDC3 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault
	1	DC2_FAULT		DCDC2 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault
	0	DC1_FAULT		DCDC1 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault

Table 81 DC Converter /VCCFAULT Mask Bits

14.7 CONFIGURING THE LDO REGULATORS

The configuration of the LDO Regulators is described in the following sections. Some of the control fields form part of the Custom Mode configuration settings and therefore will not require to be set in software in some applications.

14.7.1 LDO REGULATOR ENABLE

The LDO Regulators can be enabled in software using the register fields defined in Table 82. To reduce supply in-rush current, individual regulators should be programmed to start in different time slots within the start-up sequence.

In the WM8351 ACTIVE state, the LDO Regulators can be enabled in software using the LDO*n*_ENA bits. Setting these bits whilst in the Pre-Active state (see Figure 65) will not immediately enable the corresponding LDO Regulators; these bits will only become effective once the WM8351 has reached the ACTIVE state.

Each Regulator may be programmed to switch on in a selected timeslot within the start-up sequence. The WM8351 will set the LDO*n*_ENA field for any LDO Regulator that is enabled during the start-up sequence. Note that setting the LDO*n*_ENSLOT fields in software is only relevant to the Development Mode, as these fields are assigned preset values in each of the Custom Modes.

Each Regulator may be programmed to switch off in a selected timeslot within the shutdown sequence. If a Regulator is not allocated to one of the 14 shutdown timeslots, it will be disabled when the WM8351 enters the OFF state.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 (0Dh) or R176 (B0h) DC-DC / LDO requested	8	LDO1_ENA	0	LDO1 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.
	9	LDO2_ENA	0	LDO2 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.
	10	LDO3_ENA	0	LDO3 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.
	11	LDO4_ENA	0	LDO4 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.
Note: These bits can be accessed through R13 or through R176. Reading from or writing to either register location has the same effect.				
R201 (C9h) for LDO1 R204 (CCh) for LDO2	13:10	LDO*n*_ENSLOT [3:0]	0000	Time slot for LDO*n* start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				1111 = Start up on entering ACTIVE
R207 (CFh) for LDO3 R210 (D2h) for LDO4	9:6	LDO*n*_SDSLOT [3:0]	0000	Time slot for LDO*n* shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF
Note: *n* is a number between 1 and 4 that identifies the individual LDO regulator				

Table 82 Enabling and Disabling the LDO Regulators

14.7.2 LDO REGULATOR CONTROL

The LDO Regulators can be configured to operate in different modes using the register bits described in Table 83.

In Switch mode, the Regulators operate as current-limited switches with no voltage regulation.

In LDO Regulator mode, the Regulators generate an output voltage determined by the LDO*n*_VSEL fields. The LDO Regulators are dynamically programmable - the output voltage may be adjusted in software at any time. The Regulators are critically damped to ensure there is no voltage overshoot or undershoot when adjusting the output voltage.

The default output voltage for the LDO Regulators is set by writing to the LDO*n*_VSEL register bits. The 'image' voltage settings LDO*n*_VIMG are alternate values that may be invoked when the HIBERNATE software or hardware control is asserted.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R200 (C8h) for LDO1 R203 (CBh) for LDO2	14	LDO*n*_SWI	0	LDO*n* Regulator mode 0 = LDO voltage regulator 1 = Current-limited switch (no voltage regulation, LDO*n*_VSEL has no effect)
R206 (CEh) for LDO3 R209 (D1h) for LDO4	4:0	LDO*n*_VSEL [4:0]	Dependant on CONFIG[1:0] settings	LDO*n* Regulator output voltage (when LDO*n*_SWI=0) 1 1111 = 3.3V … (100mV steps) 1 0000 = 1.8V 0 1111 = 1.65V … (50mV steps) 0 0000 = 0.9V
R202 (CAh) for LDO1 R205 (CDh) for LDO2 R208 (D0h) for LDO3 R211 (D3h) for LDO4	4:0	LDO*n*_VIMG [4:0]	1 1100	LDO*n* Regulator output image voltage 1 1111 = 3.3V … (100mV steps) 1 0000 = 1.8V 0 1111 = 1.65V … (50mV steps) 0 0000 = 0.9V
Note: *n* is a number between 1 and 4 that identifies the individual LDO regulator				

Table 83 Controlling Regulator Voltage and Switch Mode

The LDO Regulators can also be controlled by the device HIBERNATE bit, or by hardware input signals L_PWR1, L_PWR2 and L_PWR3. Several GPIO pins can be assigned as L_PWR pins. Each Regulator can be assigned to one of these three signals, or else to the device HIBERNATE bit. The signals are active high and each Regulator's response to the selected signal is programmable as defined in Table 84.

Note that, when a GPIO pin is configured as a Hibernate input pin, and this input is asserted, then all LDO Regulators will be placed in Hibernate mode.

In order to use GPIO pins as L_PWR pins, they must be configured by setting the respective GP*n*_FN, and GP*n*_DIR bits to the appropriate value (see Section 20).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Note: *n* is a number between 1 and 4 that identifies the individual LDO regulator				
R202 (CAh) for LDO1 R205 (CDh) for LDO2	13:12	LDO*n*_HIB_MODE [1:0]	00	LDO Hibernate behaviour: 00 = Select voltage image settings 01 = disable output 10 = reserved 11 = reserved
 R208 (D0h) for LDO3 R211 (D3h) for LDO4	9:8	LDO*n*_HIB_TRIG [1:0]	00	LDO Hibernate signal select 00 = Hibernate register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3

Table 84 Configuring Hardware Control for LDO Regulators

When the LDO Regulators are disabled, the output can be set to float or else the outputs can be actively discharged through internal resistors. This feature is controlled using the register bits described in Table 85.

Note that the "float" option is only supported when at least one other LDO Regulator remains enabled. If LDO Regulators 1, 2, 3 and 4 are all disabled, then the LDO Regulator outputs will be discharged, regardless of the LDO*n*_OPFLT registers.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R200 (C8h) for LDO1 R203 (CBh) for LDO2 R206 (CEh) for LDO3 R209 (D1h) for LDO4	10	LDO*n*_OPFLT	0	Enable discharge of LDOn outputs when LDO*n* disabled 0 = Enabled - Output to be discharged 1 = Disabled - Output is left floating Note - if LDO Regulators 1, 2, 3 and 4 are all disabled, then the outputs will all be discharged, regardless of the LDO*n*_OPFLT bit.
Note: *n* is a number between 1 and 4 that identifies the individual LDO regulator				

Table 85 Output Float Control for LDO Regulators

14.7.3 INTERRUPTS AND FAULT PROTECTION

Each LDO Regulator is monitored for voltage accuracy and fault conditions. An undervoltage condition is set if the voltage falls below 95% of the required level. The action taken in response to a fault condition can be set independently for each LDO Regulator, as described in Table 86. The LDO*n*_ERRACT fields configure the fault response to disable the respective regulator or to shut down the entire system if desired. In addition, LDO Regulator fault conditions also generate a second-level interrupt (see Section 24).

To prevent false alarms during short current surges, faults are only signalled if the fault condition persists.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R201 (C9h) for LDO1 R204 (CCh) for LDO2 R207 (CFh) for LDO3 R210 (D2h) for LDO4	15:14	LDO*n*_ERRACT [1:0]	00	Action to take on fault (as well as generating an interrupt): 00 = ignore 01 = shut down regulator 10 = shut down system 11 = reserved (shut down system)
Note: *n* is a number between 1 and 4 that identifies the individual LDO regulator				

Table 86 Fault Responses for LDO Regulators

The DC-DC Converters and the LDO Regulators have a first-level interrupt, UV_INT (see Section 24). This comprises second-level interrupts from each of the DC-DC Converters and the LDO Regulators.

Each LDO Regulator has a dedicated second-level interrupt which indicates an under-voltage condition. These can be masked by setting the applicable mask bit as defined in Table 87.

ADDRESS	BIT	LABEL	DESCRIPTION
R28 (1Ch) Under Voltage Interrupt Status	11	UV_LDO4_EINT	LDO4 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	10	UV_LDO3_EINT	LDO3 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	9	UV_LDO2_EINT	LDO2 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	8	UV_LDO1_EINT	LDO1 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R36 (24h) Under Voltage Interrupt Mask	as in R28	"IM_" + name of respective bit in R28	Mask bits for LDO regulator under-voltage interrupts Each of these bits masks the respective bit in R28 when it is set to 1 (e.g. UV_LDO1_EINT in R28 does not trigger a UV_INT interrupt when IM_UV_LDO1_EINT in R36 is set).

Table 87 LDO Regulator Interrupts

The status of the LDO Regulators can be indicated and monitored externally via a GPIO pin configured as /VCC_FAULT (see Section 20). When a GPIO pin is configured as /VCC_FAULT output, a logic low level on this pin indicates that there is a fault condition on one of the LDO Regulators, DC-DC Converters, or the Current Limit switch.

The /VCC_FAULT output is configurable by the control fields in Register R215. The fields described in Table 88 determine which of the LDOs contribute to the /VCC_FAULT indication. An undervoltage or overvoltage condition on any unmasked LDO will cause the /VCC_FAULT output to be set to logic low.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R215 (D7h) VCC_FAULT	11	LDO4_FAULT	0	LDO4 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault
	10	LDO3_FAULT	0	LDO3 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault
	9	LDO2_FAULT	0	LDO2 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault
	8	LDO1_FAULT	0	LDO1 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault

Table 88 LDO Regulator /VCCFAULT mask bits

14.7.4 ADDITIONAL CONTROL FOR LDO1

By default, all DC Converters and LDOs are disabled in the OFF state. Additional control is provided to enable LDO1 to be configured differently, allowing it to be enabled in the OFF state, or else to be controlled by a GPIO pin configured as /LDO_ENA (see Section 20.2.2). These options are selected by setting the register fields described in Table 89. In practical applications, however, these options are set by the Config Mode settings and are not set by users.

Operation of LDO1 in the OFF state is subject to the restriction that VOUT1 must be set to at least 1.8V.

CONDITION	DESCRIPTION
LDO1_PIN_MODE = 0	LDO1 controlled as normal via register bits
LDO1_PIN_MODE = 1 LDO1_PIN_EN = 0	LDO1 enabled at all times
LDO1_PIN_MODE = 1 LDO1_PIN_EN = 1	LDO1 controlled by /LDO_ENA only

Table 89 LDO1 Additional Control

Notes:

1. LDO1 is always disabled in BACKUP and ZERO states.

2. When LDO1_PIN_MODE = 1, then LDO1 only operates as determined by the LDO1_VSEL field. The Hibernate settings are ignored under this configuration.

14.8 DC-DC CONVERTER OPERATION

14.8.1 OVERVIEW

The WM8351 provides four DC-DC switching converters. Three of these are Buck (Step-down) converters and one is a Boost (Step-up) converter. The principal characteristics and typical usage for each DC-DC converter are shown below.

	DC-DC 1	DC-DC 2	DC-DC 3 / 4
Typical Application	Other system components	Constant-current LED drivers or I/O supply	Digital supply for WM8351 and other components
Converter Type	Step-down	Step-up, using external NFET	Step-down
Input Voltage Range	2.7V to 5.5V		
Output Voltage Range	0.85V to 3.4V	5V to 20V	0.85V to 3.4V
Load Current Rating	Up to 1A (may be limited by application)	170mA @ 5V 40mA @ 20V	Up to 500mA (may be limited by application)
Switching Frequency	2.0MHz	1.0MHz	2.0MHz

Table 90 DC-DC Converter Characteristics

14.8.2 DC-DC STEP DOWN CONVERTERS

DC-DC Converters 1, 3 and 4 are versatile step-down, pulse-width-modulated (PWM) DC-DC converters designed to deliver high power efficiency across full load conditions. The converters offer Active and Standby/Hysteretic operating modes in order to maximise efficiency for different loads. A low-power LDO sleep mode is also available to further reduce quiescent current at very lightly loaded conditions. The DC-DC Converters maintain output voltage regulation during the switch-over between operating modes.

The step-down regulators are designed with fixed frequency current mode architecture. The current feedback loop is through the PMOS current path and is amplified and summed with an internal slope compensation network. The voltage feedback loop is through an internal feedback divider. The ON time is determined by comparing the summed current feedback and the output of the switcher error amplifier. The period is set by the internal RC oscillator, which provides a 2.0MHz clock.

A supply pin (PVDD) provides the core supply for DC-DC Converter 3. Another supply pin (LINEDCDC) provides the core supply for DC-DC Converters 1 and 4. The input voltage connection to DC-DC Converters 1, 3 and 4 is provided on PV1, PV3 and PV4 respectively. These input voltages may be provided from the LINE voltage.

The connections to DC-DC Converter 1 are illustrated in Figure 69. The equivalent circuit applies to DC-DC Converters 3 and 4 also.

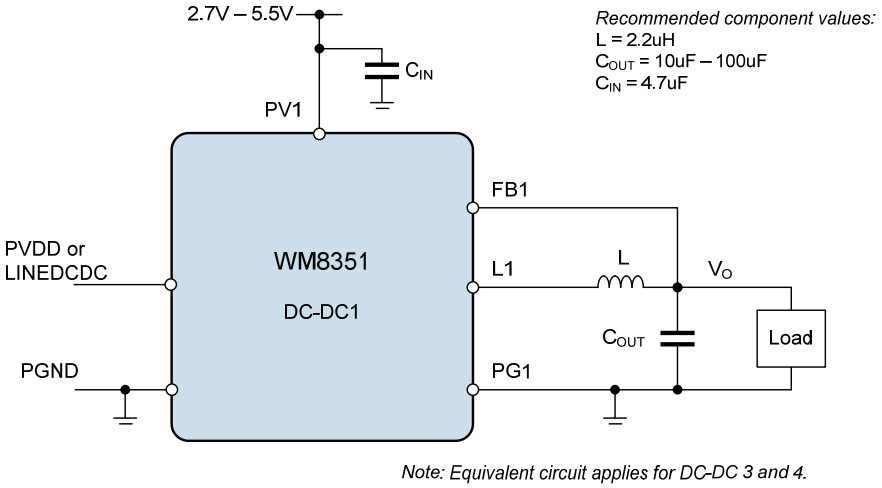


Figure 69 Step-Down DC-DC Converter Connections

The external components at the converter output are required by the DC-DC Converter integral loop compensation circuit. Note that the recommended output capacitor Cout varies according to the required transient response on DC-DC1. A single recommended value is provided for Cout on DC-DC3 and DC-DC4.

See Section 29.3 for details of the recommended external components.

14.8.3 DC-DC STEP UP CONVERTER

DC-DC Converter 2 is a versatile step-up pulse-width-modulated (PWM) DC-DC converter designed to deliver high power efficiency across full load conditions. The converter can also be used as a switch.

DC-DC Converter 2 is designed with a fixed frequency current mode architecture. The clock frequency is set by the internal RC oscillator, which provides a 1.0MHz clock.

The PVDD supply pin provides the core supply for DC-DC Converter 2.

The connections to DC-DC Converter 2 in Constant Voltage Mode are illustrated in Figure 70. See Section 29.4 for details of the connections for the Constant Current and USB operating modes of the DC-DC Step-Up Converter.

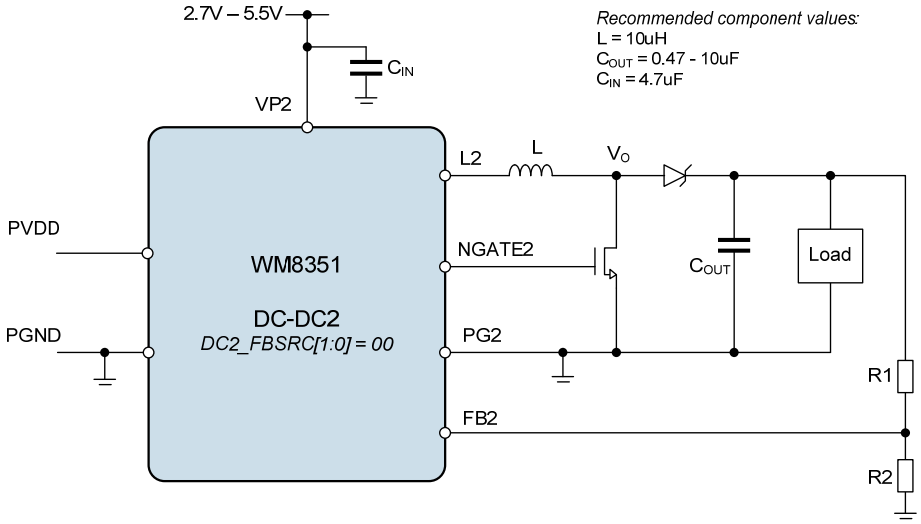


Figure 70 Step-Up DC-DC Converter Connections

The external components at the converter output are required by the DC-DC Converter integral loop compensation circuit. Note that the recommended output capacitor Cout varies according to the required output voltage.

See Section 29.4 for details of the recommended external components.

14.9 LDO REGULATOR OPERATION

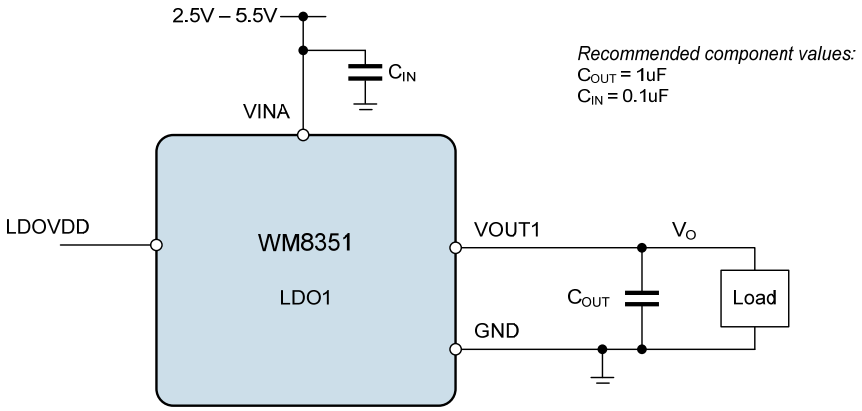
The WM8351 provides four identical LDO voltage regulators to generate accurate, low-noise supply voltages for various system components. The LDOs can also operate as current-limited switches, with no voltage regulation; this is useful for 'Hot Swap' outputs, i.e. supply rails for external devices that are plugged in when the system is already powered up - the current-limiting function prevents the in-rush current into the external device from disturbing other system power supplies.

The LDO regulators are dynamically programmable. Each regulator output is current-limited; the output voltage is automatically throttled back if the load current exceeds the limit.

A single supply pin (LDOVDD) provides the core supply for all four LDOs. The input voltage connection to LDO1 and LDO2 is provided on the VINA pin. The input voltage connection to LDO3 and LDO4 is provided on the VINB pin. These input voltages can be provided from one of the DC-DC Converters or from the LINE voltage.

Note that separate voltage regulators are provided to generate the backup supply VRTC and the microphone bias voltage MICBIAS.

The connections to LDO Regulator 1 are illustrated in Figure 71. The equivalent circuit applies to LDO2, LDO3 and LDO4.



Note: Equivalent circuit applies for LDO2, LDO3 and LDO4.
Input pin VINA supplies LDO1 and LDO2; Input pin VINB supplies LDO3 and LDO4.

Figure 71 LDO Regulator Connections

An input and output capacitor are recommended for each LDO Regulator, as illustrated above. See Section 29.5 for details of the recommended external components.

15 CURRENT LIMIT SWITCH

15.1 GENERAL DESCRIPTION

The WM8351 includes an on-chip Current Limit Switch to control external devices and to support hot-plugging of accessories and power supplies.

When the switch is enabled, it normally has a low resistance, allowing current to pass through (from the IP pin to the OP pin). If the current limit threshold is reached, the WM8351 can raise an interrupt, disable the switch and/or shut down the whole device.

15.2 CONFIGURING THE CURRENT LIMIT SWITCH

15.2.1 CURRENT LIMIT SWITCH ENABLE

The Current Limit Switch can be enabled in software using the register fields defined in Table 91.

In Active mode, the Current Limit Switch can be enabled in software using the LS_ENA bit. Setting this bit whilst in the Pre-Active state (see Figure 65) will not immediately enable the Current Limit Switch; this bit will only become effective once the WM8351 has reached the Active state.

The Current Limit Switch may be programmed to become enabled in a selected timeslot within the start-up sequence. When this happens, the WM8351 will set the LS_ENA bit. Note that setting the LS_ENSLOT field in software is only relevant to the Development Mode, as this field is assigned a preset value in each of the Custom Modes.

The Current Limit Switch may be programmed to switch off in a selected timeslot within the shutdown sequence. If the Limit Switch is not allocated to one of the 14 shutdown timeslots, it will be disabled when the WM8351 enters the OFF state.

The Current Limit Switch behaviour in Hibernate mode is controlled by the LS_HIB_MODE bit.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 (0Dh)	15	LS_ENA	0	Limit switch enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.
R176 (B0h) DC-DC / LDO requested	15			
Note: LS_ENA can be accessed through R13 or through R176. Reading from or writing to either register location has the same effect.				
R199 (C7h) Limit switch control	13:10	LS_ENSLOT [3:0]	0000	Time slot for Limit Switch start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start-up on entering ACTIVE
	9:6	LS_SDSLOT [3:0]	0000	Time slot for Limit Switch shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF
	4	LS_HIB_MODE	0	Limit switch hibernate mode setting 0 = disabled 1 = leave setting as in Active mode

Table 91 Enabling and Disabling the Current Limit Switch

15.2.2 CURRENT LIMIT SWITCH BULK DETECTION CONTROL

The Current Limit Switch can be connected to voltages which may be higher than the device LINE voltage. To support this capability, the switch is powered from the highest available voltage; this requires a bulk detection circuit in order to select the highest available voltage. The bulk detection circuit is always enabled whenever the Current Limit Switch is enabled.

It is possible to control whether the bulk detection circuit is enabled or not when the Current Limit Switch is disabled. This is controlled in Active mode by the LS_PROT bit, and in Hibernate mode by the LS_HIB_PROT bit.

Disabling the Bulk Detection circuit will reduce power consumption. It is important to note, however, that the Bulk Detection circuit should always be enabled if voltages greater than LINE could be present on IP or OP. This applies regardless of whether the Current Switch is open or closed.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R199 (C7h) Limit switch control	1	LS_HIB_PROT	1	Controls the bulk detection circuit when Limit Switch is disabled in Hibernate mode. 0 = bulk detection disabled 1 = bulk detection enabled
	0	LS_PROT	1	Controls the bulk detection circuit when Limit Switch is disabled in Active mode. 0 = bulk detection disabled 1 = bulk detection enabled

Table 92 Current Limit Switch Bulk Detection Control

15.2.3 INTERRUPTS AND FAULT PROTECTION

The response to an over-current condition is selectable. To prevent false alarms during short current surges, faults are only signalled if the fault condition persists.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R199 (C7h) Limit switch control	15:14	LS_ERRACT [1:0]	00	Current limit detection behaviour 00 = ignore 01 = disable switch 10 = shut down system 11 = shut down system

Table 93 Fault Response for the Current Limit Switch

The limit switch has its own first-level interrupt, OC_INT (see Section 24). This contains a single second-level interrupt, OC_LS_EINT, indicating an over-current condition. OC_LS_EINT can be masked by setting the IM_OC_LS_EINT bit.

ADDRESS	BIT	LABEL	DESCRIPTION
R29 (1Dh) Over Current Interrupt Status	15	OC_LS_EINT	Limit Switch Over-current interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R37 (25h) Over Current Interrupt Mask	15	IM_OC_LS_EINT	Mask bit for Limit switch over-current interrupt When set to 1, IM_OC_LS_EINT masks OC_LS_EINT in R29 and does not trigger an OC_INT interrupt when OC_LS_EINT is set).

Table 94 Current Limit Switch Interrupts

The status of the Current Limit Switch can be indicated and monitored externally via a GPIO pin configured as /VCC_FAULT (see Section 20). When a GPIO pin is configured as /VCC_FAULT output, a logic low level on this pin indicates that there is a fault condition on one of the LDO Regulators, DC-DC Converters, or the Current Limit switch.

The /VCC_FAULT output is configurable by the control fields in Register R215. The LS_FAULT bit described in Table 95 selects whether the Limit Switch contributes to the /VCC_FAULT indication. When LS_FAULT = 0, then an overcurrent condition on the Limit Switch will cause the /VCC_FAULT output to be set to logic low.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R215 (D7h) VCC_FAULT	15	LS_FAULT	0	Limit Switch fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault

Table 95 Limit Switch /VCCFAULT Mask

16 CURRENT SINKS (LED DRIVERS)

16.1 GENERAL DESCRIPTION

The WM8351 includes four pins for driving different types of LEDs.

The ISINKA pin provides a programmable constant-current sink designed to drive a string of serially connected LEDs, including white LEDs used in display backlights or in camera flash applications. Using ISINKA in conjunction with DC-DC Converter 2 provides a particularly power-efficient way to drive such LED strings. The ground connection associated with this Current Sink is the SINKGND pin.

ISINKC, ISINKD and ISINKE are regular open-drain outputs. They are alternate functions of the GPIO10, GPIO11 and GPIO12 pins respectively. These GPIOs are provided on the LINE power domain; the associated ground connection is the GND pin.

16.2 CONSTANT-CURRENT SINK

ISINKA is a dedicated LED driver pin equipped with a programmable constant current sink. It is designed to drive a string of serially connected white LEDs such as those used in display backlights or photo-flash applications. Powering LEDs in this way is particularly power efficient because no series resistor is required. DC-DC converter 2, operating as a current-controlled voltage source, is an ideal power source for LED strings. This converter can generate voltages higher than BATT or LINE, which can overcome the combined forward voltages of long LED strings (e.g. a string of 7 white LEDs with a forward voltage of 4V requires at least 28V).

16.2.1 ENABLING THE SINK CURRENT

In Active mode, ISINKA can be enabled in software using the CS1_ENA register field defined in Table 96. If required, the Current Sink function may also be controlled by the Hibernate bit.

Note that these control bits do not exist for ISINKC, ISINKD or ISINKE.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 (0Eh) Power mgmt (7)	0	CS1_ENA	0	Current Sink 1 enable (ISINKA pin) 0 = disabled 1 = enabled
R172 (ACh)	15			
Current Sink Driver A	12	CS1_HIB_MODE	0	Current Sink 1 behaviour in Hibernate mode 0 = disable current sink in Hibernate 1 = leave current sink as in Active
Note: CS1_ENA can be accessed through R14 or through R172. Reading from or writing to either register location has the same effect.				

Table 96 Enabling ISINKA

When ISINKA is used in conjunction with DC-DC Converter 2, the ISINK should always be switched on before the DC-DC Converter is switched on. Conversely, the DC-DC Converter should always be switched off before the ISINK is switched off. If high voltages are used, additional external components may also be needed to protect the WM8351.

16.2.2 PROGRAMMING THE SINK CURRENT

The sink current for ISINKA can be programmed by writing to the CS1_ISEL register bit. The current steps are logarithmic to match the logarithmic light sensitivity characteristic of the human eye. The step size is 1.5dB (i.e. the current doubles every four steps).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R172 (ACh) Current Sink Driver A	5:0	CS1_ISEL	00 0000	ISINKA current = 4.05µA × $2^{CS1\_ISEL/4}$ where CS1_ISEL is an unsigned binary number Minimum: 00 0000 = 4.05µA, Maximum: 11 1111 = 220mA (from circuit simulation) or CS1_ISEL = 13.3 × log (desired current / 4.05µA)

Table 97 Controlling the Sink Current for ISINKA

Note that currents above 40mA are not supported continuously; these settings are intended for flash mode only.

16.2.3 FLASH MODE

The current sink can either sink current continuously (LED mode) or in short bursts (flash mode). The operating mode is selected by the CS1_FLASH_MODE bit, as described in Table 98.

In LED mode, the current sink is controlled by setting CS1_DRIVE. For as long as this bit is asserted, the LED is enabled continuously.

In Flash mode, the current sink may be set to automatically flash every 4 seconds by setting CS1_FLASH_RATE = 1, or may be triggered normally by setting CS1_FLASH_RATE = 0.

When normal triggering is selected in Flash mode, the trigger control can be either a GPIO Flash input (see Section 20) or a register control. Setting CS1_TRIGSRC = 1 selects GPIO as the trigger. The flash will be edge triggered by the selected GPIO input. Setting CS1_TRIGSRC = 0 selects the register field CS1_DRIVE as the trigger. In this case, writing a 1 to CS1_DRIVE will trigger a flash; this bit will be reset at the end of the flash.

In all flash modes, the duration of each flash is set by CS1_FLASH_DUR. The status of each current sink may be read from the CS1_DRIVE bit.

In all modes, the current sink must also be enabled via the applicable CS1_ENA bit (see Table 96).

Note that some photo-flash applications may require a reservoir capacitor to store sufficient charge for the flash.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R173 (ADh) CSA Flash Control	15	CS1_FLASH_MODE	0	Determines the function of the current sink 0 = LED mode 1 = Flash mode
	14	CS1_TRIGSRC	0	Selects the trigger in Flash mode. 0 = Flash triggered by CS1_DRIVE bit 1 = Flash triggered from GPIO pin configured as FLASH This bit has no effect when CS1_FLASH_MODE=0
	13	CS1_DRIVE	0	Enables the current sink ISINKA LED mode- 0 = disable LED 1 = enabled LED FLASH mode- Register bit used to trigger the flash, if CS1_TRIGSRC is set to 0. Flash is started when the bit goes high, it is then reset at the end of the flash duration. Duration is determined by CS1_FLASH_DUR. This bit has no effect if CS1_TRIGSRC is set to 1.
	12	CS1_FLASH_RATE	0	Determines the Flash rate 0 = Normal Operation. Once per trigger (Either register bit or GPIO) 1 = Flash will be internally triggered every 4 second
	9:8	CS1_FLASH_DUR [1:0]	00	Sets duration of flash 00 = 32ms 01 = 64ms 10 = 96ms 11 = 1024ms

Table 98 Configuring Flash Mode for ISINKA

16.2.4 ON/OFF RAMP TIMING

The sink current for ISINKA can be programmed to switch on and off gradually in LED and in Flash modes. The current ramp duration is as described in Table 99.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
R173 (ADh) CSA Flash Contro	5:4	CS1_OFF_RAMP [1:0]	00	Switch-off ramp duration	
				LED Mode	Flash Mode
				00 = instant (no ramp) 01 = 0.25s 10 = 0.5s 11 = 1s	00 = instant (no ramp) 01 = 1.95ms 10 = 3.91ms 11 = 7.8ms
	1:0	CS1_ON_RAMP [1:0]	00	Switch-on ramp duration Similar to CS1_OFF_RAMP	

Table 99 Configuring On/Off Ramp Timing for ISINKA

16.2.5 INTERRUPTS AND FAULT PROTECTION

The Current Sink has its own first-level interrupt, CS_INT (see Section 24). This contains a single second-level interrupt, CS1_EINT, indicating that the Current Sink is unable to sink the amount of current that has been programmed and may be out of spec. CS1_EINT can be masked by setting the IM_CS1_EINT bit.

ADDRESS	BIT	LABEL	DESCRIPTION
R26 (1Ah) Interrupt Status 2	13	CS1_EINT	Flag to indicate drain voltage can no longer be regulated and output current may be out of spec. (Rising Edge triggered) Note: This bit is cleared once read.
R34 (22h) Interrupt Status 2 Mask	13	IM_CS1_EINT	Mask bit for Current Sink over-current interrupt When set to 1, IM_CS1_EINT masks CS1_EINT in R26 and does not trigger a CS_INT interrupt when CS1_EINT is set.

Table 100 Current Sink Interrupts

16.3 OPEN-DRAIN LED OUTPUTS

The three open-drain outputs ISINKC, ISINKD and ISINKE are alternate functions of the GPIO10, GPIO11 and GPIO12 pins, respectively (see Section 20). They can drive LEDs connected to LINE, with a series resistor. Note that the GPIO pins have other alternate functions, which will not be available that pin is configured as ISINKC, ISINKD or ISINKE.

16.4 LED DRIVER CONNECTIONS

The recommended connection for LEDs on ISINKA is illustrated in Figure 72.

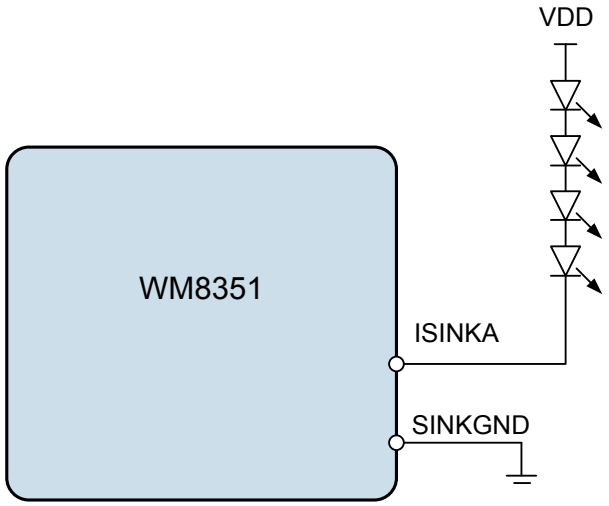


Figure 72 LED Connection to ISINKA

The recommended connections for LEDs on ISINKC, ISINKD and ISINKE are illustrated in Figure 73.

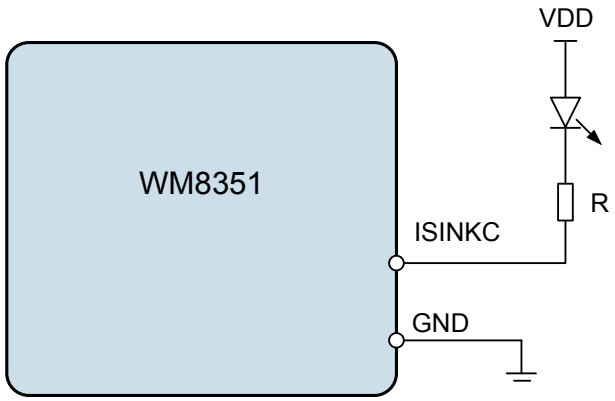


Figure 73 LED Connections to ISINKC, ISINKD and ISINKE

17 POWER SUPPLY CONTROL

17.1 GENERAL DESCRIPTION

The WM8351 can take its power supply from a Wall adaptor, a USB interface or from a single-cell lithium battery. The WM8351 autonomously chooses the most appropriate power source available, and supports hot-swapping between sources (ie. the system can remain in operation while different sources are connected and disconnected).

Comparators within the WM8351 identify which power supplies are available and select the power source in the following order of preference:

- Wall adaptor (LINE pins)
- USB power rail (USB pins)
- Battery (BATT pins)

Note that the Wall supply is always the first choice of supply, (providing that it is within required limits), even if the Wall supply voltage is lower than the USB voltage.

When Wall or USB is selected as the power source, this may be used to charge the Battery, using the integrated battery charger circuit. For battery charging to occur, the USB or LINE supply voltage must be no less than 4.0V.

Figure 74 illustrates the WM8351 connections associated with the WALL, USB and Battery supplies.

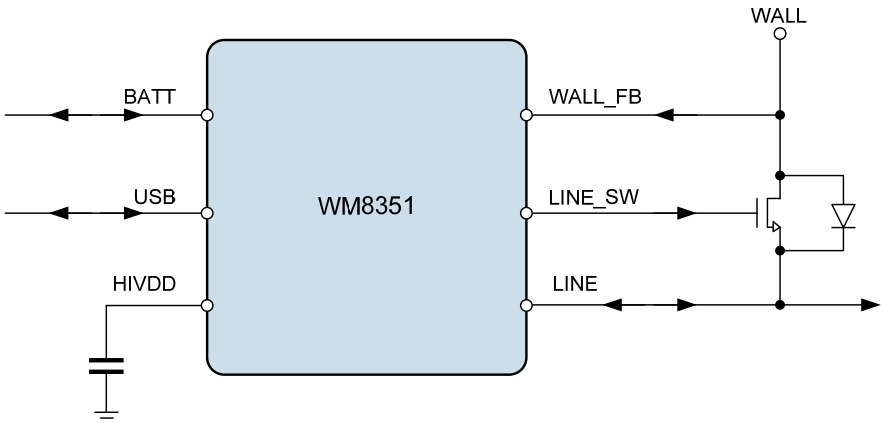


Figure 74 WM8351 Power Supply Connections

The Wall Adaptor supply connects to LINE via a FET switch as illustrated in Figure 74. The FET switch is necessary in order to provide isolation between the Wall supply and the Battery/USB supplies; this is vital in the event of the USB voltage being greater than the Wall supply voltage.

The Wall Adapter voltage is sensed directly on the WALL_FB pin; this allows the WM8351 to determine the preferred supply, including when the FET is switched off.

The gate connection to the external FET is controlled by LINE_SW, which is an alternate function that can be enabled on GPIO12 (see Section 20). Note that, if the USB connection is not used, then the FET may not be required and the Wall supply may be connected directly to LINE.

LINE is primarily an output from the WM8351; this output is the preferred supply, where the WM8351 has arbitrated between the Wall, Battery and USB connections. This output is suitable for supplying power to the other blocks of the WM8351, including the DC-DC Converters and LDO Regulators. LINE is also an input under some conditions, such as battery charging from Wall or providing power at the USB connection.

HIVDD is an external connection which exists for the purposes of decoupling only. It represents the highest available power supply connected to the WM8351. It should be noted that the preferred supply (on the LINE pin) is not necessarily the same voltage as HIVDD - the Wall supply will always be the preferred voltage when it is within the intended limits, even if it is not also the highest available source.

The main battery connects directly to the BATT pin. When the battery is the preferred supply source, this pin is an input. When battery charging is in operation, this pin is an output. (Note that the backup VRTC battery is connected separately - see Section 17.5.)

The USB interface connects directly to the USB pin. In USB Master Mode (USB is less than LINE), the WM8351 can supply power to external devices on this pin. In USB Slave Mode (USB is greater than LINE), the WM8351 can use this pin as an input to power the device and/or to charge a battery connected to the BATT pin. Note that, when USB is the preferred power supply, the Battery may also be used if necessary to supplement the current drawn from the USB pin (ie. to source current into LINE when required).

All loads connected to the WM8351 should normally be connected to the LINE pin. The inputs to the DC-DC Converters and LDOs should be connected to the LINE pin. It is not recommended to connect any load directly to the battery (BATT).

Note that the inputs to the LDOs may be connected to the outputs of the DC-DCs if desired.

17.2 BATTERY POWERED OPERATION

The WM8351 selects battery power when the Battery voltage is higher than the Wall (LINE) and USB supplies. In practical usage, this means the Battery is used when Wall (LINE) and USB are both disconnected.

The battery can also be used to supplement the USB supply when required (ie. to source current into LINE).

If the Wall (LINE) or USB supply becomes available during battery operation, then the selected power source is adjusted accordingly.

Battery pack temperature sensing is enabled by default. The battery's NTC resistor is monitored via the AUX1 pin on the WM8351, as described in Section 17.7. Note that the absence of this NTC connection will lead to a temperature failure condition being detected and battery charging will not be possible.

Safe operation of the battery charger outside the designed operating temperatures is not guaranteed when a battery NTC resistor is not used. The designed operating temperatures are noted in Section 17.7.7.

17.3 WALL ADAPTOR (LINE) POWERED OPERATION

The WM8351 selects Wall Adaptor power via the LINE pins whenever the Wall Adaptor supply is within the normal operating limits of 4.0V to 5.5V. The Wall Adaptor is also selected as the power source below 4.0V in the case where it is the highest available power source. The minimum LINE voltage is a programmable threshold in the range 2.9V to 3.6V (see Section 18). The maximum recommended operating voltage for LINE is 5.5V.

Note that USB power is not used when a suitable LINE supply is available, even if the USB supply is higher than the Wall (LINE) supply.

If the Wall (LINE) supply becomes unsuitable and a USB is available, then the USB supply will be selected as the preferred power source. Note that, when hot-swapping from Wall (LINE) to USB supply, a usable Battery must be present on the BATT pin.

When the Wall (LINE) supply is selected and a Battery is connected, then trickle charging is enabled by default, including when the WM8351 is in the OFF or HIBERNATE states. When the WM8351 is in the ACTIVE state, then fast charging may be selected under software control.

17.4 USB POWERED OPERATION

The WM8351 selects USB Slave mode by default. In USB Slave Mode, the USB pin can be used as one of the sources of power for the WM8351. In USB Master Mode (selected using the USB_MSTR register bit) the WM8351 can provide power to an external USB device.

In USB Slave mode, the WM8351 selects USB power if the Wall (LINE) supply is outside its normal operating limits and the USB supply is the highest supply source available. For a transition from OFF to ACTIVE state to occur under USB power, the USB supply must be no less than 4.0V.

The maximum current drawn from the USB supply can be set to 100mA (USB low power mode) or 500mA (USB high power mode). The default is set according to the selected Config Mode (see Section 14).

When the WM8351 is in the ACTIVE state, USB high power mode can be selected using the register bits USB_MSTR_500MA (in USB Master Mode) or USB_SLV_500MA (in USB Slave Mode) as defined in Table 101. If a USB current higher than the applicable threshold is demanded, then internal protection circuits will limit the USB current, and the USB_LIMIT_EINT interrupt will be asserted.

Short term currents higher than 500mA can also be supported. This may be necessary for supporting transient demands (eg. for a hard drive starting up). When the USB_NOLIM register field is set, the internal protection circuits are disabled, and the current limit interrupt threshold is raised to double the normal value. In 500mA mode, the current limit interrupt threshold is raised to approximately 1A. This feature must be used with caution, as the internal protection circuits are disabled when USB_NOLIM is set. The maximum steady-state current supported is 500mA; higher currents can only be supported for short term transients.

USB power may be supplemented by battery power if available and if necessary to maintain the USB current within the applicable limit. If a suitable Wall (LINE) supply becomes available during USB operation, then this will be selected as the preferred power source. Note that, when hot-swapping from USB to Wall supply, a usable Battery must be present on the BATT pin.

In USB low power mode, trickle charging is enabled by default. Trickle charging is suspended if necessary to keep within the 100mA USB limit.

In USB high power mode, fast charging is possible (subject to other conditions - see Section 17.7.4). The fast charge current is controlled dynamically as necessary to keep the overall USB current within the 500mA limit.

Note that Battery Charging from the USB source is only possible in USB Slave Mode.

USB power may be suspended by writing to the USB_SUSPEND register bit. Setting this bit to ‘1’ disconnects the WM8351 from the USB supply, resulting in the selection of Battery as the power source. USB Suspend mode is invoked under software control, by writing to the USB_SUSPEND bit. Suspend mode should be invoked whenever the USB connection is not used.

To comply with the USB 2.0 specification, the host processor should initially invoke USB Suspend mode after the WM8351 has successfully started up, and whenever the USB connection is not in use. If the USB connection is active and USB enumeration has been completed, the host processor may (but is not required to) switch the WM8351 into USB low-power mode or USB high-power mode. However, if wall adaptor power is available, it is recommended to remain in USB Suspend mode.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) System Control 2	14	USB_SUSPEND	0	Opens the USB switch 0 = USB enabled 1 = USB suspended The register bit defaults to 0, when a reset happens or LINE < UVLO or the system fail on boot due to the upper limit of the Hysteresis Comp not been met.
	13	USB_MSTR	0	Set the chip to be a USB master 0 = Slave 1 = Master The register bit defaults to 0, when a reset happens or the USB state machine moves from MASTER mode to SLAVE mode.
	11	USB_MSTR_500MA	0	Set 500mA or 100mA mode when the USB switch is in master mode 0 = 100mA 1 = 500mA
	9	USB_SLV_500MA	Dependant on CONFIG settings	Set 500mA or 100mA mode when the USB switch is in slave mode 0 = 100mA 1 = 500mA The register bit defaults to 0, when a reset happens or LINE<UVLO or the system fail on boot due to the upper limit of the Hysteresis Comp not been met.

Table 101 Selecting USB Power Modes

The USB connection has its own first-level interrupt, USB_INT (see Section 24). This contains a single second-level interrupt, USB_LIMIT_EINT, which indicates an over-current condition. USB_LIMIT_EINT can be masked by setting the IM_USB_LIMIT_EINT bit.

USB Current monitoring is effective in USB Master and USB Slave Modes. The current limit threshold is determined by USB_MSTR_500MA (in USB Master Mode) or USB_SLV_500MA (in USB Slave Mode).

ADDRESS	BIT	LABEL	DESCRIPTION
R26 (1Ah) Interrupt Status 2	10	USB_LIMIT_EINT	USB Limit Switch interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R34 (22h) Interrupt Status 2 Mask	10	IM_USB_LIMIT_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. When IM_USB_LIMIT_EINT is set to 1, then USB_LIMIT_EINT in R26 does not trigger an USB_INT interrupt when set. The default value is 0 (unmasked).

Table 102 USB Interrupt

17.5 EXTERNAL INTERRUPTS

The power supply control circuit has a first-level interrupt, EXT_INT (see Section 24). This comprises three second-level interrupts which indicate if the USB, Wall or Battery supplies have been connected or disconnected. Internal feedback signals USB_FB, WALL_FB and BATT_FB are used to indicate when the associated supplies are present. Note that these interrupt events occur on both the rising and falling edges of the trigger events. They can be masked by setting the applicable mask bits as defined in Table 103.

ADDRESS	BIT	LABEL	DESCRIPTION
R31 (1Fh) Comparator Interrupt Status	15	EXT_USB_FB_EINT	USB_FB changed interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
	14	EXT_WALL_FB_EINT	WALL_FB changed interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
	13	EXT_BATT_FB_EINT	BATT_FB changed interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
R39 (27h) Comparator Interrupt Status Mask	15:13	"IM_" + name of respective bit in R31	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R39 enables or masks the corresponding bit in R31. The default value for these bits is 0 (unmasked).

Table 103 External Interrupts

17.6 BACKUP POWER

A backup power source should be provided for the WM8351 on the VRTC pin. This can be a small rechargeable battery or a high-capacitance capacitor (supercap). The purpose of this component is to power the always-on functions such as the on-chip crystal oscillator, RTC and ALARM control registers and UVLO comparator. As these circuit blocks store settings required for start-up, it is desirable that they continue to operate even when no other power source is available.

The VRTC battery (or capacitor) maintains its charge from the Wall (LINE), USB or BATT sources. The connection is illustrated in Figure 75. The series resistor limits the VRTC charge current. The 1μF capacitor is recommended also for stability; if this capacitor is too small or is not present, the VRTC output may oscillate and cause a system reset.

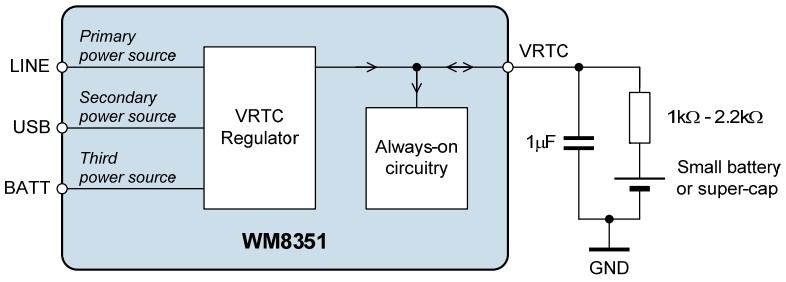


Figure 75 Backup Power

17.7 BATTERY CHARGER

17.7.1 GENERAL DESCRIPTION

The WM8351 incorporates a battery charger which is designed for single-cell lithium batteries. The battery charger can operate from either the Wall (LINE) or USB power sources. Trickle charging at 50mA is enabled by default. The battery charger configuration and termination can run without any intervention required by the host processor.

The battery charger voltage and currents are programmable. Trickle charging at either 50mA or 100mA is supported; fast charging from 50mA up to 750mA is possible under certain conditions. Note that charging from the USB power is subject to the 100mA or 500mA overall limit on the USB source (see Section 17.4).

Battery pack temperature sensing is enabled by default. The connection to the battery's NTC resistor is made using the SWVRTC pin and the AUX1 pin, as illustrated in Figure 76. The SWVRTC pin is a reference source controlled by the WM8351. The AUX1 pin (also an input to the AUXADC) is used as the input to the temperature sensing circuit. Note that the absence of the NTC connection will lead to a temperature failure condition being detected and battery charging will not be possible.

Typical connections for the WM8351 battery charger are illustrated in Figure 76. The resistor value between SWVRTC and AUX1 should be selected to match the NTC. A typical value is 100kΩ.

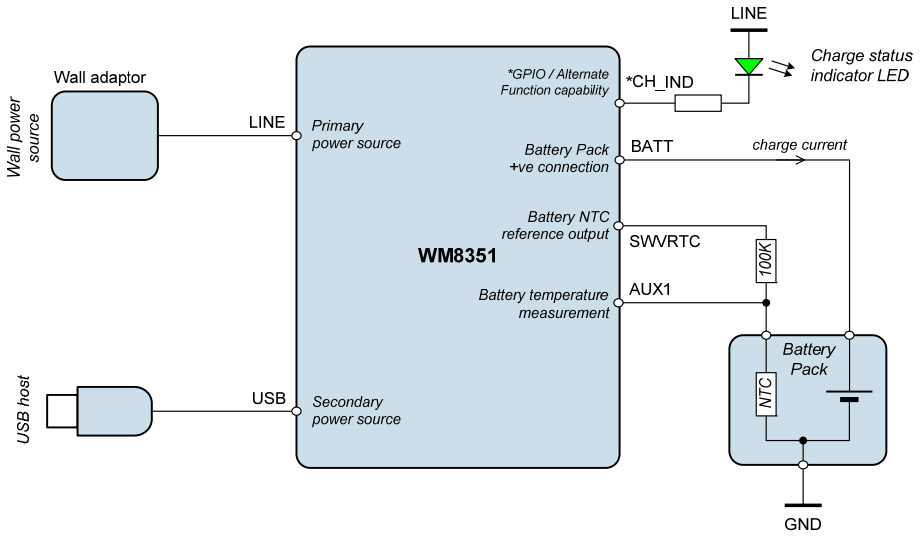


Figure 76 Typical Connections for WM8351 Battery Charger

The WM8351 monitors the battery status via the AUX1 pin and by voltage/current sensing on other pins. See Section 17.7 for details of the battery fault conditions and reporting.

If the application is intended to run without a battery present, then it is recommended that a 3.3μF capacitor be placed on the BATT pin to ensure correct charger behaviour. In this case, the Battery Charger interrupts should also be masked, as these will be invalid - see Section 17.7.8 for details of the Battery Charger Interrupts. It is recommended that the Battery Charger also be disabled in this case - note that the Battery Charger is enabled by default, including on entry to the OFF power state.

A typical battery charge cycle is illustrated in Figure 77. This shows both the trickle charge and fast charge processes.

The trickle charge mode is a constant current mode. Trickle charging is enabled when the battery voltage falls below a charging threshold voltage; it is disabled when the charge current falls to a programmable 'End of Charge' threshold level.

Fast charging consists of two phases:

In the constant current phase, the WM8351 drives a programmable constant current into the battery through the BATT pin. During this phase, the battery voltage rises monotonically until the battery reaches the target voltage.

When the battery reaches the target voltage, the charger enters the constant voltage phase, in which the WM8351 regulates BATT to the target voltage. To achieve this, the WM8351 adjusts the charge current adaptively. The charge current decreases monotonically over time. Fast charging is disabled when the current falls to a programmable 'End of Charge' threshold level.

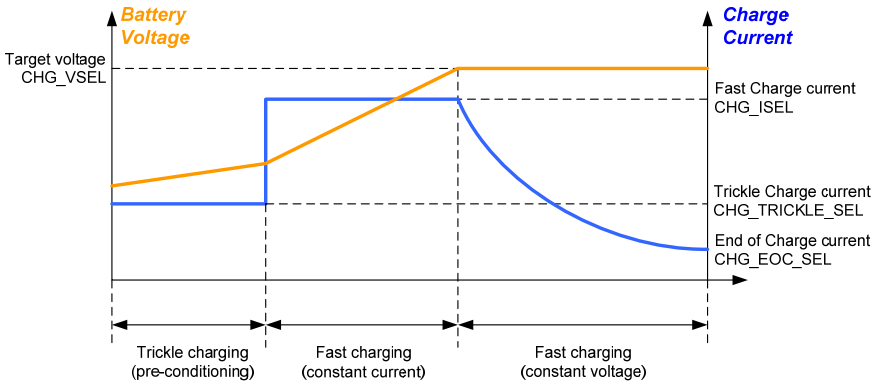


Figure 77 A Typical Charge Cycle

17.7.2 BATTERY CHARGER ENABLE

The battery charger is enabled by default when the WM8351 is in the ACTIVE, HIBERNATE or OFF states. Note that battery charging is only possible when the selected power source is within normal operating limits (see Section 7.5) and is more than 100mV higher than the battery voltage.

The battery charger can be disabled by setting the CHG_ENA register bit to '0'. When the battery charger is enabled, it autonomously checks if the conditions for charging are fulfilled and controls the charging processes accordingly. The status of the battery charger can be read from the CHG_ACTIVE register bit. (Note this bit is read-only.)

The battery charger can be paused by writing to the CHG_PAUSE register bit. This provides a simple option to halt the battery charger and to subsequently restart it without affecting the charge timer or other settings.

The battery charger target voltage is set by the CHG_VSEL field, as defined in Table 104.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) Power Mgmt (5)	9	CHG_ENA	1	CHG_ENA bit selects battery charger current control 0 = Set battery charger current to zero 1 = Enable battery charge control *Protected by security key.*
R168 (A8h) Battery charger control 1	15			
R169 (A9h) Battery charger control 2	15	CHG_ACTIVE	0	Charger Status. 0 = Battery Charging is inactive 1 = Battery Charging is active (Note CHG_ENA is just a request; the WM8351 determines if the conditions are satisfied for Battery Charging).
	14	CHG_PAUSE	0	Charger pause: 0 = Don't pause the charger 1 = Pause charging
	5:4	CHG_VSEL [1:0]	00	Battery charge voltage: 00 = 4.05V 01 = 4.1V 10 = 4.15V 11 = 4.2V
Note: CHG_ENA can be accessed through R9 or through R168. Reading from or writing to either register location has the same effect.				

Table 104 Battery Charger Control

17.7.3 TRICKLE CHARGING

Trickle charging is enabled by default when the Wall (LINE) or USB pins are selected as the power source. It is autonomously initiated, supervised and terminated by the WM8351, without requiring any intervention by the host processor.

By default, trickle charging is initiated when the battery voltage is below the battery charge voltage CHG_VSEL by more than 100mV. Setting the CHG_FRC bit allows trickle charging to be initiated at higher battery voltages.

The trickle charge current is set by the CHG_TRICKLE_SEL field, as described in Table 105.

A choke circuit is provided to enhance the trickle charge current control. This allows the charge current to be modified according to temperature conditions or according to the USB current limit restrictions.

If the WM8351 temperature is above 115°C and trickle charge temperature choking is enabled, then charging is interrupted for at least 8 seconds and until the temperature has fallen below the threshold. If trickle charge temperature choking is not enabled, then charging continues. (Note that the device shutdown temperature is set at 140°C - this threshold cannot be disabled.) Trickle charge temperature choking is controlled by the CHG_TRICKLE_TEMP_CHOKE register bit.

If the USB current limit cannot support the charge current demanded by CHG_TRICKLE_SEL and USB current choking is enabled, then the charge current will be modified, where possible, in order to continue charging. The trickle charge current cannot be controlled dynamically - the only possible charge currents are 50mA or 100mA. Therefore, the only form of USB choking in trickle charge mode is for a demanded current of 100mA to be reduced to 50mA. Trickle charge USB current choking is controlled by the CHG_TRICKLE_USB_CHOKE register bit. The time constant for the charger's attempts to increase the current after USB choking can be controlled by CHG_RECOVERY_T.

The register control fields for Trickle Charging are described in Table 105. See Section 17.7.5 for details of battery charger termination.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R168 (A8h) Battery charger control 1	9	CHG_TRICKLE_TEMP_CHOKE	0	Enable trickle charge temperature choking 0 = disable 1 = enable *Protected by security key.*
	8	CHG_TRICKLE_USB_CHOKE	0	Enable USB current choking in trickle charge 0 = disable 1 = enable *Protected by security key.*
	7	CHG_RECOVER_T	0	Time constant adjust for charger choke recovery (step-up): 0 = Step-up time constant is 180us (allows faster recovery between processor wakeups) 1 = Step-up time constant is >20ms (outside audio band) *Protected by security key*
R169 (A9h) Battery charger control 2	6	CHG_TRICKLE_SEL	0	Selects the trickle charge current. 0 = Set the trickle charge current to 50mA. 1 = Set the trickle charge current to 100mA. *Protected by security key.*
R170 (AAh) Battery charger control 3	7	CHG_FRC	0	Allows trickle-charging to be forced even if the battery voltage is above the default threshold 0 = only trickle-charge if the battery voltage is below CHG_VSEL - 100mV 1 = always trickle-charge *Protected by security key.*

Table 105 Trickle Charging Control

17.7.4 FAST CHARGING

Fast charging provides a faster way to charge the battery. This is only possible under certain conditions. Fast charging must be initiated by the system controller, and can never start autonomously.

Fast charging is normally possible in the ACTIVE state when the selected power source is Wall (LINE) or when USB high power mode is selected. The battery charger determines whether the conditions for fast charging are satisfied; these conditions include a suitable selected power source voltage (see Section 17.7.2) and a suitable battery voltage (greater than 3.1V).

If the conditions for fast charging are satisfied, this is indicated by the WM8351 setting the CHG_FAST_RDY_EINT register bit, as described in Table 106. Providing that the conditions for fast charging are satisfied, then fast charging is enabled by setting the CHG_FAST bit. If the conditions are not satisfied, then CHG_FAST will be held at 0.

The maximum fast charge current is set by the CHG_ISEL register field, as described in Table 106. During fast charging, the current may be dynamically controlled by the WM8351 in order to achieve optimum battery charging. It is recommended that the charge current limit should not be set higher than 400mA when charging from a USB power rail.

A throttle circuit is provided to enhance the fast charge current control. This allows the charge current to be modified according to temperature conditions or according to the USB current limit restrictions.

If the WM8351 temperature is above 115°C, then charging is interrupted for at least 8 seconds and until the temperature has fallen below the threshold. Temperature control of the battery charger is always enabled during Fast Charging.

If the USB current limit is reached during Fast Charging, then the charge current must be reduced. If USB current throttling is enabled, then the charge current will be controlled dynamically in order to continue charging. If USB current throttling is not enabled, then the charging will be terminated. (Note that this may give rise to an erroneous indication of 'End of Charge' as the charging may have terminated prematurely.) If USB current throttling is enabled, then 'End of Charge' will not be indicated, even if the throttle circuit causes the charger current to fall below the End of Charge current threshold. Fast charge USB current throttling is controlled by the CHG_FAST_USB_THROTTLE register bit. The time constant for the charger's attempts to increase the current after USB throttling can be controlled by CHG_THROTTLE_T.

The WM8351 will revert to Trickle charging if the conditions for fast charging are no longer satisfied. This includes selection of the OFF or HIBERNATE states, or selection of USB low power mode. The WM8351 will also revert to Trickle charging if it detects a low battery voltage condition (see Section 17.7.8).

The register control fields for Fast Charging are described in Table 106. See Section 17.7.5 for details of battery charger termination.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (15h) Interrupt Status 1	9	CHG_FAST_RDY_EINT	0	Indicates that the charger is ready to go into fast charge. (Rising Edge triggered) Note: This bit is cleared once read.
R168 (A8h) Battery charger control 1	5	CHG_FAST	0	Enable fast charging. 0 = Fast charging cannot take place. 1 = Enable fast charging (will not start until valid charging conditions are met). Note: This register is held low and can only be written to once the fast charge ready signal has gone high. *Protected by security key.*
	4	CHG_FAST_USB_THROTTLE	0	Enable USB current throttling in fast charge: 0 = Don't do any current throttling when fast charging. 1 = Do current throttle while fast charging. *Protected by security key*
R169 (A9h) Battery charger control 2	3:0	CHG_ISEL [3:0]	0110	Fast charge current limit setting. 0000 = off 0001 = 50mA 0010 = 100mA … (50mA steps) 1111 = 750mA Note: Do not set the charger to be more than 400mA when USB powered. *Protected by security key.*
R170 (AAh) Battery Charger Control 3	6:5	CHG_THROTTLE_T [1:0]	00	Time between steps when the charger throttles back due to USB ILIMIT. 00 = 8us 01 = 16us 10 = 32us 11 = 128us *Protected by security key.*

Table 106 Fast Charging Control

17.7.5 BATTERY CHARGER TIMEOUT AND TERMINATION

Fast charging and Trickle charging is terminated under any of the following conditions:

- Charge current falls below a programmable threshold
- Charger timeout
- Charger fault condition (see Section 17.7.7)

The End of Charge Current threshold can be set between 20mA and 90mA, using the CHG_EOC_SEL register field, as defined in Table 107. Care should be taken to ensure that the End of Charge Threshold is lower than the selected Charge Current Limit (CHG_ISEL and/or CHG_TRICKLE_SEL).

When the End of Charge Current threshold is reached, the CHG_END_EINT interrupt field is set (see Section 17.7.8). The action taken when the End of Charge Current threshold occurs is set by CHG_END_ACT. The battery charging will either be terminated or will continue until timeout.

When Trickle charge choking or Fast charge throttling is enabled, it is possible that these circuits may cause the charge current to be reduced below the CHG_EOC_SEL threshold even though the battery is not fully charged. When choke or throttle control is enabled, the End of Charge detection described above is disabled, and charging always continues until timeout. It is recommended that Trickle charge choking and Fast charge throttling is enabled.

The WM8351 battery charger has a programmable timer. The timer is initiated when either fast charging or trickle charging commences. The initial value of the timer may be set by writing to the CHG_TIME register field. This field can also be read back as an indicator of the charge time remaining. Note that the readback value of this field is coded differently to the write value. Due to the limited resolution provided by the 4-bit field, the readback value is approximate only, to an accuracy of around 35 minutes.

If charging is paused by setting CHG_PAUSE (see Table 104), or is paused due to temperature or maximum current conditions, the charge timer is halted so that the time limit is extended accordingly.

If the charging mode is changed by asserting or de-asserting CHG_FAST, then the timer is reset to its initial value.

If the charging mode reverts to Trickle charge mode as a result of a change in power source or a change in USB power mode, then the timer is not reset, but continues to count down from its earlier value. (Note that the charger will never autonomously switch from Trickle charge mode to Fast charge mode.)

When the Charger Timer completes, the CHG_TO_EINT interrupt field is set (see Section 17.7.8) and charging is terminated.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R168 (A8h) Battery charger control 1	12:10	CHG_EOC_SEL [1:0]	000	Selects what the end of charge current should be set to 000 = 20mA 001 = 30mA (10mA steps) ... 111 = 90mA *Protected by security key.*
	6	CHG_END_ACT	0	Action to take when charging ends: 0 = Set charge current to 0 1 = Do nothing (leave charger on till timeout) *Protected by security key.*
R169 (A9h) Battery charger control 2	11:8	CHG_TIME [3:0]	1011	Writing to his field set the charge timeout duration: 0000 = 60min 0001 = 90min 0010 = 120min 0011 = 150min 0100 = 180min 0101 = 210min 0110 = 240min 0111 = 270min 1000 = 300min 1001 = 330min 1010 = 360min 1011 = 390min 1100 = 420min 1101 = 450min 1110 = 480min 1111 = 510min Reading from this field indicates the charge time remaining: Time remaining = CHG_TIME * 2048s *Protected by security key.*

Table 107 Battery Charger Termination

17.7.6 BATTERY CHARGER STATUS

The status of the Battery Charger can be read from the CHG_STS register field, as described in Table 108. This field indicates whether the charger is active in trickle or fast charge modes.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R169 (A9h) Battery charger control 2	13:12	CHG_STS [1:0]	00	Charger status: 00 = Charger off, current set to 0. 01 = In trickle charge mode. 10 = In fast charge mode. 11 - Reserved

Table 108 Battery Charger Status

In addition to the CHG_STS register readback, the charger status can be indicated on an LED connected to a GPIO pin configured as CH_IND (see Section 20). The CH_IND function is an open-drain LED output that provides a visible indication of the charger status.

CHARGER STATUS	CH_IND ACTION
Charger current set to zero	LED off
Trickle charging	LED blinks slowly (0.5Hz)
Fast charging	LED blink s quickly (1Hz)

Table 109 Battery Charger Status via CH_IND

17.7.7 BATTERY FAULT CONDITIONS

The WM8351 continuously monitors battery temperature, chip temperature and battery voltage. In case of a fault condition, it autonomously takes appropriate action, and alerts the host processor via the applicable interrupt flags.

Battery Temperature Monitoring

The WM8351 can monitor the battery temperature via the NTC (negative temperature coefficient) resistor which is incorporated into suitable battery packs. The NTC resistor must be connected to the AUX1 pin as shown in Section 17.7.1. Typical NTC resistor values vary over a range of temperature (source of information is Vishay Dale's "R-T Curve 2").

The NTC monitoring circuit is designed to detect temperature conditions outside the typical 0°C and 45°C safe battery charging conditions. The WM8351 indicates a cold battery temperature condition is indicated by setting the CHG_BATT_COLD_EINT interrupt. A hot battery temperature is indicated by setting the CHG_BATT_HOT_EINT interrupt. Battery charging is suspended when either of these conditions is set. (Note that trickle charging will resume once the battery temperature has returned to within normal levels.)

It is possible to disable the NTC detection circuit and associated flags. This option is protected by a security key. The associated register bits are described in Table 110.

Safety warning - The battery temperature sensor is a safety mechanism and it is strongly recommended that it be used, as directed, in all applications requiring Charger functionality. Disabling this feature by any means, intentional or otherwise, could result in incorrect behaviour of the battery charger function.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R168 (A8h) Battery Charger Control 1	3	CHG_NTC_MON	1	Enable charger battery NTC detection (some batteries may not need this - turn off with caution) 0 = Charger ignores NO_NTC detection. 1 = Charger monitors NO_NTC detection. *Protected by user key, read-only in ROM configs.*
	2	CHG_BATT_HOT_MON	1	Enable charger battery temperature high detection (some batteries may not need this - turn off with caution) 0 = Charger ignores battery temperature too high. 1 = Charger monitors battery temperature too high. *Protected by user key, read-only in ROM configs.*
	1	CHG_BATT_COLD_MON	1	Enable charger battery temperature low detection (some batteries may not need this - turn off with caution) 0 = Charger ignores battery temperature low. 1 = Charger monitors battery temperature low. *Protected by user key, read-only in ROM configs.*
Note: Some batteries may not require battery temperature monitoring. Disable with caution.				

Table 110 Battery Temperature Monitoring

Chip Temperature Monitoring

The WM8351 has a built-in temperature sensor to monitor the silicon die temperature. If the chip temperature reaches the thermal warning level, the WM8351 sets the SYS_CHIP_GT115_EINT (see Section 25) and Battery Charger operation may be paused (this is programmable in Trickle Charge mode). The charger operation will resume once the chip temperature has dropped below the thermal warning level.

If the chip temperature reaches the thermal shutdown level, the WM8351 sets the SYS_CHIP_GT140_EINT interrupt and shuts down. (Battery charging is always terminated in this case.)

Battery Voltage Detection / Defective Battery Detection

A low battery voltage is an indicator that the battery may be defective or removed.

In trickle charge mode, the battery voltage is checked after 30 minutes of charging, or after a quarter of the charging time CHG_TIME (the larger of these two times applies). If the battery voltage is less than the defective battery threshold (nominal value 2.85V) at this time, then the battery charging stops and the WM8351 sets the CHG_BATT_FAIL_EINT interrupt as defined in Table 111.

The battery failure condition is cleared if the battery voltage rises above the defective battery threshold. It is also cleared if any of the WM8351 power sources (including BATT) is removed and re-applied, or if the host processor invokes USB Suspend mode. When the failure condition is cleared, the charger then reverts back to its initial state, and may re-start if the conditions for charging are fulfilled (see Section 17.7.2).

If fast charging mode is selected, and the battery voltage is less than the defective battery threshold, then the WM8351 immediately reverts to trickle charging. If the fault persists, then trickle charging stops as described above.

17.7.8 INTERRUPTS AND FAULT PROTECTION

The battery charger can raise a first-level interrupt, CHG_INT (see Section 24) to report status and fault conditions to the host processor. The CHG_INT interrupt is the logical OR of all the second-level interrupts described in Table 111.

Note: If a battery is connected to the BATT pin, but the WM8351 is being powered from the Wall or USB supplies, then disconnection of the Wall or USB supply will cause the CHG_VBATT_LT_3P1_EINT and CHG_VBATT_LT_2P85_EINT interrupts to be set.

The CHG_VBATT_LT_3P1_EINT and CHG_VBATT_LT_2P85_EINT interrupts can be masked by setting the associated mask bits defined in Table 111.

Alternatively, the EXT_USB_FB_EINT and/or EXT_WALL_FB_EINT interrupts (see Section 17.5) can be used to validate the Battery Undervoltage interrupts - if one of the External Feedback interrupts is set at the same time as the Battery Undervoltage interrupts, then the Battery Undervoltage interrupts should be ignored.

ADDRESS	BIT	LABEL	DESCRIPTION
R25 (19h) Interrupt Status 1	15	CHG_BATT_HOT_EINT	Battery temp too hot. (Rising Edge triggered) Note: This bit is cleared once read.
	14	CHG_BATT_COLD_EINT	Battery temp too cold. (Rising Edge triggered) Note: This bit is cleared once read.
	13	CHG_BATT_FAIL_EINT	Battery fail. (Rising Edge triggered) Note: This bit is cleared once read.
	12	CHG_TO_EINT	Charger timeout. (Rising Edge triggered) Note: This bit is cleared once read.
	11	CHG_END_EINT	Charging final stage. (Rising Edge triggered) Note: This bit is cleared once read.
	10	CHG_START_EINT	Charging started. (Rising Edge triggered) Note: This bit is cleared once read.
	9	CHG_FAST_RDY_EINT	Indicates that the charger is ready to go into fast charge. (Rising Edge triggered) Note: This bit is cleared once read.
	2	CHG_VBATT_LT_3P9_EINT	Battery Voltage < 3.9 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	1	CHG_VBATT_LT_3P1_EINT	Battery voltage < 3.1 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	0	CHG_VBATT_LT_2P85_EINT	Battery voltage < 2.85 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R33 (21h) Interrupt Status 1 mask	15:0	"IM_" + name of respective bit in R25 (19h)	Mask bits for battery charger interrupts Each of these bits masks the respective bit in R25 when it is set to 1 (e.g. CHG_FAST_RDY in R25 does not trigger a CHG_INT interrupt when IM_CHG_FAST_RDY in R33 is set).

Table 111 Battery Charger Interrupts

18 SYSTEM MONITORING AND UNDERVOLTAGE LOCKOUT (UVLO)

The WM8351 includes several mechanisms to prevent the system from starting up, or force it to shut down, when power sources are critically low.

The under-voltage lockout (UVLO) is a non-programmable voltage limit. When the available supplies are below this limit, the WM8351 enters the BACKUP state. The WM8351 can only proceed from BACKUP to the OFF state if LINE is above the UVLO level. Whenever the WM8351 is in ACTIVE, HIBERNATE or OFF state and LINE falls below the UVLO level, the WM8351 returns to the BACKUP state.

The UVLO limit threshold is equal to VRTC + 50mV. The precise value of VRTC may vary between devices, within the limits defined in the Electrical Characteristics (see Section 7.5).

The startup threshold is a programmable voltage limit. The WM8351 can only proceed from OFF to the ACTIVE state if LINE is above the startup threshold. (Note that, in the case of USB-powered operation, there are additional voltage requirements; see Section 17.4.). The startup threshold is determined by the PCCMP_ON_THR register field.

The shutdown threshold is determined by the PCCMP_OFF_THR register field. When LINE falls below this threshold, the WM8351 raises a SYS_HYST_COMP_FAIL_EINT interrupt. In addition, the WM8351 takes the action set by PCCOMP_ERRACT. If this bit is set, then the WM8351 will shut down in response to the LINE voltage falling below the shutdown threshold.

The startup and shutdown control register fields are described in Table 112. Note that the startup threshold should always be set higher than the shutdown threshold in order to create a hysteresis, making the system more stable.

The SYS_HYST_COMP_FAIL_EINT interrupt is one of the second-level interrupts which triggers a first-level System Interrupt, SYS_INT (see Section 24). This can be masked by setting the mask bit as described in Table 113.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R179 (B3h) Power Check Comparator	14	PCCMP_ERRACT	0	Action to take when LINE falls below PCCMP_OFF_THR level (as well as generating an interrupt) 0 = ignore 1 = shut down system
	6:4	PCCMP_OFF_THR [2:0]	010	Power check comparator system shutdown threshold value 000 = 2.9V 001 = 3.0V … 111 = 3.6V *Protected by security key.*
	2:0	PCCMP_ON_THR [2:0]	101	Power check comparator system startup threshold value 000 = 2.9V 001 = 3.0V … 111 = 3.6V *Protected by security key.*

Table 112 Battery Monitoring and UVLO Control

ADDRESS	BIT	LABEL	DESCRIPTION
R26 (1Ah) Interrupt Status 2	3	SYS_HYST_COMP_FAIL_EINT	Hysteresis comparator indication that LINE or BATT is less that shutdown threshold. (Rising Edge triggered) Note: This bit is cleared once read.
R34 (22h) Interrupt Status 2 Mask	3	IM_SYS_HYST_COMP_FAIL_EINT	Mask bit for Hysteresis comparator interrupt When set to 1, IM_SYS_HYST_COMP_FAIL_EINT masks SYS_HYST_COMP_FAIL_EINT in R29 and does not trigger an SYS_INT interrupt when SYS_HYST_COMP_FAIL_EINT is set).

Table 113 Battery Monitoring and UVLO Interrupts

19 AUXILIARY ADC

19.1 GENERAL DESCRIPTION

The WM8351 incorporates a low-power 12-bit Auxiliary ADC (AUXADC). This can be used to measure a number of internal or external voltages, with either VREF or VRTC as its reference. A programmable potential divider enables the AUXADC to measure voltages higher than the reference.

Note that the AUX1 pin is also the input for the battery pack temperature monitoring circuit and is therefore not freely available for other analogue inputs. The battery NTC input can still be sampled and readback via AUX1 in the same way as the other AUXADC inputs. The AUX1 pin may be used for other purposes if the NTC detection is disabled and/or the associated Battery Charger interrupts are masked. See Section 17.7 for details of the battery pack NTC functions.

The AUXADC circuit is illustrated in Figure 78.

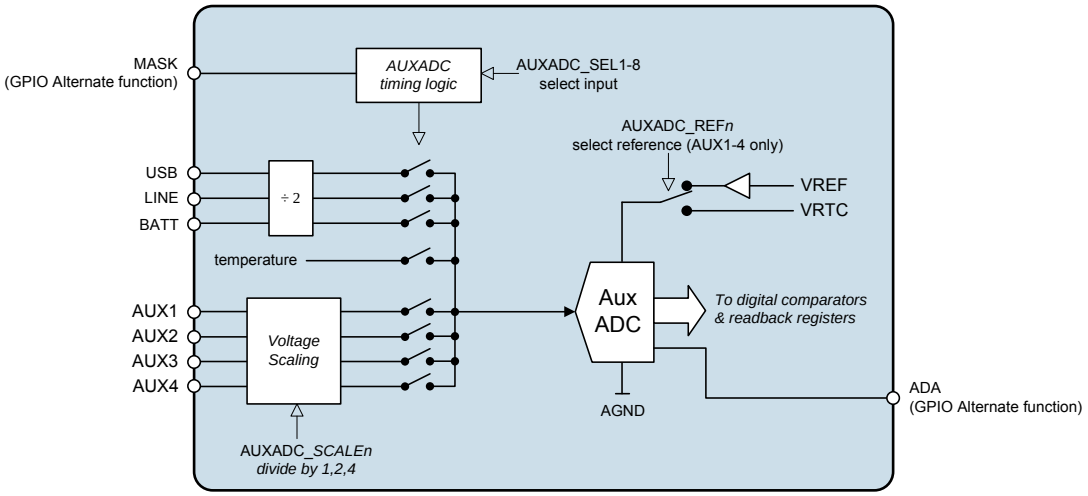


Figure 78 Auxiliary ADC

The AUXADC is enabled using the AUXADC_ENA register bit as described in Table 114.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) Power Mgmt (5)	7	AUXADC_ENA	0	AUXADC control 0 = disabled 1 = enabled
R144 (90h) Digitizer Control (1)	15			
Note: AUXADC_ENA can be accessed through R12 or through R144. Reading from or writing to either register location has the same effect.				

Table 114 AUXADC Enable

19.2 INITIATING AUXADC MEASUREMENTS

The AUXADC can measure voltages on four external pins, AUX1, AUX2, AUX3 and AUX4. It can also measure voltages on the USB, LINE and BATT pins, and also the temperature sensor level. Each of these 8 inputs can be independently selected or deselected as an AUXADC input. Whenever the AUXADC is triggered, the AUXADC performs a measurement of each of the selected AUXADC inputs. By default, none of the AUXADC inputs is selected. Therefore, the required inputs must be enabled using the AUXADC_SEL*n* bits prior to initiating an AUXADC measurement.

AUXADC measurements can be scheduled in a number of different ways, as determined by the AUXADC_CTC register bit. In Polling Mode, a set of measurements is initiated by writing a logic '1' to the AUXADC_POLL bit. (This bit is then automatically reset once the measurements have been completed.) In Continuous Mode, the WM8351 initiates a set of measurements at a time interval that is determined by the AUXADC_CRATE field.

Additional control can be provided using a GPIO pin configured as a 'MASK' input (see Section 20). The behaviour of the MASK input is selected using the AUXADC_MASKMODE register field - it can be used to inhibit any measurements triggered by the Polling or Continuous modes, or else it can be used as a hardware input to initiate a set of measurements.

Note that, when AUXADC_MASKMODE = 11, then AUXADC_CTC, AUXADC_POLL and AUXADC_CRATE have no effect. The polarity of the MASK input can be adjusted to be active high or active low using the GP*n*_CFG bits defined in Section 20, where 'n' identifies the particular GPIO pin in use.

The control fields associated with initiating AUXADC measurements are defined in Table 115.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R144 (90h) Digitiser Control (1)	14	AUXADC_CTC	0	Continuous conversion mode: 0 = Polling mode 1 = Continuous mode
	13	AUXADC_POLL	0	Writing "1" initiates a set of measurements in polling mode (AUXADC_CTC=0). This bit is automatically reset after the measurements are completed.
	7	AUXADC_SEL8	0	AUXADC TEMP input select 0 = Disable TEMP measurement 1 = Enable TEMP measurement
	6	AUXADC_SEL7	0	AUXADC BATT input select 0 = Disable BATT measurement 1 = Enable BATT measurement
	5	AUXADC_SEL6	0	AUXADC LINE input select 0 = Disable LINE measurement 1 = Enable LINE measurement
	4	AUXADC_SEL5	0	AUXADC USB input select 0 = Disable USB measurement 1 = Enable USB measurement
	3	AUXADC_SEL4	0	AUXADC AUX4 input select 0 = Disable AUX4 measurement 1 = Enable AUX4 measurement
	2	AUXADC_SEL3	0	AUXADC AUX3 input select 0 = Disable AUX3 measurement 1 = Enable AUX3 measurement
	1	AUXADC_SEL2	0	AUXADC AUX2 input select 0 = Disable AUX2 measurement 1 = Enable AUX2 measurement
	0	AUXADC_SEL1	0	AUXADC AUX1 input select 0 = Disable AUX1 measurement 1 = Enable AUX1 measurement

R145 (91h) Digitiser Control (2)	13:12	AUXADC_MASK MODE [1:0]	00	AUXADC MASK input control 00 = MASK is ignored 01 = When MASK is asserted, all AUXADC measurements are inhibited. 10 = Reserved 11 = MASK input initiates AUXADC measurements. AUXADC_POLL and AUXADC_CTC have no effect. MASK polarity is controlled by GP*n*_CFG.
	10:8	AUXADC_CRATE [2:0]	000	AUXADC measurement frequency in Continuous mode 000 = 1Hz 001 = 4Hz 010 = 8Hz 011 = 16Hz 100 = 32Hz 101 = 64Hz 110 = 128Hz 111 = 256Hz

Table 115 Initiating AUXADC Measurements

In Polling mode, setting AUXADC_POLL = 1 initiates one set of measurements, after which the AUXADC waits for a new trigger.

In Continuous mode, a set of measurements will be initiated at the frequency set by AUXADC_CRATE.

When using MASK to initiate measurements (AUXADC_MASKMODE=11), a rising edge (if GP*n*_CFG = 1) or a falling edge (if GP*n*_CFG = 0) initiates one set of AUXADC measurements. The MASK signal must be asserted for long enough for the AUXADC to perform all the selected measurements.

The AUXADC_SEL*n* bits should not be changed until all previous measurement results stored in the AUX*n* readback registers have been read.

19.3 VOLTAGE SCALING AND REFERENCES

For inputs AUX1, AUX2, AUX3 and AUX4, the AUXADC measurements may be referenced to either VRTC or VREF (see Section 21). The selected reference can be selected independently for each input, using the control fields described in Table 116. In the case of USB, BATT, LINE and Temperature, the AUXADC measurements are referenced to VRTC.

In the case of AUXADC measurements which are referenced to VREF, a buffered copy of VREF is used as an input to the AUXADC. Setting the AUXADC_RBMODE field allows this buffer to be enabled at all times when the AUXADC is enabled, or else to only be enabled when a VREF-referenced measurement is made.

In order to measure voltages that may be higher than VRTC or VREF, a programmable divider is provided on each of AUX1, AUX2, AUX3 and AUX4. These are controlled using the AUXADC_SCALE*n* bits, allowing the inputs to be divided by 1, 2 or 4. In the case of USB, BATT and LINE, a fixed 'divide by 2' applies.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R152 (98h) AUX1 R153 (99h) AUX2	14:13	AUXADC_SCALE*n* [1:0]	11	AUX*n* input select 00 = Off 01 = Input divided by 1 10 = Input divided by 2 11 = Input divided by 4
R154 (9Ah) AUX3 R155 (9Bh) AUX4	12	AUXADC_REF*n*	1	AUX*n* reference select 0 = AUX*n* measured relative to VRTC 1 = AUX*n* measured relative to VREF
R145 (91h) Digitizer Control (2)	1	AUXADC_RBMODE	1	Enable for AUXADC bandgap (VREF) buffer. 0 = AUXADC REFBUF is only enabled during conversions that use the VREF as a reference 1 = AUXADC REFBUF is always enabled when the AUXADC is enabled

Table 116 AUXADC Reference Selection

19.4 AUXADC READBACK

Measured data from the AUXADC can be accessed by reading registers R152 through to R159, as defined in Table 117. This data may be read at any time, or may be read in response to the WM8351 indicating that new data is available.

The WM8351 indicates that new AUXADC data is available by setting the AUX_DATARDY_EINT interrupt flag as described in Section 19.7. This is one of five second-level interrupts which triggers a first-level System Interrupt, AUXADC_INT (see Section 24). This interrupt can be masked by setting the mask bit as described in Table 120. The AUX_DATARDY_EINT interrupt is set high when new data is available. It is reset when the associated interrupt register R26 is read.

The WM8351 can also indicate that new AUXADC data is available via a GPIO pin configured as ADA (Aux Data Available). This flag is set high when new data is available. It is reset when the associated data has been read from the readback registers R152 through to R159. See Section 20 for details of how to configure a GPIO pin as ADA.

To avoid losing data that has not yet been read, the WM8351 can inhibit overwriting the measurement registers with new data until the previous data has been read. When the AUXADC_WAIT bit is set, then AUXADC measurements are prevented from being overwritten until they have been read. Any Poll, Continuous or Mask-triggered AUXADC measurement will be ignored if the AUXADC_WAIT feature prevents the measurement from being overwritten.

Always specify the address of the starting register. Single data read from last register is not supported.

Reading from registers R152 to R159 returns a 12-bit code which represents the most recent AUXADC measurement on the associated channel. This code can be equated to the actual voltage (or temperature) according to the following equations:

To calculate the voltage for external measurements on the AUX input pins use the following formula:

AUXn = (Output Code / 4095) x Reference Voltage x AUX Input Scale

To calculate the voltage for internal AUXADC measurements on USB, LINE and Battery:

USB, LINE & BATT = (Output Code / 4095) x VRTC x 2

To calculate the temperature (in degrees Celsius) from AUXADC measurements on TEMP:

Temperature = 460.32 - ((Output Code / 4095) x VRTC x 614.6)

where-

Output Code = the relevant AUXADC_DATA field, decoded as an unsigned integer

Reference Voltage = VRTC voltage or VREF voltage, depending on AUXADC_REF*n*

AUX Input Scale = 1, 2 or 4, depending on AUXADC_SCALE*n* [1:0]

In a typical application, the AUX1 input is the battery pack temperature sensing (NTC) input. The voltage at this input may be used as an indicator of the battery pack temperature.

The NTC input should be measured relative to the VRTC voltage. The hot temperature threshold (CHG_BATT_HOT_EINT) corresponds to 0.33 x VRTC. This equates to approximately +45°C. The cold temperature threshold (CHG_BATT_COLD_EINT) corresponds to 0.74 x VRTC. This equates to approximately 0°C.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R152 (98h) AUX1 R153 (99h) AUX2 R154 (9Ah) AUX3 R155 (9Bh) AUX4	11:0	AUXADC_DATA *n* [11:0]	000h	Measured AUXn data value relative to reference: 000 = 0V FFF = measured voltage after divide matches reference
R156 (9Ch) USB Voltage Readback	11:0	AUXADC_DATA_USB [11:0]	0h	Measured USB voltage data value.
R157 (9Dh) LINE Voltage Readback	11:0	AUXADC_DATA_LINE [11:0]	0h	Measured LINE voltage data value
R158 (9Eh) BATT Voltage Readback	11:0	AUXADC_DATA_BATT [11:0]	0h	Measured Battery Voltage
R159 (9Fh) Chip Temperature Readback	11:0	AUXADC_DATA_CHIPTEMP [11:0]	0h	Measured Internal chip temperature
R145 (91h) Digitizer Control (2)	0	AUXADC_WAIT	0	Whether the old data must be read before new conversions can be made 0 = No effect (new conversions overwrite old) 1 = New conversions are held back (and measurements delayed) until AUX_DATAn has been read.

Table 117 Reading AUXADC Measurements

In a typical application, one of the following methods is likely to be used to control the AUXADC readback:

For interrupt-driven AUXADC readback, the host processor would read the AUXADC data registers in response to the AUXADC Interrupt or ADA output. In Continuous AUXADC mode, the processor should complete this action before the next measurement occurs, in order to avoid losing any AUXADC samples. In Polling mode, the interrupt (or ADA) signal provides confirmation that the commanded set of measurements has been completed.

For host-controlled AUXADC readback, the Continuous AUXADC mode would be used, and the AUXADC_WAIT bit would be asserted. The host processor would read the AUXADC data registers periodically, causing the next AUXADC measurement to be enabled. This limits the frequency of the AUXADC measurements to the readback frequency.

19.5 CALIBRATION

The on-chip reference VREF provides a highly accurate reference voltage to the AUXADC. For best measurement accuracy, the WM8351 provides a way to determine the voltage offset of the AUXADC's VREF buffer and the gain error introduced by scaling the AUXADC input. Measured data can then be adjusted accordingly, eliminating these errors.

To determine the buffer's offset, the AUXADC AUX3 input is disconnected from the AUX3 pin and connected to the unbuffered VREF voltage. Note that input scaling must be used, (i.e. AUXADC_SCALE3 = 10 or 11), in order to ensure that the AUXADC input is within the measurable range. Measuring this voltage using the buffered VREF as the reference (AUXADC_REF3 = 1) makes it possible to calculate the combined error.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R145 (91h) Digitizer Control (2)	2	AUXADC_CAL	0	Configure AUX3 input to be the VREF supply for AUXADC calibration. 0 = AUX3 input connected to AUX3 pin 1 = AUX3 input connected to unbuffered VREF

Table 118 AUXADC Calibration

19.6 DIGITAL COMPARATORS

The WM8351 has four digital comparators which may be used to compare AUXADC measurement data against programmable threshold values. Each comparator has an associated interrupt flag, as described in Section 19.7, which indicates that the associated data is beyond the threshold value.

The digital comparators are enabled using the DCMPn_ENA register bits as described in Table 119.

The source data for each comparator is selected using the DCMP*n*_SRCSEL register bits; this selects one of the eight AUXADC channels for each comparator. Note that, if required, the same AUXADC channel may be selected for more than one comparator; this would allow more than one threshold to be monitored on the same AUXADC channel.

The DCMP*n*_GT register bits select whether an interrupt will be indicated when the measured value is above the threshold or when the measured value is below the threshold.

The threshold DCMP*n*_THR is a 12-bit code for each comparator. This field follows the same voltage scaling and voltage reference as the associated AUXADC channel source.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) Power Mgmt (5) or R163 (A3h) Generic Comparator Control	3	DCMP4_ENA	0	Digital comparator 4 enable 0 = disabled 1 = enabled
	2	DCMP3_ENA	0	Digital comparator 3 enable 0 = disabled 1 = enabled
	1	DCMP2_ENA	0	Digital comparator 2 enable 0 = disabled 1 = enabled
	0	DCMP1_ENA	0	Digital comparator 1 enable 0 = disabled 1 = enabled
R164 (A4h) Generic comparator 1 R165 (A5h) Generic Comparator 2 R166 (A6h) Generic Comparator 3 R167 (A7h) Generic Comparator 4	15:13	DCMP*n*_SRCSEL [2:0]	000	DCOMP*n* source select. 000 = AUX1 001 = AUX2 010 = AUX3 011 = AUX4 100 = USB 101 = LINE 110 = BATT 111 = TEMP
	12	DCMP*n*_GT	0	DCOMP*n* interrupt control 0 = interrupt when the source is less than threshold 1 = interrupt when the source is greater than threshold
	11:0	DCMP*n*_THR [11:0]	000h	DCOMP*n* threshold (12-bit unsigned binary number)
Note: *n* is a number between 1 and 4 that identifies the individual comparator **Note:** The Comparator Enable bits can each be accessed through two separate control registers. Reading from or writing to either register location has the same effect.				

Table 119 AUXADC Digital Comparator Control

19.7 AUXADC INTERRUPTS

The AUXADC has five second-level interrupts which can trigger a first-level System Interrupt, AUXADC_INT (see Section 24). These are described in Table 120. Each AUXADC interrupt in Register R26 can be masked by setting the associated mask bit in Register R34.

The AUX_DATARDY_EINT interrupt indicates that new AUXADC data is ready. This bit is cleared when Register R26 is read. Note that this bit is not cleared by reading the measured AUXADC data in Registers R152 to R159.

The AUXADC_DCOMP*n*_EINT interrupts indicate that the selected AUXADC channel on Comparator 'n' is beyond the programmed threshold. The DCMP*n*_GT register bits defined in Table 119 select whether an interrupt indicates the measured value is above the threshold or indicates the measured value is below the threshold.

ADDRESS	BIT	LABEL	DESCRIPTION
R26 (1Ah) Interrupt Status 2	8	AUXADC_DATARDY_EINT	Auxiliary data ready. (Rising Edge triggered) Note: This bit is cleared once read.
	7	AUXADC_DCOMP4_EINT	DCOMP4 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	6	AUXADC_DCOMP3_EINT	DCOMP3 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	5	AUXADC_DCOMP2_EINT	DCOMP2 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	4	AUXADC_DCOMP1_EINT	DCOMP1 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R34 (22h) Interrupt Status 2 Mask	8:4	"IM_" + name of respective bit in R26	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt.

Table 120 AUXADC Interrupts

20 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

20.1 GENERAL DESCRIPTION

The WM8351 has thirteen general-purpose input/output (GPIO) pins; GPIO0 - GPIO12. These can be configured as inputs or outputs, active high or active low, with optional on-chip pull-up or pull-down resistors. Alternate functions are also available for each GPIO pin.

Note that different GPIO pins are supported on different power domains. The applicable power domain is specific to a pin, not to a particular GPIO function. The power domains are as follows:

- GPIO0 to GPIO3 : VRTC
- GPIO4 to GPIO9 : DBVDD
- GPIO10 to GPIO12 : LINE

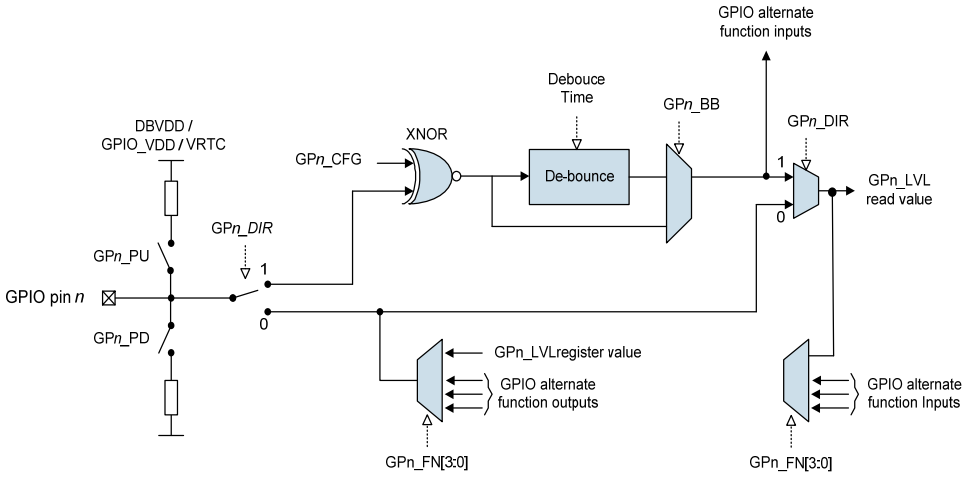


Figure 79 GPIO Equivalent Circuit

20.1.1 CONFIGURING GPIO PINS

To configure a pin as a GPIO, the corresponding GP*n*_FN register bits must be set to 0000 (see Table 125). Each GPIO pin can be set up as an input or as an output through the corresponding GP*n*_DIR register bits. Note that, when changing GP*n*_DIR, it is recommended to set GP*n*_FN = 0000 first. See Section 20.2.2 for the recommended sequence of commands when updating the GPIO pin function.

The state of a GPIO output is determined by writing to the corresponding GP*n*_LVL register bit. For GPIO inputs, reading the GP*n*_LVL bit returns the logic level at the GPIO pin.

The polarity of GPIO inputs can be selected through the corresponding GP*n*_CFG bit. For GPIO outputs, the GP*n*_CFG bit controls the electrical characteristics of the output pin.

GPIO inputs can also generate an interrupt (see Section 20.1.3). The GP*n*_INTMODE selects whether an interrupt occurs on a rising edge only, or else on both rising and falling edges. The input to this function is influenced by the polarity bit GP*n*_CFG described above.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
R129 (81h) GPIO pull-up	12:0	GP*n*_PU [12:0]	Dependant on CONFIG settings	GPIO*n* pull-up 0 = Normal 1 = Pull-up enabled Only valid when GPIO*n* is set to input. Do not select pull-up and pull-down at the same time. (see note)	
R130 (82h) GPIO pull-down	12:0	GP*n*_PD [12:0]	Dependant on CONFIG settings	GPIO*n* pull-down 0 = Normal 1 = Pull-down enabled Only valid when GPIO*n* is set to input. Do not select pull-up and pull-down at the same time. (see note)	
R131 (83h) GPIO Interrupt Mode	12:0	GP*n*_INTMODE [12:0]	0	GPIO*n* Pin Mode: 0 = GPIO interrupt is rising edge triggered and taken after the effect of GP*n*_CFG register bit 1 = GPIO interrupt is both rising and falling edge triggered	
R134 (86h) GPIO Pin Configuration	12:0	GP*n*_DIR [12:0]	Dependant on CONFIG settings	GPIO*n* pin direction 0 = Output 1 = Input	
R135 (87h) GPIO Pin Polarity / Type	12:0	GP*n*_CFG [12:0]	Dependant on CONFIG settings	Selects input polarity /output type for GPIO*n*	
				Input (GP*n*_DIR=1)	Output (GP*n*_DIR=0)
				0 = active low 1 = active high (see Note)	0 = CMOS 1 = open-drain (see Note)
R230 (E6h) GPIO pin status	12:0	GP*n*_LVL [12:0]	N/A	Logic level of GPIO*n* pin	
				Input (GP*n*_DIR=1)	Output (GP*n*_DIR=0)
				Read GP*n*_LVL to check logic level. Writing '0' clears GP*n*_EINT	Write to GP*n*_LVL to change logic level.
Note: *n* is a number between 0 and 12 that identifies the individual GPIO.					

Table 121 Configuring the GPIO Pins

Notes:

1. The GPIO input functions /MR, /WAKEUP and /LDO_ENA behave differently to other GPIO inputs. These functions are Active Low by default, when GPn_CFG = 1. These functions may be changed to Active High by setting GPn_CFG = 0.

2. If a GPIO pin is configured as an open drain output, (ie. GP*n*_DIR=0, GP*n*_CFG=1), then the external pull-up voltage must not be greater than the supply domain for the corresponding GPIO. For example, if the GPIO supply domain is DBVDD then the external pull-up voltage must be less than or equal to DBVDD.

3. Do not enable pull-up and pull-down resistors for the same GPIO pin.

4. The internal pull-up and pull-down on GPIO10, GPIO11 and GPIO12 may be too weak for many applications. If pull-up or pull-down is required on these pins, it is recommended to ensure that the pull resistance is <100kΩ. This can be achieved using an external resistor on its own or in combination with the internal resistance.

20.1.2 INPUT DE-BOUNCE

GPIO inputs have an optional de-bounce function to remove glitches from the input signal. This may be useful when the GPIO is connected to a mechanical switch. The de-bounce function can be enabled for each pin individually using GP*n*_DB, with a globally selectable de-bounce time set by GP_DBTIME.

GPIO alternative functions PWR_ON, PWR_OFF and /WAKEUP are special cases with regard to debouncing. PWR_ON and /WAKEUPthese have a debounce time of GP_DBTIME[1:0] + 40ms and PWR_OFF has a debounce time of GP_DBTIME[1:0] + 5ms.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R128 (80h) GPIO de-bounce	12:0	GP*n*_DB [12:0]	1	GPIO*n* debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0])
R133 (85h) GPIO Control	7:6	GP_DBTIME [1:0]	00	De-bounce time for all GPIO inputs 00 = 64μs 01 = 0.5ms 10 = 1ms 11 = 4ms Note: PWR_ON, PWR_OFF and /WAKEUP have additional debounce times.
Note: *n* is a number between 0 and 12 that identifies the individual GPIO.				

Table 122 Configuring GPIO De-bounce

20.1.3 GPIO INTERRUPTS

The GPIO logic can raise a first-level interrupt, GPIO_INT (see Section 24). This interrupt is the logical OR of the second-level GPIO interrupts described in Table 123.

ADDRESS	BIT	LABEL	DESCRIPTION
R30 (1Eh) GPIO Interrupt Status	12:0	GP*n*_EINT [12:0]	GPIO*n* interrupt. (Trigger controlled by GP*n* registers.) Note: This bit is cleared once read.
R38 (26h) GPIO Interrupt Mask	12:0	"IM_" + name of respective bit in R30	Mask bits for GPIO interrupts Each of these bits masks the respective bit in R30 when it is set to 1 (e.g. GP*n*_EINT in R30 does not trigger a GPIO_INT interrupt when IM_GP*n*_EINT in R38 is set).
Note: *n* is a number between 0 and 12 that identifies the individual GPIO.			

Table 123 GPIO Interrupts

20.2 GPIO ALTERNATE FUNCTIONS

20.2.1 LIST OF ALTERNATE FUNCTIONS

The following alternate functions are available.

ALTERNATE FUNCTION NAME	INPUT / OUTPUT	DESCRIPTION
ADCLRCLK	Input	Alternate Left/Right clock for CODEC ADC digital interface. When this function is selected, the LRCLK pin supports the DAC interface only, and GPIO5 provides the ADC digital interface L/R clock. See Section 12.
ADCBCLK	Input	Alternate BCLK for CODEC ADC digital interface. When this function is selected, the BCLK pin supports the DAC interface only, and GPIO6 or GPIO8 provides the ADC digital interface BCLK signal. See Section 12.
CHIP_RESET	Input	Logic input to reset the Chip. When this input is asserted, the chip performs a full reset and re-starts in accordance with the current config mode settings. Note that CHIP_RESET_ENA in register R3 should be set to 1 when using CHIP_RESET as alternative GPIO function.
CSB	Input	3-/4-wire Control Interface Chip Select pin (CSB). Note that this function is selected automatically on GPIO7 when 3-/4-wire mode is selected, ie. regardless of the GP7_FN control field. See Section 11.
FLASH	Input	Hardware trigger for flash function on ISINKA. This function is rising edge triggered. The Current Sink must be in Flash mode, and with the trigger set to GPIO. See Section 16.
HIBERNATE (Level)	Input	Logic input to place the chip into hibernate. The behaviour of some components of the WM8351 in Hibernate mode is configurable. See Section 14. This “level triggered” input is deemed to be asserted for as long as it is logic 1 (or logic 0 if the polarity is inverted).
HIBERNATE (Edge)	Input	Logic input to place the chip into hibernate. The behaviour of some components of the WM8351 in Hibernate mode is configurable. See Section 14. When the “edge triggered” input is used, Hibernate is selected when a rising edge occurs (or a falling edge if the polarity is inverted). After Hibernate has been selected by this method, a “StartUp” event (see Section 14.3.1) is required to exit from Hibernate.
HEARTBEAT	Input	Input to Watchdog function, rising edge triggered. See Section 23.
/LDO_ENA	Input	Enable signal for LDO1. See Section 14.7.4.
L_PWR1	Input	Logic input used to place DC-DC Converters or LDOs into a Low Power state. See Section 14.
L_PWR2	Input	Logic input used to place DC-DC Converters or LDOs into a Low Power state. See Section 14.
L_PWR3	Input	Logic input used to place DC-DC Converters or LDOs into a Low Power state. See Section 14.
MASK	Input	Mask input to AUXADC. This input may be used either to block all inputs to the AUXADC, or to initiate A-D Conversions. See Section 19.
/MR	Input	Logic input used to drive the /RST pin and the /RST and /MEMRST (GPIO outputs) low. Note that this input has no other effect on internal circuits. See Section 14.
PWR_OFF	Input	Logic input signal causes a controlled shutdown of the WM8351. See Section 14.
PWR_ON	Input	Power on input signal from processor (input switching threshold 1.0V). See Section 14.

ALTERNATE FUNCTION NAME	INPUT / OUTPUT	DESCRIPTION
/WAKEUP	Input	Logic input signal causes wakeup from OFF or HIBERNATE states. Can be used for accessory detection. See Section 14.
32kHz	Input	32kHz clock input to Real Time Clock. See Section 22.
ADA	Output	Aux ADC external data available signal. See Section 19. 0 = AUXADC external data not available 1 = AUXADC external data available
ADCLRCLK	Output	Alternate Left/Right clock for CODEC ADC digital interface. When this function is selected, the LRCLK pin supports the DAC interface only, and GPIO5 provides the ADC digital interface L/R clock. See Section 12.
ADCLRCLKB	Output	Inverted Left/Right clock for CODEC ADC digital interface. When this function is selected, the LRCLK pin supports the DAC interface only, and GPIO6 provides the inverted ADC digital interface L/R clock. See Section 12.
ADCBCLK	Output	Alternate BCLK for CODEC ADC digital interface. When this function is selected, the BCLK pin supports the DAC interface only, and GPIO8 provides the ADC digital interface BCLK signal. See Section 12.
/BATT_FAULT	Output	Same as /UVLO signal – indicates no power present. Should be output as soon as possible after /UVLO.
CH_IND	Output	Battery Charge status indication. This output can drive an LED, which indicates battery charging status through different flash rates. See Section 17.
CODEC_OPCLK	Output	Output clock from CODEC. Frequency is determined by OPCLK_DIV. See Section 12.
DO_CONF	Output	Output used for development mode programming. Signal goes high to indicate that external programming can take place (during the Pre-Active state). Same functionality as PWR_ON (GPIO output) but with additional programmable option to prevent reset in OFF mode. See Section 14.
FLASH_OUT	Output	Logic output asserted for the duration of a Flash. See Section 16.
FLL_CLK	Output	Output FLL clock. See Section 12.4.
ISINKC	Output	Open-drain output which can be used to drive LEDs connected to LINE via a series resistor. See Section 16.
ISINKD	Output	Open-drain output which can be used to drive LEDs connected to LINE via a series resistor. See Section 16.
ISINKE	Output	Open-drain output which can be used to drive LEDs connected to LINE via a series resistor. See Section 16.
LINE_SW	Output	Used to drive an external PFET between 'Wall' supply and LINE input, in order to prevent reverse conduction when the Wall Adapter is disconnected. See Section 17.1.
LINE_GT_BATT	Output	Output to enable external PFET to reduce IR loses when LINE is greater than BATT
MICDET	Output	Logic output indicating microphone bias current detection. 0 = Mic Bias Current not detected 1 = Mic Bias Current detected Note that an Interrupt is also generated by this event. See Section 13.12.2.
MICSHT	Output	Logic output indicating microphone bias short circuit detection. 0 = Mic Bias Short Circuit not detected 1 = Mic Bias Short Circuit detected Note that an Interrupt is also generated by this event. See Section 13.12.2.

ALTERNATE FUNCTION NAME	INPUT / OUTPUT	DESCRIPTION
/MEMRST	Output	Output used to control other subsystems such as external memory. Signal goes low to reset external memory. The status of this signal in the Hibernate state is configurable, allowing external memory contents to be retained in Hibernate. See Section 14.
P_CLK	Output	1MHz output clock in phase with the internal DC-DC converters. This signal can be used to sync external circuits (e.g. DC-DCs).
POR_B	Output	Output which toggles low to high during power-on reset
PWR_ON	Output	Output used to indicate that device is powered on (eg. to enable external DC-DC converters). This output is disabled in the OFF state.
/RST	Output	Output used to indicate system resets. Signal goes low during reset, same as the /RST pin. The pulse duration is programmable. See Section 14.
RTC	Output	Real Time Clock output - frequency is controlled by RTC_DSW[3:0]. See Section 22.
SDOUT	Output	4-wire Control Interface data output pin (SDOUT). Note that this function is selected automatically on GPIO6 when 4-wire mode is selected, ie. regardless of the GP6_FN control field. See Section 11.
/VCC_FAULT	Output	Indicates a fault condition on selectable DC Converters, LDO Regulators and the Limit Switch. The mask bits in Register 215 determine which supplies contribute to this status flag. See Section 14.6.5, Section 14.7.3 and Section 15.2.3.
VRTC	Output	Output from on-chip backup power source voltage regulator VRTC.
32kHz	Output	32kHz clock output from the Real Time Clock oscillator.

Table 124 List of GPIO Alternate Functions

20.2.2 SELECTING GPIO ALTERNATE FUNCTIONS

The function of each GPIO pin is programmable by writing to the respective GP*n* register bits. GP*n*_FN = 0000 selects the GPIO function and settings other than 0000 select various alternate functions.

The GPIO function is also determined by the value of the GP*n*_DIR register bit. Note that, when changing GP*n*_DIR, it is recommended to set GP*n*_FN = 0000 first.

When changing the function of a GPIO pin, (updating GPn_FN or GPn_DIR), it is recommended that the following sequence of actions is taken sequentially.

- Set GPn_FN = 0000
- Update the other GPIO configuration fields GP*n*_DB, GP*n*_PU, GP*n*_PD, GP*n*_CFG, GP*n*_DIR
- If the new function is an input, ensure that the input trigger is in the inactive state (ie. logic 0 for a function that is active High)
- Set GPn_FN according to the new GPIO function
- Read the GPIO Interrupt Status Register R30 (1Eh) to clear any GPIO Interrupt events
- If any bit in Register R30 (1Eh) was set when read, then read the System Interrupts Register R24 (18h) to clear the IRQ pin

Note that GPIO7 is automatically enabled as CSB in 3-wire and 4-wire control modes. GPIO6 is automatically enabled as SDOUT in 4-wire control mode. These automatic selections take precedence over all other GPIO6 and GPIO7 control fields.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R140 (8Ch GPIO function select 1	3:0	GP0_FN	Depends on status of CONF pins	Selects function of GPIO0
	7:4	GP1_FN		Selects function of GPIO1
	11:8	GP2_FN		Selects function of GPIO2
	15:12	GP3_FN		Selects function of GPIO3
R141 (8Dh) GPIO function select 2	3:0	GP4_FN		Selects function of GPIO4
	7:4	GP5_FN		Selects function of GPIO5
	11:8	GP6_FN		Selects function of GPIO6
	15:12	GP7_FN		Selects function of GPIO7
R142 (8Eh) GPIO function select 3	3:0	GP8_FN		Selects function of GPIO8
	7:4	GP9_FN		Selects function of GPIO9
	11:8	GP10_FN		Selects function of GPIO10
	15:12	GP11_FN		Selects function of GPIO11
R143 (8Fh)	3:0	GP12_FN		Selects function of GPIO12

Table 125 Control Registers to Select GPIO Alternate Functions

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R140 (8Ch GPIO function select 1	3:0	GP0_FN [3:0]	Depends on status of CONF pins	GPIO0 function definition		
					Input (GP*n*_DIR=1)	Output (GP*n*_DIR=0)
				0000	GPIO	GPIO
				0001	PWR_ON	PWR_ON
				0010	/LDO_ENA	VRTC
				0011	L_PWR1	POR_B
				0100	PWR_OFF	/RST
				0101	CHIP_RESET	
	7:4	GP1_FN [3:0]	Depends on status of CONF pins	GPIO1 function definition		
					Input	Output
				0000	GPIO	GPIO
				0001	PWR_ON	DO_CONF
				0010	/LDO_ENA	/RST
				0011	L_PWR2	/MEMRST
				0100	/WAKEUP	32kHz
	11:8	GP2_FN [3:0]	Depends on status of CONF pins	GPIO2 function definition		
					Input	Output
				0000	GPIO	GPIO
				0001	PWR_ON	PWR_ON
				0010	/WAKEUP	VRTC
				0011	32kHz	32kHz
				0100	L_PWR3	/RST
	15:12	GP3_FN [3:0]	Depends on status of CONF pins	GPIO3 function definition		
					Input	Output
				0000	GPIO	GPIO
				0001	PWR_ON	P_CLK
				0010	/LDO_ENA	VRTC
				0011	PWR_OFF	32kHz
				0100	FLASH	/MEMRST
Note: Undocumented combinations for GP*n*_FN (n = 0 to 3) are reserved						

Table 126 GPIO Function Select 1

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R141(8Dh) GPIO function select 2	3:0	GP4_FN [3:0]	Depends on status of CONF pins	GPIO4 function definition		
					Input (GP*n*_DIR=1)	Output (GP*n*_DIR=0)
				0000	GPIO	GPIO
				0001	/MR	/MEMRST
				0010	FLASH	ADA
				0011	HIBERNATE (Level)	FLASH_OUT
				0100	MASK	/VCC_FAULT
				0101	CHIP_RESET	MICSHT
				1010		MICDET
	7:4	GP5_FN [3:0]	Depends on status of CONF pins	GPIO5 function definition		
					Input	Output
				0000	GPIO	GPIO
				0001	L_PWR1	P_CLK
				0010	ADCLRCLK	ADCLRCLK
				0011	HIBERNATE (Edge)	32kHz
				0100	PWR_OFF	/BATT_FAULT
				0101	HIBERNATE (Level)	MICSHT
				0110	-	ADA
				0111	-	CODEC_OPCLK
				1010	-	MICDET
	11:8	GP6_FN [3:0]	Depends on status of CONF pins	GPIO6 function definition		
					Input	Output
				0000	GPIO	GPIO
				0001	L_PWR2	/MEMRST
				0010	FLASH	ADA
				0011	HIBERNATE (Edge)	RTC
				0100	HIBERNATE (Level)	MICDET
				0101	-	MICSHT
				0110	-	ADCLRCLKB
	15:12	GP7_FN [3:0]	Depends on status of CONF pins	GPIO7 function definition		
					Input	Output
				0000	GPIO	GPIO
				0001	L_PWR3	P_CLK
				0010	MASK	/VCCFAULT
				0011	HIBERNATE (Level)	/BATT_FAULT
				0100	-	MICDET
				0101	-	MICSHT
				0110	-	ADA
				1100	-	FLL_CLK
Note: Undocumented combinations for GP*n*_FN (n = 4 to 7) are reserved						

Table 127 GPIO Function Select 2

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R142 (8Eh) GPIO function select 3	3:0	GP8_FN [3:0]	Depends on status of CONF pins	GPIO8 function definition		
					Input (GP*n*_DIR=1)	Output (GP*n*_DIR=0)
				0000	GPIO	GPIO
				0001	/MR	/VCC_FAULT
				0010	ADCBCLK	ADCBCLK
				0011	PWR_OFF	/BATT_FAULT
				0100	HIBERNATE (Edge)	/RST
	7:4	GP9_FN [3:0]	Depends on status of CONF pins	GPIO9 function definition		
					Input	Output
				0000	GPIO	GPIO
				0001	HEARTBEAT	/VCC_FAULT
				0010	MASK	LINE_GT_BATT
				0011	PWR_OFF	/BATT_FAULT
				0100	HIBERNATE (Level)	/MEMRST
	11:8	GP10_FN [3:0]	Depends on status of CONF pins	GPIO10 function definition		
					Input	Output
				0000	GPIO	GPIO
				0001	-	ISINKC
				0010	-	LINE_GT_BATT
				0011	PWR_OFF	CH_IND
	15:12	GP11_FN [3:0]	Depends on status of CONF pins	GPIO11 function definition		
					Input	Output
				0000	GPIO	GPIO
				0001	-	ISINKD
				0010	/WAKEUP	LINE_GT_BATT
				0011	-	CH_IND
Note: Undocumented combinations for GPn_FN (n = 8 to 11) are reserved						

Table 128 GPIO Function Select 3

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R143 (8Fh) GPIO function select 4	3:0	GP12_FN [3:0]	Depends on status of CONF pins	GPIO 12 function definition		
					Input (GP*n*_DIR=1)	Output (GP*n*_DIR=0)
				0000	GPIO	GPIO
				0001	CHIP_RESET	ISINKE
				0010	-	LINE_GT_BATT
				0011	-	LINE_SW
				0100	-	32kHz
Note: Undocumented combinations are reserved						

Table 129 GPIO Function Select 4

21 VOLTAGE REFERENCES

The WM8351 generates several reference voltages used for different purposes.

The main reference voltage VREF, and additional internal references derived from it, are used in the DC-DC converters, the LDO regulators and the auxiliary ADC. VREF is highly stable, accurate, and independent of the supply voltage. It can be trimmed for improved accuracy.

The VRTC regulator (see Section 17.5) uses a separate, low-power reference at start-up.

The mid-rail reference VMID is used in the audio CODEC. It is generated from AVDD.

Each reference voltage is internally provided to those parts of the WM8351 where it is needed.

21.1 MAIN REFERENCE (VREF)

The main reference generates a highly accurate reference voltage VREF. It requires a decoupling capacitor on the C_REF pin; a 2.2uF X5R capacitor is recommended, as noted in Section 29.2; and an accurate resistor on the R_REF pin; a 100kΩ (1%) resistor is recommended, as noted in Section 29.2.

The WM8351 will malfunction if those components are omitted.

The accuracy of supply voltages generated by the WM8351 depends on VREF, and can be improved by trimming. This scales VREF by up to +15/-16% in 1% steps, to compensate for deviations from the nominal value.

The main reference can be overdriven with an externally generated reference voltage, if desired.

21.2 LOW-POWER REFERENCE

The low-power reference determines the accuracy of VRTC on start-up. Once the main bandgap has been trimmed and has settled VRTC switches across to the main bandgap for greater accuracy.

22 REAL-TIME CLOCK (RTC)

22.1 GENERAL DESCRIPTION

The WM8351 contains a Real Time Clock (RTC), which maintains the current date and time, and also has the capability to generate alarms and periodic interrupt signals. The RTC is powered by the backup supply (VRTC), in order that it can keep running when the normal power sources are unavailable.

The RTC uses the 32.768kHz clock generated by the on-chip crystal oscillator. To compensate for errors in this clock frequency, the RTC includes a frequency trim option. Alternatively the RTC can be clocked from external 32.768kHz input on a GPIO pin configured as 32kHz input. See Section 12.2 for details of the 32kHz oscillator control.

22.2 RTC CONTROL

22.2.1 MODES OF OPERATION

The Real Time Clock is enabled when RTC_TICK_ENA is set to 1. (This is the default setting.) See Table 135 for the definition of this RTC_TICK_ENA.

The RTC can operate as a 24-hour clock or else as a 12-hour clock with a separate AM/PM flag bit. The RTC time register fields can be treated as BCD (binary-coded decimal) or as binary data formats. These options are selected as described in Table 130.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) RTC Time control	15	RTC_BCD	0	RTC Coding (applies to all time registers) 0 = Binary 1 = BCD
	14	RTC_12HR	0	RTC 12/24 hours mode 1 = 12 hours (MSB of RTC_HRS indicates AM/PM) 0 = 24 hours (MSB of RTC_HRS is 0)

Table 130 RTC Modes of Operation

22.2.2 RTC TIME REGISTERS

The current time and date are held in registers R16 to R19, as described in Table 131.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (10h) RTC sec / min	14:8	RTC_MINS [6:0]	000 0000	Minutes; 0 to 59
	6:0	RTC_SECS [6:0]	000 0000	Seconds; 0 to 59
R17 (11h) RTC hour / day	10:8	RTC_DAY [2:0]	1	Day of the week; 1 to 7, 1 = Sunday
	5	RTC_HPM	0	RTC Hours AM/PM flag 0 = AM 1 = PM Only valid in 12hour mode.
	4:0	RTC_HRS [4:0]	0 0000	Hours register with 0-23 range in 24hour mode and 1-12 in 12 hour mode.
R18 (12h) RTC date	12:8	RTC_MTH [5:0]	0_0001	Month register with range 1-12.
	5:0	RTC_DATE [5:0]	00_0001	Date register with range 1-31.
R19 (13h) RTC year	13:8	RTC_YHUNDREDS [6:0]	01_0100	Year hundreds register tied to 20(dec)
	7:0	RTC_YUNITS [7:0]	0000_0000	Year units register with range 0-99.

Table 131 RTC Time Registers

The current time can be read from the registers defined above. As the content of the time registers changes every second, a single register read, executed at an arbitrary time, does not guarantee an accurate time reading. Two possible methods are recommended for reliable reading of the time registers:

- Read after interrupt: the RTC_SEC interrupt (see Section 22.5) indicates that the seconds counter has just been incremented, and that the RTC registers will not change again within the next 999ms. A register read executed immediately after an RTC_SEC interrupt can therefore be taken as an accurate time reading.
- Two consecutive reads: if two consecutive reads within a short time (less than 1s apart) return the same result, this can be taken as an accurate reading. If the two results differ, the procedure should be repeated.

22.2.3 SETTING THE TIME

When writing to the RTC time registers, the seconds counter should first be stopped in order to prevent glitches. The following procedure should be used:

- Set the RTC_SET bit to stop seconds counter
- Read the RTC_STS bit. Repeat this step until RTC_STS=1
- Set new time in Registers R16 to R19
- Clear the RTC_SET bit to re-enable seconds counter.

The RTC_SET and RTC_STS bits are defined in Table 132.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) RTC Time control	11	RTC_SET	0	Stops RTC seconds counter (instruction only) 0 = normal operation 1 = stop counter
	10	RTC_STS	0	Status of RTC seconds counter 0 = normal operation 1 = counter stopped

Table 132 Setting the RTC Time

22.2.4 RTC ALARM REGISTERS

An RTC Alarm can be set by writing to the control fields in registers R20 to R22, which are in a similar format to the RTC Time registers.

Setting any of these fields to “All 1’s” results in that field being a “don’t care” field. For example, setting the RTC_ALMDAY field to 0001 determines that the alarm is set for a Sunday, whilst setting RTC_ALMDAY to 1111 results in the programmed alarm occurring on every day of the week.

When the RTC Alarm time/date fields match the RTC time, the alarm event is signalled by the WM8351 raising the RTC_ALM_EINT interrupt. See Section 22.5 for further details.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) ALARM sec / min	14:8	RTC_ALMMINS [6:0]	000_0000	Minutes alarm register with range 0-59. All 1's sets to 'don't care' state. Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.
	6:0	RTC_ALMSECS [6:0]	000_0000	Seconds alarm register with range 0-59. All 1's set to 'don't care' state. Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.
R21 (15h) ALARM hour / day	11:8	RTC_ALMDAY [3:0]	0000	Day alarm register, with range 1-7, 1 = Sunday. All 1's sets to 'don't care' state. Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.
	5	RTC_ALMHPM	0	Alarm hours AM/PM flag 0 = AM 1 = PM Only applicable in 12 hour mode. In 24 hour mode set to 1 if RTC_ALMHRS is set to all 1's 'don't care' or 0 otherwise.
	4:0	RTC_ALMHRS [4:0]	0_0000	Hours alarm register with range 0-23 in 24 hours mode and 1-12 in 12 hour. In 12 hour mode bit 5 is used as PM/not-AM flag. All 1's sets to 'don't care' state. Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.
R22 (16h) ALARM date	12:8	RTC_ALMMTH [4:0]	0_0000	Month alarm register with range 1-12. All 1's sets to 'don't care' state.
	5:0	RTC_ALMDATE [5:0]	00_0000	Date alarm register with range 1-31. All 1's sets to 'don't care' state.

Table 133 RTC Alarm Registers

The "don't care" option (all bits set to 1) provides extra flexibility for programming ALARM duration and recurrent alarms. For example:

- Setting only RTC_ALMSEC to "don't care" produces an alarm lasting 1 minute.
- Setting only RTC_ALMDATE to "don't care" produces an alarm lasting 1 second that recurs once a week, on the day determined by RTC_ALMDAY, during the month determined by RTC_ALMMTH.
- Setting RTC_ALMSEC, RTC_ALMDATE, RTC_ALMDAY and RTC_ALMMTH to "don't care" produces a daily alarm lasting 1 minute.

22.2.5 SETTING THE ALARM

Writing to the RTC Alarm registers requires a procedure similar to that used when setting RTC time, in order to prevent accidental alarms being triggered:

- Set the RTC_ALMSET bit to disable alarms
- Read the RTC_ALMSTS bit. Repeat this step until RTC_ALMSTS=1
- Set new RTC Alarm in Registers R20 to R22
- Clear the RTC_ALMSET bit to re-enable RTC Alarm

The RTC_ALMSET and RTC_ALMSTS bits are defined in Table 134.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) RTC Time control	9	RTC_ALMSET	1	Stops alarms (instruction only) 0 = normal operation 1 = stop alarms It is recommended to stop alarms when setting the RTC alarm. This avoids false alarms.
	8	RTC_ALMSTS	1	Actual status of ALARM circuitry 0 = normal operation 1 = alarms stopped

Table 134 Setting the RTC Alarm

22.3 TRIMMING THE RTC

The RTC has a frequency trim feature to allow compensation for known and constant errors in the crystal oscillator frequency up to ±8Hz. Programming the frequency trim requires a procedure similar to that used when setting RTC and ALARM time:

- Clear the RTC_TICK_ENA bit to disable the 1 second tick generator
- Read the RTC_TICKSTS bit. Repeat this step until RTC_TICKSTS=1
- Set new RTC frequency trim value in Register R218
- Set the RTC_TICK_ENA bit to resume normal operation

The applicable register bits are defined in Table 135.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) Power Mgmt (5)	11	RTC_TICK_ENA	1	Enable RTC counting (instruction only) 0 = disabled 1 = enabled *Protected by security key.*
R218 (DAh) RTC Tick Control	15			
	14	RTC_TICKSTS	0	Status of tick request. This bit can be used to ensure the RTC is using the value of RTC_TICK_ENA. 0 = disabled 1 = enabled *Protected by security key.*
	9:0	RTC_TRIM [9:0]	00_0000_0000	RTC frequency trim. Used to adjust the count value of the Tick Gen block to compensate for crystal inaccuracies. RTC frequency trim is a 10bit fixed point <4,6> 2's complement number. MSB Scaling = -8Hz. The register indicates the error (in Hz) with respect to the ideal 32768Hz) of the input crystal frequency. e.g.: Actual crystal freq: 32769.00Hz: Required trim 0xb0001_000000 (+1.000000) Actual crystal freq: 32767.00Hz: Required trim 0xb1111_000000 (-1.000000) Actual crystal freq: 32775.58Hz: Required trim 0xb0111_100101 (+7.578125) Actual crystal freq: 32763.78Hz: Required trim 0xb1011_110010 (-4.218750) *Protected by security key.*
Note: RTC_TICK_ENA can be accessed through R12 or through R218. Reading from or writing to either register location has the same effect.				

Table 135 Controlling the RTC Frequency Trim

22.4 RTC GPIO OUTPUT

It is possible to configure GPIO6 as an RTC output, as described in Section 20. This output is a square wave that is derived from the trimmed RTC counter. The frequency can be set to values between 1Hz and 16.384kHz, as described in Table 136.

Note that, when RTC_TRIM is used to calibrate the crystal oscillator, the nominal 50% duty ratio of this output may deviate by up to 8 clock periods of the 32.768kHz oscillator on the occasions when the RTC Seconds Counter is increased (ie. once per second).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) RTC Time control	3:0	RTC_DSW [3:0]	0000	Divided Square wave select. 0000 = disabled 0001 = 1Hz 0010 = 2Hz … 1011 = 1024Hz 1100 = 2048Hz 1101 = 4096Hz 1110 = 8192Hz 1111 = 16384Hz Note: due to trim settings for crystal intolerances a single square wave period during seconds rollover may be decrease its on time period or increase its off time period by up to 8 32kHz periods.

Table 136 RTC GPIO Output

22.5 RTC INTERRUPTS

The RTC has its own first-level interrupt, RTC_INT (see Section 24). This comprises three second-level interrupts which indicate periodic events or RTC Alarm conditions.

The RTC raises an RTC_SEC_EINT interrupt on every 1 second rollover. An additional periodic interrupt, RTC_PER_EINT, is configurable with a frequency determined by the RTC_PINT field, as defined in Table 138. The RTC_ALM_EINT interrupt is triggered by the RTC Alarm function, as described in Section 22.2.4.

These interrupts can be individually masked by setting the applicable mask bit(s) as described in Table 137.

ADDRESS	BIT	LABEL	DESCRIPTION
R25 (19h) Interrupt Status 1	7	RTC_PER_EINT	RTC periodic interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	6	RTC_SEC_EINT	RTC 1s rollover complete (1Hz tick). (Rising Edge triggered) Note: This bit is cleared once read.
	5	RTC_ALM_EINT	RTC alarm signalled. (Rising Edge triggered) Note: This bit is cleared once read.
R33 (21h) Interrupt Status 1 Mask	7:5	"IM_" + name of respective bit in R25	Each bit in R33 enables or masks the corresponding bit in R25. The default value for these bits is 0 (unmasked).

Table 137 RTC Interrupts

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) RTC Time control	6:4	RTC_PINT [2:0]	010	Selects frequency of periodic interrupt output pulse (32kHz period duration) as shown below. When set time status is high, the periodic output is disabled. 000 = disabled 001 = 1 sec 010 = 1 min 011 = 1 hour 100 = 1 day 101 = 1 month 11x = disabled

Table 138 Configuring RTC Periodic Interrupts

23 WATCHDOG TIMER

The WM8351 includes a watchdog timer designed to detect a possible software fault condition where the host processor has locked up. The watchdog timer checks for any write operation to the watchdog control register R4 (04h) or receipt of a heartbeat signal from the host processor on GPIO9 (see Section 20). If neither event occurs within a programmable time, this is interpreted as a fault in the host processor. The watchdog timer then raises an interrupt and/or generates a system reset; the desired response to a watchdog timeout is set using the WDOG_MODE register field.

If GPIO9 is configured as HEARTBEAT input (GP9_FN = 0001, GP9_DIR = 1), then the Watchdog Timer can only be reset by a rising logic level applied to the GPIO9 pin.

If GPIO9 is not configured as HEARTBEAT input, then the Watchdog Timer can only be reset by a write operation to the watchdog control register R4 (04h).

If a System reset is triggered by the watchdog timeout, the WM8351 asserts the /RST pin and the /RST and /MEMRST (GPIO) reset signals, resets the internal control registers and then initiates a start-up sequence. If the watchdog timeout fault persists, then a maximum of 7 reset attempts will be made. If the watchdog timeout occurs more than 7 times, the WM8351 will remain in the OFF state until the next valid ON state transition event occurs.

The watchdog timer can be halted for debug purposes using the WDOG_DEBUG bit. The watchdog can be disabled in Hibernate mode using the WDOG_HIB_MODE bit. The watchdog timer duration is set using WDOG_TO, as described in Table 139.

The Watchdog timeout interrupt event is indicated by the SYS_WDOG_TO_EINT register field. This is one of the second-level interrupts which triggers a first-level System Interrupt, SYS_INT (see Section 24). This can be masked by setting the mask bit as described in Table 140.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) System control 1	7	WDOG_DEBUG	0	Halts watchdog timer for system debugging 0 = normal operation 1 = WDOG halt
R4 (04h) System control 2	7	WDOG_HIB_MODE	0	Watchdog behaviour in HIBERNATE state 0 = WDOG disabled in Hibernate 1 = WDOG controlled by WDOG_MODE in Hibernate
	5:4	WDOG_MODE [2:0]	Dependant on CONFIG settings	Watchdog mode 00 = Disabled 01 = SYS_WDOG_TO interrupt on time-out 10 = WKUP_WDOG_RST interrupt and System reset on time-out 11 = SYS_WDOG_TO interrupt on first time-out, WKUP_WDOG_RST interrupt and System reset on second time-out. *Protected by security key.*
	2:0	WDOG_TO [2:0]	101	Watchdog timeout (seconds) The timer is reset to this value when a HEARTBEAT signal edge is detected or the host writes to the watchdog control register. 000 = 0.125s … (time doubles with each step) 101 = 4s 11x = Reserved *Protected by security key.*
R5 (05h) System Hibernate	7	WDOG_HIB_MODE	0	Watchdog behaviour in HIBERNATE state 0 = WDOG disabled in Hibernate 1 = WDOG controlled by WDOG_MODE in Hibernate
Note: WDOG_HIB_MODE can be accessed through R4 or through R5. Reading from or writing to either register location has the same effect.				

Table 139 Controlling the Watchdog Timer

ADDRESS	BIT	LABEL	DESCRIPTION
R26 (1Ah) Interrupt Status 2	0	SYS_WDOG_TO_EINT	Watchdog timeout has occurred. (Rising Edge triggered) Note: This bit is cleared once read.
R34 (22h) Interrupt Status 2 Mask	0	IM_SYS_WDOG_TO_EINT	Mask bit for Watchdog timer interrupt When set to 1, IM_SYS_WDOG_TO_EINT masks SYS_WDOG_TO_EINT in R26 and does not trigger an SYS_INT interrupt when SYS_WDOG_TO_EINT is set).

Table 140 Watchdog Timer Interrupts

Note that, if GPIO9 is configured as VCC_FAULT output (GP9_FN = 0001, GP9_DIR = 0), then the Watchdog Timer will be configured to expect a HEARTBEAT reset trigger. In this configuration, the Watchdog Reset will never occur and the system may lock up if the Watchdog Mode is enabled.

The Watchdog Timer function cannot be supported if GPIO9 is configured as VCC_FAULT output. Either the GPIO9 must be reconfigured as some other function, or the Watchdog Timer must remain disabled.

Note that Config Mode 01 selects GPIO9 = VCC_FAULT by default.

24 INTERRUPT CONTROLLER

The WM8351 can send an interrupt signal to the host processor though the IRQ pin. Interrupts can alert the host to a wide range of events and fault conditions. Each of these can be individually enabled or masked. After receiving an interrupt, the host processor can read the interrupt registers in order to determine what caused the interrupt, and take appropriate action if required.

The WM8351 interrupt controller has two levels:

Second-level interrupts indicate a single event in one of the circuit blocks. This is indicated by setting a register bit. This bit is a “sticky” bit - once it is set, it remains at logic 1 until the host processor reads the register. When the processor reads the register, the interrupt bits in that register are cleared. First-level interrupts are the logical OR of several second-level interrupts (usually all the interrupts associated with one particular circuit block). The default polarity of IRQ is active low, meaning that the IRQ signal is the logical NOR of all first-level interrupts.

Individual second-level interrupt bits can be masked, which prevents them from setting the First-level interrupt. (Note that the “sticky” bit will be set as normal, even if that interrupt is masked.)

Individual first-level interrupts can also be masked, preventing them from asserting the IRQ output.

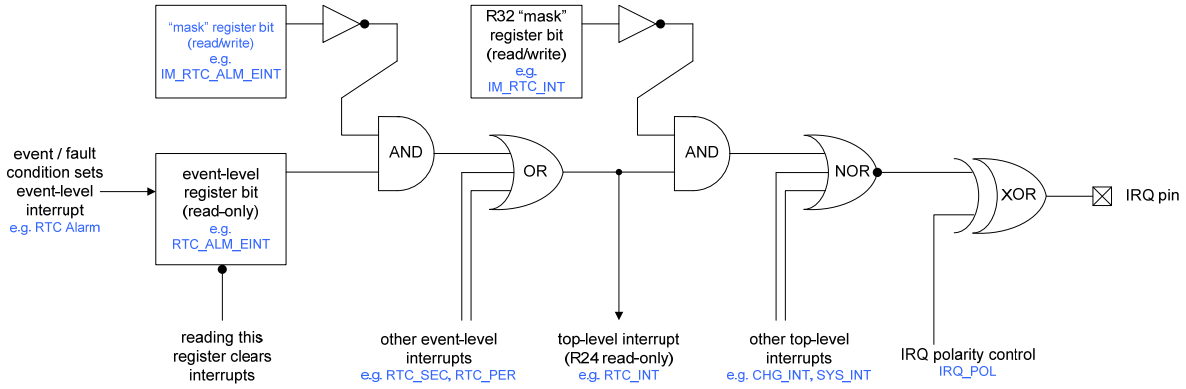


Figure 80 Interrupt Equivalent Logic

To find the cause of an interrupt signal, the host processor should first read the first-level interrupt register R24 to locate the circuit blocks(s) where the interrupt originated; after that, the precise cause(s) of the interrupt can be determined by reading the second-level interrupt register(s) as appropriate to the indicated first-level interrupt event.

24.1 CONFIGURING THE IRQ PIN

The default polarity of IRQ is active low; this can be changed to active high if desired, by writing to the IRQ_POL bit.

When the WM8351 is in the HIBERNATE state, interrupts can be disabled or can remain active. The desired behaviour can be selected using the IRQ_HIB_MODE bit.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) System Control 1	0	IRQ_POL	0	IRQ pin polarity 0 = active low (/IRQ) 1 = active high (IRQ)
R5 (05h) System Hibernate	3	IRQ_HIB_MODE	0	IRQ pin state in hibernate mode 0 = Normal operation 1 = Forced to indicate there is no IRQ.

Table 141 Interrupts in HIBERNATE State

24.2 FIRST LEVEL INTERRUPTS

Each first level interrupt has a status bit in Register R24, which can be read to determine the origin of an IRQ event. Each of these bits may be masked by setting the corresponding field in Register R32.

ADDRESS	BIT	LABEL	DESCRIPTION
R24 (18h) System Interrupts	13	OC_INT	First-level over-current interrupt. Note: This bit is cleared once read.
	12	UV_INT	First-level under-voltage interrupt. Note: This bit is cleared once read.
	9	CS_INT	First-level current sink interrupt. Note: This bit is cleared once read.
	8	EXT_INT	First-level external interrupt. Note: This bit is cleared once read.
	7	CODEC_INT	First-level codec interrupt. Note: This bit is cleared once read.
	6	GP_INT	First-level GPIO interrupt. Note: This bit is cleared once read.
	5	AUXADC_INT	First-level AUXADC comparator interrupt. Note: This bit is cleared once read.
	4	RTC_INT	First-level RTC interrupt. Note: This bit is cleared once read.
	3	SYS_INT	First-level system interrupt. Note: This bit is cleared once read.
	2	CHG_INT	First-level charger interrupt. Note: This bit is cleared once read.
	1	USB_INT	First-level USB interrupt. Note: This bit is cleared once read.
	0	WKUP_INT	First-level wakeup interrupt. Note: This bit is cleared once read.
R32 (20h) System Interrupt Mask	13:0	"IM_" + name of respective bit in R25	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R32 enables or masks the corresponding bit in R24. The default value for these bits is 1 (masked)
Note: Register is R24 is read-only.			

Table 142 First Level Interrupt Status and Mask Bits

24.3 SECOND-LEVEL INTERRUPTS

The following sections define the second-level interrupt status and control bits associated with each of the first-level bits defined in Table 142.

24.3.1 OVERCURRENT INTERRUPTS

The first-level OC_INT interrupt comprises one second-level interrupt for the limit switch. This status bit is in Register R29 and its mask bit is in Register R37, as defined in Table 143.

ADDRESS	BIT	LABEL	DESCRIPTION
R29 (1Dh) Over Current Interrupt Status	15	OC_LS_EINT	Limit Switch Over-current interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R37 (25h) Over Current Interrupt Mask	15	IM_OC_LS_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. When IM_OC_LS_EINT is set to 1, then OC_LS_EINT in R29 does not trigger an OC_INT interrupt when set. The default value is 0 (unmasked).

Table 143 Over-Current Interrupts

24.3.2 UNDERVOLTAGE INTERRUPTS

The first-level UV_INT interrupt comprises several second-level interrupts for the DC-DCs and LDOs. Each of these has a status bit in Register R28 and a mask bit in Register R36, as defined in Table 144.

ADDRESS	BIT	LABEL	DESCRIPTION
R28 (1Ch) Under Voltage Interrupt Status	11	UV_LDO4_EINT	LDO4 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	10	UV_LDO3_EINT	LDO3 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	9	UV_LDO2_EINT	LDO2 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	8	UV_LDO1_EINT	LDO1 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	3	UV_DC4_EINT	DCDC4 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	2	UV_DC3_EINT	DCDC3 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	1	UV_DC2_EINT	DCDC2 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	0	UV_DC1_EINT	DCDC1 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R36 (24h) Under Voltage Interrupt Mask	11:0	"IM_" + name of respective bit in R28	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R36 enables or masks the corresponding bit in R28. The default value for these bits is 0 (unmasked).

Table 144 Under Voltage Interrupts

24.3.3 CURRENT SINK (LED DRIVER) INTERRUPTS

The first-level CS_INT interrupt comprises one second-level interrupt for the Current Sink functions. This status bit is in Register R26 and its mask bit is in Register R34, as defined in Table 145.

ADDRESS	BIT	LABEL	DESCRIPTION
R26 (1Ah) Interrupt Status 2	13	CS1_EINT	Flag to indicate drain voltage can no longer be regulated and output current may be out of spec. (Rising Edge triggered) Note: This bit is cleared once read.
R34 (22h) Interrupt Status 2 Mask	13	IM_CS1_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. When IM_CS1_EINT is set to 1, then CS1_EINT in R26 does not trigger a CS_INT interrupt when set. The default value is 0 (unmasked).

Table 145 Current Sink Interrupts

24.3.4 EXTERNAL INTERRUPTS

The first-level EXT_INT interrupt comprises three second-level interrupts for USB, Wall and Battery supply status. Each of these has a status bit in Register R31 and a mask bit in Register R37, as defined in Table 146. These flags are triggered on the rising and falling edges of the interrupt events.

ADDRESS	BIT	LABEL	DESCRIPTION
R31 (1Fh) Comparator Interrupt Status	15	EXT_USB_FB_EINT	USB_FB changed interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
	14	EXT_WALL_FB_EINT	WALL_FB changed interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
	13	EXT_BATT_FB_EINT	BATT_FB changed interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
R39 (27h) Comparator Interrupt Status Mask	15:13	"IM_" + name of respective bit in R31	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R39 enables or masks the corresponding bit in R31. The default value for these bits is 0 (unmasked).

Table 146 External Interrupts

24.3.5 CODEC INTERRUPTS

The first-level CODEC_INT interrupt comprises four second-level interrupts for the CODEC. Each of these has a status bit in Register R31 and a mask bit in Register R39, as defined in Table 147. These flags are triggered on the rising and falling edges of the interrupt events.

ADDRESS	BIT	LABEL	DESCRIPTION
R31 (1Fh) Comparator Interrupt Status	11	CODEC_JCK_DET_L_EINT	Left channel Jack detection interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
	10	CODEC_JCK_DET_R_EINT	Right channel Jack detection interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
	9	CODEC_MICSCD_EINT	Mic short-circuit detect interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
	8	CODEC_MICD_EINT	Mic detect interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.
R39 (27h) Comparator Interrupt Status Mask	11:8	"IM_" + name of respective bit in R31	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R39 enables or masks the corresponding bit in R31. The default value for these bits is 0 (unmasked).

Table 147 CODEC Interrupts

24.3.6 GPIO INTERRUPTS

The first-level GP_INT interrupt comprises several second-level interrupts for the 13 GPIO pins. Each of these has a status bit in Register R30 and a mask bit in Register R35, as defined in Table 148.

ADDRESS	BIT	LABEL	DESCRIPTION
R30 (1Eh) GPIO Interrupt Status	12	GP12_EINT	GPIO12 interrupt. (Trigger controlled by GP12 registers.) Note: This bit is cleared once read.
	11	GP11_EINT	GPIO11 interrupt. (Trigger controlled by GP11 registers.) Note: This bit is cleared once read.
	10	GP10_EINT	GPIO10 interrupt. (Trigger controlled by GP10 registers.) Note: This bit is cleared once read.
	9	GP9_EINT	GPIO9 interrupt. (Trigger controlled by GP9 registers.) Note: This bit is cleared once read.
	8	GP8_EINT	GPIO8 interrupt. (Trigger controlled by GP8 registers.) Note: This bit is cleared once read.
	7	GP7_EINT	GPIO7 interrupt. (Trigger controlled by GP7 registers.) Note: This bit is cleared once read.
	6	GP6_EINT	GPIO6 interrupt. (Trigger controlled by GP6 registers.) Note: This bit is cleared once read.
	5	GP5_EINT	GPIO5 interrupt. (Trigger controlled by GP5 registers.) Note: This bit is cleared once read.
	4	GP4_EINT	GPIO4 interrupt. (Trigger controlled by GP4 registers.) Note: This bit is cleared once read.
	3	GP3_EINT	GPIO3 interrupt. (Trigger controlled by GP3 registers.) Note: This bit is cleared once read.
	2	GP2_EINT	GPIO2 interrupt. (Trigger controlled by GP2 registers.) Note: This bit is cleared once read.
	1	GP1_EINT	GPIO1 interrupt. (Trigger controlled by GP1 registers.) Note: This bit is cleared once read.
	0	GP0_EINT	GPIO0 interrupt. (Trigger controlled by GP0 registers.) Note: This bit is cleared once read.
R38 (26h) GPIO Interrupt Mask	12:0	"IM_" + name of respective bit in R30	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R38 enables or masks the corresponding bit in R30. The default value for these bits is 0 (unmasked).

Table 148 GPIO Interrupts

24.3.7 AUXADC AND DIGITAL COMPARATOR INTERRUPTS

The first-level AUXADC_INT interrupt comprises several second-level interrupts for the auxiliary ADC and associated digital comparators. Each of these has a status bit in Register R26 and a mask bit in Register R34, as defined in Table 149.

ADDRESS	BIT	LABEL	DESCRIPTION
R26 (1Ah) Interrupt Status 2	8	AUXADC_DATARDY_EINT	Auxiliary data ready. (Rising Edge triggered) Note: This bit is cleared once read.
	7	AUXADC_DCOMP4_EINT	DCOMP4 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	6	AUXADC_DCOMP3_EINT	DCOMP3 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	5	AUXADC_DCOMP2_EINT	DCOMP2 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	4	AUXADC_DCOMP1_EINT	DCOMP1 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R34 (22h) Interrupt Status 2 Mask	8:4	"IM_" + name of respective bit in R26	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R34 enables or masks the corresponding bit in R26. The default value for these bits is 0 (unmasked).

Table 149 AUXADC Interrupts

24.3.8 RTC INTERRUPTS

The first-level RTC_INT interrupt comprises three second-level interrupts for the Real Time Clock. Each of these has a status bit in Register R25 and a mask bit in Register R33, as defined in Table 150.

ADDRESS	BIT	LABEL	DESCRIPTION
R25 (19h) Interrupt Status 1	7	RTC_PER_EINT	RTC periodic interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	6	RTC_SEC_EINT	RTC 1s rollover complete (1Hz tick). (Rising Edge triggered) Note: This bit is cleared once read.
	5	RTC_ALM_EINT	RTC alarm signalled. (Rising Edge triggered) Note: This bit is cleared once read.
R33 (21h) Interrupt Status 1 Mask	7:5	"IM_" + name of respective bit in R25	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R33 enables or masks the corresponding bit in R25. The default value for these bits is 0 (unmasked).

Table 150 RTC Interrupts

24.3.9 SYSTEM INTERRUPTS

The first-level SYS_INT interrupt comprises four second-level interrupts for various system events. Each of these has a status bit in Register R26 and a mask bit in Register R34, as defined in Table 151.

ADDRESS	BIT	LABEL	DESCRIPTION
R26 (1Ah) Interrupt Status 2	3	SYS_HYST_COMP_FAIL_EINT	Hysteresis comparator indication that LINE or BATT is less that shutdown threshold. (Rising Edge triggered) Note: This bit is cleared once read.
	2	SYS_CHIP_GT115_EINT	Chip over 115°C temp limit. (Rising Edge triggered) Note: This bit is cleared once read.
	1	SYS_CHIP_GT140_EINT	Chip over 140°C temp limit. (Rising Edge triggered) Note: This bit is cleared once read.
	0	SYS_WDOG_TO_EINT	Watchdog timeout has occurred. (Rising Edge triggered) Note: This bit is cleared once read.
R34 (22h) Interrupt Status 2 Mask	3:0	"IM_" + name of respective bit in R26	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R34 enables or masks the corresponding bit in R26 The default value for these bits is 0 (unmasked).

Table 151 System Interrupts

24.3.10 CHARGER INTERRUPTS

The system interrupt CHG_INT interrupt comprises several second-level interrupts for the battery charger. Each of these has a status bit in Register R25 and a mask bit in Register R33, as defined in Table 152.

ADDRESS	BIT	LABEL	DESCRIPTION
R25 (19h) Interrupt Status 1	15	CHG_BATT_HOT_EINT	Battery temp too hot. (Rising Edge triggered) Note: This bit is cleared once read.
	14	CHG_BATT_COLD_EINT	Battery temp too cold. (Rising Edge triggered) Note: This bit is cleared once read.
	13	CHG_BATT_FAIL_EINT	Battery fail. (Rising Edge triggered) Note: This bit is cleared once read.
	12	CHG_TO_EINT	Charger timeout. (Rising Edge triggered) Note: This bit is cleared once read.
	11	CHG_END_EINT	Charging final stage. (Rising Edge triggered) Note: This bit is cleared once read.
	10	CHG_START_EINT	Charging started. (Rising Edge triggered) Note: This bit is cleared once read.
	9	CHG_FAST_RDY_EINT	Indicates that the charger is ready to go into fast charge. (Rising Edge triggered) Note: This bit is cleared once read.

ADDRESS	BIT	LABEL	DESCRIPTION
	2	CHG_VBATT_LT_3P9_EINT	Battery Voltage < 3.9 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	1	CHG_VBATT_LT_3P1_EINT	Battery voltage < 3.1 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
	0	CHG_VBATT_LT_2P85_EINT	Battery voltage < 2.85 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R33 (21h) Interrupt Status 1 Mask	15:9 2:0	"IM_" + name of respective bit in R25	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R33 enables or masks the corresponding bit in R25. The default value for these bits is 0 (unmasked).

Table 152 Charger Interrupts

24.3.11 USB INTERRUPTS

The first-level USB_INT interrupt comprises one second-level interrupt for the USB limit switch. This status bit is in Register R26 and its mask bit is in Register R34, as defined in Table 153.

ADDRESS	BIT	LABEL	DESCRIPTION
R26 (1Ah) Interrupt Status 2	10	USB_LIMIT_EINT	USB Limit Switch interrupt. (Rising Edge triggered) Note: This bit is cleared once read.
R34 (22h) Interrupt Status 2 Mask	10	IM_USB_LIMIT_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. When IM_USB_LIMIT_EINT is set to 1, then USB_LIMIT_EINT in R26 does not trigger an USB_INT interrupt when set. The default value is 0 (unmasked).

Table 153 USB Interrupt

24.3.12 WAKE-UP INTERRUPTS

The first-level WKUP_INT interrupt comprises several second-level interrupts. After a system reset, these indicate to the host processor why the reset occurred. Each wake-up interrupt has a status bit in Register R31 and a mask bit in Register R30, as defined in Table 154.

ADDRESS	BIT	LABEL	DESCRIPTION
R31 (1Fh) Comparator Interrupt Status	6	WKUP_OFF_STATE_EINT	Indicates that the chip started from the OFF state. (Rising Edge triggered) Note: This bit is cleared once read.
	5	WKUP_HIB_STATE_EINT	Indicated the chip started up from the hibernate state. (Rising Edge triggered) Note: This bit is cleared once read.
	4	WKUP_CONV_FAULT_EINT	Indicates the wakeup was caused by a converter fault leading to the chip being reset. (Rising Edge triggered) Note: This bit is cleared once read.
	3	WKUP_WDOG_RST_EINT	Indicates the wakeup was caused by a watchdog heartbeat being missed, and hence the chip being reset. (Rising Edge triggered) Note: This bit is cleared once read.
	2	WKUP_GP_PWR_ON_EINT	PWR_ON (Alternate GPIO function) pin has been pressed for longer than specified time. (Rising Edge triggered) Note: This bit is cleared once read.
	1	WKUP_ONKEY_EINT	ON key has been pressed for longer than specified time. (Rising Edge triggered) Note: This bit is cleared once read.
	0	WKUP_GP_WAKEUP_EINT	WAKEUP (Alternate GPIO function) pin has been pressed for longer than specified time. (Rising Edge triggered) Note: This bit is cleared once read.
R39 (27h) Comparator Interrupt Status Mask	6:0	"IM_" + name of respective bit in R31	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Each bit in R39 enables or masks the corresponding bit in R31. The default value for these bits is 0 (unmasked).

Table 154 Wake-up Interrupts

25 TEMPERATURE SENSING

25.1 CHIP TEMPERATURE MONITORING

The WM8351 has a built-in sensor to monitor its internal temperature, with two levels of over-temperature protection.

When the device temperature exceeds the thermal warning temperature, the WM8351 raises a SYS_CHIP_GT115_EINT interrupt. If the chip temperature continues to rise, and exceeds the thermal shutdown temperature, the SYS_CHIP_GT140_EINT interrupt is set and the device shuts down. After a thermal shutdown, the WM8351 can only restart after its temperature has fallen below the restart temperature.

The associated register fields are defined in Table 155.

ADDRESS	BIT	LABEL	DESCRIPTION
R26 (1Ah) Interrupt Status 2	2	SYS_CHIP_GT115_EINT	Chip over 115°C temp limit. (Rising Edge triggered) Note: This bit is cleared once read.
	1	SYS_CHIP_GT140_EINT	Chip over 140°C temp limit. (Rising Edge triggered) Note: This bit is cleared once read.
R34 (22h) Interrupt Status 2 Mask	2:1	"IM_" + name of respective bit in R26	Each bit in R34 enables or masks the corresponding bit in R26. The default value for these bits is 0 (unmasked).

Table 155 Temperature Sensing Interrupts

26 REGISTER MAP

26.1 OVERVIEW

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8351 can be configured using the Control Interface. All registers not listed and all unused bits should be set to '0'.

Key to characters in brackets: K = protected by key, M = default in metal mask, R = read-only, W = write-only, O = read-only in ROM configs, D = protected by key in development mode, read-only otherwise, n = never reset, p = reset by POR only, s = reset by state machine, sd = reset by state machine except in dev mode, u = reset on UVLO, m = reset on /MEMRST

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R0 (0h)	Reset/ID	SW_RESET/CHIP_ID[15:0] *(n)*																6143h
R1 (1h)	ID	CHIP_REV[3:0]				CONF_STS[1:0]		0	0	CUST_ID[7:0]								0000h
R2 (2h)	Revision	0	0	0	0	0	0	0	0	MASK_REV[7:0]								0001h
R3 (3h)	System Control 1	CHIP_ON *(Ms)*	SYS_RST *(KMs)*	POWERCYCLE	VCC_FAULT_OV *(Ms)*	RSTB_TO[1:0] *(M)*		BG_SLEEP *(M)*	0	WDOG_DEBUG *(K)*	CHIP_RESET_ENA *(s)*	MEM_VALID *(m)*	CHIP_SET_UP	ON_DEB_T *(K)*	0	ON_POL *(KMs)*	IRQ_POL *(Ms)*	1C02h
R4 (4h)	System Control 2	USB_SUSPEND_8MA *(M)*	USB_SUSPEND *(M)*	USB_MSTR *(Ms)*	USB_MSTR_SRC *(Ms)*	USB_MSTR_500MA *(Ms)*	USB_NOLIM	USB_SLV_500MA *(Ms)*	0	WDOG_HIB_MODE	0	WDOG_MODE[1:0] *(KMs)*		0	WDOG_TO[2:0] *(K)*			0004h 0204h 0214h 0204h
R5 (5h)	System Hibernate	HIBERNATE *(Ms)*	0	0	0	0	0	0	0	WDOG_HIB_MODE	HIB_STARTUP_SEQ	REG_RESET_HIB_MODE	RST_HIB_MODE	IRQ_HIB_MODE	MEMRST_HIB_MODE	PCCOMP_HIB_MODE	TEMPMON_HIB_MODE	0000h
R6 (6h)	Interface Control	USE_DEV_PINS *(s)*	DEV_ADDR[1:0] *(s)*		CONFIG_DONE *(s)*	RECONFIG_AT_ON	0	AUTOINC *(s)*	0	0	0	0	0	SPI_CFG *(KM)*	SPI_4WIRE *(KM)*	SPI_3WIRE *(KM)*	0	8A00h
R8 (8h)	Power mgmt (1)	CODEC_ISEL[1:0]		VBUF_ENA	0	0	OUTPUT_DRAIN_ENA	0	MIC_DET_ENA	0	0	BIAS_ENA	MICB_ENA	0	VMID_ENA	VMID[1:0]		8000h
R9 (9h)	Power mgmt (2)	0	0	0	0	IN3R_ENA	IN3L_ENA	INR_ENA	INL_ENA	MIXINR_ENA	MIXINL_ENA	OUT4_ENA	OUT3_ENA	0	0	MIXOUTR_ENA	MIXOUTL_ENA	0000h
R10 (Ah)	Power mgmt (3)	0	0	0	0	0	0	0	0	IN3R_TO_OUT2R	0	0	0	OUT2R_ENA	OUT2L_ENA	OUT1R_ENA	OUT1L_ENA	0000h
R11 (Bh)	Power mgmt (4)	0	SYSCLK_ENA	ADC_HPF_ENA	0	FLL_ENA	FLL_OSC_ENA	0	TOCLK_ENA	0	0	DACR_ENA	DACL_ENA	ADCR_ENA	ADCL_ENA	0	0	2000h
R12 (Ch)	Power mgmt (5)	0	0	0	CODEC_ENA *(s)*	RTC_TICK_ENA *(KMs)*	OSC32K_ENA *(KMs)*	CHG_ENA *(KMs)*	SW_VRTC_ENA *(s)*	AUXADC_ENA *(s)*	0	0	0	DCMP4_ENA *(s)*	DCMP3_ENA *(s)*	DCMP2_ENA *(s)*	DCMP1_ENA *(s)*	0E00h
R13 (Dh)	Power mgmt (6)	LS_ENA *(Ms)*	0	0	0	LDO4_ENA *(Ms)*	LDO3_ENA *(Ms)*	LDO2_ENA *(Ms)*	LDO1_ENA *(Ms)*	0	0	0	0	DC4_ENA *(Ms)*	DC3_ENA *(Ms)*	DC2_ENA *(Ms)*	DC1_ENA *(Ms)*	0000h
R14 (Eh)	Power mgmt (7)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CS1_ENA *(s)*	0000h
R16 (10h)	RTC Seconds/Minutes	0	RTC_MINS[6:0]							0	RTC_SECS[6:0]							0000h
R17 (11h)	RTC Hours/Day	0	0	0	0	0	RTC_DAY[2:0]			0	0	RTC_HPM	RTC_HRS[4:0]					0100h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R18 (12h)	RTC Date/Month	0	0	0	RTC_MTH[4:0]					0	0	RTC_DATE[5:0]						0101h
R19 (13h)	RTC Year	0	0	RTC_YHUNDREDS[5:0]						RTC_YUNITS[7:0]								1400h
R20 (14h)	Alarm Seconds/Minutes	0	RTC_ALMMINS[6:0]							0	RTC_ALMSECS[6:0]							0000h
R21 (15h)	Alarm Hours/Day	0	0	0	0	RTC_ALMDAY[3:0]				0	0	RTC_ALMHPM	RTC_ALMHRS[4:0]					0000h
R22 (16h)	Alarm Date/Month	0	0	0	RTC_ALMMTH[4:0]					0	0	RTC_ALMDATE[5:0]						0000h
R23 (17h)	RTC Time Control	RTC_BCD	RTC_12HR	0	0	RTC_SET	RTC_STS	RTC_ALMSET	RTC_ALMSTS	0	RTC_PINT[2:0]			RTC_DSW[3:0]				0320h
R24 (18h)	System Interrupts	0	0	OC_INT	UV_INT	0	0	CS_INT	EXT_INT	CODEC_INT	GP_INT	AUXADC_INT	RTC_INT	SYS_INT	CHG_INT	USB_INT	WKUP_INT	0000h
R25 (19h)	Interrupt Status 1	CHG_BATT_HOT_EINT	CHG_BATT_COLD_EINT	CHG_BATT_FAIL_EINT	CHG_TO_EINT	CHG_END_EINT	CHG_START_EINT	CHG_FAST_RDY_EINT	0	RTC_PER_EINT	RTC_SEC_EINT	RTC_ALM_EINT	0	0	CHG_VBATT_LT_3P9_EINT	CHG_VBATT_LT_3P1_EINT	CHG_VBATT_LT_2P85_EINT	0000h
R26 (1Ah)	Interrupt Status 2	0	0	CS1_EINT	0	0	USB_LIMIT_EINT	0	AUXADC_DATARDY_EINT	AUXADC_DCOMP4_EINT	AUXADC_DCOMP3_EINT	AUXADC_DCOMP2_EINT	AUXADC_DCOMP1_EINT	SYS_HYST_COMP_FAIL_EINT	SYS_CHIP_GT115_EINT	SYS_CHIP_GT140_EINT	SYS_WDOG_TO_EINT	0000h
R28 (1Ch)	Under Voltage Interrupt status	0	0	0	0	UV_LDO4_EINT	UV_LDO3_EINT	UV_LDO2_EINT	UV_LDO1_EINT	0	0	0	0	UV_DC4_EINT	UV_DC3_EINT	UV_DC2_EINT	UV_DC1_EINT	0000h
R29 (1Dh)	Over Current Interrupt status	OC_LS_EINT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R30 (1Eh)	GPIO Interrupt Status	0	0	0	GP12_EINT	GP11_EINT	GP10_EINT	GP9_EINT	GP8_EINT	GP7_EINT	GP6_EINT	GP5_EINT	GP4_EINT	GP3_EINT	GP2_EINT	GP1_EINT	GP0_EINT	0000h
R31 (1Fh)	Comparator Interrupt Status	EXT_USB_FB_EINT	EXT_WALL_FB_EINT	EXT_BATT_FB_EINT	0	CODEC_JCK_DET_L_EINT	CODEC_JCK_DET_R_EINT	CODEC_MICSCD_EINT	CODEC_MICD_EINT	0	WKUP_OFF_STATE_EINT	WKUP_HIB_STATE_EINT	WKUP_CONV_FAULT_EINT	WKUP_WDOG_RST_EINT	WKUP_GP_PWR_ON_EINT	WKUP_ONKEY_EINT	WKUP_GP_WAKEUP_EINT	0000h
R32 (20h)	System Interrupts Mask	0	0	IM_OC_INT *(Ms)*	IM_UV_INT *(Ms)*	0	0	IM_CS_INT *(Ms)*	IM_EXT_INT *(Ms)*	IM_CODEC_INT *(Ms)*	IM_GP_INT *(Ms)*	IM_AUXADC_INT *(Ms)*	IM_RTC_INT *(Ms)*	IM_SYS_INT *(Ms)*	IM_CHG_INT *(Ms)*	IM_USB_INT *(Ms)*	IM_WKUP_INT *(Ms)*	3FFFh
R33 (21h)	Interrupt Status 1 Mask	IM_CHG_BATT_HOT_EINT *(s)*	IM_CHG_BATT_COLD_EINT *(s)*	IM_CHG_BATT_FAIL_EINT *(s)*	IM_CHG_TO_EINT *(s)*	IM_CHG_END_EINT *(s)*	IM_CHG_START_EINT *(s)*	IM_CHG_FAST_RDY_EINT *(s)*	0	IM_RTC_PER_EINT *(s)*	IM_RTC_SEC_EINT *(s)*	IM_RTC_ALM_EINT *(s)*	0	0	IM_CHG_VBATT_LT_3P9_EINT *(s)*	IM_CHG_VBATT_LT_3P1_EINT *(s)*	IM_CHG_VBATT_LT_2P85_EINT *(s)*	0000h
R34 (22h)	Interrupt Status 2 Mask	0	0	IM_CS1_EINT *(s)*	IM_CS2_EINT *(s)*	0	IM_USB_LIMIT_EINT *(s)*	0	0	IM_AUXADC_DCOMP4_EINT *(s)*	IM_AUXADC_DCOMP3_EINT *(s)*	IM_AUXADC_DCOMP2_EINT *(s)*	IM_AUXADC_DCOMP1_EINT *(s)*	IM_SYS_HYST_COMP_FAIL_EINT *(s)*	IM_SYS_CHIP_GT115_EINT *(s)*	IM_SYS_CHIP_GT140_EINT *(s)*	IM_SYS_WDOG_TO_EINT *(s)*	0000h
R36 (24h)	Under Voltage Interrupt status Mask	0	0	0	0	IM_UV_LDO4_EINT *(s)*	IM_UV_LDO3_EINT *(s)*	IM_UV_LDO2_EINT *(s)*	IM_UV_LDO1_EINT *(s)*	0	0	0	0	IM_UV_DC4_EINT *(s)*	IM_UV_DC3_EINT *(s)*	IM_UV_DC2_EINT *(s)*	IM_UV_DC1_EINT *(s)*	0000h
R37 (25h)	Over Current Interrupt status Mask	IM_OC_LS_EINT *(s)*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R38 (26h)	GPIO Interrupt Status Mask	0	0	0	IM_GP12_EINT *(s)*	IM_GP11_EINT *(s)*	IM_GP10_EINT *(s)*	IM_GP9_EINT *(s)*	IM_GP8_EINT *(s)*	IM_GP7_EINT *(s)*	IM_GP6_EINT *(s)*	IM_GP5_EINT *(s)*	IM_GP4_EINT *(s)*	IM_GP3_EINT *(s)*	IM_GP2_EINT *(s)*	IM_GP1_EINT *(s)*	IM_GP0_EINT *(s)*	0000h
R39 (27h)	Comparator Interrupt Status Mask	IM_EXT_USB_FB_EINT *(s)*	IM_EXT_WALL_FB_EINT *(s)*	IM_EXT_BATT_FB_EINT *(s)*	0	IM_CODEC_JCK_DET_L_EINT *(s)*	IM_CODEC_JCK_DET_R_EINT *(s)*	IM_CODEC_MICSCD_EINT *(s)*	IM_CODEC_MICD_EINT *(s)*	0	IM_WKUP_OFF_STATE_EINT *(s)*	IM_WKUP_HIB_STATE_EINT *(s)*	IM_WKUP_CONV_FAULT_EINT *(s)*	IM_WKUP_WDOG_RST_EINT *(s)*	IM_WKUP_GP_PWR_ON_EINT *(s)*	IM_WKUP_ONKEY_EINT *(s)*	IM_WKUP_GP_WAKEUP_EINT *(s)*	0000h
R40 (28h)	Clock Control 1	TOCLK_ENA	TOCLK_RATE	0	0	MCLK_SEL	0	0	MCLK_DIV	BCLK_DIV[3:0]				0	OPCLK_DIV[2:0]			0040h
R41 (29h)	Clock Control 2	LRC_ADC_SEL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MCLK_DIR	0000h
R42 (2Ah)	FLL Control 1	FLL_ENA	FLL_OSC_ENA	1	1	1	FLL_OUTDIV[2:0]			FLL_RSP_RATE[3:0]				0	FLL_RATE[2:0]			3A00h
R43 (2Bh)	FLL Control 2	FLL_RATIO[4:0]					0	FLL_N[9:0]										7086h
R44 (2Ch)	FLL Control 3	FLL_K[15:0]																C226h
R45 (2Dh)	FLL Control 4	0	0	0	0	0	0	0	0	FLL_REF_FREQ	0	FLL_FRAC	0	0	0	FLL_CLK_SRC[1:0]		0000h
R48 (30h)	DAC Control	0	0	DAC_MONO	AIF_LRCLK RATE	0	0	0	0	0	0	DEEMP[1:0]		DAC_SDMCLK_RATE	0	DACL_DATINV	DACR_DATINV	0000h
R50 (32h)	DAC Digital Volume L	DACL_ENA	0	0	0	0	0	0	DAC_VU	DACL_VOL[7:0]								00C0h
R51 (33h)	DAC Digital Volume R	DACR_ENA	0	0	0	0	0	0	DAC_VU	DACR_VOL[7:0]								00C0h
R53 (35h)	DAC LR Rate	0	0	0	0	DACLRC_ENA	DACLRC_RATE[10:0]											0040h
R54 (36h)	DAC Clock Control	0	0	0	0	0	0	0	0	0	0	0	DACCLK_POL	0	DAC_CLKDIV[2:0]			0000h
R58 (3Ah)	DAC Mute	0	DAC_MUTE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000h
R59 (3Bh)	DAC Mute Volume	0	DAC_MUTEMODE	DAC_MUTERATE	DAC_SB_FILT	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R60 (3Ch)	DAC Side	0	0	ADC_TO_DACL[1:0]		ADC_TO_DACR[1:0]		0	0	0	0	0	0	0	0	0	0	0000h
R64 (40h)	ADC Control	ADC_HPF_ENA	0	0	0	0	0	ADC_HPF_CUT[1:0]		0	0	0	0	0	0	ADCL_DATINV	ADCR_DATINV	8000h
R66 (42h)	ADC Digital Volume L	ADCL_ENA	0	0	0	0	0	0	ADC_VU	ADCL_VOL[7:0]								00C0h
R67 (43h)	ADC Digital Volume R	ADCR_ENA	0	0	0	0	0	0	ADC_VU	ADCR_VOL[7:0]								00C0h
R68 (44h)	ADC Divider	0	0	0	0	ADCL_DAC_SVOL[3:0]				ADCR_DAC_SVOL[3:0]				ADCCLK_POL	ADC_CLKDIV[2:0]			0000h
R70 (46h)	ADC LR Rate	0	0	0	0	ADCLRC_ENA	ADCLRC_RATE[10:0]											0040h
R72 (48h)	Input Control	0	0	0	0	0	IN2R_ENA	IN1RN_ENA	IN1RP_ENA	0	0	0	0	0	IN2L_ENA	IN1LN_ENA	IN1LP_ENA	0303h
R73 (49h)	IN3 Input Control	IN3R_ENA	IN3R_SHORT	0	0	0	0	0	0	IN3L_ENA	IN3L_SHORT	0	0	0	0	0	0	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R74 (4Ah)	Mic Bias Control	MICB_ENA	MICB_SEL	0	0	0	0	0	0	MIC_DET_ENA	0	0	MCDTHR[2:0]			MCDSCTHR[1:0]		0000h
R76 (4Ch)	Output Control	0	0	0	0	OUT4_VROI	OUT3_VROI	OUT2_VROI	OUT1_VROI	0	0	0	OUTPUT_DRAIN_ENA	0	OUT2_FB	0	OUT1_FB	0000h
R77 (4Dh)	Jack Detect	JDL_ENA	JDR_ENA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R78 (4Eh)	Anti Pop Control	0	0	0	0	0	0	ANTI_POP[1:0]		DIS_OP_LN4[1:0]		DIS_OP_LN3[1:0]		DIS_OP_OUT2[1:0]		DIS_OP_OUT1[1:0]		0000h
R80 (50h)	Left Input Volume	INL_ENA	INL_MUTE	INL_ZC	0	0	0	0	IN_VU	INL_VOL[5:0]						0	0	0040h
R81 (51h)	Right Input Volume	INR_ENA	INR_MUTE	INR_ZC	0	0	0	0	IN_VU	INR_VOL[5:0]						0	0	0040h
R88 (58h)	Left Mixer Control	MIXOUTL_ENA	0	0	DACR_TO_MIXOUTL	DACL_TO_MIXOUTL	0	0	0	0	0	0	0	0	IN3L_TO_MIXOUTL	INR_TO_MIXOUTL	INL_TO_MIXOUTL	0800h
R89 (59h)	Right Mixer Control	MIXOUTR_ENA	0	0	DACR_TO_MIXOUTR	DACL_TO_MIXOUTR	0	0	0	0	0	0	0	IN3R_TO_MIXOUTR	0	INR_TO_MIXOUTR	INL_TO_MIXOUTR	1000h
R92 (5Ch)	OUT3 Mixer Control	OUT3_ENA	0	0	0	DACL_TO_OUT3	0	0	MIXINL_TO_OUT3	0	0	0	0	OUT4_TO_OUT3	0	0	MIXOUTL_TO_OUT3	0000h
R93 (5Dh)	OUT4 Mixer Control	OUT4_ENA	0	0	DACR_TO_OUT4	DACL_TO_OUT4	OUT4_ATTN	MIXINR_TO_OUT4	0	0	0	0	0	0	OUT3_TO_OUT4	MIXOUTR_TO_OUT4	MIXOUTL_TO_OUT4	0000h
R96 (60h)	Output Left Mixer Volume	0	0	0	0	IN3L_MIXOUTL_VOL[2:0]			0	INR_MIXOUTL_VOL[2:0]			0	INL_MIXOUTL_VOL[2:0]			0	0000h
R97 (61h)	Output Right Mixer Volume	IN3R_MIXOUTR_VOL[2:0]			0	0	0	0	0	INR_MIXOUTR_VOL[2:0]			0	INL_MIXOUTR_VOL[2:0]			0	0000h
R98 (62h)	Input Mixer Volume L	0	0	0	0	IN3L_MIXINL_VOL[2:0]			0	0	0	0	0	IN2L_MIXINL_VOL[2:0]			INL_MIXINL_VOL	0000h
R99 (63h)	Input Mixer Volume R	IN3R_MIXINR_VOL[2:0]			0	0	0	0	0	IN2R_MIXINR_VOL[2:0]			0	0	0	0	INR_MIXINR_VOL	0000h
R100 (64h)	Input Mixer Volume	OUT4_MIXIN_DST	0	0	0	0	0	0	0	0	0	0	0	OUT4_MIXIN_VOL[2:0]			0	0000h
R104 (68h)	OUT1L Volume	OUT1L_ENA	OUT1L_MUTE	OUT1L_ZC	0	0	0	0	OUT1_VU	OUT1L_VOL[5:0]						0	0	00E4h
R105 (69h)	OUT1R Volume	OUT1R_ENA	OUT1R_MUTE	OUT1R_ZC	0	0	0	0	OUT1_VU	OUT1R_VOL[5:0]						0	0	00E4h
R106 (6Ah)	OUT2L Volume	OUT2L_ENA	OUT2L_MUTE	OUT2L_ZC	0	0	0	0	OUT2_VU	OUT2L_VOL[5:0]						0	0	00E4h
R107 (6Bh)	OUT2R Volume	OUT2R_ENA	OUT2R_MUTE	OUT2R_ZC	0	0	OUT2R_INV	OUT2R_INV_MUTE	OUT2_VU	OUT2R_VOL[5:0]						0	0	02E4h
R111 (6Fh)	BEEP Volume	IN3R_TO_OUT2R	0	0	0	0	0	0	0	IN3R_OUT2R_VOL[2:0]			0	0	0	0	0	0000h
R112 (70h)	AI Formating	AIF_BCLK_INV	0	AIF_TRI	AIF_LRCLK_INV	AIF_WL[1:0]		AIF_FMT[1:0]		0	0	0	0	0	0	0	0	0A00h
R113 (71h)	ADC DAC COMP	0	0	0	0	0	0	0	0	DAC_COMP	DAC_COMPMODE	ADC_COMP	ADC_COMPMODE	0	0	0	LOOPBACK	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R114 (72h)	AI ADC Control	0	0	0	0	0	0	0	0	AIFADC_PD	AIFADCL_SRC	AIFADCR_SRC	AIFADC_TDM_CHAN	AIFADC_TDM	0	0	0	0020h
R115 (73h)	AI DAC Control	0	BCLK_MSTR	0	0	0	0	0	0	AIFDAC_PD	DACL_SRC	DACR_SRC	AIFDAC_TDM_CHAN	AIFDAC_TDM	0	DAC_BOOST[1:0]		0020h
R128 (80h)	GPIO Debounce	0	0	0	GP12_DB *(s)*	GP11_DB *(s)*	GP10_DB *(s)*	GP9_DB *(s)*	GP8_DB *(s)*	GP7_DB *(s)*	GP6_DB *(s)*	GP5_DB *(s)*	GP4_DB *(s)*	GP3_DB *(s)*	GP2_DB *(s)*	GP1_DB *(s)*	GP0_DB *(s)*	1FFFh
R129 (81h)	GPIO Pin pull up Control	0	0	0	GP12_PU *(Ms)*	GP11_PU *(Ms)*	GP10_PU *(Ms)*	GP9_PU *(Ms)*	GP8_PU *(Ms)*	GP7_PU *(Ms)*	GP6_PU *(Ms)*	GP5_PU *(Ms)*	GP4_PU *(Ms)*	GP3_PU *(Ms)*	GP2_PU *(Ms)*	GP1_PU *(Ms)*	GP0_PU *(Ms)*	0000h 0000h 0000h 0010h
R130 (82h)	GPIO Pull down Control	0	0	0	GP12_PD *(Ms)*	GP11_PD *(Ms)*	GP10_PD *(Ms)*	GP9_PD *(Ms)*	GP8_PD *(Ms)*	GP7_PD *(Ms)*	GP6_PD *(Ms)*	GP5_PD *(Ms)*	GP4_PD *(Ms)*	GP3_PD *(Ms)*	GP2_PD *(Ms)*	GP1_PD *(Ms)*	GP0_PD *(Ms)*	0000h 0000h 0110h 0000h
R131 (83h)	GPIO Interrupt Mode	0	0	0	GP12_INTMODE *(s)*	GP11_INTMODE *(s)*	GP10_INTMODE *(s)*	GP9_INTMODE *(s)*	GP8_INTMODE *(s)*	GP7_INTMODE *(s)*	GP6_INTMODE *(s)*	GP5_INTMODE *(s)*	GP4_INTMODE *(s)*	GP3_INTMODE *(s)*	GP2_INTMODE *(s)*	GP1_INTMODE *(s)*	GP0_INTMODE *(s)*	0000h
R133 (85h)	GPIO Control	0	0	0	0	0	0	0	0	GP_DBTIME[1:0] *(s)*		0	0	0	0	0	0	0000h
R134 (86h)	GPIO Configuration (i/o)	0	0	0	GP12_DIR *(Ms)*	GP11_DIR *(Ms)*	GP10_DIR *(Ms)*	GP9_DIR *(Ms)*	GP8_DIR *(Ms)*	GP7_DIR *(Ms)*	GP6_DIR *(Ms)*	GP5_DIR *(Ms)*	GP4_DIR *(Ms)*	GP3_DIR *(Ms)*	GP2_DIR *(Ms)*	GP1_DIR *(Ms)*	GP0_DIR *(Ms)*	0FFCh 0CFBh 09FAh 0BFBh
R135 (87h)	GPIO Pin Polarity / Type	0	0	0	GP12_CFG *(Ms)*	GP11_CFG *(Ms)*	GP10_CFG *(Ms)*	GP9_CFG *(Ms)*	GP8_CFG *(Ms)*	GP7_CFG *(Ms)*	GP6_CFG *(Ms)*	GP5_CFG *(Ms)*	GP4_CFG *(Ms)*	GP3_CFG *(Ms)*	GP2_CFG *(Ms)*	GP1_CFG *(Ms)*	GP0_CFG *(Ms)*	0FFCh 0C1Fh 0DF6h 0FFDh
R140 (8Ch)	GPIO Function Select 1	GP3_FN[3:0] *(Ms)*				GP2_FN[3:0] *(Ms)*				GP1_FN[3:0] *(Ms)*				GP0_FN[3:0] *(Ms)*				0013h 0300h 1310h 0310h
R141 (8Dh)	GPIO Function Select 2	GP7_FN[3:0] *(Ms)*				GP6_FN[3:0] *(Ms)*				GP5_FN[3:0] *(Ms)*				GP4_FN[3:0] *(Ms)*				0000h 1110h 0003h 0001h
R142 (8Eh)	GPIO Function Select 3	GP11_FN[3:0] *(Ms)*				GP10_FN[3:0] *(Ms)*				GP9_FN[3:0] *(Ms)*				GP8_FN[3:0] *(Ms)*				0000h 0013h 2000h 2300h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R143 (8Fh)	GPIO Function Select 4	0	0	0	0	0	0	0	0	0	0	0	0	GP12_FN[3:0] *(Ms)*				0003h 0003h 0000h 0003h
R144 (90h)	Digitiser Control (1)	AUXADC_ENA *(s)*	AUXADC_CTC *(s)*	AUXADC_POLL *(s)*	AUXADC_HIB_MODE *(s)*	0	0	0	0	AUXADC_SEL8 *(s)*	AUXADC_SEL7 *(s)*	AUXADC_SEL6 *(s)*	AUXADC_SEL5 *(s)*	AUXADC_SEL4 *(s)*	AUXADC_SEL3 *(s)*	AUXADC_SEL2 *(s)*	AUXADC_SEL1 *(s)*	0000h
R145 (91h)	Digitiser Control (2)	0	0	AUXADC_MASKMODE[1:0] *(s)*		0	AUXADC_CRATE[2:0] *(s)*			0	0	0	0	0	AUXADC_CAL *(s)*	AUXADC_RBMODE *(s)*	AUXADC_WAIT *(s)*	0002h
R152 (98h)	AUX1 Readback	0	AUXADC_SCALE1[1:0]		AUXADC_REF1	AUXADC_DATA1[11:0]												7000h
R153 (99h)	AUX2 Readback	0	AUXADC_SCALE2[1:0]		AUXADC_REF2	AUXADC_DATA2[11:0]												7000h
R154 (9Ah)	AUX3 Readback	0	AUXADC_SCALE3[1:0]		AUXADC_REF3	AUXADC_DATA3[11:0]												7000h
R155 (9Bh)	AUX4 Readback	0	AUXADC_SCALE4[1:0]		AUXADC_REF4	AUXADC_DATA4[11:0]												7000h
R156 (9Ch)	USB Voltage Readback	0	0	0	0	AUXADC_DATA_USB[11:0]												0000h
R157 (9Dh)	LINE Voltage Readback	0	0	0	0	AUXADC_DATA_LINE[11:0]												0000h
R158 (9Eh)	BATT Voltage Readback	0	0	0	0	AUXADC_DATA_BATT[11:0]												0000h
R159 (9Fh)	Chip Temp Readback	0	0	0	0	AUXADC_DATA_CHIPTEMP[11:0]												0000h
R163 (A3h)	Generic Comparator Control	0	0	0	0	0	0	0	0	0	0	0	0	DCMP4_ENA *(s)*	DCMP3_ENA *(s)*	DCMP2_ENA *(s)*	DCMP1_ENA *(s)*	0000h
R164 (A4h)	Generic comparator 1	DCMP1_SRCSEL[2:0] *(s)*			DCMP1_GT	DCMP1_THR[11:0]												0000h
R165 (A5h)	Generic comparator 2	DCMP2_SRCSEL[2:0] *(s)*			DCMP2_GT	DCMP2_THR[11:0]												0000h
R166 (A6h)	Generic comparator 3	DCMP3_SRCSEL[2:0] *(s)*			DCMP3_GT	DCMP3_THR[11:0]												0000h
R167 (A7h)	Generic comparator 4	DCMP4_SRCSEL[2:0] *(s)*			DCMP4_GT	DCMP4_THR[11:0]												0000h
R168 (A8h)	Battery Charger Control 1	CHG_ENA *(KMs)*	0	0	CHG_EOC_SEL[2:0] *(K)*			CHG_TRICKLE_TEMP_CHOKE *(Ks)*	CHG_TRICKLE_USB_CHOKE *(Ks)*	CHG_RECOVER_T *(Ks)*	CHG_END_ACT *(Ks)*	CHG_FAST *(KMs)*	CHG_FAST_USB_THROTTLE *(Ks)*	CHG_NTC_MON *(M)*	CHG_BATT_HOT_MON *(M)*	CHG_BATT_COLD_MON *(M)*	CHG_CHIP_TEMP_MON *(KM)*	A00Fh
R169 (A9h)	Battery Charger Control 2	CHG_ACTIVE *(M)*	CHG_PAUSE *(s)*	CHG_STS[1:0]		CHG_TIME[3:0] *(KM)*				CHG_MASK_WALL_FB *(Ks)*	CHG_TRICKLE_SEL *(K)*	CHG_VSEL[1:0] *(K)*		CHG_ISEL[3:0] *(K)*				0B06h
R170 (AAh)	Battery Charger Control 3	0	0	0	0	0	0	0	0	CHG_FRC *(Ks)*	CHG_THROTTLE_T[1:0] *(K)*		0	0	0	0	0	0000h
R172 (ACh)	Current Sink Driver A	CS1_ENA *(s)*	0	0	CS1_HIB_MODE *(s)*	0	0	0	0	0	0	CS1_ISEL[5:0] *(s)*						0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R173 (ADh)	CSA Flash control	CS1_FLASH_MODE *(s)*	CS1_TRIGSRC *(s)*	CS1_DRIVE *(Ms)*	CS1_FLASH_RATE *(s)*	0	0	CS1_FLASH_DUR[1:0] *(s)*		0	0	CS1_OFF_RAMP[1:0] *(s)*		0	0	CS1_ON_RAMP[1:0] *(s)*		0000h
R176 (B0h)	DCDC/LDO requested	LS_ENA *(Ms)*	0	0	0	LDO4_ENA *(Ms)*	LDO3_ENA *(Ms)*	LDO2_ENA *(Ms)*	LDO1_ENA *(Ms)*	0	0	0	0	DC4_ENA *(Ms)*	DC3_ENA *(Ms)*	DC2_ENA *(Ms)*	DC1_ENA *(Ms)*	0000h
R177 (B1h)	DCDC Active options	DCDC_DISCLKS *(s)*	0	PUTO[1:0] *(s)*		0	0	0	0	0	0	0	0	DC4_ACTIVE *(s)*	DC3_ACTIVE *(s)*	0	DC1_ACTIVE *(s)*	032Dh
R178 (B2h)	DCDC Sleep options	0	0	0	0	0	0	0	0	0	0	0	0	DC4_SLEEP *(s)*	DC3_SLEEP *(s)*	0	DC1_SLEEP *(s)*	0000h
R179 (B3h)	Power-check comparator	0	PCCMP_ERRACT *(s)*	0	PCCOMP_HIB_MODE	0	0	0	0	0	PCCMP_OFF_THR[2:0] *(KM)*			0	PCCMP_ON_THR[2:0] *(KM)*			0025h
R180 (B4h)	DCDC1 Control	DC1_CAP[1:0] *(s)*		0	0	DC1_DISOVP *(Ms)*	DC1_OPFLT	0	0	0	DC1_VSEL[6:0] *(Ms)*							000Eh 000Eh 001Ah 000Eh
R181 (B5h)	DCDC1 Timeouts	DC1_ERRACT[1:0] *(Ms)*		DC1_ENSLOT[3:0] *(Ms)*				DC1_SDSLOT[3:0]				0	0	0	0	0	0	0000h 0C00h 0800h 0400h
R182 (B6h)	DCDC1 Low Power	0	DC1_HIB_MODE[2:0]			0	0	DC1_HIB_TRIG[1:0] *(Ms)*		0	DC1_VIMG[6:0]							1006h
R183 (B7h)	DCDC2 Control	0	DC2_MODE *(s)*	0	DC2_HIB_MODE *(s)*	0	0	DC2_HIB_TRIG[1:0] *(s)*		0	DC2_ILIM *(Ms)*	0	DC2_RMPH *(Ms)*	DC2_RMPL *(Ms)*	0	DC2_FBSRC[1:0] *(Ms)*		0018h
R184 (B8h)	DCDC2 Timeouts	DC2_ERRACT[1:0] *(Ms)*		DC2_ENSLOT[3:0] *(Ms)*				DC2_SDSLOT[3:0]				0	0	0	0	0	0	0000h
R186 (BAh)	DCDC3 Control	0	0	0	0	DC3_DISOVP *(Ms)*	DC3_OPFLT	0	0	0	DC3_VSEL[6:0] *(Ms)*							0000h 0026h 0056h 0026h
R187 (BBh)	DCDC3 Timeouts	DC3_ERRACT[1:0] *(Ms)*		DC3_ENSLOT[3:0] *(Ms)*				DC3_SDSLOT[3:0]				0	0	0	0	0	0	0000h 0400h 0400h 0800h
R188 (BCh)	DCDC3 Low Power	0	DC3_HIB_MODE[2:0] *(Ms)*			0	0	DC3_HIB_TRIG[1:0] *(Ms)*		0	DC3_VIMG[6:0]							0006h
R189 (BDh)	DCDC4 Control	0	0	0	0	DC4_DISOVP *(Ms)*	DC4_OPFLT	0	0	0	DC4_VSEL[6:0] *(Ms)*							0000h 0062h 0026h 0062h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R190 (BEh)	DCDC4 Timeouts	DC4_ERRACT[1:0] *(Ms)*		DC4_ENSLOT[3:0] *(Ms)*				DC4_SDSLOT[3:0]				0	0	0	0	0	0	0000h 0800h 0C00h 1400h
R191 (BFh)	DCDC4 Low Power	0	DC4_HIB_MODE[2:0] *(Ms)*			0	0	DC4_HIB_TRIG[1:0] *(Ms)*		0	DC4_VIMG[6:0]							0006h
R199 (C7h)	Limit Switch Control	LS_ERRACT[1:0] *(Ms)*		LS_ENSLOT[3:0] *(Ms)*				LS_SDSLOT[3:0]				0	LS_HIB_MODE	0	0	LS_HIB_PROT	LS_PROT	0003h
R200 (C8h)	LDO1 Control	0	LDO1_SWI *(Ms)*	0	0	0	LDO1_OPFLT	0	0	0	0	0	LDO1_VSEL[4:0] *(Ms)*					001Ch 0006h 001Ch 0006h
R201 (C9h)	LDO1 Timeouts	LDO1_ERRACT[1:0] *(Ms)*		LDO1_ENSLOT[3:0] *(Ms)*				LDO1_SDSLOT[3:0]				0	0	0	0	0	0	0000h 0000h 0400h 0C00h
R202 (CAh)	LDO1 Low Power	0	0	LDO1_HIB_MODE[1:0] *(Ms)*		0	0	LDO1_HIB_TRIG[1:0] *(Ms)*		0	0	0	LDO1_VIMG[4:0]					001Ch
R203 (CBh)	LDO2 Control	0	LDO2_SWI *(Ms)*	0	0	0	LDO2_OPFLT	0	0	0	0	0	LDO2_VSEL[4:0] *(Ms)*					001Bh 0010h 0010h 0016h
R204 (CCh)	LDO2 Timeouts	LDO2_ERRACT[1:0] *(Ms)*		LDO2_ENSLOT[3:0] *(Ms)*				LDO2_SDSLOT[3:0]				0	0	0	0	0	0	0000h 0C00h 0C00h 0000h
R205 (CDh)	LDO2 Low Power	0	0	LDO2_HIB_MODE[1:0] *(Ms)*		0	0	LDO2_HIB_TRIG[1:0] *(Ms)*		0	0	0	LDO2_VIMG[4:0]					001Ch
R206 (CEh)	LDO3 Control	0	LDO3_SWI *(Ms)*	0	0	0	LDO3_OPFLT	0	0	0	0	0	LDO3_VSEL[4:0] *(Ms)*					001Bh 001Fh 0015h 0019h
R207 (CFh)	LDO3 Timeouts	LDO3_ERRACT[1:0] *(Ms)*		LDO3_ENSLOT[3:0] *(Ms)*				LDO3_SDSLOT[3:0]				0	0	0	0	0	0	0000h 0800h 0000h 0000h
R208 (D0h)	LDO3 Low Power	0	0	LDO3_HIB_MODE[1:0] *(Ms)*		0	0	LDO3_HIB_TRIG[1:0] *(Ms)*		0	0	0	LDO3_VIMG[4:0]					001Ch

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R209 (D1h)	LDO4 Control	0	LDO4_SWI *(Ms)*	0	0	0	LDO4_OPFLT	0	0	0	0	0	LDO4_VSEL[4:0] *(Ms)*					001Bh 000Ah 001Ah 001Ah
R210 (D2h)	LDO4 Timeouts	LDO4_ERRACT[1:0] *(Ms)*		LDO4_ENSLOT[3:0] *(Ms)*				LDO4_SDSLOT[3:0]				0	0	0	0	0	0	0000h 0800h 0000h 1000h
R211 (D3h)	LDO4 Low Power	0	0	LDO4_HIB_MODE[1:0] *(Ms)*		0	0	LDO4_HIB_TRIG[1:0] *(Ms)*		0	0	0	LDO4_VIMG[4:0]					001Ch
R215 (D7h)	VCC_FAULT Masks	LS_FAULT *(s)*	0	0	0	LDO4_FAULT *(s)*	LDO3_FAULT *(s)*	LDO2_FAULT *(s)*	LDO1_FAULT *(s)*	0	0	0	0	DC4_FAULT *(s)*	DC3_FAULT *(s)*	DC2_FAULT *(s)*	DC1_FAULT *(s)*	0000h
R216 (D8h)	Main Bandgap Control	MBG_LOAD_FUSES	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	001Fh
R217 (D9h)	OSC Control	OSC_LOAD_FUSES *(K)*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R218 (DAh)	RTC Tick Control	RTC_TICK_ENA *(KMs)*	RTC_TICKSTS *(K)*	RTC_CLKSRC *(KMs)*	OSC32K_ENA *(KMs)*	0	0	RTC_TRIM[9:0] *(K)*										9000h
R219 (DBh)	Security1	SECURITY[15:0] *(s)*																0000h
R224 (E0h)	Signal overrides	0	0	0	0	WALL_FB_GT_BATT_OVRDE	USB_FB_GT_BATT_OVRDE	FLL_OK_OVRDE	DEB_TICK_OVRDE	UVLO_B_OVRDE	RTC_ALARM_OVRDE	0	0	LINE_GT_BATT_OVRDE	LINE_GT_VRTC_OVRDE	USB_GT_LINE_OVRDE	BATT_GT_USB_OVRDE	0000h
R225 (E1h)	DCDC/LDO status	LS_STS *(s)*	0	0	0	LDO4_STS *(s)*	LDO3_STS *(s)*	LDO2_STS *(s)*	LDO1_STS *(s)*	0	0	0	0	DC4_STS *(s)*	DC3_STS *(s)*	DC2_STS *(s)*	DC1_STS *(s)*	0000h
R226 (E2h)	Charger Overides/status	CHG_BATT_HOT_OVRDE	CHG_BATT_COLD_OVRDE	0	0	CHG_END_OVRDE	0	0	0	0	0	0	0	0	CHG_BATT_LT_3P9_OVRDE	CHG_BATT_LT_3P1_OVRDE	CHG_BATT_LT_2P85_OVRDE	0000h
R227 (E3h)	misc overrides	0	0	0	CS1_NOT_REG_OVRDE	0	USB_LIMIT_OVRDE	0	0	AUX_DCOMP4_OVRDE	AUX_DCOMP3_OVRDE	AUX_DCOMP2_OVRDE	AUX_DCOMP1_OVRDE	HYST_UVLO_OK_OVRDE	CHIP_GT115_OVRDE	CHIP_GT140_OVRDE	0	0000h
R228 (E4h)	Supply overrides/status 1	0	0	0	0	0	0	0	0	0	0	0	0	OVRV_DC4_OVRDE	OVRV_DC3_OVRDE	0	OVRV_DC1_OVRDE	0000h
R229 (E5h)	Supply overrides/status 2	OVCR_LS_OVRDE	0	0	0	UNDV_LDO4_OVRDE	UNDV_LDO3_OVRDE	UNDV_LDO2_OVRDE	UNDV_LDO1_OVRDE	0	0	0	0	UNDV_DC4_OVRDE	UNDV_DC3_OVRDE	UNDV_DC2_OVRDE	UNDV_DC1_OVRDE	0000h
R230 (E6h)	GPIO Pin Status	1 *(n)*	1 *(n)*	1 *(n)*	GP12_LVL	GP11_LVL	GP10_LVL	GP9_LVL	GP8_LVL	GP7_LVL	GP6_LVL	GP5_LVL	GP4_LVL	GP3_LVL	GP2_LVL	GP1_LVL	GP0_LVL	E000h
R231 (E7h)	comparotor overrides	USB_FB_OVRDE	WALL_FB_OVRDE	BATT_FB_OVRDE	0	CODEC_JCK_DET_L_OVRDE	CODEC_JCK_DET_R_OVRDE	CODEC_MICSCD_OVRDE	CODEC_MICD_OVRDE	0	0	0	0	0	0	0	0	0000h
R233 (E9h)	State Machine status	0	0	0	0	0	USB_SM[2:0]			0	CHG_SM[2:0]			MAIN_SM[3:0]				0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R234 (EAh)	FLL Test 1	0	0	0	FLL_FRC_TRK_GAIN *(K)*	0	0	FLL_BIAS[1:0] *(K)*		FLL_POLE_SHIFT[1:0] *(K)*		0	0	0	0	0	0	1200h
R248 (F8h)	DCDC1 Test Controls	0	0	0	0	0	0	0	0	0	0	0	DC1_FORCE_PWM *(s)*	0	0	0	0	1000h
R250 (FAh)	DCDC3 Test Controls	0	0	0	0	0	0	0	0	0	0	0	DC3_FORCE_PWM *(s)*	0	0	0	0	1000h
R251 (FBh)	DCDC4 Test Controls	0	0	0	0	0	0	0	0	0	0	0	DC4_FORCE_PWM *(s)*	0	0	0	0	1000h

27 REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) Reset/ID	15:0	SW_RESET/CHIP_ID[15:0]	0110_0001_0100_0011	Reading this register returns 6143h. *Never reset.*	

Register 00h Reset/ID

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1 (01h) ID	15:12	CHIP_REV[3:0]	0000	The functional silicon revision - this tracks changes in functionality which are separate from ROM mask settings	
	11:10	CONF_STS[1:0]	00	The state of the configuration pins. This selects what register defaults should be.	
	7:0	CUST_ID[7:0]	0000_0000	The Chip Revision Number	

Register 01h ID

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2 (02h) Revision	7:0	MASK_REV[7:0]	0000_0001	The ROM Mask ID	

Register 02h Revision

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R3 (03h) System Control 1	15	CHIP_ON	0	Indicates whether the system is on or off. Writing 0 to this bit powers down the whole chip. Registers which are affected by state machine reset will get reset. Once the system is turned OFF it can be restarted by any of the valid ON event. *Reset by state machine. Default held in metal mask.*	
	14	SYS_RST	0	Allows the processors to reboot itself 0 = Do nothing 1 = Perform a processor reset by asserting the /RST and /MEMRST (GPIO) pins for the programmed duration *Protected by security key. Reset by state machine. Default held in metal mask.*	
	13	POWERCYCLE	0	Action to take on a fault (if response is set to shutdown system): 0 = Shut down 1 = Shutdown everything then go through startup sequence. i.e. Reboot the system.	
	12	VCC_FAULT_OV	1	Include over voltage in the /VCC_FAULT pin (Alternative GPIO function) 0 = Do not include over voltage in the /VCC_FAULT signal 1 = Include the over voltage in the /VCC_FAULT signal *Reset by state machine. Default held in metal mask.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	11:10	RSTB_TO[1:0]	11	Time that the /RST pin and /MEMRST output is held low after the chip reaches the active state. 00 = 15ms 01 = 30ms 10 = 60ms 11 = 120ms *Default held in metal mask.*	
	9	BG_SLEEP	0	Bandgap sleep mode 0 = never in sleep mode 1 = sleep mode is controlled by Main SM *Default held in metal mask.*	
	7	WDOG_DEBUG	0	Halts watchdog timer for system debugging 0 = normal operation 1 = WDOG halt *Protected by security key.*	
	6	CHIP_RESET_ENA	0	[No description available] *Reset by state machine.*	
	5	MEM_VALID	0	Indicates that the contents of external memory are still valid. This bit is cleared on startup and whenever /MEMRST is asserted from the main state machine. The system software should set this bit once the external memory has been set up. Controlled in hibernate mode by MEMRST_HIB_MODE 0 = External memory is not valid and needs restoring. 1 = External memory is valid. *Reset when /MEMRST is asserted.*	
	4	CHIP_SET_UP	0	A spare register bit that can be used by the system to say if the chip has been configured. It is reset by POR.	
	3	ON_DEB_T	0	ON pin Shutdown function debounce time 0 = 10s 1 = 5s *Protected by security key.*	
	1	ON_POL	1	ON pin polarity: 0 = Active high (ON) 1 = Active low (/ON) *Protected by security key. Reset by state machine. Default held in metal mask.*	
	0	IRQ_POL	0	IRQ pin polarity: 0 = Active low (/IRQ) 1 = Active high (IRQ) *Reset by state machine. Default held in metal mask.*	

Register 03h System Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R4 (04h) System Control 2	15	USB_SUSPEND_8MA	0	USB suspend mode with 8mA option 0 = USB is not suspended. 1 = USB is suspend with 8mA option enabled The register bit defaults to 0, when a reset happens or LINE<UVLO or the system fail on boot due to the upper limit of the Hysteresis Comp not been met. *Default held in metal mask.*	
	14	USB_SUSPEND	0	Opens the USB switch 0 = USB enabled 1 = USB suspended The register bit defaults to 0, when a reset happens or LINE < UVLO or the system fail on boot due to the upper limit of the Hysteresis Comp not being met. *Default held in metal mask.*	
	13	USB_MSTR	0	Set the chip to be a USB master 0 = Slave 1 = Master The register bit defaults to 0, when a reset happens or the USB state machine moves from MASTER mode to SLAVE mode. *Reset by state machine. Default held in metal mask.*	
	12	USB_MSTR_SRC	0	Master mode source selector 0 = Master mode source is DCDC2 1 = Master mode source is LINE *Reset by state machine. Default held in metal mask.*	
	11	USB_MSTR_500MA	0	Set 500mA or 100mA mode when the USB switch is in master mode 0 = 100mA 1 = 500mA *Reset by state machine. Default held in metal mask.*	
	10	USB_NOLIM	0	USB current limiting 0 = Limit the USB current as per the settings. 1 = Don't limit USB current	
	9	USB_SLV_500MA	0 1 1 1	Set 500mA or 100mA mode when the USB switch is in slave mode 0 = 100mA 1 = 500mA The register bit defaults to 0, when a reset happens or LINE<UVLO or the system fail on boot due to the upper limit of the Hysteresis Comp not being met. *Reset by state machine. Default held in metal mask.*	
	7	WDOG_HIB_MODE	0	Watchdog state in hibernate state 0 = WDOG disabled in Hibernate 1 = WDOG controlled by WDOG_MODE in Hibernate	
	5:4	WDOG_MODE[1:0]	00 00 01	00 = Disabled 01 = SYS_WDOG_TO interrupt on time-out 10 = WKUP_WDOG_RST interrupt and System	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
			00	reset on time-out 11 = SYS_WDOG_TO interrupt on first time-out, WKUP_WDOG_RST interrupt and System reset on second time-out *Protected by security key. Reset by state machine. Default held in metal mask.*	
	2:0	WDOG_TO[2:0]	100	Watchdog timeout (seconds) The timer is reset to this value when a HEARTBEAT signal edge is detected or the host writes to the watchdog control register. 000 = 0.125s … (time doubles with each step) 101 = 4s 11x = Reserved *Protected by security key.*	

Register 04h System Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R5 (05h) System Hibernate	15	HIBERNATE	0	Determines what state the chip should operate in. 0 = Active state 1 = Hibernate state The register bit defaults to 0, when a reset happens *Reset by state machine. Default held in metal mask.*	
	7	WDOG_HIB_MODE	0	Watchdog behaviour in HIBERNATE state 0 = WDOG disabled in Hibernate 1 = WDOG controlled by WDOG_MODE in Hibernate	
	6	HIB_STARTUP_SEQ	0	Direction to take when going from Hibernate state to the Active state. 0 = Hibernate to Active without going through startup state 1 = Hibernate to Active goes though startup sequence	
	5	REG_RESET_HIB_MODE	0	Action of the internal register reset signal when going from Hibernate to Active. 0 = Do a register reset when leaving the hibernate state. 1 = Do not do a register reset when leaving the hibernate state	
	4	RST_HIB_MODE	0	/RST pin state in hibernate mode: 0 = Asserted (low) 1 = Not asserted (high)	
	3	IRQ_HIB_MODE	0	IRQ pin state in hibernate mode 0 = Normal operation 1 = Forced to indicate there is no IRQ	
	2	MEMRST_HIB_MODE	0	/MEMRST (Alternative GPIO function) pin state in hibernate mode 0 = Asserted (low) 1 = Not asserted (high)	
	1	PCCOMP_HIB_MODE	0	Function of the Hysteresis Comp in hibernate. 0 = Hyst Comp is not used in hibernate state	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = Hyst comp is on in the hibernate state	
	0	TEMPMON_HIB_MODE	0	Function of the temp monitoring in hibernate. 0 = Temp monitoring is off in hibernate state 1 = Temp monitoring is on in the hibernate state	

Register 05h System Hibernate

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R6 (06h) Interface Control	15	USE_DEV_PINS	1	Selects which pins to use for the 2-wire control: 0 = Use 2-wire I/F pins as 2-wire interface 1 = Use GPIO 10 and 11 as 2-wire interface, e.g. to download settings from PIC. Only applies when CONFIG pins[1:0] = 00. *Reset by state machine.*	
	14:13	DEV_ADDR[1:0]	00	Selects device address (only valid when CONF_STS = 00) 00 = 0x34 01 = 0x36 10 = 0x3C 11 = 0x3E *Reset by state machine.*	
	12	CONFIG_DONE	0	Tells the system that the PIC micro has completed its programming. 0 = Programming still to be done 1 = Programming complete Only applies when CONFIG pins[1:0] = 00. *Reset by state machine.*	
	11	RECONFIG_AT_ON	1	Selects whether to reset the registers in the OFF state and whether to reload the device configuration from the PIC when an ON event occurs. 0 = Do not reset registers in the OFF state. Do not load configuration data when an ON event occurs. 1 = Reset registers in the OFF state. Load configuration from the PIC when an ON event occurs. Note that, in development mode, the device configuration from the PIC is always loaded when first powering up the chip. This bit must always be set to default (1) in Custom Modes 01, 10 and 11.	
	9	AUTOINC	1	Enables address auto-increment 0 = disabled 1 = enabled *Reset by state machine.*	
	3	SPI_CFG	0	Controls the SDOUT (GPIO6) pin operation in 4 wire mode 0 = SDOUT output is CMOS 1 = SDOUT output is open drain Note: SPI_4WIRE must be set for this to take effect. *Protected by security key. Default held in metal mask.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2	SPI_4WIRE	0	Selects 3-wire or 4-wire SPI mode 0 = 3-wire mode using bi-directional SDATA pin 1 = 4 wire mode using SDOUT (GPIO6) Note: SPI_3WIRE must be set for this to take effect. *Protected by security key. Default held in metal mask.*	
	1	SPI_3WIRE	0	Selects 2- or 3-/4-wire mode. 0 = 2-wire mode 1 = 3/4 wire mode *Protected by security key. Default held in metal mask.*	

Register 06h Interface Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R8 (08h) Power mgmt (1)	15:14	CODEC_ISEL[1:0]	10	CODEC Analogue current level select 00 = x 1.5 01 = x 1.0 10 = x 0.75 11 = x 0.5	
	13	VBUF_ENA	0	Forces ON the tie-off amplifiers 0 = disabled 1 = enabled	
	10	OUTPUT_DRAIN_ENA	0	Enables a drain on the outputs allowing the amplifiers to shutdown more quickly. 0 = Shutdown as normal 1 = Sink current from an external capacitor, allowing faster shutdown.	
	8	MIC_DET_ENA	0	Enable MIC detect: 0 = disabled 1 = enabled	
	5	BIAS_ENA	0	Enables bias to analogue audio CODEC circuitry 0 = disabled 1 = enabled	
	4	MICB_ENA	0	Microphone bias enable 0 = OFF (high impedance output) 1 = ON	
	2	VMID_ENA	0	Enables VMID resistor string 0 = disabled 1 = enabled	
	1:0	VMID[1:0]	00	Resistor selection for VMID potential divider 00 = off 01 = Vmid comes from 300kΩ R-string 10 = Vmid comes from 50kΩ R-string 11 = Vmid comes from 5kΩ R-string	

Register 08h Power mgmt (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R9 (09h) Power mgmt (2)	11	IN3R_ENA	0	IN3R Amplifier enable 0 = disabled 1 = enabled	
	10	IN3L_ENA	0	IN3L Amplifier enable 0 = disabled 1 = enabled	
	9	INR_ENA	0	Right input PGA enable 0 = disabled 1 = enabled	
	8	INL_ENA	0	Left input PGA enable 0 = disabled 1 = enabled	
	7	MIXINR_ENA	0	Right input mixer enable 0 = disabled 1 = enabled	
	6	MIXINL_ENA	0	Left input mixer enable 0 = disabled 1 = enabled	
	5	OUT4_ENA	0	OUT4 enable 0 = disabled 1 = enabled	
	4	OUT3_ENA	0	OUT3 enable 0 = disabled 1 = enabled	
	1	MIXOUTR_ENA	0	Right Output Mixer Enable 0 = disabled 1 = enabled	
	0	MIXOUTL_ENA	0	Left Output Mixer Enable 0 = disabled 1 = enabled	

Register 09h Power mgmt (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R10 (0Ah) Power mgmt (3)	7	IN3R_TO_OUT2R	0	BEEP mixer enable	
	3	OUT2R_ENA	0	OUT2R enable 0 = disabled 1 = enabled	
	2	OUT2L_ENA	0	OUT2L enable 0 = disabled 1 = enabled	
	1	OUT1R_ENA	0	OUT1R enable 0 = disabled 1 = enabled	
	0	OUT1L_ENA	0	OUT1L enable 0 = disabled 1 = enabled	

Register 0Ah Power mgmt (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R11 (0Bh) Power mgmt (4)	14	SYSCLK_ENA	0	CODEC SYSCLK enable 0 = disabled 1 = enabled	
	13	ADC_HPF_ENA	1	High Pass Filter enable 0 = disabled 1 = enabled	
	11	FLL_ENA	0	Master Enable for FLL 0 = disabled 1 = enabled	
	10	FLL_OSC_ENA	0	FLL OSC enable 0 = disabled 1 = enabled	
	8	TOCLK_ENA	0	Slow clock enable. Used the zero cross timeout. 0 = disabled 1 = enabled	
	5	DACR_ENA	0	Right DAC enable 0 = disabled 1 = enabled	
	4	DACL_ENA	0	Left DAC enable 0 = disabled 1 = enabled	
	3	ADCR_ENA	0	Right ADC enable 0 = disabled 1 = enabled When ADCR and ADCL are used together as a stereo pair, then both ADCs must be enabled together using a single register write to Register R11 (0Bh).	
	2	ADCL_ENA	0	Left ADC enable 0 = disabled 1 = enabled When ADCR and ADCL are used together as a stereo pair, then both ADCs must be enabled together using a single register write to Register R11 (0Bh).	

Register 0Bh Power mgmt (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R12 (0Ch) Power mgmt (5)	12	CODEC_ENA	0	Master codec enable bit. Until this bit is set, all codec registers are held in reset. 0 = All codec registers held in reset 1 = Codec registers operate normally. *Reset by state machine.*	
	11	RTC_TICK_ENA	1	Real Time Clock control. 0 = RTC is disabled 1 = RTC is enabled. *Protected by security key. Reset by state machine. Default held in metal mask.*	
	10	OSC32K_ENA	1	32kHz crystal oscillator control 0 = 32kHz OSC is disabled 1 = 32kHz OSC is enabled *Protected by security key. Reset by state machine. Default held in metal mask.*	
	9	CHG_ENA	1	Charger control	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				CHG_ENA bit selects battery charger current control 0 = Set battery charger current to zero 1 = Enable battery charge control *Protected by security key. Reset by state machine. Default held in metal mask.*	
	8	SW_VRTC_ENA	0	SW_VRTC control 0 = VRTC is not driven out on SWVRTC pin 1 = VRTC is driven out on SWVRTC pin *Reset by state machine.*	
	7	AUXADC_ENA	0	AUXADC control 0 = disabled 1 = enabled *Reset by state machine.*	
	3	DCMP4_ENA	0	Digital comparator 4 enable 0 = disabled 1 = enabled *Reset by state machine.*	
	2	DCMP3_ENA	0	Digital comparator 3 enable 0 = disabled 1 = enabled *Reset by state machine.*	
	1	DCMP2_ENA	0	Digital comparator 2 enable 0 = disabled 1 = enabled *Reset by state machine.*	
	0	DCMP1_ENA	0	Digital comparator 1 enable 0 = disabled 1 = enabled *Reset by state machine.*	

Register 0Ch Power mgmt (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R13 (0Dh) Power mgmt (6)	15	LS_ENA	0	Limit Switch enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	11	LDO4_ENA	0	LDO4 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	10	LDO3_ENA	0	LDO3 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Reset by state machine. Default held in metal mask.	
	9	LDO2_ENA	0	LDO2 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	8	LDO1_ENA	0	LDO1 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	3	DC4_ENA	0	DCDC4 converter enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	2	DC3_ENA	0	DCDC3 converter enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	1	DC2_ENA	0	DCDC2 converter enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	0	DC1_ENA	0	DCDC1 converter enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	

Register 0Dh Power mgmt (6)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R14 (0Eh) Power mgmt (7)	0	CS1_ENA	0	Current Sink 1 enable (ISINKA pin) 0 = disabled 1 = enabled *Reset by state machine.*	

Register 0Eh Power mgmt (7)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16 (10h) RTC Seconds/Minutes	14:8	RTC_MINS[6:0]	000_0000	RTC Minutes; 0 to 59	
	6:0	RTC_SECS[6:0]	000_0000	RTC Seconds; 0 to 59	

Register 10h RTC Seconds/Minutes

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R17 (11h) RTC Hours/Day	10:8	RTC_DAY[2:0]	001	RTC Day of the week register with range 1-7. 1 is Sunday	
	5	RTC_HPM	0	RTC hours AM/PM flag 0 = AM 1 = PM Only valid in 12 hour mode.	
	4:0	RTC_HRS[4:0]	0_0000	RTC Hours register with 0-23 range in 24 hour mode and 1-12 in 12 hour mode. (Bit 5 is used to indicate PM/not-AM flag in 12 hour mode.)	

Register 11h RTC Hours/Day

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R18 (12h) RTC Date/Month	12:8	RTC_MTH[4:0]	0_0001	RTC Month register with range 1-12.	
	5:0	RTC_DATE[5:0]	00_0001	RTC Date register with range 1-31	

Register 12h RTC Date/Month

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R19 (13h) RTC Year	13:8	RTC_YHUNDREDS[5:0]	01_0100	RTC Year hundreds register tied to 20(dec)	
	7:0	RTC_YUNITS[7:0]	0000_0000	RTC Year units register with range 0-99.	

Register 13h RTC Year

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R20 (14h) Alarm Seconds/Minutes	14:8	RTC_ALMMINS[6:0]	000_0000	Minutes alarm register with range 0-59. All 1's sets to 'don't care' state. Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.	
	6:0	RTC_ALMSECS[6:0]	000_0000	Seconds alarm register with range 0-59. All 1's set to 'don't care' state. Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.	

Register 14h Alarm Seconds/Minutes

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R21 (15h) Alarm Hours/Day	11:8	RTC_ALMDAY[3:0]	0000	Day alarm register, with range 1-7, 1 = Sunday. All 1's sets to 'don't care' state. Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.	
	5	RTC_ALMHPM	0	Alarm hours AM/PM flag 0 = AM 1 = PM Only applicable in 12 hour mode. In 24 hour mode set to 1 if RTC_ALMHRS is set to all 1's 'don't care' or 0 otherwise.	
	4:0	RTC_ALMHRS[4:0]	0_0000	Hours alarm register with range 0-23 in 24 hours mode and 1-12 in 12 hour. In 12 hour mode bit 5 is used as PM/not-AM flag. All 1's sets to 'don't care' state. Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.	

Register 15h Alarm Hours/Day

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R22 (16h) Alarm Date/Month	12:8	RTC_ALMMTH[4:0]	0_0000	Month alarm register with range 1-12. All 1's sets to 'don't care' state. Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.	
	5:0	RTC_ALMDATE[5:0]	00_0000	Date alarm register with range 1-31. All 1's sets to 'don't care' state. Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.	

Register 16h Alarm Date/Month

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R23 (17h) RTC Time Control	15	RTC_BCD	0	RTC Coding (applies to all time registers) 0 = Binary 1 = BCD	
	14	RTC_12HR	0	RTC 12/24 hours mode 1 = 12 hours (MSB of RTC_HRS indicates AM/PM) 0 = 24 hours (MSB of RTC_HRS is 0)	
	11	RTC_SET	0	Stops RTC seconds counter (instruction only) 0 = normal operation 1 = stop counter	
	10	RTC_STS	0	Status of RTC seconds counter 0 = normal operation 1 = counter stopped	
	9	RTC_ALMSET	1	Stops alarms (instruction only) 0 = normal operation 1 = stop alarms It is recommended to stop alarms when setting the RTC alarm. This avoids false alarms.	
	8	RTC_ALMSTS	1	Actual status of ALARM circuitry 0 = normal operation 1 = alarms stopped	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:4	RTC_PINT[2:0]	010	Selects frequency of periodic interrupt output pulse (32kHz period duration) as shown below. When set time status is high, the periodic output is disabled. 000 = disabled 001 = 1 sec 010 = 1 min 011 = 1 hour 100 = 1 day 101 = 1 month 11x = disabled	
	3:0	RTC_DSW[3:0]	0000	Divided Square wave select. 0000 = disabled 0001 = 1Hz 0010 = 2Hz … 1011 = 1024Hz 1100 = 2048Hz 1101 = 4096Hz 1110 = 8192Hz 1111 = 16384Hz Note: due to trim settings for crystal intolerances a single square wave period during seconds rollover may be decrease its on time period or increase its off time period by up to 8 32kHz periods.	

Register 17h RTC Time Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R24 (18h) System Interrupts	13	OC_INT	0	First-level over-current interrupt. Note: This bit is cleared once read.	
	12	UV_INT	0	First-level under-voltage interrupt. Note: This bit is cleared once read.	
	9	CS_INT	0	First-level current sink interrupt. Note: This bit is cleared once read.	
	8	EXT_INT	0	First-level external interrupt. Note: This bit is cleared once read.	
	7	CODEC_INT	0	First-level codec interrupt. Note: This bit is cleared once read.	
	6	GP_INT	0	First-level GPIO interrupt. Note: This bit is cleared once read.	
	5	AUXADC_INT	0	First-level AUXADC comparator interrupt. Note: This bit is cleared once read.	
	4	RTC_INT	0	First-level RTC interrupt. Note: This bit is cleared once read.	
	3	SYS_INT	0	First-level system interrupt. Note: This bit is cleared once read.	
	2	CHG_INT	0	First-level charger interrupt. Note: This bit is cleared once read.	
	1	USB_INT	0	First-level USB interrupt. Note: This bit is cleared once read.	
	0	WKUP_INT	0	First-level wakeup interrupt. Note: This bit is cleared once read.	

Register 18h System Interrupts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R25 (19h) Interrupt Status 1	15	CHG_BATT_HOT_EINT	0	Battery temp too hot. (Rising Edge triggered) Note: This bit is cleared once read.	
	14	CHG_BATT_COLD_EINT	0	Battery temp too cold. (Rising Edge triggered) Note: This bit is cleared once read.	
	13	CHG_BATT_FAIL_EINT	0	Battery fail. (Rising Edge triggered) Note: This bit is cleared once read.	
	12	CHG_TO_EINT	0	Charger timeout. (Rising Edge triggered) Note: This bit is cleared once read.	
	11	CHG_END_EINT	0	Charging final stage. (Rising Edge triggered) Note: This bit is cleared once read.	
	10	CHG_START_EINT	0	Charging started. (Rising Edge triggered) Note: This bit is cleared once read.	
	9	CHG_FAST_RDY_EINT	0	Indicates that the charger is ready to go into fast charge. (Rising Edge triggered) Note: This bit is cleared once read.	
	7	RTC_PER_EINT	0	RTC periodic interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	6	RTC_SEC_EINT	0	RTC 1s rollover complete (1Hz tick). (Rising Edge triggered) Note: This bit is cleared once read.	
	5	RTC_ALM_EINT	0	RTC alarm signalled. (Rising Edge triggered) Note: This bit is cleared once read.	
	2	CHG_VBATT_LT_3P9_EINT	0	Battery Voltage < 3.9 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	1	CHG_VBATT_LT_3P1_EINT	0	Battery voltage < 3.1 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	0	CHG_VBATT_LT_2P85_EINT	0	Battery voltage < 2.85 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	

Register 19h Interrupt Status 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R26 (1Ah) Interrupt Status 2	13	CS1_EINT	0	Flag to indicate drain voltage can no longer be regulated and output current may be out of spec. (Rising Edge triggered) Note: This bit is cleared once read.	
	10	USB_LIMIT_EINT	0	USB limit switch interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	8	AUXADC_DATARDY_EINT	0	Auxiliary data ready. (Rising Edge triggered) Note: This bit is cleared once read.	
	7	AUXADC_DCOMP4_EINT	0	DCOMP4 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	6	AUXADC_DCOMP3_EINT	0	DCOMP3 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	5	AUXADC_DCOMP2_EINT	0	DCOMP2 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	4	AUXADC_DCOMP1_EINT	0	DCOMP1 interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	3	SYS_HYST_COMP_FAIL_EINT	0	Hysteresis comparator indication that LINE or BATT is less that shutdown threshold. (Rising Edge triggered) Note: This bit is cleared once read.	
	2	SYS_CHIP_GT115_EINT	0	Chip over 115°C temp limit. (Rising Edge triggered) Note: This bit is cleared once read.	
	1	SYS_CHIP_GT140_EINT	0	Chip over 140°C temp limit. (Rising Edge triggered) Note: This bit is cleared once read.	
	0	SYS_WDOG_TO_EINT	0	Watchdog timeout has occurred. (Rising Edge triggered) Note: This bit is cleared once read.	

Register 1Ah Interrupt Status 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R28 (1Ch) Under Voltage Interrupt status	11	UV_LDO4_EINT	0	LDO4 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	10	UV_LDO3_EINT	0	LDO3 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	9	UV_LDO2_EINT	0	LDO2 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	8	UV_LDO1_EINT	0	LDO1 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	3	UV_DC4_EINT	0	DCDC4 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	2	UV_DC3_EINT	0	DCDC3 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	1	UV_DC2_EINT	0	DCDC2 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	
	0	UV_DC1_EINT	0	DCDC1 Under-voltage interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	

Register 1Ch Under Voltage Interrupt status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R29 (1Dh) Over Current Interrupt status	15	OC_LS_EINT	0	Overcurrent interrupt. (Rising Edge triggered) Note: This bit is cleared once read.	

Register 1Dh Over Current Interrupt status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30 (1Eh) GPIO Interrupt Status	12	GP12_EINT	0	GPIO12 interrupt. (Trigger controlled by GP12 registers.) Note: This bit is cleared once read.	
	11	GP11_EINT	0	GPIO11 interrupt. (Trigger controlled by GP11 registers.) Note: This bit is cleared once read.	
	10	GP10_EINT	0	GPIO10 interrupt. (Trigger controlled by GP10 registers.) Note: This bit is cleared once read.	
	9	GP9_EINT	0	GPIO9 interrupt. (Trigger controlled by GP9 registers.) Note: This bit is cleared once read.	
	8	GP8_EINT	0	GPIO8 interrupt. (Trigger controlled by GP8 registers.) Note: This bit is cleared once read.	
	7	GP7_EINT	0	GPIO7 interrupt. (Trigger controlled by GP7 registers.) Note: This bit is cleared once read.	
	6	GP6_EINT	0	GPIO6 interrupt. (Trigger controlled by GP6 registers.) Note: This bit is cleared once read.	
	5	GP5_EINT	0	GPIO5 interrupt. (Trigger controlled by GP5 registers.) Note: This bit is cleared once read.	
	4	GP4_EINT	0	GPIO4 interrupt. (Trigger controlled by GP4 registers.) Note: This bit is cleared once read.	
	3	GP3_EINT	0	GPIO3interrupt. (Trigger controlled by GP3 registers.) Note: This bit is cleared once read.	
	2	GP2_EINT	0	GPIO2 interrupt. (Trigger controlled by GP2 registers.) Note: This bit is cleared once read.	
	1	GP1_EINT	0	GPIO1 interrupt. (Trigger controlled by GP1 registers.) Note: This bit is cleared once read.	
	0	GP0_EINT	0	GPIO0 interrupt. (Trigger controlled by GP0 registers.) Note: This bit is cleared once read.	

Register 1Eh GPIO Interrupt Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R31 (1Fh) Comparator Interrupt Status	15	EXT_USB_FB_EINT	0	USB_FB changed interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.	
	14	EXT_WALL_FB_EINT	0	WALL_FB changed interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.	
	13	EXT_BATT_FB_EINT	0	BATT_FB changed interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.	
	11	CODEC_JCK_DET_L_EINT	0	Left channel Jack detction interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.	
	10	CODEC_JCK_DET_R_EINT	0	Right channel Jack detction interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.	
	9	CODEC_MICSCD_EINT	0	Mic short-circuit detect interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.	
	8	CODEC_MICD_EINT	0	Mic detect interrupt. (Rising and Falling Edge triggered) Note: This bit is cleared once read.	
	6	WKUP_OFF_STATE_EINT	0	Indicates that the chip started from the OFF state. (Rising Edge triggered) Note: This bit is cleared once read.	
	5	WKUP_HIB_STATE_EINT	0	Indicated the chip started up from the hibernate state. (Rising Edge triggered) Note: This bit is cleared once read.	
	4	WKUP_CONV_FAULT_EINT	0	Indicates the wakeup was caused by a converter fault leading to the chip being reset. (Rising Edge triggered) Note: This bit is cleared once read.	
	3	WKUP_WDOG_RST_EINT	0	Indicates the wakeup was caused by a watchdog heartbeat being missed, and hence the chip being reset. (Rising Edge triggered) Note: This bit is cleared once read.	
	2	WKUP_GP_PWR_ON_EINT	0	PWR_ON (Alternate GPIO function) pin has been pressed for longer than specified time. (Rising Edge triggered) Note: This bit is cleared once read.	
	1	WKUP_ONKEY_EINT	0	ON key has been pressed for longer than specified time. (Rising Edge triggered) Note: This bit is cleared once read.	
	0	WKUP_GP_WAKEUP_EINT	0	WAKEUP (Alternate GPIO function) pin has been pressed for longer than specified time. (Rising Edge triggered) Note: This bit is cleared once read.	

Register 1Fh Comparator Interrupt Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R32 (20h) System Interrupts Mask	13	IM_OC_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	12	IM_UV_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	9	IM_CS_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	8	IM_EXT_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	7	IM_CODEC_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	6	IM_GP_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	5	IM_AUXADC_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	4	IM_RTC_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	3	IM_SYS_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	2	IM_CHG_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	1	IM_USB_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	
	0	IM_WKUP_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine. Default held in metal mask.*	

Register 20h System Interrupts Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R33 (21h) Interrupt Status 1 Mask	15	IM_CHG_BATT_HOT_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	14	IM_CHG_BATT_COLD_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	13	IM_CHG_BATT_FAIL_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	12	IM_CHG_TO_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	11	IM_CHG_END_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	10	IM_CHG_START_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	9	IM_CHG_FAST_RDY_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	7	IM_RTC_PER_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	6	IM_RTC_SEC_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	5	IM_RTC_ALM_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	2	IM_CHG_VBATT_LT_3P9_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	1	IM_CHG_VBATT_LT_3P1_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	0	IM_CHG_VBATT_LT_2P85_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	

Register 21h Interrupt Status 1 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R34 (22h) Interrupt Status 2 Mask	13	IM_CS1_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	12	IM_CS2_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	10	IM_USB_LIMIT_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	7	IM_AUXADC_DCOMP4_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	6	IM_AUXADC_DCOMP3_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	5	IM_AUXADC_DCOMP2_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	4	IM_AUXADC_DCOMP1_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	3	IM_SYS_HYST_COMP_FAIL_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	2	IM_SYS_CHIP_GT115_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	1	IM_SYS_CHIP_GT140_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	0	IM_SYS_WDOG_TO_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	

Register 22h Interrupt Status 2 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R36 (24h) Under Voltage Interrupt status Mask	11	IM_UV_LDO4_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	10	IM_UV_LDO3_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	9	IM_UV_LDO2_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	8	IM_UV_LDO1_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	3	IM_UV_DC4_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	2	IM_UV_DC3_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	1	IM_UV_DC2_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	0	IM_UV_DC1_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	

Register 24h Under Voltage Interrupt status Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R37 (25h) Over Current Interrupt status Mask	15	IM_OC_LS_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	

Register 25h Over Current Interrupt status Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R38 (26h) GPIO Interrupt Status Mask	12	IM_GP12_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	11	IM_GP11_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	10	IM_GP10_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	9	IM_GP9_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	8	IM_GP8_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	7	IM_GP7_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	6	IM_GP6_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	5	IM_GP5_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	4	IM_GP4_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	3	IM_GP3_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	2	IM_GP2_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	1	IM_GP1_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	IM_GP0_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	

Register 26h GPIO Interrupt Status Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R39 (27h) Comparator Interrupt Status Mask	15	IM_EXT_USB_FB_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	14	IM_EXT_WALL_FB_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	13	IM_EXT_BATT_FB_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	11	IM_CODEC_JCK_DET_L_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	10	IM_CODEC_JCK_DET_R_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	9	IM_CODEC_MICSCD_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	8	IM_CODEC_MICD_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	6	IM_WKUP_OFF_STATE_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	5	IM_WKUP_HIB_STATE_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	4	IM_WKUP_CONV_FAULT_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	3	IM_WKUP_WDOG_RST_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2	IM_WKUP_GP_PWR_ON_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	1	IM_WKUP_ONKEY_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	
	0	IM_WKUP_GP_WAKEUP_EINT	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. *Reset by state machine.*	

Register 27h Comparator Interrupt Status Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R40 (28h) Clock Control 1	15	TOCLK_ENA	0	Slow clock enable. Used for both the jack insert detect debounce circuit and the zero cross timeout. 0 = slow clock disabled 1 = slow clock enabled	
	14	TOCLK_RATE	0	Slow Clock Selection (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / 2^21 (Slower Response) 1 = SYSCLK / 2^19 (Faster Response)	
	11	MCLK_SEL	0	Selects source for SYSCLK to CODEC 0 = MCLK pin 1 = FLL	
	8	MCLK_DIV	0	Selects MCLK division in slave (MCLK input) mode: 0 = divide MCLK by 1 1 = divide MCLK by 2	
	7:4	BCLK_DIV[3:0]	0100	Sets BCLK rate for Master mode 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0101 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 = SYSCLK / 32 1110 = SYSCLK / 32 1111 = SYSCLK / 32	
	2:0	OPCLK_DIV[2:0]	000	OPCLK Frequency (GPIO function) 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				100 = SYSCLK / 5.5 101 = SYSCLK / 6 110 = Reserved 111 = Reserved	

Register 28h Clock Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R41 (29h) Clock Control 2	15	LRC_ADC_SEL	0	Selects either ADCLRCLK or DACLRCLK to drive LRCLK pin in Master mode 0 = DACLRCLK 1 = ADCLRCLK	
	0	MCLK_DIR	0	Whether MCLK is an input or an output. 0 = MCLK is an input 1 = MCLK is an output	

Register 29h Clock Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R42 (2Ah) FLL Control 1	15	FLL_ENA	0	Digital Enable for FLL 0 = disabled 1 = enabled Note that FLL_OSC_ENA must be enabled before enabling FLL_ENA.	
	14	FLL_OSC_ENA	0	Analogue Enable for FLL 0 = FLL disabled 1 = FLL enabled Note that FLL_OSC_ENA must be enabled before enabling FLL_ENA.	
	10:8	FLL_OUTDIV[2:0]	010	FOUT clock divider 000 = FVCO / 2 001 = FVCO / 4 010 = FVCO / 8 011 = FVCO / 16 100 = FVCO / 32 101 = Reserved 110 = Reserved 111 = Reserved	
	7:4	FLL_RSP_RATE[3:0]	0000	FLL Loop Gain 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that these are not changed from	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				default.	
	2:0	FLL_RATE[2:0]	000	Frequency of the FLL control block 000 = FVCO / 1 (Recommended value) 001 = FVCO / 2 010 = FVCO / 4 011 = FVCO / 8 100 = FVCO / 16 101 = FVCO / 32 Recommended that these are not changed from default.	

Register 2Ah FLL Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R43 (2Bh) FLL Control 2	15:11	FLL_RATIO[4:0]	14 (0Eh)	CLK_VCO is divided by this integer, valid from 1 …31. 1 recommended for high freq reference 8 recommended for low freq reference	
	9:0	FLL_N[9:0]	086h	FLL integer multiplier N for CLK_REF	

Register 2Bh FLL Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R44 (2Ch) FLL Control 3	15:0	FLL_K[15:0]	C226h	FLL fractional multiplier K for CLK_REF. This is only used if FLL_FRAC is set.	

Register 2Ch FLL Control 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R45 (2Dh) FLL Control 4	7	FLL_REF_FREQ	0	Low frequency reference locking 0 = High frequency reference locking (recommended for reference clock > 48kHz) 1 = Lock frequency reference locking (recommended for reference clock <= 48kHz)	
	5	FLL_FRAC	0	Fractional enable 0 = Integer Mode 1 = Fractional Mode 1 recommended in all cases	
	1:0	FLL_CLK_SRC[1:0]	00	Select FLL input clock Source 00 = MCLK 01 = DACLRCLK 10 = ADCLRCLK 11 = CLK_32K_REF	

Register 2Dh FLL Control 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R48 (30h) DAC Control	13	DAC_MONO	0	Adds left and right channel and halves the resulting output to create a mono output	
	12	AIF_LRCLKRATE	0	Mode Select 1 = USB mode (272 * Fs) 0 = Normal mode (256 * Fs)	
	5:4	DEEMP[1:0]	00	DAC De-emphasis filter control 00 = No de-emphasis 01 = 32kHz sample rate 10 = 44.1kHz sample rate 11 = 48kHz sample rate	
	3	DAC_SDMCLK_RATE	0	DAC_SDMCLK_RATE allows the DAC SDM to be run at a speed higher than 64*fs. This is used for low sample rate modes to allow the SDM to run fast enough to shape the noise so that none of it appears in the audio band. On the previous version, at 8k sample rate you could hear some high frequency noise when playing back through a decent system.	
	1	DACL_DATINV	0	DAC data left channel polarity 0 = Normal 1 = Inverted	
	0	DACR_DATINV	0	DAC data right channel polarity 0 = Normal 1 = Inverted	

Register 30h DAC Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R50 (32h) DAC Digital Volume L	15	DACL_ENA	0	Left DAC enable 0 = disabled 1 = enabled	
	8	DAC_VU	0	DAC left and DAC right volume do not update until a 1 is written to either DAC_VU register bit.	
	7:0	DACL_VOL[7:0]	1100_0000	Left DAC digital volume control: 0000_0000 = Digital mute 0000_0001 = -71.625dB 0000_0010 = -71.25dB … (0.375dB steps) 1100_000 = 0dB	

Register 32h DAC Digital Volume L

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R51 (33h) DAC Digital Volume R	15	DACR_ENA	0	Right DAC enable 0 = disabled 1 = enabled	
	8	DAC_VU	0	DAC left and DAC right volume do not update until a 1 is written to either DAC_VU register bit.	
	7:0	DACR_VOL[7:0]	1100_0000	Right DAC digital volume control: 0000_0000 = Digital mute 0000_0001 = -71.625dB 0000_0010 = -71.25dB … (0.375dB steps) 1100_000 = 0dB	

Register 33h DAC Digital Volume R

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R53 (35h) DAC LR Rate	11	DACLRC_ENA	0	Enables DAC LRC generation in Master mode 0 = disabled 1 = enabled	
	10:0	DACLRC_RATE[10:0]	000_0100_0000	Determines the number of bit clocks per LRC phase (when enabled) 00000000000 = invalid ... 00000000111 = invalid 00000001000 = 8 BCPS … 11111111111 = 2047 BCPS	

Register 35h DAC LR Rate

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R54 (36h) DAC Clock Control	4	DACCLK_POL	0	DAC Clock Polarity 0 = Normal 1 = Inverted	
	2:0	DAC_CLKDIV[2:0]	000	DAC Sample rate divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2 011 = SYSCLK / 3 100 = SYSCLK / 4 101 = SYSCLK / 5.5 110 = SYSCLK / 6 111 = Reserved	

Register 36h DAC Clock Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R58 (3Ah) DAC Mute	14	DAC_MUTE	1	DAC Mute 0 = disabled 1 = enabled	

Register 3Ah DAC Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R59 (3Bh) DAC Mute Volume	14	DAC_MUTEMODE	0	DAC Soft Mute Mode 0 = Disabling soft-mute (DAC_MUTE=0) will cause the volume to change immediately to the DACL_VOL / DACR_VOL settings 1 = Disabling soft-mute (DAC_MUTE=0) will cause the volume to ramp up gradually to the DACL_VOL / DACR_VOL settings	
	13	DAC_MUTERATE	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (24kHz at fs=48k, providing maximum delay of 10.7ms) 1 = Slow ramp (1.5kHz at fs=48k, providing maximum delay of 171ms)	
	12	DAC_SB_FILT	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband mode	

Register 3Bh DAC Mute Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R60 (3Ch) DAC Side	13:12	ADC_TO_DACL[1:0]	00	DAC Left Side-tone Control 11 = Unused 10 = Mix ADCR into DACL 01 = Mix ADCL into DACL 00 = No Side-tone mix into DACL	
	11:10	ADC_TO_DACR[1:0]	00	DAC Right Side-tone Control 11 = Unused 10 = Mix ADCR into DACR 01 = Mix ADCL into DACR 00 = No Side-tone mix into DACR	

Register 3Ch DAC Side

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R64 (40h) ADC Control	15	ADC_HPF_ENA	1	High Pass Filter enable 0 = disabled 1 = enabled	
	9:8	ADC_HPF_CUT[1:0]	00	Select cut-off frequency for high-pass filter 00 = 2^-11 (first order) = 3.7Hz @44.1kHz 01 = 2^-5 (2nd order) = ~250Hz @8kHz 10 = 2^-4 (2nd order) = ~250Hz @16kHz 11 = 2^-3 (2nd order) = ~250Hz @32kHz	
	1	ADCL_DATINV	0	ADC Left channel polarity: 0 = Normal 1 = Inverted	
	0	ADCR_DATINV	0	ADC Right Channel Polarity 0 = Normal 1 = Inverted	

Register 40h ADC Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R66 (42h) ADC Digital Volume L	15	ADCL_ENA	0	Left ADC enable 0 = disabled 1 = enabled	
	8	ADC_VU	0	ADC left and ADC right volume do not update until a 1 is written to either ADC_VU register bit.	
	7:0	ADCL_VOL[7:0]	1100_0000	Left ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -71.625dB 0000 0010 = -71.25dB ... 0.375dB steps up to 1110 1111 = +17.625dB	

Register 42h ADC Digital Volume L

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R67 (43h) ADC Digital Volume R	15	ADCR_ENA	0	Right ADC enable 0 = disabled 1 = enabled	
	8	ADC_VU	0	ADC left and ADC right volume do not update until a 1 is written to either ADC_VU register bit.	
	7:0	ADCR_VOL[7:0]	1100_0000	Right ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -71.625dB 0000 0010 = -71.25dB ... 0.375dB steps up to 1110 1111 = +17.625dB	

Register 43h ADC Digital Volume R

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R68 (44h) ADC Divider	11:8	ADCL_DAC_SVOL[3:0]	0000	Controls left digital side tone volume from -36dB to 0dB in 3dB steps.	
	7:4	ADCR_DAC_SVOL[3:0]	0000	Controls right digital side tone volume from -36dB to 0dB in 3dB steps.	
	3	ADCCLK_POL	0	ADC Clock Polarity 0 = Normal 1 = Inverted	
	2:0	ADC_CLKDIV[2:0]	000	ADC Sample rate divider 000 = SYSCLK / 1.0 001 = SYSCLK / 1.5 010 = SYSCLK / 2 011 = SYSCLK / 3 100 = SYSCLK / 4 101 = SYSCLK / 5.5 110 = SYSCLK / 6 111 = Reserved	

Register 44h ADC Divider

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R70 (46h) ADC LR Rate	11	ADCLRC_ENA	0	Enables the LRC generation for the ADC 0 = disabled 1 = enabled	
	10:0	ADCLRC_RATE[10:0]	000_0100_0000	Determines the number of bit clocks per LRC phase (when enabled) 00000000000 = invalid ... 00000000111 = invalid 00000001000 = 8 BCPS … 11111111111 = 2047 BCPS	

Register 46h ADC LR Rate

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R72 (48h) Input Control	10	IN2R_ENA	0	Connect IN2R pin to right channel input PGA 0 = IN2R not connected to input PGA amplifier 1 = IN2R connected to input PGA amplifier	
	9	IN1RN_ENA	1	Connect IN1RN pin to right channel input PGA negative terminal. 0 = IN1RN not connected to input PGA 1 = IN1RN connected to right channel input PGA amplifier negative terminal.	
	8	IN1RP_ENA	1	Connect IN1RP pin to right channel input PGA amplifier positive terminal. 0 = IN1RP not connected to input PGA 1 = right channel input PGA amplifier positive terminal connected to IN1RP (constant input impedance)	
	2	IN2L_ENA	0	Connect IN2L pin to left channel input PGA amplifier 0 = IN2L not connected to input PGA amplifier 1 = IN2L connected to input PGA amplifier	
	1	IN1LN_ENA	1	Connect IN1LN pin to left channel input PGA negative terminal. 0 = IN1LN not connected to input PGA 1 = IN1LN connected to input PGA amplifier negative terminal.	
	0	IN1LP_ENA	1	Connect IN1LP pin to left channel input PGA amplifier positive terminal. 0 = IN1LP not connected to input PGA 1 = input PGA amplifier positive terminal connected to IN1LP (constant input impedance)	

Register 48h Input Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R73 (49h) IN3 Input Control	15	IN3R_ENA	0	IN3R Amplifier enable 0 = disabled 1 = enabled	
	14	IN3R_SHORT	0	Short circuit internal input resistor for IN3R amplifier. 0 = Internal resistor in circuit. 1 = Internal resistor shorted.	
	7	IN3L_ENA	0	IN3L Amplifier enable 0 = disabled 1 = enabled	
	6	IN3L_SHORT	0	Short circuit internal input resistor for IN3L amplifier. 0 = Internal resistor in circuit. 1 = Internal resistor shorted.	

Register 49h IN3 Input Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R74 (4Ah) Mic Bias Control	15	MICB_ENA	0	Microphone bias enable 0 = OFF (high impedance output) 1 = ON	
	14	MICB_SEL	0	Microphone bias voltage control: 0 = 0.9 * AVDD 1 = 0.75 * AVDD	
	7	MIC_DET_ENA	0	Enable MIC detect: 0 = Disabled 1 = Enabled	
	4:2	MCDTHR[2:0]	000	Threshold for bias current detection 000 = 160µA 001 = 330µA 010 = 500µA 011 = 680µA 100 = 850µA 101 = 1000µA 110 = 1200µA 111 = 1400µA These threshold currents scale proportionally with AVDD. The values given are for AVDD=3.3V.	
	1:0	MCDSCTHR[1:0]	00	Threshold for microphone short-circuit detection 00 = 400µA 01 = 900µA 10 = 1350µA 11 = 1800µA These threshold currents scale proportionally with AVDD. The values given are for AVDD=3.3V.	

Register 4Ah Mic Bias Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R76 (4Ch) Output Control	11	OUT4_VROI	0	VREF (AVDD/2) to OUT4 resistance 0 = approx 500 ohms 1 = approx 30 kOhms	
	10	OUT3_VROI	0	VREF (AVDD/2) to OUT3 resistance 0 = approx 500 ohms 1 = approx 30 kOhms	
	9	OUT2_VROI	0	VREF (AVDD/2) to OUT2L and OUT2R resistance 0 = approx 500 ohms 1 = approx 30 kOhms	
	8	OUT1_VROI	0	VREF (AVDD/2) to OUT1L and OUT1R resistance 0 = approx 500 ohms 1 = approx 30 kOhms	
	4	OUTPUT_DRAIN_ENA	0	Enables a drain on the outputs allowing the amplifiers to shutdown more quickly. 0 = Shutdown as normal 1 = Sink current from an external capacitor, allowing faster shutdown.	
	2	OUT2_FB	0	Enable Headphone common mode ground feedback for OUT2 0 = disabled (HPCOM unused) 1 = enabled (common mode feedback through HPCOM)	
	0	OUT1_FB	0	Enable Headphone common mode ground feedback for OUT1 0 = disabled (HPCOM unused) 1 = enabled (common mode feedback through HPCOM)	

Register 4Ch Output Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R77 (4Dh) Jack Detect	15	JDL_ENA	0	Jack Detect Enable for inputs connected to IN2L 0 = disabled 1 = enabled	
	14	JDR_ENA	0	Jack Detect Enable for input connected to IN2R 0 = disabled 1 = enabled	

Register 4Dh Jack Detect

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R78 (4Eh) Anti Pop Control	9:8	ANTI_POP[1:0]	00	Reduces pop when VMID is enabled by setting the speed of the S-ramp for VMID. 00 = no S-ramp (will pop) 01 = Fastest S-curve 10 = Medium S-curve 11 = Slowest S-curve	
	7:6	DIS_OP_LN4[1:0]	00	Sets the Discharge rate for OUT4 00 = discharge path OFF 01 = fastest discharge 10 = medium discharge 11 = slowest discharge	
	5:4	DIS_OP_LN3[1:0]	00	Sets the Discharge rate for OUT3 00 = discharge path OFF 01 = fastest discharge 10 = medium discharge 11 = slowest discharge	
	3:2	DIS_OP_OUT2[1:0]	00	Sets the discharge rate for OUT2L and OUT2R 00 = discharge path OFF 01 = fastest discharge 10 = medium discharge 11 = slowest discharge	
	1:0	DIS_OP_OUT1[1:0]	00	Sets the discharge rate for OUT1L and OUT1R 00 = discharge path OFF 01 = fastest discharge 10 = medium discharge 11 = slowest discharge	

Register 4Eh Anti Pop Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R80 (50h) Left Input Volume	15	INL_ENA	0	Left input PGA enable 0 = disabled 1 = enabled	
	14	INL_MUTE	0	Mute control for left channel input PGA: 0 = Input PGA not muted, normal operation 1 = Input PGA muted (and disconnected from the following input record mixer).	
	13	INL_ZC	0	Left channel input PGA zero cross enable: 0 = Update gain when gain register changes 1 = Update gain on 1st zero cross after gain register write.	
	8	IN_VU	0	Input left PGA and input right PGA volume do not update until a 1 is written to either IN_VU register bit.	
	7:2	INL_VOL[5:0]	01_0000	Left channel input PGA volume 000000 = -12dB 000001 = -11.25dB . 010000 = 0dB . 111111 = 35.25dB	

Register 50h Left Input Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R81 (51h) Right Input Volume	15	INR_ENA	0	Right input PGA enable 0 = disabled 1 = enabled	
	14	INR_MUTE	0	Mute control for right channel input PGA: 0 = Input PGA not muted, normal operation 1 = Input PGA muted (and disconnected from the following input record mixer).	
	13	INR_ZC	0	Right channel input PGA zero cross enable: 0 = Update gain when gain register changes 1 = Update gain on 1st zero cross after gain register write.	
	8	IN_VU	0	Input left PGA and input right PGA volume do not update until a 1 is written to either IN_VU register bit.	
	7:2	INR_VOL[5:0]	01_0000	Right channel input PGA volume 000000 = -12dB 000001 = -11.25dB . 010000 = 0dB . 111111 = 35.25dB	

Register 51h Right Input Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R88 (58h) Left Mixer Control	15	MIXOUTL_ENA	0	Left output mixer enable. 0 = disabled 1 = enabled	
	12	DACR_TO_MIXOUTL	0	Right DAC output to left output mixer 0 = not selected 1 = selected	
	11	DACL_TO_MIXOUTL	1	Left DAC output to left output mixer 0 = not selected 1 = selected	
	2	IN3L_TO_MIXOUTL	0	IN3L amplifier output to left output mixer: 0 = not selected 1 = selected	
	1	INR_TO_MIXOUTL	0	Right input PGA output to left output mixer 0 = not selected 1 = selected	
	0	INL_TO_MIXOUTL	0	Left input PGA output to left output mixer 0 = not selected 1 = selected	

Register 58h Left Mixer Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R89 (59h) Right Mixer Control	15	MIXOUTR_ENA	0	Right output mixer enable. 0 = disabled 1 = enabled	
	12	DACR_TO_MIXOUTR	1	Right DAC output to right output mixer 0 = not selected 1 = selected	
	11	DACL_TO_MIXOUTR	0	Left DAC output to right output mixer 0 = not selected 1 = selected	
	3	IN3R_TO_MIXOUTR	0	IN3R amplifier output to right output mixer: 0 = not selected 1 = selected	
	1	INR_TO_MIXOUTR	0	Right input PGA output to right output mixer 0 = not selected 1 = selected	
	0	INL_TO_MIXOUTR	0	Left input PGA output to right output mixer 0 = not selected 1 = selected	

Register 59h Right Mixer Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R92 (5Ch) OUT3 Mixer Control	15	OUT3_ENA	0	OUT3 enable 0 = disabled 1 = enabled	
	11	DACL_TO_OUT3	0	Left DAC output to OUT3 0 = disabled 1 = enabled	
	8	MIXINL_TO_OUT3	0	Left input mixer to OUT3 0 = disabled 1 = enabled	
	3	OUT4_TO_OUT3	0	OUT4 mixer to OUT3 0 = disabled 1 = enabled	
	0	MIXOUTL_TO_OUT3	0	Left output mixer to OUT3 0 = disabled 1 = enabled	

Register 5Ch OUT3 Mixer Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R93 (5Dh) OUT4 Mixer Control	15	OUT4_ENA	0	Enable OUT4 mixer 0 = disabled 1 = enabled	
	12	DACR_TO_OUT4	0	Right DAC output to OUT4 0 = disabled 1 = enabled	
	11	DACL_TO_OUT4	0	Left DAC output to OUT4 0 = Disabled 1 = Enabled	
	10	OUT4_ATTN	0	Reduce OUT4 output by 6dB 0 = Output at normal level 1 = Output reduced by 6dB	
	9	MIXINR_TO_OUT4	0	Right input mixer to OUT4 0 = disabled 1 = enabled	
	2	OUT3_TO_OUT4	0	OUT3 mixer to OUT4 This function is not supported	
	1	MIXOUTR_TO_OUT4	0	Right output mixer to OUT4 0 = disabled 1 = enabled	
	0	MIXOUTL_TO_OUT4	0	Left output mixer to OUT4 0 = disabled 1 = enabled	

Register 5Dh OUT4 Mixer Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R96 (60h) Output Left Mixer Volume	11:9	IN3L_MIXOUTL_VOL[2:0]	000	IN3L amplifier volume control to left output mixer 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer	
	7:5	INR_MIXOUTL_VOL[2:0]	000	Right input PGA volume control to left output mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer	
	3:1	INL_MIXOUTL_VOL[2:0]	000	Left input PGA volume control to left output mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer	

Register 60h Output Left Mixer Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R97 (61h) Output Right Mixer Volume	15:13	IN3R_MIXOUTR_VOL[2:0]	000	IN3R amplifier volume control to right output mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer	
	7:5	INR_MIXOUTR_VOL[2:0]	000	Right input PGA volume control to right output mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer	
	3:1	INL_MIXOUTR_VOL[2:0]	000	Left input PGA volume control to right output mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer	

Register 61h Output Right Mixer Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R98 (62h) Input Mixer Volume L	11:9	IN3L_MIXINL_VOL[2:0]	000	IN3L amplifier volume control to right input mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer	
	3:1	IN2L_MIXINL_VOL[2:0]	000	IN2L amplifier volume control to right input mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer	
	0	INL_MIXINL_VOL	0	Boost enable for left channel input PGA: 0 = PGA output has +0dB gain through input record mixer. 1 = PGA output has +20dB gain through input record mixer.	

Register 62h Input Mixer Volume L

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R99 (63h) Input Mixer Volume R	15:13	IN3R_MIXINR_VOL[2:0]	000	IN3R amplifier volume control to right input mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer	
	7:5	IN2R_MIXINR_VOL[2:0]	000	IN2R amplifier volume control to right input mixer. 000 = Path disabled (disconnected) 001 = -12dB gain through mixer 010 = -9dB gain through mixer … 111 = +6dB gain through mixer	
	0	INR_MIXINR_VOL	0	Boost enable for right channel input PGA: 0 = PGA output has +0dB gain through input record mixer. 1 = PGA output has +20dB gain through input record mixer.	

Register 63h Input Mixer Volume R

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R100 (64h) Input Mixer Volume	15	OUT4_MIXIN_DST	0	Select routing of OUT4 to input mixers. 0 = OUT4 to left input mixer. 1 = OUT4 to right input mixer.	
	3:1	OUT4_MIXIN_VOL[2:0]	000	Controls the gain of OUT4 to left and right input mixers: 000 = Path disabled (left and right mute) 001 = -12dB gain through boost stages 010 = -9dB gain through boost stages …. 111 = +6dB gain through boost stages	

Register 64h Input Mixer Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R104 (68h) OUT1L Volume	15	OUT1L_ENA	0	OUT1L enable 0 = disabled 1 = enabled	
	14	OUT1L_MUTE	0	OUT1L mute: 0 = normal operation 1 = mute	
	13	OUT1L_ZC	0	OUT1L volume zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only	
	8	OUT1_VU	0	OUT1L and OUT1R volumes do not update until a 1 is written to either OUT1_VU.	
	7:2	OUT1L_VOL[5:0]	11_1001	OUT1L volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB	

Register 68h OUT1L Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R105 (69h) OUT1R Volume	15	OUT1R_ENA	0	OUT1R enable 0 = disabled 1 = enabled	
	14	OUT1R_MUTE	0	OUT1R mute: 0 = normal operation 1 = mute	
	13	OUT1R_ZC	0	OUT1R volume zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only	
	8	OUT1_VU	0	OUT1L and OUT1R volumes do not update until a 1 is written to either OUT1_VU register bits.	
	7:2	OUT1R_VOL[5:0]	11_1001	OUT1R volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB	

Register 69h OUT1R Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R106 (6Ah) OUT2L Volume	15	OUT2L_ENA	0	OUT2L enable 0 = disabled 1 = enabled	
	14	OUT2L_MUTE	0	OUT2L mute: 0 = normal operation 1 = mute	
	13	OUT2L_ZC	0	OUT2L volume zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only	
	8	OUT2_VU	0	OUT2L and OUT2R volumes do not update until a 1 is written to either OUT2_VU register bits.	
	7:2	OUT2L_VOL[5:0]	11_1001	OUT2L volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB	

Register 6Ah OUT2L Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R107 (6Bh) OUT2R Volume	15	OUT2R_ENA	0	OUT2R enable 0 = disabled 1 = enabled	
	14	OUT2R_MUTE	0	OUT2R mute: 0 = normal operation 1 = mute	
	13	OUT2R_ZC	0	OUT2R volume zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only	
	10	OUT2R_INV	0	Enable OUT2R inverting amplifier 0 = disabled 1 = enabled This register must be set to 0 when using the non-inverting MIXOUT2R to OUT2R path. This register must be set to 1 when using the inverting MIXOUT2R to OUT2R path.	
	9	OUT2R_INV_MUTE	1	Mute output of PGA to inverting amplifier. 0 = PGA output goes to inverting amplifier 1 = PGA output goes to output driver This register must be set to 0 when using the inverting MIXOUT2R to OUT2R path. This register must be set to 1 when using the non-inverting MIXOUT2R to OUT2R path.	
	8	OUT2_VU	0	OUT2L and OUT2R volumes do not update until a 1 is written to either OUT2_VU register bits.	
	7:2	OUT2R_VOL[5:0]	11_1001	OUT2R volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB	

Register 6Bh OUT2R Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R111 (6Fh) BEEP Volume	15	IN3R_TO_OUT2R	0	Beep mixer enable 0 = disabled 1 = enabled	
	7:5	IN3R_OUT2R_VOL[2:0]	000	Beep mixer volume: 000 = -15dB … in +3dB steps 111 = +6dB	

Register 6Fh BEEP Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R112 (70h) AI Formating	15	AIF_BCLK_INV	0	0 = normal 1 = inverted	
	13	AIF_TRI	0	Sets Output enables for LRCLK and BCLK and ADCDAT to inactive state 0 = normal 1 = forces pins to Hi-Z	
	12	AIF_LRCLK_INV	0	LRCLK clock polarity 0 = normal 1 = inverted DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRCLK rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRCLK rising edge (mode B)	
	11:10	AIF_WL[1:0]	10	Data word length 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits Note: When using the Right-Justified data format (FMT=00), the maximum word length is 24 bits.	
	9:8	AIF_FMT[1:0]	10	00 = Right-justified 01 = Left justified 10 = I2S 11 = DSP / PCM mode	

Register 70h AI Formating

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R113 (71h) ADC DAC COMP	7	DAC_COMP	0	DAC Companding enable 0 = disabled 1 = enabled	
	6	DAC_COMPMODE	0	DAC Companding mode select: 0 = µ-law 1 = A-law (Note: Setting ADC_COMPMODE=1 selects 8-bit mode when DAC_COMP=0 and ADC_COMP=0)	
	5	ADC_COMP	0	ADC Companding enable 0 = disabled 1 = enabled	
	4	ADC_COMPMODE	0	ADC Companding mode select: 0 = µ-law 1 = A-law (Note: Setting ADC_COMPMODE=1 selects 8-bit mode when DAC_COMP=0 and ADC_COMP=0)	
	0	LOOPBACK	0	Digital Loopback Function 0 = No loopback. 1 = Loopback enabled, ADC data output is fed directly into DAC data input.	

Register 71h ADC DAC COMP

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R114 (72h) AI ADC Control	7	AIFADC_PD	0	Enables a pull down on ADC data pin 0 = disabled 1 = enabled	
	6	AIFADCL_SRC	0	Selects Left channel ADC output. 0 = ADC Left channel 1 = ADC Right channel	
	5	AIFADCR_SRC	1	Selects Right channel ADC output. 0 = ADC Left channel 1 = ADC Right channel	
	4	AIFADC_TDM_CHAN	0	ADCDAT TDM Channel Select 0 = ADCDAT outputs data on slot 0 1 = ADCDAT outputs data on slot 1	
	3	AIFADC_TDM	0	ADC TDM Enable 0 = Normal ADCDAT operation 1 = TDM enabled on ADCDAT	

Register 72h AI ADC Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R115 (73h) AI DAC Control	14	BCLK_MSTR	0	Enables the Audio Interface BCLK generation and enables the BCLK pin for Master mode 0 = BCLK Slave mode 1 = BCLK Master mode	
	7	AIFDAC_PD	0	Enables a pull down on DAC data pin 0 = disabled 1 = enabled	
	6	DACL_SRC	0	Selects Left channel DAC input. 0 = DAC Left channel 1 = DAC Right channel	
	5	DACR_SRC	1	Selects Right channel DAC input. 0 = DAC Left channel 1 = DAC Right channel	
	4	AIFDAC_TDM_CHAN	0	DACDAT TDM Channel Select 0 = DACDAT outputs data on slot 0 1 = DACDAT outputs data on slot 1	
	3	AIFDAC_TDM	0	DAC TDM Enable 0 = Normal DACDAT operation 1 = TDM enabled on DACDAT	
	1:0	DAC_BOOST[1:0]	00	Provides a limited set of gains to be applied to the signal 00 = 0dB 01 = +6dB 10 = +12dB 11 = Reserved (+18dB)	

Register 73h AI DAC Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R128 (80h) GPIO Debounce	12	GP12_DB	1	GPIO12 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	11	GP11_DB	1	GPIO11 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	10	GP10_DB	1	GPIO10 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	9	GP9_DB	1	GPIO9 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	8	GP8_DB	1	GPIO8 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	7	GP7_DB	1	GPIO7 debounce 0 = GPIO is not debounced.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	6	GP6_DB	1	GPIO6 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	5	GP5_DB	1	GPIO5 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	4	GP4_DB	1	GPIO4 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	3	GP3_DB	1	GPIO3 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	2	GP2_DB	1	GPIO2 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	1	GP1_DB	1	GPIO1 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	
	0	GP0_DB	1	GPIO0 debounce 0 = GPIO is not debounced. 1 = GPIO is debounced (time from GP_DBTIME[1:0]) *Reset by state machine.*	

Register 80h GPIO Debounce

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R129 (81h) GPIO Pin pull up Control	12	GP12_PU	0	GPIO12 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO12 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	11	GP11_PU	0	GPIO11 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO11 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	10	GP10_PU	0	GPIO10 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO10 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	9	GP9_PU	0	GPIO9 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO9 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	8	GP8_PU	0	GPIO8 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO8 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	7	GP7_PU	0	GPIO7 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO7 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	6	GP6_PU	0	GPIO6 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO6 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	5	GP5_PU	0	GPIO5 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO5 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	4	GP4_PU	0 0 0 1	GPIO4 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO4 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	3	GP3_PU	0	GPIO3 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO3 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	2	GP2_PU	0	GPIO2 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO2 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	1	GP1_PU	0	GPIO1 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO1 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	GP0_PU	0	GPIO0 pull-up 0 = Normal 1 = Pull-up enabled (Only valid when GPIO0 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	

Register 81h GPIO Pin pull up Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R130 (82h) GPIO Pull down Control	12	GP12_PD	0	GPIO12 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO12 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	11	GP11_PD	0	GPIO11 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO11 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	10	GP10_PD	0	GPIO10 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO10 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	9	GP9_PD	0	GPIO9 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO9 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	8	GP8_PD	0 0 1 0	GPIO8 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO8 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	7	GP7_PD	0	GPIO7 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO7 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	6	GP6_PD	0	GPIO6 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO6 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5	GP5_PD	0	GPIO5 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO5 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	4	GP4_PD	0 0 1 0	GPIO4 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO4 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	3	GP3_PD	0	GPIO3 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO3 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	2	GP2_PD	0	GPIO2 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO2 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	1	GP1_PD	0	GPIO1 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO1 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	
	0	GP0_PD	0	GPIO0 pull-down 0 = Normal 1 = Pull-down enabled (Only valid when GPIO0 is set to input. Do not select pull-up and pull-down at the same time.) *Reset by state machine. Default held in metal mask.*	

Register 82h GPIO Pull down Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R131 (83h) GPIO Interrupt Mode	12	GP12_INTMODE	0	GPIO12 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP12_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	
	11	GP11_INTMODE	0	GPIO11 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP11_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	10	GP10_INTMODE	0	GPIO10 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP10_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	
	9	GP9_INTMODE	0	GPIO9 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP9_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	
	8	GP8_INTMODE	0	GPIO8 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP8_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	
	7	GP7_INTMODE	0	GPIO7 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP7_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	
	6	GP6_INTMODE	0	GPIO6 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP6_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	
	5	GP5_INTMODE	0	GPIO5 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP5_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	
	4	GP4_INTMODE	0	GPIO4 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP4_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	
	3	GP3_INTMODE	0	GPIO3 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP3_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	
	2	GP2_INTMODE	0	GPIO2 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP2_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	GP1_INTMODE	0	GPIO1 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP1_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	
	0	GP0_INTMODE	0	GPIO0 Pin Mode 0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP0_CFG register bit. 1 = GPIO interrupt is both rising and falling edge triggered. *Reset by state machine.*	

Register 83h GPIO Interrupt Mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R133 (85h) GPIO Control	7:6	GP_DBTIME[1:0]	00	Debounce time for all GPIO inputs 00 = 64us 01 = 0.5ms 10 = 1ms 11 = 4ms Note: PWR_ON, PWR_OFF and /WAKEUP have additional debounce times. *Reset by state machine.*	

Register 85h GPIO Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R134 (86h) GPIO Configuration (i/o)	12	GP12_DIR	0	GPIO12 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	11	GP11_DIR	1	GPIO11 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	10	GP10_DIR	1 1 0 0	GPIO10 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	9	GP9_DIR	1 0 0 1	GPIO9 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	8	GP8_DIR	1 0 1 1	GPIO8 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	7	GP7_DIR	1	GPIO7 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6	GP6_DIR	1	GPIO6 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	5	GP5_DIR	1	GPIO5 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	4	GP4_DIR	1	GPIO4 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	3	GP3_DIR	1	GPIO3 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	2	GP2_DIR	1 0 0 0	GPIO2 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	1	GP1_DIR	0 1 1 1	GPIO1 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	
	0	GP0_DIR	0 1 0 1	GPIO0 pin direction 0 = Output 1 = Input *Reset by state machine. Default held in metal mask.*	

Register 86h GPIO Configuration (i/o)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R135 (87h) GPIO Pin Polarity / Type	12	GP12_CFG	0	GPIO12 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	
	11	GP11_CFG	1	GPIO11 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	10	GP10_CFG	1	GPIO10 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	
	9	GP9_CFG	1 0 0 1	GPIO9 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	
	8	GP8_CFG	1 0 1 1	GPIO8 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	
	7	GP7_CFG	1 0 1 1	GPIO7 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	
	6	GP6_CFG	1 0 1 1	GPIO6 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	
	5	GP5_CFG	1 0 1 1	GPIO5 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4	GP4_CFG	1	GPIO4 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	
	3	GP3_CFG	1 1 0 1	GPIO3 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	
	2	GP2_CFG	1	GPIO2 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	
	1	GP1_CFG	0 1 1 0	GPIO1 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	
	0	GP0_CFG	0 1 0 1	GPIO0 pin polarity/type: Input: 0 = Active low 1 = Active high Output: 0 = CMOS 1 = Open drain *Reset by state machine. Default held in metal mask.*	

Register 87h GPIO Pin Polarity / Type

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R140 (8Ch) GPIO Function Select 1	15:12	GP3_FN[3:0]	0000 0000 0001 0000	GPIO3 alternate function: Input: 0000 = GPIO 0001 = PWR_ON 0010 = LDO_ENA 0011 = PWR_OFF 0100 = FLASH Output:	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0000 = GPIO 0001 = P_CLK 0010 = VRTC 0011 = 32kHz 0100 = /MEMRST *Reset by state machine. Default held in metal mask.*	
	11:8	GP2_FN[3:0]	0000 0011 0011 0011	GPIO2 alternate function: Input: 0000 = GPIO 0001 = PWR_ON 0010 = /WAKEUP 0011 = 32KHZ 0100 = L_PWR3 Output: 0000 = GPIO 0001 = PWR_ON 0010 = VRTC 0011 = 32KHZ 0100 = /RST *Reset by state machine. Default held in metal mask.*	
	7:4	GP1_FN[3:0]	0001 0000 0001 0001	GPIO1 alternate function: Input: 0000 = GPIO 0001 = PWR_ON 0010 = /LDO_ENA 0011 = L_PWR2 0100 = /WAKEUP Output: 0000 = GPIO 0001 = DO_CONF 0010 = /RST 0011 = /MEMRST 0100 = 32KHz *Reset by state machine. Default held in metal mask.*	
	3:0	GP0_FN[3:0]	0011 0000 0000 0000	GPIO0 alternate function: Input- 0000 = GPIO 0001 = PWR_ON 0010 = /LDO_ENA 0011 = L_PWR1 0100 = PWR_OFF 0101 = CHIP_RESET Output: 0000 = GPIO 0001 = PWR_ON 0010 = VRTC 0011 = POR_B 0100 = /RST *Reset by state machine. Default held in metal mask.*	

Register 8Ch GPIO Function Select 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R141 (8Dh) GPIO Function Select 2	15:12	GP7_FN[3:0]	0000 0001 0000 0000	GPIO7 alternate function: Input: 0000 = GPIO 0001 = L_PWR3 0010 = MASK 0011 = Hibernate (level) Output: 0000 = GPIO 0001 = P_CLK (1MHz) 0010 = /VCC_FAULT 0011 = /BATT_FAULT 0100 = MICDET 0101 = MICSHT 0110 = ADA 1100 = FLL_CLK*Reset by state machine. Default held in metal mask.*	
	11:8	GP6_FN[3:0]	0000 0001 0000 0000	GPIO6 alternate function: Input: 0000 = GPIO 0001 = L_PWR2 0010 = FLASH 0011 = Hibernate (Edge) 0100 = Hibernate (Level) Output: 0000 = GPIO 0001 = /MEMRST 0010 = ADA 0011 = RTC 0100 = MICDET 0101 = MICSHT 0110 = ADCLRCLKB *Reset by state machine. Default held in metal mask.*	
	7:4	GP5_FN[3:0]	0000 0001 0000 0000	GPIO5 alternate function: Input: 0000 = GPIO 0001 = L_PWR1 0010 = ADCLRCLK 0011 = Hibernate (Edge) 0100 = PWR_OFF 0101 = Hibernate (Level) Output: 0000 = GPIO 0001 = P_CLK 0010 = ADCLRCLK 0011 = 32kHz 0100 = /BATT_FAULT 0101 = MICSHT 0110 = ADA 0111 = CODEC_OPCLK 1010 = MICDET *Reset by state machine. Default held in metal mask.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	GP4_FN[3:0]	0000 0000 0011 0001	GPIO4 alternate function: Input: 0000 = GPIO 0001 = /MR 0010 = FLASH 0011 = Hibernate (level) 0100 = MASK 0101 = CHIP_RESET Output: 0000 = GPIO 0001 = /MEMRST 0010 = ADA 0011 = FLASH_OUT 0100 = /VCC_FAULT 0101 = MICSHT 1010 = MICDET *Reset by state machine. Default held in metal mask.*	

Register 8Dh GPIO Function Select 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R142 (8Eh) GPIO Function Select 3	15:12	GP11_FN[3:0]	0000 0000 0010 0010	GPIO11 alternate function: Input: 0000 = GPIO 0010 = /WAKEUP Output: 0000 = GPIO 0001 = ISINKD 0010 = LINE_GT_BATT 0011 = CH_IND *Reset by state machine. Default held in metal mask.*	
	11:8	GP10_FN[3:0]	0000 0000 0000 0011	GPIO10 alternate function: Input: 0000 = GPIO 0011 = PWR_OFF Output: 0000 = GPIO 0001 = ISINKC 0010 = LINE_GT_BATT 0011 = CH_IND *Reset by state machine. Default held in metal mask.*	
	7:4	GP9_FN[3:0]	0000 0001 0000 0000	GPIO9 alternate function: Input: 0000 = GPIO 0001 = HEARTBEAT 0010 = MASK 0011 = PWR_OFF 0100 = HIBERNATE (Level) Output: 0000 = GPIO 0001 = /VCC_FAULT 0010 = LINE_GT_BATT	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0011 = /BATT_FAULT 0100 = /MEMRST *Reset by state machine. Default held in metal mask.*	
	3:0	GP8_FN[3:0]	0000 0011 0000 0000	GPIO8 alternate function: Input: 0000 = GPIO 0001 = /MR 0010 = ADCBCLK 0011 = PWR_OFF 0100 = HIBERNATE (edge) Output: 0000 = GPIO 0001 = /VCC_FAULT 0010 = ADCBCLK 0011 = /BATT_FAULT 0100 = /RST *Reset by state machine. Default held in metal mask.*	

Register 8Eh GPIO Function Select 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R143 (8Fh) GPIO Function Select 4	3:0	GP12_FN[3:0]	0011 0011 0000 0011	GPIO12 alternate function: Input: 0000 = GPIO 0001 = CHIP_RESET Output: 0000 = GPIO 0001 = ISINKE 0010 = LINE_GT_BATT 0011 = LINE_SW 0100 = 32kHz *Reset by state machine. Default held in metal mask.*	

Register 8Fh GPIO Function Select 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R144 (90h) Digitiser Control (1)	15	AUXADC_ENA	0	AUXADC control 0 = disabled 1 = enabled *Reset by state machine.*	
	14	AUXADC_CTC	0	Continuous conversion mode: 0 = Polling mode 1 = Continuous mode *Reset by state machine.*	
	13	AUXADC_POLL	0	Writing “1” initiates a set of measurements in polling mode (AUXADC_CTC=0). This bit is automatically reset after the measurements are completed. *Reset by state machine.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	12	AUXADC_HIB_MODE	0	AUXADC state in hibernate mode: 0 = Leave AUXADC as in Active 1 = Disable AUXADC. *Reset by state machine.*	
	7	AUXADC_SEL8	0	AUXADC TEMP input select 0 = Disable TEMP measurement 1 = Enable TEMP measurement *Reset by state machine.*	
	6	AUXADC_SEL7	0	AUXADC BATT input select 0 = Disable BATT measurement 1 = Enable BATT measurement *Reset by state machine.*	
	5	AUXADC_SEL6	0	AUXADC LINE input select 0 = Disable LINE measurement 1 = Enable LINE measurement *Reset by state machine.*	
	4	AUXADC_SEL5	0	AUXADC USB input select 0 = Disable USB measurement 1 = Enable USB measurement *Reset by state machine.*	
	3	AUXADC_SEL4	0	AUXADC AUX4 input select 0 = Disable AUX4 measurement 1 = Enable AUX4 measurement *Reset by state machine.*	
	2	AUXADC_SEL3	0	AUXADC AUX3 input select 0 = Disable AUX3 measurement 1 = Enable AUX3 measurement *Reset by state machine.*	
	1	AUXADC_SEL2	0	AUXADC AUX2 input select 0 = Disable AUX2 measurement 1 = Enable AUX2 measurement *Reset by state machine.*	
	0	AUXADC_SEL1	0	AUXADC AUX1 input select 0 = Disable AUX1 measurement 1 = Enable AUX1 measurement *Reset by state machine.*	

Register 90h Digitiser Control (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R145 (91h) Digitiser Control (2)	13:12	AUXADC_MASKMODE[1:0]	00	AUXADC MASK input control 00 = MASK is ignored 01 = When MASK is asserted, all AUXADC measurements are inhibited. 10 = Reserved 11 = MASK input initiates AUXADC measurements. AUXADC_POLL and AUXADC_CTC have no effect. MASK polarity is controlled by GPn_CFG. *Reset by state machine.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	10:8	AUXADC_CRATE[2:0]	000	AUXADC measurement frequency in Continuous mode 000 = 1Hz 001 = 4Hz 010 = 8Hz 011 = 16Hz 100 = 32Hz 101 = 64Hz 110 = 128Hz 111 = 256Hz *Reset by state machine.*	
	2	AUXADC_CAL	0	Configure AUX3 input to be the VREF supply for AUXADC calibration. 0 = AUX3 input connected to AUX3 pin 1 = AUX3 input connected to unbuffered VREF *Reset by state machine.*	
	1	AUXADC_RBMODE	1	Enable for AUXADC bandgap (VREF) buffer. 0 = AUXADC REFBUF is only enabled during conversions that use the VREF as a reference 1 = AUXADC REFBUF is always enabled when the AUXADC is enabled *Reset by state machine.*	
	0	AUXADC_WAIT	0	Whether the old data must be read before new conversions can be made 0 = No effect (new conversions overwrite old) 1 = New conversions are held back (and measurements delayed) until AUX_DATAn has been read. *Reset by state machine.*	

Register 91h Digitiser Control (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R152 (98h) AUX1 Readback	14:13	AUXADC_SCALE1[1:0]	11	AUX1 input select: 00 = Off 01 = Input divided by 1 10 = Input divided by 2 11 = Input divided by 4	
	12	AUXADC_REF1	1	AUX1 reference select 0 = AUX1 measured relative to VRTC 1 = AUX1 measured relative to VREF	
	11:0	AUXADC_DATA1[11:0]	0000_0000_0000	Measured AUX1 data value relative to reference: 000 = 0V FFF = measured voltage after divide matches reference	

Register 98h AUX1 Readback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R153 (99h) AUX2 Readback	14:13	AUXADC_SCALE2[1:0]	11	AUX2 input select: 00 = Off 01 = Input divided by 1 10 = Input divided by 2 11 = Input divided by 4	
	12	AUXADC_REF2	1	AUX2 reference select 0 = AUX2 measured relative to VRTC 1 = AUX2 measured relative to VREF	
	11:0	AUXADC_DATA2[11:0]	0000_0000_0000	Measured AUX2 data value relative to reference: 000 = 0V FFF = measured voltage after divide matches reference	

Register 99h AUX2 Readback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R154 (9Ah) AUX3 Readback	14:13	AUXADC_SCALE3[1:0]	11	AUX3 input select: 00 = Off 01 = Input divided by 1 10 = Input divided by 2 11 = Input divided by 4	
	12	AUXADC_REF3	1	AUX3 reference select 0 = AUX3 measured relative to VRTC 1 = AUX3 measured relative to VREF	
	11:0	AUXADC_DATA3[11:0]	0000_0000_0000	Measured AUX3 data value relative to reference: 000 = 0V FFF = measured voltage after divide matches reference	

Register 9Ah AUX3 Readback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R155 (9Bh) AUX4 Readback	14:13	AUXADC_SCALE4[1:0]	11	AUX4 input select: 00 = Off 01 = Input divided by 1 10 = Input divided by 2 11 = Input divided by 4	
	12	AUXADC_REF4	1	AUX4 reference select 0 = AUX4 measured relative to VRTC 1 = AUX4 measured relative to VREF	
	11:0	AUXADC_DATA4[11:0]	0000_0000_0000	Measured AUX4 data value relative to reference: 000 = 0V FFF = measured voltage after divide matches reference	

Register 9Bh AUX4 Readback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R156 (9Ch) USB Voltage Readback	11:0	AUXADC_DATA_USB[11:0]	0000_0000_0000	Measured USB voltage data value.	

Register 9Ch USB Voltage Readback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R157 (9Dh) LINE Voltage Readback	11:0	AUXADC_DATA_LINE[11:0]	0000_0000_0000	Measured LINE voltage data value.	

Register 9Dh LINE Voltage Readback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R158 (9Eh) BATT Voltage Readback	11:0	AUXADC_DATA_BATT[11:0]	0000_0000_0000	Measured Battery voltage.	

Register 9Eh BATT Voltage Readback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R159 (9Fh) Chip Temp Readback	11:0	AUXADC_DATA_CHIPTEMP[11:0]	0000_0000_0000	Measured internal chip temperature	

Register 9Fh Chip Temp Readback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R163 (A3h) Generic Comparator Control	3	DCMP4_ENA	0	Digital comparator 4 enable 0 = disabled 1 = enabled *Reset by state machine.*	
	2	DCMP3_ENA	0	Digital comparator 3 enable 0 = disabled 1 = enabled *Reset by state machine.*	
	1	DCMP2_ENA	0	Digital comparator 2 enable 0 = disabled 1 = enabled *Reset by state machine.*	
	0	DCMP1_ENA	0	Digital comparator 1 enable 0 = disabled 1 = enabled *Reset by state machine.*	

Register A3h Generic Comparator Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R164 (A4h) Generic comparator 1	15:13	DCMP1_SRCSEL[2:0]	000	DCOMP1 source select. 000 = AUX1 001 = AUX2 010 = AUX3 011 = AUX4 100 = USB 101 = LINE 110 = BATT 111 = TEMP *Reset by state machine.*	
	12	DCMP1_GT	0	DCOMP1 interrupt control 0 = interrupt when the source is less than threshold 1 = interrupt when the source is greater than threshold	
	11:0	DCMP1_THR[11:0]	0000_0000_0000	DCOMP1 threshold (12-bit unsigned binary number)	

Register A4h Generic comparator 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R165 (A5h) Generic comparator 2	15:13	DCMP2_SRCSEL[2:0]	000	DCOMP2 source select. 000 = AUX1 001 = AUX2 010 = AUX3 011 = AUX4 100 = USB 101 = LINE 110 = BATT 111 = TEMP *Reset by state machine.*	
	12	DCMP2_GT	0	DCOMP2 interrupt control 0 = interrupt when the source is less than threshold 1 = interrupt when the source is greater than threshold	
	11:0	DCMP2_THR[11:0]	0000_0000_0000	DCOMP2 threshold (12-bit unsigned binary number)	

Register A5h Generic comparator 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R166 (A6h) Generic comparator 3	15:13	DCMP3_SRCSEL[2:0]	000	DCOMP3 source select. 000 = AUX1 001 = AUX2 010 = AUX3 011 = AUX4 100 = USB 101 = LINE 110 = BATT 111 = TEMP *Reset by state machine.*	
	12	DCMP3_GT	0	DCOMP3 interrupt control 0 = interrupt when the source is less than threshold 1 = interrupt when the source is greater than threshold	
	11:0	DCMP3_THR[11:0]	0000_0000_0000	DCOMP3 threshold (12-bit unsigned binary number)	

Register A6h Generic comparator 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R167 (A7h) Generic comparator 4	15:13	DCMP4_SRCSEL[2:0]	000	DCOMP4 source select. 000 = AUX1 001 = AUX2 010 = AUX3 011 = AUX4 100 = USB 101 = LINE 110 = BATT 111 = TEMP *Reset by state machine.*	
	12	DCMP4_GT	0	DCOMP4 interrupt control 0 = interrupt when the source is less than threshold 1 = interrupt when the source is greater than threshold	
	11:0	DCMP4_THR[11:0]	0000_0000_0000	DCOMP4 threshold (12-bit unsigned binary number)	

Register A7h Generic comparator 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R168 (A8h) Battery Charger Control 1	15	CHG_ENA	1	CHG_ENA bit selects battery charger current control 0 = Set battery charger current to zero 1 = Enable battery charge control *Protected by security key. Reset by state machine. Default held in metal mask.*	
	12:10	CHG_EOC_SEL[2:0]	000	Selects what the end of charge current should be set to 000 = 20mA 001 = 30mA (10mA steps) ... 111 = 90mA *Protected by security key.*	
	9	CHG_TRICKLE_TEMP_CHOKE	0	Enable trickle charge temperature choking 0 = disable 1 = enable *Protected by security key. Reset by state machine.*	
	8	CHG_TRICKLE_USB_CHOKE	0	Enable USB current choking in trickle charge 0 = disable 1 = enable *Protected by security key. Reset by state machine.*	
	7	CHG_RECOVER_T	0	Time constant adjust for charger choke recovery (step-up): 0 = Step-up time constant is 180us (allows faster recovery between processor wakeups) 1 = Step-up time constant is >20ms (outside audio band) *Protected by security key. Reset by state machine.*	
	6	CHG_END_ACT	0	Action to take when charging ends: 0 = Set charge current to 0 1 = Do nothing (leave charger on till timeout) *Protected by security key. Reset by state machine.*	
	5	CHG_FAST	0	Enable fast charging. 0 = Fast charging cannot take place. 1 = Enable fast charging (will not start until valid charging conditions are met). Note: This register is held low and can only be written to once the fast charge ready signal has gone high. *Protected by security key. Reset by state machine. Default held in metal mask.*	
	4	CHG_FAST_USB_THROTTLE	0	Enable USB current throttling in fast charge: 0 = Don't do any current throttling when fast charging. 1 = Do current throttle while fast charging.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Protected by security key. Reset by state machine.	
	3	CHG_NTC_MON	1	Enable charger battery NTC detection (some batteries may not need this - turn off with caution) 0 = Charger ignores NO_NTC detection. 1 = Charger monitors NO_NTC detection. *Default held in metal mask.*	
	2	CHG_BATT_HOT_MON	1	Enable charger battery temperature high detection (some batteries may not need this - turn off with caution) 0 = Charger ignores battery temperature too high. 1 = Charger monitors battery temperature too high. *Default held in metal mask.*	
	1	CHG_BATT_COLD_MON	1	Enable charger battery temperature low detection (some batteries may not need this - turn off with caution) 0 = Charger ignores battery temperature low. 1 = Charger monitors battery temperature low. *Default held in metal mask.*	
	0	CHG_CHIP_TEMP_MON	1	Enable charger chip temperature detection (some batteries may not need this - turn off with caution) 0 = Charger ignores chip temperature 1 = Charger monitors chip temperature *Protected by security key. Default held in metal mask.*	

Register A8h Battery Charger Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R169 (A9h) Battery Charger Control 2	15	CHG_ACTIVE	0	Charger Status. 0 = Battery Charging is inactive 1 = Battery Charging is active (Note CHG_ENA is just a request; the WM8351 determines if the conditions are satisfied for Battery Charging). *Default held in metal mask.*	
	14	CHG_PAUSE	0	0 = Don't pause the charger 1 = Pause charging *Reset by state machine.*	
	13:12	CHG_STS[1:0]	00	00 = Charger off, current set to 0. 01 = In trickle charge mode. 10 = In fast charge mode. 11 = Reserved	
	11:8	CHG_TIME[3:0]	1011	Writing to his field set the charge timeout duration: 0000 = 60min 0001 = 90min 0010 = 120min 0011 = 150min	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0100 = 180min 0101 = 210min 0110 = 240min 0111 = 270min 1000 = 300min 1001 = 330min 1010 = 360min 1011 = 390min 1100 = 420min 1101 = 450min 1110 = 480min 1111 = 510min Reading from this field indicates the charge time remaining: Time remaining = CHG_TIME * 2048s *Protected by security key. Default held in metal mask.*	
	7	CHG_MASK_WALL_FB	0	Selects whether to ignore the WALL_FB signal when charging from LINE. 0 = Does not mask the WALL_FB signal 1 = Mask the WALL_FB signal. Note: Care needs to be taken when using this bit. *Protected by security key. Reset by state machine.*	
	6	CHG_TRICKLE_SEL	0	Selects the trickle charge current. 0 = Set the trickle charge current to 50mA. 1 = Set the trickle charge current to 100mA. *Protected by security key.*	
	5:4	CHG_VSEL[1:0]	00	Battery charge voltage: 00 = 4.05V 01 = 4.1V 10 = 4.15V 11 = 4.2V *Protected by security key.*	
	3:0	CHG_ISEL[3:0]	0110	Fast charge current limit setting. 0000 = off 0001 = 50mA 0010 = 100mA … (50mA steps) 1111 = 750mA Note: Do not set the charger to be more than 400mA when USB powered. *Protected by security key.*	

Register A9h Battery Charger Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R170 (AAh) Battery Charger Control 3	7	CHG_FRC	0	Allows trickle-charging to be forced even if the battery voltage is above the default threshold 0 = only trickle-charge if the battery voltage is below CHG_VSEL-100mV 1 = always trickle-charge *Protected by security key. Reset by state machine.*	
	6:5	CHG_THROTTLE_T[1:0]	00	Time between steps when the charger throttles back due to USB current limit. 00 = 8us 01 = 16us 10 = 32us 11 = 128us *Protected by security key.*	

Register AAh Battery Charger Control 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R172 (ACh) Current Sink Driver A	15	CS1_ENA	0	Current Sink 1 enable (ISINKA pin) 0 = disabled 1 = enabled *Reset by state machine.*	
	12	CS1_HIB_MODE	0	Current Sink 1 behaviour in Hibernate mode 0 = disable current sink in Hibernate 1 = leave current sink as in Active *Reset by state machine.*	
	5:0	CS1_ISEL[5:0]	00_0000	ISINKA current 00_0000 = 4.05uA 00_0001 = 4.85uA 00_0010 = 5.64uA 00_0011 = 6.83uA 00_0100 = 8.02uA 00_0101 = 9.6uA 00_0110 = 11.2uA 00_0111 = 13.5uA 00_1000 = 16.1uA 00_1001 = 19.3uA 00_1010 = 22.4uA 00_1011 = 27.2uA 00_1100 = 32uA 00_1101 = 38.3uA 00_1110 = 44.7uA 00_1111 = 54.1uA 01_0000 = 64.1uA 01_0001 = 76.8uA 01_0010 = 89.5uA 01_0011 = 109uA 01_0100 = 128uA 01_0101 = 153uA 01_0110 = 178uA 01_0111 = 216uA 01_1000 = 256uA	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				01_1001 = 307uA 01_1010 = 358uA 01_1011 = 434uA 01_1100 = 510uA 01_1101 = 612uA 01_1110 = 713uA 01_1111 = 865uA 10_0000 = 1.02mA 10_0001 = 1.22mA 10_0010 = 1.42mA 10_0011 = 1.73mA 10_0100 = 2.03mA 10_0101 = 2.43mA 10_0110 = 2.83mA 10_0111 = 3.43mA 10_1000 = 4.08mA 10_1001 = 4.89mA 10_1010 = 5.7mA 10_1011 = 6.91mA 10_1100 = 8.13mA 10_1101 = 9.74mA 10_1110 = 11.3mA 10_1111 = 13.7mA 11_0000 = 16.3mA 11_0001 = 19.6mA 11_0010 = 22.8mA 11_0011 = 27.6mA 11_0100 = 32.5mA 11_0101 = 39mA 11_0110 = 45.4mA 11_0111 = 54.9mA 11_1000 = 65.3mA 11_1001 = 78.2mA 11_1010 = 91.2mA 11_1011 = 111mA 11_1100 = 130mA 11_1101 = 156mA 11_1110 = 181mA 11_1111 = 220mA *Reset by state machine.*	

Register ACh Current Sink Driver A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R173 (ADh) CSA Flash control	15	CS1_FLASH_MODE	0	Determines the function of the current sink 0 = LED mode 1 = Flash mode *Reset by state machine.*	
	14	CS1_TRIGSRC	0	Selects the trigger for the flash 0 = Flash is triggered by CS1_DRIVE bit 1 = Flash is triggered from GPIO pin configured as FLASH This bit has no effect when CS1_FLASH_MODE=0 *Reset by state machine.*	
	13	CS1_DRIVE	0	Enables the current sink ISINKA LED mode- 0 = disable LED 1 = enabled LED FLASH mode- Register bit used to trigger the flash, if CS1_TRIGSRC is set to 0. Flash is started when the bit goes high, it is then reset at the end of the flash duration. Duration is determined by CS1_FLASH_DUR. This bit has no effect if CS1_TRIGSRC is set to 1. *Reset by state machine. Default held in metal mask.*	
	12	CS1_FLASH_RATE	0	Determines the Flash rate 0 = Normal Operation. Once per trigger (Either register bit or GPIO) 1 = Flash will be internally triggered every 4 seconds *Reset by state machine.*	
	9:8	CS1_FLASH_DUR[1:0]	00	Sets duration of flash 00 = 32ms 01 = 64ms 10 = 96ms 11 = 1024ms *Reset by state machine.*	
	5:4	CS1_OFF_RAMP[1:0]	00	Switch-off ramp duration LED mode- 00 = instant (no ramp) 01 = 0.25s 10 = 0.5s 11 = 1s Flash mode- 00 = instant (no ramp) 01 = 1.95ms 10 = 3.91ms 11 = 7.8ms *Reset by state machine.*	
	1:0	CS1_ON_RAMP[1:0]	00	Switch-on ramp duration	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				LED mode- 00 = instant (no ramp) 01 = 0.25s 10 = 0.5s 11 = 1s Flash mode- 00 = instant (no ramp) 01 = 1.95ms 10 = 3.91ms 11 = 7.8ms *Reset by state machine.*	

Register ADh CSA Flash control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R176 (B0h) DCDC/LDO requested	15	LS_ENA	0	Limit Switch enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	11	LDO4_ENA	0	LDO4 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	10	LDO3_ENA	0	LDO3 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	9	LDO2_ENA	0	LDO2 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	8	LDO1_ENA	0	LDO1 enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	3	DC4_ENA	0	DCDC4 converter enable 0 = disabled 1 = enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	2	DC3_ENA	0	DCDC3 converter enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	1	DC2_ENA	0	DCDC2 converter enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	
	0	DC1_ENA	0	DCDC1 converter enable 0 = disabled 1 = enabled Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. *Reset by state machine. Default held in metal mask.*	

Register B0h DCDC/LDO requested

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R177 (B1h) DCDC Active options	15	DCDC_DISCLKS	0	DCDC clock enable 0 = DCDC Clocks enabled 1 = DCDC1, 3 and 4 clocks disabled. Note: This feature is useful in reducing the current consumption if all 3 Step-Down DC-DCs are in LDO mode. The requirement is to put them in LDO mode and then at least 100us is required before clocks are disabled. Again while coming out of LDO mode first enable the clocks and then at least 100us wait and then come out of LDO mode. This can only be used if the processor is alive to set and unset this bit. *Reset by state machine.*	
	13:12	PUTO[1:0]	00	Power up time out value for all converters 00 = 0.5ms 01 = 2ms 10 = 32ms 11 = 256ms *Reset by state machine.*	
	3	DC4_ACTIVE	1	DC-DC 4 Active mode 0 = Select Standby mode 1 = Select Active mode *Reset by state machine.*	
	2	DC3_ACTIVE	1	DC-DC 3 Active mode 0 = Select Standby mode 1 = Select Active mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Reset by state machine.	
	0	DC1_ACTIVE	1	DC-DC 1 Active mode 0 = Select Standby mode 1 = Select Active mode *Reset by state machine.*	

Register B1h DCDC Active options

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R178 (B2h) DCDC Sleep options	3	DC4_SLEEP	0	DC-DC 4 Sleep mode 0 = Normal DC-DC operation 1 = Select LDO mode *Reset by state machine.*	
	2	DC3_SLEEP	0	DC-DC 3 Sleep mode 0 = Normal DC-DC operation 1 = Select LDO mode *Reset by state machine.*	
	0	DC1_SLEEP	0	DC-DC 1 Sleep mode 0 = Normal DC-DC operation 1 = Select LDO mode *Reset by state machine.*	

Register B2h DCDC Sleep options

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R179 (B3h) Power-check comparator	14	PCCMP_ERRACT	0	Action when supply falls below PCCMP_OFF_THR level 0 = Generate critical supply interrupt only 1 = Generate interrupt and trigger hard shut down *Reset by state machine.*	
	12	PCCOMP_HIB_MODE	0	Function of Hyst Comp in the hibernate state 0 = Hyst Comp is not used in hibernate state 1 = Hyst comp is on in the hibernate state	
	6:4	PCCMP_OFF_THR[2:0]	010	Power check comparator critical battery ("system turn off") threshold value 000 = 2.9V 001 = 3.0V … 111 = 3.6V *Protected by security key. Default held in metal mask.*	
	2:0	PCCMP_ON_THR[2:0]	101	Power check comparator ("system turn on") threshold value 000 = 2.9V 001 = 3.0V … 111 = 3.6V *Protected by security key. Default held in metal mask.*	

Register B3h Power-check comparator

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R180 (B4h) DCDC1 Control	15:14	DC1_CAP[1:0]	00	DC-DC1 Output Capacitor 00 = 10uF, 30uF, 45uF 01 = 60uF, 85uF 10 = Not used 11 = 100uF *Reset by state machine.*	
	11	DC1_DISOVP	0	Over voltage Protection 0 = enabled 1 = disabled *Reset by state machine. Default held in metal mask.*	
	10	DC1_OPFLT	0	Enable discharge of DC-DC1 outputs when DC-DC1 is disabled 0 = Enabled - Output to be discharged 1 = Disabled - Output is left floating	
	6:0	DC1_VSEL[6:0]	000_1110 000_1110 001_1010 000_1110	DC-DC1 Converter output voltage settings in 25mV steps. Maximum output = 3.4V. 110 0110 = 3.4V 110 0010 = 3.3V 101 0110 = 3.0V 100 1110 = 2.8V …… 010 0110 = 1.8V 000 1110 = 1.2V 000 0110 = 1.0V 000 0000 = 0.85V *Reset by state machine. Default held in metal mask.*	

Register B4h DCDC1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R181 (B5h) DCDC1 Timeouts	15:14	DC1_ERRACT[1:0]	00	Action to take on DC-DC1 fault (as well as generating an interrupt): 00 = ignore 01 = shut down converter 10 = shut down system 11 = reserved (shut down system) *Reset by state machine. Default held in metal mask.*	
	13:10	DC1_ENSLOT[3:0]	0000 0011 0010 0001	Time slot for DC-DC1 start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start-up on entering ACTIVE *Reset by state machine. Default held in metal mask.*	
	9:6	DC1_SDSLOT[3:0]	0000	Time slot for DC-DC1 shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF	

Register B5h DCDC1 Timeouts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R182 (B6h) DCDC1 Low Power	14:12	DC1_HIB_MODE[2:0]	001	DC-DC1 Hibernate behaviour: 000 = Use current settings (no change) 001 = Select voltage image settings 010 = Force standby mode 011 = Force standby mode and voltage image settings. 100 = Force LDO mode 101 = Force LDO mode and voltage image settings. 110 = Reserved. 111 = Disable output	
	9:8	DC1_HIB_TRIG[1:0]	00	DC-DC1 Hibernate signal select 00 = HIBERNATE register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3 Note that Hibernate is also selected when a GPIO Hibernate input is asserted. *Reset by state machine. Default held in metal mask.*	
	6:0	DC1_VIMG[6:0]	000_0110	DC-DC1 Converter output image voltage settings in 25mv steps. Maximum output = 3.4V. 110 0110 = 3.4V 110 0010 = 3.3V 101 0110 = 3.0V 100 1110 = 2.8V …… 010 0110 = 1.8V 000 1110 = 1.2V 000 0110 = 1.0V 000 0000 = 0.85V	

Register B6h DCDC1 Low Power

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R183 (B7h) DCDC2 Control	14	DC2_MODE	0	DC-DC2 Converter Mode 0 = Boost mode 1 = Switch mode *Reset by state machine.*	
	12	DC2_HIB_MODE	0	DC-DC2 Hibernate behaviour: 0 = Continue as in Active state 1 = Disable converter output *Reset by state machine.*	
	9:8	DC2_HIB_TRIG[1:0]	00	DC-DC2 Hibernate signal select 00 = HIBERNATE register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3 Note that Hibernate is also selected when a GPIO Hibernate input is asserted. *Reset by state machine.*	
	6	DC2_ILIM	0	DC-DC2 peak current limit select 0 = Higher peak current 1 = Lower peak current *Reset by state machine. Default held in metal mask.*	
	4	DC2_RMPH	1	DC-DC2 compensation ramp {DC2_RMPH, DC2_RMPL} 00 = 20V < VOUT ≤ 30V 01 = 10V < VOUT ≤ 20V 10 = 5V < VOUT ≤ 10V 11 = VOUT ≤ 5V (will be chosen automatically if DC2_FBSRC=11) *Reset by state machine. Default held in metal mask.*	
	3	DC2_RMPL	1	DC-DC2 compensation ramp {DC2_RMPH, DC2_RMPL} 00 = 20V < VOUT ≤ 30V 01 = 10V < VOUT ≤ 20V 10 = 5V < VOUT ≤ 10V 11 = VOUT ≤ 5V (will be chosen automatically if DC2_FBSRC=11) *Reset by state machine. Default held in metal mask.*	
	1:0	DC2_FBSRC[1:0]	00	DC-DC2 voltage feedback selection 00 = voltage feedback (using external resistor divider on pin FB2) 01 = current sink ISINKA used as feedback 10 = Reserved 11 = voltage feedback (using internal resistor divider on pin USB) *Reset by state machine. Default held in metal mask.*	

Register B7h DCDC2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R184 (B8h) DCDC2 Timeouts	15:14	DC2_ERRACT[1:0]	00	Action to take on DC-DC2 fault (as well as generating an interrupt): 00 = ignore 01 = shut down converter 10 = shut down system 11 = reserved (shut down system) *Reset by state machine. Default held in metal mask.*	
	13:10	DC2_ENSLOT[3:0]	0000	Time slot for DC-DC2 start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start-up on entering ACTIVE *Reset by state machine. Default held in metal mask.*	
	9:6	DC2_SDSLOT[3:0]	0000	Time slot for DC-DC2 shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF	

Register B8h DCDC2 Timeouts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R186 (BAh) DCDC3 Control	11	DC3_DISOVP	0	Over voltage Protection 0 = enabled 1 = disabled *Reset by state machine. Default held in metal mask.*	
	10	DC3_OPFLT	0	Enable discharge of DC-DC3 outputs when DC-DC3 is disabled 0 = Enabled - Output to be discharged 1 = Disabled - Output is left floating	
	6:0	DC3_VSEL[6:0]	000_0000 010_0110 101_0110 010_0110	DC-DC3 Converter output voltage settings in 25mV steps. Maximum output = 3.4V. 110 0110 = 3.4V 110 0010 = 3.3V 101 0110 = 3.0V 100 1110 = 2.8V …… 010 0110 = 1.8V 000 1110 = 1.2V 000 0110 = 1.0V 000 0000 = 0.85V *Reset by state machine. Default held in metal mask.*	

Register BAh DCDC3 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R187 (BBh) DCDC3 Timeouts	15:14	DC3_ERRACT[1:0]	00	Action to take on DC-DC3 fault (as well as generating an interrupt): 00 = ignore 01 = shut down converter 10 = shut down system 11 = reserved (shut down system) *Reset by state machine. Default held in metal mask.*	
	13:10	DC3_ENSLOT[3:0]	0000 0001 0001 0010	Time slot for DC-DC3 start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start-up on entering ACTIVE *Reset by state machine. Default held in metal mask.*	
	9:6	DC3_SDSLOT[3:0]	0000	Time slot for DC-DC3 shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF	

Register BBh DCDC3 Timeouts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R188 (BCh) DCDC3 Low Power	14:12	DC3_HIB_MODE[2:0]	000	DC-DC3 Hibernate behaviour: 000 = Use current settings (no change) 001 = Select voltage image settings 010 = Force standby mode 011 = Force standby mode and voltage image settings. 100 = Force LDO mode 101 = Force LDO mode and voltage image settings. 110 = Reserved. 111 = Disable output *Reset by state machine. Default held in metal mask.*	
	9:8	DC3_HIB_TRIG[1:0]	00	DC-DC3 Hibernate signal select 00 = HIBERNATE register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3 Note that Hibernate is also selected when a GPIO Hibernate input is asserted. *Reset by state machine. Default held in metal mask.*	
	6:0	DC3_VIMG[6:0]	000_0110	DC-DC3 Converter output image voltage settings in 25mv steps. Maximum output = 3.4V.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				110 0110 = 3.4V 110 0010 = 3.3V 101 0110 = 3.0V 100 1110 = 2.8V …… 010 0110 = 1.8V 000 1110 = 1.2V 000 0110 = 1.0V 000 0000 = 0.85V	

Register BCh DCDC3 Low Power

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R189 (BDh) DCDC4 Control	11	DC4_DISOVP	0	Over voltage Protection 0 = enabled 1 = disabled *Reset by state machine. Default held in metal mask.*	
	10	DC4_OPFLT	0	Enable discharge of DC-DC4 outputs when DC-DC4 is disabled 0 = Enabled - Output to be discharged 1 = Disabled - Output is left floating	
	6:0	DC4_VSEL[6:0]	000_0000 110_0010 010_0110 110_0010	DC-DC4 Converter output voltage settings in 25mV steps. Maximum output = 3.4V. 110 0110 = 3.4V 110 0010 = 3.3V 101 0110 = 3.0V 100 1110 = 2.8V …… 010 0110 = 1.8V 000 1110 = 1.2V 000 0110 = 1.0V 000 0000 = 0.85V *Reset by state machine. Default held in metal mask.*	

Register BDh DCDC4 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R190 (BEh) DCDC4 Timeouts	15:14	DC4_ERRACT[1:0]	00	Action to take on DC-DC4 fault (as well as generating an interrupt): 00 = ignore 01 = shut down converter 10 = shut down system 11 = reserved (shut down system) *Reset by state machine. Default held in metal mask.*	
	13:10	DC4_ENSLOT[3:0]	0000 0010 0011 0101	Time slot for DC-DC4 start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start-up on entering ACTIVE *Reset by state machine. Default held in metal mask.*	
	9:6	DC4_SDSLOT[3:0]	0000	Time slot for DC-DC4 shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF	

Register BEh DCDC4 Timeouts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R191 (BFh) DCDC4 Low Power	14:12	DC4_HIB_MODE[2:0]	000	DC-DC4 Hibernate behaviour: 000 = Use current settings (no change) 001 = Select voltage image settings 010 = Force standby mode 011 = Force standby mode and voltage image settings. 100 = Force LDO mode 101 = Force LDO mode and voltage image settings. 110 = Reserved. 111 = Disable output *Reset by state machine. Default held in metal mask.*	
	9:8	DC4_HIB_TRIG[1:0]	00	DC-DC4 Hibernate signal select 00 = HIBERNATE register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3 Note that Hibernate is also selected when a GPIO Hibernate input is asserted. *Reset by state machine. Default held in metal mask.*	
	6:0	DC4_VIMG[6:0]	000_0110	DC-DC4 Converter output image voltage settings in 25mv steps. Maximum output = 3.4V.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				110 0110 = 3.4V 110 0010 = 3.3V 101 0110 = 3.0V 100 1110 = 2.8V …… 010 0110 = 1.8V 000 1110 = 1.2V 000 0110 = 1.0V 000 0000 = 0.85V	

Register BFh DCDC4 Low Power

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R199 (C7h) Limit Switch Control	15:14	LS_ERRACT[1:0]	00	Current limit detection behaviour 00 = ignore 01 = disable switch 10 = shut down system 11 = shut down system *Reset by state machine. Default held in metal mask.*	
	13:10	LS_ENSLOT[3:0]	0000	Time slot for Limit Switch start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start-up on entering ACTIVE *Reset by state machine. Default held in metal mask.*	
	9:6	LS_SDSLOT[3:0]	0000	Time slot for Limit Switch shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF	
	4	LS_HIB_MODE	0	Limit switch hibernate mode setting 0 = disabled 1 = leave setting as in Active mode	
	1	LS_HIB_PROT	1	Controls the bulk detection circuit when Limit Switch is disabled in Hibernate mode. 0 = bulk detection disabled 1 = bulk detection enabled	
	0	LS_PROT	1	Controls the bulk detection circuit when Limit Switch is disabled in Active mode. 0 = bulk detection disabled 1 = bulk detection enabled	

Register C7h Limit Switch Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R200 (C8h) LDO1 Control	14	LDO1_SWI	0	LDO1 Regulator mode 0 = LDO voltage regulator 1 = Current-limited switch (no voltage regulation, LDO1_VSEL has no effect) *Reset by state machine. Default held in metal mask.*	
	10	LDO1_OPFLT	0	Enable discharge of LDO1 outputs when LDO1 is disabled 0 = Enabled - Output to be discharged 1 = Disabled - Output is left floating Note - if LDO Regulators 1, 2, 3 and 4 are all disabled, then the outputs will all be discharged, regardless of the LDO*n*_OPFLT bit.	
	4:0	LDO1_VSEL[4:0]	1_1100 0_0110 1_1100 0_0110	LDO1 Regulator output voltage (when LDO1_SWI=0) 1 1111 = 3.3V … (100mV steps) 1 0000 = 1.8V 0 1111 = 1.65V … (50mV steps) 0 0000 = 0.9V *Reset by state machine. Default held in metal mask.*	

Register C8h LDO1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R201 (C9h) LDO1 Timeouts	15:14	LDO1_ERRACT[1:0]	00	Action to take on LDO1 fault (as well as generating an interrupt): 00 = ignore 01 = shut down regulator 10 = shut down system 11 = reserved (shut down system) *Reset by state machine. Default held in metal mask.*	
	13:10	LDO1_ENSLOT[3:0]	0000 0000 0001 0011	Time slot for LDO1 start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start up on entering ACTIVE *Reset by state machine. Default held in metal mask.*	
	9:6	LDO1_SDSLOT[3:0]	0000	Time slot for LDO1 shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF	

Register C9h LDO1 Timeouts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R202 (CAh) LDO1 Low Power	13:12	LDO1_HIB_MODE[1:0]	00	LDO1 Hibernate behaviour: 00 = Select voltage image settings 01 = disable output 10 = reserved 11 = reserved *Reset by state machine. Default held in metal mask.*	
	9:8	LDO1_HIB_TRIG[1:0]	00	LDO1 Hibernate signal select 00 = Hibernate register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3 *Reset by state machine. Default held in metal mask.*	
	4:0	LDO1_VIMG[4:0]	1_1100	LDO1 Regulator output image voltage 1 1111 = 3.3V … (100mV steps) 1 0000 = 1.8V 0 1111 = 1.65V … (50mV steps) 0 0000 = 0.9V	

Register CAh LDO1 Low Power

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R203 (CBh) LDO2 Control	14	LDO2_SWI	0	LDO2 Regulator mode 0 = LDO voltage regulator 1 = Current-limited switch (no voltage regulation, LDO2_VSEL has no effect) *Reset by state machine. Default held in metal mask.*	
	10	LDO2_OPFLT	0	Enable discharge of LDO2 outputs when LDO2 is disabled 0 = Enabled - Output to be discharged 1 = Disabled - Output is left floating Note - if LDO Regulators 1, 2, 3 and 4 are all disabled, then the outputs will all be discharged, regardless of the LDO*n*_OPFLT bit.	
	4:0	LDO2_VSEL[4:0]	1_1011 1_0000 1_0000 1_0110	LDO2 Regulator output voltage (when LDO2_SWI=0) 1 1111 = 3.3V … (100mV steps) 1 0000 = 1.8V 0 1111 = 1.65V … (50mV steps) 0 0000 = 0.9V *Reset by state machine. Default held in metal mask.*	

Register CBh LDO2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R204 (CCh) LDO2 Timeouts	15:14	LDO2_ERRACT[1:0]	00	Action to take on LDO2 fault (as well as generating an interrupt): 00 = ignore 01 = shut down regulator 10 = shut down system 11 = reserved (shut down system) *Reset by state machine. Default held in metal mask.*	
	13:10	LDO2_ENSLOT[3:0]	0000 0011 0011 0000	Time slot for LDO2 start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start up on entering ACTIVE *Reset by state machine. Default held in metal mask.*	
	9:6	LDO2_SDSLOT[3:0]	0000	Time slot for LDO2 shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF	

Register CCh LDO2 Timeouts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R205 (CDh) LDO2 Low Power	13:12	LDO2_HIB_MODE[1:0]	00	LDO2 Hibernate behaviour: 00 = Select voltage image settings 01 = disable output 10 = reserved 11 = reserved *Reset by state machine. Default held in metal mask.*	
	9:8	LDO2_HIB_TRIG[1:0]	00	LDO2 Hibernate signal select 00 = Hibernate register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3 *Reset by state machine. Default held in metal mask.*	
	4:0	LDO2_VIMG[4:0]	1_1100	LDO2 Regulator output image voltage 1 1111 = 3.3V … (100mV steps) 1 0000 = 1.8V 0 1111 = 1.65V … (50mV steps) 0 0000 = 0.9V	

Register CDh LDO2 Low Power

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R206 (CEh) LDO3 Control	14	LDO3_SWI	0	LDO3 Regulator mode 0 = LDO voltage regulator 1 = Current-limited switch (no voltage regulation, LDO3_VSEL has no effect) *Reset by state machine. Default held in metal mask.*	
	10	LDO3_OPFLT	0	Enable discharge of LDO3 outputs when LDO3 is disabled 0 = Enabled - Output to be discharged 1 = Disabled - Output is left floating Note - if LDO Regulators 1, 2, 3 and 4 are all disabled, then the outputs will all be discharged, regardless of the LDO*n*_OPFLT bit.	
	4:0	LDO3_VSEL[4:0]	1_1011 1_1111 1_0101 1_1001	LDO3 Regulator output voltage (when LDO3_SWI=0) 1 1111 = 3.3V … (100mV steps) 1 0000 = 1.8V 0 1111 = 1.65V … (50mV steps) 0 0000 = 0.9V *Reset by state machine. Default held in metal mask.*	

Register CEh LDO3 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R207 (CFh) LDO3 Timeouts	15:14	LDO3_ERRACT[1:0]	00	Action to take on LDO3 fault (as well as generating an interrupt): 00 = ignore 01 = shut down regulator 10 = shut down system 11 = reserved (shut down system) *Reset by state machine. Default held in metal mask.*	
	13:10	LDO3_ENSLOT[3:0]	0000 0010 0000 0000	Time slot for LDO3 start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start up on entering ACTIVE *Reset by state machine. Default held in metal mask.*	
	9:6	LDO3_SDSLOT[3:0]	0000	Time slot for LDO3 shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF	

Register CFh LDO3 Timeouts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R208 (D0h) LDO3 Low Power	13:12	LDO3_HIB_MODE[1:0]	00	LDO3 Hibernate behaviour: 00 = Select voltage image settings 01 = disable output 10 = reserved 11 = reserved *Reset by state machine. Default held in metal mask.*	
	9:8	LDO3_HIB_TRIG[1:0]	00	LDO3 Hibernate signal select 00 = Hibernate register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3 *Reset by state machine. Default held in metal mask.*	
	4:0	LDO3_VIMG[4:0]	1_1100	LDO3 Regulator output image voltage 1 1111 = 3.3V … (100mV steps) 1 0000 = 1.8V 0 1111 = 1.65V … (50mV steps) 0 0000 = 0.9V	

Register D0h LDO3 Low Power

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R209 (D1h) LDO4 Control	14	LDO4_SWI	0	LDO4 Regulator mode 0 = LDO voltage regulator 1 = Current-limited switch (no voltage regulation, LDO4_VSEL has no effect) *Reset by state machine. Default held in metal mask.*	
	10	LDO4_OPFLT	0	Enable discharge of LDO4 outputs when LDO4 is disabled 0 = Enabled - Output to be discharged 1 = Disabled - Output is left floating Note - if LDO Regulators 1, 2, 3 and 4 are all disabled, then the outputs will all be discharged, regardless of the LDO*n*_OPFLT bit.	
	4:0	LDO4_VSEL[4:0]	1_1011 0_1010 1_1010 1_1010	LDO4 Regulator output voltage (when LDO4_SWI=0) 1 1111 = 3.3V … (100mV steps) 1 0000 = 1.8V 0 1111 = 1.65V … (50mV steps) 0 0000 = 0.9V *Reset by state machine. Default held in metal mask.*	

Register D1h LDO4 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R210 (D2h) LDO4 Timeouts	15:14	LDO4_ERRACT[1:0]	00	Action to take on LDO4 fault (as well as generating an interrupt): 00 = ignore 01 = shut down regulator 10 = shut down system 11 = reserved (shut down system) *Reset by state machine. Default held in metal mask.*	
	13:10	LDO4_ENSLOT[3:0]	0000 0010 0000 0100	Time slot for LDO4 start-up 0000 = Disabled (do not start up) 0001 = Start-up in time slot 1 … (total 14 slots available) 1110 = Start-up in time slot 14 1111 = Start up on entering ACTIVE *Reset by state machine. Default held in metal mask.*	
	9:6	LDO4_SDSLOT[3:0]	0000	Time slot for LDO4 shutdown. 0000 = Shut down on entering OFF 0001 = Shutdown in time slot 1 …. (total 14 slots available) 1110 = Shutdown in time slot 14 1111 = Shut down on entering OFF	

Register D2h LDO4 Timeouts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R211 (D3h) LDO4 Low Power	13:12	LDO4_HIB_MODE[1:0]	00	LDO4 Hibernate behaviour: 00 = Select voltage image settings 01 = disable output 10 = reserved 11 = reserved *Reset by state machine. Default held in metal mask.*	
	9:8	LDO4_HIB_TRIG[1:0]	00	LDO4 Hibernate signal select 00 = Hibernate register bit 01 = L_PWR1 10 = L_PWR2 11 = L_PWR3 *Reset by state machine. Default held in metal mask.*	
	4:0	LDO4_VIMG[4:0]	1_1100	LDO4 Regulator output image voltage 1 1111 = 3.3V … (100mV steps) 1 0000 = 1.8V 0 1111 = 1.65V … (50mV steps) 0 0000 = 0.9V	

Register D3h LDO4 Low Power

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R215 (D7h) VCC_FAULT Masks	15	LS_FAULT	0	Limit Switch fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault *Reset by state machine.*	
	11	LDO4_FAULT	0	LDO4 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault *Reset by state machine.*	
	10	LDO3_FAULT	0	LDO3 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault *Reset by state machine.*	
	9	LDO2_FAULT	0	LDO2 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault *Reset by state machine.*	
	8	LDO1_FAULT	0	LDO1 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault *Reset by state machine.*	
	3	DC4_FAULT	0	DCDC4 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault *Reset by state machine.*	
	2	DC3_FAULT	0	DCDC3 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault *Reset by state machine.*	
	1	DC2_FAULT	0	DCDC2 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault *Reset by state machine.*	
	0	DC1_FAULT	0	DCDC1 fault mask for the /VCC_FAULT 0 = don't mask converter fault 1 = mask converter fault *Reset by state machine.*	

Register D7h VCC_FAULT Masks

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R216 (D8h) Main Bandgap Control	15	MBG_LOAD_FUSES	0	Enables the current to the bandgap trim fuses. This must be set to 1 when writing the fuses. To read the trim value held in the fuse, this bit must be set and then reset.	

Register D8h Main Bandgap Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R217 (D9h) OSC Control	15	OSC_LOAD_FUSES	0	Enables the current to the bandgap trim fuses. This must be set to 1 when writing the fuses. To read the trim value, this bit must be set and then reset. *Protected by security key.*	

Register D9h OSC Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R218 (DAh) RTC Tick Control	15	RTC_TICK_ENA	1	Enable RTC counting (instruction only) 0 = disabled 1 = enabled *Protected by security key. Reset by state machine. Default held in metal mask.*	
	14	RTC_TICKSTS	0	Status of tick request. This bit can be used to ensure the RTC is using the value of RTC_TICK_ENA. 0 = disabled 1 = enabled *Protected by security key.*	
	13	RTC_CLKSRC	0	RTC 32Khz clock source. 0 = take 32Khz from 32K OSC 1 = take 32Khz from GPIOx (Alternative GPIO function) *Protected by security key. Reset by state machine. Default held in metal mask.*	
	12	OSC32K_ENA	1	On chip 32Khz OSC enable 0 = disable 1 = enable *Protected by security key. Reset by state machine. Default held in metal mask.*	
	9:0	RTC_TRIM[9:0]	00_0000_0000	RTC frequency trim. Used to adjust the count value of the Tick Gen block to compensate for crystal inaccuracies. RTC frequency trim is a 10bit fixed point <4,6> 2's complement number. MSB Scaling = -8Hz. The register indicates the error (in Hz) with respect to the ideal 32768Hz) of the input crystal frequency. e.g.: Actual crystal freq: 32769.00Hz: Required trim 0xb0001_000000 (+1.000000) Actual crystal freq: 32767.00Hz: Required trim 0xb1111_000000 (-1.000000) Actual crystal freq: 32775.58Hz: Required trim 0xb0111_100101 (+7.578125) Actual crystal freq: 32763.78Hz: Required trim	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0xb1011_110010 (-4.218750) *Protected by security key.*	

Register DAh RTC Tick Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R219 (DBh) Security1	15:0	SECURITY[15:0]	0000_0000_0000_0000	The value 0013h needs to be set in this register to allow write access to the security locked registers. *Reset by state machine.*	

Register DBh Security1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R224 (E0h) Signal overrides	11	WALL_FB_GT_BATT_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	10	USB_FB_GT_BATT_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	9	FLL_OK_OVRDE	0	0 = normal operation 1 = Overrides the FLL_OK	
	8	DEB_TICK_OVRDE	0	Overrides the ticks in the debounce block 0 = normal 1 = All ticks are overwritten with 16KHz ticks	
	7	UVLO_B_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	6	RTC_ALARM_OVRDE	0	Override for RTC_ALARM signal 0 = normal 1 = Alarm = 1	
	3	LINE_GT_BATT_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	2	LINE_GT_VRTC_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	1	USB_GT_LINE_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	0	BATT_GT_USB_OVRDE	0	[No description available]	

Register E0h Signal overrides

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R225 (E1h) DCDC/LDO status	15	LS_STS	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. *Reset by state machine.*	
	11	LDO4_STS	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. *Reset by state machine.*	
	10	LDO3_STS	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. *Reset by state machine.*	
	9	LDO2_STS	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. *Reset by state machine.*	
	8	LDO1_STS	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. *Reset by state machine.*	
	3	DC4_STS	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. *Reset by state machine.*	
	2	DC3_STS	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. *Reset by state machine.*	
	1	DC2_STS	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. *Reset by state machine.*	
	0	DC1_STS	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. *Reset by state machine.*	

Register E1h DCDC/LDO status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R226 (E2h) Charger Overides/status	15	CHG_BATT_HOT_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	14	CHG_BATT_COLD_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	11	CHG_END_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	2	CHG_BATT_LT_3P9_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	1	CHG_BATT_LT_3P1_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	0	CHG_BATT_LT_2P85_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	

Register E2h Charger Overides/status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R227 (E3h) misc overrides	12	CS1_NOT_REG_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	10	USB_LIMIT_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	7	AUX_DCOMP4_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	6	AUX_DCOMP3_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	5	AUX_DCOMP2_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	4	AUX_DCOMP1_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	3	HYST_UVLO_OK_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				bit is set to 1.	
	2	CHIP_GT115_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	1	CHIP_GT140_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	

Register E3h misc overrides

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R228 (E4h) Supply overrides/status 1	3	OVRV_DC4_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_OV_OVRDE bit is set to 1.	
	2	OVRV_DC3_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_OV_OVRDE bit is set to 1.	
	0	OVRV_DC1_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_OV_OVRDE bit is set to 1.	

Register E4h Supply overrides/status 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R229 (E5h) Supply overrides/status 2	15	OVCR_LS_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_OC_OVRDE bit is set to 1.	
	11	UNDV_LDO4_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1.	
	10	UNDV_LDO3_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1.	
	9	UNDV_LDO2_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1.	
	8	UNDV_LDO1_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1.	
	3	UNDV_DC4_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1.	
	2	UNDV_DC3_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				debounce logic when the CONVERTER_UV_OVRDE bit is set to 1.	
	1	UNDV_DC2_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1.	
	0	UNDV_DC1_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1.	

Register E5h Supply overrides/status 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R230 (E6h) GPIO Pin Status	15	1	1	Unused *Never reset.*	
	14	1	1	Unused *Never reset.*	
	13	1	1	Unused *Never reset.*	
	12	GP12_LVL	0	Logic level of GPIO12 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP12_EINT Output- Write sets the value to drive the GPIO pin	
	11	GP11_LVL	0	Logic level of GPIO11 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP11_EINT Output- Write sets the value to drive the GPIO pin	
	10	GP10_LVL	0	Logic level of GPIO10 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP10_EINT Output- Write sets the value to drive the GPIO pin	
	9	GP9_LVL	0	Logic level of GPIO9 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP9_EINT Output- Write sets the value to drive the GPIO pin	
	8	GP8_LVL	0	Logic level of GPIO8 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP8_EINT	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Output- Write sets the value to drive the GPIO pin	
	7	GP7_LVL	0	Logic level of GPIO7 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP7_EINT Output- Write sets the value to drive the GPIO pin	
	6	GP6_LVL	0	Logic level of GPIO6 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP6_EINT Output- Write sets the value to drive the GPIO pin	
	5	GP5_LVL	0	Logic level of GPIO5 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP5_EINT Output- Write sets the value to drive the GPIO pin	
	4	GP4_LVL	0	Logic level of GPIO4 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP4_EINT Output- Write sets the value to drive the GPIO pin	
	3	GP3_LVL	0	Logic level of GPIO3 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP3_EINT Output- Write sets the value to drive the GPIO pin	
	2	GP2_LVL	0	Logic level of GPIO2 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP2_EINT Output- Write sets the value to drive the GPIO pin	
	1	GP1_LVL	0	Logic level of GPIO1 pin Input- Reads the logic level of GPIO pin Writing '0' clears GP1_EINT Output- Write sets the value to drive the GPIO pin	
	0	GP0_LVL	0	Logic level of GPIO0 pin Input-	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Reads the logic level of GPIO pin Writing '0' clears GP0_EINT Output- Write sets the value to drive the GPIO pin	

Register E6h GPIO Pin Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R231 (E7h) comparotor overrides	15	USB_FB_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	14	WALL_FB_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	13	BATT_FB_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	11	CODEC_JCK_DET_L_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	10	CODEC_JCK_DET_R_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	9	CODEC_MICSCD_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	
	8	CODEC_MICD_OVRDE	0	Readback of the raw signal value. Allow direct control of this signal's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.	

Register E7h comparotor overrides

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R233 (E9h) State Machine status	10:8	USB_SM[2:0]	000	Readback tell you what state the USB state machine is in. This is useful for debugging your setup. 0001 = 100mA Slave 0101 = 500mA Slave 0100 = Suspend 0010 = Master Line 0110 = Master DCDC	
	6:4	CHG_SM[2:0]	000	Readback tell you what state the Charger state machine is in. This is useful for debugging your setup. 0000 = OFF 0001 = TRICKLE 0010 = TRICKLE_CHOKE	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0011 = TRICKLE_OVERTEMP 0100 = FAST 0110 = FAST_CHOKE 0101 = FAST_OVERTEMP	
	3:0	MAIN_SM[3:0]	0000	Readback tell you what state the MAIN state machine is in. This is useful for debugging your setup. 0010 = OFF 1101 = PRE-ACTIVE 1100 = HIBERNATE 1111 = ACTIVE	

Register E9h State Machine status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R234 (EAh) FLL Test 1	12	FLL_FRC_TRK_GAIN	1	Force the FLL_TRK_GAIN 0 : Lets FLL_TRK_GAIN control the FLL 1 : Forces FLL_TRK_GAIN to 0 until FLL_LOCK goes high *Protected by security key.*	
	9:8	FLL_BIAS[1:0]	10	FLL bias control *Protected by security key.*	
	7:6	FLL_POLE_SHIFT[1:0]	00	Test register to control analogue poles with FLL loop *Protected by security key.*	

Register EAh FLL Test 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R248 (F8h) DCDC1 Test Controls	4	DC1_FORCE_PWM	0	Force DC-DC1 PWM mode 0 = Normal DC-DC operation 1 = Force DC-DC PWM mode *Reset by state machine.*	

Register F8h DCDC1 Test Controls

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R250 (FAh) DCDC3 Test Controls	4	DC3_FORCE_PWM	0	Force DC-DC3 PWM mode 0 = Normal DC-DC operation 1 = Force DC-DC PWM mode *Reset by state machine.*	

Register FAh DCDC3 Test Controls

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R251 (FBh) DCDC4 Test Controls	4	DC4_FORCE_PWM	0	Force DC-DC4 PWM mode 0 = Normal DC-DC operation 1 = Force DC-DC PWM mode *Reset by state machine.*	

Register FBh DCDC4 Test Controls

28 DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.025dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple			+/- 0.025		dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs		-60		dB
Group Delay			21/fs		
ADC High Pass Filter					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		
DAC Filter					
Passband	+/- 0.035dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple			+/-0.035		dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs		-55		dB
Group Delay			29/fs		

Terminology

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

28.1 DAC FILTER RESPONSES

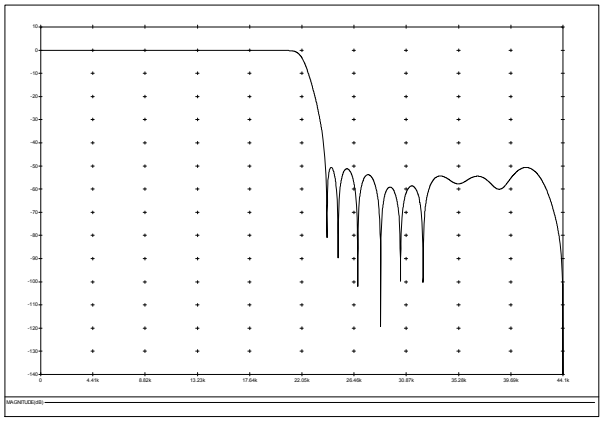


Figure 81 DAC Digital Filter Frequency Response (Normal Mode)

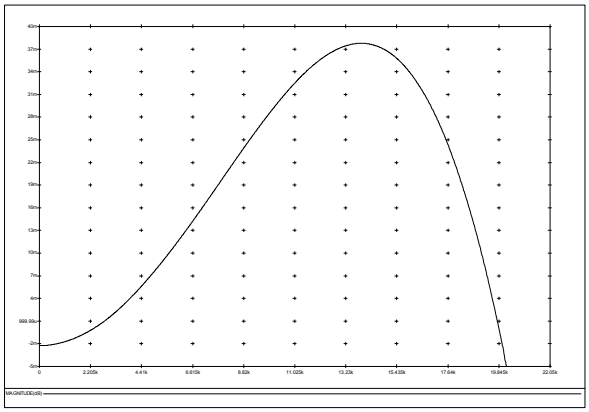


Figure 82 DAC Digital Filter Ripple (Normal Mode)

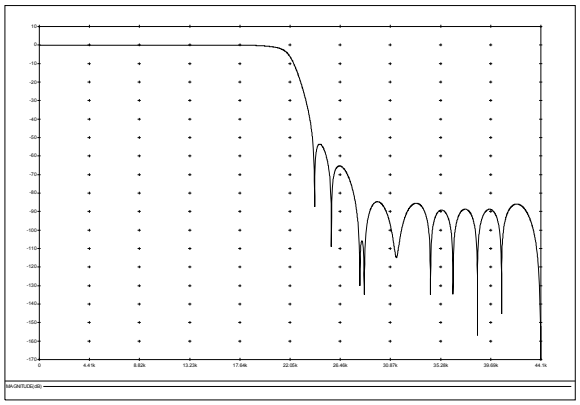


Figure 83 DAC Digital Filter Frequency Response (Sloping Stopband Mode)

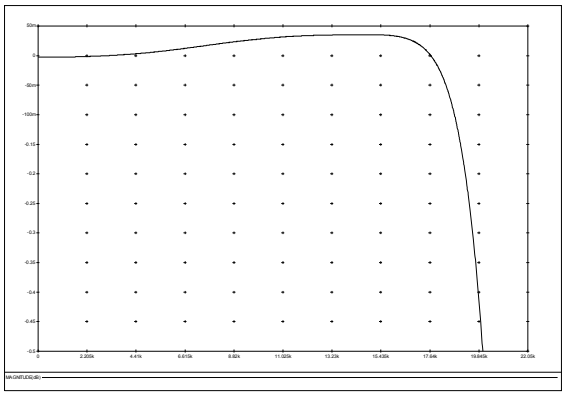


Figure 84 DAC Digital Filter Ripple (Sloping Stopband Mode)

28.2 ADC FILTER RESPONSES

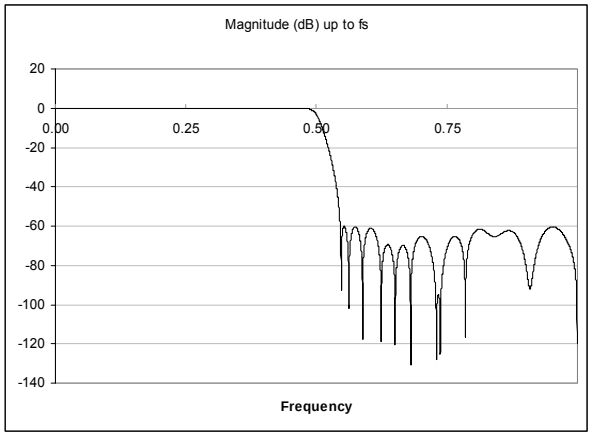


Figure 85 ADC Digital Filter Frequency Response

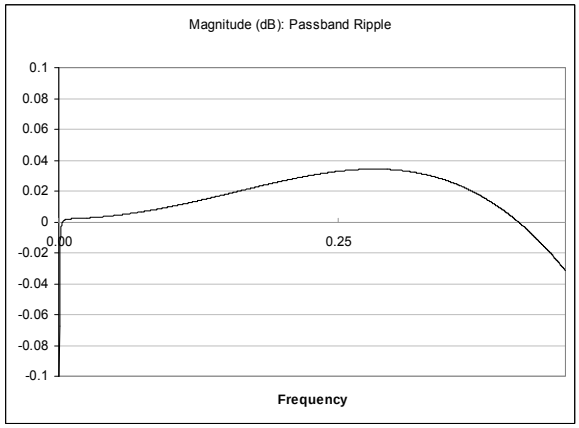


Figure 86 ADC Digital Filter Ripple

29 APPLICATIONS INFORMATION

29.1 TYPICAL CONNECTIONS

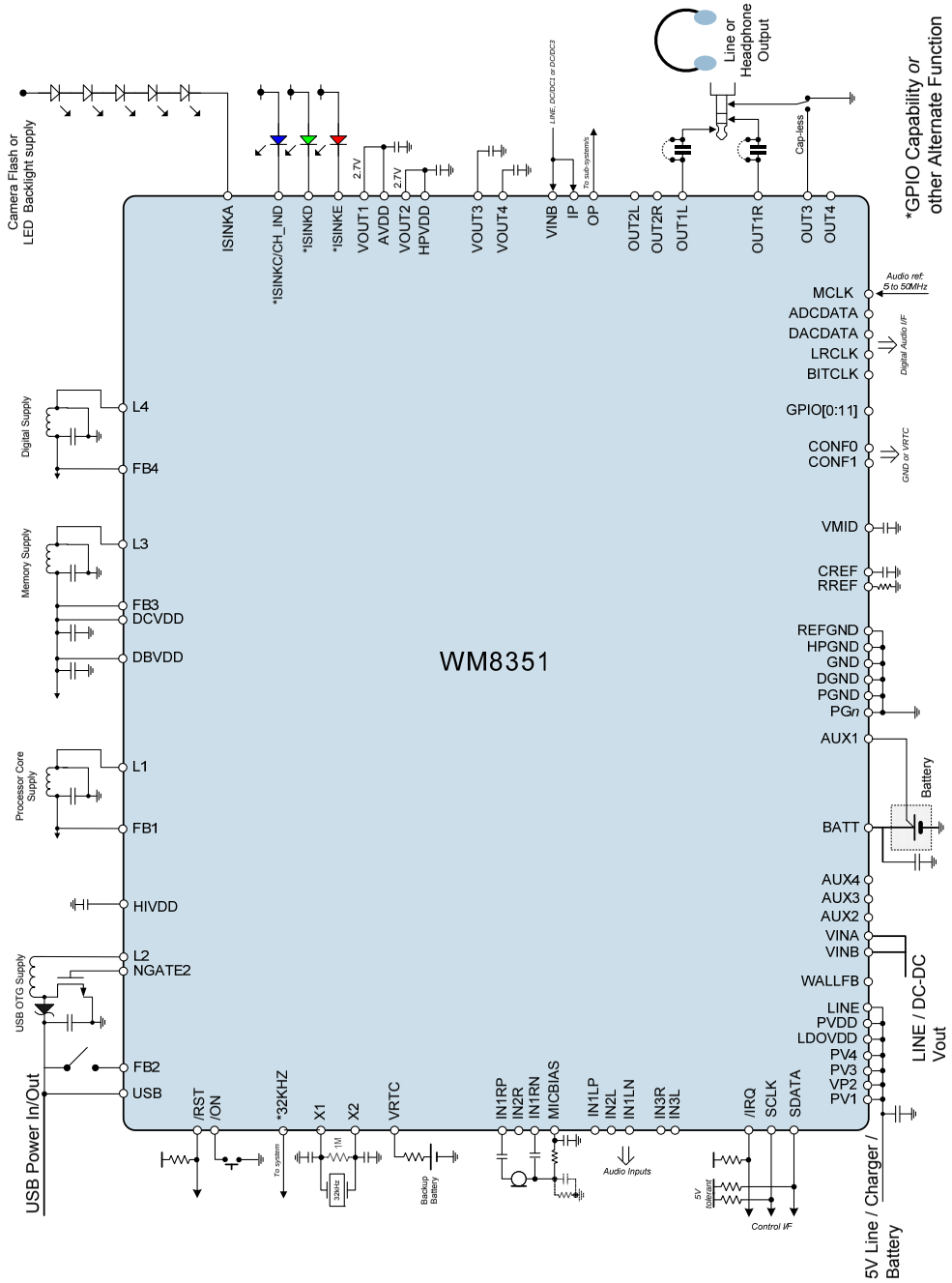


Figure 87 WM8351 Typical Connections Diagram

For detailed schematics, bill of materials and recommended external components refer to the WM8351 evaluation board users manual.

29.2 VOLTAGE REFERENCE (VREF) COMPONENTS

A decoupling capacitor is required between CREF and REFGND; a 2.2uF X5R capacitor is recommended.

A reference resistor is required between RREF and REFGND; a 100kΩ (1%) resistor is recommended.

29.3 DC-DC (STEP-DOWN) CONVERTER EXTERNAL COMPONENTS

The recommended connections to the DC-DC (Step-Down) Converters are illustrated in Figure 88.

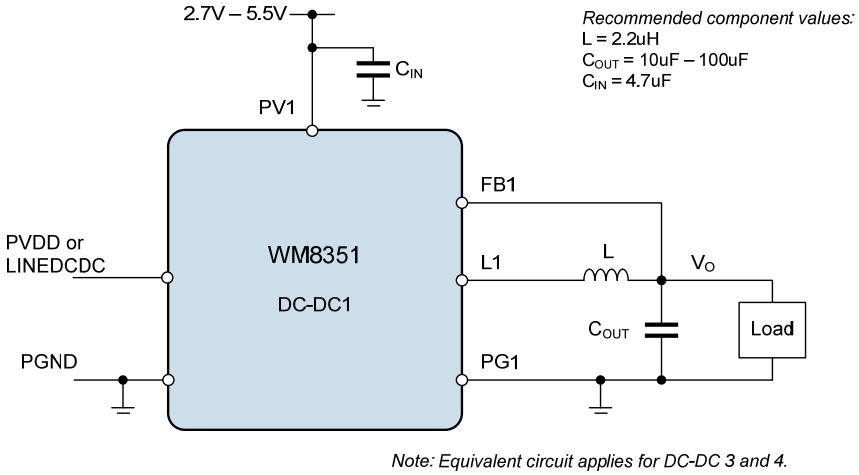


Figure 88 DC-DC (Step-Down) Converters External Components

When selecting suitable capacitors, is it imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. It should be noted that some components' capacitance changes significantly depending on the DC voltage applied. Ceramic X7R or X5R types are recommended.

The choice of output capacitor for DC-DC1 varies depending on the required transient response. A value of 30μF is recommended in the first instance. Larger values (up to 100μF) may be required for optimum performance under large load transient conditions. Smaller values (down to 10μF) may be sufficient for a steady load in some applications.

For layout and size reasons, users may choose to implement large values of output capacitance by connecting two or more capacitors in parallel.

To ensure stable operation, the register field DC1_CAP must be set according to the output capacitance, as detailed in Table 156.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R180 (B4h)	15:14	DC1_CAP	00	DC-DC1 Output Capacitor 00 = 10uF, 30uF, 45uF 01 = 60uF, 85uF 10 = Not used 11 = 100uF

Table 156 Register Control for DC-DC1 Output Capacitor

When selecting a suitable output inductor, the inductance value and the saturation current must be compatible with the operating conditions of the converter.

The magnitude of the inductor current ripple is dependant on the inductor value and can be determined by the following equation:

$$\triangle I_L = \frac{V_{OUT} \cdot (1 - (V_{OUT} / V_{IN}))}{L \cdot F_{SW}}$$

$\triangle I_L$ = Inductor ripple current
V_{OUT} = Output voltage
V_{IN} = Input voltage
L = Inductance
F_{SW} = Switching frequency (2MHz)

As a minimum requirement, the DC current rating should be equal to the maximum load current plus one half of the inductor current ripple:

$$I_{Lpeak} = I_{OUTmax} + (\triangle I_L / 2)$$

I_{Lpeak} = Inductor peak current
I_{OUTmax} = Maximum load current
$\triangle I_L$ = Inductor ripple current

To be suitable for the application, the chosen inductor must have a saturation current that is higher than the peak inductor current given by the above equation. To maximise the converter efficiency, the inductor should also have a low DC Resistance (DCR), resulting in minimum conduction losses. Care should also be taken to ensure that the inductor is effective at the applicable operating temperature.

Wolfson recommends the following external components for use with DC-DC Converter 1. Note that the choice of output capacitor should be determined as described above.

COMPONENT	VALUE	PART NUMBER	SIZE
L	2.2µH	Coilcraft LPS3010-222ML (1.4A)	
C_{OUT}	10µF	Murata GRM219R60J106KE19B	0805
	22µF	Murata GRM21BR60J226M	0805
	47µF	Murata GRM31CR60J476M	1206
	100µF	Murata GRM31CR60J107M	1206
C_{IN}	4.7µF	Murata GRM188R60J475KE19D	0603

Table 157 Recommended External Components - DC-DC1

Wolfson recommends the following external components for use with DC-DC Converters 3 and 4.

COMPONENT	VALUE	PART NUMBER	SIZE
L	2.2µH	Murata LQM31PN2R2M00 (0.9A)	1206
C_{OUT}	10µF	Murata GRM219R60J106KE19B	0805
C_{IN}	4.7µF	Murata GRM188R60J475KE19D	0603

Table 158 Recommended External Components - DC-DC3 and DC-DC4

29.4 DC-DC (STEP-UP) CONVERTER EXTERNAL COMPONENTS

The DC-DC (Step-Up) Converter can operate as a Switch or as a Boost Converter. In Boost mode, it operates in one of three different modes, set by the DC2_FBSRC register field. The following subsections describe each of these modes in turn.

29.4.1 DC-DC (STEP-UP) CONVERTER - CONSTANT VOLTAGE MODE

Constant voltage mode is selected by setting DC1_FBSRC[1:0] = 00, as described in Section 14.6.4. The recommended connections to the DC-DC (Step-Up) Converter in this mode are illustrated in Figure 89.

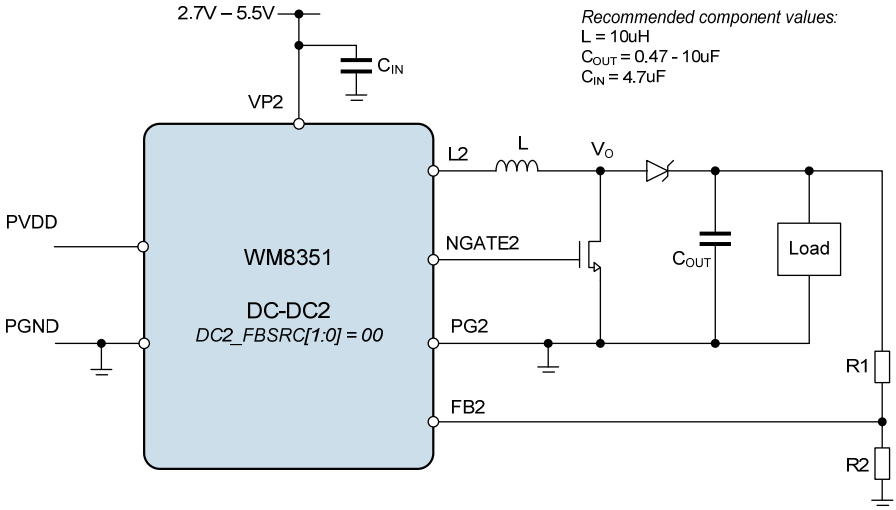


Figure 89 DC-DC (Step-Up) Converter External Components - Constant Voltage Mode

The DC-DC (Step-Up) Converter is capable of generating output voltages of up to 30V. The output voltage is determined by the two external resistors R1 and R2, which form a resistive divider between load connection and the voltage feedback pin FB2 or FB5. The output voltage is set as described in the following equation:

$$V_{OUT} = \frac{(R1/R2) + 1}{2}$$

Setting R2 to 47kΩ is recommended for most applications; R1 can be calculated using the following equation, given the required output voltage:

$$R1 = R2 \,.\, (2V_{OUT} - 1)$$

When selecting suitable capacitors, is it imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. Ceramic X7R or X5R types are recommended.

The choice of output capacitor for DC-DC2 varies depending on the required output voltage. For a 20V output, 0.47μF is recommended. For a 5V output, 10μF is recommended.

When selecting a suitable output inductor, the inductance value and the saturation current must be compatible with the operating conditions of the converter.

The magnitude of the inductor current ripple is dependent on the inductor value and can be determined by the following equation:

$$\triangle I_L = \frac{V_{OUT} - V_{IN}}{L \cdot F_{SW}}$$

$\triangle I_L$ = Inductor ripple current
V_{OUT} = Output voltage
V_{IN} = Input voltage
L = Inductance
F_{SW} = Switching frequency (1MHz)

The inductor current is also a function of the DC-DC Converter maximum input current, which can be determined by the following equation:

$$I_{INmax} = \frac{I_{OUTmax}}{\text{efficiency}} \times \frac{V_{OUT}}{V_{IN}}$$

I_{OUTmax} = Maximum load current
I_{INmax} = Maximum input current
V_{OUT} = Output voltage
V_{IN} = Input voltage

As a minimum requirement, the DC current rating should be equal to the maximum input current plus one half of the inductor current ripple.

$$I_{Lpeak} = I_{OUTmax} + (\triangle I_L / 2)$$

I_{Lpeak} = Inductor peak current
I_{OUTmax} = Maximum load current
$\triangle I_L$ = Inductor ripple current

To be suitable for the application, the chosen inductor must have a saturation current that is higher than the peak inductor current given by the above equation. To maximise the converter efficiency, the inductor should also have a low DC Resistance (DCR), resulting in minimum conduction losses. Care should also be taken to ensure that the inductor is effective at the applicable operating temperature.

See Section 29.4.4 for recommended inductor, capacitor and FET component details.

29.4.2 DC-DC (STEP-UP) CONVERTER - CONSTANT CURRENT MODE

Constant current mode is selected by setting DC2_FBSRC[1:0] = 01, as described in Section 14.6.4. This results in the DC Converter controlling the current at ISINKA. The recommended connections to the DC-DC (Step-Up) Converter in this mode are illustrated in Figure 90.

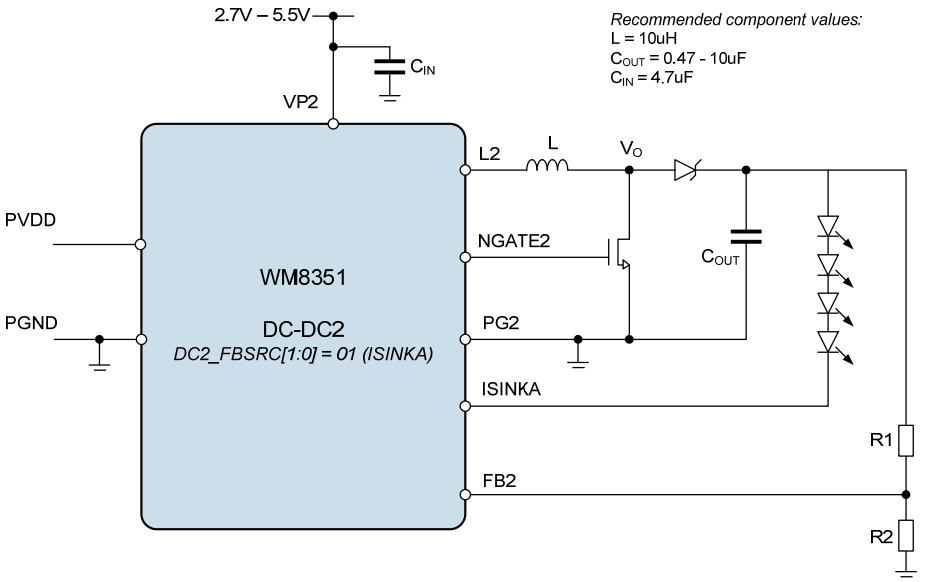


Figure 90 DC-DC (Step-Up) Converter External Components - Constant Current Mode

In the constant current mode, the DC-DC Converter output voltage is controlled by the WM8351 in order to achieve the required current in ISINKA. The required current is set by the CS1_ISEL register field, as described in Section 16.2.2. A typical application for this mode would be a white LED driver, where several LEDs are connected in series to achieve uniform brightness.

The DC-DC (Step-Up) Converters are capable of generating output voltages of up to 30V. The maximum output voltage is determined by the two external resistors R1 and R2, which form a resistive divider between load connection and the voltage feedback pin FB2 or FB5.

The choice of resistors R1 and R2 follows the same equations as for the constant voltage mode (see Section 29.4.1). Note that, in constant current mode, the resistors determine the maximum output voltage. The actual voltage will be determined by the selected ISINK current, subject to the device limits.

The choice of Capacitors, Inductor and FET in constant current mode is the same as for the constant voltage mode; see Section 29.4.4 for specific recommended component details.

When ISINKA is used in conjunction with DC-DC Converter 2, the ISINK should always be switched on before the DC-DC Converter is switched on. Conversely, the DC-DC Converter should always be switched off before the ISINK is switched off.

29.4.3 DC-DC (STEP-UP) CONVERTER - USB MODE

USB mode is selected by setting DC2_FBSRC[1:0] = 11 as described in Section 14.6.4. This mode generates a 5V output, suitable for USB interfaces. The recommended connections to the DC-DC (Step-Up) Converter in this mode are illustrated in Figure 91.

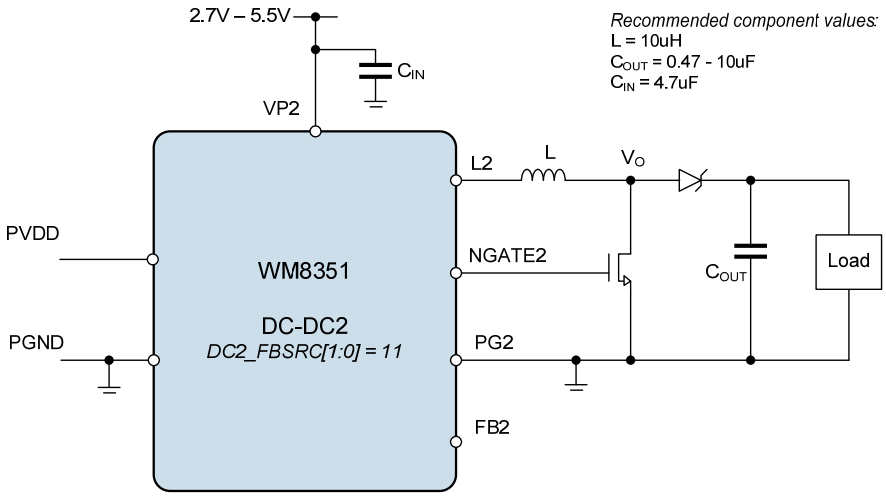


Figure 91 DC-DC (Step-Up) Converter External Components - USB Mode

In the USB mode, the DC-DC (Step-Up) Converter uses an internal resistor chain to control the output voltage. This results in a fixed 5V output, suitable for USB interfaces.

The DC-DC (Step-Up) Converter may be configured as USB OTG supplement by setting USB_MSTR = 1 as described in Section 17.4. (The DC-DC Converter USB mode must also be selected by setting DC2_FBSRC[1:0] = 11). The output of the DC-DC Converter should be connected to the USB pin in order to provide voltage feedback.

The choice of Capacitors, Inductor and FET in constant current mode is the same as for the constant voltage mode; see Section 29.4.4 for specific recommended component details.

29.4.4 DC-DC (STEP-UP) CONVERTER RECOMMENDED COMPONENTS

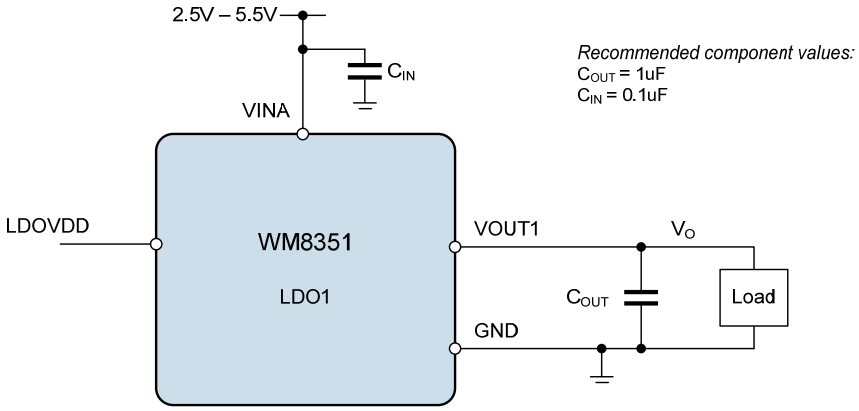
Wolfson recommends the following external components for use with DC-DC Converter 2. Note that the choice of output capacitor should be determined as described in Section 29.4.1.

COMPONENT	VALUE	PART NUMBER	SIZE
L	10µH	Taiyo Yuden NR4012T100M (0.7A)	
C_{OUT}	0.47µF	Murata GRM21BR71E474KC01L	0805
	4.7µF	Murata GRM188R60J475KE19D	0603
	10µF	Murata GRM219R60J106KE19B	0805
C_{IN}	4.7µF	Murata GRM188R60J475KE19D	0603
FET		On Semiconductor NTHD4N02F N-Channel FETKY	

Table 159 Recommended External Components - DC-DC2

29.5 LDO REGULATOR EXTERNAL COMPONENTS

The recommended connections to the LDO Regulators are illustrated in Figure 92.



Note: Equivalent circuit applies for LDO2, LDO3 and LDO4.
Input pin VINA supplies LDO1 and LDO2; Input pin VINB supplies LDO3 and LDO4.

Figure 92 LDO Regulators External Components

When selecting suitable capacitors, is it imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. Ceramic X7R or X5R types are recommended.

Wolfson recommends the following external components for use with LDO Regulators 1, 2, 3 and 4. Note that larger capacitors will improve load transient response and power supply rejection. A maximum of 10µF is possible at the output; a maximum of 1µF is possible at the input.

COMPONENT	VALUE	PART NUMBER	SIZE
C_{OUT}	1µF	Murata GRM155R60J105KE19D	0402
C_{IN}	0.1µF	Phycomp 06032R104K7B2	0603

Table 160 Recommended External Components - LDO1, LDO2, LDO3 and LDO4

29.6 PCB LAYOUT

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. Poor regulation and instability can result.

Simple design rules can be implemented to negate these effects:

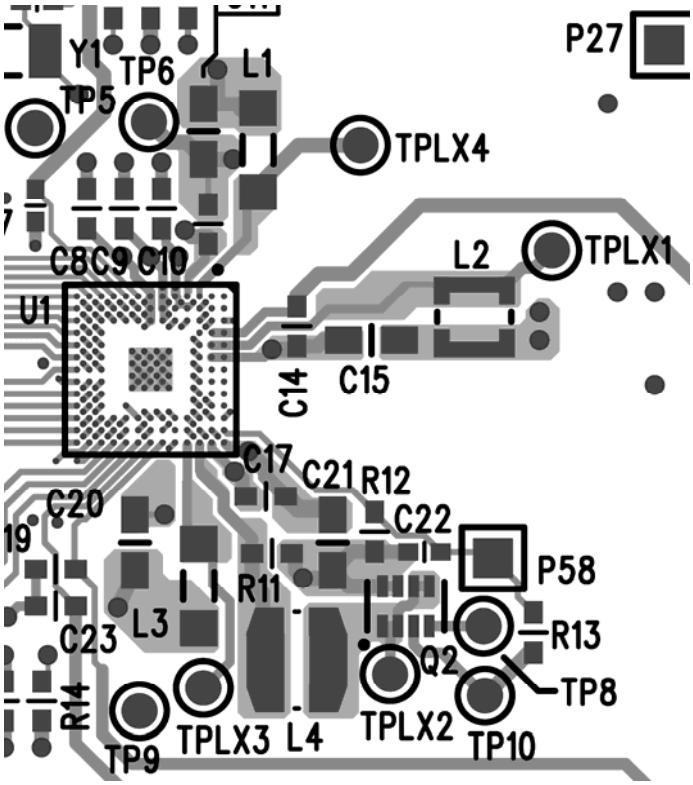
External input and output capacitors should be placed as close to the device as possible using short wide traces between the external power components.

Route output voltage feedback on an inner plane away from inductor and LX nodes to minimise noise and magnetic interference.

Use a local ground island for each individual converter connected at a single point onto a fully flooded ground plane.

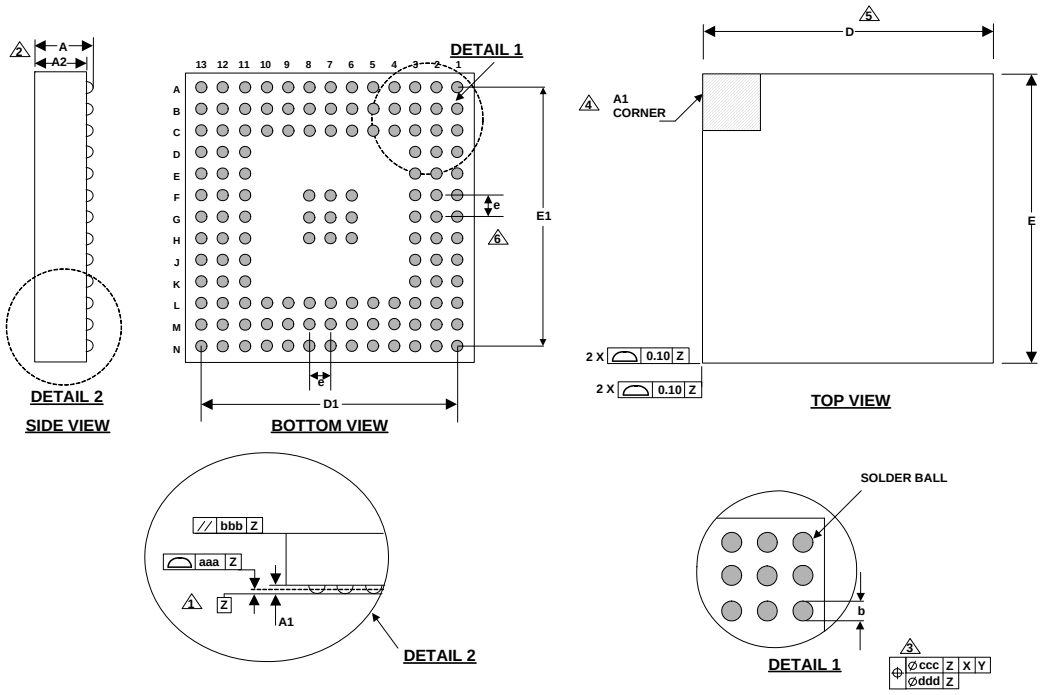
Current loop areas should be kept as small as possible with loop areas changing little during alternating switching cycles.

Studying the layout below shows, for example, DCDC1 layout with external components C16, L3, C17. The input capacitor, C16, is close into the IC and shares a small ground island with C17 the output capacitor. The inductor, L3, is then situated in close proximity to C17 to keep loop area small and current flowing in the same direction during alternating switching cycles. Note also the use of short wide traces with all power tracking on a single (top) layer.



30 PACKAGE DIAGRAM

B: 129 BALL BGA PLASTIC PACKAGE 7 x 7 x 0.94 mm BODY, 0.50 mm BALL PITCH **DM040.C**



Symbols		Dimensions (mm)		
	MIN	NOM	MAX	NOTE
A			1.00	
A1	0.18		0.28	
A2		0.66		
b	0.27		0.37	
D		7.00 BSC		
D1		6.00 BSC		
E		7.00 BSC		
E1		6.00 BSC		
e		0.50 BSC		6
Tolerances of Form and Position				
aaa	0.08			
bbb	0.10			
ccc	0.15			
ddd	0.05			
REF:	JEDEC, MO-195			

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. DIMENSION 'b' IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -Z-.
4. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
6. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
8. FALLS WITHIN JEDEC, MO-195

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32 REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
01/02/11	4.4	PH	REG_RESET_HIB_MODE description corrected, p109, 221
07/04/11	4.5	PH	Watchdog description updated, noting maximum number of reset attempts.
18/04/12	4.5	JMacD	Order codes changed from WM8351GEB/V and WM8351GEB/RV to WM8351**C**GEB/V and WM8351**C**GEB/RV to reflect change to copper wire bonding.
18/04/12	4.5	JMacD	Package diagram updated to DM040.C