NYC0102BLT1G

Sensitive Gate Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed and tested for highly−sensitive triggering in low-power switching applications.

Features

- High dv/dt
- Gating Current < 200 μA
- Miniature SOT−23 Package for High Density PCB
- This is a Halogen−Free Device
- This is a Pb−Free Device

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (R_{GK} = IK, T_J = −40 to +110°C, Sine Wave, 50 to 60 Hz	V_{DRM}, V_{RRM}	200	V
On-State Current RMS (180° Conduction Angle, T_C = 80°C)	$I_{T(RMS)}$	0.25	A
Peak Non-repetitive Surge Current, T_A = 25°C, (1/2 Cycle, Sine Wave, 60 Hz)	I_{TSM}	7.0	A
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	0.2	A^2s
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec, T_A = 25°C)	P_{GM}	0.1	W
Forward Average Gate Power (t = 8.3 msec, T_A = 25°C)	$P_{G(AV)}$	0.02	W
Forward Peak Gate Current (Pulse Width ≤ 20 μs, T_A = 25°C)	I_{FGM}	0.5	A
Reverse Peak Gate Voltage (Pulse Width ≤ 1.0 μs, T_A = 25°C)	V_{RGM}	8.0	V
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board T_A = 25°C	P_D	225	mW
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	380	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

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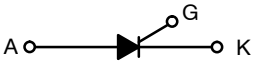
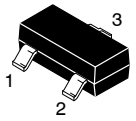
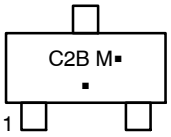
0.25 AMP, 200 VOLT SCRs





SOT−23
CASE 318
STYLE 8

MARKING DIAGRAM



C2B = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

PIN ASSIGNMENT	
1	Cathode
2	Gate
3	Anode

ORDERING INFORMATION

Device	Package	Shipping†
NYC0102BLT1G	SOT−23 (Pb−Free)	3000/Tape & Reel

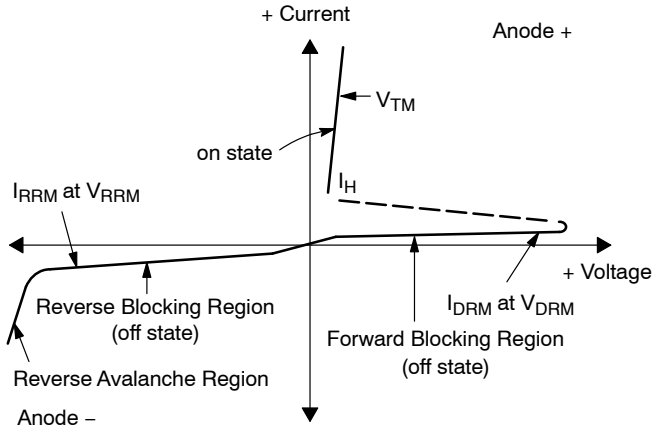
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Forward Blocking Current (V_{DRM} = 200 V, R_{GK} = 1 kΩ)	T_C = 25°C T_C = 125°C	I_{DRM}	– –	– –	1.0 100	μA μA
Peak Repetitive Reverse Blocking Current (V_{DRM} = 200 V, R_{GK} = 1 kΩ)	T_C = 25°C T_C = 125°C	I_{RRM}	– –	– –	1.0 100	μA μA
ON CHARACTERISTICS						
Peak Forward On−State Voltage (I_{TM} = 0.4 A, t_p < 1 ms, T_C = 25°C)		V_{TM}	–	–	1.7	V
Gate Trigger Current (V_D = 12 V, R_L = 100 Ω, T_C = 25°C)		I_{GT}	–	–	200	μA
Gate Trigger Voltage (V_D = 12 V, R_L = 100 Ω, T_C = 25°C)		V_{GT}	–	–	0.8	V
Holding Current (I_T = 50 mA, R_{GK} = 1 kΩ, T_C = 25°C)		I_H	–	–	6.0	mA
Gate Non−Trigger Voltage (V_D = V_{DRM}, R_L = 3.3 kΩ, T_C = 125°C)		V_{GD}	0.1	–	–	V
Latching Current (I_G = 1.0 mA, R_{GK} = 1 kΩ, T_C = 25°C)		I_L	–	–	7.0	mA
Gate Reverse Voltage (I_{RG} = 10 μA)		V_{RG}	8.0	–	–	V
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off−State Voltage (R_{GK} = 1 kΩ, T_C = 125°C)		dv/dt	200	–	–	V/μs
Critical Rate of Rise of On−State Current (I_G = 2xI_{GT} 60 Hz, t_r < 100 ns, T_J = 125°C)		di/dt	–	–	50	A/μs

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak on State Voltage
I_H	Holding Current



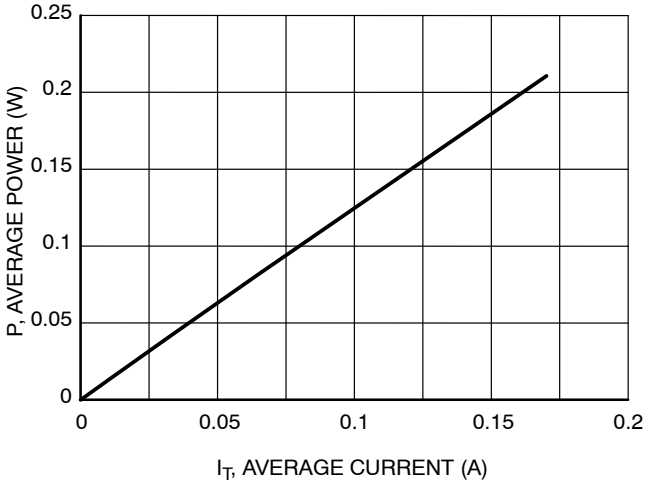


Figure 1. Maximum Average Power vs. Average Current

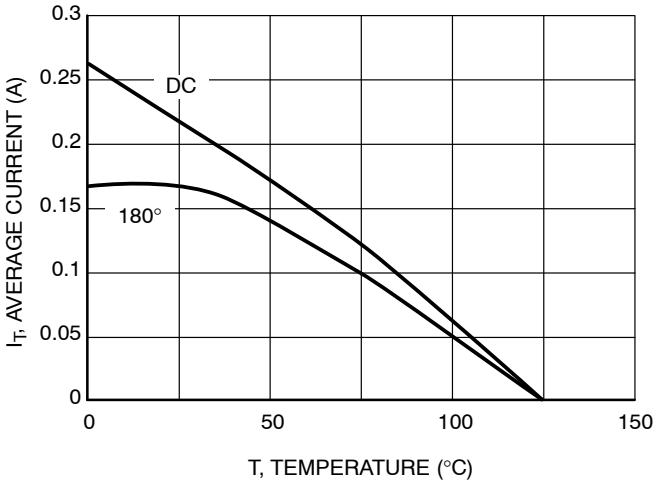


Figure 2. Current Derating

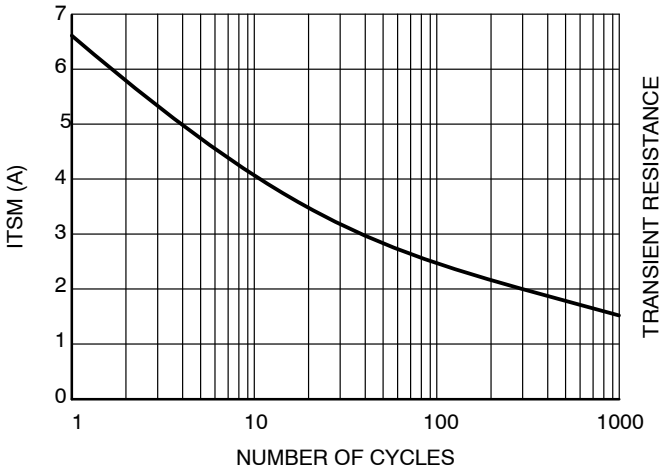


Figure 3. Surge Current ITSM vs. Number of Cycles

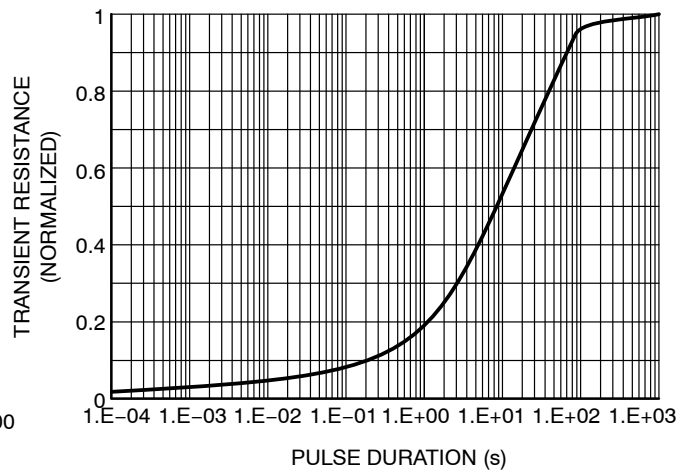


Figure 4. Thermal Response

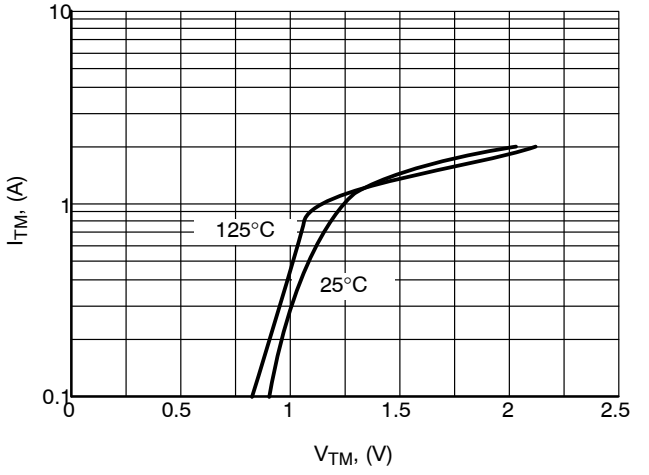


Figure 5. ON−State Characteristics

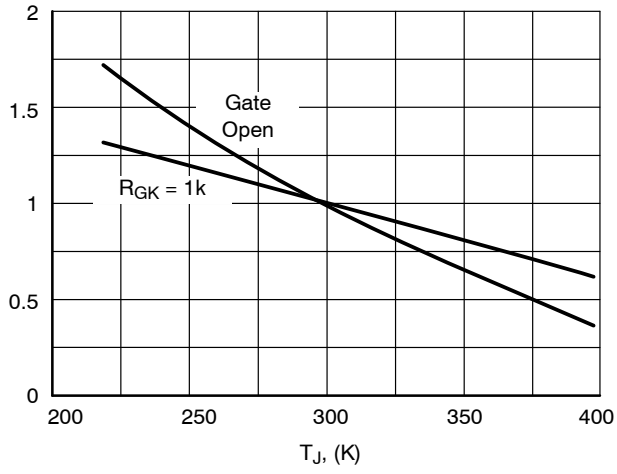


Figure 6. Gate Trigger Current vs. T_J (Normalized to 25°C)

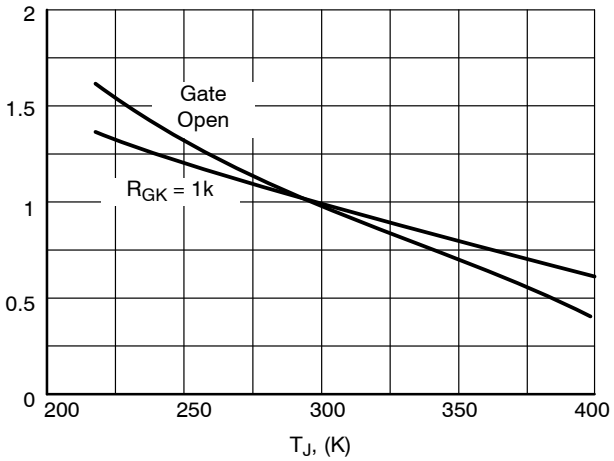


Figure 7. Gate Trigger Current vs. T_J (Normalized to 25°C)

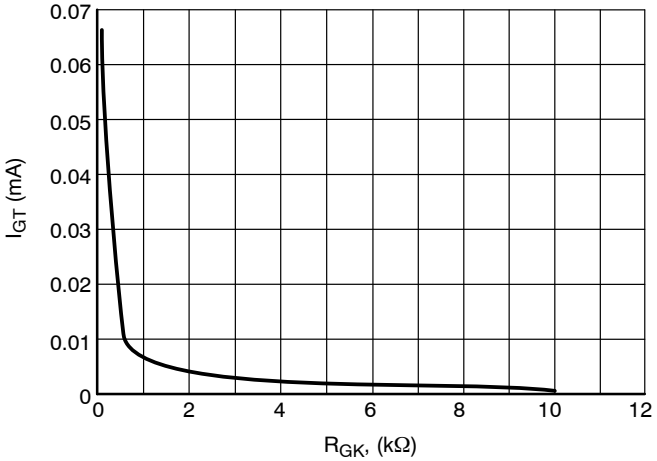


Figure 8. Gate Trigger Current vs. R_{GK}

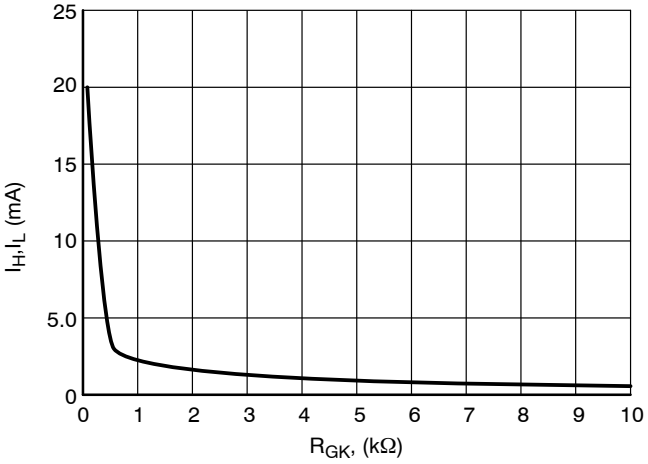


Figure 9. Holding and Latching Current vs. R_{GK}

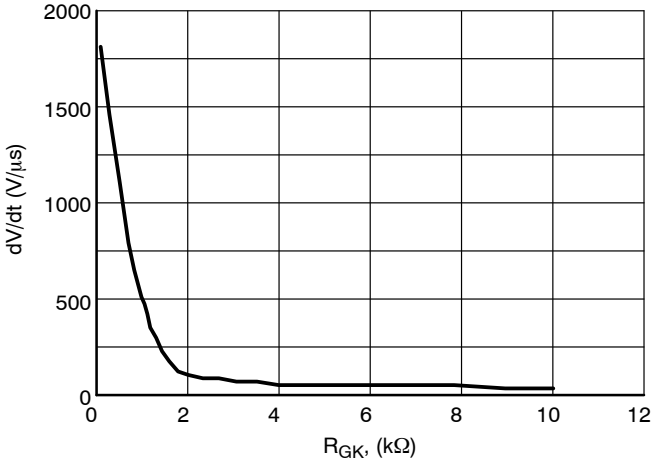


Figure 10. dV/dt vs. R_{GK}

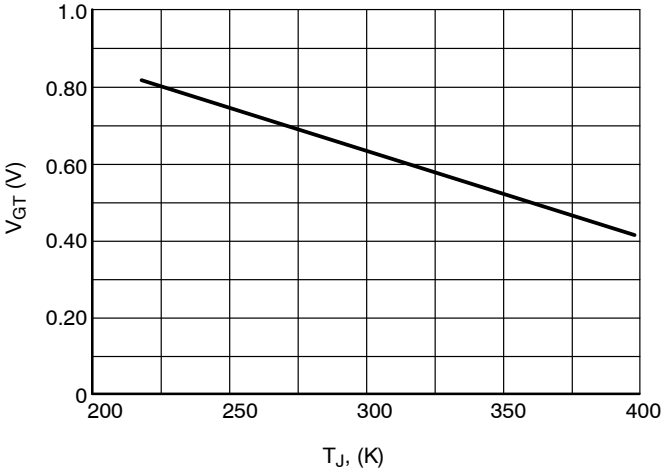
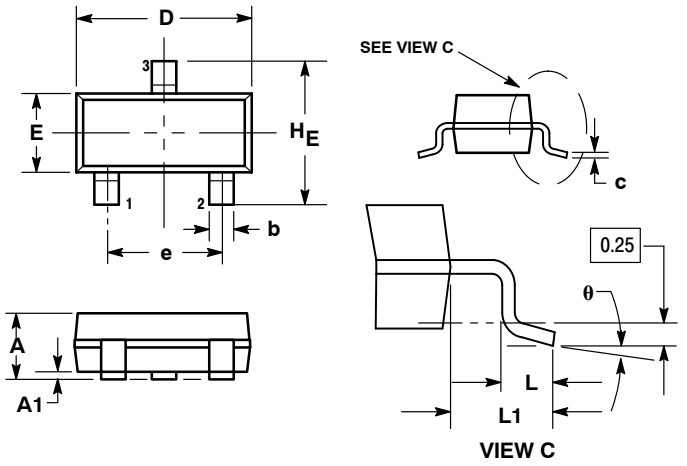


Figure 11. Gate Triggering Voltage vs. T_J

NYC0102BLT1G

PACKAGE DIMENSIONS

SOT−23 (TO−236)]
CASE 318−08
ISSUE AN

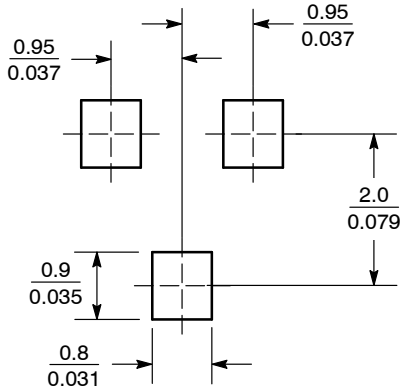


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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