FAIRCHILD

SEMICONDUCTOR™

74LVT162244 • 74LVTH162244
Low Voltage 16-Bit Buffer/Line Driver
with 3-STATE Outputs
and 25Ω Series Resistors in the Outputs

General Description

The LVT162244 and LVTH162244 contain sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The LVT162244 and LVTH162244 are designed with equivalent 25Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH162244 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT162244 and LVTH162244 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

■ Input and output interface capability to systems at 5V V_{CC}

■ Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH162244), also available without bushold feature (74LVT162244).

■ Live insertion/extraction permitted

■ Power Up/Power Down high impedance provides glitch-free bus loading

■ Outputs include equivalent series resistance of 25Ω to make external termination resistors unnecessary and reduce overshoot and undershoot

■ Functionally compatible with the 74 series 162244

■ Latch-up performance exceeds 500 mA

■ ESD performance:

  Human-body model > 2000V

  Machine model > 200V

  Charged-device > 1000V

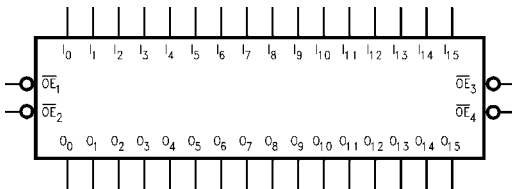■ Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Ordering Code:

Order Number	Package Number	Package Description
74LVT162244G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVT162244MEA (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT162244MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH162244G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVTH162244MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [Tube]
74LVTH162244MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [Tape and Reel]
74LVTH162244MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [Tube]
74LVTH162244MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [Tape and Reel]

Note 1: Ordering code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
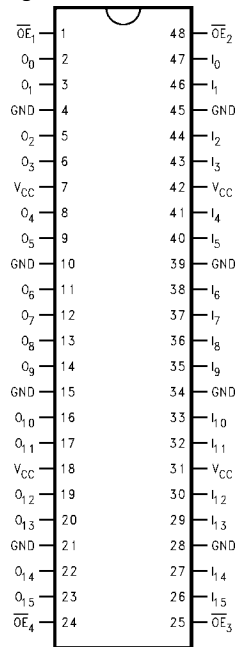
74LVT162244 • 74LVTH162244

Logic Symbol

Connection Diagrams

Pin Assignment for SSOP and TSSOP

$\overline{OE}_1$	1	48	$\overline{OE}_2$
O_0	2	47	I_0
O_1	3	46	I_1
GND	4	45	GND
O_2	5	44	I_2
O_3	6	43	I_3
V_{CC}	7	42	V_{CC}
O_4	8	41	I_4
O_5	9	40	I_5
GND	10	39	GND
O_6	11	38	I_6
O_7	12	37	I_7
O_8	13	36	I_8
O_9	14	35	I_9
GND	15	34	GND
O_{10}	16	33	I_{10}
O_{11}	17	32	I_{11}
V_{CC}	18	31	V_{CC}
O_{12}	19	30	I_{12}
O_{13}	20	29	I_{13}
GND	21	28	GND
O_{14}	22	27	I_{14}
O_{15}	23	26	I_{15}
$\overline{OE}_4$	24	25	$\overline{OE}_3$

Pin Assignment for FBGA

(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active LOW)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs
NC	No Connect
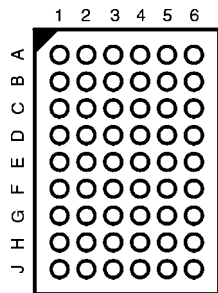
FBGA Pin Assignments

	1	2	3	4	5	6
A	O_0	NC	$\overline{OE}_1$	$\overline{OE}_2$	NC	I_0
B	O_2	O_1	NC	NC	I_1	I_2
C	O_4	O_3	V_{CC}	V_{CC}	I_3	I_4
D	O_6	O_5	GND	GND	I_5	I_6
E	O_8	O_7	GND	GND	I_7	I_8
F	O_{10}	O_9	GND	GND	I_9	I_{10}
G	O_{12}	O_{11}	V_{CC}	V_{CC}	I_{11}	I_{12}
H	O_{14}	O_{13}	NC	NC	I_{13}	I_{14}
J	O_{15}	NC	$\overline{OE}_4$	$\overline{OE}_3$	NC	I_{15}

Truth Table

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level   L = LOW Voltage Level
Z = High Impedance   X = Immaterial

Functional Description

The LVT162244 and LVTH162244 contain sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Logic Diagram
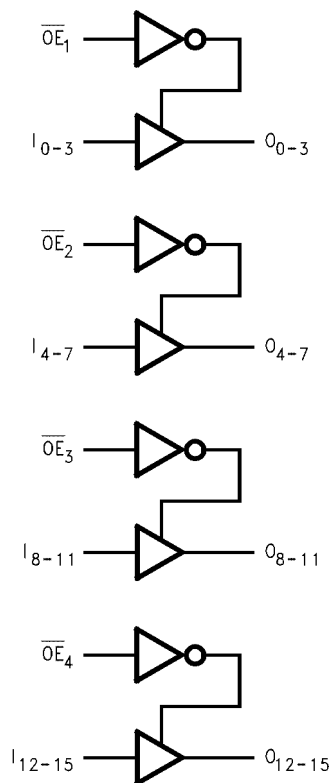
Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current	−50	$V_I <$ GND	mA
I_{OK}	DC Output Diode Current	−50	$V_O <$ GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		−12	mA
I_{OL}	LOW-Level Output Current		12	mA
T_A	Free Air Operating Temperature	−40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	T_A = −40°C to +85°C		Units	Conditions
				Min	Max		
V_{IK}	Input Clamp Diode Voltage		2.7		−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \leq$ 0.1V or
V_{IL}	Input LOW Voltage		2.7–3.6		0.8	V	$V_O \geq V_{CC}$ − 0.1V
V_{OH}	Output HIGH Voltage		2.7–3.6	V_{CC}−0.2		V	I_{OH} = −100 μA
			3.0	2.0			I_{OH} = −12 mA
V_{OL}	Output LOW Voltage		2.7		0.2	V	I_{OL} = 100 μA
			3.0		0.8		I_{OL} = 12 mA
$I_{I(HOLD)}$ (Note 5)	Bushold Input Minimum Drive		3.0	75		μA	V_I = 0.8V
				−75			V_I = 2.0V
$I_{I(OD)}$ (Note 5)	Bushold Input Over-Drive Current to Change State		3.0	500		μA	(Note 6)
				−500			(Note 7)
I_I	Input Current		3.6		10	μA	V_I = 5.5V
		Control Pins	3.6		±1		V_I = 0V or V_{CC}
		Data Pins	3.6		−5		V_I = 0V
					1		$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0		±100	μA	0V $\leq V_I$ or $V_O \leq$ 5.5V
$I_{PU/PD}$	Power Up/Down 3-STATE Current		0–1.5V		±100	μA	V_O = 0.5V to 3.0V
							V_I = GND or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6		−5	μA	V_O = 0.5V
I_{OZH}	3-STATE Output Leakage Current		3.6		5	μA	V_O = 3.0V
I_{OZH^+}	3-STATE Output Leakage Current		3.6		10	μA	$V_{CC} < V_O \leq$ 5.5V
I_{CCH}	Power Supply Current		3.6		0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current		3.6		5	mA	Outputs LOW
I_{CCZ}	Power Supply Current		3.6		0.19	mA	Outputs Disabled

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_CC (V)	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Conditions
I_CCZ+	Power Supply Current	3.6		0.19	mA	$V_{CC} \leq V_O \leq 5.5V$, Outputs Disabled
ΔI_CC	Increase in Power Supply Current (Note 8)	3.6		0.2	mA	One Input at V_{CC} − 0.6V Other Inputs at V_{CC} or GND

Note 5: Applies to bushold versions only (74LVTH162244).

Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 8: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 9)

Symbol	Parameter	V_CC (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	Units	Conditions C_L = 50 pF, R_L = 500Ω
V_OLP	Quiet Output Maximum Dynamic V_OL	3.3		0.8		V	(Note 10)
V_OLV	Quiet Output Minimum Dynamic V_OL	3.3		−0.8		V	(Note 10)

Note 9: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 10: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

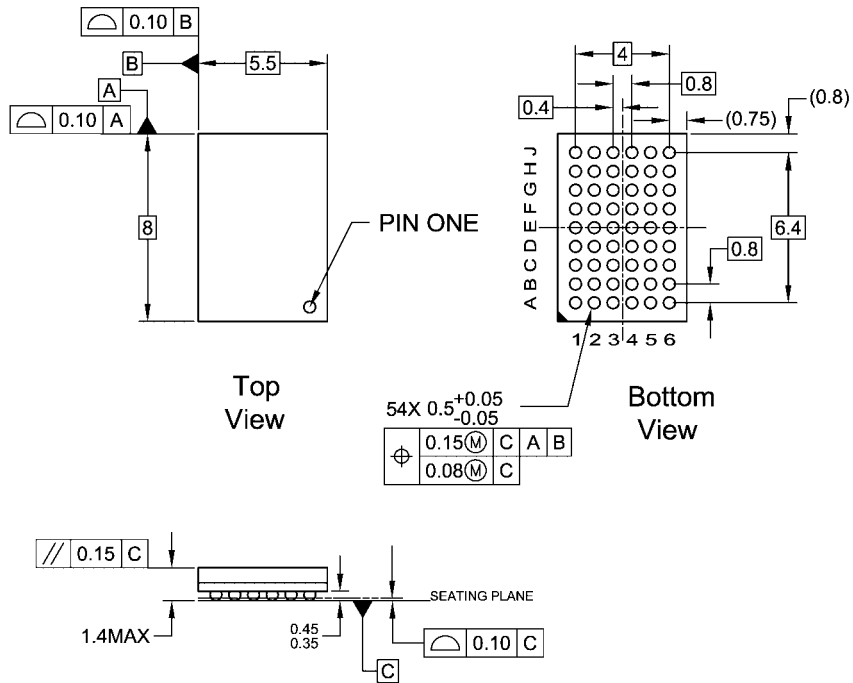| Symbol	Parameter	T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω V_CC = 3.3V ± 0.3V Min	V_CC = 3.3V ± 0.3V Max	V_CC = 2.7V Min	V_CC = 2.7V Max	Units
t_PLH	Propagation Delay Data to Output	1.4	4.0	1.4	4.8	ns
t_PHL		1.2	3.7	1.2	4.1	
t_PZH	Output Enable Time	1.2	5.1	1.2	6.5	ns
t_PZL		1.4	5.4	1.4	6.9	
t_PHZ	Output Disable Time	2.0	5.0	2.0	5.4	ns
t_PLZ		1.5	5.0	1.5	5.4	
t_OSHL	Output to Output Skew		1.0		1.0	ns
t_OSLH	(Note 11)					

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 12)

Symbol	Parameter	Conditions	Typical	Units
C_IN	Input Capacitance	V_{CC} = 0V, V_I = 0V or V_{CC}	4	pF
C_OUT	Output Capacitance	V_{CC} = 3.0V, V_O = 0V or V_{CC}	8	pF

Note 12: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

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Physical Dimensions inches (millimeters) unless otherwise noted

| 0.10 | B |

B

5.5

A

| 0.10 | A |

8

PIN ONE

Top
View

4

0.8

0.4

(0.8)

(0.75)

A B C D E F G H J

6.4

0.8

1 2 3 4 5 6

Bottom
View

$54X\ 0.5^{+0.05}_{-0.05}$

| ⊕ | 0.15Ⓜ | C | A | B |
| | 0.08Ⓜ | C | | |

| // | 0.15 | C |

SEATING PLANE

1.4MAX

0.45
0.35

| 0.10 | C |

C

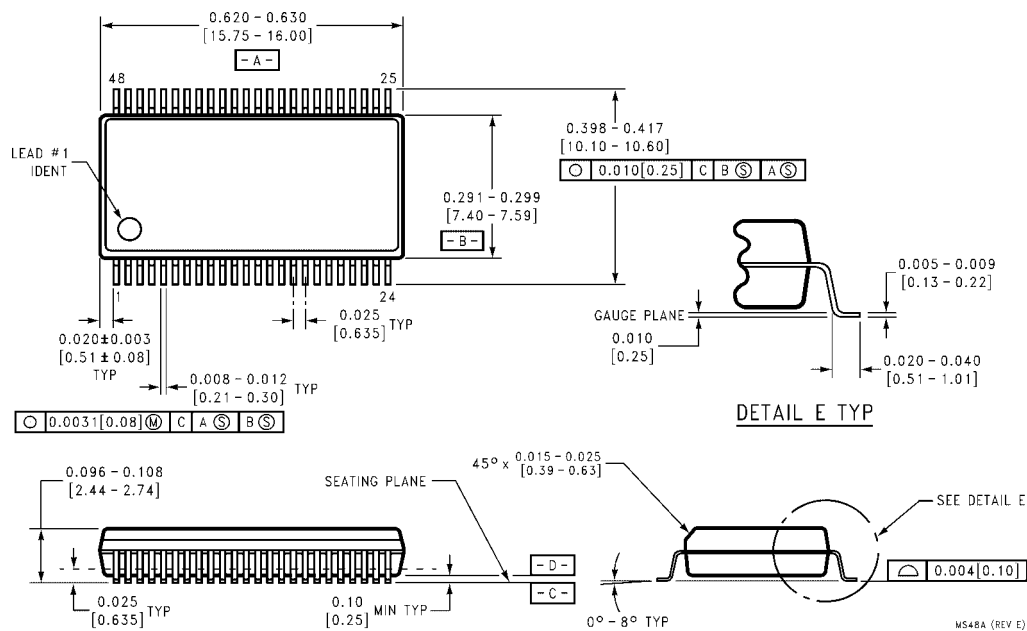NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
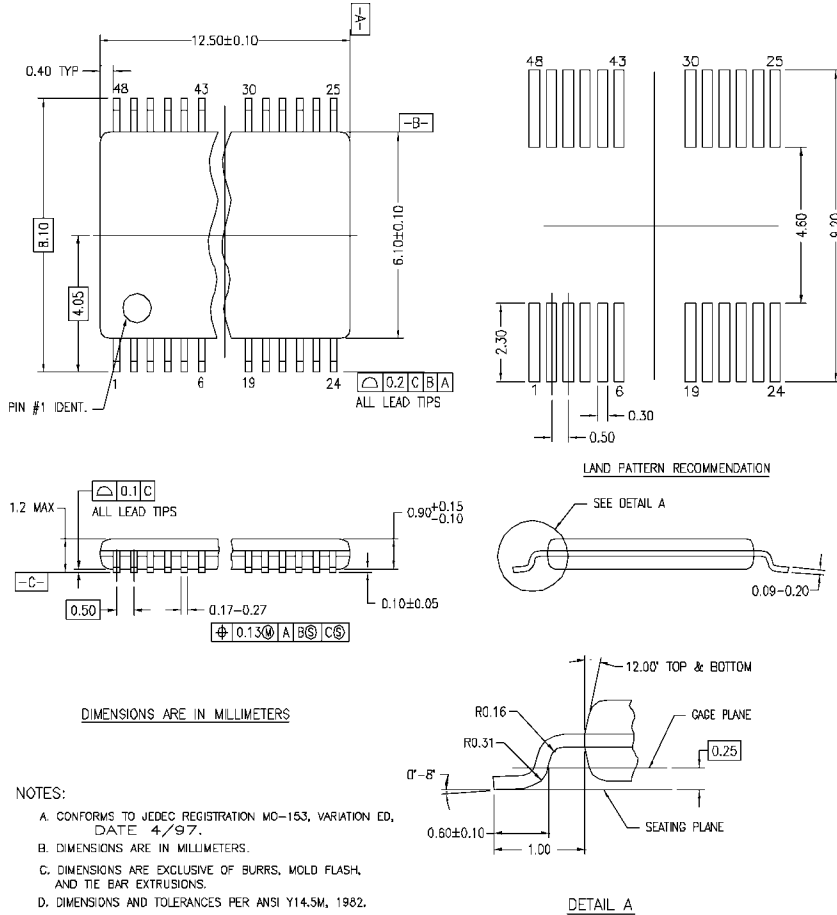D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.620 – 0.630
[15.75 – 16.00]
– A –

48   25

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]

⊘ 0.010[0.25] C B Ⓢ A Ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

1   24

0.025
[0.635] TYP

0.020±0.003
[0.51 ± 0.08]
TYP

0.008 – 0.012
[0.21 – 0.30] TYP

⊘ 0.0031[0.08] Ⓜ C A Ⓢ B Ⓢ

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE
0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

– D –
– C –

0.025
[0.635] TYP

0.10
[0.25] MIN TYP

0° – 8° TYP

△ 0.004[0.10]

MS48A (REV E)

48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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