FAIRCHILD SEMICONDUCTOR®

December 2007

74VHC125
Quad Buffer with 3-STATE Outputs

Features

- High Speed: t_{PD} = 3.8ns (Typ.) at V_{CC} = 5V
- Lower power dissipation: I_{CC} = 4 µA (Max.) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power down protection is provided on all inputs
- Low noise: V_{OLP} = 0.8V (Max.)
- Pin and function compatible with 74HC125

General Description

The VHC125 contains four independent non-inverting buffers with 3-STATE outputs. It is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology and achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

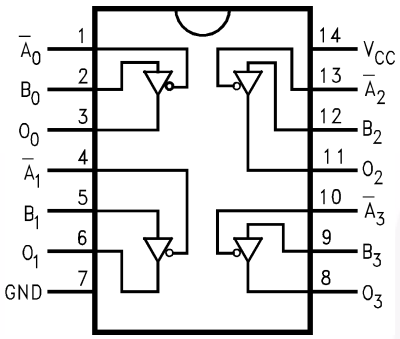
Ordering Information

Order Number	Package Number	Package Description
74VHC125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

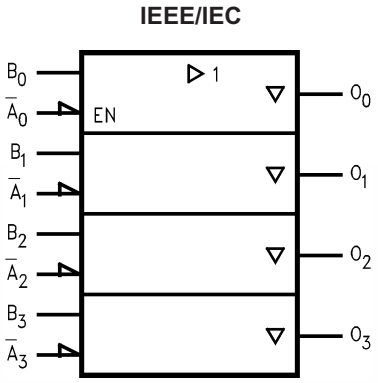
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
$\overline{A}_n$, B_n	Inputs
O_n	Outputs

Function Table

Inputs		Output
$\overline{A}_n$	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

Z = HIGH Impedance

X = Immaterial

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC} / GND Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time,	
	V_{CC} = 3.3V ± 0.3V	0ns/V ~ 100ns/V
	V_{CC} = 5.0V ± 0.5V	0ns/V ~ 20ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C Min.	25°C Typ.	25°C Max.	–40°C to +85°C Min.	–40°C to +85°C Max.	Units
V_{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V
		3.0–5.5			0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V
		3.0–5.5					0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –50µA	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		I_{OH} = –4mA	2.58			2.48		
		4.5		I_{OH} = –8mA	3.94			3.80		
V_{OL}	LOW Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50µA		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		I_{OL} = 4mA			0.36		0.44	
		4.5		I_{OL} = 8mA			0.36		0.44	
I_{OZ}	3-STATE Output Off-State Current	5.5	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC} or GND				±0.25		±2.5	µA
I_{IN}	Input Leakage Current	0–5.5	V_{IN} = 5.5V or GND				±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND				4.0		40.0	µA

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C Typ.	T_A = 25°C Limits	Units
V_{OLP}[2]	Quiet Output Maximum Dynamic V_{OL}	5.0	C_L = 50pF	0.5	0.8	V
V_{OLV}[2]	Quiet Output Minimum Dynamic V_{OL}	5.0	C_L = 50pF	–0.5	–0.8	V
V_{IHD}[2]	Minimum HIGH Level Dynamic Input Voltage	5.0	C_L = 50pF		3.5	V
V_{ILD}[2]	Maximum HIGH Level Dynamic Input Voltage	5.0	C_L = 50pF		1.5	V

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C			T_A = –40°C to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time	3.3 ± 0.3		C_L = 15pF		5.6	8.0	1.0	9.5	ns
				C_L = 50pF		8.1	11.5	1.0	13.0	
		5.0 ± 0.5		C_L = 15pF		3.8	5.5	1.0	6.5	ns
				C_L = 50pF		5.3	7.5	1.0	8.5	
t_{PZL}, t_{PZH}	3-STATE Output Enable Time	3.3 ± 0.3	R_L = 1kΩ	C_L = 15pF		5.4	8.0	1.0	9.5	ns
				C_L = 50pF		7.9	11.5	1.0	13.0	
		5.0 ± 0.5		C_L = 15pF		3.6	5.1	1.0	6.0	ns
				C_L = 50pF		5.1	7.1	1.0	8.0	
t_{PLZ}, t_{PHZ}	3-STATE Output Disable Time	3.3 ± 0.3	R_L = 1kΩ	C_L = 50pF		9.5	13.2	1.0	15.0	ns
		5.0 ± 0.5		C_L = 50pF		6.1	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	3.3 ± 0.3	(3)	C_L = 50pF			1.5		1.5	ns
		5.0 ± 0.5		C_L = 50pF			1.0		1.0	
C_{IN}	Input Capacitance		V_{CC} = Open			4	10		10	pF
C_{OUT}	Output Capacitance		V_{CC} = 5.0V			6				pF
C_{PD}	Power Dissipation Capacitance		(4)			14				pF

Notes:

3. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$; $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$.

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (Opr.) = C_{PD} • V_{CC} • f_{IN} + I_{CC} / 4 (per bit).

Physical Dimensions

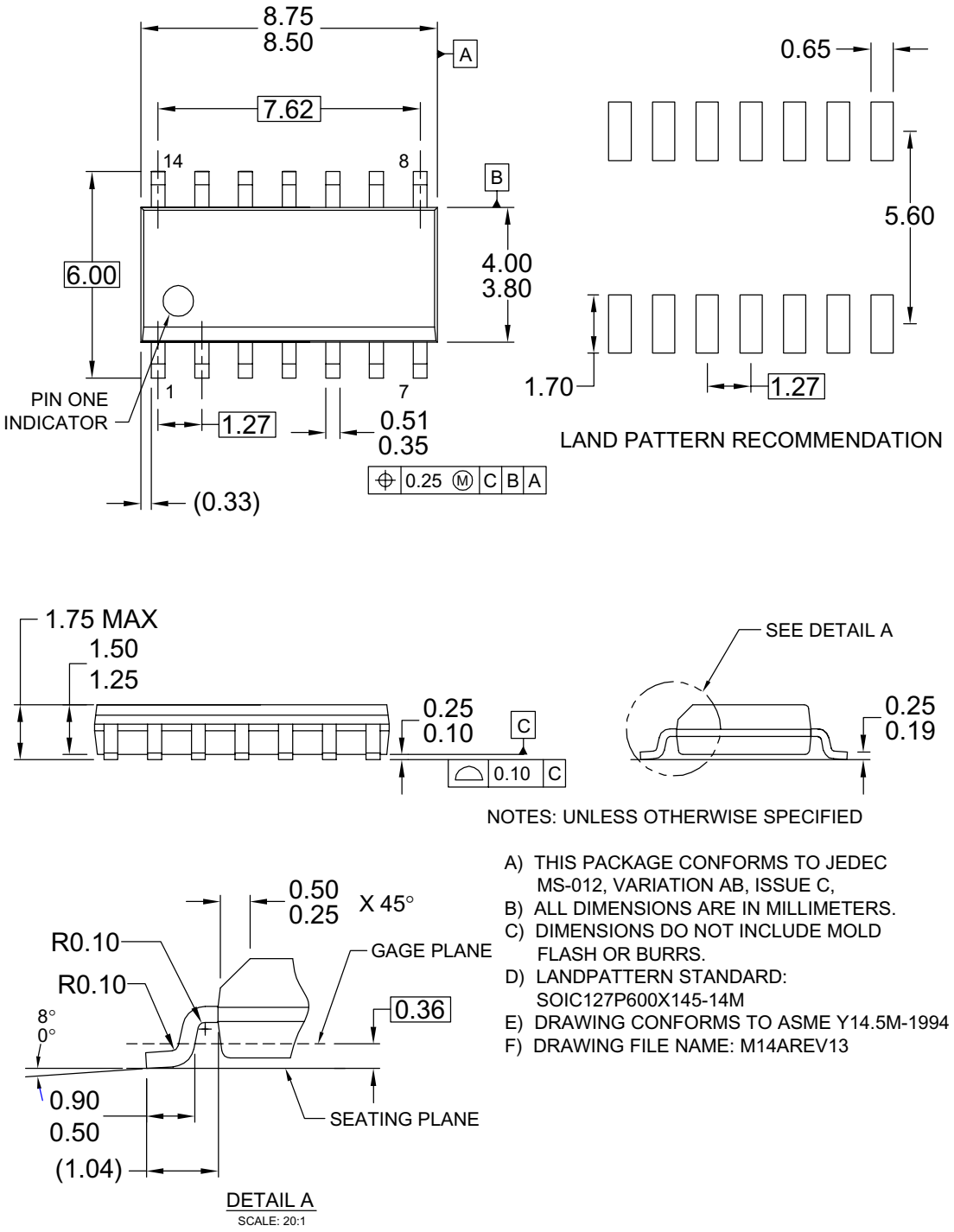


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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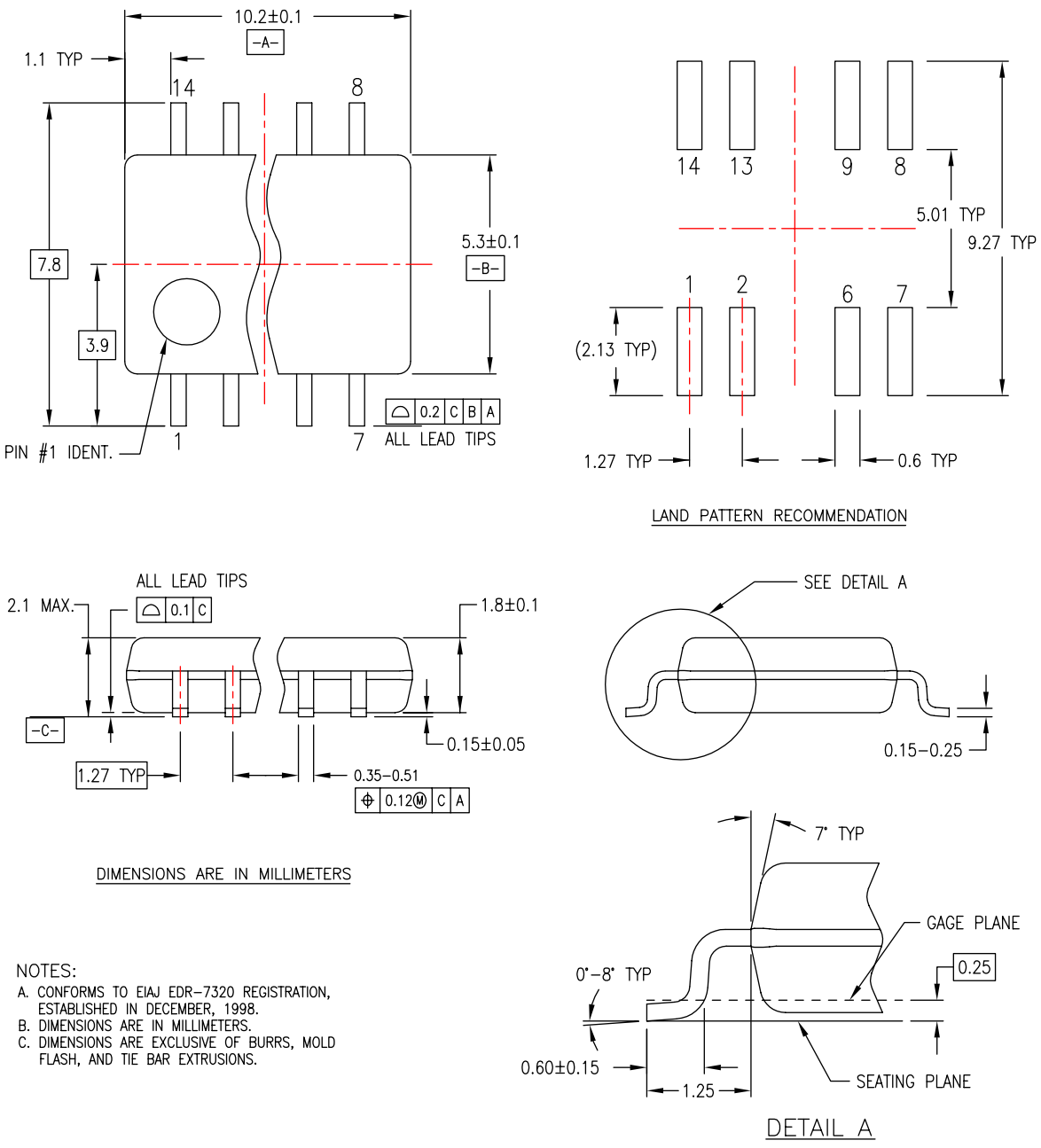
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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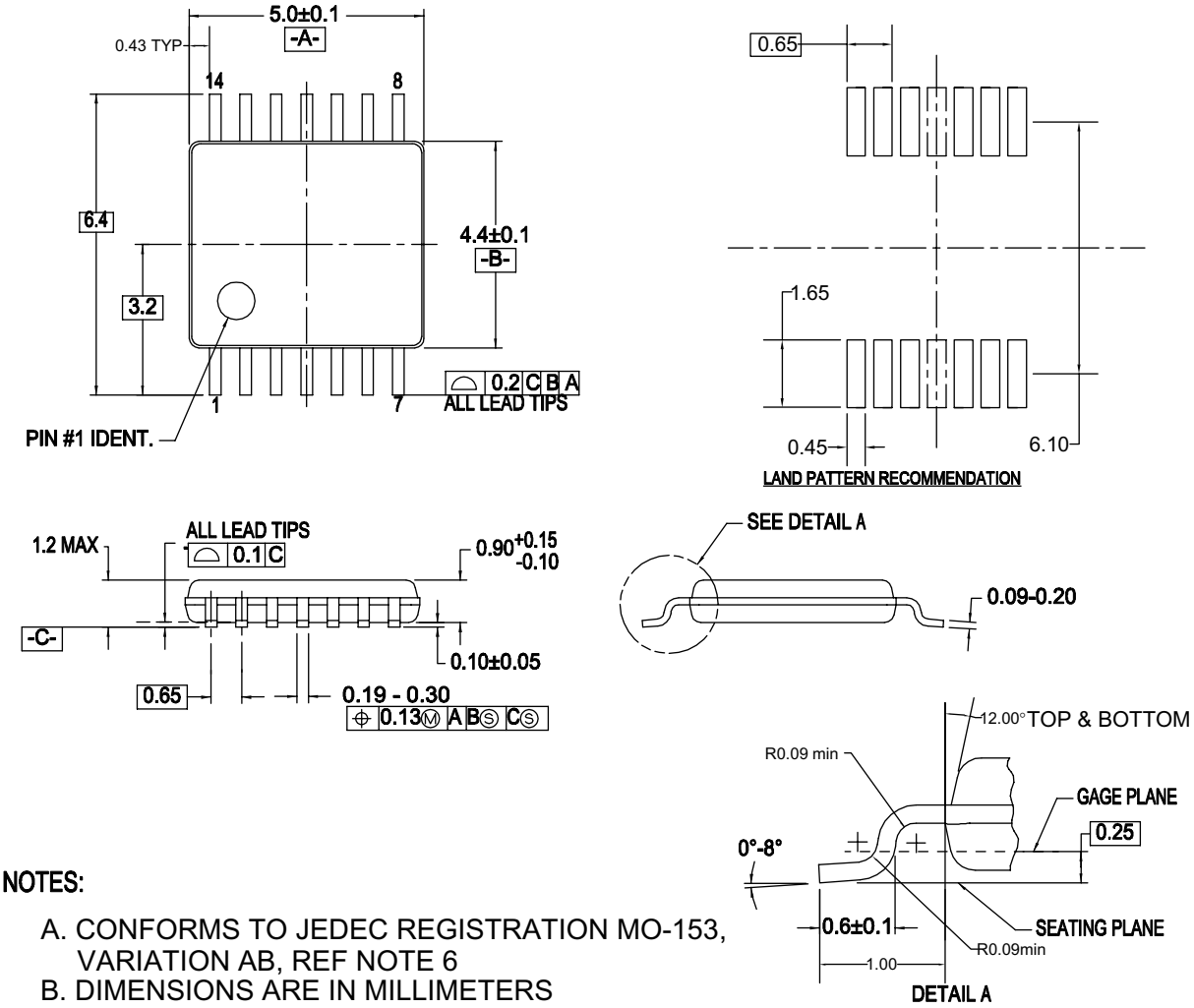
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS

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D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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