

FDP18N50 / FDPF18N50 / FDPF18N50T

500V N-Channel MOSFET

Features

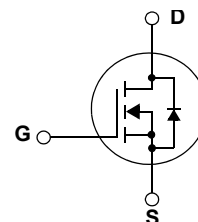
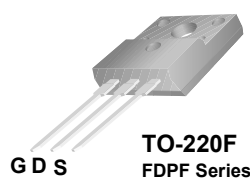
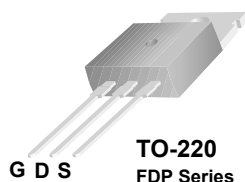
- 18A, 500V, $R_{DS(on)} = 0.265\Omega @V_{GS} = 10V$
- Low gate charge (typical 45 nC)
- Low C_{rss} (typical 25 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



Absolute Maximum Ratings

| Symbol | Parameter | FDP18N50 | FDPF18N50 / FDPF18N50T | Unit |
|----------------|---|--|------------------------|---------------------|
| V_{DSS} | Drain-Source Voltage | 500 | | V |
| I_D | Drain Current | - Continuous ($T_C = 25^\circ\text{C}$) | 18 | 18 * |
| | | - Continuous ($T_C = 100^\circ\text{C}$) | 10.8 | 10.8 * |
| I_{DM} | Drain Current - Pulsed (Note 1) | 72 | 72 * | A |
| V_{GSS} | Gate-Source voltage | ± 30 | | V |
| E_{AS} | Single Pulsed Avalanche Energy (Note 2) | 945 | | mJ |
| I_{AR} | Avalanche Current (Note 1) | 18 | | A |
| E_{AR} | Repetitive Avalanche Energy (Note 1) | 23.5 | | mJ |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | 4.5 | | V/ns |
| P_D | Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C | 235 | 38.5 | W |
| | | 1.88 | 0.3 | W/ $^\circ\text{C}$ |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | | $^\circ\text{C}$ |
| T_L | Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds | 300 | | $^\circ\text{C}$ |

* Drain current limited by maximum junction temperature

Thermal Characteristics

| Symbol | Parameter | FDP18N50 | FDPF18N50 / FDPF18N50T | Unit |
|-----------------|---|----------|------------------------|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 0.53 | 3.3 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta CS}$ | Thermal Resistance, Case-to-Sink Typ. | 0.5 | -- | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 62.5 | 62.5 | $^\circ\text{C}/\text{W}$ |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|------------|---------|-----------|------------|----------|
| FDP18N50 | FDP18N50 | TO-220 | - | - | 50 |
| FDPF18N50 | FDPF18N50 | TO-220F | - | - | 50 |
| FDPF18N50T | FDPF18N50T | TO-220F | - | - | 50 |

Electrical Characteristics T_C = 25°C unless otherwise noted

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|--|------|-------|---------|----------|
| Off Characteristics | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} = 0V, I _D = 250μA | 500 | -- | -- | V |
| ΔBV _{DSS} / ΔT _J | Breakdown Voltage Temperature Coefficient | I _D = 250μA, Referenced to 25°C | -- | 0.5 | -- | V/°C |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 500V, V _{GS} = 0V V _{DS} = 400V, T _C = 125°C | -- | -- | 1 10 | μA μA |
| I _{GSSF} | Gate-Body Leakage Current, Forward | V _{GS} = 30V, V _{DS} = 0V | -- | -- | 100 | nA |
| I _{GSSR} | Gate-Body Leakage Current, Reverse | V _{GS} = -30V, V _{DS} = 0V | -- | -- | -100 | nA |
| On Characteristics | | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} = V _{GS} , I _D = 250μA | 3.0 | -- | 5.0 | V |
| R _{DS(on)} | Static Drain-Source On-Resistance | V _{GS} = 10V, I _D = 9A | -- | 0.220 | 0.265 | Ω |
| g _{FS} | Forward Transconductance | V _{DS} = 40V, I _D = 9A (Note 4) | -- | 25 | -- | S |
| Dynamic Characteristics | | | | | | |
| C _{iss} | Input Capacitance | V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz | -- | 2200 | 2860 | pF |
| C _{oss} | Output Capacitance | | -- | 330 | 430 | pF |
| C _{rss} | Reverse Transfer Capacitance | | -- | 25 | 40 | pF |
| Switching Characteristics | | | | | | |
| t _{d(on)} | Turn-On Delay Time | V _{DD} = 250V, I _D = 18A R _G = 25Ω (Note 4, 5) | -- | 55 | 120 | ns |
| t _r | Turn-On Rise Time | | -- | 165 | 340 | ns |
| t _{d(off)} | Turn-Off Delay Time | | -- | 95 | 200 | ns |
| t _f | Turn-Off Fall Time | | -- | 90 | 190 | ns |
| Q _g | Total Gate Charge | V _{DS} = 400V, I _D = 18A V _{GS} = 10V (Note 4, 5) | -- | 45 | 60 | nC |
| Q _{gs} | Gate-Source Charge | | -- | 12.5 | -- | nC |
| Q _{gd} | Gate-Drain Charge | | -- | 19 | -- | nC |
| Drain-Source Diode Characteristics and Maximum Ratings | | | | | | |
| I _S | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 18 | A |
| I _{SM} | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 72 | A |
| V _{SD} | Drain-Source Diode Forward Voltage | V _{GS} = 0V, I _S = 18A | -- | -- | 1.4 | V |
| t _{rr} | Reverse Recovery Time | V _{GS} = 0V, I _S = 18A di/dt = 100A/μs (Note 4) | -- | 500 | -- | ns |
| Q _{rr} | Reverse Recovery Charge | | -- | 5.4 | -- | μC |

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 5.2mH, I_{AS} = 18A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 18A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

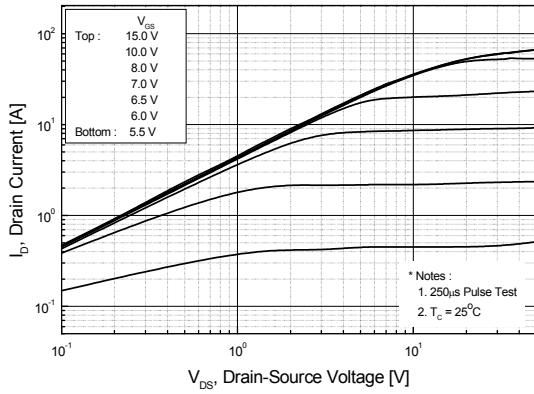


Figure 2. Transfer Characteristics

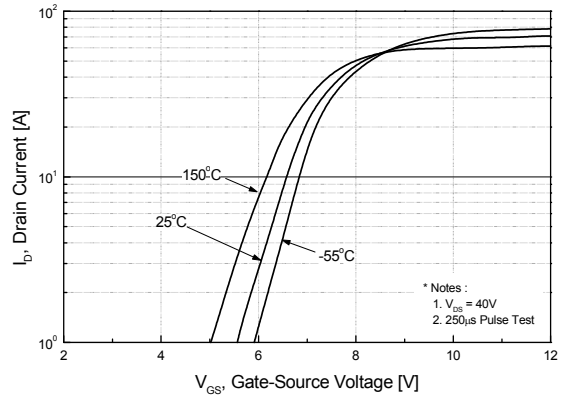


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

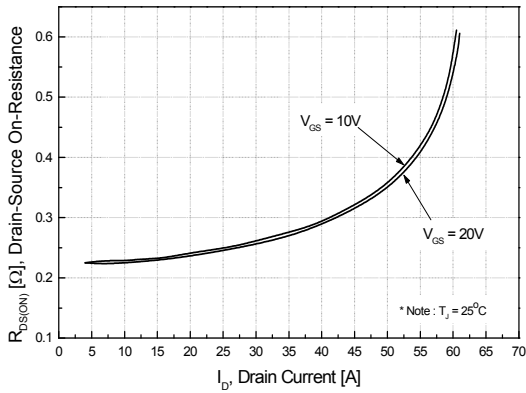


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

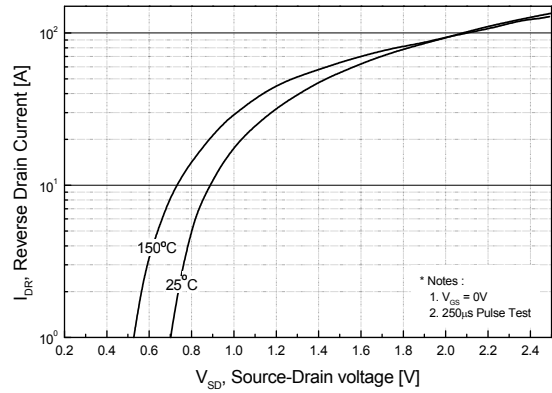


Figure 5. Capacitance Characteristics

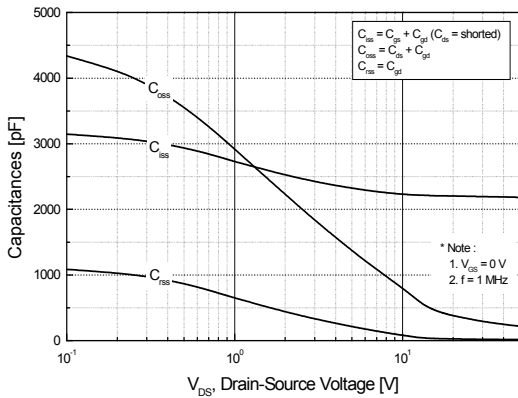
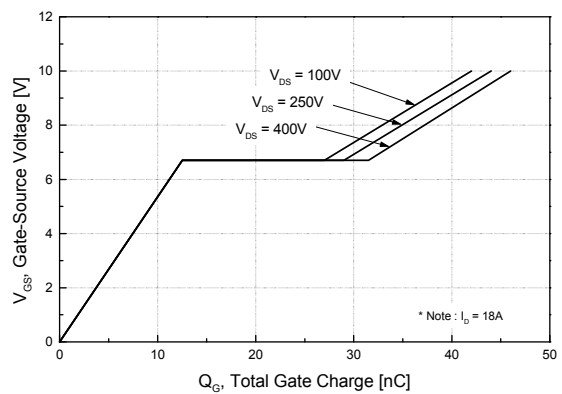


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

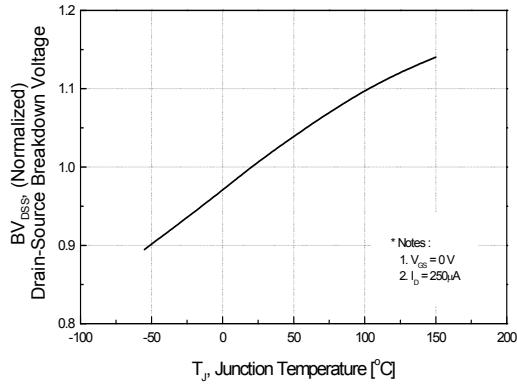


Figure 8. On-Resistance Variation vs. Temperature

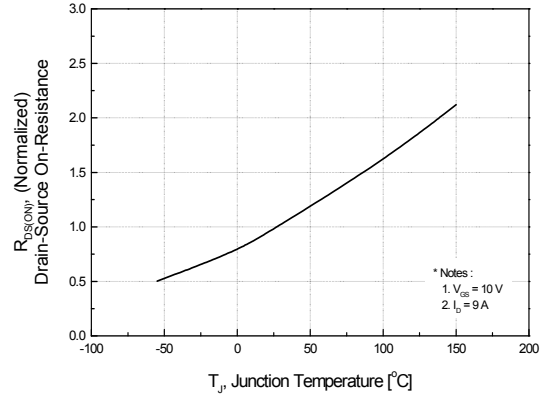


Figure 9-1. Maximum Safe Operating Area - FDP18N50

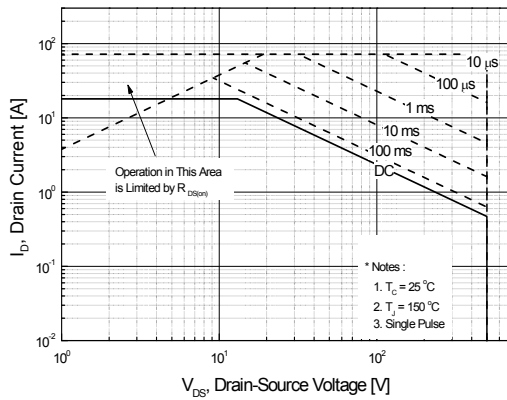


Figure 9-2. Maximum Safe Operating Area - FDPF18N50 / FDPF18N50T

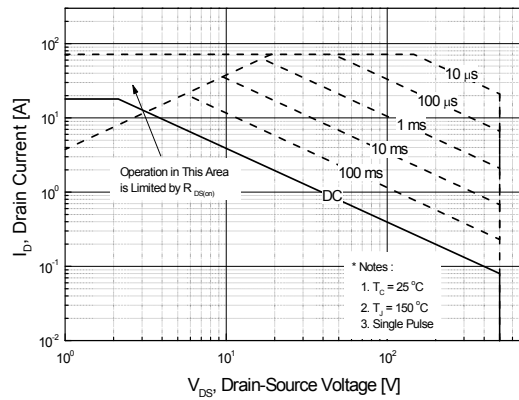
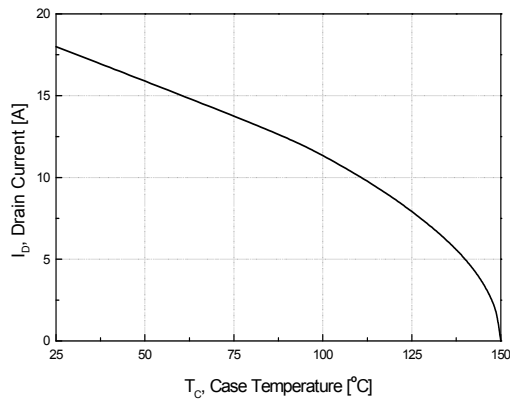


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve - FDP18N50

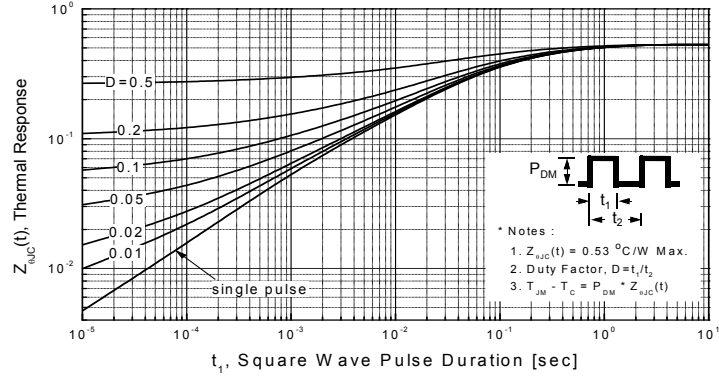
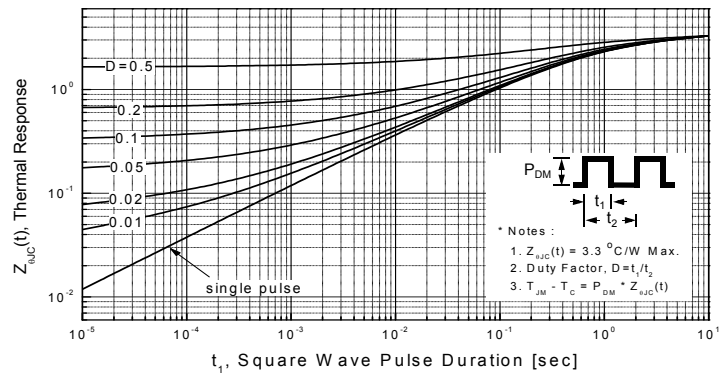
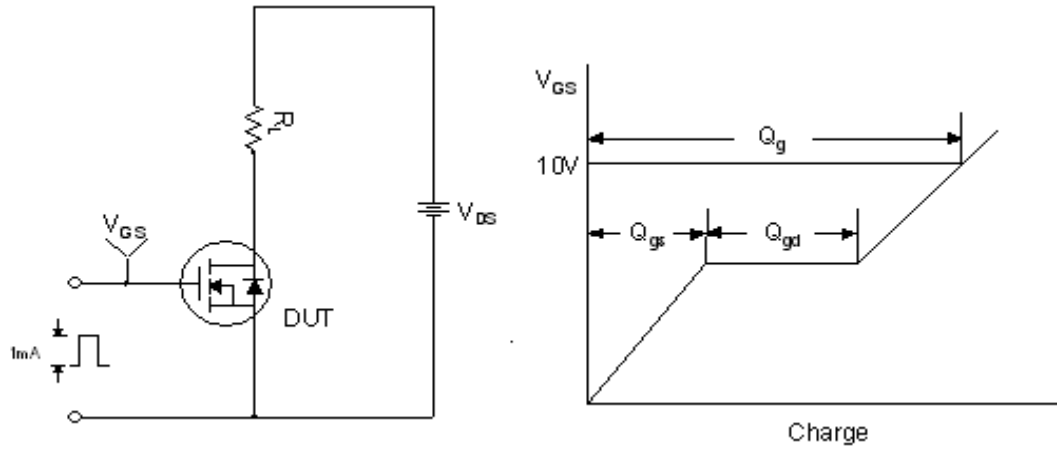


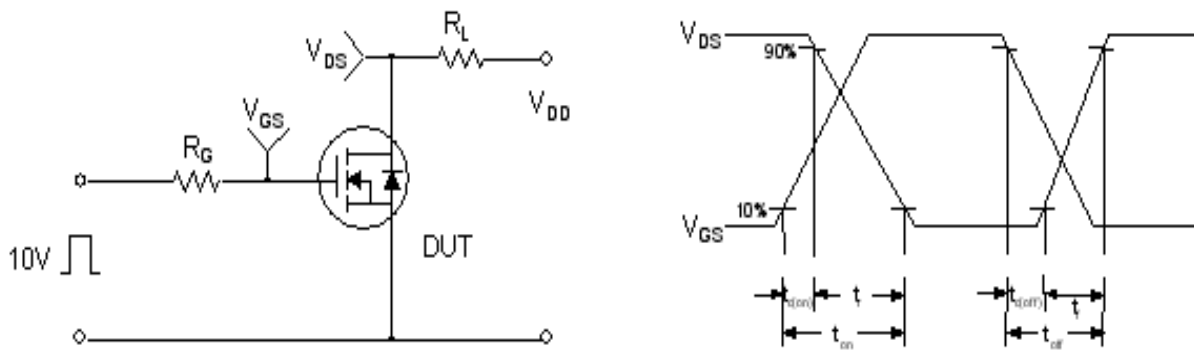
Figure 11-2. Transient Thermal Response Curve - FDPF18N50 / FDPF18N50T



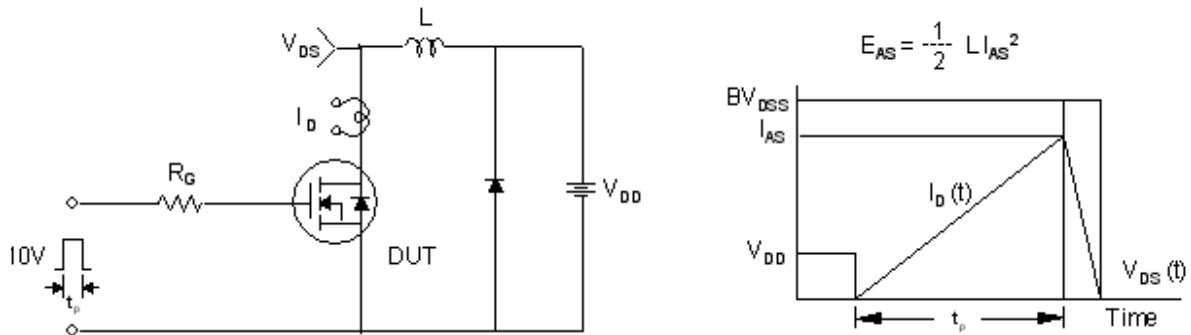
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

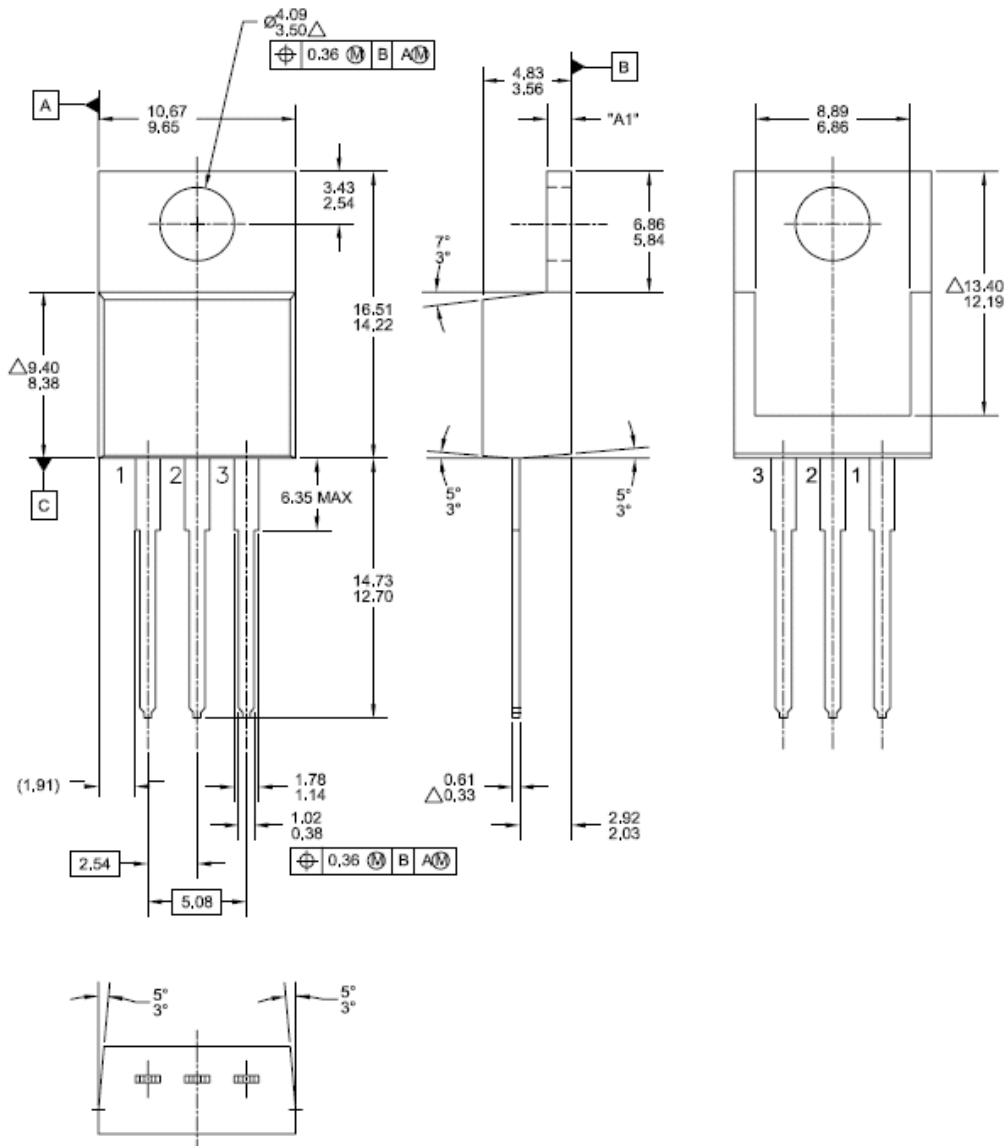


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-220

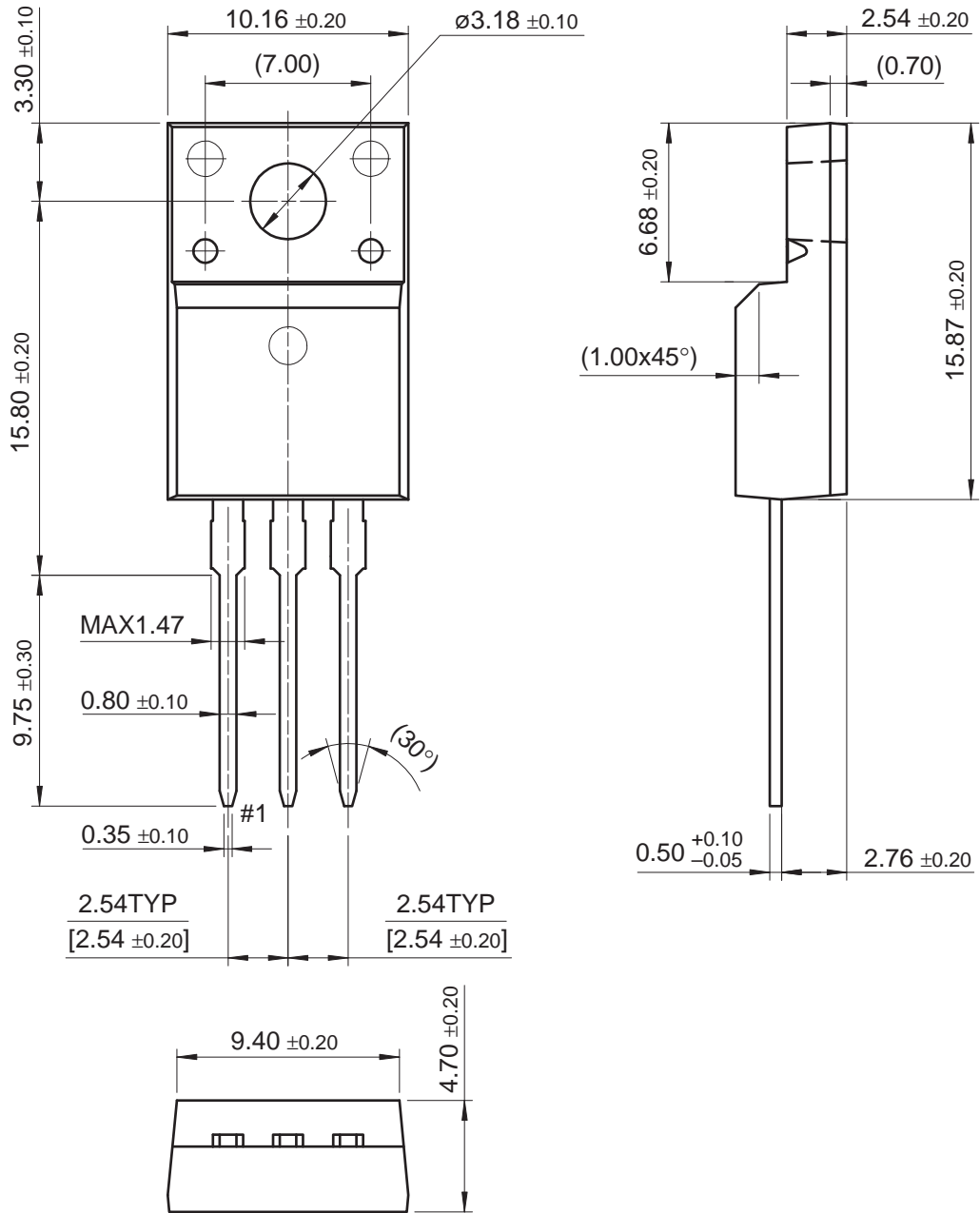


Dimensions in Millimeters

FDP18N50 / FDPF18N50 / FDPF18N50T 500V N-Channel MOSFET

Mechanical Dimensions

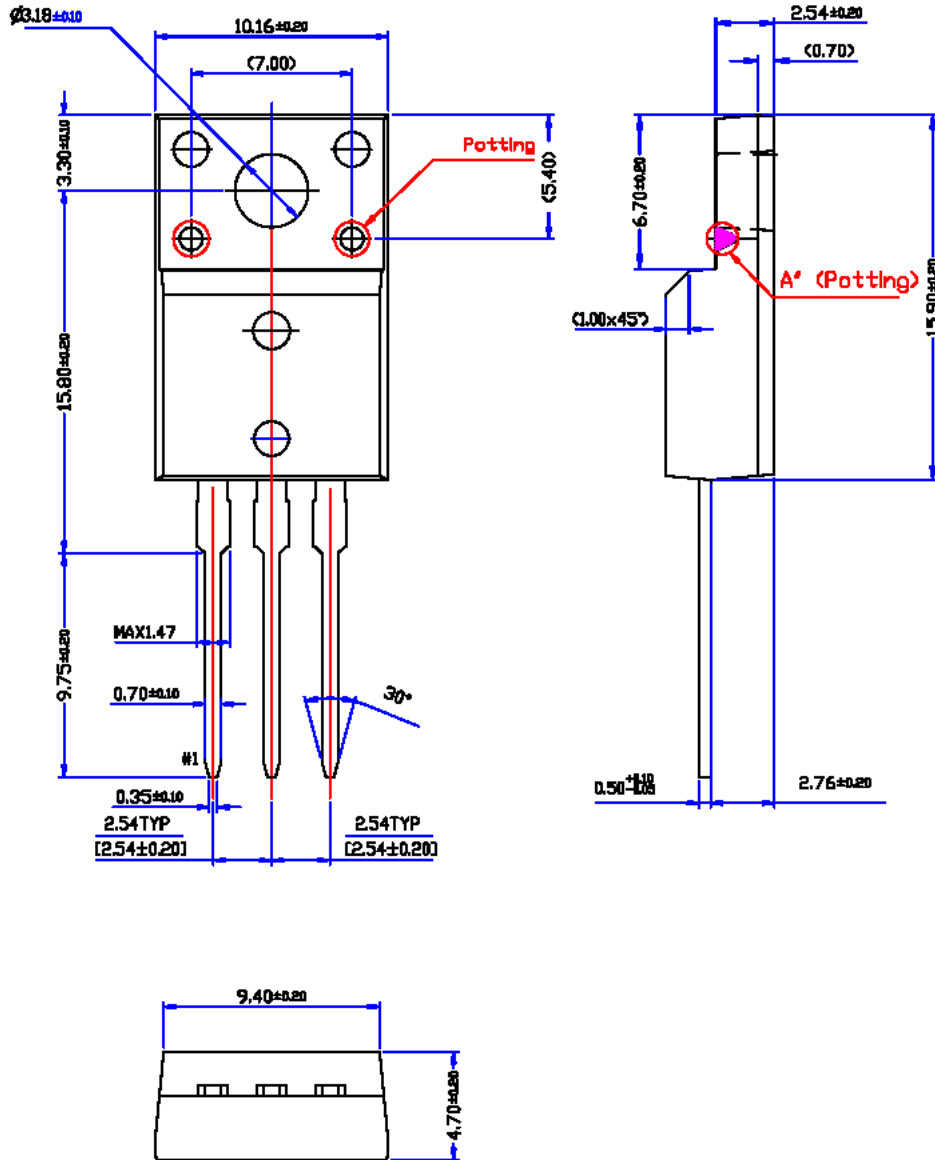
TO-220F



Dimensions in Millimeters

Package Dimensions

TO-220F Potted








* Front/Back Side Isolation Voltage : AC 2500V

Dimensions in Millimeters



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