Freescale Semiconductor
Advance Information

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MAC7100 Microcontroller Family Hardware Specifications

Covers MAC7101, MAC7106, MAC7111, MAC7116, MAC7121, MAC7126, MAC7131, MAC7136, MAC7141[1]

32-bit Embedded Controller Division

1. With preliminary information on MAC7112, MAC7122, MAC7142 devices.

This document provides electrical specifications, pin assignments, and package diagrams for MAC7100 family of microcontroller devices. For functional characteristics, refer to the *MAC7100 Microcontroller Family Reference Manual* (MAC7100RM).

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1 Overview

The MAC7100 Family of microcontrollers (MCUs) are members of a pin-compatible family of 32-bit Flash-memory-based devices developed specifically for embedded automotive applications. The pin-compatible family concept enables users to select between different memory and peripheral options for scalable designs. All MAC7100 Family members are composed of a 32-bit ARM7TDMI-S™ central processing unit, up to 1 Mbyte of embedded Flash EEPROM for program storage, up to 32 Kbytes of embedded Flash for data and/or program storage, and up to 48 Kbytes of RAM. The family is implemented with an enhanced DMA (eDMA) controller to improve performance for transfers between memory and many of the on-chip peripherals. The peripheral set includes asynchronous serial communications interfaces (eSCI), serial peripheral interfaces (DSPI),

inter-integrated circuit (I^2C™) bus controllers, FlexCAN interfaces, an enhanced modular I/O subsystem (eMIOS), 10-bit analog-to-digital converter (ATD) module(s), general-purpose timers (PIT) and two special-purpose timers (RTI and SWT). The peripherals share a large number of general purpose input-output (GPIO) pins, all of which are bidirectional and available with interrupt capability to trigger wake-up from low-power chip modes. Refer to Table 2 for a comparison of family members and availability of peripheral modules on each device.

The use of a PLL allows power drain and performance to be balanced to best fit requirements. The operating frequency of devices in the family is up to a maximum of 50 MHz. The internal data paths between the CPU core, eDMA, memory and peripherals are all 32 bits wide, further improving performance for 32-bit applications. The MAC7111, MAC7116, MAC7131 and MAC7136 also offer a 16-bit wide external data bus with 22 address lines. The family of devices is capable of operating over a junction temperature range of –40° C to 150° C.

2 Ordering Information

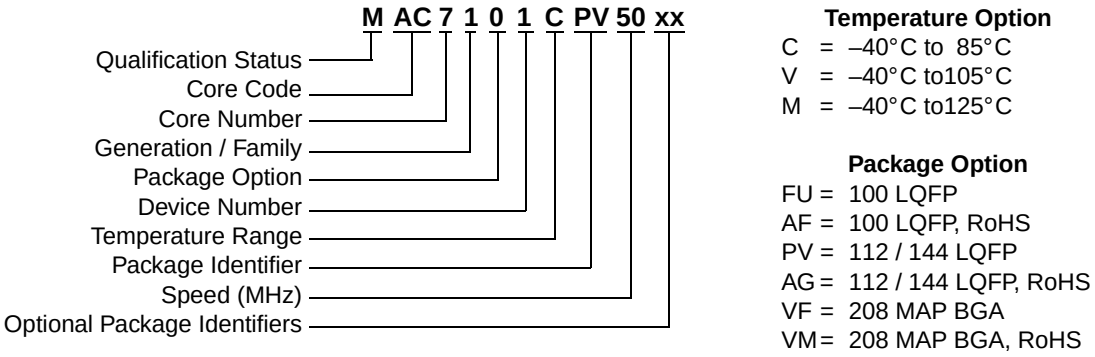


Figure 1. Order Part Number Example

The mask set of a device is marked with a four-character code consisting of a letter, two numerical digits, and a letter, for example L49P. Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code, for example 0L49P.

Table 1. MAC7100 Family Mask Set to Part Number Correspondence

Mask Set	Status	Part Number(s)
0L49P	Engineering samples	PAC7101, PAC7111, PAC7121, PAC7131, PAC7141
1L49P	Limited production, pre-qualification	PAC7101, PAC7111, PAC7121, PAC7131, PAC7141
0L47W	Limited production, pre-qualification	PAC7101, PAC7111, PAC7121, PAC7131, PAC7141
1L47W	Fully-qualified, production	MAC7101, MAC7111, MAC7121, MAC7131, MAC7141
0L61W	Engineering samples	PAC7112, PAC7122, PAC7142
0L38Y	Engineering samples	PAC7106, PAC7116, PAC7126, PAC7136
1L38Y	Fully-qualified, production	MAC7106, MAC7116, MAC7126, MAC7136

Table 2. MAC7100 Family Device Derivatives

Module Options		MAC7101	MAC7111	MAC7121	MAC7131	MAC7141	MAC7112	MAC7122	MAC7142	MAC7106	MAC7116	MAC7126	MAC7136
Program Flash		512 KBytes					256 KBytes			1 MByte			
Data Flash		32 KBytes											
SRAM		32 KBytes					16 KBytes			48 KBytes			
External Bus		—	Yes	—	Yes	—	—	—	—	—	Yes	—	Yes
ATD Modules [1]	A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	B	Yes	—	—	Yes	—	—	—	—	Yes	—	—	Yes
CAN Modules	A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	C	Yes	Yes	Yes	Yes	—	—	—	—	Yes	Yes	Yes	Yes
	D	Yes	Yes	Yes	Yes	—	—	—	—	Yes	Yes	Yes	Yes
eSCI Modules	A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	C	Yes	Yes	Yes	Yes	—	Yes	Yes	—	Yes	Yes	Yes	Yes
	D	Yes	Yes	Yes	Yes	Yes	—	—	—	Yes	Yes	Yes	Yes
DSPI Modules	A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes [2]
	B	Yes	Yes	Yes [3]	Yes	Yes	Yes	Yes [3]	Yes	Yes	Yes	Yes [3]	Yes [2]
I^2C Module		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
eMIOS Module		16 channels, 16-bit											
Timer Module		10 channels, 24-bit											
General-Purpose I/O Ports/Pins	A	10	16	10	16	4	16	10	4	10	16	10	16
	B	16	16	15	16	16	16	15	16	16	16	15	16
	C	12	16	1	16	—	16	1	—	12	16	1	16
	D	10 [4]	16 [4]	11 [4]	16 [4]	10 [4]	16	11	10	10	16	11	16
	E	16	16	16	16	16	16	16	16	16	16	16	16
	F	16	16	16	16	16	16	16	16	16	16	16	16
	G	16	16	16	16	10	16	16	10	16	16	16	16
	H	16	—	—	16	—	—	—	—	16	—	—	16
	I	—	—	—	—	—	—	—	—	—	—	—	16
Total (max.)		112 [4]	112 [4]	85 [4]	128 [4]	72 [4]	112	85	72	112	112	85	144
Package		144 LQFP	144 LQFP	112 LQFP	208 BGA	100 LQFP	144 LQFP	112 LQFP	100 LQFP	144 LQFP	144 LQFP	112 LQFP	208 BGA

NOTES:
1. 16 channels, 8/10-bit, per module.
2. Four additional chip selects available.
3. PB11 / PCS2_B not available on non-L49P-mask devices; PB10 / PCS5_B / $\overline{\text{PCSS\_B}}$ not available on mask L47W devices.
4. Reduce these values by one for mask set L49P devices (PD2 is not available for general-purpose use).

3 Electrical Characteristics

This section contains electrical information for MAC7100 Family microcontrollers. The information is preliminary and subject to change without notice.

MAC7100 Family devices are specified and tested over the 5 V and 3.3 V ranges. For operation at any voltage within that range, the 3.3 V specifications generally apply. However, no production testing is done to verify operation at intermediate supply voltage levels.

3.1 Parameter Classification

The electrical parameters shown in this appendix are derived by various methods. To provide a better understanding to the designer, the following classification is used. Parameters are tagged accordingly in the column labeled “C” of the parametric tables, as appropriate.

Table 3. Parametric Value Classification

P	Parameters guaranteed during production testing on each individual device.
C	Parameters derived by the design characterization and by measuring a statistically relevant sample size across process variations.
T	Parameters derived by design characterization on a small sample size from typical devices under typical conditions (unless otherwise noted). All values shown in the typical column are within this classification, even if not so tagged.
D	Parameters derived mainly from simulations.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. Functional operation outside these maximums is not guaranteed. Stress beyond these limits may affect reliability or cause permanent damage to the device.

MAC7100 Family devices contain circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either $V_{SS}5$[1] or $V_{DD}5$[1]).

Table 4. Absolute Maximum Ratings

Num	Rating	Symbol	Min	Max	Unit
A1a	I/O Drivers Supply Voltage	$V_{DD}X$	–0.3	+6.0	V
A2	Digital Logic Supply Voltage [1]	$V_{DD}2.5$	–0.3	+3.0	V
A3	PLL Supply Voltage [1]	$V_{DD}PLL$	–0.3	+3.0	V
A4	Analog Supply Voltage	$V_{DD}A$	–0.3	+6.0	V
A5	Analog Reference	$V_{RH,}$ V_{RL}	–0.3	+6.0	V
A6	Voltage difference $V_{DD}X$ to $V_{DD}A$	Δ_{VDDX}	–0.3	+0.3	V
A7	Voltage difference $V_{SS}X$ to $V_{SS}A$	Δ_{VSSX}	–0.3	+0.3	V
A8	Voltage difference $V_{RH} – V_{RL}$	$V_{RH} – V_{RL}$	–0.3	+6.0	V

1. Refer to Section 3.7, “Power Supply,” for definition of $V_{SS}5$ and $V_{DD}5$.

Table 4. Absolute Maximum Ratings (continued)

Num	Rating	Symbol	Min	Max	Unit
A9	Voltage difference $V_{DD}A - V_{RH}$	$V_{DD}A - V_{RH}$	–0.3	+6.0	V
A10	Digital I/O Input Voltage	V_{IN}	–0.3	+6.0	V
A11	XFC, EXTAL, XTAL inputs	V_{ILV}	–0.3	+3.0	V
A12	TEST input	V_{TEST}	–0.3	— [2]	V
	Instantaneous Maximum Current [3]				
A13	Single pin limit for XFC, EXTAL, XTAL [4]	I_{DL}	–25	+25	mA
A14	Single pin limit for all digital I/O pins [5]	I_D	–25	+25	mA
A15	Single pin limit for all analog input pins [5]	I_{DA}	–25	+25	mA
A16	Single pin limit for TEST [2]	I_{DT}	–0.25	0	mA
A17	Storage Temperature Range	T_{stg}	–65	+155	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply from the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
2. This pin is clamped low to $V_{SS}X$, but not clamped high, and must be tied low in applications.
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, use the larger of the calculated values using $V_{POSCLAMP} = V_{DD}A + 0.3V$ and $V_{NEGCLAMP} = –0.3$ V.
4. These pins are internally clamped to V_{SS}PLL and V_{DD}PLL.
5. All I/O pins are internally clamped to $V_{SS}X$ and $V_{DD}X$, $V_{SS}R$ and $V_{DD}R$ or $V_{SS}A$ and $V_{DD}A$.

3.3 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulses per pin positive negative	—	— 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	—	— 3 3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
B1	C	Human Body Model (HBM)	V_{HBM}	2000	—	V
B2	C	Machine Model (MM)	V_{MM}	200	—	V
B3	C	Charge Device Model (CDM)	V_{CDM}	500	—	V
B4	C	Latch-up Current at T_A = 125°C positive negative	I_{LAT}	 +100 –100	—	mA
B5	C	Latch-up Current at T_A = 27°C positive negative	I_{LAT}	 +200 –200	—	mA

3.4 Operating Conditions

Unless otherwise noted, the following conditions apply to all parametric data. Refer to the temperature rating of the device (C, V, M) with respect to ambient temperature (T_A) and junction temperature (T_J). For power dissipation calculations refer to Section 3.6, “Power Dissipation and Thermal Characteristics.”

Table 7. MAC7100 Family Device Operating Conditions

Num	Rating		Symbol	Min	Typ	Max	Unit
C1	I/O Drivers Supply Voltage		$V_{DD}X$	3.15	5	5.5	V
C2	Digital Logic Supply Voltage [1]		$V_{DD}2.5$	2.35	2.5	2.75	V
C3	PLL Supply Voltage [1]		$V_{DD}PLL$	2.35	2.5	2.75	V
C4	Analog Supply Voltage		$V_{DD}A$	3.15	5	5.5	V
C5	Voltage Difference $V_{DD}X$ to $V_{DD}A$		$\Delta_{VDD}X$	–0.1	0	0.1	V
C6	Voltage Difference $V_{SS}X$ to $V_{SS}A$		$\Delta_{VSS}X$	–0.1	0	0.1	V
C7	Oscillator Frequency		f_{OSC} [2]	0.5	—	16	MHz
C8	System Clock Frequency		f_{SYS} [2]	0.5	—	50	MHz
C9a	MAC71xxC	Operating Junction Temperature Range [3]	T_J	–40	—	110	°C
C9b		Operating Ambient Temperature Range [3]	T_A	–40	25	85	°C
C10a	MAC71xxV	Operating Junction Temperature Range [3]	T_J	–40	—	130	°C
C10b		Operating Ambient Temperature Range [3]	T_A	–40	25	105	°C
C11a	MAC71xxM	Operating Junction Temperature Range [3]	T_J	–40	—	150	°C
C11b		Operating Ambient Temperature Range [3]	T_A	–40	25	125	°C

NOTES:
1. These ratings apply only when the VREG is disabled and the device is powered from an external source.
2. Throughout this document, t_{OSC} refers to 1 ÷ f_{OSC}, and t_{SYS} refers to 1 ÷ f_{SYS}.
3. Refer to Section 3.6, “Power Dissipation and Thermal Characteristics,” for more details about the relation between ambient temperature T_A and device junction temperature T_J.

3.4.1 Input/Output Pins

The I/O pins operate at a nominal level of 3.3 V to 5 V. This class of pins is comprised of the clocks, control and general purpose/peripheral pins. The internal structure of these pins is identical; however, some functionality may be disabled (for example, for analog inputs the output drivers, pull-up/down resistors are permanently disabled).

3.4.2 Oscillator Pins

The pins XFC, EXTAL, XTAL are dedicated to the oscillator and operate at a nominal level of 2.5V.

3.5 Input/Output Characteristics

This section describes the characteristics of all I/O pins in both 3.3 V and 5 V operating conditions. All parameters are not always applicable; for example, not all pins feature pull up/down resistances.

Table 8. 5.0 V I/O Characteristics

Conditions shown in Table 7 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
D1a	P	Input High Voltage	V_{IH}	0.65 × $V_{DD}5$ [1]	—	—	V
D1b	T	Input High Voltage	V_{IH}	—	—	$V_{DD}5$ + 0.3 [1]	V
D2a	P	Input Low Voltage	V_{IL}	—	—	0.35 × $V_{DD}5$ [1]	V
D2b	T	Input Low Voltage	V_{IL}	$V_{SS}5$ – 0.3 [1]	—	—	V
D3	C	Input Hysteresis	V_{HYS}	—	250	—	mV
D4	P	Input Leakage Current (pins in high impedance input mode) V_{in} = $V_{DD}5$ or $V_{SS}5$ [1]	I_{in}	–1 [2]	—	1 [2]	µA
D5	P	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –2mA Full Drive I_{OH} = –10mA	V_{OH}	$V_{DD}5$ – 0.8	—	—	V
D6	P	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +2mA Full Drive I_{OL} = +10mA	V_{OL}	—	—	0.8	V
D7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	—	—	–130	µA
D8	P	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	–10	—	—	µA
D9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	—	—	130	µA
D10	P	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	—	—	µA
D11	D	Input Capacitance	C_{in}	—	6	—	pF
D12	T	Injection current [3] Single Pin limit Total Device Limit. Sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	mA
D13	P	Port Interrupt Input Pulse filtered [4]	t_{PULSE}	—	—	3	µs
D14	P	Port Interrupt Input Pulse passed [4]	t_{PULSE}	10	—	—	µs

NOTES:
1. Refer to Section 3.7, “Power Supply,” for definition of $V_{SS}5$ and $V_{DD}5$.
2. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8℃ to 12℃ in the temperature range from 50℃ to 125℃.
3. Refer to Section 3.7.1, “Current Injection,” for more details
4. Parameter only applies in STOP or Pseudo STOP mode.

Table 9. 3.3 V I/O Characteristics

Conditions shown in Table 7, with $V_{DD}X$ = 3.3 V –5%/+10% and a temperature maximum of +140°C unless otherwise noted.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
E1a	P	Input High Voltage	V_{IH}	0.65 × $V_{DD}5$ [1]	—	—	V
E1b	T	Input High Voltage	V_{IH}	—	—	$V_{DD}5$ + 0.3 [1]	V
E2a	P	Input Low Voltage	V_{IL}	—	—	0.35 × $V_{DD}5$ [1]	V
E2b	T	Input Low Voltage	V_{IL}	$V_{SS}5$ – 0.3 [1]	—	—	V
E3	C	Input Hysteresis	V_{HYS}	—	250	—	mV
E4	P	Input Leakage Current (pins in high impedance input mode) V_{in} = $V_{DD}5$ or $V_{SS}5$ [1]	I_{in}	–1 [2]	—	1 [2]	µA
E5	P	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –0.75mA Full Drive I_{OH} = –4.5mA	V_{OH}	$V_{DD}5$ – 0.4	—	—	V
E6	P	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +0.9mA Full Drive I_{OL} = +5.5mA	V_{OL}	—	—	0.4	V
E7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	—	—	–60	µA
E8	P	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	–6	—	—	µA
E9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	—	—	60	µA
E10	P	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	6	—	—	µA
E11	D	Input Capacitance	C_{in}	—	6	—	pF
E12	T	Injection current [3] Single Pin limit Total Device Limit. Sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	mA
E13	P	Port Interrupt Input Pulse filtered [4]	t_{PULSE}	—	—	3	µs
E14	P	Port Interrupt Input Pulse passed [4]	t_{PULSE}	10	—	—	µs

NOTES:
1. Refer to Section 3.7, “Power Supply,” for definition of $V_{SS}5$ and $V_{DD}5$.
2. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8℃ to 12℃ in the temperature range from 50℃ to 125℃.
3. Refer to Section 3.7.1, “Current Injection,” for more details
4. Parameter only applies in STOP or Pseudo STOP mode.

3.6 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded.

Note that the JEDEC specification reserves the symbol $R_{\theta JA}$ or θ_{JA} (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. $R_{\theta JMA}$ or θ_{JMA} (Theta-JMA) will be used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, θ_{JA}, will continue to be commonly used.

The average chip-junction temperature (T_J) in °C is obtained from the formula:

$$T_J = T_A + P_D \cdot \Theta_{JA} \quad \textit{Eqn. 1}$$

where

T_J = Junction Temperature (◦C)
T_A = Ambient Temperature (◦C)
P_D = Total Chip Power Dissipation (W)
Θ_{JA} = Package Thermal Resistance (◦C/W)

The total power dissipation is calculated as:

$$P_D = P_{INT} + P_{IO} \quad \textit{Eqn. 2}$$

where

P_{INT} = Chip Internal Power Dissipation (W)
P_{IO} = Input / Output Power Dissipation (W)

Two cases must be considered for P_{INT}:

1. Internal voltage regulator enabled:

$$P_{INT} = (I_{DD}R \times V_{DD}R) + (I_{DD}A \times V_{DD}A) \quad \textit{Eqn. 3}$$

2. Internal voltage regulator disabled ($V_{DD}R = V_{SS}R$ = system ground):

$$P_{INT} = (I_{DD}2.5 \times V_{DD}2.5) + (I_{DD}PLL \times V_{DD}PLL) + (I_{DD}A \times V_{DD}A) \quad \textit{Eqn. 4}$$

P_{IO} is the sum of all output currents on input/output pins associated with $V_{DD}X$:

$$P_{IO} = \sum_i R_{DSON} \cdot (I_{IO_i})^2 \quad \textit{Eqn. 5}$$

where

$$R_{DSON} = \frac{V_{OL}}{I_{OL}} \text{ (for outputs driven low)} \quad \textit{Eqn. 6}$$

or

$$R_{DSON} = \frac{V_{DD}X - V_{OH}}{I_{OL}} \text{ (for outputs driven high)} \quad \textit{Eqn. 7}$$

Table 10. Thermal Resistance 1/8 Simulation Model Packaging Parameters

Component	Conductivity
Mold Compound	0.9 W/m K
Leadframe (Copper)	263 W/m K
Die Attach	1.7 W/m K

3.6.1 Thermal Resistance Simulation Details

Table 11. Thermal Resistance for Case Outline 983–02, 100 Lead 14x14 mm LQFP, 0.5 mm Pitch

Rating	Environment	Symbol	Value	Unit	Comments
Junction to Ambient (Natural Convection)	Single layer board (1s)	$R_{\theta JA}$	44	℃/W	1, 2
Junction to Ambient (Natural Convection)	Four layer board (2s2p)	$R_{\theta JMA}$	34	℃/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Single layer board (1s)	$R_{\theta JMA}$	37	℃/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Four layer board (2s2p)	$R_{\theta JMA}$	29	℃/W	1, 3
Junction to Board		$R_{\theta JB}$	18	℃/W	4
Junction to Case		$R_{\theta JC}$	7	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

Table 12. Thermal Resistance for Case Outline 987–01, 112 Lead 20x20 mm LQFP, 0.65 mm Pitch

Rating	Environment	Symbol	Value	Unit	Comments
Junction to Ambient (Natural Convection)	Single layer board (1s)	$R_{\theta JA}$	42	℃/W	1, 2
Junction to Ambient (Natural Convection)	Four layer board (2s2p)	$R_{\theta JMA}$	34	℃/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Single layer board (1s)	$R_{\theta JMA}$	35	℃/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Four layer board (2s2p)	$R_{\theta JMA}$	30	℃/W	1, 3
Junction to Board		$R_{\theta JB}$	22	℃/W	4
Junction to Case		$R_{\theta JC}$	7	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

Table 13. Thermal Resistance for Case Outline 918–03, 144 Lead 20x20 mm LQFP, 0.5 mm Pitch

Rating	Environment	Symbol	Value	Unit	Comments
Junction to Ambient (Natural Convection)	Single layer board (1s)	$R_{\theta JA}$	42	℃/W	1, 2
Junction to Ambient (Natural Convection)	Four layer board (2s2p)	$R_{\theta JMA}$	34	℃/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Single layer board (1s)	$R_{\theta JMA}$	35	℃/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Four layer board (2s2p)	$R_{\theta JMA}$	30	℃/W	1, 3
Junction to Board		$R_{\theta JB}$	22	℃/W	4
Junction to Case		$R_{\theta JC}$	7	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

Table 14. Thermal Resistance for Case Outline 1159A-01, 208 Lead 17x17 mm MAP BGA, 1.0 mm Pitch

Rating	Environment	Symbol	Value	Unit	Comments
Junction to Ambient (Natural Convection)	Single layer board (1s)	$R_{\theta JA}$	46	℃/W	1, 2
Junction to Ambient (Natural Convection)	Four layer board (2s2p)	$R_{\theta JMA}$	29	℃/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Single layer board (1s)	$R_{\theta JMA}$	38	℃/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Four layer board (2s2p)	$R_{\theta JMA}$	26	℃/W	1, 3
Junction to Board		$R_{\theta JB}$	19	℃/W	4
Junction to Case		$R_{\theta JC}$	7	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

Comments:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board at the center lead. For fused lead packages, the adjacent lead is used.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.7 Power Supply

The MAC71xx Family utilizes several pins to supply power to the oscillator, PLL, digital core, I/O ports and ATD. In the context of this section, $V_{DD}5$ is used for $V_{DD}A$, $V_{DD}R$ or $V_{DD}X$; $V_{SS}5$ is used for $V_{SS}A$, $V_{SS}R$ or $V_{SS}X$ unless otherwise noted. $I_{DD}5$ denotes the sum of the currents flowing into the $V_{DD}A$, $V_{DD}X$, and $V_{DD}R$. V_{DD} is used for $V_{DD}2.5$, and $V_{DD}PLL$, V_{SS} is used for $V_{SS}2.5$ and $V_{SS}PLL$. I_{DD} is used for the sum of the currents flowing into $V_{DD}2.5$ and $V_{DD}PLL$.

3.7.1 Current Injection

The power supply must maintain regulation within the $V_{DD}5$ or $V_{DD}2.5$ operating range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}5$) is greater than $I_{DD}5$, the injection current may flow out of $V_{DD}5$ and could result in the external power supply going out of regulation. It is important to ensure that the external $V_{DD}5$ load will shunt current greater than the maximum injection current. The greatest risk will be when the MCU is consuming very little power (for example, if no system clock is present, or if the clock rate is very low).

3.7.2 Power Supply Pins

The $V_{DD}R - V_{SS}R$ pair supplies the internal voltage regulator. The $V_{DD}A - V_{SS}A$ pair supplies the A/D converter and the reference circuit of the internal voltage regulator. The $V_{DD}X - V_{SS}X$ pair supplies the I/O pins. $V_{DD}PLL - V_{SS}PLL$ pair supplies the oscillator and PLL.

All $V_{DD}X$ pins are internally connected by metal. All $V_{SS}X$ pins are internally connected by metal. All $V_{SS}2.5$ pins are internally connected by metal. $V_{DD}A$, $V_{DD}X$ and $V_{DD}R$ as well as $V_{SS}A$, $V_{SS}X$ and $V_{SS}R$ are connected by anti-parallel diodes for ESD protection.

3.7.3 Supply Current Characteristics

Table 15 and Table 16 list supply current characteristics for MAC71*x*1 and MAC71*x*6 devices at 40 MHz and 50 MHz operation, respectively. Characteristics for MAC71*x*2 devices are to be determined (TBD).

All current measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled at the specified system frequency, using a 4 MHz oscillator in low power mode. Production testing is performed using a square wave signal at the EXTAL input. In expanded modes, the currents are highly dependent on the load and duty cycle on the address, data and control signals, thus no general numbers can be given. A good estimate is to take the single chip currents and add the currents due to the external loads.

Table 15. MAC71*x*1/6 [1] Device Supply Current Characteristics – 40 MHz

Conditions shown in Table 7, with f_{SYS} = 40 MHz.							
Num	**C**	**Rating**		**Symbol**	**Typ**	**Max**	**Unit**
F1	P	Run Supply Current, Single Chip		$I_{DD}R_{reg}$	100	130	mA
F2	C	Doze Supply Current		$I_{DD}D_{reg}$	Run ≥ Doze ≥ Pseudo Stop		
F3	P	Pseudo Stop Supply Current (OSC on)	–40° C [2]	$I_{DD}PS_{reg}$	400 / 500 [3]	600 / 700 [3]	µA
	P		25° C [2]		400 / 500 [3]	600 / 700 [3]	µA
	C		85° C [2]		800 / 1000 [3]	2000 / 2500 [3]	µA
	C		105° C [2]		1200 / 1500 [3]	3500 / 4000 [3]	µA
	P		125° C [2]		1500 / 2000 [3]	5500 / 6000 [3]	µA
F4	P	Stop Supply Current ($T_J = T_A$ assumed)	–40° C [2]	$I_{DD}S_{reg}$	30	150	µA
	P		25° C [2]		30	150	µA
	C		85° C [2]		330	2500	µA
	C		105° C [2]		470	3500	µA
	P		125° C [2]		660	5000	µA

NOTES:
1. MAC71*x*2 characteristics are to be determined (TBD).
2. 85°C, 105°C, and 125°C refer to the "C", "V", and "M" Temperature Options, respectively.
3. RTI disabled / enabled.

Table 16. MAC71*x*1/6 [1] Device Supply Current Characteristics – 50 MHz

Conditions shown in Table 7, with f_{SYS} = 50 MHz.							
Num	**C**	**Rating**		**Symbol**	**Typ**	**Max**	**Unit**
G1	P	Run Supply Current, Single Chip		$I_{DD}R_{reg}$	120	150	mA
G2	C	Doze Supply Current		$I_{DD}D_{reg}$	Run ≥ Doze ≥ Pseudo Stop		
G3	P	Pseudo Stop Supply Current (OSC on)	–40° C [2]	$I_{DD}PS_{reg}$	400 / 500 [3]	600 / 700 [3]	µA
	P		25° C [2]		400 / 500 [3]	600 / 700 [3]	µA
	C		85° C [2]		800 / 1000 [3]	2000 / 2500 [3]	µA
	C		105° C [2]		1200 / 1500 [3]	3500 / 4000 [3]	µA
	P		125° C [2]		1500 / 2000 [3]	5500 / 6000 [3]	µA
G4	P	Stop Supply Current ($T_J = T_A$ assumed)	–40° C [2]	$I_{DD}S_{reg}$	30	150	µA
	P		25° C [2]		30	150	µA
	C		85° C [2]		330	2500	µA
	C		105° C [2]		470	3500	µA
	P		125° C [2]		660	5000	µA

NOTES:
1. MAC71*x*2 characteristics are to be determined (TBD).
2. 85°C, 105°C, and 125°C refer to the "C", "V", and "M" Temperature Options, respectively.
3. RTI disabled / enabled.

3.7.4 Voltage Regulator Characteristics

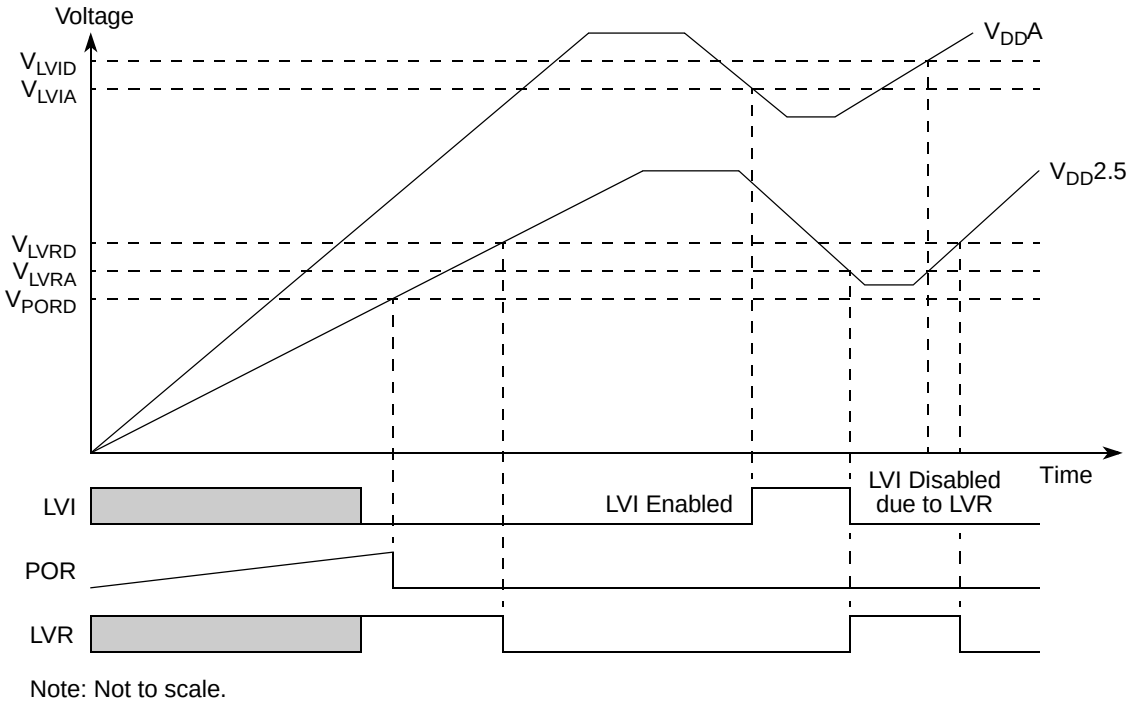
Table 17. VREG Operating Conditions

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
H1	P	Input Voltages	V_{VDDRA}	3.15	—	5.5	V
H2	P	Output Voltage, Digital Logic Full Performance Mode Reduced Power Mode Shutdown Mode	$V_{DD}2.5$	 2.45 1.60 — [1]	 2.5 2.5 — [1]	 2.75 2.75 — [1]	 V V V
H3	P	Output Voltage, PLL Full Performance Mode Reduced Power Mode [2] Reduced Power Mode [3] Shutdown Mode	$V_{DD}PLL$	 2.35 2.00 1.60 — [1]	 2.5 2.5 2.5 — [1]	 2.75 2.75 2.75 — [1]	 V V V V
H4	P	Low Voltage Interrupt [4] Assert Level Negate Level	 V_{LVIA} V_{LVID}	 4.10 4.25	 4.37 4.52	 4.66 4.77	 V V
H5	P	Low Voltage Reset [5] Assert Level	 V_{LVRA}	 2.25	 2.35	 —	 V
H6	P	Power On Reset [6] Assert Level Negate Level	 V_{PORA} V_{PORD}	 0.97 —	 — —	 — 2.05	 V V

NOTES:
1. High impedance output.
2. Current $I_{DD}PLL$ = 1 mA (Low Power Oscillator).
3. Current $I_{DD}PLL$ = 3 mA (Standard Oscillator).
4. Monitors $V_{DD}A$, active only in full performance mode. This interrupt indicates that I/O and ATD performance may be degraded due to low supply voltage.
5. Monitors $V_{DD}2.5$, active only in full performance mode. Only POR is active in reduced performance mode.
6. Monitors $V_{DD}2.5$, active in all modes.

3.7.5 Chip Power Up and Voltage Drops

The VREG sub-modules LVI (low voltage interrupt), POR (power on reset) and LVR (low voltage reset) handle chip power-up or drops of the supply voltage. Refer to Figure 2.



Note: Not to scale.

Figure 2. VREG Chip Power-up and Voltage Monitoring

3.7.6 Output Loads

The on-chip voltage regulator is intended to supply the internal logic and oscillator circuits. No external DC load is allowed. Capacitive loads are specified in Table 18. Capacitors with X7R dielectricum are required.

Table 18. VREG Recommended Load Capacitances

Rating	Symbol	Min	Typ	Max	Unit
Load Capacitance per V_{DD}2.5 pin [1]	C_{LVDD}	200	220	12000	nF
Load Capacitance on V_{DD}PLL pin	$C_{LVDDfcPLL}$	90	220	5000	nF

NOTES:
1. Refer to Table 38 for the specific number of V_{DD}2.5 pins on various packages. Each V_{DD}2.5 pin should have the recommended loading as described in Section 3.7.3, “Circuit Board Layout,” of the *MAC7100 Microcontroller Family Reference Manual* (MAC7100RM).

3.8 Clock and Reset Generator

This section describes the electrical characteristics for the oscillator, phase-locked loop, clock monitor and reset generator.

3.8.1 Oscillator Characteristics

The MAC7100 Family features an internal low power loop controlled Pierce oscillator and a full swing Pierce oscillator/external clock mode. The selection of loop controlled Pierce oscillator or full swing Pierce oscillator/external clock depends on the level of the $\overline{\text{XCLKS}}$ signal at the rising edge of the $\overline{\text{RESET}}$ signal. Before asserting the oscillator to the internal system clock distribution subsystem, the quality of the oscillation is checked for each start from either power on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Clock Monitor Assert Frequency f_{CMFA}.

Table 19. Oscillator Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
J1a	C	Crystal oscillator range (loop controlled Pierce)	f_{OSC} [1]	4.0	—	16	MHz
J1b	C	Crystal oscillator range (full swing Pierce) [2] [3]	f_{OSC} [1]	0.5	—	40	MHz
J2	P	Startup Current	I_{OSC}	100	—	—	μA
J3	C	Oscillator start-up time (loop controlled Pierce)	t_{UPOSC}	—	3 [4]	50 [5]	ms
J4	D	Clock Quality check time-out	t_{CQOUT}	0.45	—	2.5	s
J5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
J6	P	External square wave input frequency [3]	f_{EXT}	0.5	—	50	MHz
J7	D	External square wave pulse width low	t_{EXTL}	9.5	—	—	ns
J8	D	External square wave pulse width high	t_{EXTH}	9.5	—	—	ns
J9	D	External square wave rise time	t_{EXTR}	—	—	1	ns
J10	D	External square wave fall time	t_{EXTF}	—	—	1	ns
J11	D	Input Capacitance (EXTAL, XTAL pins)	C_{IN}	—	7	—	pF

NOTES:
1. If CLKSEL[PLLSEL] is clear then the system clock (f_{SYS}) is equal to f_{OSC}, otherwise it is equal to f_{VCO} (table Table 20, K3). Throughout this document, t_{SYS} is used to specify a unit of time equal to $1 \div f_{SYS}$.
2. Depending on the crystal; a damping series resistor might be necessary
3. $\overline{\text{XCLKS}}$ asserted (low) during reset
4. f_{OSC} = 4 MHz, C = 22 pF (refer to the *MAC7100 Microcontroller Family Reference Manual* (MAC7100RM) for circuit board layout recommendations, including oscillator capacitor placement and values).
5. Maximum value is for extreme cases using high Q, low frequency crystals

3.8.2 PLL Filter Characteristics

The oscillator provides the reference clock for the PLL as shown in Figure 3. The voltage controlled oscillator (VCO) of the PLL is also the system clock source in self clock mode. In order to operate reliably, care must be taken to select proper values for external loop filter components.

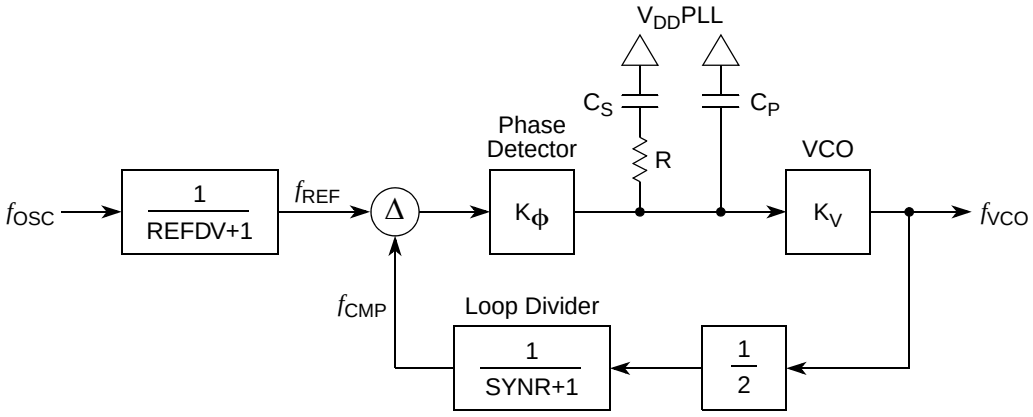


Figure 3. Basic PLL Functional Diagram

The procedure described below can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from Table 20. First, the VCO Gain at the desired VCO output frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{VCO})}{K_1 \cdot 1V}} \qquad \textit{Eqn. 8}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V \qquad \textit{Eqn. 9}$$

i_{ch} is the current in tracking mode. The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, a typical value for the stability factor is 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{REF}}{\pi \cdot (\zeta + \sqrt{1 + \zeta^2})} \frac{1}{10} \rightarrow f_C < \frac{f_{REF}}{4 \cdot 10}; (\zeta = 0.9) \qquad \textit{Eqn. 10}$$

And finally the frequency relationship is defined as:

$$n = \frac{f_{VCO}}{f_{REF}} = 2 \cdot (SYNR + 1) \qquad \textit{Eqn. 11}$$

With the above inputs the resistance can be calculated as:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} \qquad \textit{Eqn. 12}$$

The capacitance C_S can now be calculated as:

$$C_S = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) \qquad \textit{Eqn. 13}$$

The capacitance C_P should be chosen in the range of:

$$C_S \div 20 \leq C_P \leq C_S \div 10 \qquad \textit{Eqn. 14}$$

The stabilization delays shown in Table 20 are dependant on PLL operational settings and external component selection (for example, the crystal and XFC filter).

3.8.2.1 Jitter Information

With each transition of the clock f_{CMP}, the deviation from the reference clock f_{REF} is measured and input voltage to the VCO is adjusted accordingly. The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in Figure 4. It is important to note that the pre-scaler used by timers and serial modules will eliminate the effect of PLL jitter to a large extent.

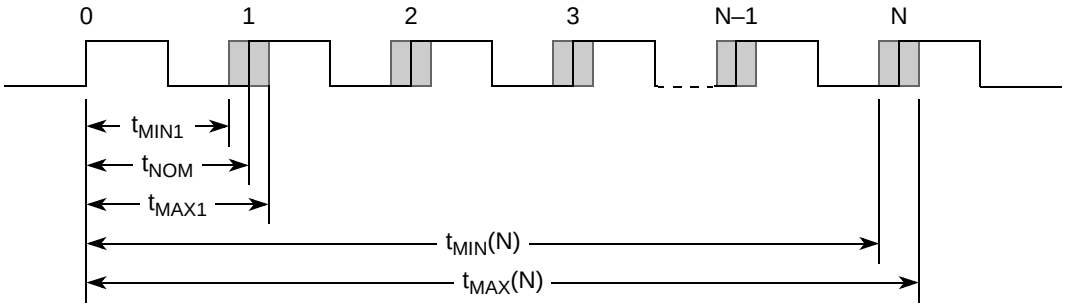


Figure 4. Jitter Definitions

The relative deviation of t_{NOM} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N). Thus, jitter is defined as:

$$J(N) = \max\left(\left|1 - \frac{t_{MAX}(N)}{N \cdot t_{NOM}}\right|, \left|1 - \frac{t_{MIN}(N)}{N \cdot t_{NOM}}\right|\right) \qquad \textit{Eqn. 15}$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2 \qquad \textit{Eqn. 16}$$

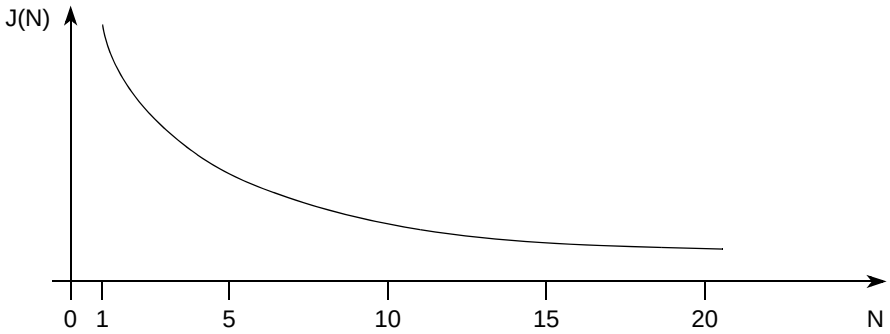


Figure 5. Maximum Bus Clock Jitter Approximation

3.8.3 PLL Characteristics

Table 20. PLL Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
K1		PLL reference frequency, crystal oscillator range	f_{REF}	0.5	—	16	MHz
K2	P	Self Clock Mode frequency	f_{SCM}	2	—	5.5	MHz
K3	D	VCO locking range	f_{VCO} [1]	8	—	50	MHz
K4	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3	—	4	% [2]
K5	D	Lock Detection	$\|\Delta_{Lock}\|$	0	—	1.5	% [2]
K6	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5	—	2.5	% [2]
K7	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6	—	8	% [2]
K8	C	PLLON Total Stabilization delay (Auto Mode) [3]	t_{stab}	—	0.5 [4]	3 [5]	ms
K9	D	PLLON Acquisition mode stabilization delay [3]	t_{acq}	—	0.3 [4]	1 [5]	ms
K10	D	PLLON Tracking mode stabilization delay [3]	t_{al}	—	0.2 [4]	2 [5]	ms
K11	D	Charge pump current acquisition mode	$\| i_{ch} \|$	—	38.5	—	µA
K12	D	Charge pump current tracking mode	$\| i_{ch} \|$	—	3.5	—	µA
K13	D	Jitter fit VCO loop gain parameter	K_1	—	–195	—	MHz/V
K14	D	Jitter fit VCO loop frequency parameter	f_1	—	126	—	MHz
K15	C	Jitter fit parameter 1	j_1	—	—	1.3	% [4]
K16	C	Jitter fit parameter 2	j_2	—	—	0.12	% [4]

NOTES:
1. If CLKSEL[PLLSEL] is set then the system clock (f_{SYS}) is equal to f_{VCO}, otherwise it is equal to f_{OSC} (table Table 19, J1a or J1b). Throughout this document, t_{SYS} is used to specify a unit of time equal to $1 \div f_{SYS}$.
2. Percentage deviation from target frequency
3. PLL stabilization delay is highly dependent on operational requirement and external component values (for example, crystal and XFC filter component values). Notes 4 and 5 show component values for a typical configurations. Appropriate XFC filter values should be chosen based on operational requirement of system.
4. f_{OSC} = 4 MHz, f_{VCO} = 40 MHz (REFDV = 0x00, SYNR = 0x04), C_S = 2.2 nF, C_P = 220 pF, R_S = 5.6 KΩ.
5. f_{OSC} = 4 MHz, f_{VCO} = 16 MHz (REFDV = 0x00, SYNR = 0x01), C_S = 4.7 nF, C_P = 470 pF, R_S = 2.7 KΩ.

3.8.4 Crystal Monitor Time-out

The time-out Table 21 shows the delay for the crystal monitor to trigger when the clock stops, either at the high or at the low level. The corresponding clock period with an ideal 50% duty cycle is twice this time-out value.

Table 21. Crystal Monitor Time-Outs

Min	Typ	Max	Unit
6	10	18.5	µs

3.8.5 Clock Quality Checker

The timing for the clock quality check is derived from the oscillator and the VCO frequency range in Table 20. These numbers define the upper time limit for the individual check windows to complete.

Table 22. CRG Maximum Clock Quality Check Timings

Clock Check Windows	Value	Unit
Check Window	9.1 to 20.0	ms
Timeout Window	0.46 to 1.0	s

3.8.6 Startup

Table 23 summarizes several startup characteristics. Refer to Section 4.3.6.10, “CRG Operating Mode Details,” in the *MAC7100 Microcontroller Family Reference Manual* (MAC7100RM) for details.

Table 23. CRG Startup Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
L1	D	Reset input pulse width	PW_{RSTL}	2	—	—	t_{OSC}
L2	D	Startup from Reset	n_{RST}	192	—	196	t_{OSC}
L3	D	$\overline{XIRQ}$, $\overline{IRQ}$ pulse width, edge-sensitive mode	PW_{IRQ}	20	—	—	ns

3.8.6.1 Power On and Low Voltage Reset (POR and LVR)

The V_{PORR} and V_{PORA} levels are derived from $V_{DD}2.5$. The V_{LVRA} level is derived from $V_{DD}2.5$. They are also valid if the device is powered externally. After releasing a POR or LVR reset, the oscillator and clock quality checks start. After t_{CQOUT} (Table 19, J4) if no valid oscillation is detected, the MCU will start using the internal self-generated clock. The minimum startup time is given by t_{uposc} (Table 19, J3).

3.8.6.2 SRAM Data Retention

SRAM content integrity is guaranteed if the CRGFLG[PORF] bit is not set following a reset operation.

3.8.6.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL}, the CRG generates an internal reset and the CPU fetches the reset vector without a clock quality check, if there was stable oscillation before reset.

3.8.6.4 Stop Recovery

The MCU can return from stop to run mode in response to an external interrupt or an API. Two delays occur before the MCU resumes execution. First, the voltage regulator must exit reduced power mode and return to full performance mode (this assumes that the internal regulator is used rather than driving $V_{DD}2.5$ and V_{DD}PLL with an external regulator). Second, a clock quality check is performed in the same manner as for a power-on reset before releasing the clocks to the system.

3.8.6.5 Pseudo Stop Recovery

Recovery from pseudo stop mode is similar to stop mode in that the VREG must return to FPM, but since the oscillator is not stopped there is no delay for clock stabilization. The MCU is returned to run mode by internal or external interrupts.

3.8.6.6 Doze Recovery

Recovery from doze mode avoids both the VREG and oscillator recovery periods. The MCU is returned to run mode by internal or external interrupts.

3.9 External Bus Timing

Table 24 lists processor bus input timings, which are shown in Figure 6, Figure 7 and Figure 8.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output. All other timing relationships can be derived from these values.

Table 24. External Bus Input Timing Specifications [1]

Num	C	Rating	Symbol	Min	Max	Unit
M1	P	CLKOUT period [2]	t_{CYC}	20	—	ns
Control Inputs						
M2a	P	Control input valid to CLKOUT high [3]	t_{CVCH}	13	—	ns
M3a	P	CLKOUT high to control inputs invalid [3]	t_{CHCII}	0	—	ns
Data Inputs						
M4	P	Data input (DATA[15:0]) valid to CLKOUT high	t_{DIVCH}	9	—	ns
M5	P	CLKOUT high to data input (DATA[15:0]) invalid	t_{CHDII}	0	—	ns

NOTES:
1. Assumes CLKOUT is configured for full drive strength (via the PIM CONFIG2_D[RDS] bit).
2. CLKOUT is equal to the system clock, f_{SYS}. If CLKSEL[PLLSEL] is set then f_{SYS} is equal to f_{VCO} (table Table 20, K3); if it is clear then f_{SYS} is equal to f_{OSC} (table Table 19, J1a or J1b). Throughout this document, t_{CYC} is used to specify a unit of time equal to 1 ÷ CLKOUT (which is equal to t_{fsys}).
3. The $\overline{TA}$ pin is the only control input on MAC7100 family devices.

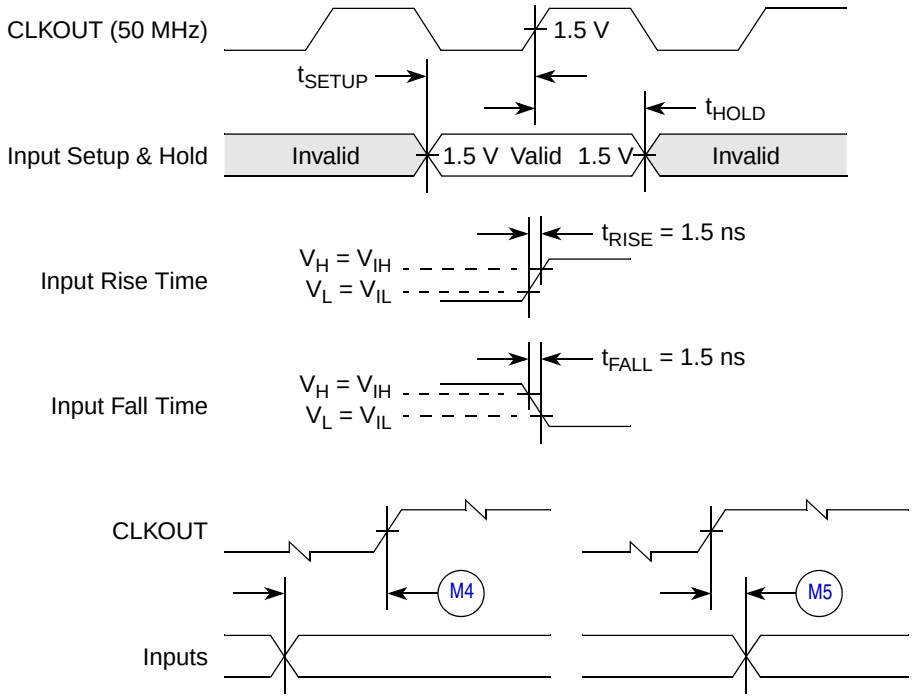


Figure 6. General Input Timing Requirements

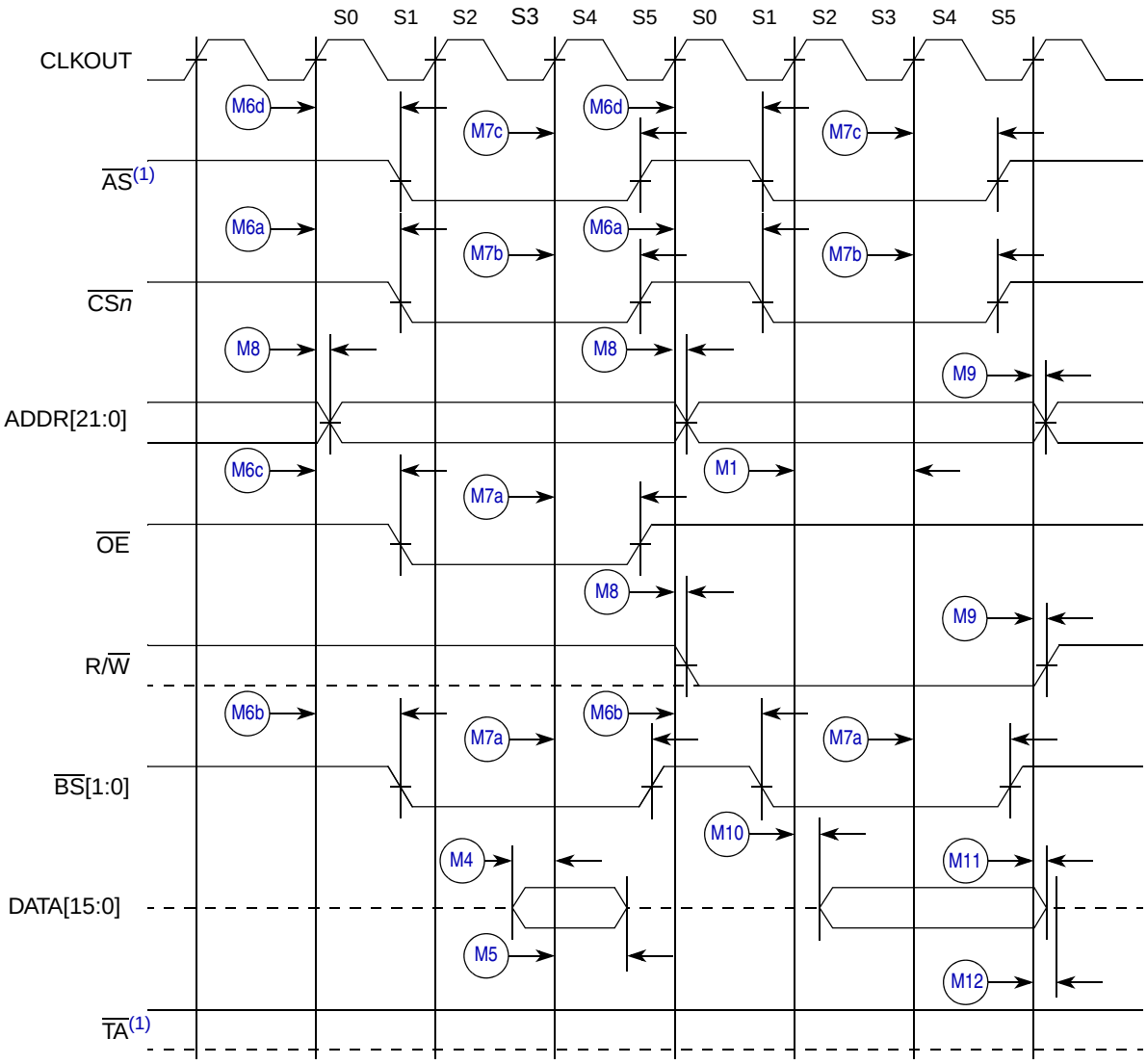
3.9.1 Read and Write Bus Cycles

Table 25 lists processor bus output timings. Read/write bus timings listed in Table 25 are shown in Figure 7 and Figure 8.

Table 25. External Bus Output Timing Specifications [1]

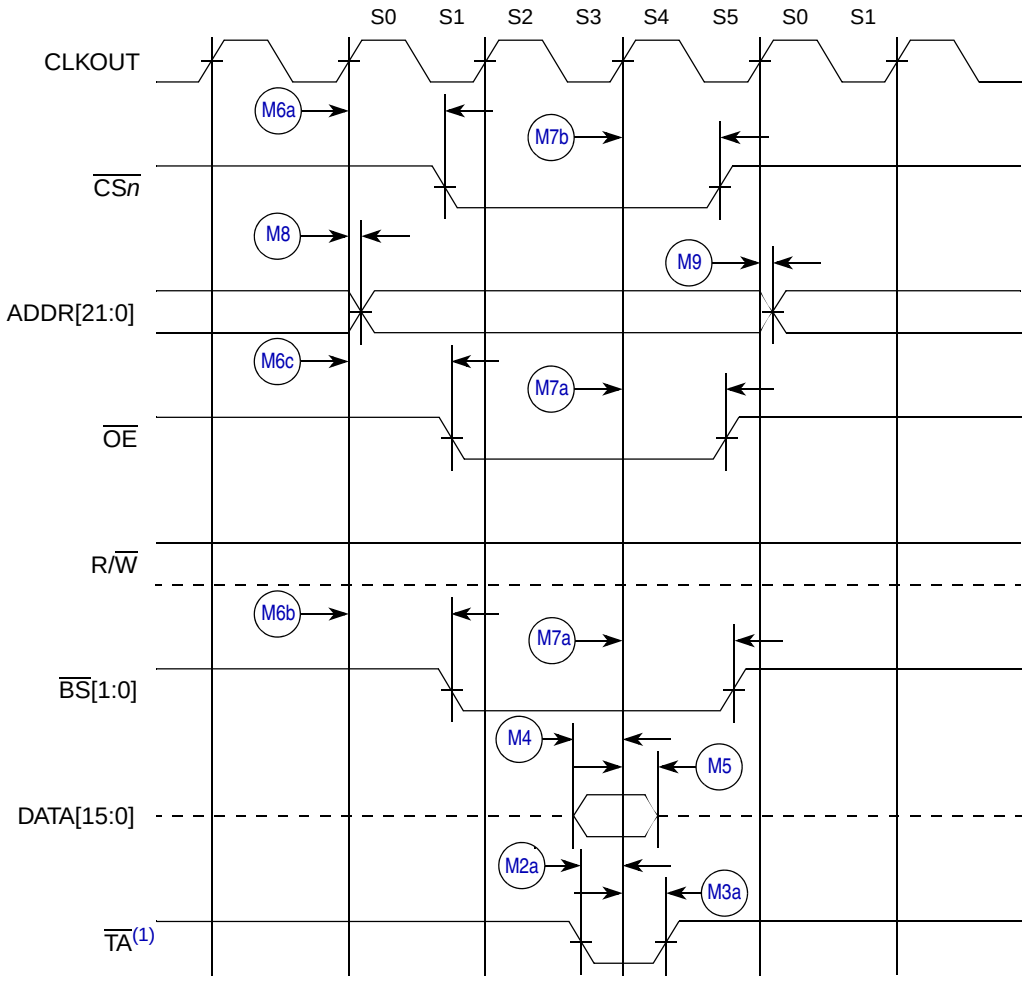
Num	C	Rating	Symbol	Min	Max	Unit
Control Outputs						
M6a	P	CLKOUT high [2] to chip selects ($\overline{CS}$[2:0]) valid	t_{CHCV}	—	$0.5t_{CYC}$ + 10	ns
M6b	P	CLKOUT high [2] to byte selects ($\overline{BS}$[1:0]) valid	t_{CHBV}	—	$0.5t_{CYC}$ + 10	ns
M6c	P	CLKOUT high [2] to output select ($\overline{OE}$) valid	t_{CHOV}	—	$0.5t_{CYC}$ + 10	ns
M6d	P	CLKOUT high [2] to address strobe ($\overline{AS}$) valid	t_{CHASV}	—	$0.5t_{CYC}$ + 10	ns
M7a	P	CLKOUT high [2] to control output ($\overline{BS}$[1:0], $\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$ + 2	—	ns
M7b	P	CLKOUT high [2] to chip selects ($\overline{CS}$[2:0]) invalid	t_{CHCI}	$0.5t_{CYC}$ + 2	—	ns
M7c	P	CLKOUT high [2] to address strobe ($\overline{AS}$) invalid	t_{CHASI}	$0.5t_{CYC}$ + 2	—	ns
Address and Attribute Outputs						
M8	P	CLKOUT high to address (ADDR[21:0]) and control (R/$\overline{W}$) valid	t_{CHAV}	—	10	ns
M9	P	CLKOUT high to address (ADDR[21:0]) and control (R/$\overline{W}$) invalid	t_{CHAI}	2	—	ns
Data Outputs						
M10	P	CLKOUT high to data output (DATA[15:0]) valid	t_{CHDOV}	—	13	ns
M11	P	CLKOUT high to data output (DATA[15:0]) invalid	t_{CHDOI}	2	—	ns
M12	D	CLKOUT high to data output (DATA[15:0]) high impedance	t_{CHDOZ}	—	9	ns

NOTES:
1. Assumes CLKOUT, $\overline{CS}n$, $\overline{BS}n$, $\overline{OE}$, $\overline{AS}$, ADDR[21:0] and DATA[15:0] are configured for full drive strength (via the PIM).
2. The $\overline{CS}n$, $\overline{BS}n$, $\overline{OE}$ and $\overline{AS}$ signals are synchronous to the falling edge of CLKOUT. Therefore, changes on these signals are triggered by the falling edge of CLKOUT, even though they are specified in relation to the rising edge.



1. The TA / AS signals are multiplexed on a single pin, so only one function may be used during bus transactions.

Figure 7. Read/Write Bus Cycles, Internal Termination



1. The TA / AS signals are multiplexed on a single pin, so AS is not available when external cycle termination is used.

Figure 8. Read Bus Cycle, External Termination

3.10 Analog-to-Digital Converter

Table 26 and Table 27 show conditions under which the ATD operates. The following constraints exist to obtain full-scale, full range results: $V_{SS}A \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DD}A$. This constraint exists because the sample buffer amplifier cannot drive beyond the ATD power supply levels. If the input level goes outside of this range it will effectively be clipped.

Table 26. ATD Operating Characteristics in 5.0 V Range

Conditions shown in Table 7 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
N1	D	Reference Potential Low High	V_{RL} V_{RH}	$V_{SS}A$ $V_{DD}A \div 2$	— —	$V_{DD}A \div 2$ $V_{DD}A$	V V
N2	C	Differential Reference Voltage [1]	$V_{RH} - V_{RL}$	4.50	5.00	5.50	V
N3	D	ATD Clock Frequency	f_{ATDCLK}	0.5	—	2.0	MHz
N4	D	ATD 10-bit Conversion Period f_{ATDCLK} Cycles [2] @ 2.0MHz f_{ATDCLK}	N_{CONV10} T_{CONV10}	14 7	— —	28 14	Cycles µs
N5	D	ATD 8-bit Conversion Period f_{ATDCLK} Cycles [2] @ 2.0MHz f_{ATDCLK}	N_{CONV8} T_{CONV8}	12 6	— —	26 13	Cycles µs
N6	D	Stop Recovery Time ($V_{DD}A$ = 5.0 V)	T_{REC}	—	—	20	µs
N7	P	Reference Supply current 1 ATD module on	I_{REF}	—	0.200	0.255	mA
N8	P	Reference Supply current 2 ATD modules on	I_{REF}	—	0.400	0.510	mA

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 4.50 V
2. Minimum time assumes a sample period of 2 ATD clocks; maximum time assumes a sample period of 16 ATD clocks.

Table 27. ATD Operating Characteristics in 3.3 V Range

Conditions shown in Table 7, with $V_{DD}X$ = 3.3 V –5/+10% and a temperature maximum of +140°C unless otherwise noted.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
P1	D	Reference Potential Low High	V_{RL} V_{RH}	$V_{SS}A$ $V_{DD}A \div 2$	— —	$V_{DD}A \div 2$ $V_{DD}A$	V V
P2	C	Differential Reference Voltage [1]	$V_{RH} - V_{RL}$	3.15	3.3	3.6	V
P3	D	ATD Clock Frequency	f_{ATDCLK}	0.5	—	2.0	MHz
P4	D	ATD 10-bit Conversion Period f_{ATDCLK} Cycles [2] @ 2.0MHz f_{ATDCLK}	N_{CONV10} T_{CONV10}	14 7	— —	28 14	Cycles µs
P5	D	ATD 8-bit Conversion Period f_{ATDCLK} Cycles [2] @ 2.0MHz f_{ATDCLK}	N_{CONV8} T_{CONV8}	12 6	— —	26 13	Cycles µs
P6	D	Stop Recovery Time ($V_{DD}A$ = 3.3 V)	T_{REC}	—	—	20	µs
P7	P	Reference Supply current 1 ATD module on	I_{REF}	—	0.130	0.170	mA
P8	P	Reference Supply current 2 ATD modules on	I_{REF}	—	0.260	0.340	mA

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 3.15 V
2. Minimum time assumes a sample period of 2 ATD clocks; maximum time assumes a sample period of 16 ATD clocks.

3.10.1 Factors Influencing Accuracy

Three factors—source resistance, source capacitance and current injection—have an influence on the accuracy of the ATD.

3.10.1.1 Source Resistance

Due to the input pin leakage current as specified in Table 8 in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum specified source resistance R_S, results in an error of less than 1/2 LSB (2.5 mV) at the maximum leakage current. If the device or operating conditions are less than the worst case, or leakage-induced errors are acceptable, larger values of source resistance are allowed.

3.10.1.2 Source Capacitance

When sampling, an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external capacitance and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1 LSB, then the external filter capacitor must be calculated as, $C_f \geq 1024 \times (C_{INS} - C_{INN})$.

3.10.1.3 Current Injection

There are two cases to consider:

1. A current is injected into the channel being converted. The channel being stressed has conversion values of 0x3FF (0xFF in 8-bit mode) for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance. The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K \times R_S \times I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table 28. ATD Electrical Characteristics

Conditions are shown in Table 7 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Q1	C	Max input Source Resistance	R_S	—	—	1	kΩ
Q2	C	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}	 — —	 10 22	 — —	 pF pF
Q3	C	Disruptive Analog Input Current	I_{NA}	–2.5	—	2.5	mA
Q4	C	Coupling Ratio positive current injection	K_p	—	—	TBD	A / A
Q5	C	Coupling Ratio negative current injection	K_n	—	—	TBD	A / A

3.10.2 ATD Accuracy

Table 29 and Table 30 specify the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table 29. ATD Conversion Performance in 5.0 V Range

Conditions shown in Table 7 except as noted here: f_{ATDCLK} = 2.0 MHz, 4.5 V ≤ $V_{DD}A$ ≤ 5.5 V							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
R1	P	10-bit Resolution	LSB	—	5 [1]	—	mV
R2	P	10-bit Differential Nonlinearity	DNL	–1	—	1	Counts
R3	P	10-bit Integral Nonlinearity	INL	–2.5	±1.5	2.5	Counts
R4	P	10-bit Absolute Error [2]	AE	–3	±2.0	3	Counts
R5	P	8-bit Resolution	LSB	—	20 [1]	—	mV
R6	P	8-bit Differential Nonlinearity	DNL	–0.5	—	0.5	Counts
R7	P	8-bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
R8	P	8-bit Absolute Error [2]	AE	–1.5	±1.0	1.5	Counts

NOTES:
1. Assumes $V_{REF} = V_{RH} - V_{RL}$ = 5.12 V, other V_{REF} conditions result in different LSB resolutions.
2. These values include the quantization error which is inherently ½ count for any A/D converter.

Table 30. ATD Conversion Performance in 3.3 V Range

Conditions shown in Table 7 except as noted here: f_{ATDCLK} = 2.0 MHz, 3.15 V ≤ $V_{DD}A$ ≤ 3.6 V							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
S1	P	10-bit Resolution	LSB	—	3.25 [1]	—	mV
S2	P	10-bit Differential Nonlinearity	DNL	–1.5	—	1.5	Counts
S3	P	10-bit Integral Nonlinearity	INL	–3.5	±1.5	3.5	Counts
S4	P	10-bit Absolute Error [2]	AE	–5	±2.0	5	Counts
S5	P	8-bit Resolution	LSB	—	13 [1]	—	mV
S6	P	8-bit Differential Nonlinearity	DNL	–0.5	—	0.5	Counts
S7	P	8-bit Integral Nonlinearity	INL	–1.5	±1.0	1.5	Counts
S8	P	8-bit Absolute Error [2]	AE	–1.5	±1.0	1.5	Counts

NOTES:
1. Assumes $V_{REF} = V_{RH} - V_{RL}$ = 3.33 V, other V_{REF} conditions result in different LSB resolutions.
2. These values include the quantization error which is inherently ½ count for any A/D converter.

For the following definitions, see Figure 9.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps:

$$DNL(i) = \frac{V_i - V_{i-1}}{1\ LSB} - 1 \qquad \textit{Eqn. 17}$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1\ LSB} - n \qquad \textit{Eqn. 18}$$

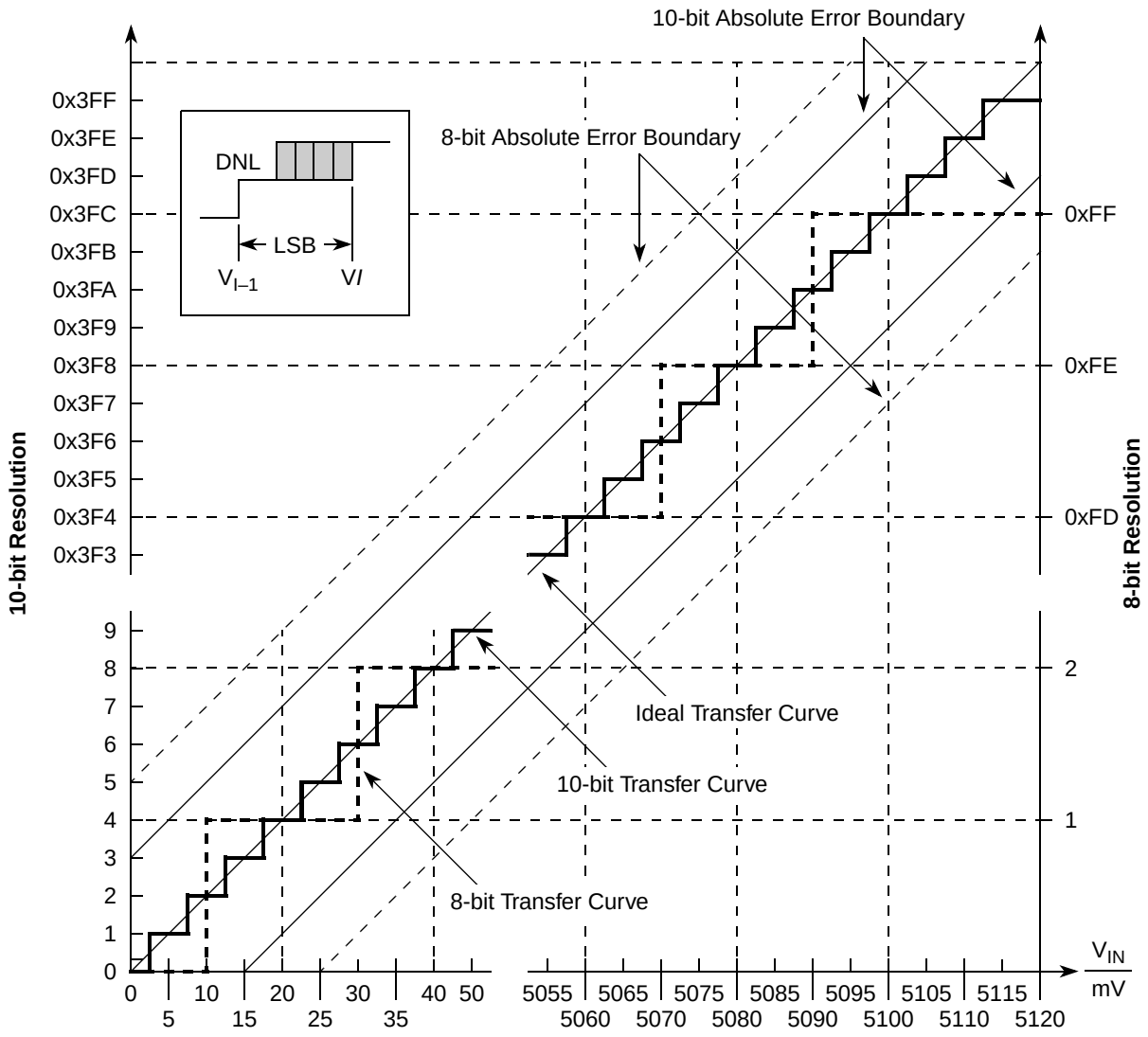


Figure 9. ATD Accuracy Definitions

NOTE

Figure 9 shows only definitions, for specification values refer to Table 29.

3.10.3 ATD Timing Specifications

Table 31. ATD External Trigger Timing Specifications

Num	C	Parameter	Symbol	Min	Max	Unit
T1	D	ETRIG Period (Level-Sensitive Trigger Mode)	T_{PERIOD}	1 + N_{CONVn} [1]	—	f_{ATDCLK} Cycles
T2	D	ETRIG Minimum Pulse Width Edge-Sensitive Trigger Mode Level-Sensitive Trigger Mode	t_{PW}	 1 2	 — —	f_{ATDCLK} Cycles
T3	D	ETRIG Level Recovery [2]	t_{LR}	1	—	f_{ATDCLK} Cycles
T4	D	Conversion Start Delay	t_{DLY}	—	2	f_{ATDCLK} Cycles

NOTES:
1. N_{CONVn} denotes 8- or 10-bit conversion time (refer to specifications N4, N5, P4 and P5). In order to achieve the minimum period between conversions when using level-sensitive triggering, ETRIG must remain asserted this long.
2. Time prior to the end of a conversion that ETRIG must be negated in order to prevent the start of another conversion.

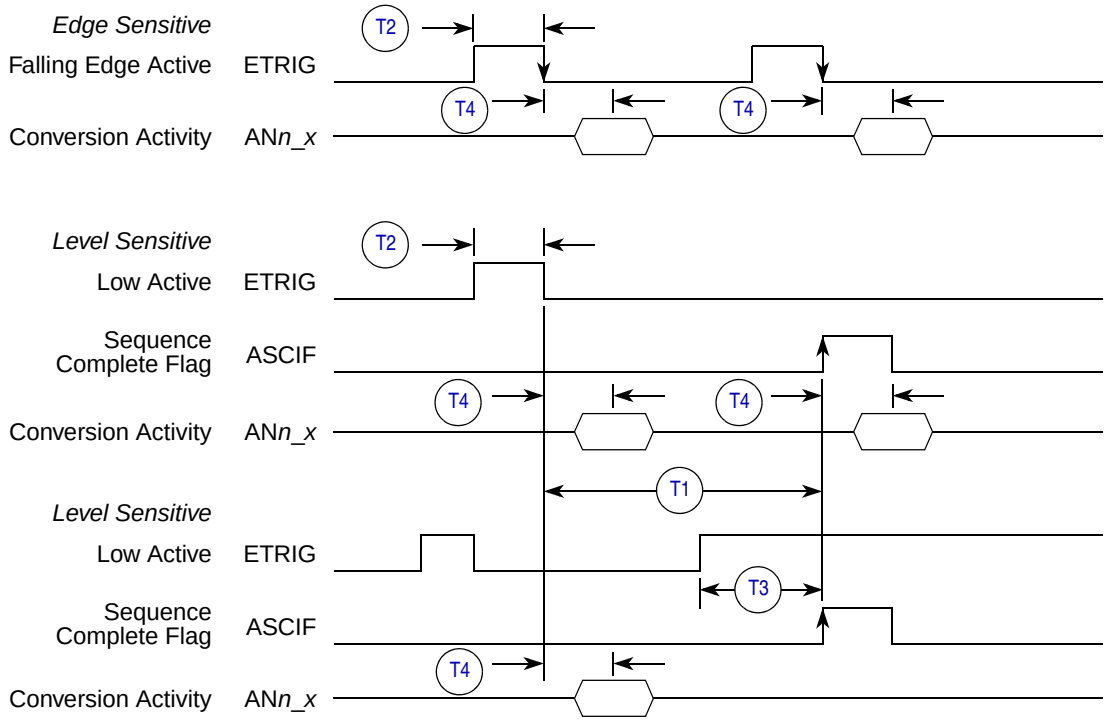


Figure 10. ATD External Trigger Timing Diagram

3.11 Serial Peripheral Interface

3.11.1 Master Mode

Master mode timing values are shown in Table 32 and illustrated in Figure 11 and Figure 12.

Table 32. SPI Master Mode Timing Characteristics

Conditions are shown in Table 7 unless otherwise noted, C_{LOAD} = 200 pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
U1a	P	Operating Frequency (baud rate)	f_{OP} [1]	$\frac{1}{7 \times 32,678}$	—	½ [2]	f_{IPS}
U1b	P	SCK Period ($t_{SCK} = 1 \div f_{OP}$, $t_{IPS} = 1 \div f_{IPS}$)	t_{SCK} [1]	2 [2]	—	7 × 32,768	t_{IPS}
U2	D	Enable Lead Time	t_{lead}	½	—	—	t_{SCK}
U3	D	Enable Lag Time	t_{lag}	½	—	—	t_{SCK}
U4	D	Clock (SCK) High or Low Time	t_{wsck}	t_{IPS} – 30	—	1024 t_{IPS}	ns
U5	D	Data Setup Time (Inputs)	t_{su}	25	—	—	ns
U6	D	Data Hold Time (Inputs)	t_{hi}	0	—	—	ns
U9	D	Data Valid (after Enable Edge)	t_v	—	—	25	ns
U10	D	Data Hold Time (Outputs)	t_{ho}	0	—	—	ns
U11	D	Rise Time Inputs and Outputs	t_r	—	—	25	ns
U12	D	Fall Time Inputs and Outputs	t_f	—	—	25	ns

NOTES:
1. Refer to *MAC7100 Microcontroller Family Reference Manual* (MAC7100RM) Chapter 22 for all available baud rates.
2. On mask set L49P and L47W devices, U1a maximum = ¼ and U1b minimum = 4.

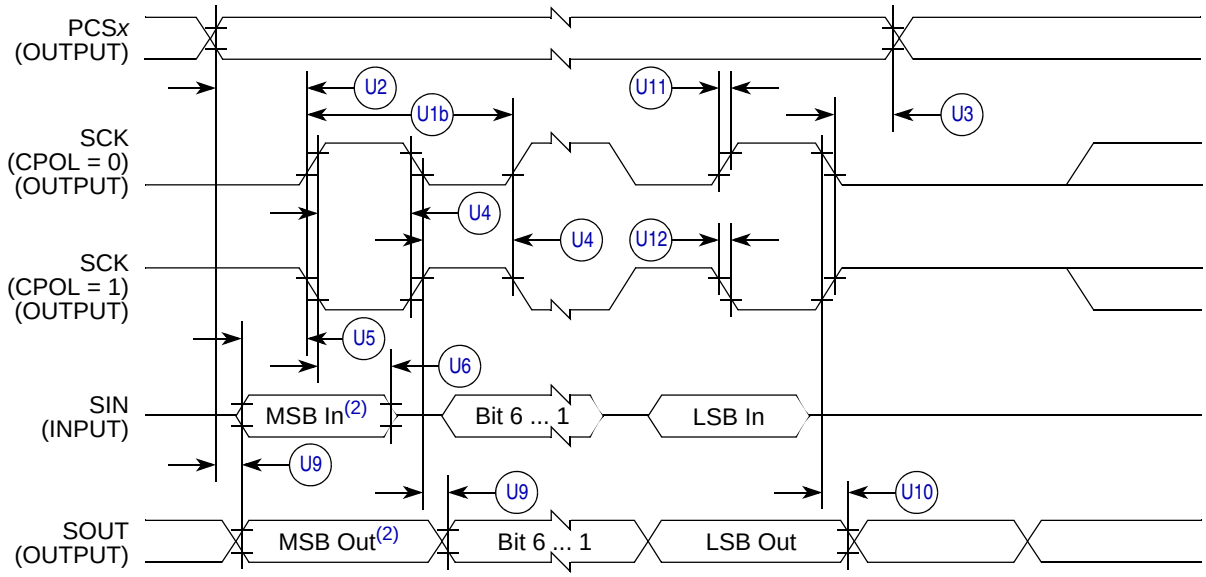
3.11.2 Slave Mode

Slave mode timing values are shown in Table 33 and illustrated in Figure 13 and Figure 14.

Table 33. SPI Slave Mode Timing Characteristics

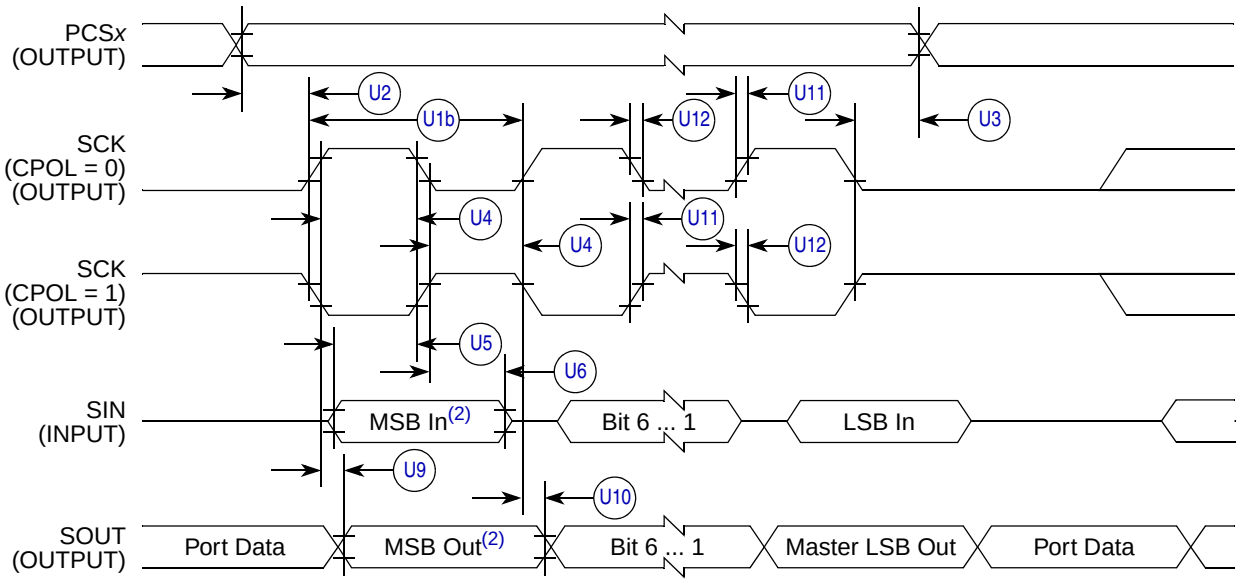
Conditions are shown in Table 7 unless otherwise noted, C_{LOAD} = 200 pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
V1a	P	Operating Frequency	f_{OP}	$\frac{1}{7 \times 32,678}$	—	½ [1]	f_{IPS}
V1b	P	SCK Period ($t_{SCK} = 1 \div f_{OP}$, $t_{IPS} = 1 \div f_{IPS}$)	t_{SCK}	2 [1]	—	7 × 32,768	t_{IPS}
V2	D	Enable Lead Time	t_{lead}	1	—	—	t_{IPS}
V3	D	Enable Lag Time	t_{lag}	1	—	—	t_{IPS}
V4	D	Clock (SCK) High or Low Time	t_{wsck}	t_{IPS} – 30	—	—	ns
V5	D	Data Setup Time (Inputs)	t_{su}	25	—	—	ns
V6	D	Data Hold Time (Inputs)	t_{hi}	25	—	—	ns
V7	D	Slave Access Time	t_a	—	—	1	t_{IPS}
V8	D	Slave SIN Disable Time	t_{dis}	—	—	1	t_{IPS}
V9	D	Data Valid (after SCK Edge)	t_v	—	—	25	ns
V10	D	Data Hold Time (Outputs)	t_{ho}	0	—	—	ns
V11	D	Rise Time Inputs and Outputs	t_r	—	—	25	ns
V12	D	Fall Time Inputs and Outputs	t_f	—	—	25	ns

NOTES:
1. On mask set L49P and L47W devices, V1a maximum = ¼ and V1b minimum = 4.



1. If configured as output.
2. LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 11. SPI Master Timing (CPHA = 0)



1. If configured as output.
2. LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI Master Timing (CPHA = 1)

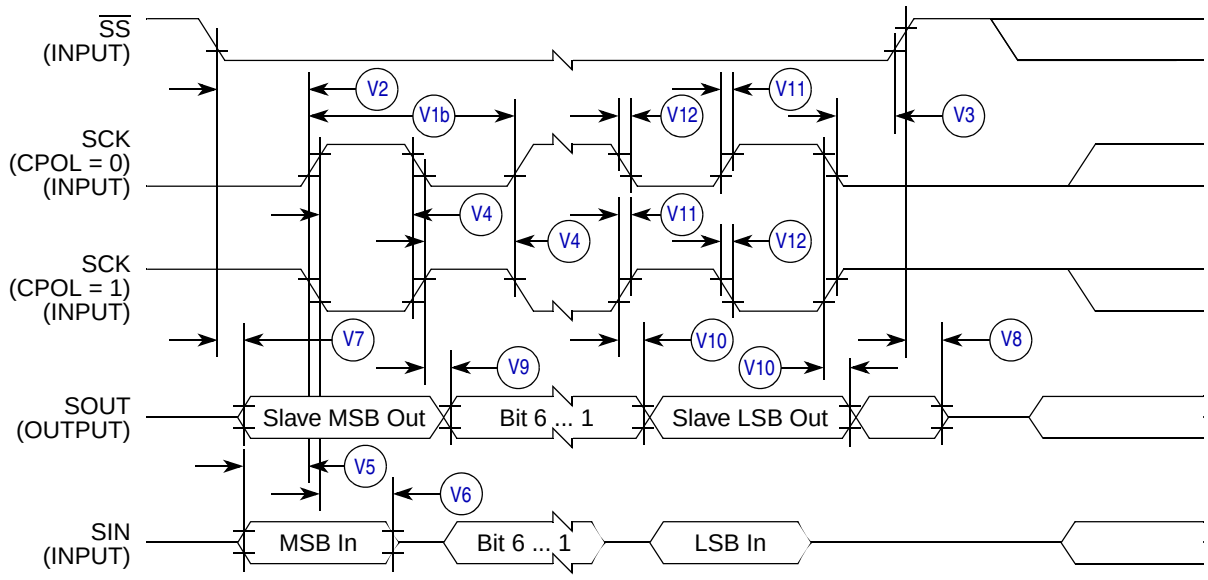


Figure 13. SPI Slave Timing (CPHA = 0)

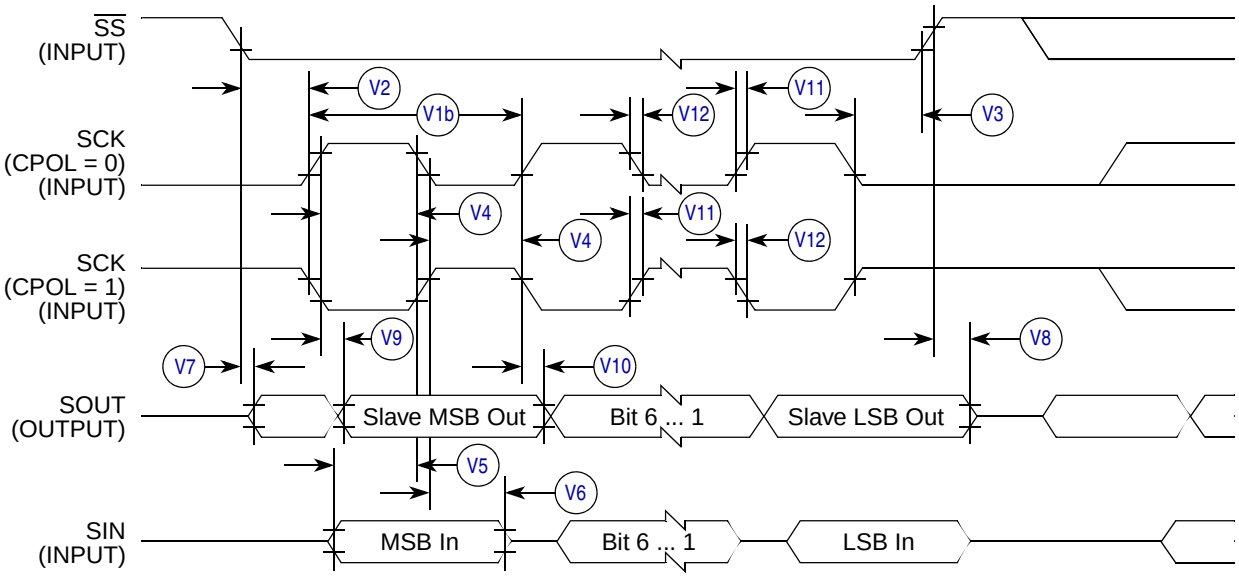


Figure 14. SPI Slave Timing (CPHA = 1)

3.12 FlexCAN Interface

Table 34. FlexCAN Wake-up Pulse Characteristics

Conditions are shown in Table 7 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
W1	P	FlexCAN Wake-up dominant pulse filtered	t_{WUP}	—	—	2	µs
W2	P	FlexCAN Wake-up dominant pulse passed	t_{WUP}	5	—	—	µs

3.13 Common Flash Module

NOTE

Unless otherwise noted the abbreviation NVM (Non-Volatile Memory) is used for both program Flash and data Flash.

The time base for all program and data Flash operations, f_{NVMOP}, is derived from the IPS bus clock, f_{IPS}, using the CFMCLKD register to control the divider ratio. Throughout this section, t_{IPS} refers to $1 \div f_{IPS}$, and t_{NVMOP} refers to $1 \div f_{NVMOP}$. An f_{NVMOP} frequency range limit is imposed for performing program or erase operations. The CFM does not monitor the frequency and will not prevent program or erase operation at frequencies above or below the following limits:

$$150\ \text{KHz} < f_{NVMOP} \leq 200\ \text{KHz} \qquad \textit{Eqn. 19}$$

f_{NVMOP} = 200 KHz gives the fastest program and erase performance. Setting CFMCLKD to a value such that f_{NVMOP} < 150 KHz should be avoided, as this can damage the Flash memory due to overstress. Setting CFMCLKD to a value such that f_{NVMOP} > 200 KHz can result in incomplete programming or erasure of the Flash memory array cells.

3.13.1 Mass Erase Timing

The time required to erase the entire NVM array (both program and data) is calculated using the formula:

$$t_{mass} \approx 20000 \cdot t_{NVMOP} \qquad \textit{Eqn. 20}$$

The setup time can be ignored for this operation.

3.13.2 Blank Check Timing

The time it takes to perform a blank check on the program or data Flash is dependant on the location of the first non-blank word, starting from relative address zero. One f_{IPS} cycle is required per word to be verified, and the time required for the operation is calculated using the formula:

$$t_{check} = (\text{locations} + 15) \cdot t_{IPS} \qquad \textit{Eqn. 21}$$

3.13.3 Page Erase Timing

The time required to erase a 4 Kbyte program or 1 Kbyte data Flash logical page is calculated using the formulas:

$$t_{erap} = 4096 \cdot t_{NVMOP} + 15 \cdot t_{IPS} \quad \textit{Eqn. 22}$$

$$t_{erad} = 1024 \cdot t_{NVMOP} + 15 \cdot t_{IPS} \quad \textit{Eqn. 23}$$

3.13.4 Page Erase Verify Timing

The time required to verify that a program Flash page is erased depends on the location of the first non-blank word. The time required for the operation is calculated using the formula:

$$t_{pevp} = \left[\left(\frac{4 \times 1024}{4}\right) + 15\right] \times t_{IPS} \quad \textit{Eqn. 24}$$

The time required to verify that a data Flash page is erased is calculated using the formula:

$$t_{pevd} = \left[\left(\frac{1 \times 1024}{4}\right) + 15\right] \times t_{IPS} \quad \textit{Eqn. 25}$$

3.13.5 Programming Timing

Programming time is dependant on the f_{IPS} and f_{NVMOP} frequencies, and is calculated for a single word using the formula:

$$t_{swpgm} = 9 \cdot t_{NVMOP} + 25 \cdot t_{IPS} \quad \textit{Eqn. 26}$$

Burst programming can be utilized with the program Flash, where up to 32 words in a row can be programmed consecutively by keeping the command pipeline filled. The time to program a consecutive word is calculated using the formula:

$$t_{bwpgm} = 4 \cdot t_{NVMOP} + 9 \cdot t_{IPS} \quad \textit{Eqn. 27}$$

Therefore, the time to program a 32-word row is calculated using the formula:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm} \quad \textit{Eqn. 28}$$

Note that burst programming is more than 2 times faster than single word programming.

3.13.6 Data Signature Timing[1]

The time required to perform a data signature command is dependant on the number of words or half-words compressed during the operation, and is calculated using the formula:

$$t_{dsig} = (\text{Words or Half-Words} + 15) \cdot t_{IPS} \quad \textit{Eqn. 29}$$

1. This feature is not available on mask set L49P and L47W devices.

3.13.7 CFM Timing Specifications

Table 35 lists the time required to execute various operations described in the Section 3.13.1 through Section 3.13.6. For operating conditions other than those assumed below, Equation 19 through Equation 29 must be used to calculate the timing for specific commands under those conditions.

Table 35. CFM Timing Characteristics

Conditions are shown in Table 7 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
X1	D	System Clock	$f_{NVMfsys}$	0.5	—	50 [1]	MHz
X2	D	Bus frequency for Programming or Erase Operations	$f_{NVMfips}$	1	—	—	MHz
X3	D	Program/Erase Operating Frequency	f_{NVMOP}	150	—	200	kHz
X4	P	Programming Time, [2] Single Word f_{SYS} = 50 MHz	t_{swpgm}	47.1	—	71.0	µs
		f_{SYS} = 40 MHz		48.1	—	71.0	
X5	D	Programming Time, [2] Consecutive Word Burst f_{SYS} = 50 MHz	t_{bwpgm}	20.8	—	30.5	µs
		f_{SYS} = 40 MHz		21.3	—	30.5	
X6	D	Programming Time, [2] 32-word Row Burst f_{SYS} = 50 MHz	t_{brpgm}	693.1	—	1,016.5	µs
		f_{SYS} = 40 MHz		706.8	—	1,016.5	
X7a	P	Page Erase Time, [2] Program Flash f_{SYS} = 50 MHz	t_{erap}	21.0	—	26.6	ms
		f_{SYS} = 40 MHz		21.3	—	26.6	
X7b	P	Page Erase Time, [2] Data Flash f_{SYS} = 50 MHz	t_{erad}	5.2	—	6.7	ms
		f_{SYS} = 40 MHz		5.3	—	6.7	
X8	P	Mass Erase Time [2]	t_{mass}	100	—	130	ms
X9a	D	Blank Check Time, [3] Program Flash per Block MAC71*x*1, MAC71*x*6	$t_{bcheckp}$	16	—	131,087	t_{IPS}
		MAC71*x*2		16	—	65,551	
X9b	D	Blank Check Time, [3] Data Flash per Block	$t_{bcheckd}$	16	—	8,207	t_{IPS}
X9c	D	Page Erase Verify Time [3] Program Flash	t_{pevp}	16	—	1,039	t_{IPS}
		Data Flash	t_{pevd}	16	—	271	
X10	D	Data Signature Time [4] MAC71*x*6, Program	t_{dsig}	17	—	262,159	t_{IPS}
		MAC71*x*1, Program		17	—	131,087	
		MAC71*x*2, Program		17	—	65,551	
		MAC71*xx*, Data		17	—	16,399	

NOTES:
1. Subject to restrictions in Table 19 and Table 20 for operating characteristics of the oscillator and PLL.
2. Minimum erase and programming times are achieved with the indicated maximum f_{SYS} (which is $f_{IPS} \times 2$, and subject to the limits of Table 19 and Table 20) and corresponding maximum f_{NVMOP}. Maximum erase and programming times are dependent on the combination of f_{NVMOP} and f_{IPS}; values shown are calculated for f_{IPS} = 2 MHz and f_{NVMOP} = 154 KHz.
3. Minimum blank check or page erase verify time assumes the first word in the array is blank and the second is not. Maximum blank check or page erase verify time assumes the entire block or page is blank.
4. Data signature timing is dependant on the number of words or half-words compressed for the program and data arrays, respectively. Minimum time is for two words or half-words; maximum time is for the entire array.

3.13.8 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures. The failure rates for data retention and program/erase cycling are specified at the operating conditions noted. The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table 36. NVM Reliability Characteristics

Conditions shown in Table 7 unless otherwise noted.				
Num	**C**	**Rating**	**Min**	**Unit**
X11	C	Program/Data Flash Program/Erase endurance (–40C to +125C)	10,000	Cycles
X12	C	Program/Data Flash Data Retention Lifetime	15	Years

NOTE

All values shown in Table 36 are target values and subject to characterization. For Flash cycling performance, each program operation must be preceded by an erase.

4 Device Pin Assignments

The MAC7100 Family is available in 208-pin ball grid array (MAP BGA), 144-pin low profile quad flat (LQFP), 112-pin LQFP, and 100-pin LQFP package options. The family of devices offer pin-compatible packaged devices to assist with system development and accommodate a direct application enhancement path. Refer to Table 2 for a comparison of the peripheral sets and package options for each device.

Most pins perform two or more functions, which are described in more detail in the *MAC7100 Microcontroller Family Reference Manual* (MAC7100RM). Table 37, Table 38 and Figure 15 through Figure 22 show the pin assignments for various devices and packages.

Table 37. Signal Pin Assignments

Primary / GPIO Function	Peripheral Function [1]	External Bus Function [1]	Debug Function [1]	Read on Reset	Pin Number (by Device)							
					7101 7106	7111 7116	7112	7121 7126	7122	7131	7136	7141 7142
EXTAL	—	—	—	—	60	60	60	48	48	T10	T10	45
XTAL	—	—	—	—	61	61	61	49	49	T11	T11	46
XFC	—	—	—	—	58	58	58	46	46	T9	T9	43
$\overline{\text{RESET}}$	—	—	—	—	48	48	48	36	36	T7	T7	33
TDI	—	—	—	—	128	128	128	102	102	A8	A8	93
TDO	—	—	—	—	129	129	129	103	103	B8	B8	94
TCK	—	—	—	—	130	130	130	104	104	A7	A7	95
TMS	—	—	—	—	131	131	131	105	105	B7	B7	96
—	—	$\overline{\text{TA}}$ / $\overline{\text{AS}}$ [2]	—	—	—	79	—	—	—	M14	M14	—
PA0	—	DATA0 [3]	$\overline{\text{MCKO}}$ [4]	—	138	138	138	106	106	B5	B5	—
PA1	—	DATA1 [3]	$\overline{\text{EVTO}}$	—	137	137	137	—	—	C5	C5	—
PA2	—	DATA2 [3]	$\overline{\text{EVTI}}$	—	136	136	136	—	—	A5	A5	—
PA3	—	DATA3 [3]	MDO0	—	135	135	135	—	—	C6	C6	—
PA4	—	DATA4 [3]	MDO1	—	134	134	134	—	—	B6	B6	—
PA5	—	DATA5 [3]	$\overline{\text{MSEO}}$	—	133	133	133	—	—	A6	A6	—
PA6	—	DATA6 [3]	$\overline{\text{RDY}}$	—	132	132	132	—	—	C7	C7	—
PA7	—	DATA7 [3]	—	—	—	98	98	74	74	H15	H15	65
PA8	—	DATA8 [3]	—	—	—	97	97	73	73	H13	H13	64
PA9	—	DATA9 [3]	—	—	—	96	96	72	72	H14	H14	63
PA10	—	DATA10 [3]	—	—	—	95	95	71	71	H16	H16	—
PA11	—	DATA11 [3]	—	—	—	94	94	70	70	J15	J15	—
PA12	—	DATA12 [3]	—	—	—	93	93	69	69	J14	J14	—
PA13	—	DATA13 [3]	—	—	67	67	67	53	53	R12	R12	—
PA14	—	DATA14 [3]	—	$\overline{\text{PS}}$ [3]	66	66	66	52	52	T12	T12	—
PA15	—	DATA15 [3]	—	$\overline{\text{AA}}$ [3]	65	65	65	51	51	P11	P11	48
PB0	SDA	—	—	—	15	15	15	11	11	G1	G1	8
PB1	SCL	—	—	—	16	16	16	12	12	H3	H3	9
PB2	SIN_A	—	—	—	17	17	17	13	13	H2	H2	10
PB3	SOUT_A	—	—	—	18	18	18	14	14	H1	H1	11
PB4	SCK_A	—	—	—	19	19	19	15	15	J3	J3	12
PB5	PCS0_A / $\overline{\text{SS\_A}}$	—	—	—	20	20	20	16	16	J1	J1	13
PB6	PCS1_A	—	—	—	21	21	21	17	17	J2	J2	14
PB7	PCS2_A	—	—	—	22	22	22	18	18	K1	K1	15

Table 37. Signal Pin Assignments (continued)

Primary / GPIO Function	Peripheral Function [1]	External Bus Function [1]	Debug Function [1]	Read on Reset	Pin Number (by Device)							
					7101 7106	7111 7116	7112	7121 7126	7122	7131	7136	7141 7142
PB8	PCS5_A / $\overline{\text{PCSS\_A}}$	—	—	—	23	23	23	19	19	K2	K2	16
PB9	PCS0_B / $\overline{\text{SS\_B}}$	—	—	—	72	72	72	56	56	T14	T14	51
PB10	PCS5_B / $\overline{\text{PCSS\_B}}$	—	—	—	73	73	73	57 [5]	57	R14	R14	52
PB11	PCS2_B	—	—	—	74	74	74	— [5]	—	N14	N14	53
PB12	PCS1_B	—	—	—	75	75	75	58	58	P15	P15	54
PB13	SCK_B	—	—	—	76	76	76	59	59	P16	P16	55
PB14	SOUT_B	—	—	—	77	77	77	60	60	N15	N15	56
PB15	SIN_B	—	—	—	78	78	78	61	61	N16	N16	57
PC0	—	ADDR0 [3]	—	—	9	9	9	—	—	F1	F1	—
PC1	—	ADDR1 [3]	—	—	10	10	10	—	—	F3	F3	—
PC2	—	ADDR2 [3]	—	—	11	11	11	—	—	G2	G2	—
PC3	—	ADDR3 [3]	—	—	12	12	12	—	—	G3	G3	—
PC4	—	ADDR4 [3]	—	—	28	28	28	—	—	L3	L3	—
PC5	—	ADDR5 [3]	—	—	29	29	29	—	—	M2	M2	—
PC6	—	ADDR6 [3]	—	—	30	30	30	—	—	M3	M3	—
PC7	—	ADDR7 [3]	—	—	31	31	31	—	—	N3	N3	—
PC8	—	ADDR8 [3]	—	—	44	44	44	—	—	P5	P5	—
PC9	—	ADDR9 [3]	—	—	45	45	45	—	—	R6	R6	—
PC10	—	ADDR10 [3]	—	—	46	46	46	—	—	P6	P6	—
PC11	—	ADDR11 [3]	—	—	47	47	47	—	—	T6	T6	—
PC12	—	ADDR12 [3]	—	—	—	88	88	—	—	K14	K14	—
PC13	—	ADDR13 [3]	—	—	—	89	89	—	—	K13	K13	—
PC14	—	ADDR14 [3]	—	—	—	90	90	—	—	K15	K15	—
PC15	—	ADDR15 [3]	—	—	—	91	91	67	67	J16	J16	—
PD0	—	$\overline{\text{BS0}}$ [3]	—	MODB	70	70	70	54	54	T13	T13	49
PD1	—	$\overline{\text{BS1}}$ [3]	—	MODA	71	71	71	55	55	R13	R13	50
PD2 [6]	—	CLKOUT	—	$\overline{\text{XCLKS}}$	80	80	80	62	62	M16	M16	58
PD3	$\overline{\text{XIRQ}}$	—	—	—	81	81	81	63	63	M15	M15	59
PD4	$\overline{\text{IRQ}}$	—	—	—	82	82	82	64	64	L16	L16	60
PD5	—	ADDR16 [3]	—	—	—	92	92	68	68	J13	J13	—
PD6	—	ADDR17 [3]	—	—	—	119	119	95	95	C10	C10	86
PD7	—	ADDR18 [3]	—	—	—	120	120	96	96	D10	D10	87
PD8	—	ADDR19 [3]	—	—	—	121	121	97	97	D9	D9	88
PD9	—	ADDR20 [3]	—	—	—	122	122	98	98	B9	B9	89
PD10	—	ADDR21 [3]	—	—	—	123	123	99	99	D8	D8	90
PD11	—	$\overline{\text{OE}}$ [3]	—	—	68	68	68	—	—	P12	P12	—
PD12	—	$\overline{\text{CS2}}$ [3]	—	—	69	69	69	—	—	P13	P13	—
PD13	—	$\overline{\text{CS1}}$ [3]	—	—	83	83	83	—	—	L13	L13	—
PD14	—	$\overline{\text{CS0}}$ [3]	—	—	84	84	84	—	—	L14	L14	—
PD15	—	R/$\overline{\text{W}}$ [3]	—	—	85	85	85	—	—	L15	L15	—
PE0	AN0_A	—	MCKO'	—	89	99	99	75	75	G16	G16	66
PE1	AN1_A	—	$\overline{\text{EVTO}}$'	—	91	100	100	76	76	G15	G15	67

Table 37. Signal Pin Assignments (continued)

Primary / GPIO Function	Peripheral Function [1]	External Bus Function [1]	Debug Function [1]	Read on Reset	Pin Number (by Device)							
					7101 7106	7111 7116	7112	7121 7126	7122	7131	7136	7141 7142
PE2	AN2_A	—	$\overline{\text{EVTI}}$'	—	93	101	101	77	77	F13	F13	68
PE3	AN3_A	—	MDO0'	—	95	102	102	78	78	F14	F14	69
PE4	AN4_A	—	MDO1'	—	97	103	103	79	79	E13	E13	70
PE5	AN5_A	—	$\overline{\text{MSEO}}$'	—	99	104	104	80	80	E14	E14	71
PE6	AN6_A	—	$\overline{\text{RDY}}$'	—	101	105	105	81	81	D15	D15	72
PE7	AN7_A	—	—	—	103	106	106	82	82	C15	C15	73
PE8	AN8_A	—	—	—	105	107	107	83	83	C14	C14	74
PE9	AN9_A	—	—	—	107	108	108	84	84	D14	D14	75
PE10	AN10_A	—	—	—	113	113	113	89	89	B13	B13	80
PE11	AN11_A	—	—	—	115	114	114	90	90	C12	C12	81
PE12	AN12_A	—	—	—	117	115	115	91	91	A12	A12	82
PE13	AN13_A	—	—	—	119	116	116	92	92	B11	B11	83
PE14	AN14_A	—	—	—	121	117	117	93	93	A10	A10	84
PE15	AN15_A	—	—	—	123	118	118	94	94	A9	A9	85
PF0	eMIOS0	—	Debug Status [7]	NEXPS	43	43	43	35	35	T5	T5	32
PF1	eMIOS1	—	Debug Status [7]	NEXPR	42	42	42	34	34	R5	R5	31
PF2	eMIOS2	—	Debug Status [7]	—	41	41	41	33	33	T4	T4	30
PF3	eMIOS3	—	Debug Status [7]	—	40	40	40	32	32	R4	R4	29
PF4	eMIOS4	—	Debug Status [7]	—	39	39	39	31	31	T3	T3	28
PF5	eMIOS5	—	Debug Status [7]	—	38	38	38	30	30	P4	P4	27
PF6	eMIOS6	—	Debug Status [7]	—	37	37	37	29	29	R3	R3	26
PF7	eMIOS7	—	Debug Status [7]	—	36	36	36	28	28	R1	R1	25
PF8	eMIOS8	—	Debug Status [7]	—	35	35	35	27	27	P2	P2	24
PF9	eMIOS9	—	Debug Status [7]	—	34	34	34	26	26	P1	P1	23
PF10	eMIOS10	—	Debug Status [7]	—	33	33	33	25	25	N2	N2	22
PF11	eMIOS11	—	Debug Status [7]	—	32	32	32	24	24	N1	N1	21
PF12	eMIOS12	—	Debug Status [7]	—	27	27	27	23	23	M1	M1	20
PF13	eMIOS13	—	Debug Status [7]	—	26	26	26	22	22	L2	L2	19
PF14	eMIOS14	—	Debug Status [7]	—	25	25	25	21	21	L1	L1	18
PF15	eMIOS15	—	Debug Status [7]	—	24	24	24	20	20	K3	K3	17
PG0	RXD_B	—	—	—	141	141	141	109	109	A3	A3	97
PG1	TXD_B	—	—	—	142	142	142	110	110	C4	C4	98
PG2	RXD_A	—	—	—	143	143	143	111	111	B3	B3	99
PG3	TXD_A	—	—	—	144	144	144	112	112	C2	C2	100
PG4	CNTX_A	—	—	—	1	1	1	1	1	D3	D3	1
PG5	CNRX_A	—	—	—	2	2	2	2	2	C1	C1	2
PG6	CNTX_B	—	—	—	7	7	7	7	7	E1	E1	3
PG7	CNRX_B	—	—	—	8	8	8	8	8	F2	F2	4
PG8	CNTX_C [8]	—	—	—	3	3	3	3	3	D2	D2	—
PG9	CNRX_C [8]	—	—	—	4	4	4	4	4	D1	D1	—
PG10	CNTX_D [8]	—	—	—	5	5	5	5	5	E3	E3	—
PG11	CNRX_D [8]	—	—	—	6	6	6	6	6	E2	E2	—
PG12	RXD_D [8]	—	—	—	51	51	51	39	39	R7	R7	36
PG13	TXD_D [8]	—	—	—	52	52	52	40	40	R8	R8	37

Table 37. Signal Pin Assignments (continued)

Primary / GPIO Function	Peripheral Function [1]	External Bus Function [1]	Debug Function [1]	Read on Reset	Pin Number (by Device)							
					7101 7106	7111 7116	7112	7121 7126	7122	7131	7136	7141 7142
PG14	RXD_C	—	—	—	139	139	139	107	107	A4	A4	—
PG15	TXD_C	—	—	—	140	140	140	108	108	B4	B4	—
PH0	AN0_B	—	—	—	88	—	—	—	—	G13	G13	—
PH1	AN1_B	—	—	—	90	—	—	—	—	G14	G14	—
PH2	AN2_B	—	—	—	92	—	—	—	—	F16	F16	—
PH3	AN3_B	—	—	—	94	—	—	—	—	F15	F15	—
PH4	AN4_B	—	—	—	96	—	—	—	—	E16	E16	—
PH5	AN5_B	—	—	—	98	—	—	—	—	E15	E15	—
PH6	AN6_B	—	—	—	100	—	—	—	—	D16	D16	—
PH7	AN7_B	—	—	—	102	—	—	—	—	C16	C16	—
PH8	AN8_B	—	—	—	104	—	—	—	—	B16	B16	—
PH9	AN9_B	—	—	—	106	—	—	—	—	B14	B14	—
PH10	AN10_B	—	—	—	108	—	—	—	—	D13	D13	—
PH11	AN11_B	—	—	—	114	—	—	—	—	A13	A13	—
PH12	AN12_B	—	—	—	116	—	—	—	—	B12	B12	—
PH13	AN13_B	—	—	—	118	—	—	—	—	C11	C11	—
PH14	AN14_B	—	—	—	120	—	—	—	—	A11	A11	—
PH15	AN15_B	—	—	—	122	—	—	—	—	B10	B10	—
PI0	PCS3_A	—	—	—	—	—	—	—	—	—	C3	—
PI1	PCS4_A	—	—	—	—	—	—	—	—	—	D5	—
PI2	PCS6_A	—	—	—	—	—	—	—	—	—	D4	—
PI3	PCS7_A	—	—	—	—	—	—	—	—	—	E4	—
PI4	PCS3_B	—	—	—	—	—	—	—	—	—	G4	—
PI5	PCS4_B	—	—	—	—	—	—	—	—	—	J4	—
PI6	PCS6_B	—	—	—	—	—	—	—	—	—	K4	—
PI7	PCS7_B	—	—	—	—	—	—	—	—	—	L4	—
PI8	—	—	—	—	—	—	—	—	—	—	N4	—
PI9	—	—	—	—	—	—	—	—	—	—	P3	—
PI10	—	—	—	—	—	—	—	—	—	—	R2	—
PI11	—	—	—	—	—	—	—	—	—	—	R15	—
PI12	—	—	—	—	—	—	—	—	—	—	N11	—
PI13	—	—	—	—	—	—	—	—	—	—	N12	—
PI14	—	—	—	—	—	—	—	—	—	—	N13	—
PI15	—	—	—	—	—	—	—	—	—	—	P14	—

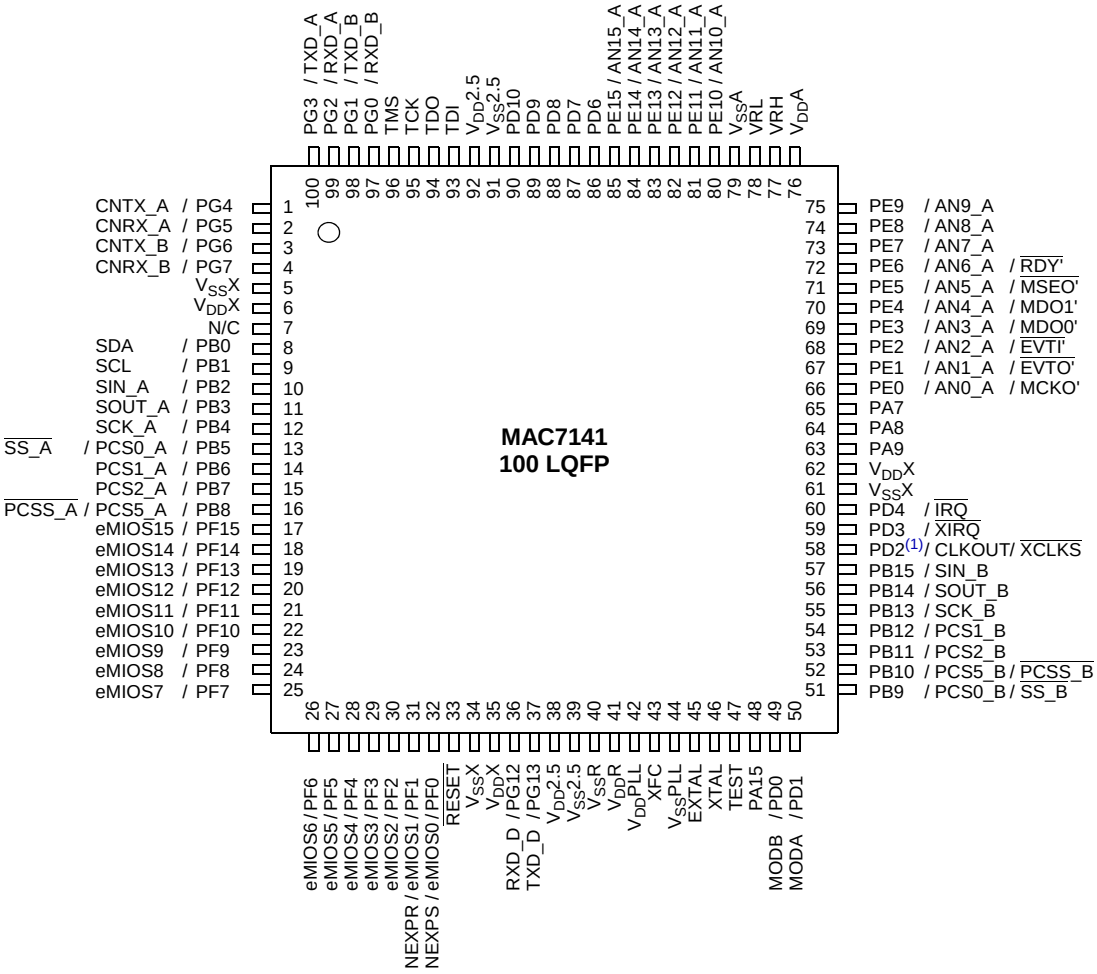
NOTES:
1. The MAC7100 family maximum peripheral configurations are listed in these columns. Some family members do not implement the full complement of ATD, CAN, DSPI and eSCI peripherals. Refer to Table 2 on page 3 for availability of peripheral functions on various devices.
2. $\overline{AS}$ function not available on mask set L49P devices.
3. MAC7111, MAC7116, MAC7131 and MAC7136 only.
4. The MCKO function cannot be used on MAC7121 devices (the alternate Nexus port must be used).
5. On MAC7121 mask set L49P devices, PB11 / PCS2_B is bonded out on pin 57.
6. PD2 function not available on mask set L49P devices.
7. Optional debug status port not available on mask set L49P devices.
8. CAN C, CAN D and eSCI D not available on MAC7112, MAC7122 and MAC7142 devices.

Table 38. Power Supply, Voltage Regulator and Reference Pin Assignments

Pin Name	Pin Number (by Device)			
	7101 / 7106 / 7111 / 7112 / 7116	**7121 / 7122 / 7126**	**7131 / 7136**	**7141 / 7142**
$V_{DD}X$	14, 50, 64, 87, 124	10, 38, 66	C9, H4, K16, P7, P10	6, 35, 62
$V_{SS}X$	13, 49, 63, 86, 125 **7101 / 7106 / 7112 only:** 79	9, 37, 65	A1, A2, B1, B2, F4, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M4, M13, R9, R10, R16, T1, T2, T15, T16 **7131 only:** C3, D4, D5, E4, G4, J4, K4, L4, N4, N11, N12, N13, P3, P14, R9, R10	5, 34, 61
$V_{DD}R$	56	44	P9	41
$V_{SS}R$	55	43	N5, N6	40
$V_{DD}2.5$	53, 127	41, 101	C8, P8	38, 92
$V_{SS}2.5$	54, 126	42, 100	D6, D7, N7, N8	39, 91
$V_{DD}PLL$	57	45	T8	42
$V_{SS}PLL$	59	47	N9, N10	44
$V_{DD}A$	109	85	A16, B15, C13	76
$V_{SS}A$	112	88	D11, D12	79
V_{RH}	110	86	A15	77
V_{RL}	111	87	A14	78
TEST [1]	62	50	R11	47
N/C	—	—	—	7

NOTES:
1. This pin is reserved for Freescale factory testing, and must be tied to system ground in all applications.

4.1 MAC7141 Pin Diagram



1. PD2 function not available on L49P mask set devices.

Figure 15. Pin Assignments for MAC7141 in 100-pin LQFP

4.2 MAC7142 Pin Diagram

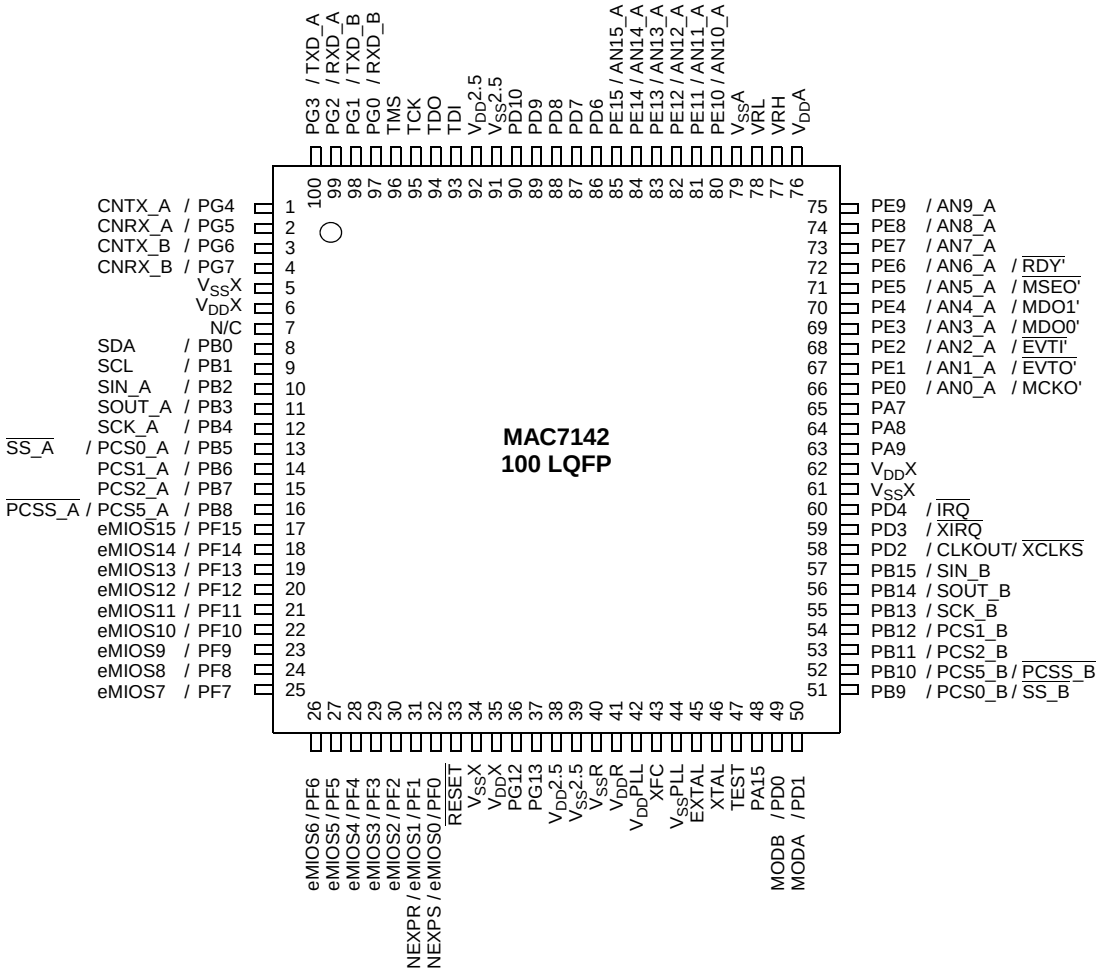
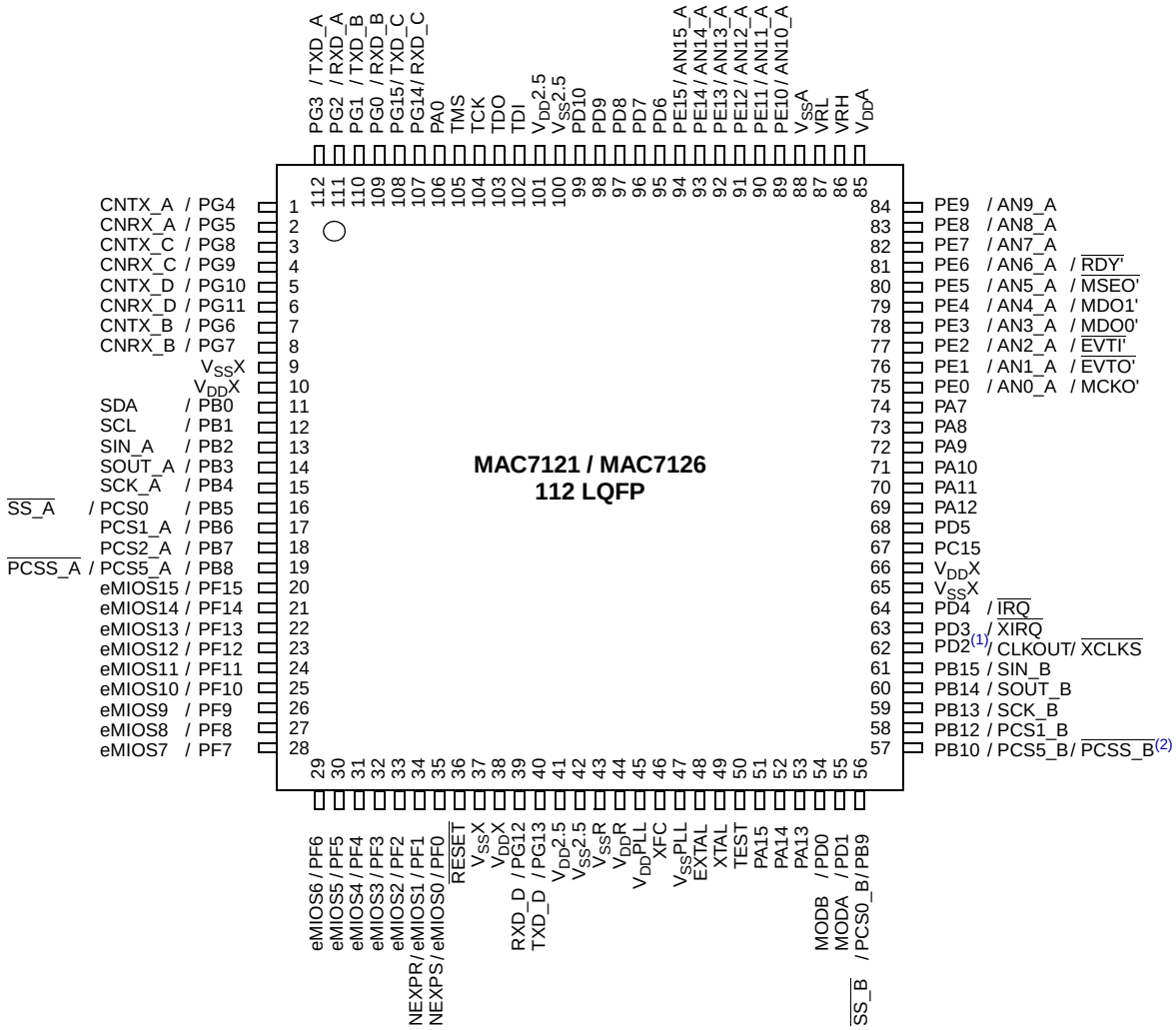


Figure 16. Pin Assignments for MAC7142 in 100-pin LQFP

4.3 MAC7121 / MAC7126 Pin Diagram



1. PD2 function not available on L49P mask set devices.
2 On L49P mask set devices, PB11 / PCS2_B is bonded out on pin 57.

Figure 17. Pin Assignments for MAC7121 / MAC7126 in 112-pin LQFP

4.4 MAC7122 Pin Diagram

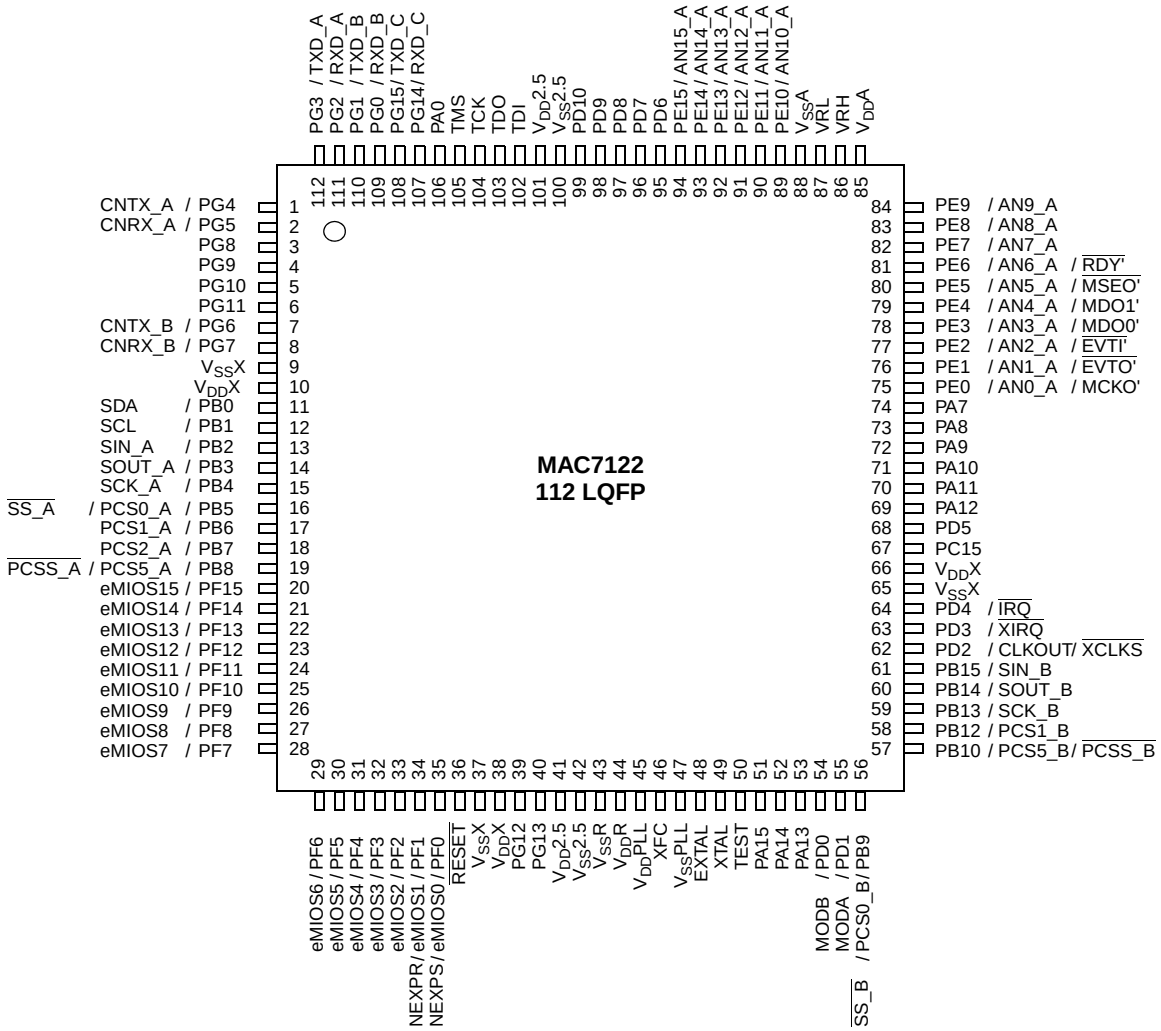
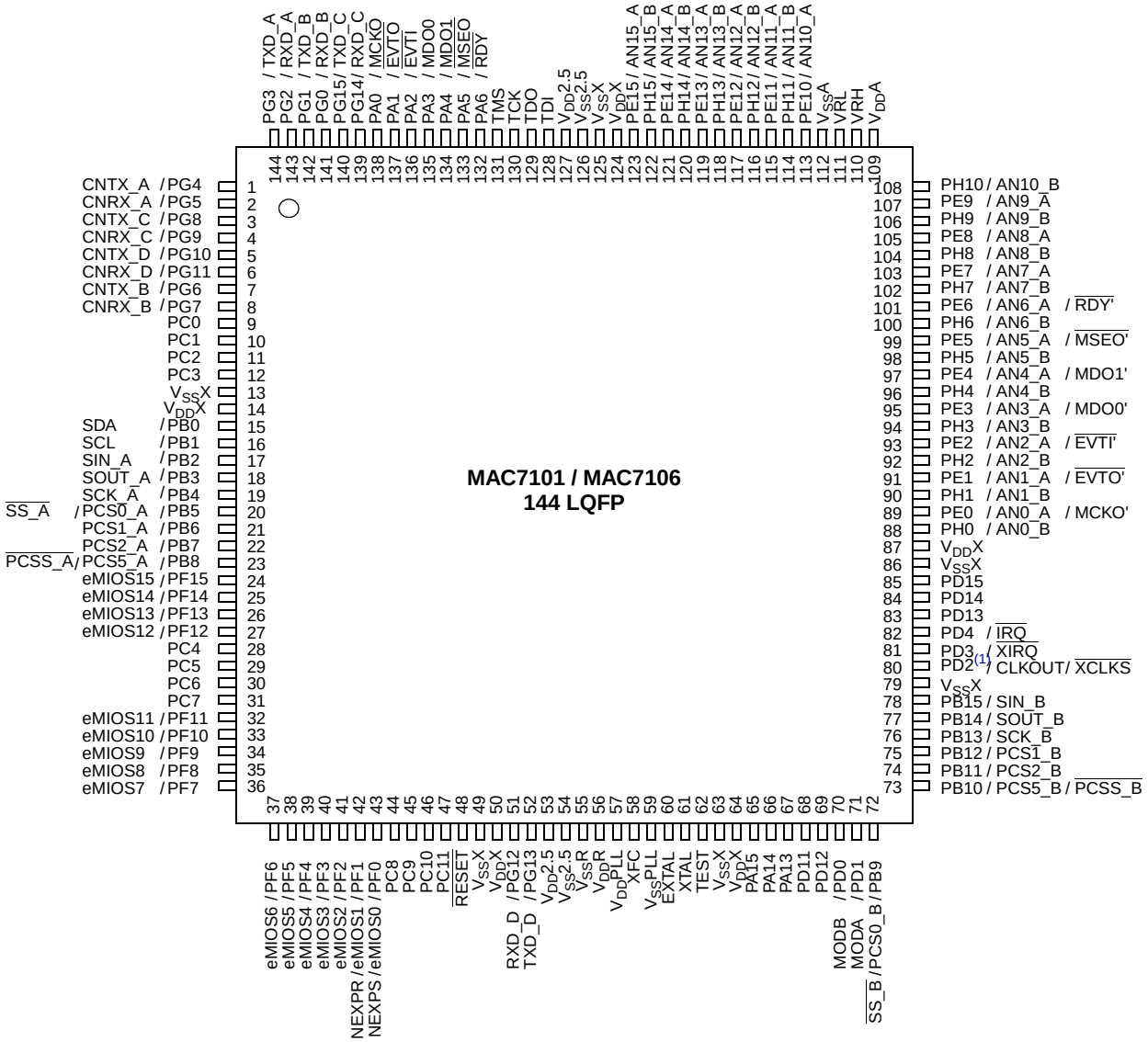


Figure 18. Pin Assignments for MAC7122 in 112-pin LQFP

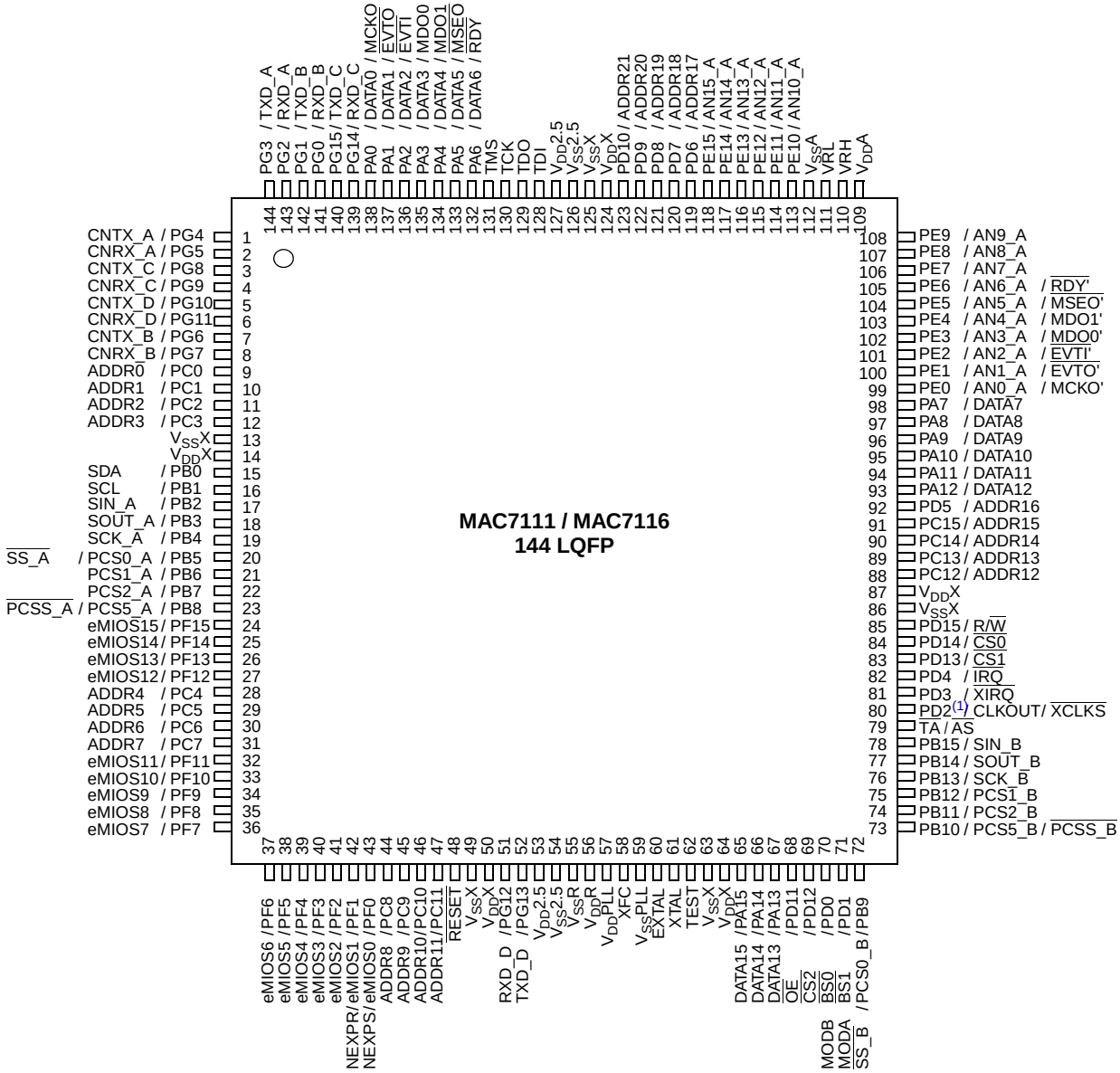
4.5 MAC7101 / MAC7106 Pin Diagram



1. PD2 function not available on L49P mask set devices.

Figure 19. Pin Assignments for MAC7101 / MAC7106 in 144-pin LQFP

4.6 MAC7111 / MAC7116 Pin Diagram



1. PD2 function not available on L49P mask set devices.

Figure 20. Pin Assignments for MAC7111 / MAC7116 in 144-pin LQFP

4.7 MAC7112 Pin Diagram

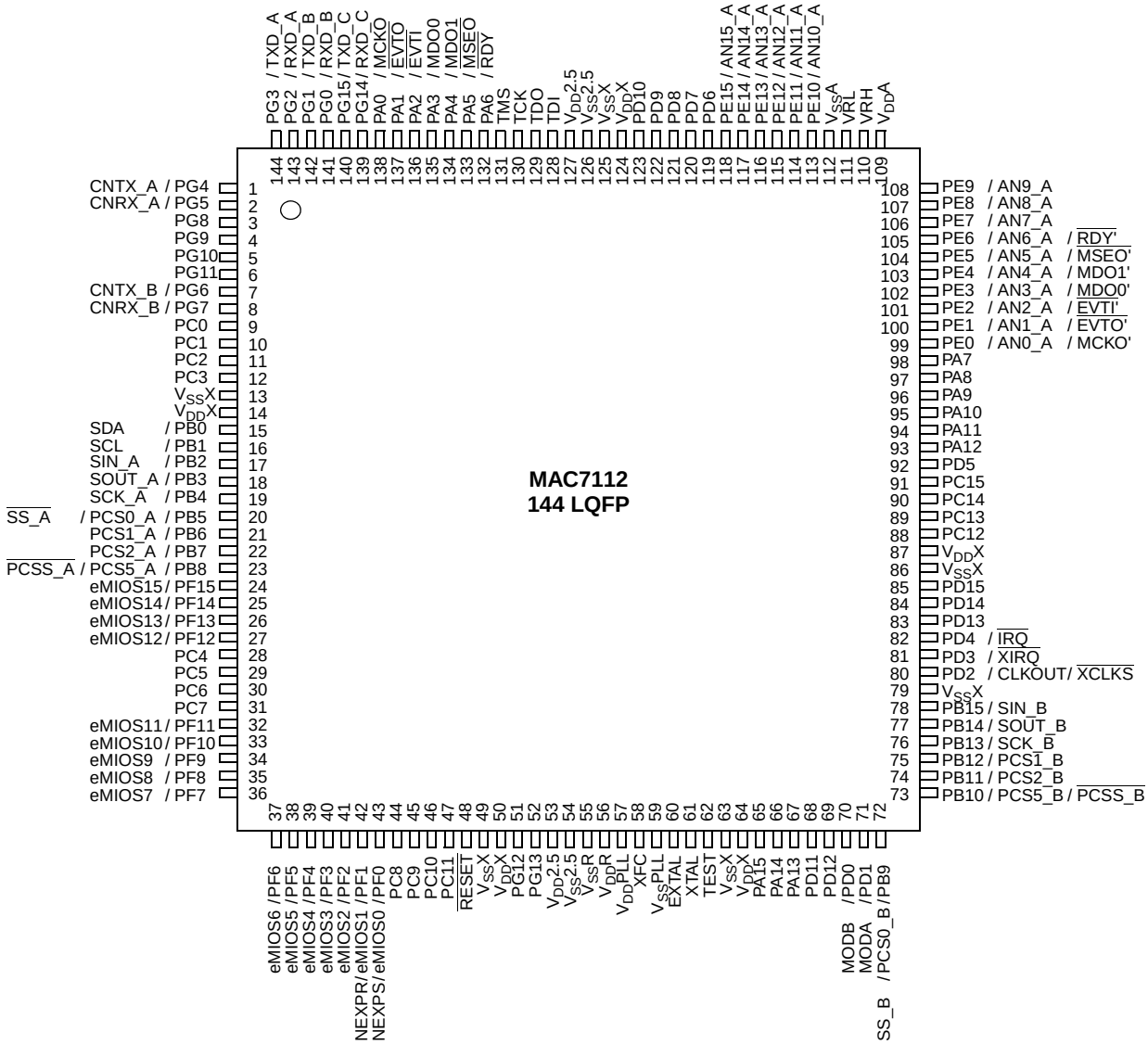


Figure 21. Pin Assignments for MAC7112 in 144-pin LQFP

4.8 MAC7131 Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	$V_{SS}X$	$V_{SS}X$	PG0	PG14	PA2	PA5	TCK	TDI	PE15	PE14	PH14	PE12	PH11	V_{RL}	V_{RH}	$V_{DD}A$
B	$V_{SS}X$	$V_{SS}X$	PG2	PG15	PA0	PA4	TMS	TDO	PD9	PH15	PE13	PH12	PE10	PH9	$V_{DD}A$	PH8
C	PG5	PG3	$V_{SS}X$	PG1	PA1	PA3	PA6	$V_{DD}2.5$	$V_{DD}X$	PD6	PH13	PE11	$V_{DD}A$	PE8	PE7	PH7
D	PG9	PG8	PG4	$V_{SS}X$	$V_{SS}X$	$V_{SS}2.5$	$V_{SS}2.5$	PD10	PD8	PD7	$V_{SS}A$	$V_{SS}A$	PH10	PE9	PE6	PH6
E	PG6	PG11	PG10	$V_{SS}X$									PE4	PE5	PH5	PH4
F	PC0	PG7	PC1	$V_{SS}X$									PE2	PE3	PH3	PH2
G	PB0	PC2	PC3	$V_{SS}X$			$V_{SS}X$	$V_{SS}X$	$V_{SS}X$	$V_{SS}X$			PH0	PH1	PE1	PE0
H	PB3	PB2	PB1	$V_{DD}X$			$V_{SS}X$	$V_{SS}X$	$V_{SS}X$	$V_{SS}X$			PA8	PA9	PA7	PA10
J	PB5	PB6	PB4	$V_{SS}X$			$V_{SS}X$	$V_{SS}X$	$V_{SS}X$	$V_{SS}X$			PD5	PA12	PA11	PC15
K	PB7	PB8	PF15	$V_{SS}X$			$V_{SS}X$	$V_{SS}X$	$V_{SS}X$	$V_{SS}X$			PC13	PC12	PC14	$V_{DD}X$
L	PF14	PF13	PC4	$V_{SS}X$									PD13	PD14	PD15	PD4
M	PF12	PC5	PC6	$V_{SS}X$									$V_{SS}X$	$\overline{TA}/\overline{AS}$[1]	PD3	PD2[1]
N	PF11	PF10	PC7	$V_{SS}X$	$V_{SS}R$	$V_{SS}R$	$V_{SS}2.5$	$V_{SS}2.5$	$V_{SS}PLL$	$V_{SS}PLL$	$V_{SS}X$	$V_{SS}X$	$V_{SS}X$	PB11	PB14	PB15
P	PF9	PF8	$V_{SS}X$	PF5	PC8	PC10	$V_{DD}X$	$V_{DD}2.5$	$V_{DD}R$	$V_{DD}X$	PA15	PD11	PD12	$V_{SS}X$	PB12	PB13
R	PF7	$V_{SS}X$	PF6	PF3	PF1	PC9	PG12	PG13	$V_{SS}X$	$V_{SS}X$	TEST	PA13	PD1	PB10	$V_{SS}X$	$V_{SS}X$
T	$V_{SS}X$	$V_{SS}X$	PF4	PF2	PF0	PC11	$\overline{RESET}$	$V_{DD}PLL$	XFC	EXTAL	XTAL	PA14	PD0	PB9	$V_{SS}X$	$V_{SS}X$

1. $\overline{AS}$ and PD2 functions not available on L49P mask set devices.

Figure 22. Pin Assignments for MAC7131 in 208-pin MAP BGA

4.9 MAC7136 Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	$V_{SS}X$	$V_{SS}X$	PG0	PG14	PA2	PA5	TCK	TDI	PE15	PE14	PH14	PE12	PH11	V_{RL}	V_{RH}	$V_{DD}A$
B	$V_{SS}X$	$V_{SS}X$	PG2	PG15	PA0	PA4	TMS	TDO	PD9	PH15	PE13	PH12	PE10	PH9	$V_{DD}A$	PH8
C	PG5	PG3	PI0	PG1	PA1	PA3	PA6	$V_{DD}2.5$	$V_{DD}X$	PD6	PH13	PE11	$V_{DD}A$	PE8	PE7	PH7
D	PG9	PG8	PG4	PI2	PI1	$V_{SS}2.5$	$V_{SS}2.5$	PD10	PD8	PD7	$V_{SS}A$	$V_{SS}A$	PH10	PE9	PE6	PH6
E	PG6	PG11	PG10	PI3									PE4	PE5	PH5	PH4
F	PC0	PG7	PC1	$V_{SS}X$									PE2	PE3	PH3	PH2
G	PB0	PC2	PC3	PI4			$V_{SS}X$	$V_{SS}X$	$V_{SS}X$	$V_{SS}X$			PH0	PH1	PE1	PE0
H	PB3	PB2	PB1	$V_{DD}X$			$V_{SS}X$	$V_{SS}X$	$V_{SS}X$	$V_{SS}X$			PA8	PA9	PA7	PA10
J	PB5	PB6	PB4	PI5			$V_{SS}X$	$V_{SS}X$	$V_{SS}X$	$V_{SS}X$			PD5	PA12	PA11	PC15
K	PB7	PB8	PF15	PI6			$V_{SS}X$	$V_{SS}X$	$V_{SS}X$	$V_{SS}X$			PC13	PC12	PC14	$V_{DD}X$
L	PF14	PF13	PC4	PI7									PD13	PD14	PD15	PD4
M	PF12	PC5	PC6	$V_{SS}X$									$V_{SS}X$	$\overline{TA}$ / $\overline{AS}$	PD3	PD2
N	PF11	PF10	PC7	PI8	$V_{SS}R$	$V_{SS}R$	$V_{SS}2.5$	$V_{SS}2.5$	$V_{SS}PLL$	$V_{SS}PLL$	PI12	PI13	PI14	PB11	PB14	PB15
P	PF9	PF8	PI9	PF5	PC8	PC10	$V_{DD}X$	$V_{DD}2.5$	$V_{DD}R$	$V_{DD}X$	PA15	PD11	PD12	PI15	PB12	PB13
R	PF7	PI10	PF6	PF3	PF1	PC9	PG12	PG13	$V_{SS}X$	$V_{SS}X$	TEST	PA13	PD1	PB10	PI11	$V_{SS}X$
T	$V_{SS}X$	$V_{SS}X$	PF4	PF2	PF0	PC11	$\overline{RESET}$	$V_{DD}PLL$	XFC	EXTAL	XTAL	PA14	PD0	PB9	$V_{SS}X$	$V_{SS}X$

Figure 23. Pin Assignments for MAC7136 in 208-pin MAP BGA

5 Mechanical Information

As indicated in Table 2, MAC7100 Family devices are available in several packages. Please refer to the freescale.com web site for the most up-to-date package availability and mechanical information. The table below lists available package identifiers and Freescale document numbers for reference.

Table 39. Package Identifiers and Mechanical Specifications

Package Type	Case Identifier	Mechanical Specification Document
100-lead LQFP	983-02	98ASS23308W
112-lead LQFP	987-02	98ASS23330W
144-lead LQFP	918-03	98ASS23177W
208-lead MAP BGA	1159A-01	98ARS23882W

Revision History

<table>
<tr><th>Version No.
Release Date</th><th>Description of Changes</th><th>Page Numbers</th></tr>
<tr><td>v0.1
29-Oct-03</td><td>First public customer release (preliminary).</td><td></td></tr>
<tr><td>v1.0
14-Sep-04</td><td>General
• Converted to Freescale identity, with blue cross-reference highlights for enhanced PDF navigation, and miscellaneous updates for presentation consistency.
• The order of Section 3.5 and Section 3.6 were reversed for better content flow. This has caused specification numbering to change as detailed below.

Note: Content consolidation and reorganization has resulted in the following table and specification number changes (the first spec number of each table is shown):

<table>
<tr><th>Table Title</th><th>Rev. 1.0</th><th>Rev. 0.1</th></tr>
<tr><td>5.0 V I/O Characteristics</td><td>Table 8 D1a</td><td>Table 15 F1</td></tr>
<tr><td>3.3 V I/O Characteristics</td><td>Table 9 E1a</td><td>Table 16 G1</td></tr>
<tr><td>Section 3.6, “Power Dissipation and Thermal Characteristics”</td><td>Table 10 to Table 14</td><td>Table 7 to Table 11</td></tr>
<tr><td>MAC71x1/6 Device Supply Current Characteristics – 40 MHz</td><td>Table 15 F1</td><td>Table 12 D1a</td></tr>
<tr><td>MAC71x1/6 Device Supply Current Characteristics – 50 MHz</td><td>Table 16 G1</td><td>N/A</td></tr>
<tr><td>VREG Operating Conditions</td><td>Table 17 H1</td><td>Table 13 E1</td></tr>
<tr><td>VREG Recommended Load Capacitances</td><td>Table 18</td><td>Table 14</td></tr>
<tr><td>Oscillator Characteristics</td><td>Table 19 J1a</td><td>Table 17 H1a</td></tr>
<tr><td>PLL Characteristics</td><td>Table 20 K1</td><td>Table 18 J1</td></tr>
<tr><td>Crystal Monitor Time-Outs</td><td>Table 21</td><td>Table 19</td></tr>
<tr><td>CRG Maximum Clock Quality Check Timings</td><td>Table 22</td><td>Table 20</td></tr>
<tr><td>CRG Startup Characteristics</td><td>Table 23 L1</td><td>Table 21 K1</td></tr>
<tr><td>External Bus Input Timing Specifications</td><td>Table 24 M1</td><td>Table 22 L1</td></tr>
<tr><td>External Bus Output Timing Specifications</td><td>Table 25 M6a</td><td>Table 23 L6a</td></tr>
<tr><td>ATD Operating Characteristics in 5.0 V Range</td><td>Table 26 N1</td><td>Table 24 M1</td></tr>
<tr><td>ATD Operating Characteristics in 3.3 V Range</td><td>Table 27 P1</td><td>Table 25 N1</td></tr>
<tr><td>ATD Electrical Characteristics</td><td>Table 28 Q1</td><td>Table 26 P1</td></tr>
<tr><td>ATD Conversion Performance in 5.0 V Range</td><td>Table 29 R1</td><td>Table 27 Q1</td></tr>
<tr><td>ATD Conversion Performance in 3.3 V Range</td><td>Table 30 S1</td><td>Table 28 R1</td></tr>
<tr><td>ATD Electrical Characteristics (Operating)</td><td>N/A</td><td>Table 29 S1</td></tr>
<tr><td>ATD Performance Specifications</td><td>N/A</td><td>Table 30 T1</td></tr>
<tr><td>ATD Timing Specifications</td><td>N/A</td><td>Table 31 U1</td></tr>
<tr><td>ATD External Trigger Timing Specifications</td><td>Table 31 T1</td><td>Table 32 V1</td></tr>
<tr><td>SPI Master Mode Timing Characteristics</td><td>Table 32 U1a</td><td>Table 33 W1a</td></tr>
<tr><td>SPI Slave Mode Timing Characteristics</td><td>Table 33 V1a</td><td>Table 34 X1a</td></tr>
<tr><td>FlexCAN Wake-up Pulse Characteristics</td><td>Table 34 W1</td><td>Table 35 Y1</td></tr>
<tr><td>CFM Timing Characteristics</td><td>Table 35 X1</td><td>Table 36 Z1</td></tr>
<tr><td>NVM Reliability Characteristics</td><td>Table 36 X9b</td><td>Table 37 Z10</td></tr>
</table>
</td><td>7, 8</td></tr>
<tr><td></td><td>Section 2, “Ordering Information”
• Added Table 1, mask set information
• Updated Table 2 with expanded port pin counts, MAC71x2 and MAC71x6 family members
• Pin assignment changes for mask set L47W devices:
— In Table 37, PB10 / PCS5_B / PCSS_B changed to pin 57, footnote for L49P</td><td>2
3

36</td></tr>
</table>

Revision History (continued)

Version No. Release Date	Description of Changes	Page Numbers
v1.0 14-Sep-04 (continued)	**Section 3, "Electrical Characteristics"**	
	• Section 3.2, "Absolute Maximum Ratings"	
	— A1a renamed to $V_{DD}X$	4
	— A4 "rating" changed to Analog (from ATD)	4
	— A9 minimum changed to –0.3	5
	— A12 maximum value removed, footnote reference added	5
	— Table 8, Table 9 footnotes added regarding $V_{DD}5/V_{SS}5$	7, 8
	• Section 3.4, "Operating Conditions"	
	— C1 renamed to $V_{DD}X$	6
	— C4 added (C5 to C11b renumbered)	6
	— C8 maximum changed from 40 MHz to 50 MHz	6
	• Section 3.5, "Input/Output Characteristics"	
	— Table 8 spec D4 updated (from TBD)	7
	— Table 9 spec E4 changed to 1 µA to match D4	8
	• Section 3.6, "Power Dissipation and Thermal Characteristics"	
	— Reworked Equation 1 through Equation 4 and supporting text	9
	— Section 3.6.1 and Table 10 name changed from "Power Dissipation..."	10
	• Section 3.7, "Power Supply"	
	— Added MAC71*x*1 designation and footnotes to Table 15 / Table 16	12
	— Table 15 designated for 40 MHz, and	
	– Numerous TBD entries replaced with values	
	– Run Supply Current collapsed from fifteen spec items to one	
	– Removed separate Core/Regulator/Pins specs for Run/Pseudo Stop/Stop modes	
	– F1 and F3 descriptions changed	
	– F1, F2, F3 and F4 values updated	
	— Table 16 added for 50 MHz specifications	12
	— Table 17, deleted I_{REG} spec (Regulator Current in Reduced Power, Shutdown Modes)	13
	— Table 18, $V_{DD}2.5$ load capacitance typical changed, with clarification footnote	14
	• Section 3.8, "Clock and Reset Generator"	
	— Table 19 updates	15
	– Changed specs J1b and J6 maximum from 40 MHz to 50 MHz	
	– Reversed polarity of $\overline{\text{XCLKS}}$ reference in footnote (3)	
	– J1b maximum changed to 40 MHz	
	– V_{DCBIAS} removed	
	– Added footnote to define t_{fsys} as 1 ÷ f_{SYS} for use elsewhere in the document	
	— Updated Section 3.8.2, "PLL Filter Characteristics"	16
	— Table 20 updates	18
	– Changed spec K3 maximum from 40 MHz to 50 MHz	
	– Added footnote to define t_{fsys} as 1 ÷ f_{SYS} for use elsewhere in the document	
	— Table 23 updates	19
	– Removed V_{PORR} and V_{PORA}, as they duplicated H6	
	– Removed t_{WRS}	
	• Section 3.9, "External Bus Timing"	
	— Table 24 updates	20
	– M1 minimum changed from 25 ns to 20 ns (Figure 6 also updated)	
	– Reworded footnote (1)	
	– Added footnote (2) to define t_{CYC} as 1 ÷ CLKOUT	
	— Table 25 updates	21
	– Added footnote (1)	
	– Consolidated previous NOTES into footnote (2), (Figure 7, Figure 8 also updated)	

Revision History (continued)

Version No. Release Date	Description of Changes	Page Numbers
v1.0 14-Sep-04 (continued)	**Section 3, "Electrical Characteristics" (continued)** • Section 3.10, "Analog-to-Digital Converter" — Rev. 0.1 redundant and superfluous content deleted – Section 3.10.3, "ATD Electrical Specifications," (included Table 29 and Table 30) – Table 31, "ATD Performance Specifications" (redundant with v0.1 Table 27 and Table 28, now Table 29 and Table 30) — Table 26 updates – Deleted previous spec M6 – Changed spec N7 and N8 values — Table 27 updates – Deleted previous spec N6 – Changed spec P7 and P8 values – Changed spec P2 and footnote (1) to specify 3.15 V — Table 28 updates – Changed spec Q2 parameter classification from T to C and 10 pF and 22 pF values moved from maximum to typical — Table 29 updates – Operating conditions $V_{DD}A$ minimum changed to 4.5 V – V_{REF} description moved from "conditions" header to new footnote (1) — Table 30 updates – Operating conditions $V_{DD}A$ minimum changed to 3.15 V – V_{REF} description moved from "conditions" header to new footnote (1) — Table 31 updates – Spec T1 description clarified, max removed, min added with footnote – Spec T2 modified to show both edge- and level-sensitive modes — Figure 10 modified to remove "Max Frequency" label and clearly separate edge- and level-sensitive mode timing examples • Section 3.11, "Serial Peripheral Interface" — Table 32 updates – Changed specs U1a, U1b and U4 to use f_{IPS} and t_{IPS} for clarity and consistency with MAC7100RM – Changed U1a max to ½ and U1b min to 2 to account for the DBR bit — Table 33 updates – Changed specs V1a, V1b, V2, V3, V4, V7, V8 to use f_{IPS} and t_{IPS} for clarity and consistency with MAC7100RM – Changed V1a max to ½ and V1b min to 2 to account for the DBR bit • Section 3.13, "Common Flash Module" — Significant rework to match MAC7100RM clock naming, references and timing calculations for clarity and consistency — Changed X1 maximum from 40 MHz to 50 MHz (Table 35)	24 24 24 25 26 26 28 28 29 29 32 to 35 34

Revision History (continued)

Version No. Release Date	Description of Changes	Page Numbers
v1.0 14-Sep-04 (continued)	**Section 4, "Device Pin Assignments"** • Table 37 and Table 38 added • Added PD2 label / footnote to Figure 15, Figure 17, Figure 19, Figure 20 and Figure 22 • Section 4.2, "MAC7142 Pin Diagram" / Figure 16 added • Section 4.3, "MAC7121 / MAC7126 Pin Diagram" / Figure 17 updated — PB10 / PCS5_B / PCSS_B bonded out on pin 57, footnote for L49P — Added MAC71*x*6 device information • Section 4.4, "MAC7122 Pin Diagram" / Figure 18 added • Section 4.5, "MAC7101 / MAC7106 Pin Diagram" / Figure 19 updated — Added MAC71*x*6 device information • Section 4.6, "MAC7111 / MAC7116 Pin Diagram" / Figure 20 updated — Added $\overline{AS}$ to $\overline{TA}$ pin — Added MAC71*x*6 device information • Section 4.7, "MAC7112 Pin Diagram" / Figure 21 added • Section 4.8, "MAC7131 Pin Diagram" / Figure 22 corrected, updated — Changed pins C8 & P8 from $V_{SS}2.5$ to $V_{DD}2.5$ — Changed pin T8 from $V_{SS}PLL$ to $V_{DD}PLL$ — Added $\overline{AS}$ to $\overline{TA}$ pin • Section 4.9, "MAC7136 Pin Diagram" / Figure 23 added	 36, 40 41, 43, 45, 46, 48 42 43 44 45 46 47 48 49
v1.1 **1-Dec-04**	**Section 3, "Electrical Characteristics"** • Section 3.7, "Power Supply" — Table 15 spec F4 –40° C and 25° C max value changed — Table 16 spec G4 –40° C and 25° C max value changed • Section 3.8, "Clock and Reset Generator" — Table 19 spec J3 typical TBD entry replaced with value — Table 20 specs K15 and K16 maximum TBD entries replaced with values	 12 12 15 18
v1.1.1 **3-Dec-04**	**Section 3, "Electrical Characteristics"** • Section 3.7, "Power Supply" — Table 15 spec F3 –40° C, 25° C and 125° C typ and max values and unit changed — Table 16 spec G3 –40° C, 25° C and 125° C typ and max value and unit changed	 12 12
v1.2 **10-Feb--06**	**Section 1, "Overview"** • Moved 71x6 device numbers from footnote to "covered" list **Section 2, "Ordering Information"** • Added AF, AG and VM package identifiers to Figure 1 • Added 1L38Y to Table 1 **Section 3, "Electrical Characteristics"** • Replaced TBD values in Table 15 and Table 16 with final qualification data, changed table titles and footnotes to reflect 71x6 inclusion. **Section 5, "Mechanical Information"** • Removed obsolete package diagrams, replaced with document IDs available on web site.	 1 2 2 12 50

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