

μ PD70F3826, 70F3827, 70F3828, 70F3829, 70F3830, 70F3831, 70F3832, 70F3833, 70F3834, 70F3835, 70F3836, 70F3837

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–V850ES/JE3-E, V850ES/JF3-E, V850ES/JG3-E– RENESAS MCU

Description

The μ PD70F3826, 70F3827, 70F3828, 70F3829 (V850ES/JF3-E), and μ PD70F3830, 70F3831, 70F3832, 70F3833 (V850ES/JF3-E), and μ PD70F3834, 70F3835, 70F3836, 70F3837 (V850ES/JG3-E) are products of the V850 32-bit single-chip microcontrollers, and include peripheral functions such as ROM/RAM, timer/counters, serial interfaces, an A/D converter, a DMA controller, a CAN controller, a USB function controller, and an Ethernet controller.

In addition to their high real-time responsiveness and one-clock-pitch execution of instructions, the V850ES/JE3-E, V850ES/JF3-E, and V850ES/JG3-E include instructions executed via a hardware multiplier, saturation instructions, and bit manipulation instructions.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850ES/JE3-E, V850ES/JF3-E, V850ES/JG3-E Hardware User's Manual: To be prepared

V850ES Architecture User's Manual:

U15943E

Features

- Number of instructions: 83
- Minimum instruction execution time:
20 ns (@ 50 MHz operation with main clock (fx))
- Clock
 - Main clock oscillation: $f_x = 3$ to 6.25 MHz
 - Subclock oscillation: $f_{XT} = 32.768$ kHz
 - Internal oscillation: $f_R = 220$ kHz (TYP.)
- General-purpose registers: 32 bits \times 32 registers
- Instruction set:
Signed multiplication, saturation operations, 32-bit shift instructions, bit manipulation instructions, load/store instructions
- Memory space:
64 MB linear address space
- Internal memory
Flash memory: 64/128/256 KB
RAM: 32/48/64 KB
(Including 16 KB of data RAM area)
- I/O lines Total: 26/42/62
- Interrupts and exceptions
Non-maskable interrupts: 2 sources
Maskable interrupts: 63/78/85 sources
- Timer/counters
 - 16-bit timer/event counter AA (TAA): 5 channels
 - 16-bit timer/event counter AB (TAB): 1 channel
 - Motor control function supported
 - 16-bit interval timer M (TMM): 4 channels
 - 16-bit encoder timer T (TMT): 1 channel
- Real-time counter: 1 channel
- Watchdog timer: 1 channel
- Real-time output function: 6 channels
- A/D converter: 10-bit resolution \times 10/10 channels
- Ethernet controller: 1 channel
- USB function controller: 1 channel
- Serial interface
 - CAN :1 channel (μ PD70F3829, 70F3833, 70F3837 only)
 - Asynchronous serial interface C(UARTC): 3/4 channels
 - Clocked serial interface F(CSIF): 2/3/5 channels
 - I²C bus interface: 2/3 channels
- DMA controller: 4 channels
- Power save function:
HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE mode
- On-chip debug function
- Package: 64-pin LQFP (V850ES/JE3-E)
64-pin WQFN (V850ES/JE3-E)
80-pin LQFP (V850ES/JF3-E)
100-pin LQFP (V850ES/JG3-E)
113-pin FBGA (Under planing)
- Operating supply voltage: 2.85 to 3.6 V

Function list (V850ES/JE3-E)

| Generic Name | | V850ES/JE3-E | | | |
|-------------------------------|------------------------------------|--|------------|------------|------------|
| Product Name | | μPD70F3826 | μPD70F3827 | μPD70F3828 | μPD70F3829 |
| Internal memory | Flash memory | 64 KB | 128 KB | 256 KB | 256 KB |
| | Internal RAM | 16 KB | 32 KB | 48 KB | 48 KB |
| | Data RAM | 16 KB | 16 KB | 16 KB | 16 KB |
| Memory space | | 64 MB | | | |
| General-purpose register | | 32 bits × 32 registers | | | |
| Clocks | Main clock oscillation | PLL mode : f _x = 3 to 6.25 MHz, f _{xx} = 24 to 50 MHz (multiplication by 8) Clock through mode : f _x = 3 to 6.25 MHz (internal : f _{xx} = 3 to 6.25 MHz) | | | |
| | Subclock oscillation | f _{xT} = 32.768 kHz | | | |
| | Internal oscillation | f _R = 220 kHz (TYP.) | | | |
| | Minimum instruction execution time | 20 ns (@ 50 MHz operation with main system clock (f _{xx})) | | | |
| I/O ports | | I/O: 26 (5 V tolerant : 12) | | | |
| Timer | 16-bit TAA | 5 channels (among which two channels have the interval function only) | | | |
| | 16-bit TAB | - | | | |
| | 16-bit TMM | 4 channels | | | |
| | 16-bit TMT | 1 channel (Interval function only) | | | |
| | Motor control | - | | | |
| | Watch timer | 1 channel (RTC) | | | |
| | WDT | 1 channel | | | |
| Real-time output function | | 6 bits × 1 channel | | | |
| 10-bit A/D converter | | 10 channels | | | |
| Serial interface | CSIF/UARTC | 1 channel | | | |
| | CSIF/UARTC/I ² C | 1 channel | | | |
| | CSIF | - | | | |
| | UARTC/I ² C | 1 channel | | | - |
| | UARTC/I ² C/CAN | - | - | - | 1 channel |
| USB function | | 1 channel | | | |
| Ethernet controller | | 1 channel | | | |
| DMA controller | | 4 channels (transfer target: on-chip peripheral I/O, internal RAM) | | | |
| Interrupt source | External ^{Note 1, 2} | 7(7) | 7(7) | 7(7) | 7(7) |
| | Internal | 54 | 54 | 54 | 58 |
| Power-save function | | HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes | | | |
| Reset factor | | RESET pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI) | | | |
| On-chip debugging | | MINICUBE®, MINICUBE2 supported | | | |
| Operating supply voltage | | 2.85 to 3.6 V | | | |
| Operating ambient temperature | | -40 to +85°C | | | |
| Package | | 64-pin plastic LQFP (fine pitch) (10 × 10 mm), 64-pin plastic WQFN (9 × 9 mm), | | | |

- Notes**
1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.
 2. Include NMI.

Function list (V850ES/JF3-E)

| Generic Name | | V850ES/JF3-E | | | |
|-------------------------------|------------------------------------|--|------------|------------|------------|
| Product Name | | μPD70F3830 | μPD70F3831 | μPD70F3832 | μPD70F3833 |
| Internal memory | Flash memory | 64 KB | 128 KB | 256 KB | 256 KB |
| | Internal RAM | 16 KB | 32 KB | 48 KB | 48 KB |
| | Data RAM | 16 KB | 16 KB | 16 KB | 16 KB |
| Memory space | | 64 MB | | | |
| General-purpose register | | 32 bits × 32 registers | | | |
| Clocks | Main clock oscillation | PLL mode : $f_x = 3$ to 6.25 MHz, $f_{xx} = 24$ to 50 MHz (multiplication by 8) Clock through mode : $f_x = 3$ to 6.25 MHz (internal : $f_{xx} = 3$ to 6.25 MHz) | | | |
| | Subclock oscillation | $f_{XT} = 32.768$ kHz | | | |
| | Internal oscillation | $f_R = 220$ kHz (TYP.) | | | |
| | Minimum instruction execution time | 20 ns (@ 50 MHz operation with main system clock (f_{xx})) | | | |
| I/O ports | | I/O: 42 (5 V tolerant : 28) | | | |
| Timer | 16-bit TAA | 5 channels | | | |
| | 16-bit TAB | 1 channel | | | |
| | 16-bit TMM | 4 channels | | | |
| | 16-bit TMT | 1 channel | | | |
| | Motor control | 1 channel | | | |
| | Watch timer | 1 channel (RTC) | | | |
| | WDT | 1 channel | | | |
| Real-time output function | | 6 bits × 1 channel | | | |
| 10-bit A/D converter | | 10 channels | | | |
| Serial interface | CSIF/UARTC | 1 channel | | | |
| | CSIF/UARTC/I ² C | 2 channels | | | |
| | CSIF | - | | | |
| | UARTC/I ² C | 1 channel | | | - |
| | UARTC/I ² C/CAN | - | | | 1 channel |
| USB function | | 1 channel | | | |
| Ethernet controller | | 1 channel | | | |
| DMA controller | | 4 channels (transfer target: on-chip peripheral I/O, internal RAM) | | | |
| Interrupt source | External ^{Note 1, 2} | 19(19) | 19(19) | 19(19) | 19(19) |
| | Internal | 57 | 57 | 57 | 61 |
| Power-save function | | HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes | | | |
| Reset factor | | RESET pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI) | | | |
| On-chip debugging | | MINICUBE, MINICUBE2 supported | | | |
| Operating supply voltage | | 2.85 to 3.6 V | | | |
| Operating ambient temperature | | -40 to +85°C | | | |
| Package | | 80-pin plastic LQFP (fine pitch) (12 × 12 mm) | | | |

- Notes**
1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.
 2. Include NMI.

Function list (V850ES/JG3-E)

| Generic Name | | V850ES/JG3-E | | | |
|-------------------------------|------------------------------------|--|------------|------------|------------|
| Product Name | | μPD70F3834 | μPD70F3835 | μPD70F3836 | μPD70F3837 |
| Internal memory | Flash memory | 64 KB | 128 KB | 256 KB | 256 KB |
| | Internal RAM | 16 KB | 32 KB | 48 KB | 48 KB |
| | Data RAM | 16 KB | 16 KB | 16 KB | 16 KB |
| Memory space | | 64 MB | | | |
| General-purpose register | | 32 bits × 32 registers | | | |
| Clocks | Main clock oscillation | PLL mode : f _x = 3 to 6.25 MHz, f _{xx} = 24 to 50 MHz (multiplication by 8) Clock through mode : f _x = 3 to 6.25 MHz (internal : f _{xx} = 3 to 6.25 MHz) | | | |
| | Subclock oscillation | f _{xT} = 32.768 kHz | | | |
| | Internal oscillation | f _R = 220 kHz (TYP.) | | | |
| | Minimum instruction execution time | 20 ns (@ 50 MHz operation with main system clock (f _{xx})) | | | |
| I/O ports | | I/O: 62 (5 V tolerant : 35) | | | |
| Timer | 16-bit TAA | 5 channels | | | |
| | 16-bit TAB | 1 channel | | | |
| | 16-bit TMM | 4 channels | | | |
| | 16-bit TMT | 1 channel | | | |
| | Motor control | 1 channel | | | |
| | Watch timer | 1 channel (RTC) | | | |
| | WDT | 1 channel | | | |
| Real-time output function | | 6 bits × 1 channel | | | |
| 10-bit A/D converter | | 10 channels | | | |
| Serial interface | CSIF/UARTC | 1 channel | | | |
| | CSIF/UARTC/I ² C | 2 channels | | | |
| | CSIF | 2 channels | | | |
| | UARTC/I ² C | 1 channel | | | – |
| | UARTC/I ² C/CAN | – | | | 1 channel |
| USB function | | 1 channel | | | |
| Ethernet controller | | 1 channel | | | |
| DMA controller | | 4 channels (transfer target: on-chip peripheral I/O, internal RAM) | | | |
| Interrupt source | External ^{Note 1, 2} | 22(22) | 22(22) | 22(22) | 22(22) |
| | Internal | 61 | 61 | 61 | 65 |
| Power-save function | | HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes | | | |
| Reset factor | | RESET pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI) | | | |
| On-chip debugging | | MINICUBE, MINICUBE2 supported | | | |
| Operating supply voltage | | 2.85 to 3.6 V | | | |
| Operating ambient temperature | | –40 to +85°C | | | |
| Package | | 100-pin plastic LQFP (fine pitch) (14 × 14 mm), 113-pin plastic FBGA ^{Note3} | | | |

- Notes**
1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.
 2. Include NMI.
 3. Under planning.

APPLICATIONS

- Applications that require Ethernet controller
Home audio, printers, and scanners.

ORDERING INFORMATION

- V850ES/JE3-E

| Part Number | Package | On-Chip Flash Memory |
|---------------------|--|----------------------|
| μPD70F3826GB-GAH-AX | 64-pin plastic LQFP (fine pitch) (10 × 10) | 64 KB |
| μPD70F3827GB-GAH-AX | 64-pin plastic LQFP (fine pitch) (10 × 10) | 128 KB |
| μPD70F3828GB-GAH-AX | 64-pin plastic LQFP (fine pitch) (10 × 10) | 256 KB |
| μPD70F3829GB-GAH-AX | 64-pin plastic LQFP (fine pitch) (10 × 10) | 256 KB |
| μPD70F3826K8-6B4-AX | 64-pin plastic WQFN (9 × 9) | 64 KB |
| μPD70F3827K8-6B4-AX | 64-pin plastic WQFN (9 × 9) | 128 KB |
| μPD70F3828K8-6B4-AX | 64-pin plastic WQFN (9 × 9) | 256 KB |
| μPD70F3829K8-6B4-AX | 64-pin plastic WQFN (9 × 9) | 256 KB |

- V850ES/JF3-E

| Part Number | Package | On-Chip Flash Memory |
|---------------------|--|----------------------|
| μPD70F3830GK-GAK-AX | 80-pin plastic LQFP (fine pitch) (12 × 12) | 64 KB |
| μPD70F3831GK-GAK-AX | 80-pin plastic LQFP (fine pitch) (12 × 12) | 128 KB |
| μPD70F3832GK-GAK-AX | 80-pin plastic LQFP (fine pitch) (12 × 12) | 256 KB |
| μPD70F3833GK-GAK-AX | 80-pin plastic LQFP (fine pitch) (12 × 12) | 256 KB |

- V850ES/JG3-E

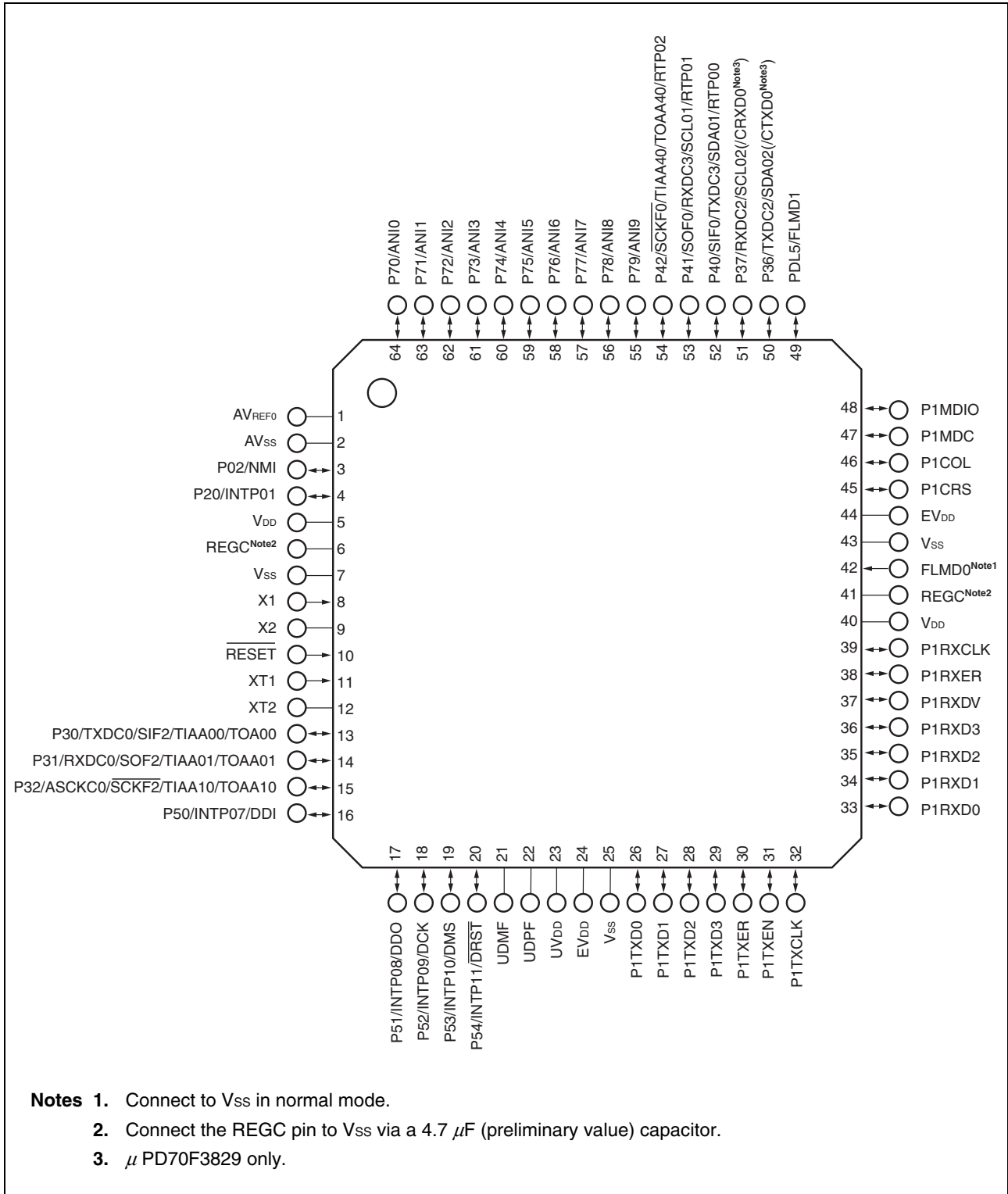
| Part Number | Package | On-Chip Flash Memory |
|-------------------------------------|---|----------------------|
| μPD70F3834GC-UEU-AX | 100-pin plastic LQFP (fine pitch) (14 × 14) | 64 KB |
| μPD70F3835GC-UEU-AX | 100-pin plastic LQFP (fine pitch) (14 × 14) | 128 KB |
| μPD70F3836GC-UEU-AX | 100-pin plastic LQFP (fine pitch) (14 × 14) | 256 KB |
| μPD70F3837GC-UEU-AX | 100-pin plastic LQFP (fine pitch) (14 × 14) | 256 KB |
| μPD70F3837F1-CAH-AX ^{Note} | 113-pin plastic FBGA (8 × 8) | 256 KB |

Note Under planning

Remark The V850ES/Jx3-E microcontrollers are lead-free products.

PIN CONFIGURATION

- V850ES/JE3-E
 64-pin plastic LQFP (fine pitch) (10 × 10)
 μPD70F3826GB-GAH-AX μPD70F3827GB-GAH-AX
 μPD70F3828GB-GAH-AX μPD70F3829GB-GAH-AX



• V850ES/JE3-E

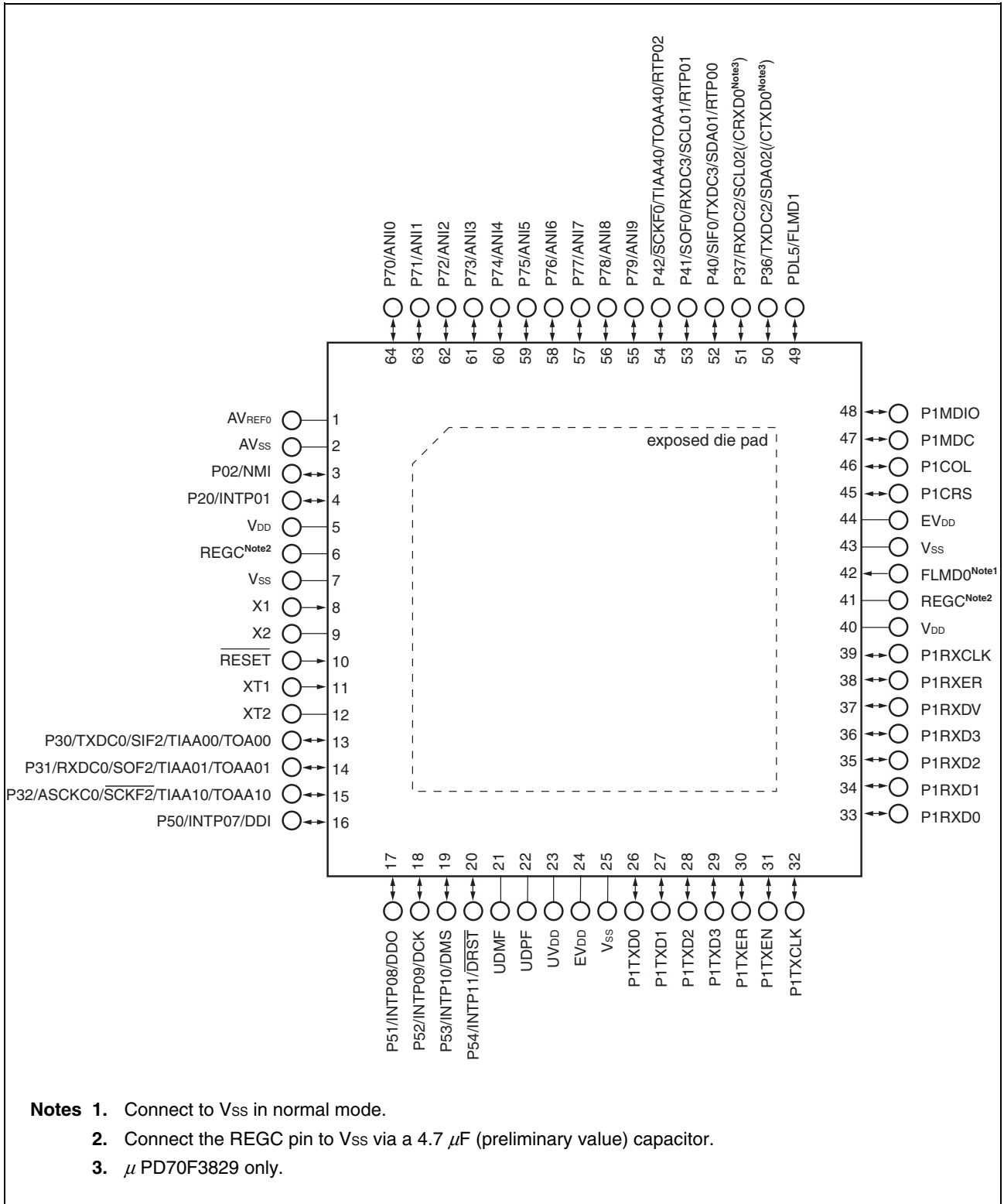
64-pin plastic WQFN (9 × 9)

μPD70F3826K8-6B4-AX

μPD70F3827K8-6B4-AX

μPD70F3828 K8-6B4-AX

μPD70F3829K8-6B4-AX



• V850ES/JF3-E

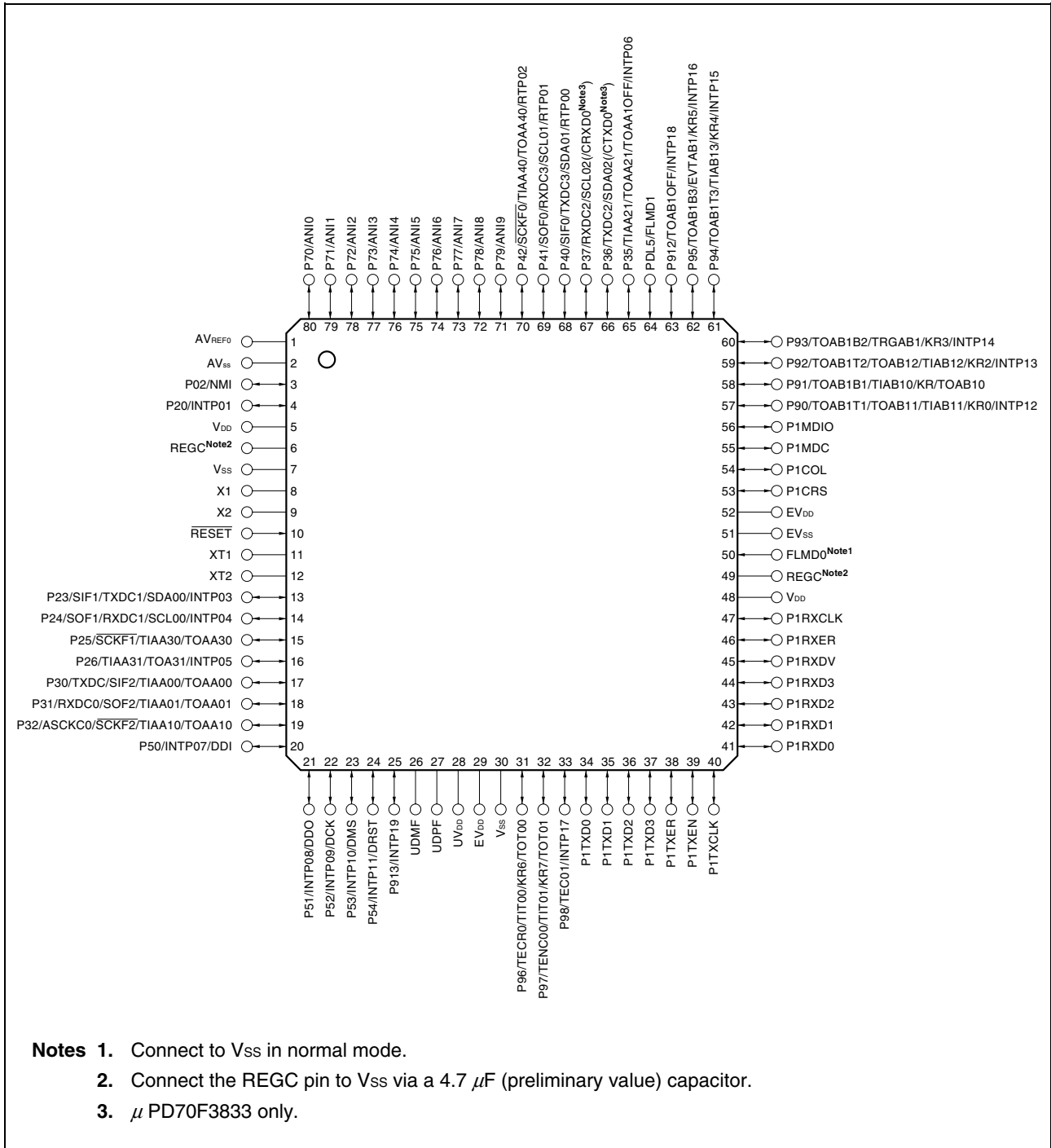
80-pin plastic LQFP (fine pitch) (12 × 12)

μPD70F3830GK-GAK-AX

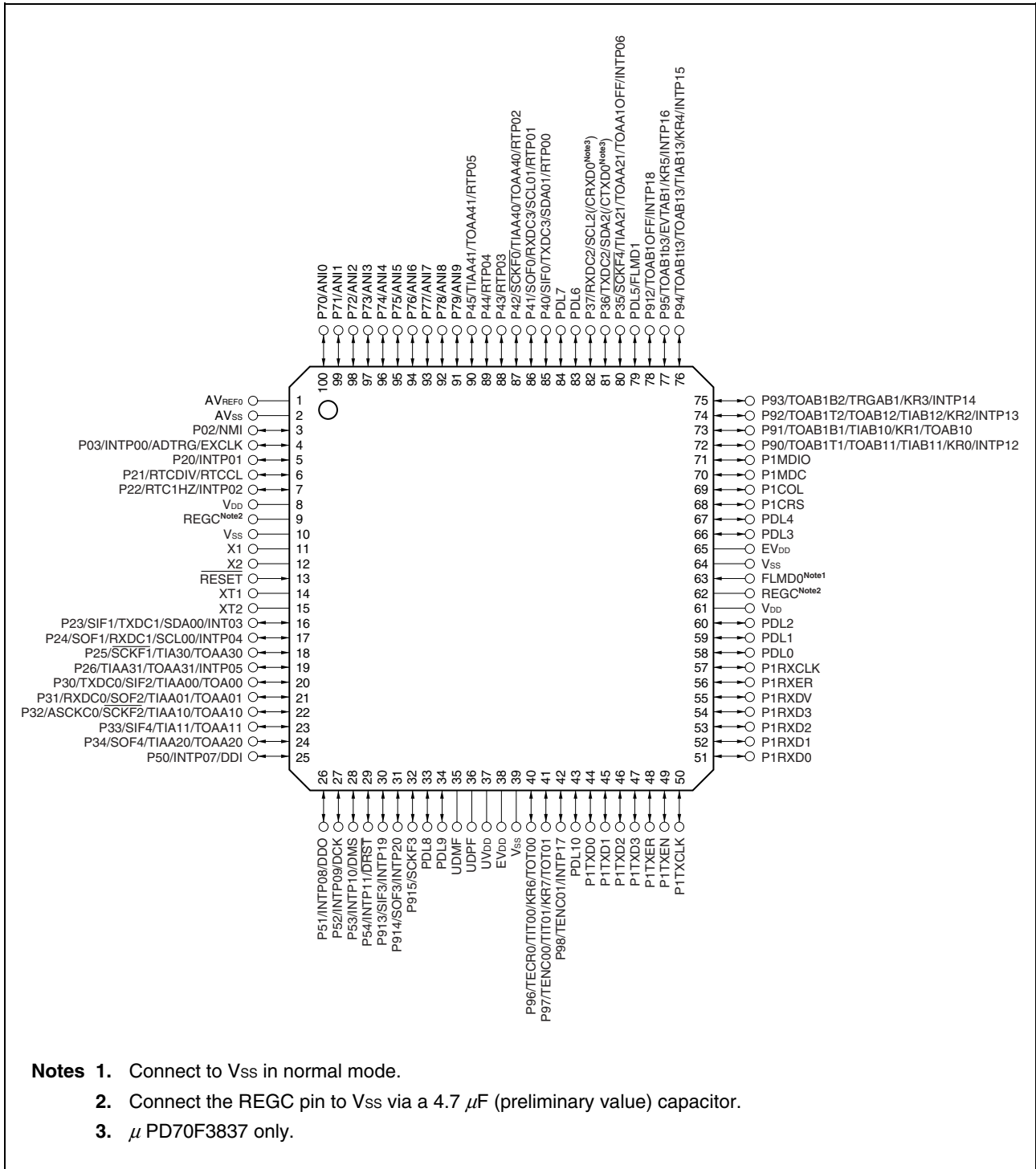
μPD70F3831GK-GAK-AX

μPD70F3832GK-GAK-AX

μPD70F3833GK-GAK-AX



- V850ES/JG3-E
 100-pin plastic LQFP (fine pitch) (14 × 14)
 μPD70F3834GC-UEU-AX μPD70F3835GC-UEU-AX
 μPD70F3836GC-UEU-AX μPD70F3837GC-UEU-AX



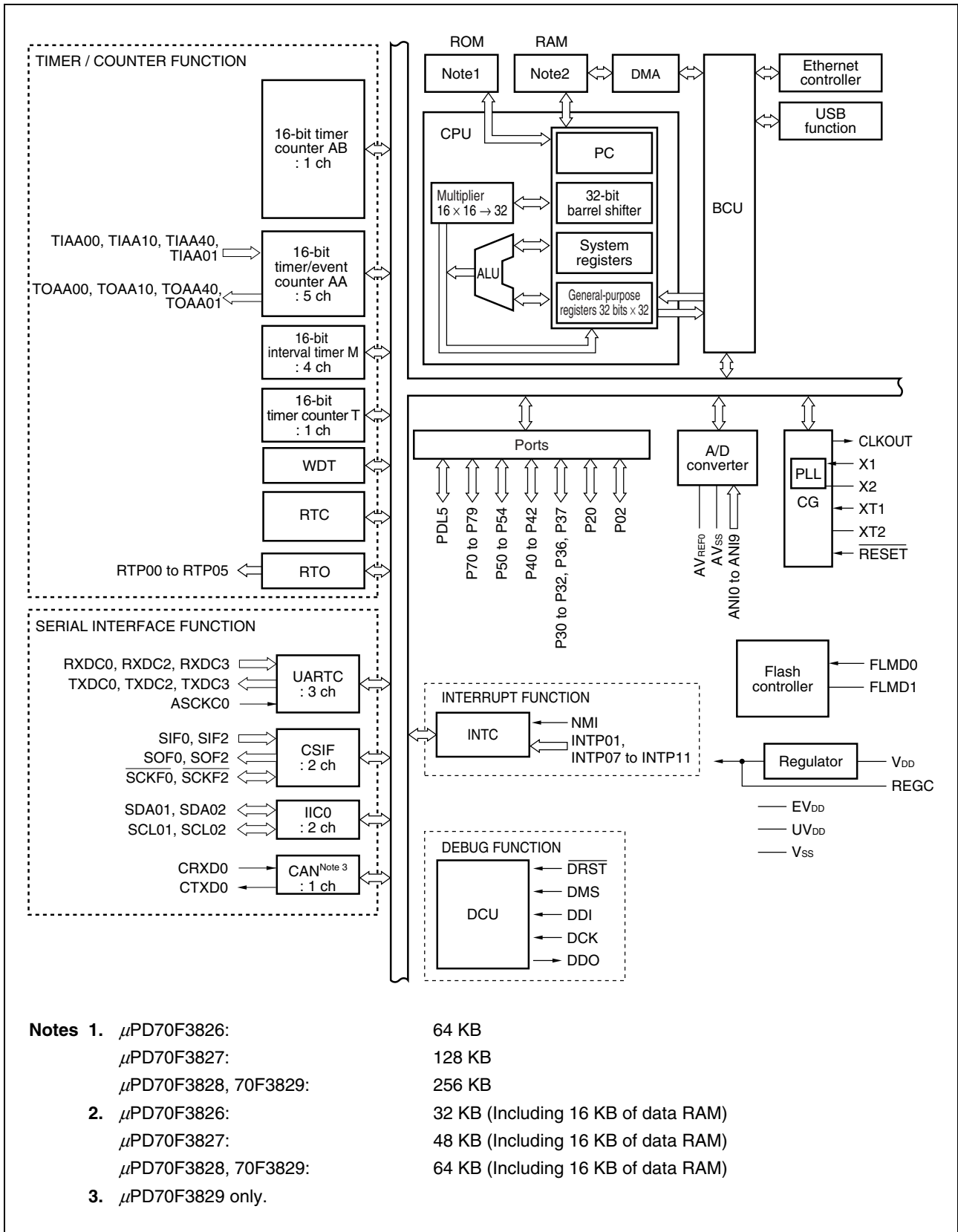
- Notes**
1. Connect to Vss in normal mode.
 2. Connect the REGC pin to Vss via a 4.7 μF (preliminary value) capacitor.
 3. μPD70F3837 only.

PIN IDENTIFICATION

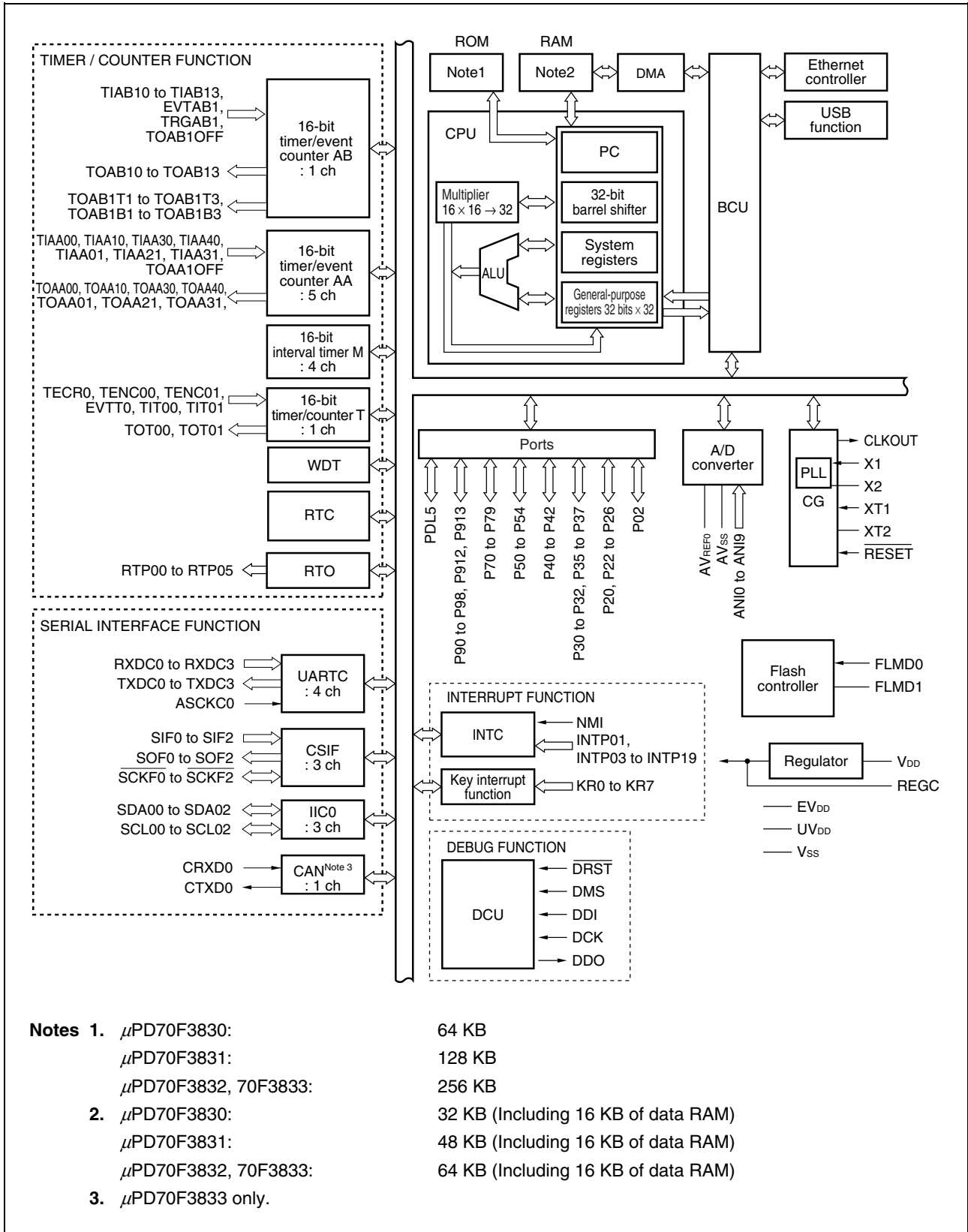
| | | | |
|-----------------------------|--------------------------------|--|-------------------------------|
| ADTRG: | A/D Trigger Input | RXDC0 to RXDC3 | Receive Data |
| ANI0 to ANI9: | Analog Input | $\overline{\text{SCKF0}}$ to $\overline{\text{SCKF4}}$: | Serial Clock |
| ASCKC0: | Asynchronous Serial Clock | SCL00 to SCL02: | Serial Clock |
| AVREF0: | Analog Reference Voltage | SDA00 to SDA02: | Serial Data |
| AVSS: | Grand for Analog Pin | SIF0 to SIF4: | Serial Input |
| CRXD0: | CAN Receive Data | SOF0 to SOF4: | Serial Output |
| CTXD0: | CAN Transmit Data | TECR0: | Timer Encoder Clear Input |
| DCK: | Debug Clock | TENC00, TENC01: | Timer Encoder Input |
| DDI: | Debug Data Input | TIAA00, TIAA01, | Timer Input |
| DDO: | Debug Data Output | TIAA10, TIAA11, | |
| DMS: | Debug Mode Select | TIAA20, TIAA21, | |
| $\overline{\text{DRST}}$: | Debug Reset | TIAA30, TIAA31, | |
| EVDD: | Power Supply for External Pin | TIAA40, TIAA41, | |
| EVTAB1: | Timer Event Count Input | TIAB10 to TIAB13, | |
| EXCLK | USB clock | TIT00, TIT01: | |
| FLMD0, FLMD1: | Flash Programming Mode | TOAA00, TOAA01, | Timer Output |
| INTP00 to INTP20: | External Interrupt Input | TOAA10, TOAA11, | |
| KR0 to KR7: | Key Return | TOAA20, TOAA21, | |
| NMI: | Non-maskable Interrupt Request | TOAA30, TOAA31, | |
| P02, P03: | Port0 | TOAA40, TOAA41, | |
| P1COL, P1CRS, | Ethernet PHY Interface | TOAB10 to TOAB13, | |
| P1MDC, P1MDIO, | | TOAB1B1 to TOAB1B3, | |
| P1RXCLK, | | TOAB1T1 to TOAB1T3, | |
| P1RXD0 to P1RXD3, | | TOT00, TOT01: | |
| P1RXDV, P1RXER | | TOAA1OFF, | Timer Output Off |
| P1TXCLK, | | TOAB1OFF | |
| P1TXD0 to P1TXD3, | | TRGAB1: | Timer Trigger Input |
| P1TXEN, P1TXER: | | TXDC0 to TXDC3: | Serial Output |
| P20 to P26 | Port2 | UDMF: | USB Data I/O (-) Function |
| P30 to P37: | Port3 | UDPF: | USB Data I/O (+) Function |
| P40 to P45: | Port4 | UVDD: | Power Supply for External USB |
| P50 to P54: | Port5 | VDD: | Power Supply |
| P70 to P79: | Port7 | VSS: | Ground |
| P90 to P98, | Port9 | X1, X2: | Crystal for Main Clock |
| P912 to P915: | | XT1, XT2: | Crystal for Sub-clock |
| PDL0 to PDL10: | Port DL | | |
| REGC: | Regulator Control | | |
| $\overline{\text{RESET}}$: | Reset | | |
| RTC1HZ, RTCCL, | Real-time Counter Clock Output | | |
| RTCDIV: | | | |
| RTP00 to RTP05: | Real-time Output Port | | |

INTERNAL BLOCK DIAGRAM

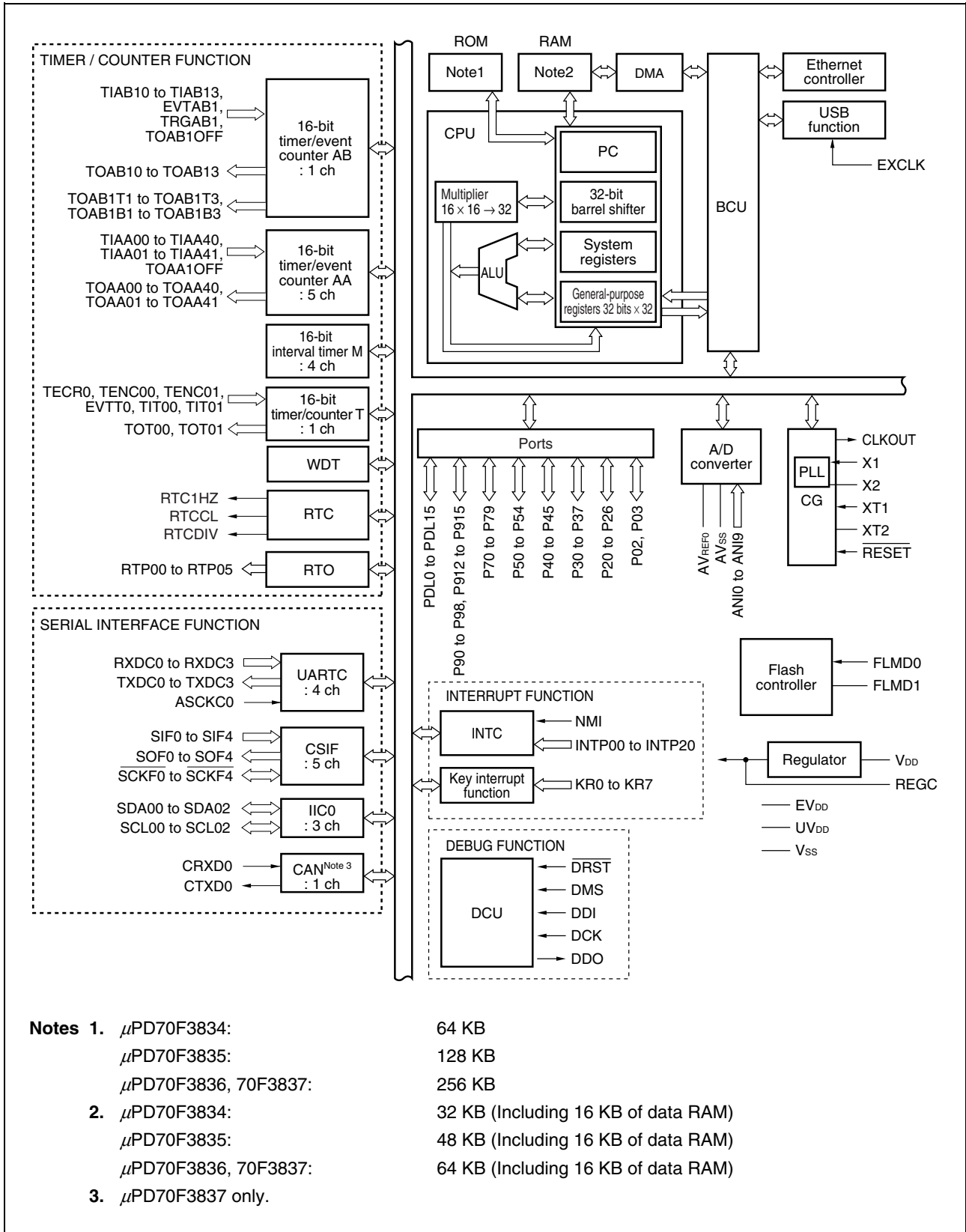
• V850ES/JE3-E



• V850ES/JF3-E



• V850ES/JG3-E



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1. PIN FUNCTIONS

1.1 Port Pins

(1/2)

| Pin Name | I/O | Function | Alternate Function | Pin number | | |
|----------|-----------------------------------|---|---|------------|-------|-------|
| | | | | JE3-E | JF3-E | JG3-E |
| P02 | I/O | Port 0 2-bit I/O port(V850ES/JG3-E) 1-bit I/O port(V850ES/JE3-E, V850ES/JF3-E) Input/output can be specified in 1-bit units. | NMI | 3 | 3 | 3 |
| P03 | | | INTP00/ADTRG/EXCLK | - | - | 4 |
| P20 | I/O | Port 2 7-bit I/O port(V850ES/JG3-E) 5-bit I/O port(V850ES/JF3-E) 1-bit I/O port(V850ES/JE3-E) Input/output can be specified in 1-bit units. | INTP01 | 4 | 4 | 5 |
| P21 | | | RTGDIV/RTCCCL | - | - | 6 |
| P22 | | | RTC1HZ/INTP02 | - | - | 7 |
| P23 | | | SIF1/TXDC1/SDA00/INTP03 | - | 13 | 16 |
| P24 | | | SOF1/RXDC1/SDL00/INTP04 | - | 14 | 17 |
| P25 | | | SCKF1/TIAA30/TOAA30 | - | 15 | 18 |
| P26 | | | TIAA31/TOAA31/INTP05 | - | 16 | 19 |
| P30 | I/O | Port 3 8-bit I/O port(V850ES/JG3-E) 6-bit I/O port(V850ES/JF3-E) 5-bit I/O port(V850ES/JE3-E) Input/output can be specified in 1-bit units. | TXDC0/SIF2/TIAA00/TOAA00 | 13 | 17 | 20 |
| P31 | | | RXDC0/SOF2/TIAA01/TOAA01 | 14 | 18 | 21 |
| P32 | | | ASCKC0/SCKF2/TIAA10/TOAA10 | 15 | 19 | 22 |
| P33 | | | SIF4/TIAA11/TOAA11 | - | - | 23 |
| P34 | | | SOF4/TIAA20/TOAA20 | - | - | 24 |
| P35 | | | SCKF4/TIAA21/TOAA21 /TOAA1OFF/INTP06 | - | - | 80 |
| | | | TIAA21/TOAA21/TOAA1OFF/INTP06 | - | 65 | - |
| P36 | | | TXDC2/SDA02/CTXD0 ^{Note} | 50 | 66 | 81 |
| P37 | RXDC2/SCL02/CRXD0 ^{Note} | 51 | 67 | 82 | | |
| P40 | I/O | Port 4 6-bit I/O port(V850ES/JG3-E) 3-bit I/O port(V850ES/JE3-E, V850ES/JF3-E) Input/output can be specified in 1-bit units. | SIF0/TXDC3/SDA01/RTP00 | 52 | 68 | 85 |
| P41 | | | SOF0/RXDC3/SCL01/RTP01 | 53 | 69 | 86 |
| P42 | | | SCKF0/TIAA40/TOAA40/RTP02 | 54 | 70 | 87 |
| P43 | | | RTP03 | - | - | 88 |
| P44 | | | RTP04 | - | - | 89 |
| P45 | | | TIAA41/TOAA41/RTP05 | - | - | 90 |
| P50 | I/O | Port 5 5-bit I/O port Input/output can be specified in 1-bit units. | INTP07/DDI | 16 | 20 | 25 |
| P51 | | | INTP08/DDO | 17 | 21 | 26 |
| P52 | | | INTP09/DCK | 18 | 22 | 27 |
| P53 | | | INTP10/DMS | 19 | 23 | 28 |
| P54 | | | INTP11/DRST | 20 | 24 | 29 |

Note Available only in on-chip CAN controller products

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

(2/2)

| Pin Name | I/O | Function | Alternate Function | Pin number | | |
|----------|-------|---|----------------------------------|---|-------|-------|
| | | | | JE3-E | JF3-E | JG3-E |
| P70 | I/O | Port 7 10-bit I/O port Input/output can be specified in 1-bit units. | ANI0 | 64 | 80 | 100 |
| P71 | | | ANI1 | 63 | 79 | 99 |
| P72 | | | ANI2 | 62 | 78 | 98 |
| P73 | | | ANI3 | 61 | 77 | 97 |
| P74 | | | ANI4 | 60 | 76 | 96 |
| P75 | | | ANI5 | 59 | 75 | 95 |
| P76 | | | ANI6 | 58 | 74 | 94 |
| P77 | | | ANI7 | 57 | 73 | 93 |
| P78 | | | ANI8 | 56 | 72 | 92 |
| P79 | | | ANI9 | 55 | 71 | 91 |
| P90 | I/O | Port 9 13-bit I/O port(V850ES/JG3-E) 11-bit I/O port(V850ES/JF3-E) Input/output can be specified in 1-bit units. | TOAB1T1/TOAB11/TIAB11/KR0/INTP12 | - | 57 | 72 |
| P91 | | | TOAB1B1/TIAB10/KR1/TOAB10 | - | 58 | 73 |
| P92 | | | TOAB1T2/TOAB12/TIAB12/KR2/INTP13 | - | 59 | 74 |
| P93 | | | TOAB1B2/TRGAB1/KR3/INTP14 | - | 60 | 75 |
| P94 | | | TOAB1T3/TOAB13/TIAB13/KR4/INTP15 | - | 61 | 76 |
| P95 | | | TOAB1B3/EVTB1/KR5/INTP16 | - | 62 | 77 |
| P96 | | | TECR0/TIT00/KR6/TOT00 | - | 31 | 40 |
| P97 | | | TENC00/TIT01/KR7/TOT01 | - | 32 | 41 |
| P98 | | | TENC01/INTP17 | - | 33 | 42 |
| P912 | | | TOAB1OFF/INTP18 | - | 63 | 78 |
| P913 | | | SIF31/INTP19 | - | - | 30 |
| | | | INTP19 | - | 25 | - |
| P914 | | | SOF3/INTP20 | - | - | 31 |
| P915 | | | SCKF3 | - | - | 32 |
| PDL0 | | | I/O | Port DL 11-bit I/O port(V850ES/JG3-E) 1-bit I/O port(V850ES/JF3-E, V850ES/JE3-E) Input/output can be specified in 1-bit units. | - | - |
| PDL1 | - | - | | | - | 59 |
| PDL2 | - | - | | | - | 60 |
| PDL3 | - | - | | | - | 66 |
| PDL4 | - | - | | | - | 67 |
| PDL5 | FLMD1 | 49 | | | 64 | 79 |
| PDL6 | - | - | | | - | 83 |
| PDL7 | - | - | | | - | 84 |
| PDL8 | - | - | | | - | 33 |
| PDL9 | - | - | | | - | 34 |
| PDL10 | - | - | - | 43 | | |

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

1.2 Non-Port Pins

(1/5)

| Pin Name | I/O | Function | Alternate Function | Pin number | | |
|-----------------------|---------|--|--------------------------------------|------------|--------|--------|
| | | | | JE3-E | JF3-E | JG3-E |
| ADTRG | Input | External trigger input for A/D converter | P03/INTP00/EXCLK | – | – | 4 |
| ANI0 | Input | Analog voltage input for A/D converter | P70 | 64 | 80 | 100 |
| ANI1 | | | P71 | 63 | 79 | 99 |
| ANI2 | | | P72 | 62 | 78 | 98 |
| ANI3 | | | P73 | 61 | 77 | 97 |
| ANI4 | | | P74 | 60 | 76 | 96 |
| ANI5 | | | P75 | 59 | 75 | 95 |
| ANI6 | | | P76 | 58 | 74 | 94 |
| ANI7 | | | P77 | 57 | 73 | 93 |
| ANI8 | | | P78 | 56 | 72 | 92 |
| ANI9 | | | P79 | 55 | 71 | 91 |
| ASCKC0 | Input | UARTC0 baud rate clock input | P32/SCKF2/TIAA10/TOAA10 | 15 | 19 | 22 |
| AVREF0 | – | Reference voltage input for A/D converter, and positive power supply for port 7 | – | 1 | 1 | 1 |
| AVSS | – | Ground voltage for A/D converter | – | 2 | 2 | 2 |
| CRXD0 ^{Note} | Input | CAN receive data input | P37/RXDC2/SCL02 | 51 | 67 | 82 |
| CTXD0 ^{Note} | Output | CAN transmit data output | P36/TXDC2/SDA02 | 50 | 66 | 81 |
| DCK | Input | Clock input for on-chip debugging | P52/INTP09 | 18 | 22 | 27 |
| DDI | Input | Data input for on-chip debugging | P50/INTP07 | 16 | 20 | 25 |
| DDO | Output | Data output for on-chip debugging In the on-chip debug mode, high-level output is forcibly set. | P51/INTP08 | 17 | 21 | 26 |
| DMS | Input | Mode select signal input for on-chip debugging | P53/INTP10 | 19 | 23 | 28 |
| DRST | Input | Reset signal input for on-chip debugging | P54/INTP11 | 20 | 24 | 29 |
| EVDD | – | Positive power supply for external (same potential as VDD) | – | 24, 44 | 29, 52 | 38, 65 |
| EVTAB1 | Input | External event count input of TAB1 | P95/TOAB1B3/KR5/INTP16 | – | 62 | 77 |
| EXCLK | Input | USB clock signal input | P03/INTP00/ADTRG | – | – | 4 |
| FLMD0 | Input | Flash programming mode setting pins | – | 42 | 50 | 63 |
| FLMD1 | Input | | PDL5/AD5 | 49 | 64 | 79 |
| INTP00 | Input | External interrupt request input (maskable, analog noise elimination). Analog noise elimination or digital noise elimination selectable for INTP02 pin. | P03/ADTRG/EXCLK | – | – | 4 |
| INTP01 | | | P20 | 4 | 4 | 5 |
| INTP02 | | | P22/RTC1HZ | – | – | 7 |
| INTP03 | | | P23/SIF1/TXDC1/SDA00 | – | 13 | 16 |
| INTP04 | | | P24/SOF1/RXDC1/SDL00 | – | 14 | 17 |
| INTP05 | | | P26/TIAA31/TOAA31 | – | 16 | 19 |
| INTP06 | | | P35/SCKF4/TIAA21/TOAA21 /TOAA1OFF | – | – | 80 |
| | | | P35/TIAA21/TOAA21/TOAA1OFF | – | 65 | – |
| INTP07 | | | P50/DDI | 16 | 20 | 25 |
| INTP08 | | | P51/DDO | 17 | 21 | 26 |
| INTP09 | | | P52/DCK | 18 | 22 | 27 |
| INTP10 | P53/DMS | 19 | 23 | 28 | | |

Note Available only in on-chip CAN controller products

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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| Pin Name | I/O | Function | Alternate Function | Pin number | | |
|----------|--------|--|-----------------------------------|------------|-----------|-------|
| | | | | JE3-E | JF3-E | JG3-E |
| INTP11 | Input | External interrupt request input (maskable, analog noise elimination). | P54/DRST | 20 | 24 | 29 |
| INTP12 | | | P90/TOAB1T1/TOAB11/TIAB11 /KR0 | - | 57 | 72 |
| INTP13 | | | P92/TOAB1T2/TOAB12/TIAB12 /KR2 | - | 59 | 74 |
| INTP14 | | | P93/TOAB1B2/TRGAB1/KR3 | - | 60 | 75 |
| INTP15 | | | P94/TOAB1T3/TOAB13/TIAB13 /KR4 | - | 61 | 76 |
| INTP16 | | | P95/TOAB1B3/EVTAB1/KR5 | - | 62 | 77 |
| INTP17 | | | P98/TENC01 | - | 33 | 42 |
| INTP18 | | | P912/TOAB1OFF | - | 63 | 78 |
| INTP19 | | | P913/SIF3 | - | - | 30 |
| INTP20 | | | P913 | - | 25 | - |
| | | | | | P914/SOF3 | - |
| KR0 | Input | Key interrupt input (analog noise elimination) | P90/TOAB1T1/TOAB11/TIAB11 /INTP12 | - | 57 | 72 |
| KR1 | | | P91/TOAB1B1/TIAB10/TOAB10 | - | 58 | 73 |
| KR2 | | | P92/TOAB1T2/TOAB12/TIAB12 /INTP13 | - | 59 | 74 |
| KR3 | | | P93/TOAB1B2/TRGAB1/INTP14 | - | 60 | 75 |
| KR4 | | | P94/TOAB1T3/TOAB13/TIAB13 /INTP15 | - | 61 | 76 |
| KR5 | | | P95/TOAB1B3/EVTAB1/INTP16 | - | 62 | 77 |
| KR6 | | | P96/TECR0/TIT00/TOT00 | - | 31 | 40 |
| KR7 | | | P97/TENC00/TIT01/TOT01 | - | 32 | 41 |
| NMI | Input | External interrupt (non-maskable, analog noise elimination) | P02 | 3 | 3 | 3 |
| P1COL | Input | Collision detection input for Ethernet | - | 46 | 54 | 69 |
| P1CRS | Input | Carrier detection input for Ethernet | - | 45 | 53 | 68 |
| P1MDC | Output | Serial transmit clock output | - | 32 | 40 | 50 |
| P1MDIO | I/O | Serial I/O | - | 47 | 55 | 70 |
| P1RXCLK | Input | Receive clock input for Ethernet | - | 48 | 56 | 71 |
| P1RXD0 | Input | Receive data input for Ethernet | - | 39 | 47 | 57 |
| P1RXD1 | Input | Receive data input for Ethernet | - | 33 | 41 | 51 |
| P1RXD2 | Input | Receive data input for Ethernet | - | 34 | 42 | 52 |
| P1RXD3 | Input | Receive data input for Ethernet | - | 35 | 43 | 53 |
| P1RXDV | Input | Receive data VALID input for Ethernet | - | 36 | 44 | 54 |
| P1RXER | Input | Receive data error input for Ethernet | - | 37 | 45 | 55 |
| P1TXCLK | Output | Transmit clock output for Ethernet | - | 38 | 46 | 56 |
| P1TXD0 | Output | Transmit data output for Ethernet | - | 26 | 34 | 44 |
| P1TXD1 | Output | Transmit data output for Ethernet | - | 27 | 35 | 45 |
| P1TXD2 | Output | Transmit data output for Ethernet | - | 28 | 36 | 46 |
| P1TXD3 | Output | Transmit data output for Ethernet | - | 29 | 37 | 47 |
| P1TXEN | Output | Transmit data enable output for Ethernet | - | 31 | 39 | 49 |
| P1TXER | Output | Transmit error output for Ethernet | - | 30 | 38 | 48 |

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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| Pin Name | I/O | Function | Alternate Function | Pin number | | |
|----------|--------|---|------------------------------------|------------|-------|-------|
| | | | | JE3-E | JF3-E | JG3-E |
| REGC | – | Connecting capacitor for regulator output stabilization (4.7 μF (preliminary value)) | – | 6, 41 | 6, 49 | 9, 62 |
| RESET | Input | System reset input | – | 10 | 10 | 13 |
| RTC1HZ | Output | Real-time counter correction clock (1 Hz) output | P22/INTP02 | – | – | 7 |
| RTCC | Output | Real-time counter clock (original 32 kHz clock) output | P21/RTCDIV | – | – | 6 |
| RTCDIV | Output | Real-time counter clock (divided 32 kHz clock) output | P21/RTCC | – | – | 6 |
| RTP00 | Output | Real-time output port RTP00, RTP01 are N-ch open-drain output selectable. | P40/SIF0/TXDC3/SDA01 | 52 | 68 | 85 |
| RTP01 | | | P41/SOF0/RXDC3/SCL01 | 53 | 69 | 86 |
| RTP02 | | | P42/SCKF0/TIAA40/TOAA40 | 54 | 70 | 87 |
| RTP03 | | | P43 | – | – | 88 |
| RTP04 | | | P44 | – | – | 89 |
| RTP05 | | | P45/TIAA41/TOAA41 | – | – | 90 |
| RXDC0 | Input | Serial receive data input (UARTC0 to UARTC3) | P31/SOF2/TIAA01/TOAA01 | 14 | 18 | 21 |
| RXDC1 | | | P24/SOF1/SDL00/INTP04 | – | 14 | 17 |
| RXDC2 | | | P37/SCL02/CRXD0 ^{Note} | 51 | 67 | 82 |
| RXDC3 | | | P41/SOF0/SCL01/RTP01 | 53 | 69 | 86 |
| SCKF0 | I/O | Serial clock I/O (CSIF0 to CSIF4) | P42/TIAA40/TOAA40/RTP02 | 54 | 70 | 87 |
| SCKF1 | | | P25/TIAA30/TOAA30 | – | 15 | 18 |
| SCKF2 | | | P32/ASCKC0/TIAA10/TOAA10 | 15 | 19 | 22 |
| SCKF3 | | | P915 | – | – | 32 |
| SCKF4 | | | P35/TIAA21/TOAA21/TOAA1OFF /INTP06 | – | – | 80 |
| SCL00 | I/O | Serial clock I/O (I ² C00 to I ² C02) N-ch open-drain output selectable. | P24/SOF1/RXDC1/INTP04 | – | 14 | 17 |
| SCL01 | | | P41/SOF0/RXDC3/RTP01 | 53 | 69 | 86 |
| SCL02 | | | P37/RXDC2/CRXD0 ^{Note} | 51 | 67 | 82 |
| SDA00 | I/O | Serial transmit/receive data I/O (I ² C00 to I ² C02) N-ch open-drain output selectable. | P23/SIF1/TXDC1/INTP03 | – | 13 | 16 |
| SDA01 | | | P40/SIF0/TXDC3/RTP00 | 52 | 68 | 85 |
| SDA02 | | | P36/TXDC2/CTXD0 ^{Note} | 50 | 66 | 81 |
| SIF0 | Input | Serial receive data input (CSIF0 to CSIF4) | P40/TXDC3/SDA01/RTP00 | 52 | 68 | 85 |
| SIF1 | | | P23/TXDC1/SDA00/INTP03 | – | 13 | 16 |
| SIF2 | | | P30/TXDC0/TIAA00/TOAA00 | 13 | 17 | 20 |
| SIF3 | | | P913/INTP19 | – | – | 30 |
| SIF4 | | | P33/TIAA11/TOAA11 | – | – | 23 |
| SOF0 | Output | Serial transmit data output (CSIF0 to CSIF4) N-ch open-drain output selectable. | P41/RXDC3/SCL01/RTP01 | 53 | 69 | 86 |
| SOF1 | | | P24/RXDC1/SDL00/INTP04 | – | 14 | 17 |
| SOF2 | | | P31/RXDC0/TIAA01/TOAA01 | 14 | 18 | 21 |
| SOF3 | | | P914/INTP20 | – | – | 31 |
| SOF4 | | | P34/TIAA20/TOAA20 | – | – | 24 |
| TECR0 | Input | Encoder clear input of TMT0 | P96/TIT00/KR6/TOT00 | – | 31 | 40 |
| TENC00 | | Encoder input/external event input/external trigger input of TMT0 | P97/TIT01/KR7/TOT01 | – | 32 | 41 |
| TENC01 | | Encoder input of TMT0 | P98/INTP17 | – | 33 | 42 |

Note Available only in on-chip CAN controller products

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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| Pin Name | I/O | Function | Alternate Function | Pin number | | |
|----------|------------------------------------|--|--|------------------------|-------|-------|
| | | | | JE3-E | JF3-E | JG3-E |
| TIAA00 | Input | Capture trigger input/external event input/external trigger input (TAA0) | P30/TXDC0/SIF2/TOAA00 | 13 | 17 | 20 |
| TIAA01 | | Capture trigger input (TAA0) | P31/RXDC0/SOF2/TOAA01 | 14 | 18 | 21 |
| TIAA10 | | Capture trigger input/external event input/external trigger input (TAA1) | P32/ASCKC0/SCKF2/TOAA10 | 15 | 19 | 22 |
| TIAA11 | | Capture trigger input (TAA1) | P33/SIF4/TXDB0/TOAA11 | - | - | 23 |
| TIAA20 | | Capture trigger input/external event input/external trigger input (TAA2) | P34/SOF4/RXDB0/TOAA20 | - | - | 24 |
| TIAA21 | | Capture trigger input (TAA2) | P35/SCKF4/TOAA21/TOAA1OFF /INTP06 | - | - | 80 |
| | | | TIAA21/TOAA21/TOAA1OFF/INT P06 | - | 65 | - |
| TIAA30 | | Capture trigger input/external event input/external trigger input (TAA3) | P25/SCKF1/TOAA30 | - | 15 | 18 |
| TIAA31 | | Capture trigger input (TAA3) | P26/TOAA31/INTP05 | - | 16 | 19 |
| TIAA40 | | Capture trigger input/external event input/external trigger input (TAA4) | P42/SCKF0/TOAA40/RTP02 | 54 | 70 | 87 |
| TIAA41 | | Capture trigger input (TAA4) | P45/SCKE0/TOAA41/RTP05 | - | - | 90 |
| TIAB10 | | Input | Capture trigger input/external event input/external trigger input (TAB1) N-ch open-drain output selectable. | P91/TOAB1B1/KR1/TOAB10 | - | 58 |
| TIAB11 | Capture trigger input (TAB1) | | P90/TOAB1T1/TOAB11/KR0/INTP12 | - | 57 | 72 |
| TIAB12 | N-ch open-drain output selectable. | | P92/TOAB1T2/TOAB12/KR2/INTP13 | - | 59 | 74 |
| TIAB13 | | | P94/TOAB1T3/TOAB13/KR4/INTP15 | - | 61 | 76 |
| TIT00 | Input | Capture trigger input of TMT0 | P96/TECR0/KR6/TOT00 | - | 31 | 40 |
| TIT01 | | N-ch open-drain output selectable. | P97/TENC00/KR7/TOT01 | - | 32 | 41 |
| TOAA00 | Output | Timer output (TAA0) | P30/TXDC0/SIF2/TIAA00 | 13 | 17 | 20 |
| TOAA01 | | N-ch open-drain output selectable. | P31/RXDC0/SOF2/TIAA01 | 14 | 18 | 21 |
| TOAA10 | | Timer output (TAA1) | P32/ASCKC0/SCKF2/TIAA10 | 15 | 19 | 22 |
| TOAA11 | | N-ch open-drain output selectable. | P33/SIF4/TIAA11 | - | - | 23 |
| TOAA1OFF | Input | TAA1 High-impedance output control signal input | P35/SCKF4/TIAA21/TOAA21/INTP06 | - | - | 80 |
| | | | P35/TIAA21/TOAA21/INTP06 | - | 65 | - |
| TOAA20 | Output | Timer output (TAA2) | P34/SOF4/TIAA20 | - | - | 24 |
| TOAA21 | | N-ch open-drain output selectable. | P35/SCKF4/TIAA21/TOAA1OFF /INTP06 | - | - | 80 |
| | | | P35/TIAA21/TOAA1OFF/INTP06 | - | 65 | - |
| TOAA30 | | Timer output (TAA3) | P25/SCKF1/TIAA30/ | - | 15 | 18 |
| TOAA31 | | N-ch open-drain output selectable. | P26/TIAA31/INTP05 | - | 16 | 19 |
| TOAA40 | | Timer output (TAA4) | P42/SCKF0/TIAA40/RTP02 | 54 | 70 | 87 |
| TOAA41 | | N-ch open-drain output selectable. | P45/SCKE0/TIAA41/RTP05 | - | - | 90 |
| TOAB10 | Output | Timer output (TAB1) | P91/TOAB1B1/TIAB10/KR1 | - | 58 | 73 |
| TOAB11 | | N-ch open-drain output selectable. | P90/TOAB1T1/TIAB11/KR0/INTP12 | - | 57 | 72 |
| TOAB12 | | | P92/TOAB1T2/TIAB12/KR2/INTP13 | - | 59 | 74 |
| TOAB13 | | | P94/TOAB1T3/TIAB13/KR4/INTP15 | - | 61 | 76 |

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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| Pin Name | I/O | Function | Alternate Function | Pin number | | |
|------------------|--------|---|---------------------------------|------------|-------|-------|
| | | | | JE3-E | JF3-E | JG3-E |
| TOAB1B1 | Output | Pulse signal output for 6-phase PWM low arm of TAB1 | P91/TIAB10/KR1/TOAB10 | - | 58 | 73 |
| TOAB1B2 | | | P93/TRGAB1/KR3/INTP14 | - | 60 | 75 |
| TOAB1B3 | | | P95/EVTAB1/KR5/INTP16 | - | 62 | 77 |
| TOAB1OFF | Input | TAB1 High-impedance output control signal input | P912/INTP18 | - | 63 | 78 |
| TOAB1T1 | Output | Pulse signal output for 6-phase PWM high arm of TAB1. N-ch open-drain output selectable. | P90/TOAB11/TIAB11/KR0/INTP12 | - | 57 | 72 |
| TOAB1T2 | | | P92/TOAB12/TIAB12/KR2/INTP13 | - | 59 | 74 |
| TOAB1T3 | | | P94/TOAB13/TIAB13/KR4/INTP15 | - | 61 | 76 |
| TOT00 | Output | Timer output of TMT0 | P96/TECR0/TIT00/KR6 | - | 31 | 40 |
| TOT01 | | N-ch open-drain output selectable | P97/TENC00/TIT01/KR7 | - | 32 | 41 |
| TRGAB1 | Input | External trigger input of TAB1 N-ch open-drain output selectable | P93/TOAB1B2/KR3/INTP14 | - | 60 | 75 |
| TXDC0 | Output | Serial transmit data output (UARTC0 to UARTC3) N-ch open-drain output selectable. | P30/SIF2/TIAA00/TOAA00 | 13 | 17 | 20 |
| TXDC1 | | | P23/SIF1/SDA00/INTP03 | - | 13 | 16 |
| TXDC2 | | | P36/SDA02/CTXD0 ^{Note} | 50 | 66 | 81 |
| TXDC3 | | | P40/SIF0/SDA01/RTP00 | 52 | 68 | 85 |
| UDMF | I/O | USB data I/O (-) function | - | 21 | 26 | 35 |
| UDPF | | USB data I/O (+) function | - | 22 | 27 | 36 |
| UV _{DD} | - | 3.3 V positive power supply for USB | - | 23 | 28 | 37 |
| V _{DD} | - | Positive power supply for internal circuit | - | 5 | 5 | 8 |
| V _{SS} | - | Ground potential for internal circuit | - | 7 | 7 | 10 |
| X1 | Input | Connecting resonator for main clock | - | 8 | 8 | 11 |
| X2 | - | | - | 9 | 9 | 12 |
| XT1 | Input | Connecting resonator for subclock | - | 8 | 11 | 14 |
| XT2 | - | | - | 9 | 12 | 15 |

Note Available only in on-chip CAN controller products.

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

1.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 1-1. For the schematic circuit diagram of each type, refer to **Figure 1-1**.

Table 1-1. Types of Pin I/O Circuits (1/3)

| Pin Name | Alternate Function | I/O Circuit Type | Recommended Connection of Unused Pins | JE3-E | JF3-E | JG3-E |
|------------|---|------------------|--|----------|----------|-----------|
| P02 | NMI | 10-D | Input: Independently connect to EV _{DD} or V _{SS} via a resistor. Output: Leave open. | 3 | 3 | 3 |
| P03 | INTP00/ADTRG/EXCLK | | | - | - | 4 |
| P20 | TOAB02/INTP01 | 10-D | Input: Independently connect to EV _{DD} or V _{SS} via a resistor. Output: Leave open. | 4 | 4 | 5 |
| P21 | RTCDIV/RTCCL | | | - | - | 6 |
| P22 | RTC1HZ/INTP02 | | | - | - | 7 |
| P23 | SIF1/TXDC1/SDA00/INTP03 | | | - | 13 | 16 |
| P24 | SOF1/RXDC1/SCL00/INTP04 | | | - | 14 | 17 |
| P25 | SCKF1/TIAA30/TOAA30 | | | - | 15 | 18 |
| P26 | TIAA31/TOAA31/INTP05 | | | - | 16 | 19 |
| P27 | TIAB03/TOAB03/INTP21 | | | 4 | 4 | 5 |
| P30 | TXDC0/SIF2/TIAA00/TOAA00 | 10-D | Input: Independently connect to EV _{DD} or V _{SS} via a resistor. Output: Leave open. | 13 | 17 | 20 |
| P31 | RXDC0/SOF2/TIAA01/TOAA01 | | | 14 | 18 | 21 |
| P32 | ASCKC0/SCKF2/TIAA10/TOAA10 | | | 15 | 19 | 22 |
| P33 | SIF4/TIAA11/TOAA11 | | | - | - | 23 |
| P34 | SOF4/TIAA20/TOAA20 | | | - | - | 24 |
| P35 | SCKF4/TIAA21/TOAA21 /TOAA1OFF/INTP06 ----- TIAA21/TOAA21/TOAA1OFF/INTP06 | | | - | - | 80 |
| P36 | TXDC2/SDA02/CTXD0 ^{Note} | | | - | 65 | - |
| P37 | RXDC2/SCL02/CRXD0 ^{Note} | | | 50 | 66 | 81 |
| P40 | SIF0/TXDC3/SDA01/RTP00 | 10-D | Input: Independently connect to EV _{DD} or V _{SS} via a resistor. Output: Leave open. | 52 | 68 | 85 |
| P41 | SOF0/RXDC3/SCL01/RTP01 | | | 53 | 69 | 86 |
| P42 | SCKF0/TIAA40/TOAA40/RTP02 | | | 54 | 70 | 87 |
| P43 | RTP03 | | | - | - | 88 |
| P44 | RTP04 | | | - | - | 89 |
| P45 | TIAA41/TOAA41/RTP05 | | | - | - | 90 |
| P50 | INTP07/DDI | 10-D | Input: Independently connect to EV _{DD} or V _{SS} via a resistor. Output: Leave open. | 16 | 20 | 25 |
| P51 | INTP08/DDO | | | 17 | 21 | 26 |
| P52 | INTP09/DCK | | | 18 | 22 | 27 |
| P53 | INTP10/DMS | | | 19 | 23 | 28 |
| P54 | INTP11/DRST | 10-N | Input: Independently connect to V _{SS} via a resistor. Fixing to V _{DD} level is prohibited. Output: Leave open. Internally pull-down after reset by RESET pin. | 20 | 24 | 29 |
| P70 to P79 | ANI0 to ANI9 | 11-G | Input: Independently connect to AV _{REF0} or AV _{SS} via a resistor. Output: Leave open. | 64 to 55 | 80 to 71 | 100 to 91 |

Note Available only in on-chip CAN controller products.

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Table 1-1. Types of Pin I/O Circuits (2/3)

| Pin Name | Alternate Function | I/O Circuit Type | Recommended Connection of Unused Pins | JE3-E | JF3-E | JG3-E | |
|--------------------|-----------------------------------|------------------|--|-------------|---|------------------|----|
| P90 | TOAB1T1/TOAB11/TIAB11/KR0 /INTP12 | 10-D | Input: Independently connect to EV _{DD} or V _{SS} via a resistor. Output: Leave open. | - | 57 | 72 | |
| P91 | TOAB1B1/TIAB10/KR1/TOAB10 | | | - | 58 | 73 | |
| P92 | TOAB1T2/TOAB12/TIAB12/KR2 /INTP13 | | | - | 59 | 74 | |
| P93 | TOAB1B2/TRGAB1/KR3/INTP14 | | | - | 60 | 75 | |
| P94 | TOAB1T3/TOAB13/TIAB13/KR4 /INTP15 | | | - | 61 | 76 | |
| P95 | TOAB1B3/EVTB1/KR5/INTP16 | | | - | 62 | 77 | |
| P96 | TECR0/TIT00/KR6/TOT00 | | | - | 31 | 40 | |
| P97 | TENC00/TIT01/KR7/TOT01 | | | - | 32 | 41 | |
| P98 | TENC01/INTP17 | | | - | 33 | 42 | |
| P912 | TOAB1OFF/INTP18 | | | - | 63 | 78 | |
| P913 | SIF3/INTP19 | | | - | - | 30 | |
| | INTP19 | | | - | 25 | - | |
| P914 | SOF3/INTP20 | | | - | - | 31 | |
| P915 | SCKF3 | | | - | - | 32 | |
| PDL0 to PDL4 | - | | | 5 | Input: Independently connect to EV _{DD} or V _{SS} via a resistor. | - | - |
| PDL5 | FLMD1 | 5 | Output: Leave open. | 49 | 64 | 79 | |
| PDL6 to PDL10 | - | 5 | | - | - | 83,84, 33,34, 43 | |
| AV _{REF0} | - | - | Directly connect to V _{DD} and always supply power. | 1 | 1 | 1 | |
| AV _{SS} | - | - | Directly connect to V _{SS} . | 2 | 2 | 2 | |
| EV _{DD} | - | - | Directly connect to V _{DD} and always supply power. | 24, 44 | 29, 52 | 38, 65 | |
| FLMD0 | - | - | Connect to V _{SS} in other than flash mode. | 42 | 50 | 63 | |
| P1COL | - | 5 | Independently connect to EV _{DD} or V _{SS} via a resistor. | 46 | 54 | 69 | |
| P1CRS | - | 5 | | 45 | 53 | 68 | |
| P1MDIO | - | 5 | | 47 | 55 | 70 | |
| P1RXCLK | - | 5 | | 48 | 56 | 71 | |
| P1RXD0 | - | 5 | | 39 | 47 | 57 | |
| P1RXD1 | - | 5 | | 33 | 41 | 51 | |
| P1RXD2 | - | 5 | | 34 | 42 | 52 | |
| P1RXD3 | - | 5 | | 35 | 43 | 53 | |
| P1RXDV | - | 5 | | 36 | 44 | 54 | |
| P1RXER | - | 5 | | 37 | 45 | 55 | |
| P1TXCLK | - | 5 | | 38 | 46 | 56 | |
| P1MDC | - | 5 | | Leave open. | 32 | 40 | 50 |
| P1TXD0 | - | 5 | | | 26 | 34 | 44 |
| P1TXD1 | - | 5 | | | 27 | 35 | 45 |
| P1TXD2 | - | 5 | | | 28 | 36 | 46 |
| P1TXD3 | - | 5 | 29 | | 37 | 47 | |
| P1TXEN | - | 5 | 31 | | 39 | 49 | |
| P1TXER | - | 5 | 30 | | 38 | 48 | |

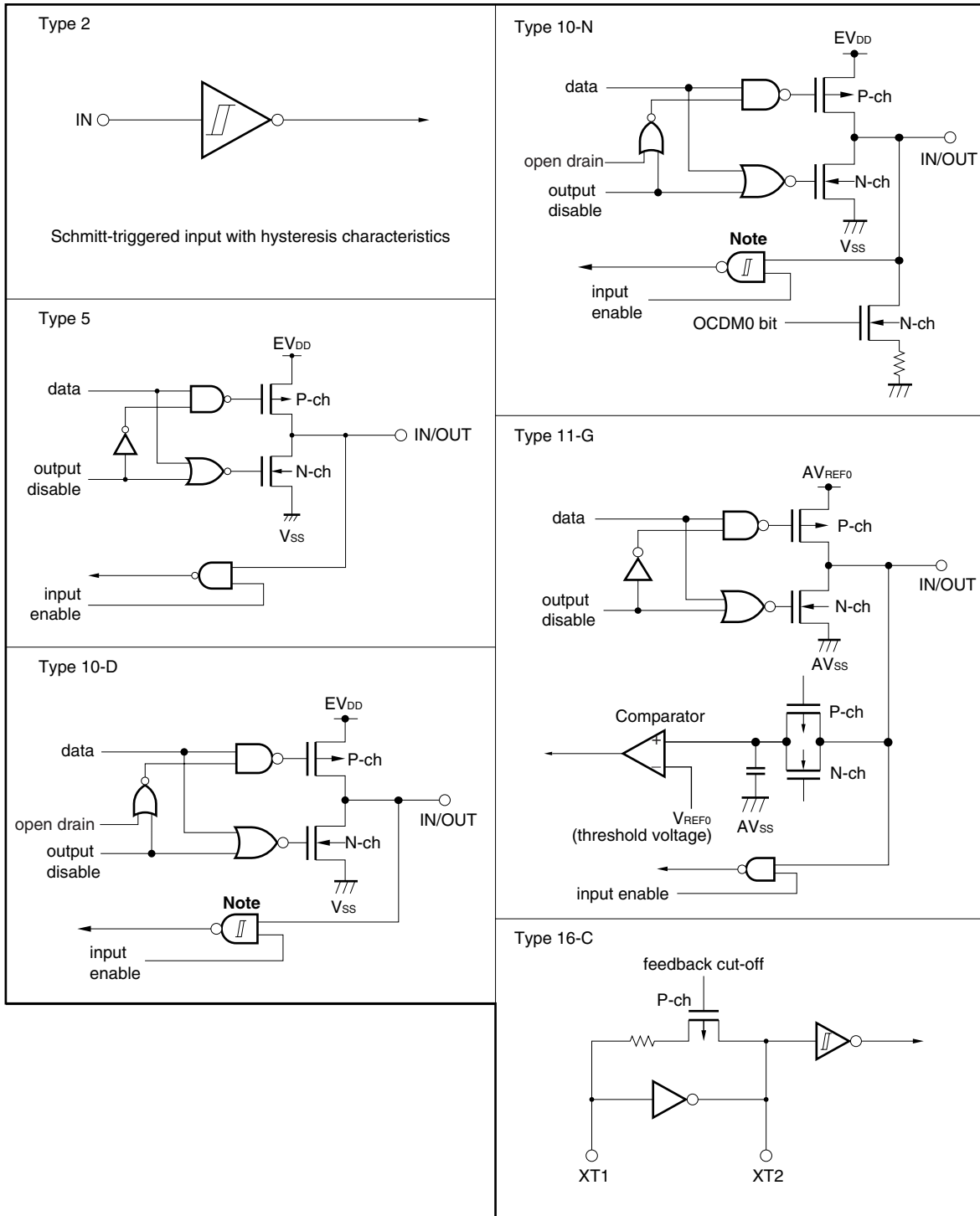
Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Table 1-1. Types of Pin I/O Circuits (3/3)

| Pin Name | Alternate Function | I/O Circuit Type | Recommended Connection of Unused Pins | JE3-E | JF3-E | JG3-E |
|------------------|--------------------|------------------|---|-------|-------|-------|
| REGC | – | – | Connect to regulator output stabilization (4.7 μF (preliminary value)) capacitor. | 6, 41 | 6, 49 | 9, 62 |
| RESET | – | 2 | – | 10 | 10 | 13 |
| UDMF | – | – | Leave open. | 21 | 26 | 35 |
| UDPF | – | – | Leave open. | 22 | 27 | 36 |
| UV _{DD} | – | – | Directly connect to V _{DD} and always supply power. | 23 | 28 | 37 |
| V _{DD} | – | – | – | 5 | 5 | 8 |
| V _{SS} | – | – | – | 7 | 7 | 10 |
| X1 | – | – | – | 8 | 8 | 11 |
| X2 | – | – | – | 9 | 9 | 12 |
| XT1 | – | 16-C | Connect to V _{SS} via a resistor. | 8 | 11 | 14 |
| XT2 | – | 16-C | Leave open. | 9 | 12 | 15 |

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Figure 1-1. Pin I/O Circuits



Note Hysteresis characteristics are not available in port mode.

2. CPU FUNCTIONS

The CPU of the V850ES/JE3-E, V850ES/JF3-E and V850ES/JG3-E is based on RISC architecture and executes most instructions in a 1-clock cycle by using a 5-stage pipeline.

The features of the CPU are as follows.

- Minimum instruction execution time: 20 ns (@ 50 MHz operation with main clock (f_{xx}))
30.5 μs (@ 32.768 kHz operation with sub-clock (f_{XT}))
- Memory space Program space: 64 MB linear
 Data space: 4 GB linear
- General-purpose registers: 32 bits × 32 registers
- Internal 32-bit architecture
- 5-stage pipeline control
- Multiplication/division instructions
- Saturation operation instructions
- 1-clock 32-bit shift instruction
- Load/store instructions with long/short format
- Internal memory

Table 2-1. ROM/RAM

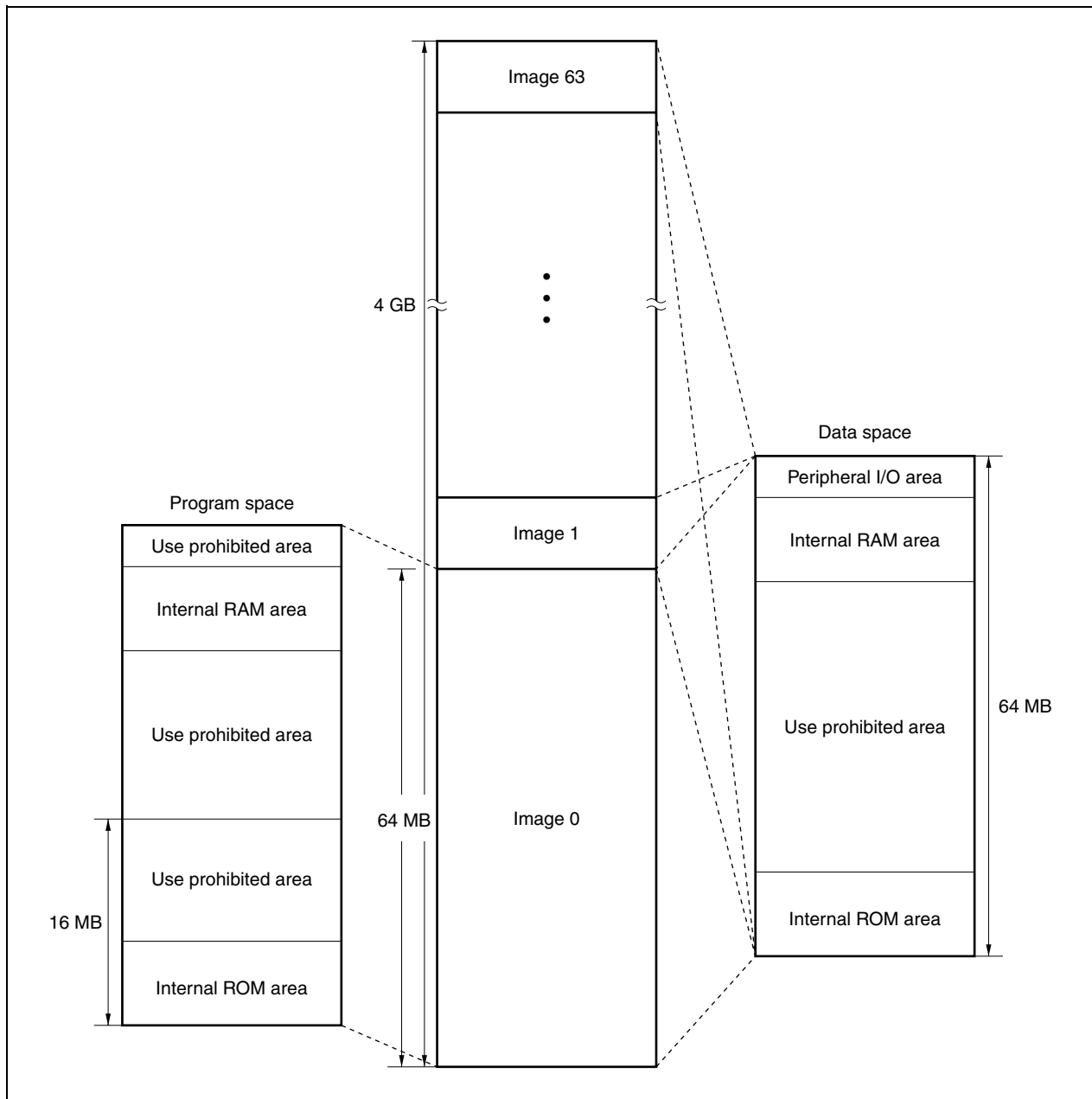
| Generic Name | Products | Flash Memory Size | RAM Size | |
|--------------|------------|-------------------|--------------|----------|
| | | | Internal RAM | Data RAM |
| V850ES/JE3-E | μPD70F3826 | 64 KB | 16 KB | 16 KB |
| | μPD70F3827 | 128 KB | 32 KB | 16 KB |
| | μPD70F3828 | 256 KB | 48 KB | 16 KB |
| | μPD70F3829 | 256 KB | 48 KB | 16 KB |
| V850ES/JF3-E | μPD70F3830 | 64 KB | 16 KB | 16 KB |
| | μPD70F3831 | 128 KB | 32 KB | 16 KB |
| | μPD70F3832 | 256 KB | 48 KB | 16 KB |
| | μPD70F3833 | 256 KB | 48 KB | 16 KB |
| V850ES/JG3-E | μPD70F3834 | 64 KB | 16 KB | 16 KB |
| | μPD70F3835 | 128 KB | 32 KB | 16 KB |
| | μPD70F3836 | 256 KB | 48 KB | 16 KB |
| | μPD70F3837 | 256 KB | 48 KB | 16 KB |

- Four types of bit manipulation instructions
 - SET1
 - CLR1
 - NOT1
 - TST1

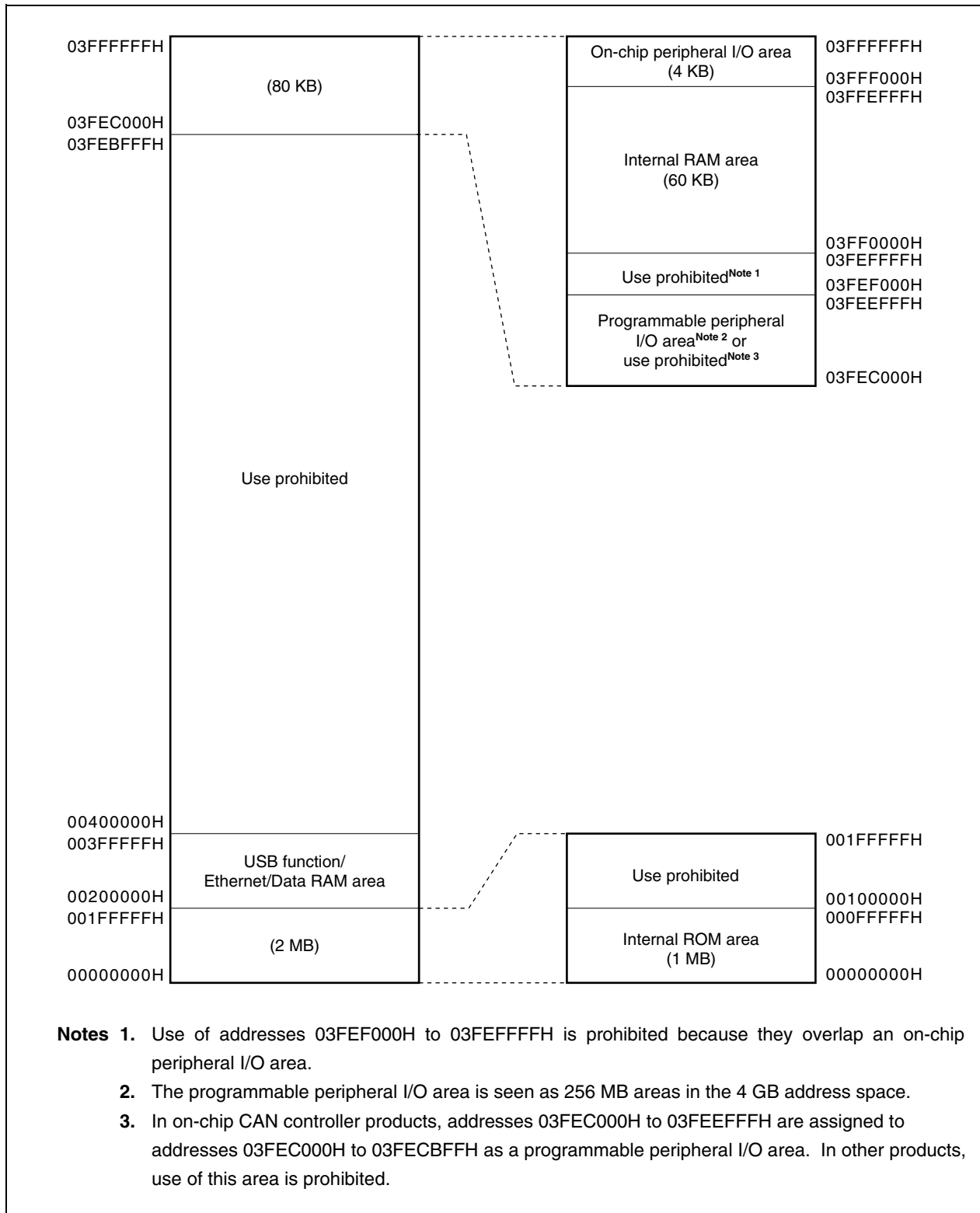
3. MEMORY MAP

The memory maps of the V850ES/JE3-E, V850ES/JF3-E and V850ES/JF3-E are shown below.

○ Address Space



○ Data Memory Map

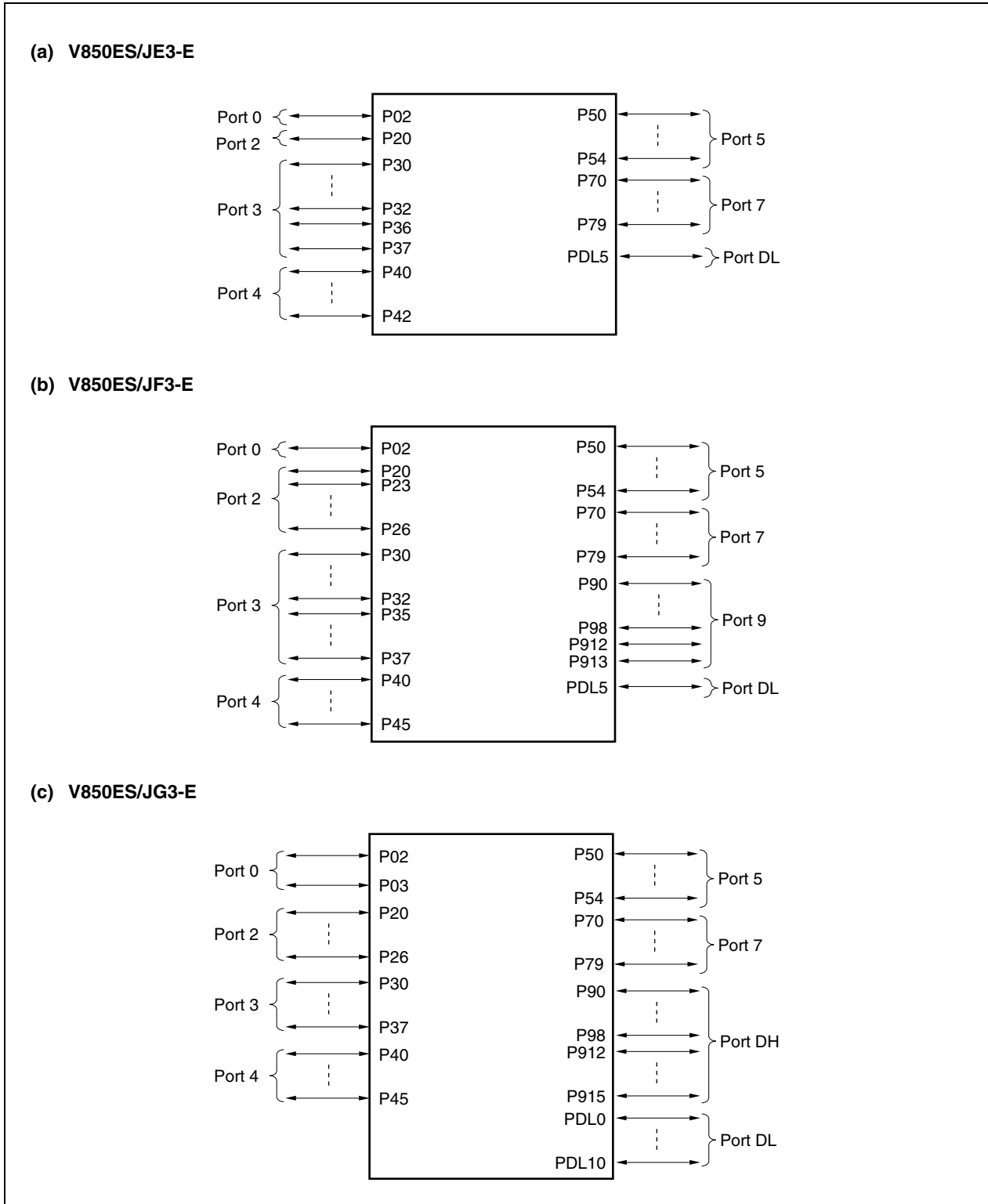


4. PORTS

The number of I/O ports of the V850ES/Jx3-E is shown below.

| Product Name | V850ES/JF3-E | V850ES/JF-E | V850ES/JG3-E |
|--------------------------------|--------------|-------------|--------------|
| Number of ports (5 V tolerant) | 26 (12) | 42 (28) | 62 (35) |

The following figure shows the basic configurations of ports.

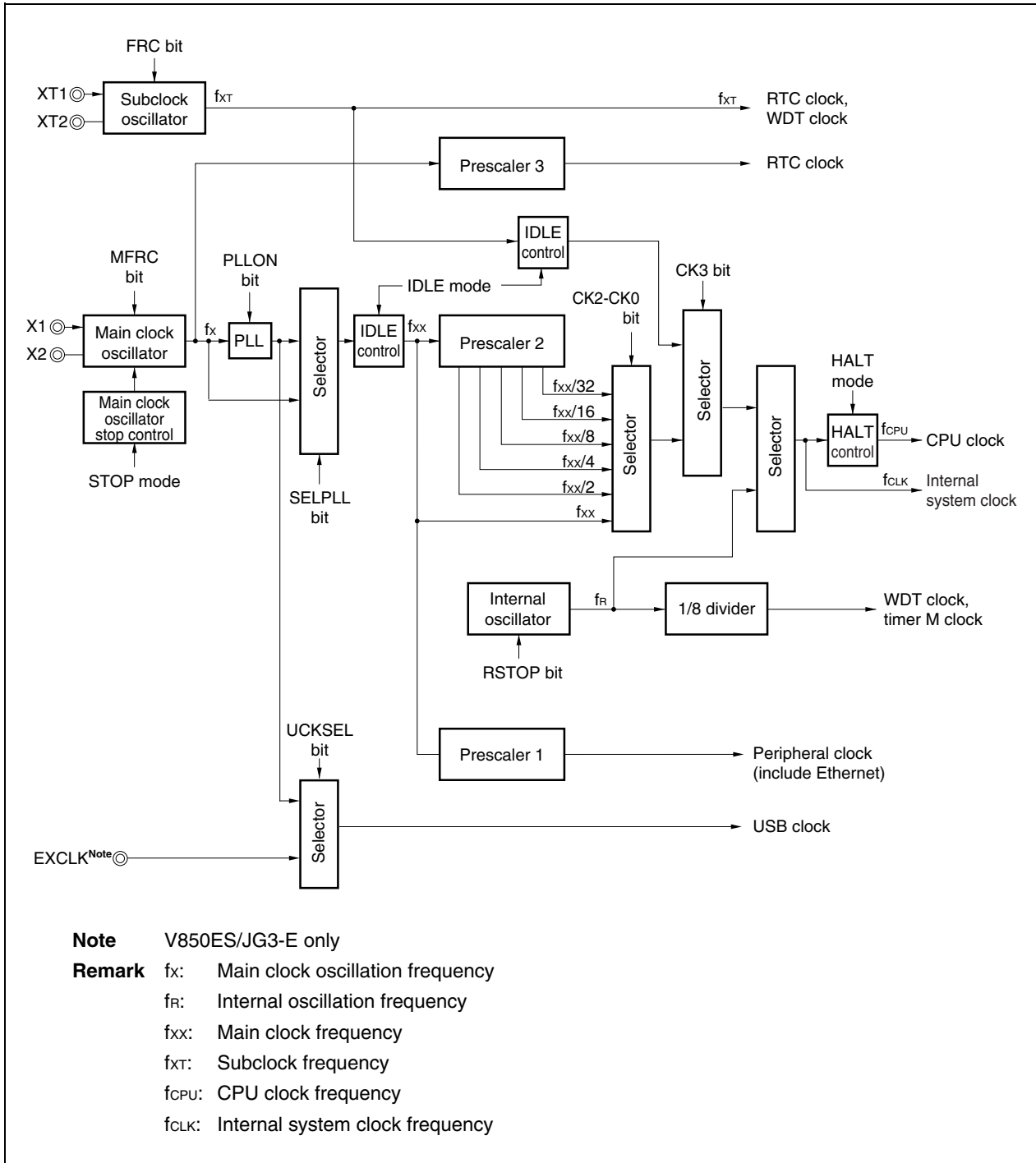


5. CLOCK GENERATION FUNCTION

The clock generation function has the following features.

- Main clock oscillator
 - PLL mode (×8): $f_x = 3$ to 6.25 MHz ($f_{xx} = 24$ to 50 MHz)
 - Clock through mode: $f_x = 3$ to 6.25 MHz ($f_{xx} = 3$ to 6.25 MHz)
- Subclock oscillator
 - $f_{XT} = 32.768$ kHz
- Internal oscillator ($f_R = 220$ kHz)
 - Default clock of watchdog timer
 - Sampling clock for clock monitor function of the main clock oscillator
 - Can be used as the internal system clock after the main clock is stopped
- Internal system clock generation
 - 7 levels (f_{xx} , $f_{xx}/2$, $f_{xx}/4$, $f_{xx}/8$, $f_{xx}/16$, $f_{xx}/32$, f_{XT})
- Peripheral clock generation
- Clock output function

The following figure shows the configuration of the clock generation function.



6. 16-BIT TIMER/EVENT COUNTER AA (TAA)

The number of TAA of the V850ES/Jx3-E is shown below.

| Product Name | V850ES/JF3-E | V850ES/JF-E | V850ES/JG3-E |
|------------------------|--|---------------------------|---------------------------|
| Number of channel | 5 channels (TAA0 to TAA4 ^{Note}) | 5 channels (TAA0 to TAA4) | 5 channels (TAA0 to TAA4) |
| Number of timer output | 4 | 7 | 10 |

Note TAA2 and TAA3 have Interval timer function only.

The timer/counter function has the following features.

- 16 bit timer/counter (TAA_n)
- Clock selection: 8 ways
- Capture/trigger input pins (TIAA_{n0}, TIAA_{n1}): 2
- External event count input pin^{Note}: 1
- External trigger input pin^{Note}: 1
- Timer/counter: 1
- Capture/compare registers: 2
(32-bit capture function available by using a cascade connection with timer AA.)
- Capture/compare match interrupt request signals: 2
- Timer output pins (TOAA_{n0}, TOAA_{n1}): 2

The TAA_n function has the following features.

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Timer tuning function
- Simultaneous start function

Note The external event count input pin and external trigger input pin also function as the capture trigger input pin (TIAA_{n0}).

Remark n = 0 to 4

7. 16-BIT TIMER/EVENT COUNTER AB (TAB)

The number of TAB of the V850ES/Jx3-E is shown below.

| Product Name | V850ES/JF3-E | V850ES/JF-E | V850ES/JG3-E |
|------------------------|-----------------------------------|------------------|------------------|
| Number of channel | 1 channel (TAB1 ^{Note}) | 1 channel (TAB1) | 1 channel (TAB1) |
| Number of timer output | - | 4 | 4 |

Note Interval timer function only.

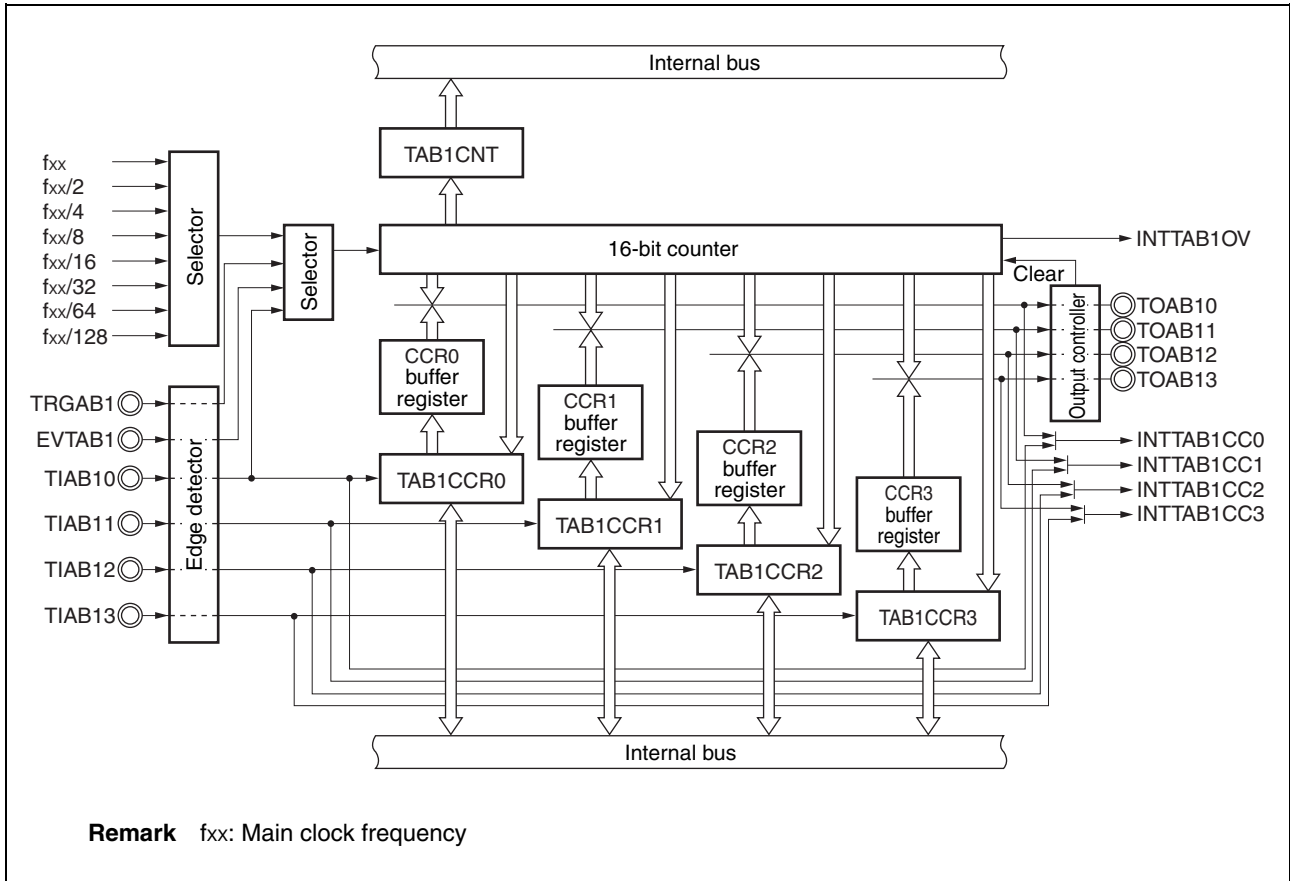
The TAB function has the following features.

- 16-bit timer/counter (TAB1)
- Clock selection: 8 ways
- Capture/trigger input pins (TIAB10 to TIAB13): 4
- External event count input pin (EVTAB1): 1
- External trigger input pin (TRGAB1): 1
- Timer/counter: 1
- Capture/compare registers: 4
- Capture/compare match interrupt request signals: 4
- Timer output pins (TOAB10 to TOAB13): 4

The TAB1 function has the following features.

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Triangular wave PWM output
- Timer tuning function

The following figure shows the configuration of TAB.



8. 16-BIT TIMER/EVENT COUNTER T (TMT)

The number of TAB of the V850ES/Jx3-E is shown below.

| Product Name | V850ES/JF3-E | V850ES/JF-E | V850ES/JG3-E |
|------------------------|-----------------------------------|------------------|------------------|
| Number of channel | 1 channel (TMT0 ^{Note}) | 1 channel (TMT0) | 1 channel (TMT0) |
| Number of timer output | - | 2 | 2 |

Note Interval timer function only.

The TMT function has the following features.

- 16 bit timer/counter (TMT)
- Clock selection: 8 ways
- Capture/trigger input pins (TIT00, TIT01) : 2
- External event count input pin^{Note 1} : 1
- Encoder input pin (TENC00, TENC01) : 2
- Encoder clear input pin (TECR0) : 1
- External trigger input pin^{Note 1}: 1
- Timer/counter: 1
- Capture/compare registers: 2
- Capture/compare match interrupt request signals: 2
- Timer output pins (TOT00, TOT01) : 2

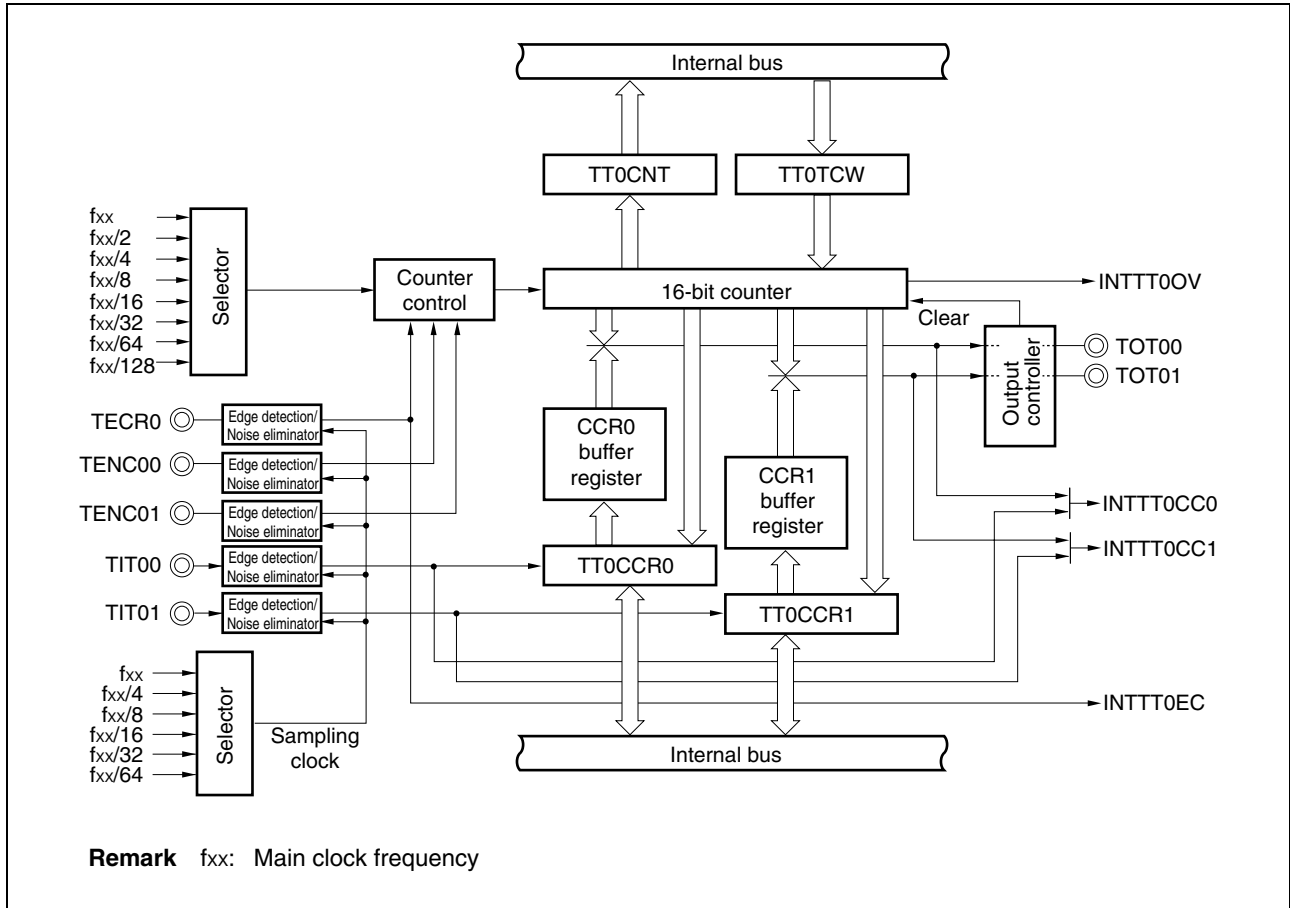
The TMT function has the following features^{Note 2}.

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Triangular wave PWM output
- Encoder count function

Notes1. The external trigger input pin and the external event count input pin also function as the encoder input pin (TENC00)

2. The TMT0 function of V850ES/JE3-E is only Interval timer.

The following figure shows the configuration of TMT.



9. 16-BIT INTERVAL TIMER M (TMM)

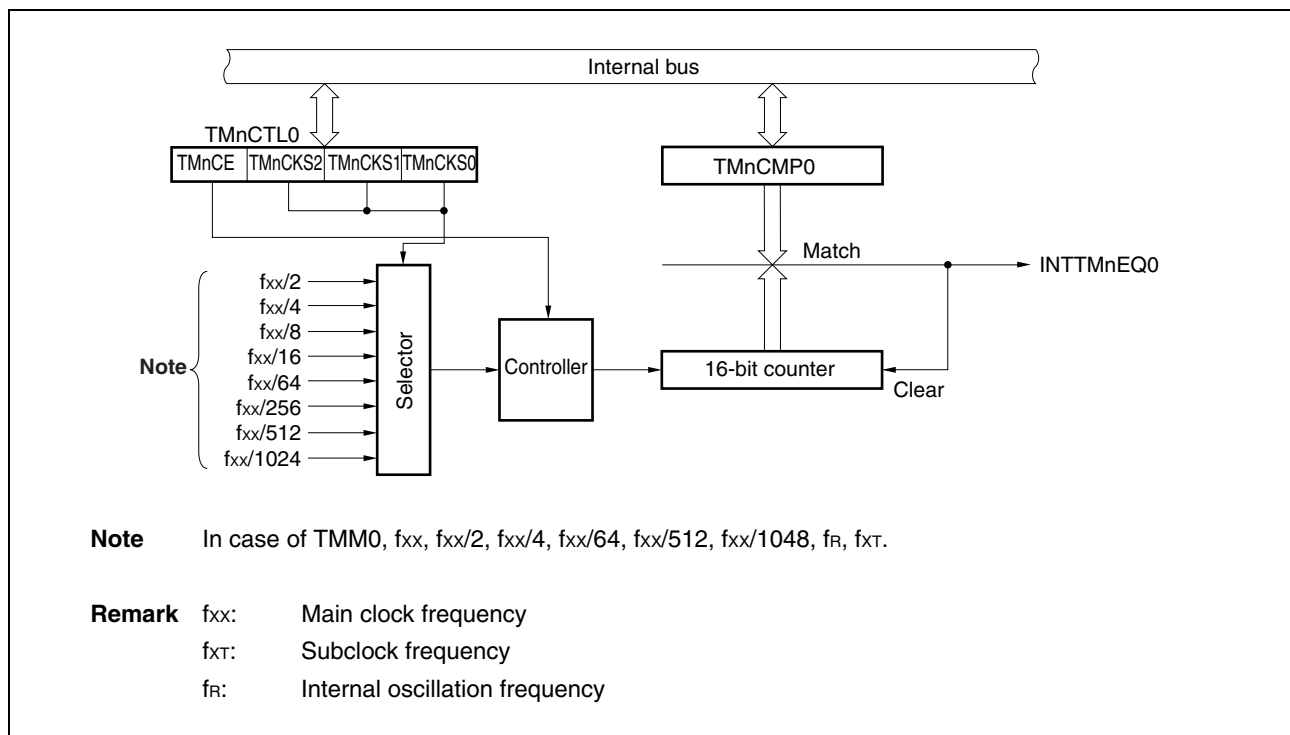
The number of TMM of the V850ES/Jx3-E is shown below.

| Product Name | V850ES/JF3-E | V850ES/JF-E | V850ES/JG3-E |
|-------------------|------------------------------|------------------------------|------------------------------|
| Number of channel | 4 channels (TMM0 to TMM3) | 4 channels (TMM0 to TMM3) | 4 channels (TMM0 to TMM3) |

The TMM function has the following features.

- Interval function
- Clock selection: 8 ways
- 16 bit counter × 1 (Not available to counter lead in timer count operation)
- Compare register × 1 (Not available to write compare register in timer count operation)
- Compare match interrupt × 1

The following figure shows the configuration of TMM.



10. MOTOR CONTROL FUNCTION

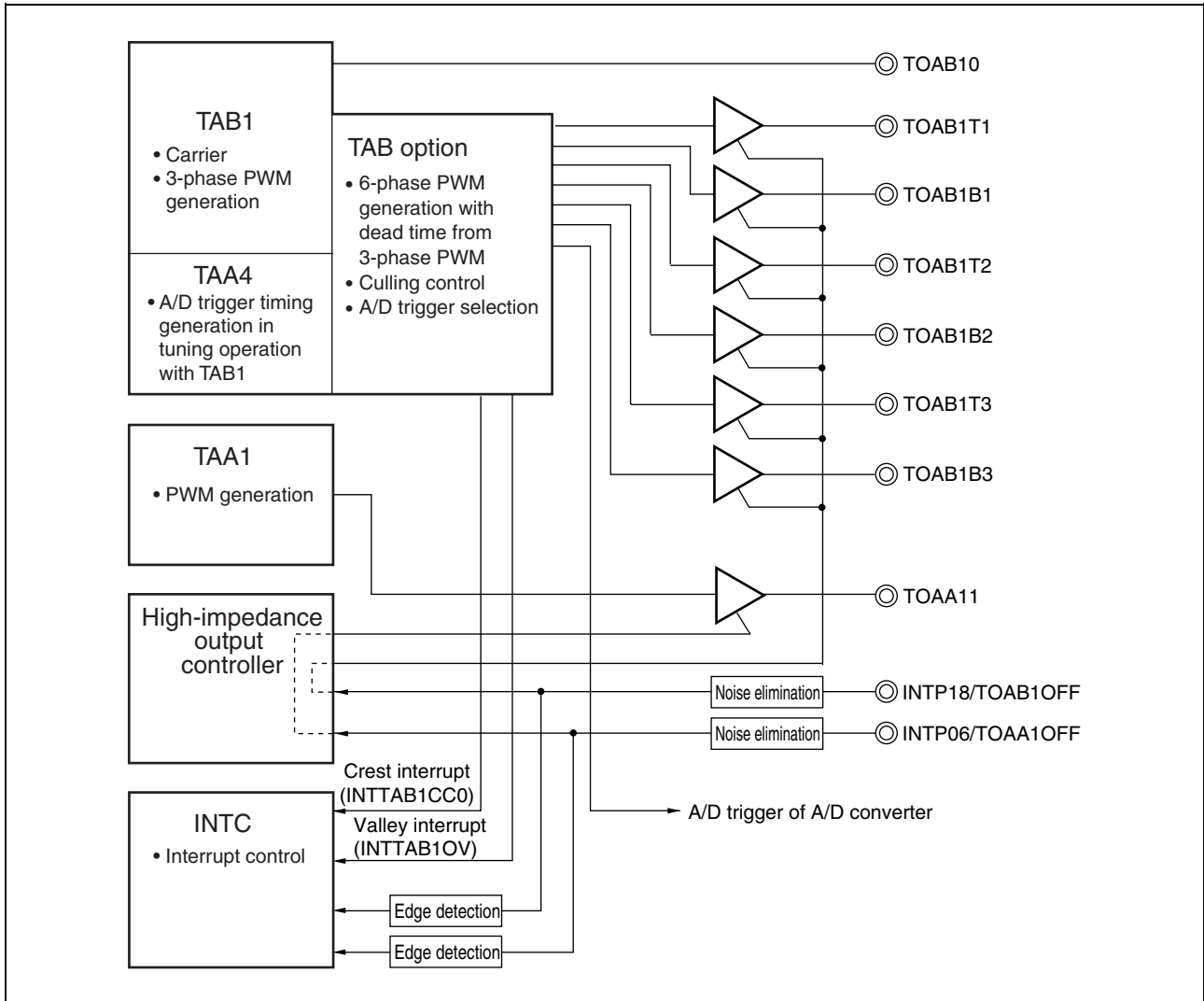
In the V850ES/JF3-E and V850ES/JG3-E, one channel of motor control function is provided.

Timer AB1 (TAB) and the TAB option (TABOP) can be used as an inverter function that controls a motor.

It performs a tuning operation with timer AA4 (TAA4) and A/D conversion of the A/D converter can be started when the value of TAB matches the value of TAA4. The following operations can be performed as motor control functions.

- 6-phase PWM output function with 16-bit resolution (with dead-timer, for upper and lower arms)
- Timer tuning operation function (tunable with TAA4)
- Cycle setting function (cycle can be changed during operation of crest or valley interrupt)
- Compare register rewriting: Anytime rewrite, batch rewrite, or intermittent rewrite
(selectable during TAB operation)
- Interrupt and transfer culling functions
- Dead-time setting function
- A/D trigger timing function of the A/D converter (four types of timing can be generated)
- 0% output and 100% output available
- 0% output and 100% output selectable by crest interrupt and valley interrupt
- Forced output stop function
 - At valid edge detection by external pin input (INTP06/TOAA1OFF, INTP18/TOAB1OFF)
 - When stoppage of the main clock oscillation is detected by clock monitor function

The following figure shows the configuration of motor control function.



11. REAL-TIME COUNTER

In the V850ES/Jx3-E, one channel of real-time counter is provided.

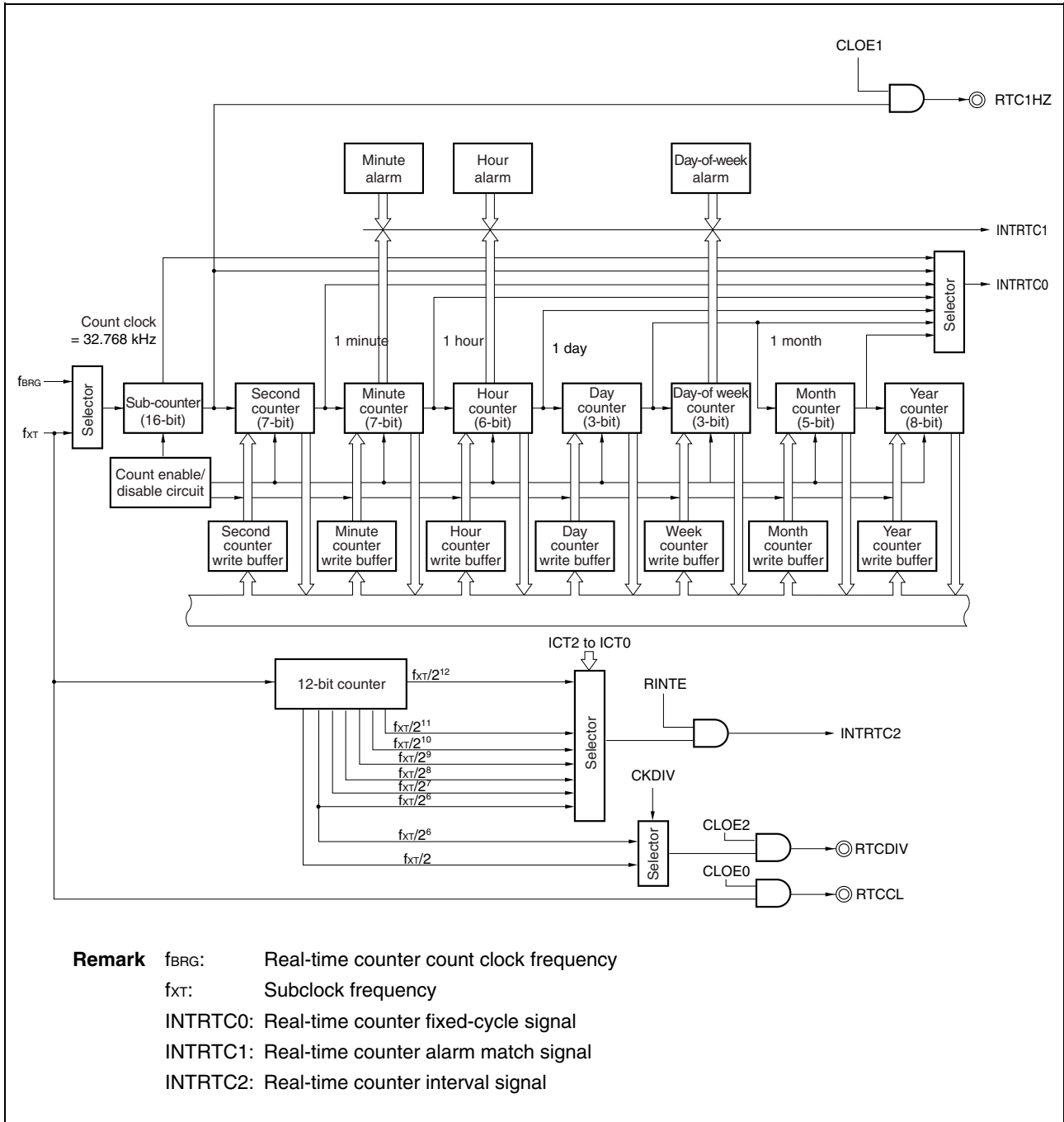
The real-time counter has the following features.

- It has counters for year, month, week, day, hours, minutes and seconds, and it can count up to 99 years.
- The year, month, week, day, hour, minute and second counters show the count in BCD code^{Note 1}.
- Alarm interrupt function
- Fixed-cycle interrupt function (cycle: 1 month to 0.5 seconds)
- Interval interrupt function (cycle: 1.95 to 125 ms)
- 1 Hz pin output
- 32.768 kHz pin output
- 512 Hz or 16.384 kHz pin output
- Watch error correction function
- Subclock operation or main clock operation^{Note 2} selectable

Notes 1. BCD (binary-coded decimal) code is the code that represents each digit of a decimal number in 4-bit binary numerals.

2. The main clock can be divided into 32.768 kHz f_{BRG} with the baud rate generator dedicated to the real-time counter.

The following figure shows the configuration of real-time timer.



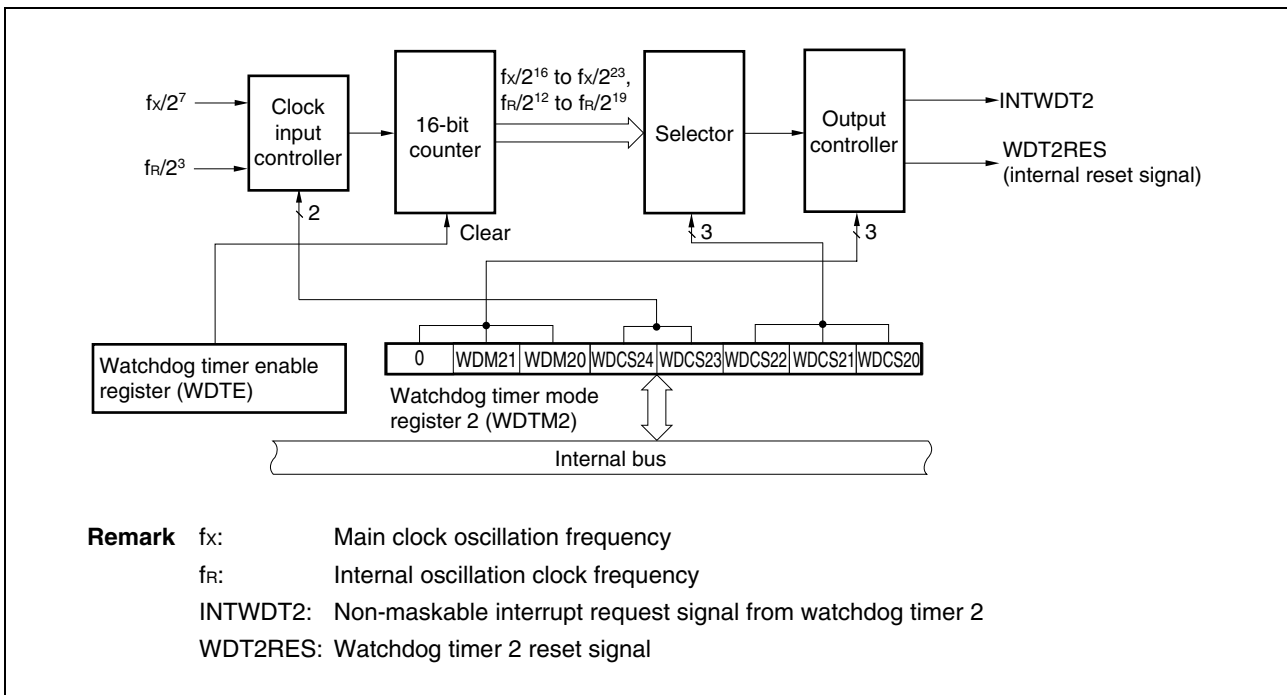
12. WATCHDOG TIMER 2 FUNCTIONS

In the V850ES/Jx3-E, one channel of watchdog timer 2 is provided.

The watchdog timer has the following functions.

- Reset mode: Reset operation upon overflow of watchdog timer (generates the WDT2RES signal)
- Non-maskable interrupt request mode: NMI operation upon overflow of watchdog timer (generates the INTWDT2 signal)

The following figure shows the configuration of the watchdog timer functions.



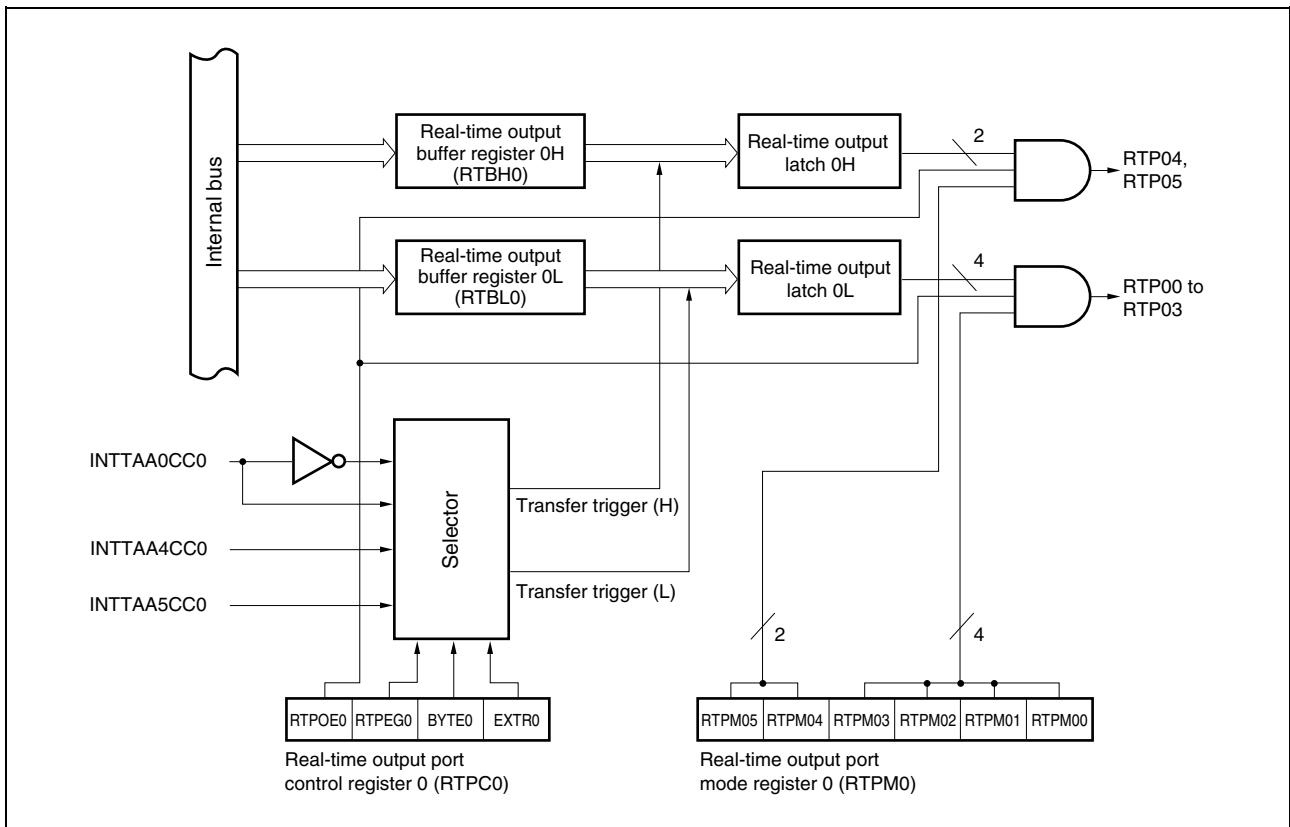
13. REAL-TIME OUTPUT FUNCTION (RTO)

In the V850ES/Jx3-E, one channel of real-time output is provided.

The RTO has the following features.

- 6-bit real-time output port: 1 channel
- The real-time output port can be set to the port mode or real-time output port mode in 1-bit units.

The RTO has the following configurations.



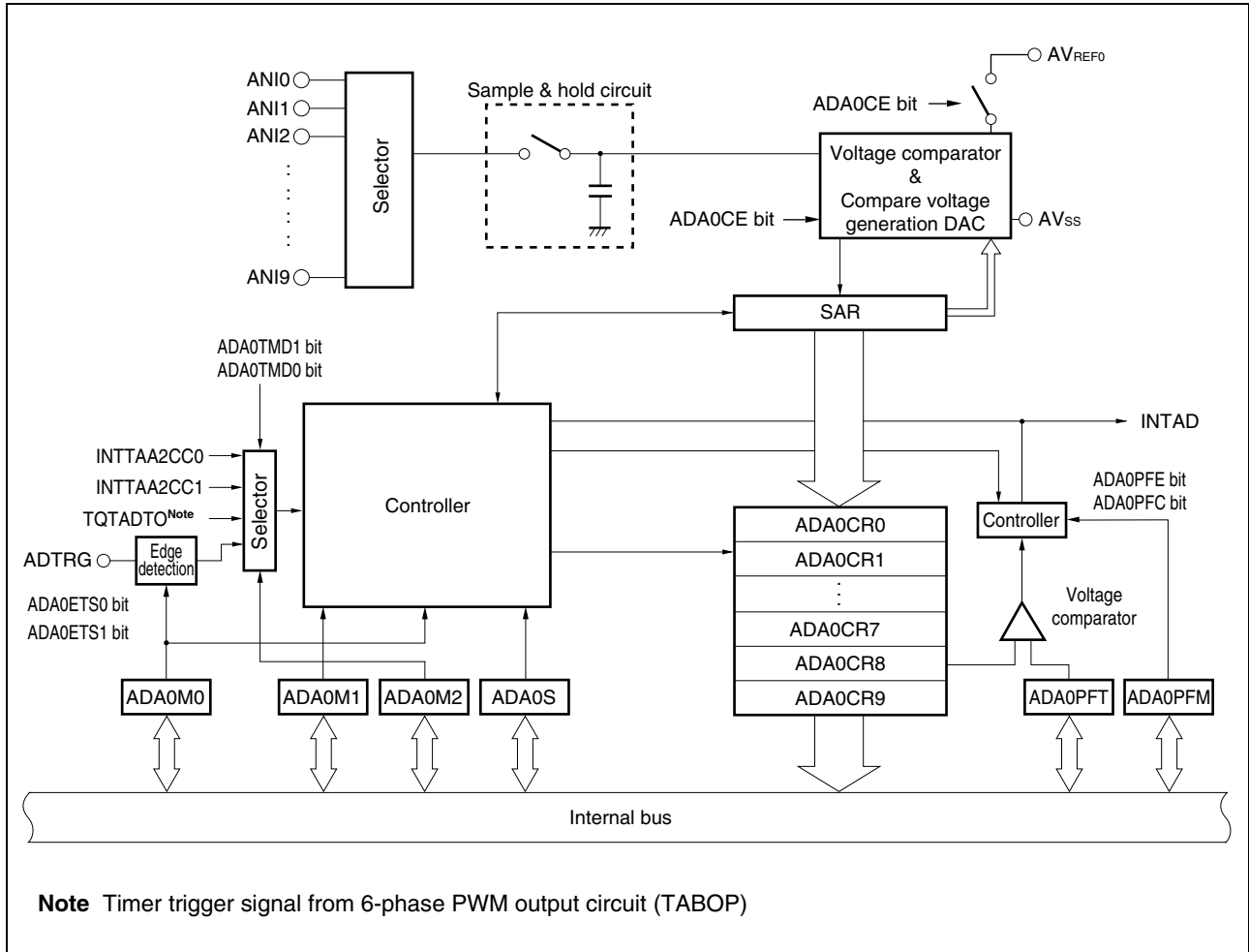
14. A/D CONVERTER

An A/D converter unit with ten channels is provided in the V850ES/Jx3-E.

The A/D converter has the following features.

- 10-bit resolution
- 10 channels
- Successive approximation method
- Operating voltage: $AV_{REF0} = 3.0$ to 3.6 V
- Analog input voltage: 0 V to AV_{REF0}
- The following functions are provided as operation modes.
 - Continuous select mode
 - Continuous scan mode
 - One-shot select mode
 - One-shot scan mode
- The following functions are provided as trigger modes.
 - Software trigger mode
 - External trigger mode (external, 1)
 - Timer trigger mode
- Power-fail monitor function (conversion result compare function)

The following figure shows the configuration of the A/D converter.



15. ASYNCHRONOUS SERIAL INTERFACE C (UARTC)

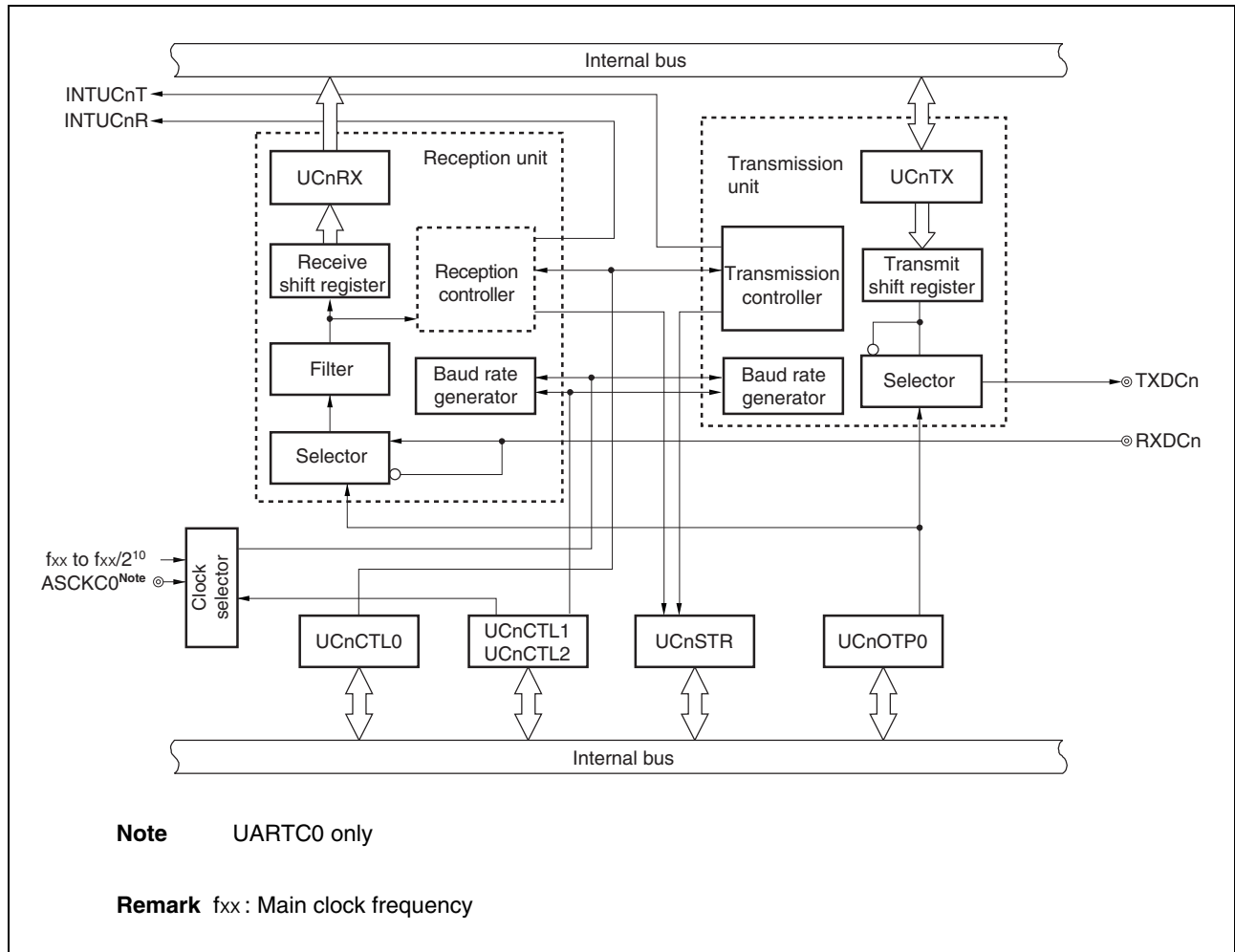
The number of UARTC of the V850ES/Jx3-E is shown below.

| Product Name | V850ES/JF3-E | V850ES/JF-E | V850ES/JG3-E |
|-------------------|---|----------------------------------|----------------------------------|
| Number of channel | 3 channels (UARTC0, UARTC2 and UARTC3) | 4 channels (UARTC0 to UARTC3) | 4 channels (UARTC0 to UARTC3) |

The UARTC has the following features.

- Transfer rate: 300 bps to 3.125 Mbps (using internal system clock of 24 MHz and dedicated baud rate generator)
- Full-duplex communication: On-chip UARTCn receive data register (UCnRX)
On-chip UARTCn transmit data register (UCnTX)
- 2-pin configuration: TXDCn: Transmit data output pin
RXDCn: Receive data input pin
- Reception error detect function
 - Parity error
 - Framing error
 - Overrun error
 - LIN communication data consistency error detect function
 - SBF reception success detect function
- Interrupt sources: 2 types
 - Reception completion interrupt (INTUCnR): This interrupt occurs upon transfer of receive data from the receive shift register to receive data register after serial transfer completion, in the reception enabled status.
 - Transmission enable interrupt (INTUCnT): This interrupt occurs upon transfer of transmit data from the transmit data register to the transmit shift register in the transmission enabled status.
- Character length: 7, 8, 9 bits
- Parity function: Odd, even, 0, none
- Transmission stop bit: 1, 2 bits
- On-chip dedicated baud rate generator
- MSB-/LSB-first transfer selectable
- Transmit/receive data inverted input/output possible
- SBF (Sync Break Field) transmission/reception in the LIN (Local Interconnect Network) communication format possible
 - 13 to 20 bits are selectable for SBF transmission
 - Recognition of 11 bits or more possible for SBF reception in LIN format
 - SBF reception flag provided

The following figure shows the configuration of UARTC.



16. CLOCKED SERIAL INTERFACE F (CSIF)

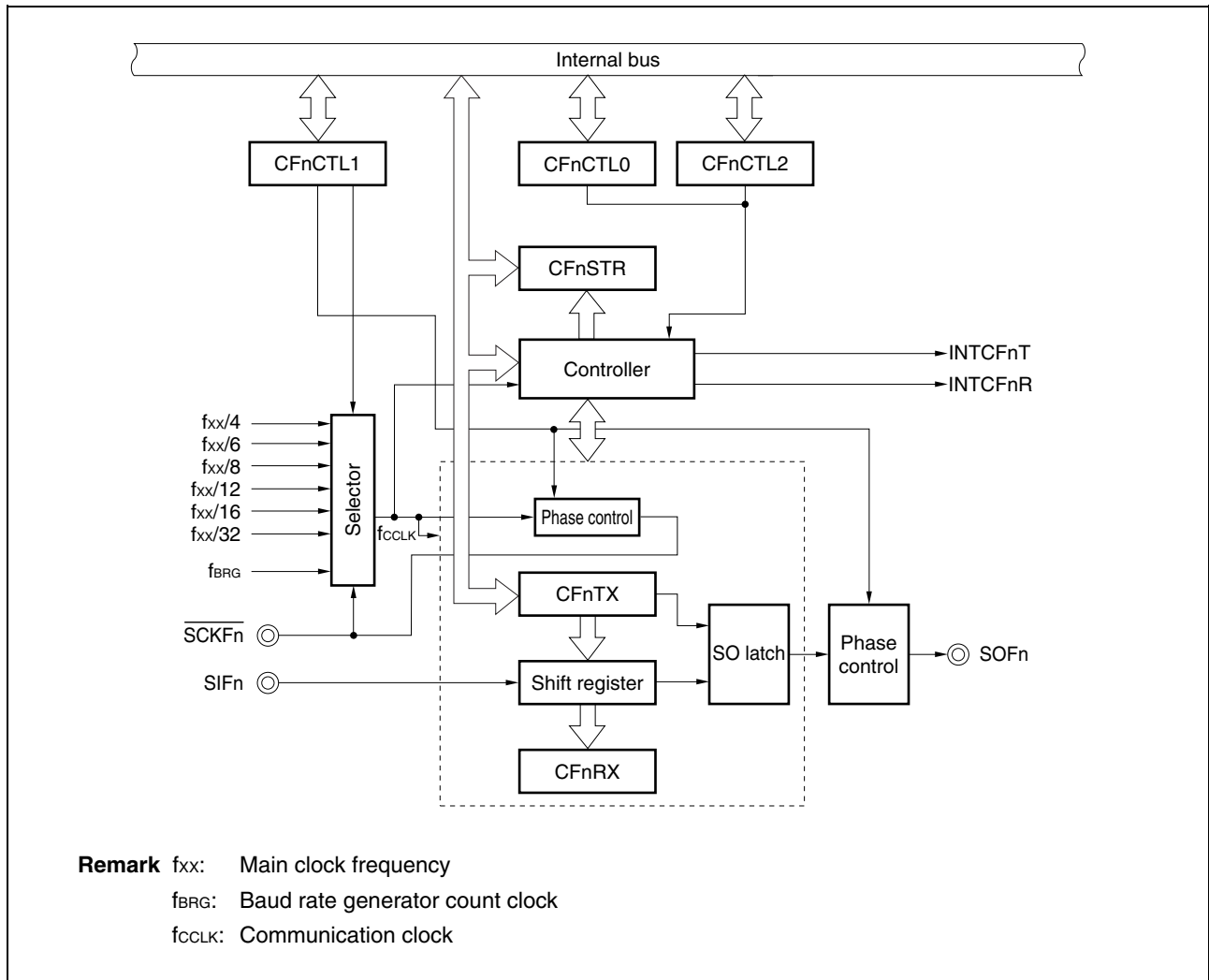
The number of CSIF of the V850ES/Jx3-E is shown below.

| Product Name | V850ES/JF3-E | V850ES/JF-E | V850ES/JG3-E |
|-------------------|---------------------------------|--------------------------------|--------------------------------|
| Number of channel | 2 channels (CSIF0 and CSIF2) | 3 channels (CSIF0 to CSIF2) | 5 channels (CSIF0 to CSIF4) |

- Transfer rate: 8 Mbps max. (f_{xx} = 50 MHz, using internal clock)
- Master mode and slave mode selectable
- 8-bit to 16-bit transfer, 3-wire serial interface
- Interrupt request signals (INTCFnT, INTCFnR)
- Serial clock and data phase switchable
- Transfer data length selectable in 1-bit units between 8 and 16 bits
- Transfer data MSB-first/LSB-first switchable
- 3-wire
 - SOFn: Serial data output
 - SIFn: Serial data input
 - SCKFn: Serial clock I/O

Transmission mode, reception mode, and transmission/reception mode specifiable

The following figure shows the configuration of CSIF.



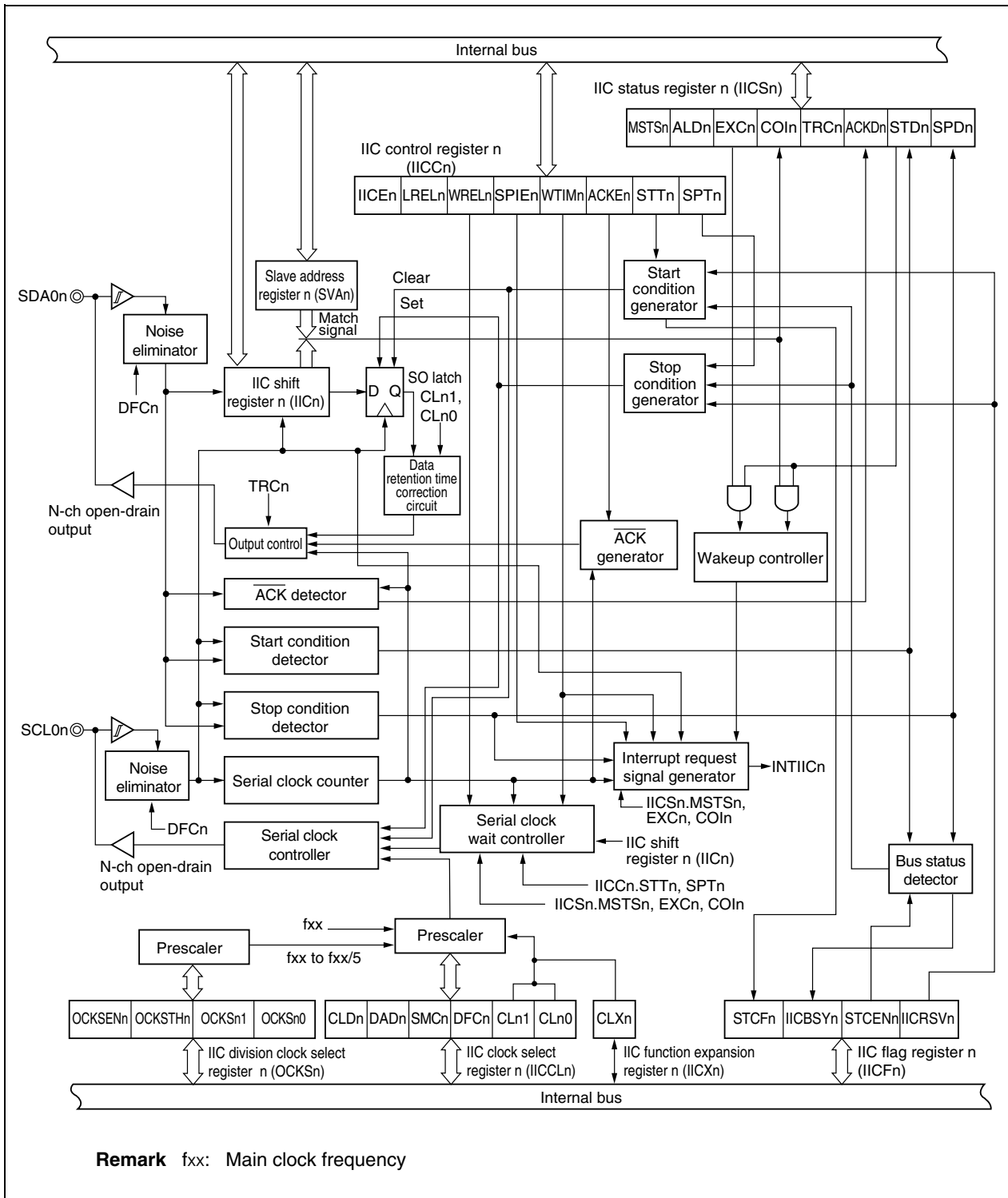
17. I²C BUS

The number of I²C bus of the V850ES/Jx3-E is shown below.

| Product Name | V850ES/JF3-E | V850ES/JF-E | V850ES/JG3-E |
|-------------------|---|--|--|
| Number of channel | 2 channels (I ² C01 and I ² C02) | 3 channels (I ² C00 to I ² C02) | 3 channels (I ² C00 to I ² C02) |

- Transfer rate: Standard mode (100 kbps max.)/high-speed mode (400 kbps max.)
- Conforms to I²C bus format (multimaster supported)
- 2-wire SCL0n: Serial clock pin
SDA0n: Serial data bus pin

The following figure shows the configuration of I²C.

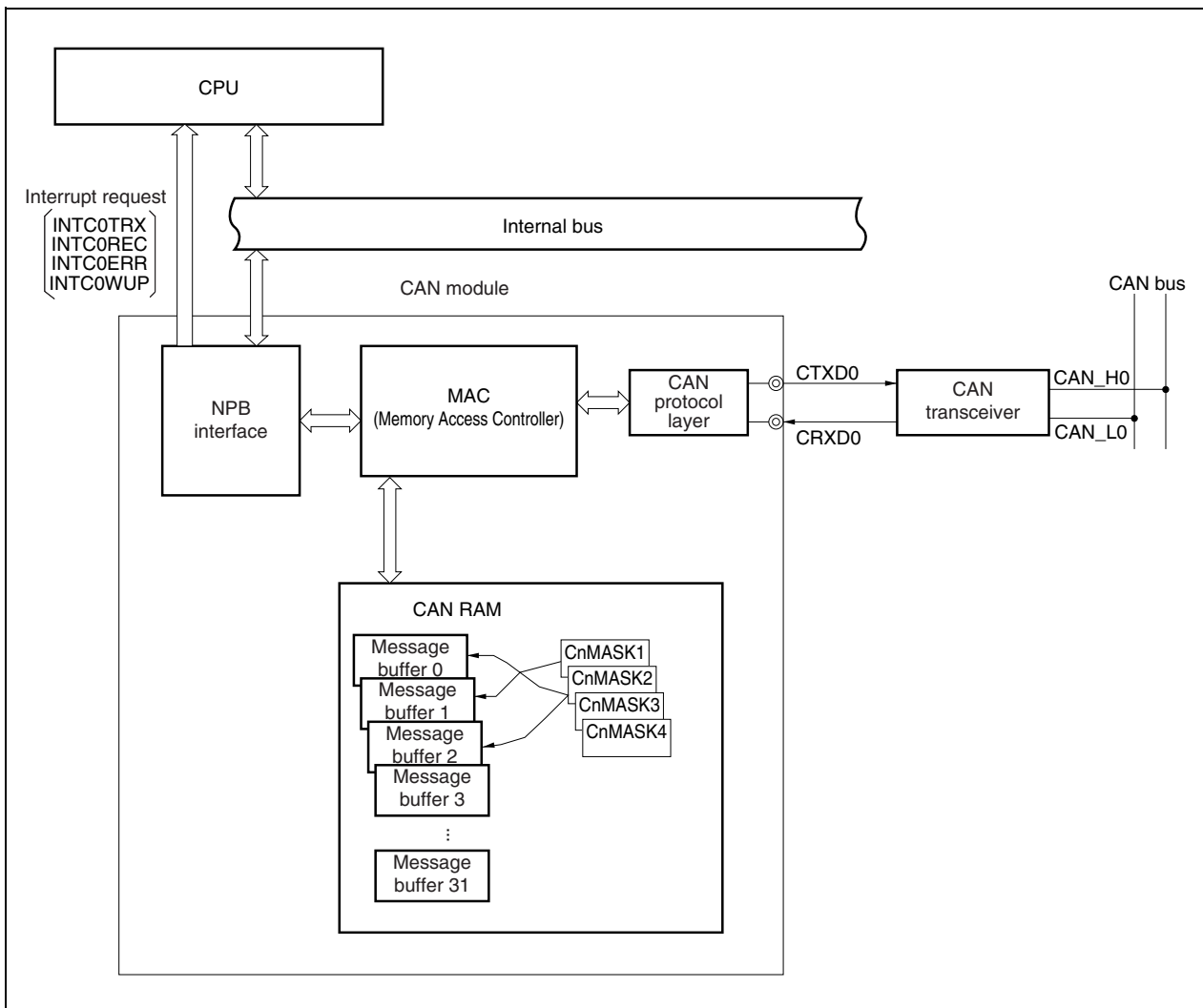


18. CAN CONTROLLER

In the μPD70F3829, 70F3833, 70F3837, one channel of CAN controller is provided.

- Compliant with ISO 11898 and tested according to ISO/DIS 16845 (CAN conformance test)
- Standard frame and extended frame transmission/reception enabled
- Transfer rate: 1 Mbps max. (CAN clock input ≥ 8 MHz)
- 32 message buffers/channels
- Receive/transmit history list function
- Automatic block transmission function
- Multi-buffer receive block function
- Mask setting of four patterns is possible for each channel

The following figure shows the configuration of CAN controller.



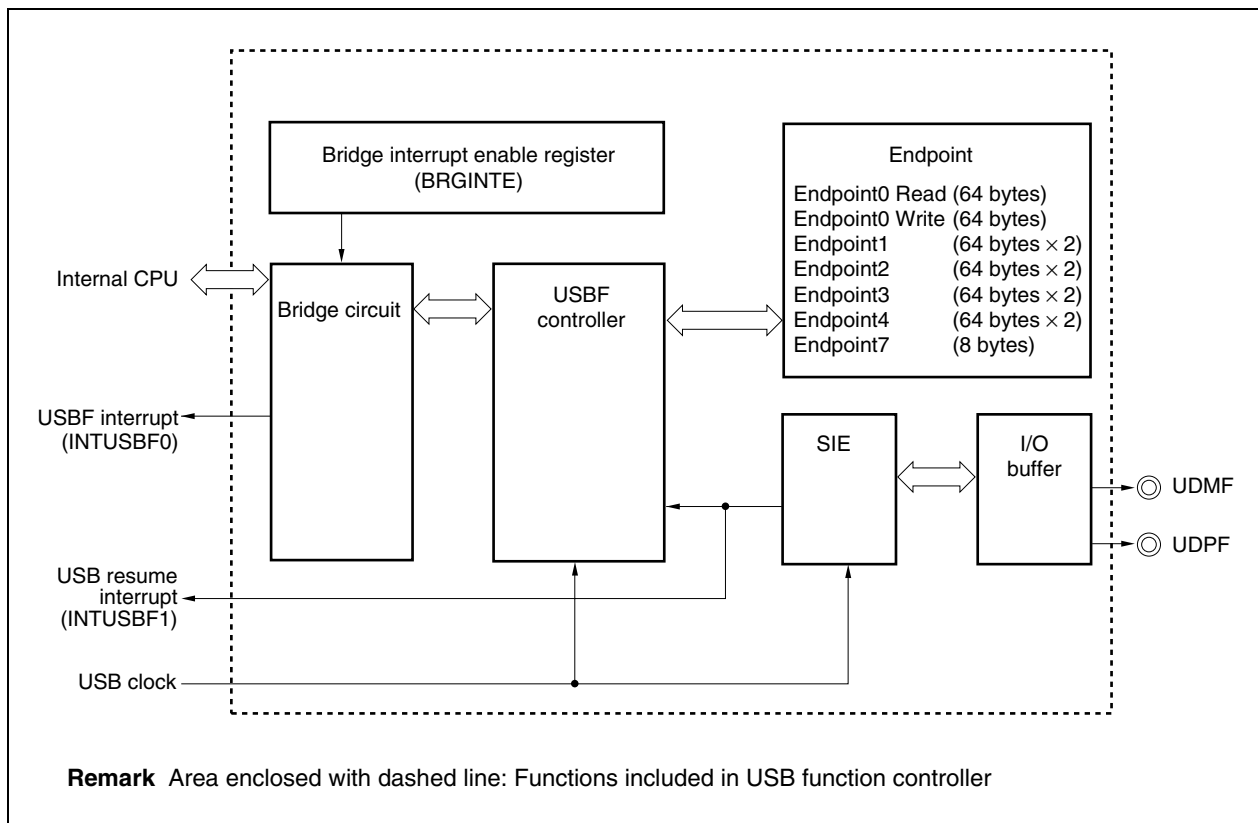
19. USB FUNCTION CONTROLLER (USBF)

In the V850ES/Jx3-E, one channel of USBF is provided.

- Conforms to the Universal Serial Bus (USB) Specification.
- USB 2.0-compatible full-speed transfer (12 Mbps) supported
- Endpoint for transfer incorporated

| Endpoint Name | FIFO Size (Bytes) | Transfer Type | Remark |
|-----------------|-------------------|-------------------------|------------------------|
| Endpoint0 Read | 64 | Control transfer | - |
| Endpoint0 Write | 64 | Control transfer | - |
| Endpoint1 | 64 × 2 | Bulk 1 transfer (IN) | 2-buffer configuration |
| Endpoint2 | 64 × 2 | Bulk 1 transfer (OUT) | 2-buffer configuration |
| Endpoint3 | 64 × 2 | Bulk 2 transfer (IN) | 2-buffer configuration |
| Endpoint4 | 64 × 2 | Bulk 2 transfer (OUT) | 2-buffer configuration |
| Endpoint7 | 8 | Interrupt transfer (IN) | - |

The following figure shows the configuration of USB function controller.

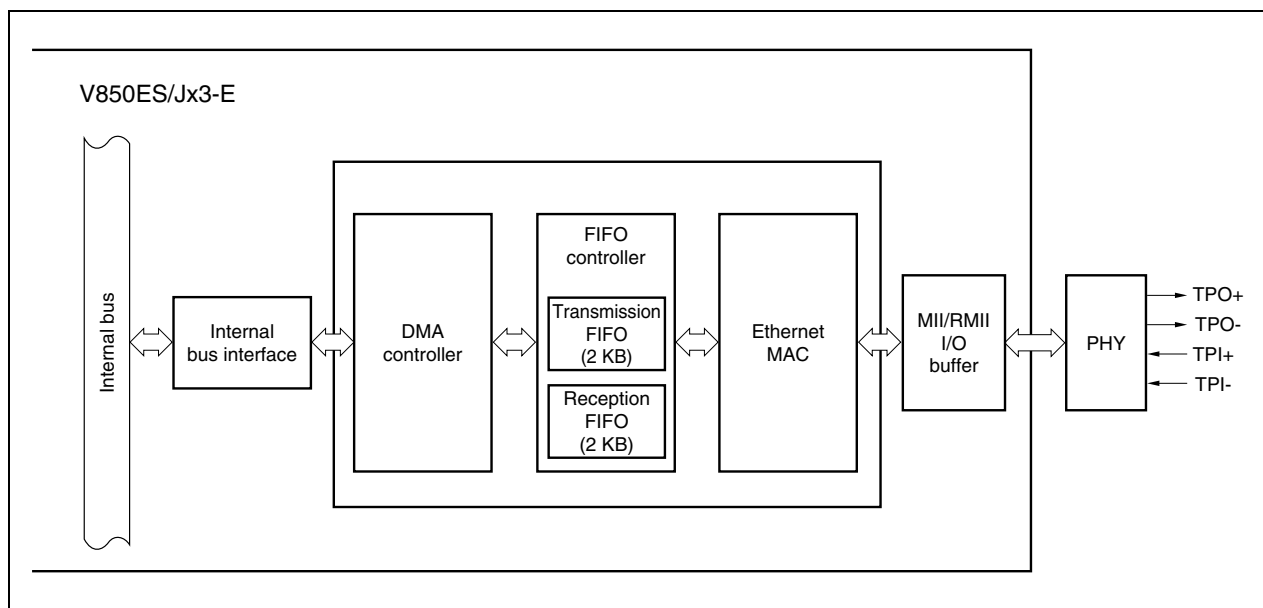


20. ETHERNET CONTROLLER

In the V850ES/Jx3-E, one channel of Ethernet controller is provided.

- 10 Mbps/100 Mbps MAC function conforming to the IEEE802.3 standard
 - Full-duplex and half-duplex communications and a flow control function are supported
 - On-chip packet filtering function based on address type
 - On-chip VLAN detection function
- Ethernet-dedicated DMA controller
 - Reception status DMA transfer possible
 - Reading (in pointer-chain format), analysis, and writing back of buffer descriptors possible
 - Interrupt control functions for packet transfers
- FIFO controller
 - Transmission/reception FIFO size: Transmission FIFO (2 KB), reception FIFO (2 KB)
 - On-chip FIFO status register
 - Interrupts occur in accordance with the transmission/reception status and FIFO status.
- MII is supported as the interface with physical-layer devices (PHY)
- On-chip reception checksum calculation function conforming to RFC1071

The following figure shows the configuration of USB function controller.

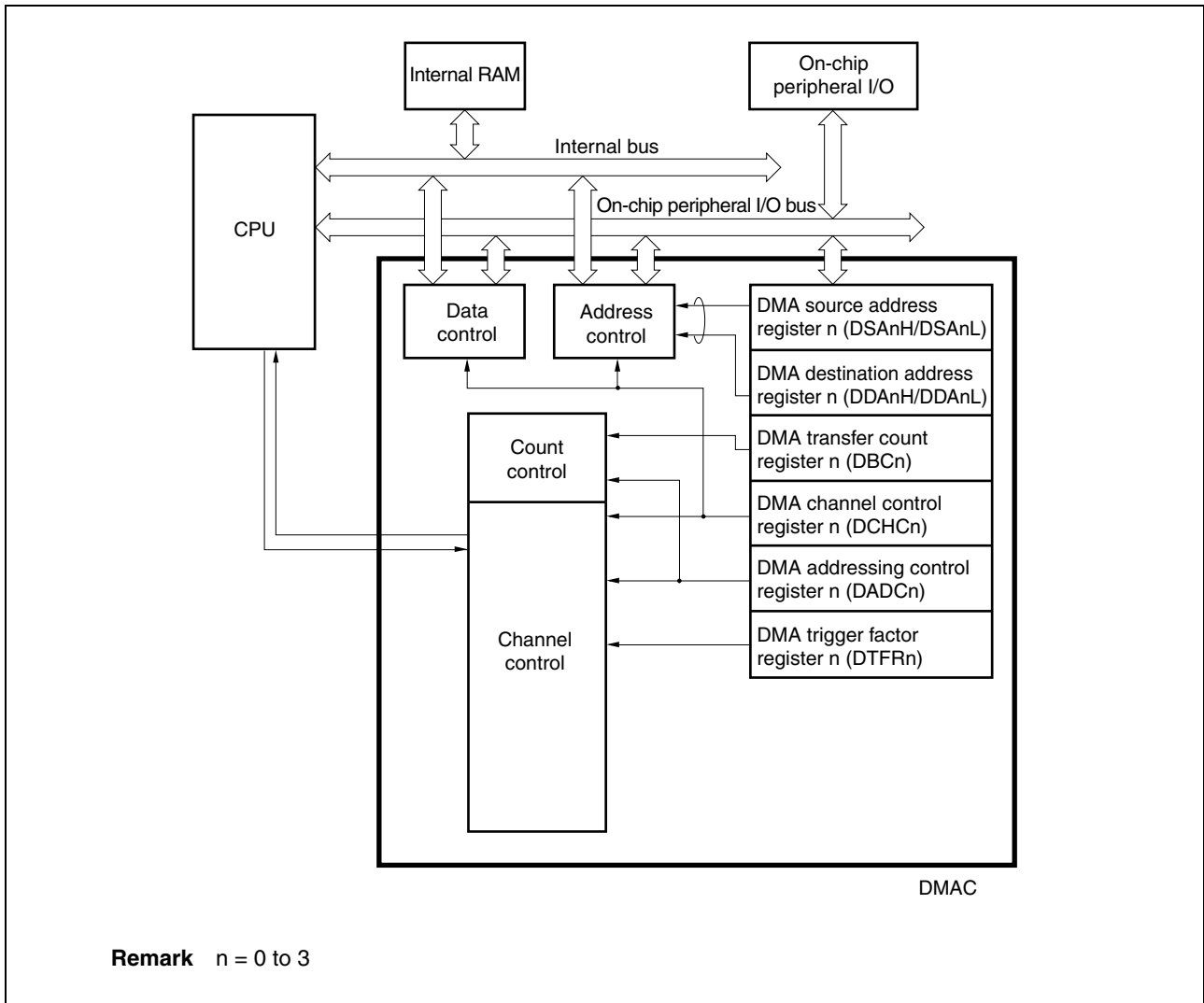


21. DMA CONTROLLER

In the V850ES/Jx3-E, four channels of DMA controller are provided.

- 4 independent DMA channels
- Transfer unit: 8/16 bits
- Maximum transfer count: 65,536 (2^{16})
- Transfer type: Two-cycle transfer
- Transfer mode: Single transfer mode
- Transfer requests
 - Request by interrupts from on-chip peripheral I/O (serial interface, timer/counter, real-time counter, A/D converter) or interrupts from external input pin
 - Requests by software trigger
- Transfer targets
 - Internal RAM \Leftrightarrow Peripheral I/O
 - Peripheral I/O \Leftrightarrow Peripheral I/O

The following figure shows the configuration of DMA controller.



22. INTERRUPT/EXCEPTION PROCESSING FUNCTION

The features of interrupt/exception processing function is shown below.

○ Interrupts

| | | Internal | | | External | | |
|--------------|------------|--------------|----------|-------|--------------|----------|-------|
| | | Non maskable | Maskable | Total | Non maskable | Maskable | Total |
| V850ES/JE3-E | μPD70F3826 | 1 | 53 | 54 | 1 | 6 | 7 |
| | μPD70F3827 | 1 | 53 | 54 | 1 | 6 | 7 |
| | μPD70F3828 | 1 | 53 | 54 | 1 | 6 | 7 |
| | μPD70F3829 | 1 | 57 | 58 | 1 | 6 | 7 |
| V850ES/JF3-E | μPD70F3830 | 1 | 56 | 57 | 1 | 18 | 19 |
| | μPD70F3831 | 1 | 56 | 57 | 1 | 18 | 19 |
| | μPD70F3832 | 1 | 56 | 57 | 1 | 18 | 19 |
| | μPD70F3833 | 1 | 60 | 61 | 1 | 18 | 19 |
| V850ES/JG3-E | μPD70F3834 | 1 | 60 | 61 | 1 | 21 | 22 |
| | μPD70F3835 | 1 | 60 | 61 | 1 | 21 | 22 |
| | μPD70F3836 | 1 | 60 | 61 | 1 | 21 | 22 |
| | μPD70F3837 | 1 | 64 | 65 | 1 | 21 | 22 |

- 8 levels of programmable priorities
- Masks interrupt requests according to priority
- Masks can be specified for each maskable interrupt request.
- Noise elimination, edge detection, and valid edge specification for external interrupt request signals.

○ Exceptions

- Software exceptions: 32 sources
- Exception trap: 2 sources (illegal opcode exception, debug trap)

Interrupt/exception sources are listed in Table 22-1.

Table 22-1. Interrupt Source List (1/3)

| Type | Classification | Default Priority | Name | Trigger | Generating Unit | Interrupt Control Register | JE3E | JF3E | JG3E |
|--------------------|----------------|------------------|-------------------|---|-----------------|----------------------------|------|------|------|
| Reset | Interrupt | – | RESET | RESET pin input/reset input from internal source | RESET | – | √ | √ | √ |
| Non-maskable | Interrupt | – | NMI | NMI pin valid edge input | Pin | – | √ | √ | √ |
| | | – | INTWDT2 | WDT2 overflow | WDT2 | – | √ | √ | √ |
| Software exception | Exception | – | TRAP0n (n = 0-FH) | TRAP instruction | – | – | √ | √ | √ |
| | | – | TRAP1n (n = 0-FH) | TRAP instruction | – | – | √ | √ | √ |
| Exception trap | Exception | – | ILGOP/DBG0 | Illegal instruction code/DBTRAP instruction | – | – | √ | √ | √ |
| Maskable | Interrupt | 0 | INTLVI | Detection of low voltage | POCLVI | LVIIC | √ | √ | √ |
| | | 1 | INTP00 | Detection of external interrupt pin input edge (INTP00) | Pin | PIC0 | | | √ |
| | | 2 | INTP01 | Detection of external interrupt pin input edge (INTP01) | Pin | PIC1 | √ | √ | √ |
| | | 3 | INTP02 | Detection of external interrupt pin input edge (INTP02) | Pin | PIC2 | – | – | √ |
| | | 4 | INTP03 | Detection of external interrupt pin input edge (INTP03) | Pin | PIC3 | – | √ | √ |
| | | 5 | INTP04 | Detection of external interrupt pin input edge (INTP04) | Pin | PIC4 | – | √ | √ |
| | | 6 | INTP05 | Detection of external interrupt pin input edge (INTP05) | Pin | PIC5 | – | √ | √ |
| | | 7 | INTP06 | Detection of external interrupt pin input edge (INTP06) | Pin | PIC6 | – | √ | √ |
| | | 8 | INTP07 | Detection of external interrupt pin input edge (INTP07) | Pin | PIC7 | √ | √ | √ |
| | | 9 | INTP08 | Detection of external interrupt pin input edge (INTP08) | Pin | PIC8 | √ | √ | √ |
| | | 10 | INTP09 | Detection of external interrupt pin input edge (INTP09) | Pin | PIC9 | √ | √ | √ |
| | | 11 | INTP10 | Detection of external interrupt pin input edge (INTP10) | Pin | PIC10 | √ | √ | √ |
| | | 12 | INTP11 | Detection of external interrupt pin input edge (INTP11) | Pin | PIC11 | √ | √ | √ |
| | | 13 | INTP12 | Detection of external interrupt pin input edge (INTP12) | Pin | PIC12 | – | √ | √ |
| | | 14 | INTP13 | Detection of external interrupt pin input edge (INTP13) | Pin | PIC13 | – | √ | √ |
| | | 15 | INTP14 | Detection of external interrupt pin input edge (INTP14) | Pin | PIC14 | – | √ | √ |
| | | 16 | INTP15 | Detection of external interrupt pin input edge (INTP15) | Pin | PIC15 | – | √ | √ |
| | | 17 | INTP16 | Detection of external interrupt pin input edge (INTP16) | Pin | PIC16 | – | √ | √ |
| | | 18 | INTP17 | Detection of external interrupt pin input edge (INTP17) | Pin | PIC17 | – | √ | √ |
| | | 19 | INTP18 | Detection of external interrupt pin input edge (INTP18) | Pin | PIC18 | – | √ | √ |
| | | 20 | INTP19 | Detection of external interrupt pin input edge (INTP19) | Pin | PIC19 | – | √ | √ |
| | | 21 | INTP20 | Detection of external interrupt pin input edge (INTP20) | Pin | PIC20 | – | – | √ |
| | | 32 | INTTAB1OV | TAB1 overflow | TAB1 | TAB1OVIC | √ | √ | √ |
| | | 33 | INTTAB1CC0 | TAB1 capture 0/compare 0 match | TAB1 | TAB1CCIC0 | √ | √ | √ |
| | | 34 | INTTAB1CC1 | TAB1 capture 1/compare 1 match | TAB1 | TAB1CCIC1 | √ | √ | √ |
| | | 35 | INTTAB1CC2 | TAB1 capture 2/compare 2 match | TAB1 | TAB1CCIC2 | √ | √ | √ |
| | | 36 | INTTAB1CC3 | TAB1 capture 3/compare 3 match | TAB1 | TAB1CCIC3 | √ | √ | √ |
| | | 37 | INTTT0OV | TMT0 overflow | TMT0 | TT0OVIC | √ | √ | √ |
| | | 38 | INTTT0CC0 | TMT0 capture 0/compare 0 match | TMT0 | TT0CCIC0 | √ | √ | √ |
| | | 39 | INTTT0CC1 | TMT0 capture 1/compare 1 match | TMT0 | TT0CCIC1 | √ | √ | √ |
| | | 40 | INTTT0EC | TMT0 encoder input | TMT0 | TT0ECIC | – | – | √ |

Table 22-1. Interrupt Source List (2/3)

| Type | Classification | Default Priority | Name | Trigger | Generating Unit | Interrupt Control Register | JE3E | JF3E | JG3E |
|----------|----------------|---|---------------------------------|--|---------------------------|------------------------------|------|------|------|
| Maskable | Interrupt | 41 | INTTAA0OV | TAA0 overflow | TAA0 | TAA0OVIC | √ | √ | √ |
| | | 42 | INTTAA0CC0 | TAA0 capture 0/compare 0 match | TAA0 | TAA0CCIC0 | √ | √ | √ |
| | | 43 | INTTAA0CC1 | TAA0 capture 1/compare 1 match | TAA0 | TAA0CCIC1 | √ | √ | √ |
| | | 44 | INTTAA1OV | TAA1 overflow | TAA1 | TAA1OVIC | √ | √ | √ |
| | | 45 | INTTAA1CC0 | TAA1 capture 0/compare 0 match | TAA1 | TAA1CCIC0 | √ | √ | √ |
| | | 46 | INTTAA1CC1 | TAA1 capture 1/compare 1 match | TAA1 | TAA1CCIC1 | √ | √ | √ |
| | | 47 | INTTAA2OV | TAA2 overflow | TAA2 | TAA2OVIC | √ | √ | √ |
| | | 48 | INTTAA2CC0 | TAA2 capture 0/compare 0 match | TAA2 | TAA2CCIC0 | √ | √ | √ |
| | | 49 | INTTAA2CC1 | TAA2 capture 1/compare 1 match | TAA2 | TAA2CCIC1 | √ | √ | √ |
| | | 50 | INTTAA3OV | TAA3 overflow | TAA3 | TAA3OVIC | √ | √ | √ |
| | | 51 | INTTAA3CC0 | TAA3 capture 0/compare 0 match | TAA3 | TAA3CCIC0 | √ | √ | √ |
| | | 52 | INTTAA3CC1 | TAA3 capture 1/compare 1 match | TAA3 | TAA3CCIC1 | √ | √ | √ |
| | | 53 | INTTAA4OV | TAA4 overflow | TAA4 | TAA4OVIC | √ | √ | √ |
| | | 54 | INTTAA4CC0 | TAA4 capture 0/compare 0 match | TAA4 | TAA4CCIC0 | √ | √ | √ |
| | | 55 | INTTAA4CC1 | TAA4 capture 1/compare 1 match | TAA4 | TAA4CCIC1 | √ | √ | √ |
| | | 59 | INTTM0EQ0 | TMM0 compare match | TMM0 | TM0EQIC0 | √ | √ | √ |
| | | 60 | INTTM1EQ0 | TMM1 compare match | TMM1 | TM1EQIC0 | √ | √ | √ |
| | | 61 | INTTM2EQ0 | TMM2 compare match | TMM2 | TM2EQIC0 | √ | √ | √ |
| | | 62 | INTTM3EQ0 | TMM3 compare match | TMM3 | TM3EQIC0 | √ | √ | √ |
| | | 67 | INTCF0R /INTUC3R /INTIIC1 | CSIF0 transfer completion/UARTC3 reception completion/UARTC3 reception error/IIC1 transfer completion | CSIF0 /UARTC3 /IIC1 | CE0RIC /UC3RIC /IIC1C1 | √ | √ | √ |
| | | 68 | INTCF0T /INTUC3T | CSIF0 continuous transfer write enable/ UARTC3 continuous transfer write enable | CSIF0 /UARTC3 | CF0TIC /UC3TIC | √ | √ | √ |
| | | 69 | INTCF1R /INTUC1R /INTIIC0 | CSIF1 reception completion/ CSIF1 reception error /UARTC1 reception completion/UARTC1 reception error/IIC0 transfer completion | CSIF1 /UARTC1 /IIC0 | CF1RIC /UC1RIC /IIC0C0 | - | - | √ |
| | | 70 | INTCF1T /INTUC1T | CSIF1 continuous transfer write enable/ UARTC1 continuous transfer write enable | CSIF1 /UARTC1 | CF1TIC /UC1TIC | - | - | √ |
| | | 71 | INTCF2R /INTUC0R | CSIF2 reception completion/CSIF2 reception error/ UARTC0 reception completion/UARTC0 reception error | CSIF2 /UARTC0 | CF2RIC /UC0RIC | √ | √ | √ |
| | | 72 | INTCF2T /INTUC0T | CSIF2 continuous transfer write enable/UARTC0 continuous transfer write enable | CSIF2 /UARTC0 | CF2TIC /UC0TIC | √ | √ | √ |
| | | 73 | INTCF3R | CSIF3 reception completion/CSIF3 reception error | CSIF3 | CF3RIC | - | √ | √ |
| | | 74 | INTCF3T | CSIF3 continuous transfer write enable | CSIF3 | CF3TIC | - | √ | √ |
| | | 78 | INTCF4R | CSIF4 reception completion/CSIF4 reception error | CSIF4 | CF4RIC | - | √ | √ |
| | | 79 | INTCF4T | CSIF4 continuous transfer write enable | CSIF4 | CF4TIC | - | √ | √ |
| | | 87 | INTUC2R /INTIIC2 | UARTC2 reception completion/UARTC2 reception error/IIC2 transfer completion | UARTC2 /IIC2 | UC2RIC /IIC2C2 | √ | √ | √ |
| 88 | INTUC2T | UARTC2 continuous transfer write enable | UARTC2 | UC2TIC | √ | √ | √ | | |
| 90 | INTAD | A/D converter completion | A/D | ADIC | √ | √ | √ | | |

Table 22-1. Interrupt/Exception Source List (3/3)

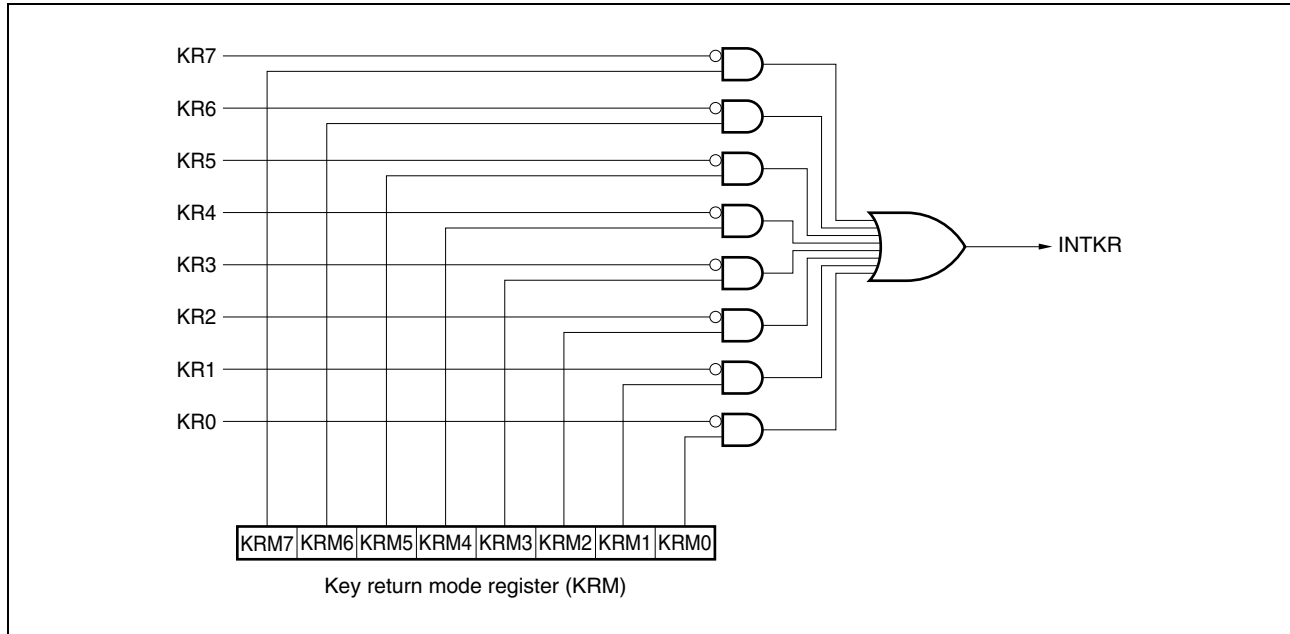
| Type | Classification | Default Priority | Name | Trigger | Generating Unit | Interrupt Control Register | JE3E | JF3E | JG3E |
|----------|----------------|-------------------|-----------|------------------------------|---------------------|----------------------------|---------------------|---------------------|---------------------|
| Maskable | Interrupt | 91 | INTDMA0 | DMA0 transfer completion | DMA | DMAIC0 | √ | √ | √ |
| | | 92 | INTDMA1 | DMA1 transfer completion | DMA | DMAIC1 | √ | √ | √ |
| | | 93 | INTDMA2 | DMA2 transfer completion | DMA | DMAIC2 | √ | √ | √ |
| | | 94 | INTDMA3 | DMA3 transfer completion | DMA | DMAIC3 | √ | √ | √ |
| | | 95 | INTKR | Key return interrupt | KR | KRIC | √ | √ | √ |
| | | 96 | INTRTC0 | RTC fixed-cycle signal | RTC | RTC0IC | √ | √ | √ |
| | | 97 | INTRTC1 | RTC alarm match | RTC | RTC1IC | √ | √ | √ |
| | | 98 | INTRTC2 | RTC interval signal | RTC | RTC2IC | √ | √ | √ |
| | | 99 | INTUSBF0 | USB interrupt | USB | UFIC0 | √ | √ | √ |
| | | 100 | INTUSBF1 | USB resume interrupt | USB | UFIC1 | √ | √ | √ |
| | | 101 | INTEMRX | Packet reception | Ethernet | ETMRXIC | √ | √ | √ |
| | | 102 | INTEMTX | Packet transmission | Ethernet | ETMTXIC | √ | √ | √ |
| | | 103 | INTEMRQ | Received packet read request | Ethernet | ETMRQIC | √ | √ | √ |
| | | 104 | INTEMF5 | FIFO status | Ethernet | ETMFSIC | √ | √ | √ |
| | | 105 | INTEMTS | Transmission status | Ethernet | ETMTSIC | √ | √ | √ |
| | | 106 | INTEMRS | Reception status | Ethernet | ETMRSIC | √ | √ | √ |
| | | 107 | INTEMOV | Statistic counter overflow | Ethernet | ETMOVIC | √ | √ | √ |
| | | 108 | INTEBER | Error interrupt | Ethernet | ETBERIC | √ | √ | √ |
| | | 110 | INTC0ERR | CAN0 error | CAN0 | ERRIC0 | √ ^{Note 1} | √ ^{Note 2} | √ ^{Note 3} |
| | | 111 | INTC0WUP1 | CAN0 wakeup | CAN0 | WUPIC0 | √ ^{Note 1} | √ ^{Note 2} | √ ^{Note 3} |
| 112 | INTC0REC | CAN0 reception | CAN0 | RECIC0 | √ ^{Note 1} | √ ^{Note 2} | √ ^{Note 3} | | |
| 113 | INTC0TRX | CAN0 transmission | CAN0 | TRXIC0 | √ ^{Note 1} | √ ^{Note 2} | √ ^{Note 3} | | |

- Notes 1. μ PD70F3829 only
 2. μ PD70F3833 only
 3. μ PD70F3837 only

23. KEY INTERRUPT FUNCTION (V850ES/JF3-E, V850ES/JG3-E)

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7).

The following figure shows the configuration of key interrupt.



24. STANDBY FUNCTION

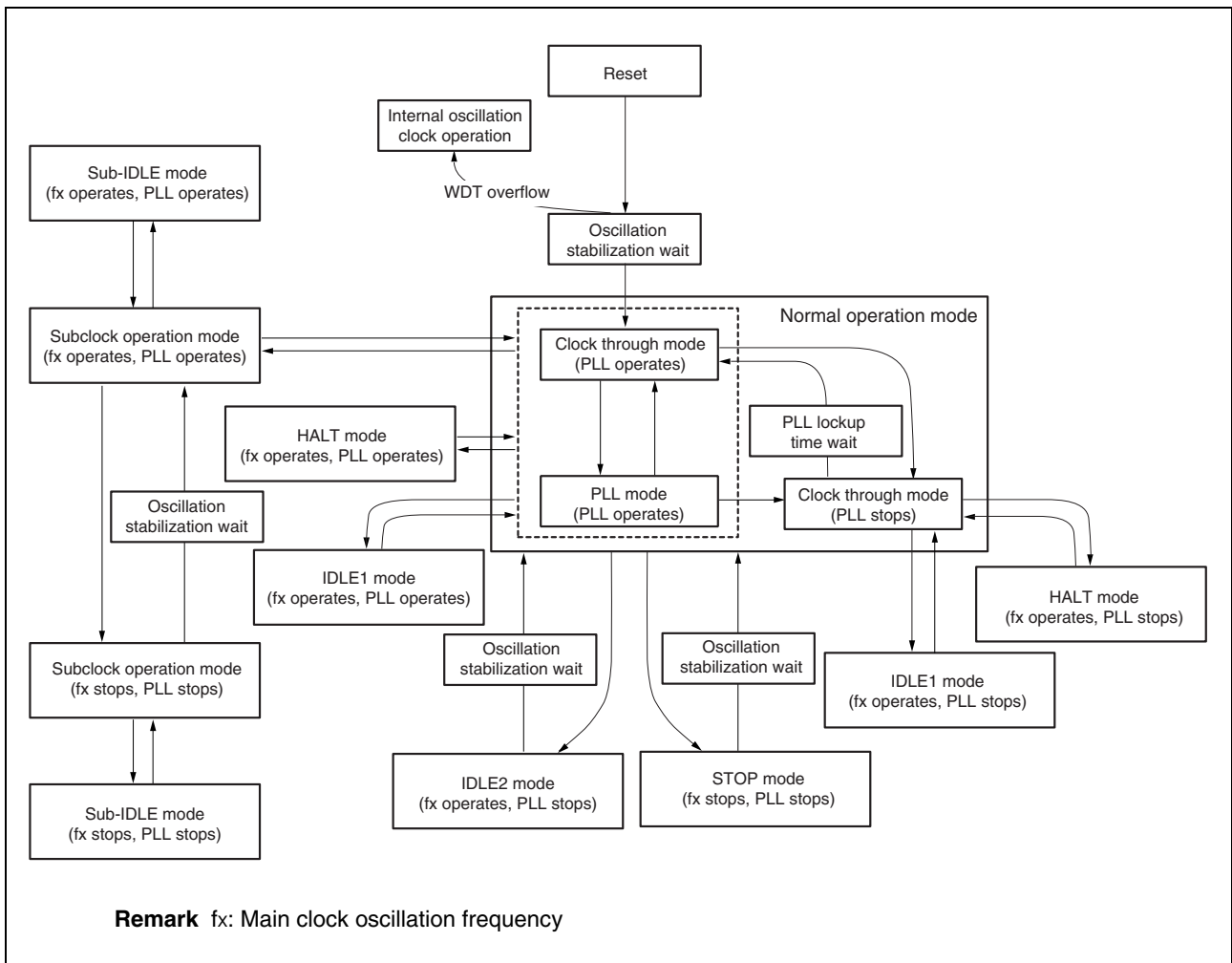
The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. The available standby modes are listed in Table 24-1.

Table 24-1. Standby Modes

| Mode | Function Overview |
|-------------------------|---|
| HALT mode | Mode to stop only the operating clock of the CPU |
| IDLE1 mode | Mode to stop all the operations of the internal circuit except the oscillator, PLL operation ^{Note} , and flash memory |
| IDLE2 mode | Mode to stop all the operations of the internal circuit except the oscillator |
| STOP mode | Mode to stop all the operations of the internal circuit except the subclock oscillator |
| Subclock operation mode | Mode to operate internal system clock by subclock |
| Sub-IDLE mode | Mode to stop all the operations of the internal circuit except the oscillator in subclock operation mode |

Note PLL retains the previous operation status.

The following figure shows the status transitions of the standby function.



26. CLOCK MONITOR, LOW-VOLTAGE DETECTOR

(1) Clock monitor

The clock monitor samples the main clock by using the internal oscillation clock (f_R) and generates a reset request signal when oscillation of the main clock is stopped.

(2) Low-voltage detector

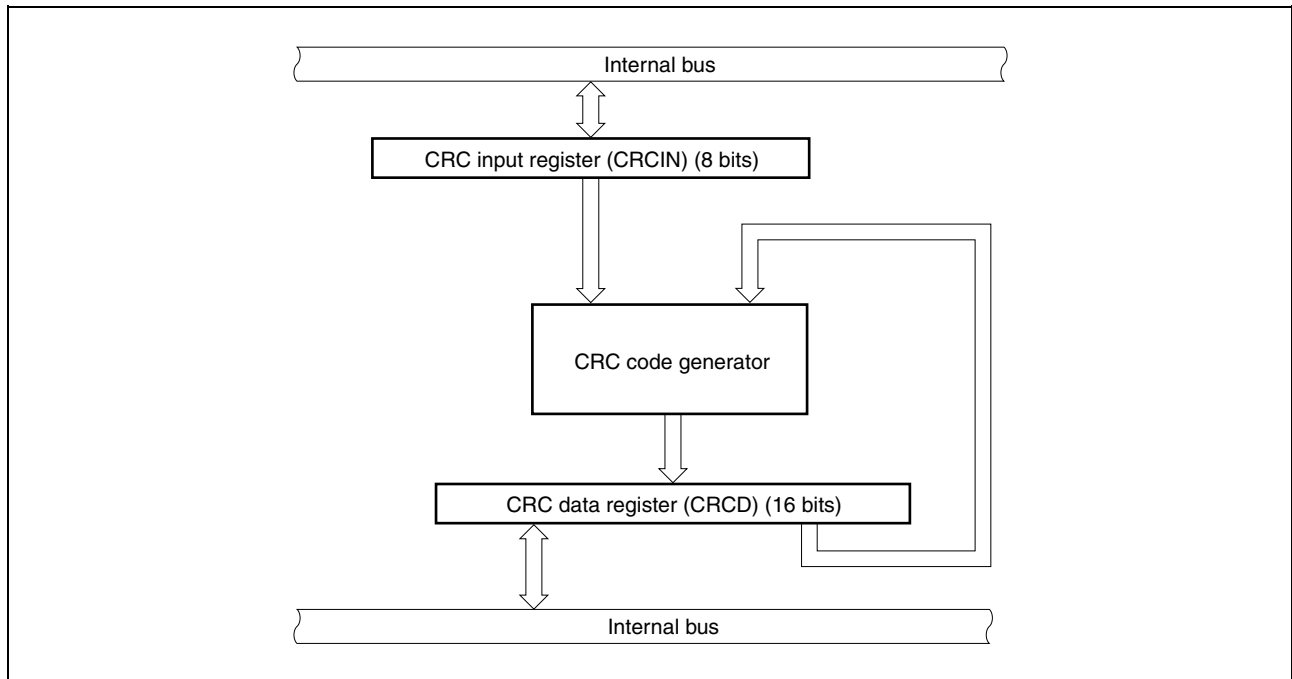
The low-voltage detector (LVI) has the following functions.

- Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}) and generates an interrupt request signal or internal reset signal when $V_{DD} < V_{LVI}$.
- An interrupt request signal or internal reset signal can be selected.
- Can operate in STOP mode.
- Operation can be stopped by software.

27. CRC FUNCTIONS

The outline of the CRC function is shown below.

- CRC operation circuit for detection of data block errors
- Generation of 16-bit CRC code using a CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) generation polynomial for blocks of data of any length in 8-bit units
- CRC code is set to the CRCD data register each time 1-byte data is transferred to the CRCIN register, after the initial value is set to the CRCD register.

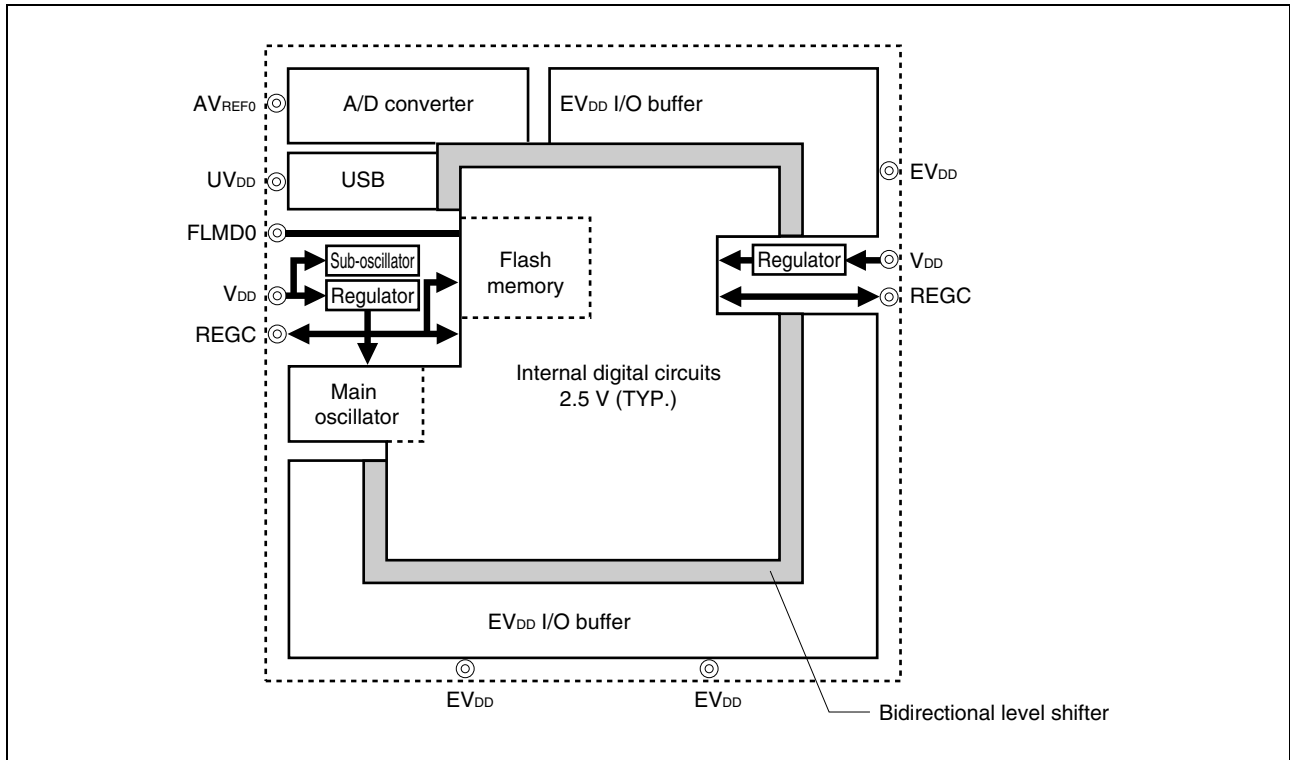


28. REGULATOR FUNCTION

The V850ES/Jx3-E includes a regulator to reduce power consumption and noise.

This regulator supplies a stepped-down V_{DD} power supply voltage to the oscillator block and internal logic circuits except the A/D converter and output buffers). The regulator output voltage is set to 2.5 V (TYP.).

The outline of the regulator functions is shown below.



29. FLASH MEMORY

Flash memory versions offer the following advantages for development environments and mass production applications.

- For altering software after the V850ES/Jx3-E is soldered onto the target system.
- For data adjustment when starting mass production.
- For differentiating software according to the specification in small scale production of various models.
- For facilitating inventory management.
- For updating software after shipment.

The flash memory in the V850ES/Jx3-E has the following features.

- 4-byte/1-clock access (when instruction is fetched)
- Memory size: 64/128/256 KB
- Rewrite voltage: Erase/write with a single power supply
- Rewriting method
 - Rewriting by communication with dedicated flash programmer via serial interface (on-board/off-board programming)
 - Rewriting flash memory by user program (self programming)
- Flash memory write prohibit function supported (security function)
- Safe rewriting of entire flash memory area by self programming using boot swap function
- Interrupts can be acknowledged during self programming.

30. ON-CHIP DEBUG FUNCTION

Debugging can be implemented with the V850ES/Jx3-E mounted on the target system.

The NEC Electronics on-chip debug emulators MINICUBE and MINICUBE2 are planned to support the V850ES/Jx3-E.

○ MINICUBE

An on-chip debug function is implemented by using the DCU (debug control unit) in the V850ES/Jx3-E, using the $\overline{\text{DRST}}$, DCK, DMS, DDI, and DDO pins as the debug interface pins.

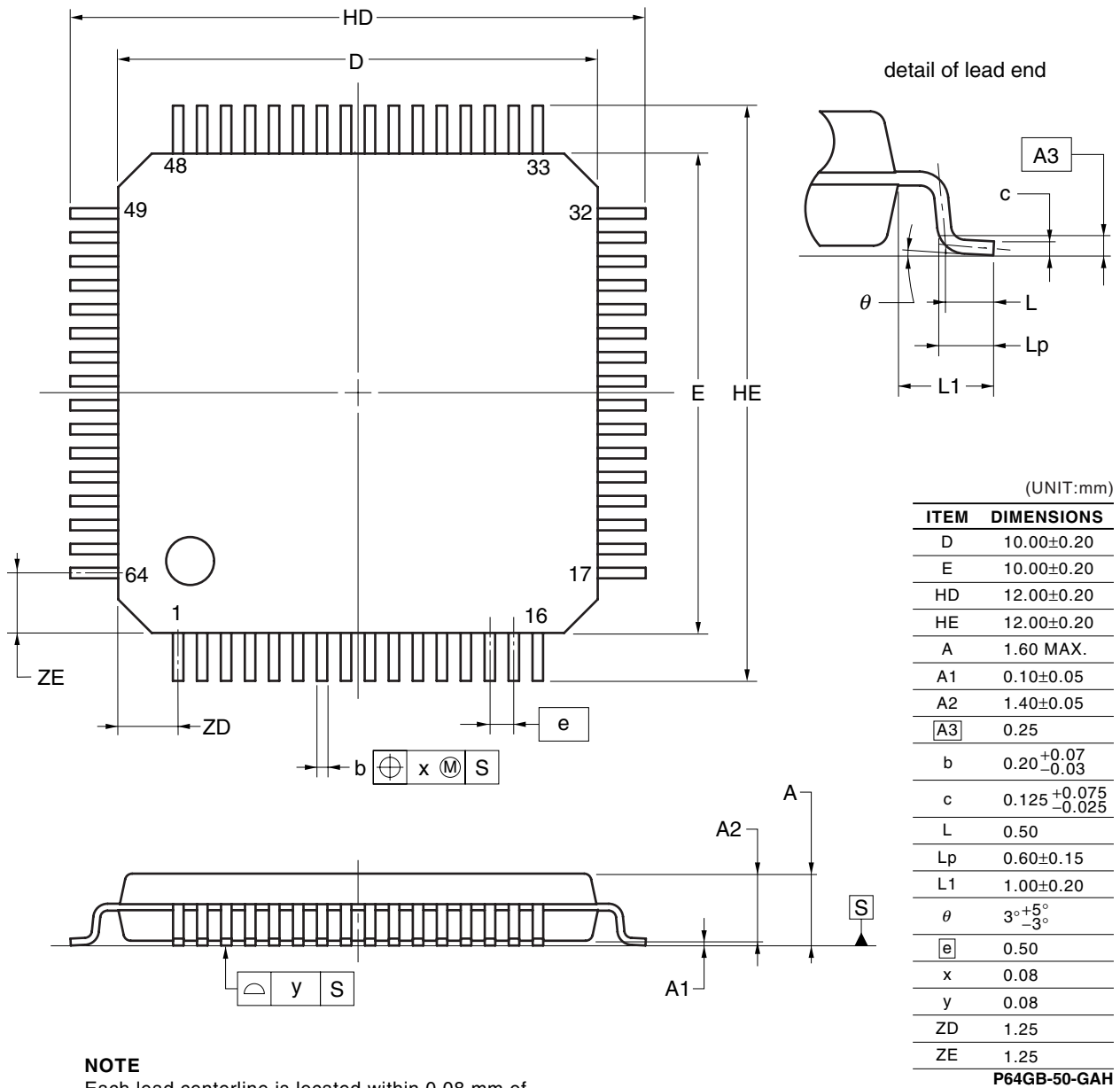
○ MINICUBE2

An on-chip debug function is implemented by using the user resources (on-chip flash memory, internal RAM, etc.) instead of the DCU, and using the SIF0, SOF0, and $\overline{\text{SCKF0}}$ pins or the SIF3, SOF3, and $\overline{\text{SCKF3}}$ pins or the RXDC0 and TXDC0 pins as the interface pins.

31. PACKAGE DRAWINGS

- V850ES/JE3-E

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)

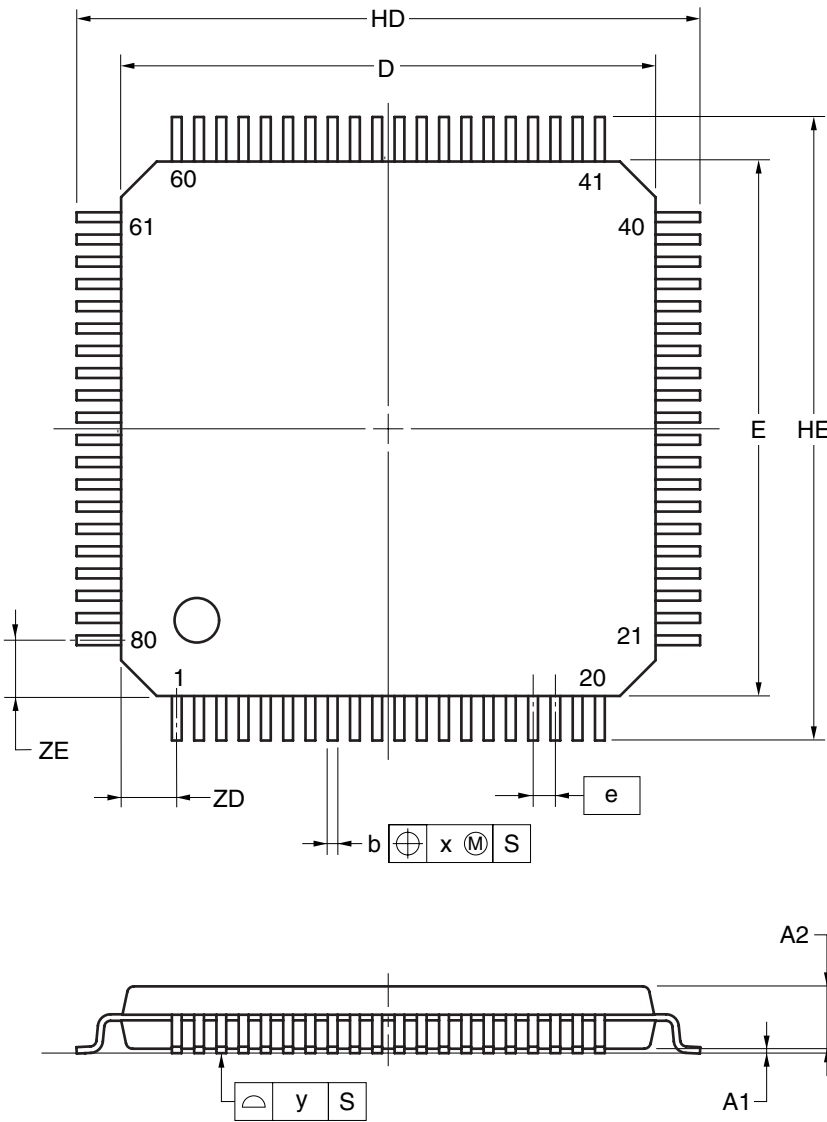


NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

• V850ES/JF3-E

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)



detail of lead end

(UNIT:mm)

| ITEM | DIMENSIONS |
|------|---|
| D | 12.00±0.20 |
| E | 12.00±0.20 |
| HD | 14.00±0.20 |
| HE | 14.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.20 ^{+0.07} _{-0.03} |
| c | 0.125 ^{+0.075} _{-0.025} |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | 3° ^{+5°} _{-3°} |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.25 |
| ZE | 1.25 |

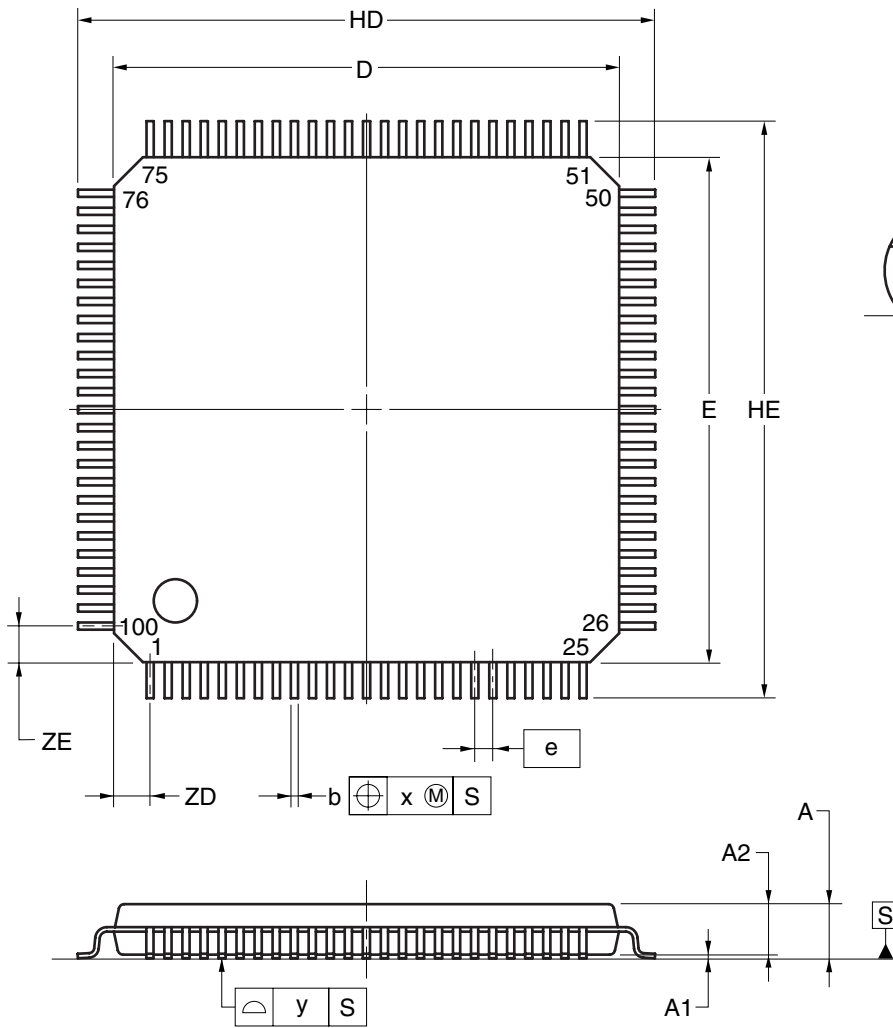
P80GK-50-GAK

NOTE

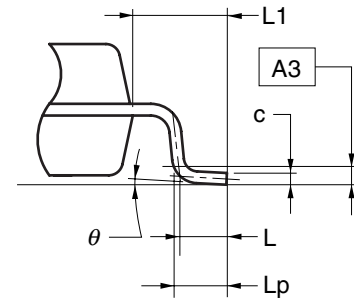
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

- V850ES/JG3-E

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end



(UNIT:mm)

| ITEM | DIMENSIONS |
|------|---|
| D | 14.00±0.20 |
| E | 14.00±0.20 |
| HD | 16.00±0.20 |
| HE | 16.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.20 ^{+0.07} _{-0.03} |
| c | 0.125 ^{+0.075} _{-0.025} |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | 3° ^{+5°} _{-3°} |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.00 |
| ZE | 1.00 |

P100GC-50-UEU-1

| | |
|-------------------------|--|
| Revision History | μ PD70F3826, 70F3827, 70F3828, 70F3829, 70F3830, 70F3831, 70F3832, 70F3833, 70F3834, 70F3835, 70F3836, 70F3837 Data Sheet |
|-------------------------|--|

| Rev. | Date | Description | |
|------|--------------|-------------|-----------------------|
| | | Page | Summary |
| 0.01 | Sep 30, 2010 | – | First Eddition Issued |
| | | | |

All documents should contain the following section break and paragraph as the last item. The footers of this document refer to the paragraph in order to reference the last page of the document.

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhichunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852-2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan, R.O.C.
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Laviel'or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141