

BB506M

Build in Biasing Circuit MOS FET IC UHF RF Amplifier

R07DS0289EJ0200 (Previous: REJ03G1604-0100) Rev.2.00 Mar 28, 2011

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- High gain
- PG = 24 dB typ. (f = 900 MHz)
- Low noise NF = 1.4 dB typ. (f = 900 MHz)
- Low output capacitance
 - Coss = 1.1 pF typ. (f = 1 MHz)
- Provide mini mold packages: MPAK-4 (SOT-143mod)

Outline

RENESAS Package code: PLSP0004ZA-A (Package name: MPAK-4)



1. Source 2. Gate1 3. Gate2 4. Drain

Notes: 1. Marking is "FS-".

2. BB506M is individual type number of RENESAS BBFET.

Absolute Maximum Ratings

 $(Ta = 25^{\circ}C)$ Item Symbol Ratings Unit Drain to source voltage V_{DS} 6 V V Gate1 to source voltage V_{G1S} +6 -0 V Gate2 to source voltage V_{G2S} +6 -0 Drain current 30 I_D mΑ Pch^{Note3} Channel power dissipation 300 mW Channel temperature Tch 150 °C Storage temperature Tstg -55 to +150 °C

Notes: 3. Value on the glass epoxy board (50 mm \times 40 mm \times 1 mm).

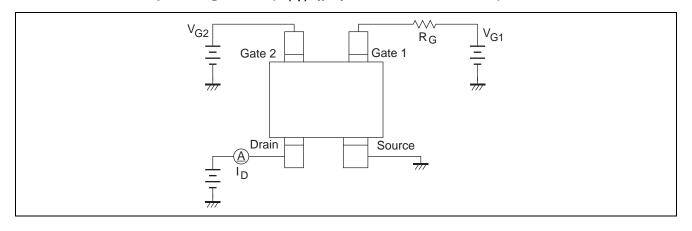
This device is sensitive to electro static discharge. An adequate careful handling procedure is requested.



Electrical Characteristics

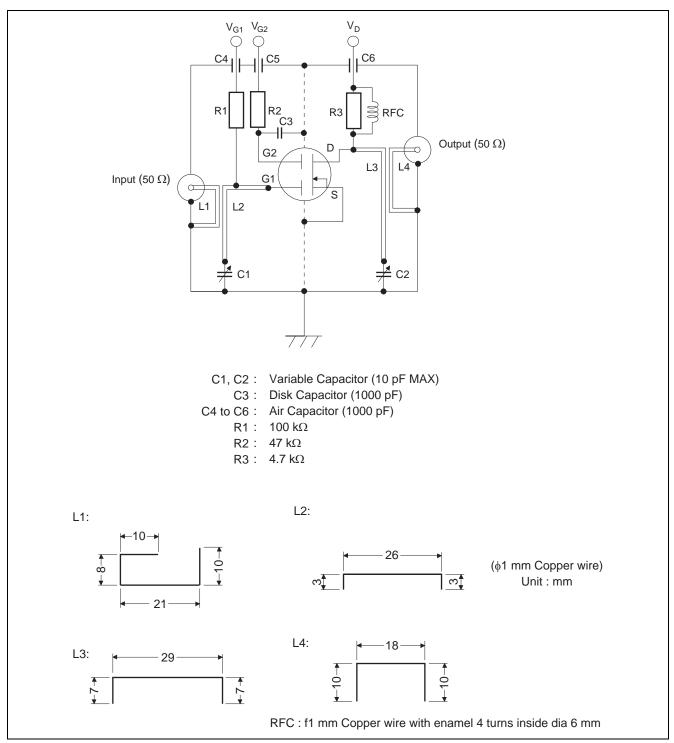
						$(Ta = 25^{\circ}C)$
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	6	—		V	$I_D = 200 \ \mu A, \ V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	V _{(BR)G1SS}	+6	—	—	V	I_{G1} = +10 µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	V _{(BR)G2SS}	+6	_	_	V	I_{G2} = +10 µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I _{G1SS}	—	_	+100	nA	$V_{G1S} = +5 V, V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I _{G2SS}	—	—	+100	nA	$V_{G2S} = +5 V, V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	V _{G1S(off)}	0.5	0.8	1.1	V	$V_{DS} = 5 \text{ V}, V_{G2S} = 4 \text{ V}, I_D = 100 \ \mu\text{A}$
Gate2 to source cutoff voltage	V _{G2S(off)}	0.4	0.7	1.0	V	$V_{DS} = 5 \text{ V}, V_{G1S} = 5 \text{ V}, I_D = 100 \ \mu\text{A}$
Drain current	I _{D(op)}	12	16	20	mA	
Forward transfer admittance	y _{fs}	27	32	38	mS	
Input capacitance	Ciss	1.2	1.6	2.0	pF	$V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V$
Output capacitance	Coss	0.7	1.1	1.5	pF	$R_G = 100 \text{ k}\Omega, \text{ f} = 1 \text{ MHz}$
Power gain	PG	19	24	29	dB	$V_{DS} = 5 V, V_{G1} = 5V, V_{G2S} = 4 V$
Noise figure	NF		1.4	2.1	dB	R _G = 100 kΩ, f = 900 MHz

Bias Circuit for Operating Items ($I_{D(op)}$, $|y_{fs}|$, Ciss, Coss, NF, PG)



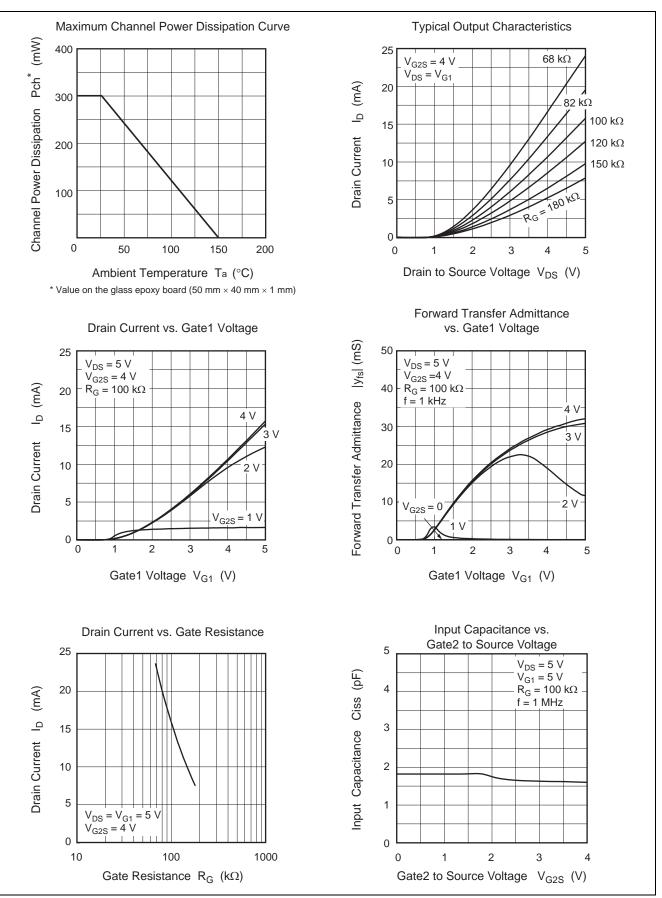




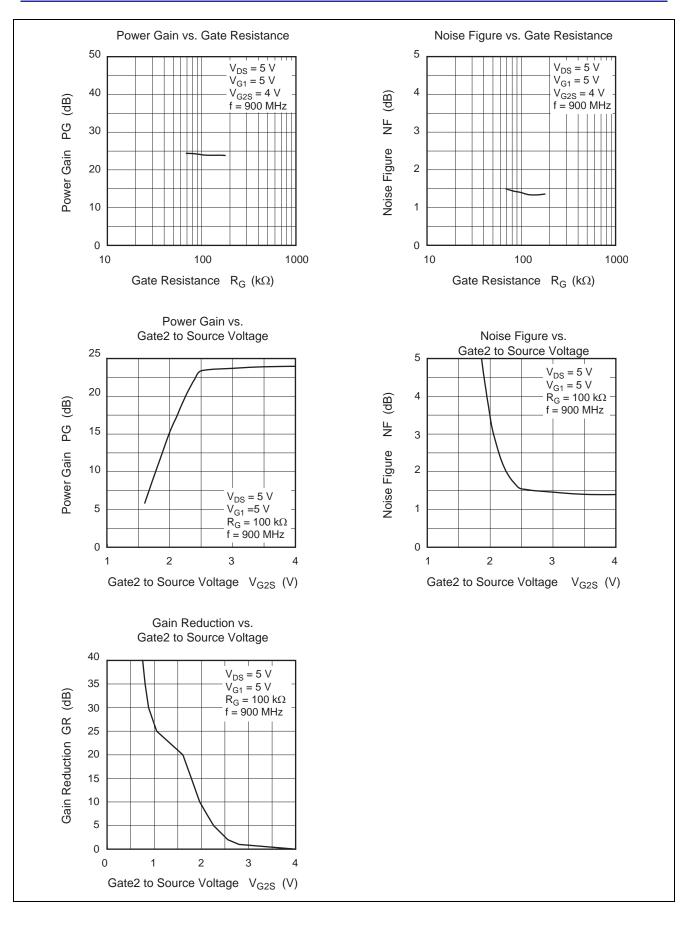




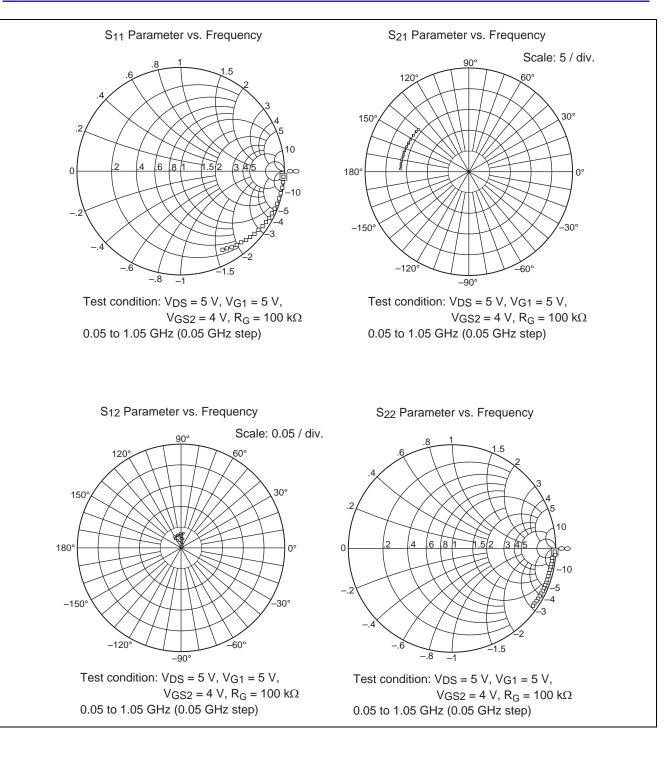
Main Characteristics











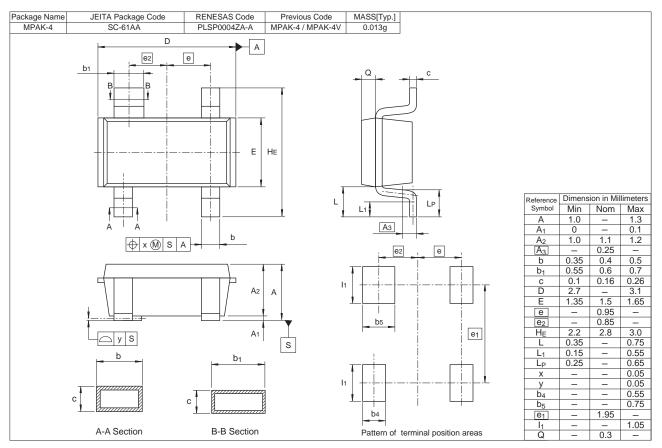


S parameter

Freq	S11		S21		S12		S22	
(MHz)	Mag	Deg	Mag	Deg	Mag	Deg	Mag	Deg
50	0.995	-3.3	3.28	177.9	0.001	17.6	0.991	-1.8
100	0.991	-6.2	3.26	175.5	0.001	75.6	0.996	-3.6
150	0.992	-9.3	3.28	173.7	0.002	73.8	0.995	-5.2
200	0.987	-12.4	3.26	171.3	0.002	79.5	0.997	-7.0
250	0.984	-15.5	3.27	170.0	0.004	116.5	0.995	-8.6
300	0.981	-18.6	3.24	167.3	0.003	89.6	0.993	-10.3
350	0.975	-21.7	3.23	165.8	0.004	76.3	0.992	-11.8
400	0.967	-24.8	3.24	163.3	0.004	87.0	0.989	-13.9
450	0.964	-27.9	3.22	161.9	0.004	91.9	0.991	-15.5
500	0.958	-30.8	3.22	159.4	0.006	89.0	0.987	-17.0
550	0.951	-33.9	3.22	157.9	0.006	100.4	0.988	-18.9
600	0.939	-37.0	3.20	155.4	0.004	84.2	0.985	-20.4
650	0.933	-40.3	3.20	154.1	0.004	85.4	0.984	-22.2
700	0.922	-43.5	3.20	150.7	0.007	80.4	0.983	-23.7
750	0.916	-46.5	3.19	150.7	0.007	93.5	0.981	-25.5
800	0.900	-49.6	3.19	146.7	0.006	108.8	0.979	-27.2
850	0.892	-52.8	3.18	146.4	0.005	122.9	0.978	-28.9
900	0.883	-56.2	3.18	142.8	0.005	120.3	0.975	-30.6
950	0.866	-59.2	3.17	142.3	0.006	104.0	0.970	-32.3
1000	0.858	-62.0	3.16	139.8	0.006	121.3	0.970	-33.8



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
BB506MFS-TL-E	3000	
BB506MFS-TL-H		

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