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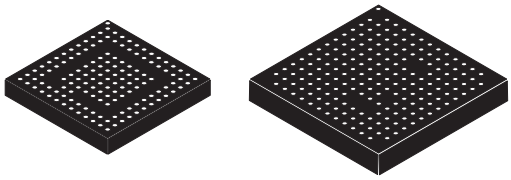
RoHS

Power Management Integrated Circuit (PMIC) for i.MX35/51

13892

POWER MANAGEMENT

The MC13892 is a Power Management Integrated Circuit (PMIC) designed specifically for use with the Freescale i.MX35 and i.MX51 families. It is also compatible with the i.MX27, i.MX31, and i.MX37 application processors targeting netbooks, ebooks, smart mobile devices, smart phones, personal media players, and portable navigation devices.



VK SUFFIX
98ASA10820D
139-PIN 7X7MM BGA

VL SUFFIX
98ASA10849D
186-PIN 12X12MM BGA

ORDERING INFORMATION

See Device Variation Table on Page 2.

Features

- Battery charger system forwall charging and USB charging
- 10-bit ADC for monitoring battery and other inputs, plus a coulomb counter support module
- Four adjustable output buck regulators for direct supply of the processor core and memory
- 12 adjustable output LDOs with internal and external pass devices
- Boost regulator for supplying RGB LEDs
- Serial backlight drivers for displays and keypad, plus RGB LED drivers
- Power control logic with processor interface and event detection
- Real time clock and crystal oscillator circuitry, with coin cell backup and support for external secure real time clock on a companion system processor IC
- Touch screen interface
- SPI/I²C bus interface for control and register access

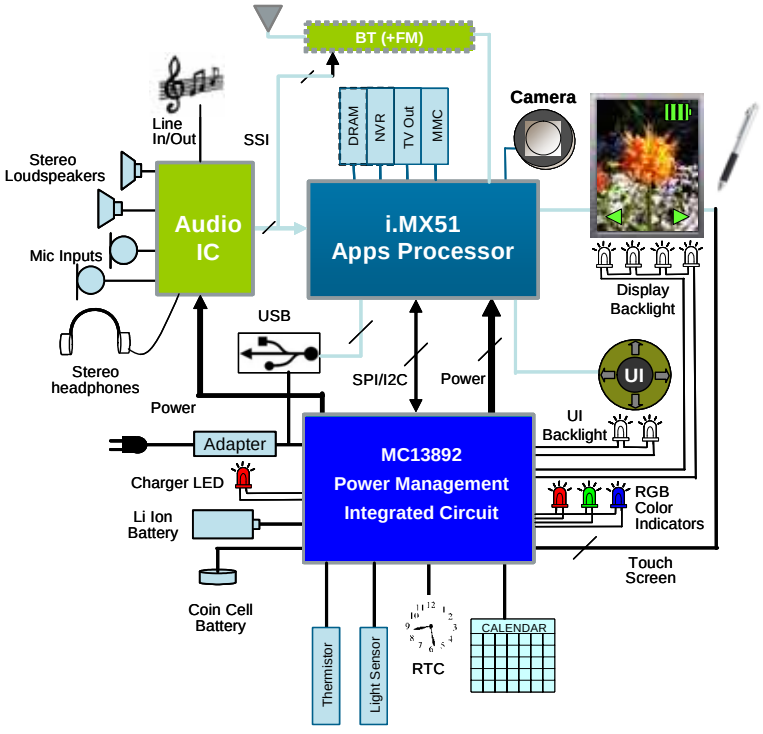


Figure 1. MC13892 Typical Operating Circuit

DEVICE VARIATIONS

Table 1. MC13892 Device Variations

Part Number[1]	Notes	Package	Temperature Range (T_A)	Pin Map	Description
MC13892CJVK MC13892AJVK	(2) (3)	139-PIN 7x7 mm BGA	-40 to +85 ℃	Figure 3	Global Reset Function Default ON
MC13892DJVK MC13892BJVK	(2) (4) (3)	139-PIN 7x7 mm BGA	-40 to +85 ℃	Figure 3	Global Reset Function Default OFF
MC13892VK MC13892JVK	(3) (3)	139-PIN 7x7 mm BGA	-40 to +85 ℃	Figure 3	No Global Reset Function
MC13892CJVL MC13892AJVL	(2) (3)	186-PIN 12x12 mm BGA	-40 to +85 ℃	Figure 4	Global Reset Function Default ON
MC13892DJVL MC13892BJVL	(2) (4) (3)	186-PIN 12x12 mm BGA	-40 to +85 ℃	Figure 4	Global Reset Function Default OFF
MC13892VL MC13892JVL	(3) (3)	186-PIN 12x12 mm BGA	-40 to +85 ℃	Figure 4	No Global Reset Function

Notes

1. For Tape and Reel product, add an “R2” suffix to the part number.
2. Recommended for all new designs
3. Not recommended for new designs
4. Backward compatible replacement part for MC13892VK, MC13892JVK, MC13892VL, MC13892JVL, MC13892BJVK, and MC13892BJVL

INTERNAL BLOCK DIAGRAM

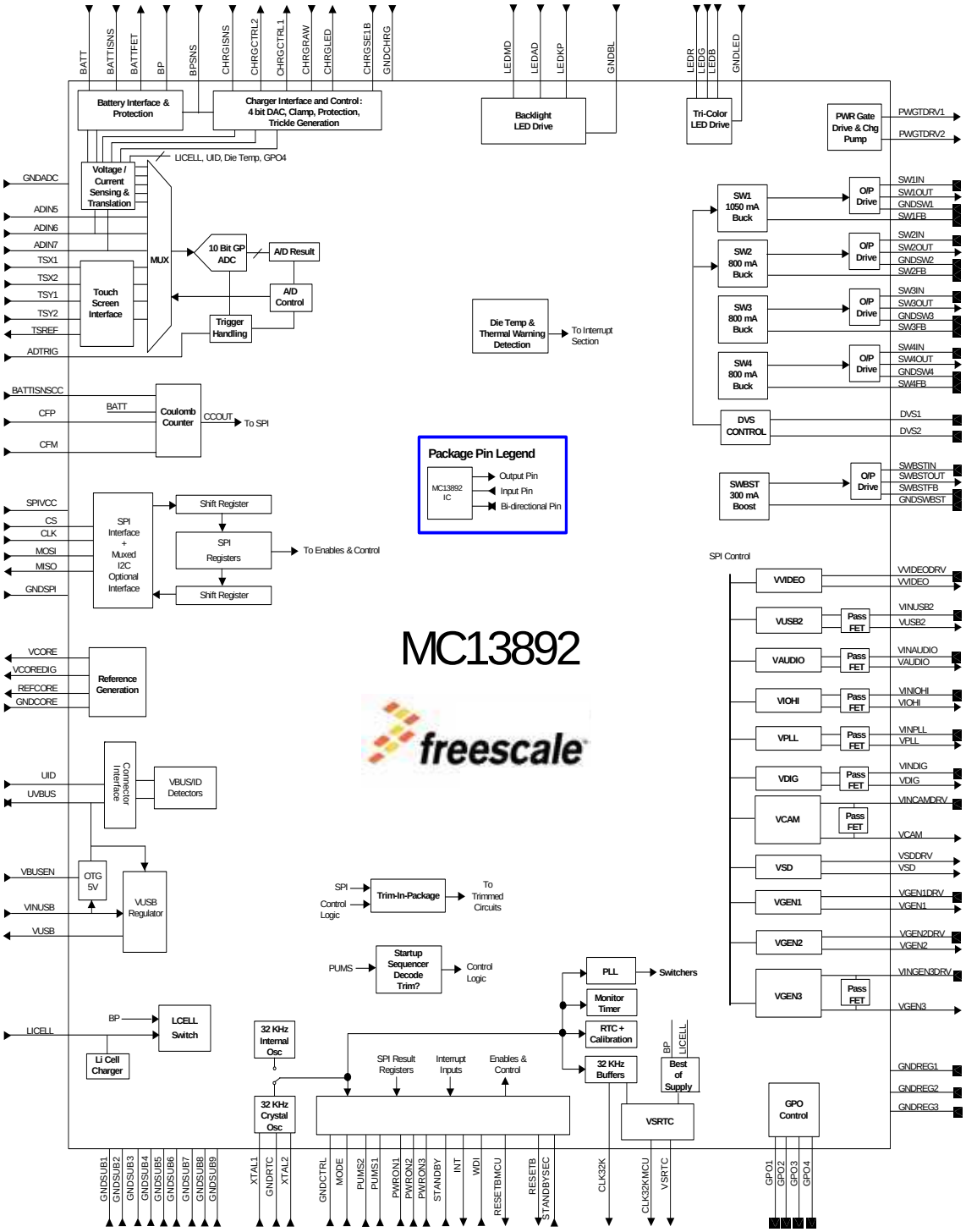


Figure 2. MC13892 Simplified Internal Block Diagram

PIN CONNECTIONS

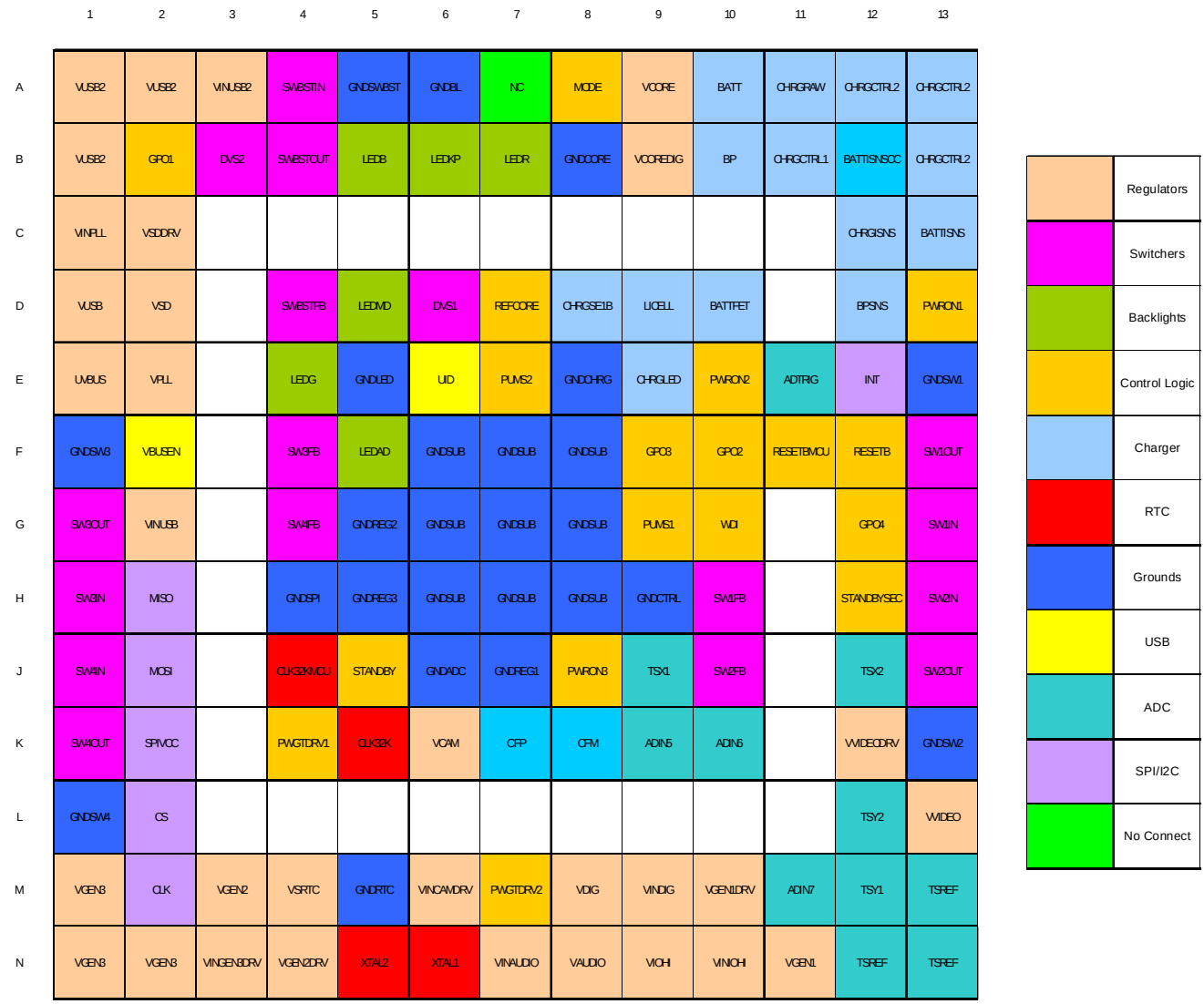


Figure 3. MC13892VK Pin Connections

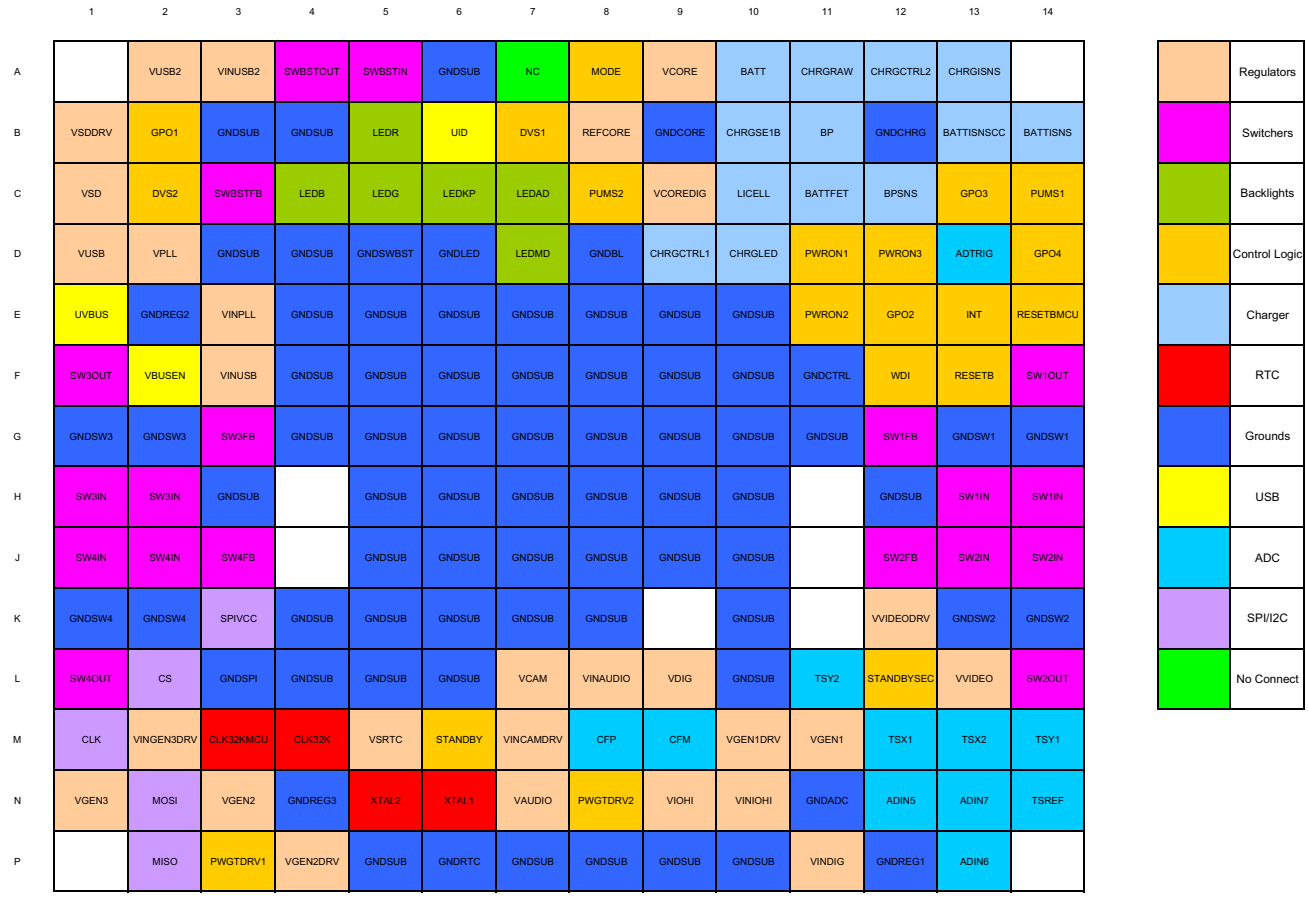


Figure 4. MC13892VL Pin Connections

Table 2. MC13892 Pin Definitions

A functional description of each pin can be found in the Functional Description.

Pin Number on the 13982VK 7x7 mm	Pin Number on the 13982VL 12x12 mm	Pin Name	Rating (V)	Pin Function	Formal Name	Definition
A1, A2, B1	A2	VUSB2	3.6	Output	USB 2 Supply	Output regulator for USB PHY
A3	A3	VINUSB2	5.5	Power	USB 2 Supply Input	Input regulator VUSB2
A4	A5	SWBSTIN	5.5	Power	Switcher Boost Power Input	Switcher BST input
A5	D5	GNDSWBST	–	Ground	Switcher Boost Ground	Ground for switcher BST
A6	D8	GNDBL	–	Ground	Backlight LED Ground	Ground for serial LED drive
A7	A7	NC	–	–	No Connect	Do not connect
A8	A8	MODE	9.0	Input	Mode Configuration	USB LBP mode, normal mode, test mode selection,& anti-fuse bias
A9	A9	VCORE	3.6	Output	Core Supply	Regulated supply output for the IC analog core circuitry
A10	A10	BATT	5.5	Input	Battery Connection	1. Battery positive pin 2. Battery current sensing point 2 3. Battery supply voltage sense
A11	A11	CHRGRAW	20	I/O	Charger Input	1. Charger input 2. Output to battery supplied accesories
A12, A13, B13	A12	CHRGCTRL2	5.5	Output	Charger Control 2	Driver output for charger path FETs M2
B2	B2	GPO1	3.6	Output	General Purpose Output 1	General purpose output 1
B3	C2	DVS2	3.6	Input	Dynamic Voltage Scaling Control 2	Switcher 2 DVS input pin
B4	A4	SWBSTOUT	7.5	Power	Switcher Boost Output	Switcher BST BP supply
B5	C4	LEDB	7.5	Input	LED Driver	General purpose LED current sink driver Blue
B6	C6	LEDKP	28	Input	LED Driver	Keypad lighting LED current sink driver
B7	B5	LEDR	7.5	Input	LED Driver	General purpose LED current sink driver Red
B8	B9	GNDCORE	–	Ground	Core Ground	Ground for the IC core circuitry
B9	C9	VCOREDIG	1.5	Output	Digital Core Supply	Regulated supply output for the IC digital core circuitry
B10	B11	BP	5.5	Power	Battery Plus	1. Application supply point 2. Input supply to the IC core circuitry 3. Application supply voltage sense
B11	D9	CHRGCTRL1	20	Output	Charger Control 1	Driver output for charger path FETs M1
B12	B13	BATTISNSCC	4.8	Input	Battery Current Sense	Accumulated current counter current sensing point
C1	E3	VINPLL	5.5	Power	PLL Supply Input	Input regulator processor PLL
C2	B1	VSDDRV	5.5	Output	VSD Driver	Drive output regulated SD card
C12	A13	CHRGISNS	4.8	Input	Charger Current Sense	Charge current sensing point 1
C13	B14	BATTISNS	4.8	Input	Battery Current Sense	Battery current sensing point 1

Table 2. MC13892 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Description.

Pin Number on the 13982VK 7x7 mm	Pin Number on the 13982VL 12x12 mm	Pin Name	Rating (V)	Pin Function	Formal Name	Definition
D1	D1	VUSB	3.6	Output	USB Supply	USB transceiver regulator output
D2	C1	VSD	3.6	Output	SD Card Supply	Output regulator SD card
D4	C3	SWBSTFB	3.6	Input	Switcher Boost Feedback	Switcher BST feedback
D5	D7	LEDMD	28	Input	LED Driver	Main display backlight LED current sink driver
D6	B7	DVS1	3.6	Input	Dynamic Voltage Scaling Control 1	Switcher 1DVS input pin
D7	B8	REFCORE	3.6	Output	Core Reference	Main bandgap reference
D8	B10	CHRGSE1B	3.6	Input	Charger Select	Charger forced SE1 detection input
D9	C10	LICELL	3.6	I/O	Coin Cell Connection	1. Coin cell supply input 2. Coin cell charger output
D10	C11	BATTFET	4.8	Output	Battery FET Connection	Driver output for battery path FET M3
D12	C12	BPSNS	4.8	Input	Battery Plus Sense	1. BP sense point 2. Charge current sensing point 2
D13	D11	PWRON1	3.6	Input	Power On 1	Power on/off button connection 1
E1	E1	UVBUS	20	I/O	USB Bus	1. USB transceiver cable interface 2. VBUS & OTG supply output
E2	D2	VPLL	3.6	Output	Voltage Supply for PLL	Output regulator processor PLL
E4	C5	LEDG	7.5	Input	PWM Driver for Green LED	General purpose LED current sink driver Green
E5	D6	GNDLED	–	Ground	LED Ground	Ground for LED drivers
E6	B6	UID	5.5	Input	USB ID	USB OTG transceiver cable ID
E7	C8	PUMS2	3.6	Input	Power Up Mode Select 2	Power up mode supply setting 2
E8	B12	GNDCHRG	–	Ground	Charger Ground	Ground for charger interface
E9	D10	CHRGLED	20	Output	Charger LED	Trickle LED driver output 1
E10	E11	PWRON2	3.6	Input	Power On 2	Power on/off button connection 2
E11	D13	ADTRIG	3.6	Input	ADC Trigger	ADC trigger input
E12	E13	INT	3.6	Output	Interrupt Signal	Interrupt to processor
E13	G13, G14	GNDSW1	–	Ground	Switcher 1 Ground	Ground for switcher 1
F1	G1, G2	GNDSW3	–	Ground	Switcher 3 Ground	Ground for switcher 3
F2	F2	VBUSEN	3.6	Input	VBUS Enable	External VBUS enable pin for OTG supply
F4	G3	SW3FB	3.6	Input	Switcher 3 Feedback	Switcher 3 feedback
F5	C7	LEDAD	28	Input	Auxiliary Display LED	Auxiliary display backlight LED sinking current driver
F6	A6, B3, B4, D3, D4, E4, E5, E6	GNDSUB1	–	Ground	Ground 1	Non critical signal ground and thermal heat sink

Table 2. MC13892 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Description.

Pin Number on the 13982VK 7x7 mm	Pin Number on the 13982VL 12x12 mm	Pin Name	Rating (V)	Pin Function	Formal Name	Definition
F7	E7, E8, E9, E10, F4, F5, F6	GNDSUB2	–	Ground	Ground 2	Non critical signal ground and thermal heat sink
F8	F7, F8, F9, F10, G4, G5, G6, G7, G8	GNDSUB3	–	Ground	Ground 3	Non critical signal ground and thermal heat sink
F9	C13	GPO3	–	Output	General Purpose Output 3	General purpose output 3
F10	E12	GPO2	3.6	Output	General Purpose Output 2	General purpose output 2
F11	E14	RESETBMCU	3.6	Output	MCU Reset	Reset output for processor
F12	F13	RESETB	3.6	Output	Peripheral Reset	Reset output for peripherals
F13	F14	SW1OUT	5.5	Output	Switcher 1 Output	Switcher 1 output
G1	F1	SW3OUT	5.5	Output	Switcher 3 Output	Switcher 3 output
G2	F3	VINUSB	7.5	Input	VUSB Supply Input	Input option for UVUSB; tie to SWBST at top level
G4	J3	SW4FB	3.6	Input	Switcher 4 Feedback	Switcher 4 feedback
G5	E2	GNDREG2	–	Ground	Regulator 2 Ground	Ground for regulators 2
G6	G9, G10, G11, H3, H5, H6, H7, H8	GNDSUB4	–	Ground	Ground 4	Non critical signal ground and thermal heat sink
G7	H9, H10, H12, J5, J6, J7	GNDSUB5	–	Ground	Ground 5	Non critical signal ground and thermal heat sink
G8	J8, J9, J10, K4, K5, K6, K7	GNDSUB6	–	Ground	Ground 6	Non critical signal ground and thermal heat sink
G9	C14	PUMS1	3.6	Input	Power Up Mode Select 1	Power up mode supply setting 1
G10	F12	WDI	3.6	Input	Watchdog Input	Watchdog input
G12	D14	GPO4	3.6	Output	General Purpose Output 4	General purpose output 4
G13	H13, H14	SW1IN	5.5	Input	Switcher 1 Input	Input voltage for switcher 1
H1	H1, H2	SW3IN	5.5	Power	Switcher 3 Input	Switcher 3 input
H2	P2	MISO	3.6	I/O	Master In Slave Out	Primary SPI read output
H4	L3	GNDSPI	–	Ground	SPI Ground	Ground for SPI interface
H5	N4	GNDREG3	–	Ground	Regulator 3 Ground	Ground for regulators 3
H6	K8, K10, L4, L5, L6, L10	GNDSUB7	–	Ground	Ground 7	Non critical signal ground and thermal heat sink
H7	P5, P7, P8, P9, P10	GNDSUB8	–	Ground	Ground 8	Non critical signal ground and thermal heat sink
H8	–	GNDSUB9	–	Ground	Ground 9	Non critical signal ground and thermal heat sink
H9	F11	GNDCTRL	–	Ground	Logic Control Ground	Ground for control logic

Table 2. MC13892 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Description.

Pin Number on the 13982VK 7x7 mm	Pin Number on the 13982VL 12x12 mm	Pin Name	Rating (V)	Pin Function	Formal Name	Definition
H10	G12	SW1FB	3.6	Input	Switcher 1 Feedback	Switcher 1 feedback
H12	L12	STANDBYSEC	3.6	Input	Secondary Standby Signal	Standby input signal from peripherals
H13	J13, J14	SW2IN	5.5	Input	Switcher 2 Input	Input voltage for Switcher 2
J1	J1, J2	SW4IN	5.5	Power	Switcher 4 Input	Switcher 4 input
J2	N2	MOSI	3.6	Input	Master Out Slave In	Primary SPI write input
J4	M3	CLK32KMCU	3.6	Output	32 kHz Clock for MCU	32 kHz clock output for processor
J5	M6	STANDBY	3.6	Input	Standby Signal	Standby input signal from processor
J6	N11	GNDADC	–	Ground	ADC Ground	Ground for A to D circuitry
J7	P12	GNDREG1	–	Ground	Regulator 1 Ground	Ground for regulators 1
J8	D12	PWRON3	3.6	Input	Power On 3	Power on/off button connection 3
J9	M12	TSX1	3.6	Input	Touch Screen Interface X1	Touch screen interface X1
J10	J12	SW2FB	3.6	Input	Switcher 2 Feedback	Switcher 2 feedback
J12	M13	TSX2	3.6	Input	Touch Screen Interface X2	Touch screen interface X2
J13	L14	SW2OUT	5.5	Output	Switcher 2 Output	Switcher 2 output
K1	L1	SW4OUT	5.5	Output	Switcher 4 Output	Switcher 4 output
K2	K3	SPIVCC	3.6	Input	Supply Voltage for SPI	Supply for SPI bus and audio bus
K4	P3	PWGTDRV1	4.8	Output	Power Gate Driver 1	Power gate driver 1
K5	M4	CLK32K	3.6	Output	32 kHz Clock	32 kHz clock output for peripherals
K6	L7	VCAM	3.6	Output	Camera Supply	Output regulator camera
K7	M8	CFP	4.8	Passive	Current Filter Positive	Accumulated current filter cap plus pin
K8	M9	CFM	4.8	Passive	Current Filter Negative	Accumulated current filter cap minus pin
K9	N12	ADIN5	4.8	Input	ADC Channel 5 Input	ADC generic input channel 5
K10	P13	ADIN6	4.8	Input	ADC Channel 6 Input	ADC generic input channel 6
K12	K12	VVIDEODRV	5.5	Output	VVIDEO Driver	Drive output regulator VVIDEO
K13	K13, K14	GNDSW2	–	Ground	Switcher 2 Ground	Ground for switcher 2
L1	K1, K2	GNDSW4	–	Ground	Switcher 4 Ground	Ground for switcher 4
L2	L2	CS	3.6	Input	Chip Select	Primary SPI select input
L12	L11	TSY2	3.6	Input	Touch Screen Interface Y2	Touch screen interface Y2
L13	L13	VVIDEO	3.6	Output	Video Supply	Output regulator TV DAC
M1, N1, N2	N1	VGEN3	3.6	Output	General Purpose Regulator 3	Output GEN3 regulator
M2	M1	CLK	3.6	Input	Clock	Primary SPI clock input
M3	N3	VGEN2	3.6	Output	General Purpose Regulator 2	Output GEN2 regulator

Table 2. MC13892 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Description.

Pin Number on the 13982VK 7x7 mm	Pin Number on the 13982VL 12x12 mm	Pin Name	Rating (V)	Pin Function	Formal Name	Definition
M4	M5	VSRTC	3.6	Output	SRTC Supply	Output regulator for SRTC module on processor
M5	P6	GNDRTC	–	Ground	Real Time Clock Ground	Ground for the RTC block
M6	M7	VINCAMDRV	5.5	I/O	Camera Regulator Supply Input and Driver Output	1. Input regulator camera using internal PMOS FET. 2. Drive output regulator for camera voltage using external PNP device.
M7	N8	PWGTDRV2	4.8	Output	Power Gate Driver 2	Power gate driver 2
M8	L9	VDIG	3.6	Output	Digital Supply	Output regulator digital
M9	P11	VINDIG	5.5	Input	VDIG Supply Input	Input regulator digital
M10	M10	VGEN1DRV	5.5	Output	VGEN1 Driver	Drive output GEN1 regulator
M11	N13	ADIN7	4.8	Input	ADC Channel 7 Input	ADC generic input channel 7, group 1
M12	M14	TSY1	3.6	Input	Touch Screen Interface Y1	Touch screen interface Y1
M13, N12, N13	N14	TSREF	3.6	Output	Touch Screen Reference	Touch screen reference
N3	M2	VINGEN3DRV	5.5	Power/Output	VGEN3 Supply Input and Driver Output	1. Input VGEN3 regulator 2. Drive VGEN3 output regulator
N4	P4	VGEN2DRV	5.5	Output	VGEN2 Driver	Drive output GEN2 regulator
N5	N5	XTAL2	2.5	Input	Crystal Connection 2	32.768 kHz oscillator crystal connection 2
N6	N6	XTAL1	2.5	Input	Crystal Connection 1	32.768 kHz oscillator crystal connection 1
N7	L8	VINAUDIO	5.5	Power	Audio Supply Input	Input regulator VAUDIO
N8	N7	VAUDIO	3.6	Output	Audio Supply	Output regulator for audio
N9	N9	VIOHI	3.6	Output	High Voltage IO Supply	Output regulator high voltage IO, efuse
N10	N10	VINIOHI	5.5	Input	High Voltage IO Supply Input	Input regulator high voltage IO
N11	M11	VGEN1	3.6	Output	General Purpose Regulator 1	Input GEN1 regulator

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Charger and USB Input Voltage[5]	V_{CHRGR}	-0.3 to 20	V
MODE pin Voltage	V_{MODE}	-0.3 to 9.0	V
Main/Aux/Keypad Current Sink Voltage	V_{LEDMD}, V_{LEDAD}, V_{LEDKP}	-0.3 to 28	V
Battery Voltage	V_{BATT}	-0.3 to 4.8	V
Coin Cell Voltage	V_{LICELL}	-0.3 to 3.6	V
ESD Voltage[6] Human Body Model - HBM with Mode pin excluded[9] Charge Device Model - CDM	V_{ESD}	 ±1500 ±250	V
THERMAL RATINGS			
Ambient Operating Temperature Range	T_A	-40 to +85	℃
Operating Junction Temperature Range	T_J	-40 to +125	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃
THERMAL RESISTANCE			
Peak Package Reflow Temperature During Reflow[7], [8]	T_{PPRT}	Note 8	℃

Notes

5. USB Input Voltage applies to UVBUS pin only
6. ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω) and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF).
7. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
8. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
9. Mode Pin is not ESD protected.

Table 4. Dissipation Ratings

Rating Parameter	Condition	Symbol	VK Package	VL Package	Unit
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	104	65	℃/W
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JMA}$	54	42	℃/W
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	88	55	℃/W
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	49	38	℃/W
Junction to Board		$R_{\theta JB}$	32	28	℃/W
Junction to Case		$R_{\theta JC}$	29	22	℃/W
Junction to Package Top	Natural Convection	θJT	7.0	5.0	℃/W

STATIC ELECTRICAL CHARACTERISTICS

Table 5. Static Electrical Characteristics

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT CONSUMPTION					
RTC Mode All blocks disabled, no main battery attached, coin cell is attached to LICELL (10) RTC	I_{RTC}	 –	 3.00	 6.00	µA
OFF Mode (All blocks disabled, main battery attached) (10) MC13892 core and RTC module	I_{OFF}	 –	 10	 30	µA
Power Cut Mode (All blocks disabled, no main battery attached, coin cell is attached and valid) (10) MC13892 core and RTC module	I_{PCUT}	 –	 3.0	 6.0	µA
ON Standby mode - Low-power mode 4 buck regulators in low-power mode, 3 regulators (11)	I_{STBY}	–	230	295	µA
ON Mode - Typical use case 4 buck regulators in PWMPS mode, 5 Regulators (12)	I_{ON}	–	459	1500	µA
I/O CHARACTERISTICS (13)					
PWRON1, PWRON2, PWRON3, Pull-up (14) Input Low, 47 kOhm Input High, 1.0 MOhm		 0.0 1.0	 – –	 0.3 VCOREDIG	V
CHRGSE1B, Pull-up (15) Input Low Input High		 0.0 1.0	 – –	 0.3 VCORE	V
STANDBY, STANDBYSEC, WDI, ADTRIG, Weak Pull-down (16),(17) Input Low Input High		 0.0 1.0	 – –	 0.3 3.6	V
CLK32K, CMOS Output Low, -100 µA Output High, 100 µA		 0.0 SPIVCC -0.2	 – –	 0.2 SPIVCC	V
CLK32KMCU, CMOS Output Low, -100 µA Output High, 100 µA		 0.0 VSRTC- 0.2	 – –	 0.2 VSRTC	V
RESETB, RESETBMCU, Open Drain (18) Output Low, -2.0 mA Output High, Open Drain		 0.0 0.0	 – –	 0.4 3.6	V

Notes
10. Valid at 25 °C only.
11. VPLL, VIOHI, VGEN2
12. VPLL, VIOHI, VGEN2, VAUDIO, VVIDEO
13. SPIVCC is typically connected to the output of buck regulator: SW4 and set to 1.800 V
14. Input has internal pull-up to VCOREDIG equivalent to 200 kOhm
15. Input has internal pull-up to VCORE equivalent to 100 kOhm
16. SPIVCC needs to remain enabled for proper detection of WDI High to avoid involuntary shutdown
17. A weak pull-down represents a nominal internal pull down of 100 nA, unless otherwise noted
18. RESETB & RESETBMCU have open drain outputs, external pull-ups are required

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
I/O CHARACTERISTICS (CONTINUED) (19)					
VSRTC, Voltage Output		1.1	–	1.3	V
DVS1, DVS2, Weak Pull-down (20) Input Low Input High		 0.0 0.7* SPIVCC	 – –	 0.3* SPIVCC 3.1	V
GPO1, CMOS Output Low, -400 µA Output High, 400 µA To VCORE		 0.0 VCORE- 0.2 200	 – – –	 0.2 VCORE 500	V Ohm
GPO2, GPO3, GPO4, CMOS Output Low, -100 µA Output High, 100 µA		 0.0 VIOHI - 0.2	 – –	 0.2 VIOHI	V
GPO4, Analog Input		0.0	–	VCORE+0.3	V
CS, CLK, MOSI, VBUSEN, Weak Pull-down on CS and VBUSEN (20) Input Low Input High		 0.0 0.7* SPIVCC	 – –	 0.3* SPIVCC SPIVCC+0.3	V
CS, MOSI (at Booting for SPI / I^2C decoding), Weak Pull-down on CS (21) Input Low Input High		 0.0 0.7 * VCORE	 – –	 0.3 * VCORE VCORE	V
MISO, INT, CMOS (22) Output Low, -100 µA Output High, 100 µA		 0.0 SPIVCC -0.2	 – –	 0.2 SPIVCC	V
PUMS1, PUMS2 (22) PUMSxS = 00 PUMSxS = 01, Load < 10 pF PUMSxS = 10 PUMSxS = 11		 0.0 Open 1.3 2.5	 – – – –	 0.3 Open 2.0 3.1	V
MODE (23) Input Low Input Med Input High		 0.0 1.1 VCORE	 – – –	 0.4 1.7 9.0	V

Notes

19. SPIVCC is typically connected to the output of buck regulator: SW4 and set to 1.800 V
20. A weak pull-down represents a nominal internal pull down of 100 nA unless otherwise noted
21. The weak pull-down on CS is disabled if a VIH is detected at startup to avoid extra consumption in I^2C mode
22. The output drive strength is programmable
23. Input state is latched in first phase of cold start, refer to Power Control System for description of PUMS configuration
24. Input state is not latched

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
32 KHZ CRYSTAL OSCILLATOR					
Operating Voltage Oscillator and RTC Block from BP	V_{XTAL}	1.2	–	4.65	V
Coincell Disconnect Threshold At LICELL	V_{LCD}	1.8	–	2.0	V
Output Low CLK32K, CLK32KMCU Output sink 100 µA	V_{CLKLO}	0.0	–	0.2	V
Output High CLK32K Output source 100 µA CLK32KMCU Output source 100 µA	V_{CLKHI} $V_{CLKMCUHI}$	$SPIV_{CC}$-0.2 V_{SRTC}-0.2	– –	$SPIV_{CC}$ V_{SRTC}	V
VSRTC GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} Valid Coin Cell range Or valid BP	V_{LICELL} BP	1.8 UVDET	– –	3.6 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{SRTC}	0.0	–	50	µA
Bypass Capacitor Value	C_{SRTC}	–	1.0	–	µF
VSRTC ACTIVE MODE – DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{SRTC}	1.15	1.20	1.25	V
CLK AND MISO					
Input Low CS, MOSI, CLK	V_{INCSLO} $V_{INMOSILO}$ $V_{INCLKLO}$	0.0	–	0.3*$SPIV_{CC}$	V
Input High CS, MOSI, CLK	V_{INCSHI} $V_{INMOSIHI}$ $V_{INCLKHI}$	0.7*$SPIV_{CC}$	–	$SPIV_{CC}$+0.3	V
Output Low MISO, INT Output sink 100 µA	$V_{OMISOLO}$ V_{OINTLO}	0.0	–	0.2	V
Output High MISO, INT Output source 100 µA	$V_{OMISOHI}$ V_{OINTHI}	$SPIV_{CC}$-0.2	–	$SPIV_{CC}$	V
SPIVCC Operating Range	$SPIV_{CC}$	1.75	–	3.1	V

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK REGULATORS					
Operating Input Voltage	V_{SWIN}				V
PWM operation, 0 < IL < I_{MAX}		3.0	–	4.65	
PFM operation, 0 < IL < I_{MAX}		2.8	–	4.65	
Extended PWM or PFM operation[25]		UVDET	–	4.65	
Output Voltage Range	V_{SW1}				V
Switcher 1		0.6	–	1.375	
Switchers 2, 3, and 4		0.6	–	1.850	
Output Accuracy					mV
PWM mode including ripple, load regulation, and transients [26]	V_{SWLOPP}	Nom-50	Nom	Nom+50	
PFM Mode, including ripple, load regulation, and transients	$V_{SWLIPPI}$	Nom-50	Nom	Nom+50	
Maximum Continuous Load Current, I_{MAX}, V_{INMIN}<BP<4.65 V					mA
SW1 in PWM mode (SWILIMB = 0, no max current limit)	I_{SW1}	800	–	–	
SW1 in PWM Mode (SWILIMB = 1, no max current limit)[27]		1050	–	–	
SW2, SW3, SW4 in PWM mode (SWILIMB = 0, no max current limit)	$I_{SW2,3,4}$	800	–	–	
SW2, SW3, SW4 in PWM mode (SWILIMB = 1, no max current limit)[27]	$I_{SW2,3,4}$	800	–	–	
SW1, SW2, SW3, SW4 in PFM mode	$I_{SW1, 2, 3, 4}$	–	50	–	
Maximum Peak Load Current, I_{PEAK}, BP ≤ 4.2 V,					mA
SW1 in PWM Mode (SWILIMB = 1, no max current limit)[27]	I_{SW1}	1250	–	–	
SW4 in PWM Mode (SWILIMB = 1, no max current limit)[27]	I_{SW4}	1000	–	–	

Notes

25. In the extended operating range the performance may be degraded
26. Transient loading for load steps of ILmax/2
27. In this mode, current limit protection is disabled for SW1 - SW4 by setting SWILIMB = 1. Therefore, the load on SW1-4 should not exceed the conditions specified in the table above. Application needs to provide current limit protection circuitry either in battery or as pre-regulated supply to BP.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK REGULATORS (CONTINUED)					
Automatic Mode Change Threshold, Switchover between PFM and PWM modes	AMC_{TH}	–	50	–	mA
Efficiency					η
PFM, 0.9 V, 1.0 mA		–	75	–	
PFM, 01.8 V, 1.0 mA		–	85	–	
PWM Pulse Skipping, 1.25 V, 50 mA		–	78	–	
PWM Pulse Skipping, 1.8 V, 50 mA		–	82	–	
PWM, 1.25 V, 500 mA		–	78	–	
PWM, 1.8 V, 500 mA		–	82	–	
External Components, Used as a condition for all other parameters					
Inductor for SW2, SW3, SW4[28]	L_{SW234}	-20%	2.2	+20%	µH
Inductor for SW1[28]	L_{SW1}	-30%	1.5	+30%	µH
Inductor Resistance	R_{WSW}	–	–	0.16	Ω
Bypass Capacitor for SW2, SW3, SW4[29]	C_{OSW234}	-35%	10	+35%	µF
Bypass Capacitor for SW1[30]	C_{OSW1}	-35%	2x22	+35%	µF
Bypass Capacitor ESR	ESR_{SW}	5.0	–	50	mΩ
Input Capacitor[31]		1.0	4.7	–	µF
SWBST					
Average Output Voltage[32] 3.0 V < V_{IN} < 4.65 (1), 0 < IL < IL_{MAX}[33]	V_{BST}	Nom-5%	5.0	Nom+5%	V
Output Ripple 3.0 V < V_{IN} < 4.65, 0 < IL < IL_{MAX}, Excluding reverse recovery of Schottky diode	V_{BSTPP}	–	–	120	mVpp
Average Load Regulation V_{IN} = 3.6 V, 0 < IL < IL_{MAX}	V_{BSTLOR}	–	–	0.5	mV/mA
Average Line Regulation 3.0 V < V_{IN} < 4.65 V, IL = IL_{MAX}	V_{BSTLIR}	–	–	50	mV

Notes

28. Preferred device TDK VLS252012 series at 2.5x2.0 mm footprint and 1.2 mm max height
29. Preferably 0603 style 6.3 V rated X5R/X7R type at 35% total make tolerance, temperature spread and DC bias derating such as TDK C1608X5R0J106M
30. Preferably 0805 style 6.3 V rated X5R/X7R type at 35% total make tolerance, temperature spread and DC bias derating such as TDK C2012X5R0J226M
31. Preferably 0603 style 6.3 V rated X5R/X7R type at 35% total make tolerance, temperature spread and DC bias derating such as TDK C1608X5R0J475
32. Output voltage when configured to supply VBUS in OTG mode can be as high as 5.75 V
33. Vin is the low side of the inductor that is connected to BP.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SWBST (CONTINUED)					
Maximum Continuous Load Current IL_{MAX} 3.0 V < V_{IN} < 4.65, V_{OUT} = 5.0 V	I_{BST}	300	–	–	mA
Start-up Overshoot IL = 0 mA	V_{BSTOS}	–	–	500	mV
Efficiency, IL = IL_{MAX}	$SWBST_{EFF}$	–	80	–	%
External Components - Used as a condition for all other parameters					
Inductor[34]	L_{BST}	-20%	2.2	+20%	µH
Inductor Resistance	R_W_{BST}	–	–	0.2	Ω
Inductor saturation current at 30% loss in inductance value	IL_{SAT}	1.0	–	–	A
Bypass Capacitor[35]	CO_{BST}	-60%	10	+35%	µF
Bypass Capacitor ESR at resonance	ESR_{BST}	1.0	–	10	mΩ
Input Capacitor	C_{BSTD}	1.0	4.7	–	µF
Diode current capability	I_{BSTDPK}	850	–	–	mAdc
Diode current capability	I_{BSTDPK}	1500	–	–	mApk
NMOS Off Leakage, SWBSTIN = 4.5 V, SWBSTEN = 0	I_{BSTIK}	–	1.0	5.0	µA
VVIDEO					
Operating Input Voltage Range V_{INMIN} to V_{INMAX}	$V_{INVIDEO}$	V_{NOM}+0.25	–	4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX} (Not exceeding PNP max power)	I_{VIDEO}	0.0	–	350	mA
Minimum Bypass Capacitor Value Used as a condition for all other parameters	CO_{VIDEO}	1.1	2.2	–	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{VIDEO}	20	–	100	mΩ
VVIDEO ACTIVE MODE DC					
Output Voltage V_{OUT} V_{INMIN} < V_{IN} < V_{INMAX}, IL_{MIN} < IL < IL_{MAX}	ΔV_{VIDEO}	V_{NOM} - 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, For any V_{INMIN} < V_{IN} < V_{INMAX}	$V_{VIDEOLOPP}$	–	–	0.20	mV/mA
Line Regulation V_{INMIN} < V_{IN} < V_{INMAX}, For any IL_{MIN} < IL < IL_{MAX}	$V_{VIDEOLIPP}$	–	5.0	8.0	mV
Short-circuit Protection Threshold V_{INMIN} < V_{IN} < V_{INMAX}, Short-circuit V_{OUT} to GND	$I_{VIDEOSHT}$	IL_{MAX}+20%	–	–	mA

Notes

34. Preferred device TDK VLS252012 series at 2.5x2.0 mm footprint and 1.2 mm max height
35. Applications of SWBST should take into account impact of tolerance and voltage derating on the bypass capacitor at the output level.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 ℃ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VVIDEO LOW-POWER MODE DC - VVIDEOMODE = 1					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MINLP} < IL < IL_{MAXLP}$	$\Delta V_{VIDEOLO}$	V_{NOM} -3%	V_{NOM}	V_{NOM} +3%	V
Current Load Range ILminlp to IL_{MAXLP}	$I_{VIDEOLO}$	0.0	–	3.0	mA
VAUDIO					
Operating Input Voltage Range V_{INMIN} to V_{INMAX}	V_{AUDIO}	V_{NOM}+0.25	–	4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{AUDIO}	0.0	–	150	mA
Minimum Bypass Capacitor Value	C_{OAUDIO}	0.65	2.2	–	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{AUDIO}	0.0	–	0.1	Ω
VAUDIO ACTIVE MODE DC					
Output Voltage V_{OUT} ($V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$)	V_{AUDIO}	V_{NOM} - 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation (1.0 mA < IL < IL_{MAX}, For any $V_{INMIN} < V_{IN} < V_{INMAX}$)	$V_{AUDIOLOR}$	–	–	0.25	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, For any $IL_{MIN} < IL < IL_{MAX}$	$V_{AUDIOLIR}$	–	5.0	8.0	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to GND	$I_{AUDIOSHT}$	IL_{MAX}+20%	–	–	mA
VPLL AND VDIG					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} VDIG, VPLL all settings, BP biased VPLL, VDIG [1:0] = 00,01 VPLL, VDIG [1:0] = 10, 11, External Switcher	V_{INPLL}, V_{INDIG}	 UVDET 1.75 2.15	 – SW4 = 1.8 2.2	 4.65 4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{PLL}, I_{DIG}	0.0	–	50	mA
Minimum Bypass Capacitor Value Used as a condition for all other parameters	C_{OPLL}, C_{ODIG}	0.65	2.2	–	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{PLL}, ESR_{DIG}	0.0	–	0.1	Ω
VPLL AND VDIG ACTIVE MODE DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{PLL}, V_{DIG}	V_{NOM} - 0.05	V_{NOM}	V_{NOM} + 0.05	V
Load Regulation 1.0 mA < IL < IL_{MAX} for any $V_{INMIN} < V_{IN} < V_{INMAX}$	V_{PLLLOR}, V_{DIGLOR}	–	–	0.35	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$ for any $IL_{MIN} < IL < IL_{MAX}$	V_{PLLLIR}, V_{DIGLIR}	–	5.0	8.0	mV
VIOHI					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} V_{NOM} = 2.775 V	V_{INIOHI}	V_{NOM}+0.25	–	4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{IOHI}	0.0	–	100	mA
Minimum Bypass Capacitor Value	C_{OIOHI}	0.65	2.2	–	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{IOHI}	0.0	–	100	mΩ

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VIOHI ACTIVE MODE DC					
Output Voltage V_{OUT} - (V_{NOM} = 2.775) $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{IOH}	V_{NOM} -3%	V_{NOM}	V_{NOM} +3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, for any $V_{INMIN} < V_{IN} < V_{INMAX}$	V_{IOHLOR}	–	–	0.35	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	V_{IOHLIR}	–	5.0	8.0	mV
VCAM					
Operating Input Voltage Range V_{INMIN} to V_{INMAX}	V_{INCAM}	V_{NOM} +0.25	–	4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX} Internal pass FET External PNP	I_{CAM}	 0.0 0.0	 – –	 65 250	mA
Minimum Bypass Capacitor Value Internal pass device External PNP (not exceeding PNP max power)	C_{OCAM}	 0.65 1.1	 2.2 2.2	 – –	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{CAM}	 20	 –	 100	mΩ
VCAM ACTIVE MODE DC					
Output Voltage V_{OUT} (V_{NOM} = 2.775) $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{CAM}	V_{NOM} - 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, for any $V_{INMIN} < V_{IN} < V_{INMAX}$	V_{CAMLOR}	–	–	0.25	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	V_{CAMLIR}	–	5.0	8.0	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to GND	I_{CAMSHT}	IL_{MAX}+20%	–	–	mA
VCAM LOW-POWER MODE DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MINLP} < IL < IL_{MAXLP}$	V_{CAMLO}	V_{NOM} -3%	V_{NOM}	V_{NOM} +3%	V
Current Load Range IL_{MINLP} to IL_{MAXLP}	I_{CAMLO}	0.0	–	3.0	mA
VSD					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} VSD[2:0] = 010 to 111 VSD[2:0] = 010 to 111, Extended Operation VSD[2:0] = 000, 001 [000] BP Supplied VSD[2:0] = 000 External Switcher Supplied	V_{INSD}	 V_{NOM}+0.25 UVDET UVDET 2.15	 – – – 2.20	 4.65 4.65 4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX} Not exceeding PNP max power	I_{SD}	 0.0	 –	 250	mA
Minimum Bypass Capacitor Value	C_{OSD}	1.1	2.2	–	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{SD}	 20	 –	 100	mΩ

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VSD ACTIVE MODE DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{SD}	V_{NOM} - 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < $IL < IL_{MAX}$, for any $V_{INMIN} < V_{IN} < V_{INMAX}$	V_{SDLOR}	–	–	0.25	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	V_{SDLIR}	–	5.0	8.0	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to GND	I_{SDSHT}	IL_{MAX}+20%	–	–	mA
VSD LOW-POWER MODE DC - VSDMODE = 1					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MINLP} < IL < IL_{MAXLP}$	V_{SDLO}	V_{NOM} -3%	V_{NOM}	V_{NOM} +3%	V
Current Load Range IL_{MINLP} to IL_{MAXLP}	I_{SDLO}	0.0	–	3.0	mA
VUSB GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} Supplied by VBUS Supplied by SWBST	V_{INUSB}	 4.4 –	 5.0 –	 5.25 5.75	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{USB}	0.0	–	100	mA
Bypass Capacitor Value Range	C_{OUSB}	0.65	2.2	–	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{USB}	0.0	–	0.1	Ω
VUSB ACTIVE MODE DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{USB}	V_{NOM} - 4%	3.3	V_{NOM} + 4%	V
Load Regulation 0 < $IL < IL_{MAX}$ from DM/DP for any $V_{INMIN} < V_{IN} < V_{INMAX}$	V_{USBLOR}	–	–	1.0	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	V_{USBLIR}	–	–	20	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to GND	V_{USBSHT}	IL_{MAX}+20%	–	–	mA
VUSB2					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} Extended operation	V_{INUSB2}	V_{NOM} +0.25 UVDET	– –	4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{USB2}	0.0	–	50	mA
Minimum Bypass Capacitor Value Used as a condition for all other parameters	C_{OUSB2}	0.65	2.2	–	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{USB2}	0.0	–	0.1	Ω

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 ℃ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VUSB2 ACTIVE MODE DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{USB2}	V_{NOM} -3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, for any $V_{INMIN} < V_{IN} < V_{INMAX}$	$V_{USB2LOR}$	–	–	0.35	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	$V_{USB2LIR}$	–	5.0	8.0	mV
UVBUS					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} VINUSB supplied by SWBST	$V_{INUVBUS}$	4.75	5.0	5.25	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{UVBUS}	0.0	–	100	mA
Minimum Bypass Capacitor Value	C_{OUVBUS}	(36)	(36)	6.5 (37)	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	$V_{INUVBUS}$	(36)	(36)	(37)	Ω
UVBUS ACTIVE MODE DC					
Output Voltage Vout $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{UVBUS}	4.4	5.0	5.25	V
VGEN1					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} All settings, BP biased VGEN1=00,01, External switcher supplied	V_{INGEN1}	UVDET < V_{NOM} +0.25 2.15	– 2.2	4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX} (not exceeding PNP max power)	I_{GEN1}	0.0	–	200	mA
Extended input voltage range (BP biased, performance may be out of specification for output levels VGEN1[1:0] = 10 to 11)		UVDET	–	4.65	V
Minimum Bypass Capacitor Value	C_{OGEN1}	1.1	2.2	+35%	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{GEN1}	20	–	100	mΩ
VGEN1 ACTIVE MODE DC					
Output Voltage V_{OUT} VGEN1 = 00, 01, $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$ VGEN1 = 10, 11, $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$	V_{GEN1}	V_{NOM} – 0.05 V_{NOM} – 3%	V_{NOM} V_{NOM}	V_{NOM} + 0.05 V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, for any $V_{INMIN} < V_{IN} < V_{INMAX}$	$V_{GEN1LOR}$	–	–	0.25	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	$V_{GEN1LIR}$	–	5.0	8.0	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to GND	$V_{GEN1SHT}$	IL_{MAX}+20%	–	–	mA

Notes

36. Filtering is shared with CHRGRAW (shorted at board level). 2.2 µF is typically included at the CHRGRAW pin.
37. 6.5 µF is the maximum allowable capacitance on VBUS including all tolerances of filtering capacitance on VBUS and CHRGRAW (which are shorted at the board level).

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VGEN1 LOW-POWER MODE DC - VGEN1MODE = 1					
Output Voltage V_{OUT} - V_{INMIN} < V_{IN} < V_{INMAX}, IL_{MINLP} < IL < IL_{MAXLP} VGEN1 = 00, 01 VGEN1 = 10, 11	V_{GEN1LO}	 V_{NOM} - 0.05 V_{NOM} -3%	 V_{NOM} V_{NOM}	 V_{NOM} + 0.05 V_{NOM} +3%	V
Current Load Range IL_{MINLP} to IL_{MAXLP}	I_{GEN1LO}	0.0	–	3.0	mA
VGEN2 GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} All settings, BP biased VGEN2=000,001, External switcher supplied	V_{INGEN2}	UVDET< V_{NOM}+0.25 2.15	– 2.2	4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX} (Not exceeding PNP max power)	I_{GEN2}	0.0	–	350	mA
Minimum Bypass Capacitor Value	C_{OGEN2}	1.1	2.2	+35%	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{GEN2}	 20	 –	 100	mΩ
VGEN2 ACTIVE MODE DC					
Output Voltage V_{OUT} VGEN2 = 000, 001, 010, V_{INMIN} < V_{IN} < V_{INMAX} IL_{MIN} < IL < IL_{MAX} VGEN2 = 011, 100, 101, 110, 111, V_{INMIN} < V_{IN} < V_{INMAX} IL_{MIN} < IL < IL_{MAX}	V_{GEN2}	 V_{NOM} -0.05 V_{NOM} -3%	 V_{NOM} V_{NOM}	 V_{NOM} +0.05 V_{NOM} +3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, For any V_{INMIN} < V_{IN} < V_{INMAX}	$V_{GEN2LOR}$	 –	 –	 0.20	mV/mA
Line Regulation V_{INMIN} < V_{IN} < V_{INMAX}, For any IL_{MIN} < IL < IL_{MAX}	$V_{GEN2LIR}$	 –	 5.0	 8.0	mV
Short-circuit Protection Threshold V_{INMIN} < V_{IN} < V_{INMAX}, Short-circuit V_{OUT} to GND	$V_{GEN2SHT}$	 IL_{MAX}+20%	 –	 –	mA
VGEN2 LOW-POWER MODE DC - VGEN2MODE=1					
Output Voltage V_{OUT} - V_{INMIN} < V_{IN} < V_{INMAX}, IL_{MINLP} < IL < IL_{MAXLP} VGEN2 = 000 to 010 VGEN2 = 011 to 111	VGEN2LO	 V_{NOM} -0.05 V_{NOM} -3%	 V_{NOM} V_{NOM}	 V_{NOM} +0.05 V_{NOM} +3%	V
Current Load Range IL_{MINLP} to IL_{MAXLP}	I_{GEN2LO}	0.0	–	3.0	mA
VGEN3 GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} VGEN3CONFIG, VGEN3 = 01, 11 VGEN3CONFIG, VGEN3 = 00, 10	V_{INGEN3}	 V_{NOM}+0.2 UVDET	 – –	 4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX} Internal Pass FET External PNP (Not exceeding PNP max power)	I_{GEN3}	 0.0 0.0	 – –	 50 200	mA
Minimum Bypass Capacitor Value Internal pass device External pass device	C_{OGEN3}	 0.65 1.1	 2.2 2.2	 – –	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{GEN3}	 20	 –	 100	mΩ

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VGEN3 ACTIVE MODE DC					
Output Voltage V_{OUT} VGEN2 = 000, 001, 010, $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$	V_{GEN3}	V_{NOM} -3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, For any $V_{INMIN} < V_{IN} < V_{INMAX}$	$V_{GEN3LOR}$	–	–	0.40	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, For any $IL_{MIN} < IL < IL_{MAX}$	$V_{GEN3SHT}$	–	5.0	9.0	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short circuit V_{OUT} to GND	$V_{GEN3SHT}$	IL_{MAX}+20%	–	–	mA
VGEN3 LOW-POWER MODE DC					
Output Voltage V_{OUT} - (Accuracy) $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MINLP} < IL < IL_{MAXLP}$	V_{GEN3LO}	V_{NOM} -3%	V_{NOM}	V_{NOM} +3%	V
Current Load Range IL_{MINLP} to IL_{MAXLP}	I_{GEN3LO}	0.0	1.0	3.0	mA
CHARGE PATH REGULATOR					
Input Operating Voltage - CHRGRAW	V_{INCHRG}	$BATT_{MIN}$	–	5.6	V
Output Voltage Spread - VCHRG[2:0]=011, 1XX Charge current 1.0 mA to 100 mA Charge current 100 mA and above	BP_{SP}	 -1.5 -3.0	 – –	 1.5 1.5	%
Current Limit Tolerance (38) ICHRG[3:0] = 0001 ICHRG[3:0] = 0100 ICHRG[3:0] = 0110 All other settings	ΔI_{LIM}	 68 360 500 –	 80 400 560 –	 92 440 620 15	 mA mA mA %
Start-up Overshoot - Unloaded	$BP_{OS-START}$	v	–	2.0	%
Configuration Input Capacitance - CHRGRAW(39) Load Capacitor - BPSNS(39) Cable length	 C_{INCHRG} C_{BP} L_C	 – 10 –	 2.2 – –	 – 47 3.0	 µF µF m
THERMAL					
Thermal Warning Lower Threshold	T_{WL}	–	100	–	℃
Thermal Warning Higher Threshold	T_{WH}	–	120	–	℃
Thermal Warning Hysteresis	T_{WHYS}	–	3.0	–	℃
Thermal Protection Threshold	T_{PT}	–	140	–	℃
BACKLIGHT LED DRIVERS					
Absolute Accuracy - All current settings		–	–	15	%
Matching - At 400 mV, 21 mA		–	–	3.0	%
Leakage - LEDxDC[5:0] = 000000		–	–	1.0	µA
SIGNALING LED DRIVERS					
Absolute Accuracy - All current settings		–	–	15	%
Matching - At 400 mV, 21 mA		–	–	10	%
Leakage - LEDxDC[5:0] = 000000		–	–	1.0	µA

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40 °C ≤ T_A ≤ 85 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ACTIVE MODE DC					
Output Voltage V_{OUT} - (V_{NOM} = 2.775), V_{INMIN} < V_{IN} < V_{INMAX}, IL_{MIN} < IL < IL_{MAX}		4.4	5.0	5.25	V
ADC					
Converter Core Input Range Single ended voltage readings Differential readings		 0.0 -1.2	 – –	 2.4 1.2	V
Maximum Input Voltage(40) Channels ADIN5, ADIN6 and ADIN7		 –	 –	 BP	V
Integral Nonlinearity		–	–	3	LSB
Differential Nonlinearity		–	–	1	LSB
Zero Scale Error (Offset) after auto calibration		–	–	1	LSB
Full Scale Error (Gain) after auto calibration		–	–	5	LSB
Drift Over-temperature - Including scaling		–	–	1	LSB
Source Impedance No bypass capacitor at input Bypass capacitor at input 10 nF		 – –	 – –	 5.0 30	KΩ
TOUCH SCREEN					
Plate Maximum Voltage X, Y(41)		–	–	VCORE	V
Plate Resistance X, Y		100	–	1000	Ω
Resistance Between Plates Settling Time - Contact Position measurement		180 3.0	– –	1200 5.5	Ω µs
TOUCH SCREEN IN STAND ALONE MODE(42)					
Max Load Current - Active Mode		–	–	20	mA
Output Voltage - 0.0<IL<20 mA		-3%	1.20	+3%	V
PSRR - IL=15 mA		50	–	–	dB
Bypass Capacitor ESR		0.0	–	0.1	Ω
Bypass Capacitance		0.65	2.2	+35%	µF

Notes

38. Excludes spread and tolerance due to board and 100 mOhm sense resistor tolerances.
39. An additional derating of 35% is allowed.
40. ADIN5, 6 and 7 inputs must not exceed BP voltage.
41. TS[xy][1,2] inputs must not exceed BP or VCORE
42. All characteristics in this table are applicable only for non touch screen operation. This applies to Touch Screen in Standalone mode and below.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.65 V, -40 ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
32 KHZ CRYSTAL OSCILLATOR					
RTC oscillator start-up time Upon application of power	t_{RTCST}	–	–	1.0	Sec
CLK32K Rise and Fall Time - CL = 50 pF CLK32KDRV[1:0] = 00 (default) CLK32KDRV[1:0] = 01 CLK32KDRV[1:0] = 10 CLK32KDRV[1:0] = 11	$t_{CLK32KET}$	 – – – –	 22 11 High Z 44	 – – – –	ns
CLK32KMCU Rise and Fall Time CL = 12 pF	$t_{CLK32KMCUET}$	–	22	–	ns
CLK32K and CLK32KMCU Output Duty Cycle Crystal on XTAL1, XTAL2 pins	$t_{CLK32KDC}$, $t_{CLK32KMCUDC}$	45	–	55	%
CLK AND MISO					
MISO Rise and Fall Time, CL = 50 pF, SPIVCC = 1.8 V SPIDRV [1:0] = 00 (default) SPIDRV [1:0] = 01 SPIDRV [1:0] = 10 SPIDRV [1:0] = 11	t_{MISOET}	 – – – –	 11 6.0 High Z 22	 – – – –	ns
BUCK REGULATORS					
Turn-on Time, Enable to 90% of end value, IL = 0	t_{ONPWM}	–	–	500	µs
SWBST					
Turn-on Time Enable to 90% of V_{OUT}, IL = 0	t_{ONBST}	–	–	2.0	ms
Transient Load Response, IL from 1.0 mA to 100 mA in 1.0 µs steps Maximum transient Amplitude Time to settle 80% of transient	A_{TMAX}	 – –	 – –	 300 500	 mV µs
Transient Load Response, IL from 100 mA to 1.0 mA Maximum transient Amplitude Time to settle 80% of transient	A_{TMAX}	 – –	 – –	 300 20	 mV µs
VVIDEO ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV V_{IN} = V_{NOM} + 1.0 V	$V_{VIDEOPSSR}$	 35 50	 40 60	 – –	dB
Max Output Noise - V_{IN} = V_{INMIN}, IL = 75% of IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 10 kHz >10 kHz – 1.0 MHz	$V_{VIDEOON}$	 – – –	 -114 -124 -129	 – – –	dBV/√Hz
Turn-on Time Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VVIDEOt_{ON}$	–	–	1.0	ms
VVIDEO ACTIVE MODE - AC (CONTINUED)					
Turn-off Time Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VVIDEOt_{OFF}$	0.1	–	10	ms
Transient Load Response V_{IN} = V_{INMIN}, V_{INMAX}	$V_{VIDEOTLOR}$	–	1.0	2.0	%

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.65 V, -40 ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Transient Line Response IL = 75% of IL_{MAX}	$V_{VIDEOTLIR}$	–	5.0	8.0	mV
Mode Transition Time From low-power to active, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VVIDEOt_{MOD}$	–	–	100	µs
Mode Transition Response From low-power to active and from active to low-power, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$V_{VIDEOMTR}$	–	1.0	2.0	%
VAUDIO					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV, > UVDET V_{IN} = V_{NOM} + 1.0 V, > UVDET	$V_{AUDIOPSSR}$	 35 50	 40 60	 – –	dB
Max Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*ILmax 100 Hz – 1.0 kHz >1.0 kHz – 10 kHz >10 kHz – 1.0 MHz	$V_{AUDIOON}$	 – – –	 -114 -124 -129	 – – –	dBV/√Hz
Turn-on Time Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VAUDIOt_{ON}$	–	–	1.0	ms
Turn-off Time Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VAUDIOt_{OFF}$	0.1	–	10	ms
Transient Load Response - See Transient Waveforms on page 84, V_{IN} = V_{INMIN}, V_{INMAX}	$V_{AUDIOTLOR}$	–	1.0	2.0	%
Transient Line Response - See Transient Waveforms on page 84 IL = 75% of IL_{MAX}	$V_{AUDIOTLIR}$	–	5.0	8.0	mV
VPLL AND VDIG ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = UVDET V_{IN} = V_{NOM} + 1.0 V, > UVDET	VPLLPSSR	 35 50	 40 60	 – –	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*IL_{MAX} 100 Hz – 1.0 kHz >1 kHz – 1.0 MHz	VPLLON	 – –	 20 2.5	 – –	 dB/dec µV/√Hz
Turn-on Time Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VPLLt_{ON}$	–	–	100	µs
Turn-off Time Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VPLLt_{OFF}$	0.1	–	10	ms
Transient Load Response - See Transient Waveforms on page 84 V_{IN} = V_{INMIN}, V_{INMAX}	$V_{PLLTLOR}$, $V_{DIGTLOR}$	–	50	70	mV
Transient Line Response - See Transient Waveforms on page 84 IL = 75% of IL_{MAX}	$V_{PLLTLIR}$, $V_{DIGTLIR}$	–	5.0	8.0	mV

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.65 V, -40 ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VIOHI ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV, > UVDET V_{IN} = V_{NOM} + 1.0 V, > UVDET	$V_{IOHIPSSR}$	 35 50	 40 60	 – –	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 1.0 MHz	V_{IOHION}	 – –	 20 1.0	 – –	 dB/dec µV/√Hz
Turn-on Time Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VIOHIt_{ON}$	 –	 –	 1.0	ms
Turn-off Time Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VIOHIt_{OFF}$	 0.1	 –	 10	ms
Transient Load Response - See Transient Waveforms on page 84 V_{IN} = V_{INMIN}, V_{INMAX}	$V_{IOHITLOR}$	 –	 1.0	 2.0	%
Transient Line Response - See Transient Waveforms on page 84 IL = 75% of IL_{MAX}	$V_{IOHITLIR}$	 –	 5.0	 8.0	mV
Mode Transition Time - See Transient Waveforms on page 84 From low-power to active, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$V_{IOHIMTR}$	 –	 –	 10	µs
Mode Transition Response From low-power to active and from active to low-power, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$V_{IOHIMTR}$	–	1.0	2.0	%
VCAM ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV V_{IN} = V_{NOM} + 1.0 V	$V_{CAMPSSR}$	 35 50	 40 60	 – –	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 1.0 MHz	V_{CAMON}	 – –	 20 1.0	 – –	 dB/dec µV/√Hz
Turn-on Time (Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	$VCAMt_{ON}$	–	–	1.0	ms
Turn-off Time (Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	$VCAMt_{OFF}$	0.1	–	10	ms
Transient Load Response - See Transient Waveforms on page 84 V_{IN} = V_{INMIN}, V_{INMAX} VCAM = 01, 10, 11 VCAM = 00	V_{CAMLOR}	 – –	 1.0 50	 2.0 70	 % mV
Transient Line Response - See Transient Waveforms on page 84 IL = 75% of IL_{MAX}	V_{CAMLIR}	 –	 5.0	 8.0	mV
Mode Transition Time - See Transient Waveforms on page 84 From low-power to active, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VCAMt_{MOD}$	 –	 –	 100	µs
Mode Transition Response From low-power to active and from, active to low-power, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	V_{CAMMTR}	–	1.0	2.0	%

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.65 V, -40 ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VSD ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV V_{IN} = V_{NOM} + 1.0 V	V_{SDPSSR}	 35 50	 40 60	 – –	dB
Max Output Noise - V_{IN} = V_{INMIN}, IL = 75% of IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 10 kHz >10 kHz – 1.0 MHz	V_{SDON}	 – – –	 -115 -126 -132	 – – –	dBV/√Hz
Turn-on Time (Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	$VSDt_{ON}$	–	–	1.0	ms
Turn-off Time (Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	$VSDt_{OFF}$	0.1	–	10	ms
Transient Load Response - See Transient Waveforms on page 84 V_{IN} = V_{INMIN}, V_{INMAX} - VSD[2:0] = 010 to 111 - VSD[2:0] = 000 to 001	V_{SDTLOR}	 – –	 1.0 –	 2.0 70	 % mV
Transient Line Response - See Transient Waveforms on page 84 IL = 75% of IL_{MAX}	V_{SDTLIR}	 –	 5.0	 8.0	mV
Mode Transition Time - See Transient Waveforms on page 84 From low-power to active, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VSDt_{MOD}$	 –	 –	 100	µs
Mode Transition Response - See Transient Waveforms on page 84 From low-power to active and from active to low-power, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	V_{SDMTR}	 –	 1.0	 2.0	%
VUSB ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV	$V_{USBPSSR}$	 35	 40	 –	dB
Max Output Noise - V_{IN} = V_{INMIN}, IL = 75% of IL_{MAX} 100 Hz – 50 kHz >50 kHz – 1.0 MHz	V_{USBON}	 – –	 1.0 0.2	 – –	µV/√Hz
VUSB2 ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV V_{IN} = V_{NOM} + 1.0 V	$V_{USB2PSSR}$	 35 50	 40 60	 – –	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 1.0 MHz	V_{USB2ON}	 – –	 20 0.2	 – –	 dB/dec µV/√Hz
Turn-on Time Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VUSB2t_{ON}$	 –	 –	 100	µs
Turn-off Time Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VUSBt_{OFF}$	 0.1	 –	 10	ms
Start-up Overshoot V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	V_{USB2OS}	 –	 1.0	 2.0	%
Transient Load Response - See Transient Waveforms on page 84 V_{IN} = V_{INMIN}, V_{INMAX}	$V_{USB2TLOR}$	 –	 1.0	 2.0	%
Transient Line Response - See Transient Waveforms on page 84 IL = 75% of IL_{MAX}	$V_{USB2TLIR}$	 –	 5.0	 8.0	mV

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.65 V, -40 ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
UVBUS ACTIVE MODE DC					
Turn-on Time VBUS Rise Time per USB OTG with max loading of 6.5 µF+10 µF	$UVBUSt_{ON}$	– –	– –	100 –	ms
Turn-off Time Disable to 0.8 V, per USB OTG specification parameter VA_SESS_VLD, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$UVBUSt_{OFF}$	–	–	1.3	sec
VGEN1 ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = UVDET V_{IN} = V_{NOM} + 1.0 V, > UVDET	$V_{GEN1PSSR}$	 35 50	 40 60	 – –	dB
Max Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 10 kHz >10 kHz – 1.0 MHz	V_{GEN1ON}	 – – –	 -115 -126 -132	 – – –	dBV/√Hz
Turn-on Time Enable to 90% of end value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VGEN1t_{ON}$	–	–	1.0	ms
Turn-off Time Disable to 10% of initial value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VGEN1t_{OFF}$	0.1	–	10	ms
Transient Load Response - See Transient Waveforms on page 84 V_{IN} = V_{INMIN}, V_{INMAX} - VGEN1[1:0] = 10 to 11 - VGEN[1:0] = 00 to 01	$V_{GEN1TLOR}$	 – –	 1.0 –	 3.0 70	 % mV
Transient Line Response - See Transient Waveforms on page 84 IL = 75% of IL_{MAX}	$V_{GEN1TLIR}$	–	5.0	8.0	mV
Mode Transition Time - See Transient Waveforms on page 84 From low-power to active V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VGEN1t_{MOD}$	–	–	100	µs
Mode Transition Response - See Transient Waveforms on page 84 From low-power to active and from active to low-power V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$V_{GEN1MTR}$	–	1.0	2.0	%
VGEN2 ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV V_{IN} = V_{NOM} + 1.0 V	$V_{GEN2PSSR}$	 35 50	 40 60	 – –	dB
Max Output Noise - V_{IN} = V_{INMIN}, IL = IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 10 kHz >10 kHz – 1.0 MHz	V_{GEN2ON}	 – – –	 -115 -126 -132	 – – –	dBV/√Hz
Turn-on Time Enable to 90% of end value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VGEN2t_{ON}$	–	–	1.0	ms
Turn-off Time (Disable to 10% of initial value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	$VGEN2t_{OFF}$	0.1	–	10	ms
Transient Load Response - See Transient Waveforms on page 84 V_{IN} = V_{INMIN}, V_{INMAX} - VGEN2[2:0] = 100 to 111 - VGEN2[2:0] = 000 to 011	$V_{GEN2TLOR}$	 – –	 1.0 –	 3.0 70	 % mV
Transient Line Response - See Transient Waveforms on page 84 IL = 75% of IL_{MAX}	$V_{GEN2TLIR}$	–	5.0	8.0	mV

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.65 V, -40 ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VGEN2 ACTIVE MODE - AC (CONTINUED)					
Mode Transition Time - See Transient Waveforms on page 84 From low-power to active V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VGEN2t_{MOD}$	–	–	100	µs
Mode Transition Response - See Transient Waveforms on page 84 From low-power to active and from active to low-power V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$V_{GEN2MTR}$	–	1.0	2.0	%
VGEN3 ACTIVE MODE - AC					
PSRR IL = 75% of IL_{MAX}, 20 Hz to 20 kHz, V_{IN} = V_{INMIN} +100 mV V_{IN} = V_{NOM}+1.0 V	$V_{GEN3PSSR}$	 35 45	 40 50	 – –	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 75% of IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 1.0 MHz	V_{GEN3ON}	 – –	 20 1.0	 – –	 dB/dec µV/√Hz
Turn-on Time Enable to 90% of end value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VGEN3t_{ON}$	–	–	1.0	ms
Turn-off Time Disable to 10% of initial value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VGEN3t_{OFF}$	0.1	–	5.0	ms
Transient Load Response V_{IN} = V_{INMIN}, V_{INMAX} - VGEN3 = 1 - VGEN3 = 0	$V_{GEN3TLOR}$	 – –	 1.0 –	 2.0 70	 % mV
Transient Line Response (IL = 75% of IL_{MAX})	$V_{GEN3TLIR}$	–	5.0	8.0	mV
Mode Transition Time From low-power to active V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VGEN3t_{MOD}$	–	–	100	µs
Mode Transition Response From low-power to active and from active to low-power, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$V_{GEN3MTR}$	–	1.0	2.0	%
UVBUS - ACTIVE MODE DC					
Turn-on Time - VBUS Rise Time por USB OTG with max loading of 6.5 µF+10 µF		–	–	100	ms
Turn-off Time - Disable to 0.8 V, per USB OTG specification parameter VA_SESS_VLD V_{IN} = V_{INMIN}, V_{INMAX}, IL=0		–	–	1.3	sec
ADC					
Conversion Time per Channel - PLLX[2:0] = 100		–	–	10	µs
Turn On Delay If Switcher PLL was active If Switcher PLL was inactive		 – –	 0.0 5.0	 – 10	µs
TOUCH SCREEN					
Turn-on Time - 90% of output		–	–	500	µs

FUNCTIONAL DESCRIPTION

FUNCTIONAL PIN DESCRIPTION

CHARGER

CHRGRAW

1. Charger input. The charger voltage is measured through an ADC at this pin. The UVBUS pin must be shorted to CHRGRAW in cases where the charger is being supplied from the USB cable. The minimum voltage for this pin depends on BATTMIN threshold value (see Battery Interface and Control).

2. Output to battery supplied accessories. The battery voltage can be applied to an accessory by enabling the charge path for the accessory via the CHRGRAW pin. To accomplish this, the charger needs to be configured in reverse supply mode.

CHRGCTRL1

Driver output for charger path FET M1.

CHRGCTRL2

Driver output for charger path FET M2.

CHRGISNS

Charge current sensing point 1. The charge current is read by monitoring the voltage drop over the charge current 100 mΩ sense resistor connected between CHRGISNS and BPSNS.

BPSNS

1. BP sense point. BP voltage is sensed at this pin and compared with the voltage at CHRGRAW.

2. Charge current sensing point 2. The charge current is read by monitoring the voltage drop over the charge current 100 mΩ sense resistor. This resistor is connected between CHRGISNS and BPSNS.

BP

This pin is the application supply point, the input supply to the IC core circuitry. The application supply voltage is sensed through an ADC at this pin.

BATTFET

Driver output for battery path FET M3. If no charging system is required or single path is implemented, the pin BATTFET must be floating.

BATTISNS

Battery current sensing point 1. The current flowing out of and into the battery can be read via the ADC by monitoring the voltage drop over the sense resistor between BATT and BATTISNS.

BATT

Battery positive terminal. Battery current sensing point 2. The supply voltage of the battery is sensed through an ADC on this pin. The current flowing out of and into the battery can be read via the ADC by monitoring the voltage drop over the sense resistor between BATT and BATTISNS.

BATTISNSCC

Accumulated current counter current sensing point. This is the coulomb counter current sense point. It should be connected directly to the 0.020 Ω sense resistor via a separate route from BATTISNS. The coulomb counter monitors the current flowing in/out of the battery by integrating the voltage drop over the BATTISNCC and the BATT pin.

CFP AND CFM

Accumulated current filter cap plus and minus pins respectively. The coulomb counter will require a 10 μF output capacitor connected between these pins to perform a first order filtering of the signal across R1.

CHRGSE1B

An unregulated wall charger configuration can be built in which case this pin must be pulled low. When charging through USB, it can be left open since it is internally pulled up to VCORE. The recommendation is to place an external FET that can pull it low or left it open, depending on the charge method.

CHRGLED

Trickle LED driver output 1. Since normal LED control via the SPI bus is not always possible in the standalone operation, a current sink is provided at the CHRGLED pin. This LED is to be connected between this pin and CHRGRAW.

GNDCHRG

Ground for charger interface.

LEDR, LEDG AND LEDB

General purpose LED driver output Red, Green and Blue respectively. Each channel provides flexible LED intensity control. These pins can also be used as general purpose open drain outputs for logic signaling, or as generic PWM generator outputs.

GNDLED

Ground for LED drivers

IC CORE

VCORE

Regulated supply output for the IC analog core circuitry. It is used to define the PUMS VIH level during initialization. The bandgap and the rest of the core circuitry are supplied from VCORE. Place a 2.2 μF capacitor from this pin to GNDCORE.

VCOREDIG

Regulated supply output for the IC digital core circuitry. No external DC loading is allowed on VCOREDIG. VCOREDIG is kept powered as long as there is a valid supply and/or coin cell. Place a 2.2 μF capacitor from this pin to GNDCORE.

REFCORE

Main bandgap reference. All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at REFCORE. No external DC loading is allowed on REFCORE. Place a 100 nF capacitor from this pin to GNDCORE.

GNDCORE

Ground for the IC core circuitry.

POWER GATING

PWGTDRV1 AND PWGTDRV2

Power Gate Drivers.

PWGTDRV1 is provided for power gating peripheral loads sharing the processor core supply domain(s) SW1, and/or SW2, and/or SW3. In addition, PWGTDRV2 provides support to power gate peripheral loads on the SW4 supply domain.

In typical applications, SW1, SW2, and SW3 will both be kept active for the processor modules in state retention, and SW4 retained for the external memory in self refresh mode. SW1, SW2, and SW3 power gating FET drive would typically be connected to PWGTDRV1 (for parallel NMOS switches). SW4 power gating FET drive would typically be connected to PWGTDRV2. When Low-power Off mode is activated, the power gate drive circuitry will be disabled, turning off the NMOS power gate switches to isolate the maintained supply domains from any peripheral loading.

SWITCHERS

SW1IN, SW2IN, SW3IN AND SW4IN

Switchers 1, 2, 3, and 4 input. Connect these pins to BP to supply Switchers 1, 2, 3, and 4.

SW1FB, SW2FB, SW3FB AND SW4FB

Switchers 1, 2, 3, and 4 feedback. Switchers 1, 2, 3, and 4 output voltage sense respectively. Connect these pins to the farther point of each of their respective SWxOUT pin, in order to sense and maintain voltage stability.

SW1OUT

Switcher 1 output. Buck regulator for processor core(s).

GNDSW1

Ground for Switcher 1.

SW2OUT

Switcher 2 output. Buck regulator for processor SOG, etc.

GNDSW2

Ground for Switcher 2.

SW3OUT

Switcher 3 output. Buck regulator for internal processor memory and peripherals.

GNDSW3

Ground for switcher 3.

SW4OUT

Switcher 4 output. Buck regulator for external memory and peripherals.

GNDSW4

Ground for switcher 4.

DVS1 AND DVS2

Switcher 1 and 2 DVS input pins. Provided for pin controlled DVS on the buck regulators targeted for processor core supplies. The DVS pins may be reconfigured for Switcher Increment / Decrement (SID) mode control. When transitioning from one voltage to another, the output voltage slope is controlled in steps of 25 mV per time step. These pins must be set high in order for the DVS feature to be enabled for each of switchers 1 or 2, or low to disable it.

SWBSTIN

Switcher BST input. The 2.2 μH switcher BST inductor must be connected here.

SWBSTOUT

Power supply for gate driver for the internal power NMOS that charges SWBST inductor. It must be connected to BP.

SWBSTFB

Switcher BST feedback. When SWBST is configured to supply the UVBUS pin in OTG mode the feedback will be switched to sense the UVBUS pin instead of the SWBSTFB pin.

GNDSWBST

Ground for switcher BST.

REGULATORS

VINIOHI

Input of VIOHI regulator. Connect this pin to BP in order to supply VIOHI regulator.

VIOHI

Output regulator for high voltage IO. Fixed 2.775 V output for high-voltage level interface.

VINPLL AND VINDIG

The input of the regulator for processor PLL and Digital regulators respectively. VINDIG and VINPLL can be connected to either BP or a 1.8 V switched mode power supply rail, such as from SW4 for the two lower set points of each regulator (the 1.2 and 1.25 V output for VPLL, and 1.05 and 1.25 V output for VDIG). In addition, when the two upper set points are used (1.50 and 1.8 V outputs for VPLL, and 1.65 and 1.8 V for VDIG), they can be connected to either BP or a 2.2 V nominal external switched mode power supply rail, to improve power dissipation.

VPLL

Output of regulator for processor PLL. Quiet analog supply (PLL, GPS).

VDIG

Output regulator Digital. Low voltage digital (DPLL, GPS).

VVIDEODRV

Drive output for VVIDEO external PNP transistor.

VVIDEO

Output regulator TV DAC. This pin must be connected to the collector of the external PNP transistor of the VVIDEO regulator.

VINAUDIO

Input regulator VAUDIO. Typically connected to BP.

VAUDIO

Output regulator for audio supply.

VINUSB2

Input regulator VUSB2. This pin must always be connected to BP even if the regulators are not used by the application.

VUSB2

Output regulator for powering USB PHY.

VINCAMDRV

1. Input regulator camera using internal PMOS FET. Typically connected to BP.

2. Drive output regulator for camera voltage using external PNP device. In this case, this pin must be connected to the base of the PNP in order to drive it.

VCAM

Output regulator for the camera module. When using an external PNP device, this pin must be connected to its collector.

VSDDRV

Drive output for the VSD external PNP transistor.

VSD

Output regulator for multi-media cards such as micro SD, RS-MMC.

VGEN1DRV

Drive output for the VGEN1 external PNP transistor.

VGEN1

Output of general purpose 1 regulator.

VGEN2DRV

Drive output for the VGEN2 external PNP transistor.

VGEN2

Output of general purpose 2 regulator.

VINGEN3DRV

1. Input for the VGEN3 regulator when no external PNP transistor used. Typically connected to BP.

2. Drive output for VGEN3 in case an external PNP transistor is used on the application. In this case, this pin must be connected the base of the PNP transistor.

VGEN3

Output of general purpose 3 regulator.

VSRTC

Output regulator for the SRTC module on the processor. The VSRTC regulator provides the CLK32KMCU output level (1.2 V). Additionally, it is used to bias the low-power SRTC domain of the SRTC module integrated on certain FSL processors.

GNDREG1

Ground for regulators 1.

GNDREG2

Ground for regulators 2.

GNDREG3

Ground for regulators 3.

GENERAL OUTPUTS

GPO1

General purpose output 1. Intended to be used for battery thermistor biasing. In this case, connect a 10 KΩ resistor from GPO1 to ADIN5, and one from ADIN5 to GND.

GPO2

General purpose output 2.

GPO3

General purpose output 3.

GPO4

General purpose output 4. It can be configured for a muxed connection into Channel 7 of the GP ADC.

CONTROL LOGIC

LICELL

Coin cell supply input and charger output. The LICELL pin provides a connection for a coin cell backup battery or supercap. If the main battery is deeply discharged, removed, or contact-bounced (i.e., during a power cut), the RTC system and coin cell maintained logic will switch over to the LICELL for backup power. This pin also works as a current-limited voltage source for battery charging. A small capacitor should be placed from LICELL to ground under all circumstances.

XTAL1

32.768 kHz Oscillator crystal connection 1.

XTAL2

32.768 kHz Oscillator crystal connection 2.

GNDRTC

Ground for the RTC block.

CLK32K

32 kHz Clock output for peripherals. At system start-up, the 32 kHz clock is driven to CLK32K (provided as a peripheral clock reference), which is referenced to SPIVCC. The CLK32K is restricted to state machine activation in normal on mode.

CLK32KMCU

32 kHz Clock output for processor. At system start-up, the 32 kHz clock is driven to CLK32KMCU (intended as the CKIL input to the system processor) referenced to VSRTC. The driver is enabled by the start-up sequencer and the CLK32KMCU is programmable for Low-power Off mode control by the state machine.

RESETB AND RESETBMCU

Reset output for peripherals and processor respectively. These depend on the Power Control Modes of operation (See Functional Device Operation on page 40). These are meant as reset for the processor, or peripherals in a power up condition, or to keep one in reset while the other is up and running.

WDI

Watchdog input. This pin must be high to stay in the On mode. The WDI IO supply voltage is referenced to SPIVCC (normally connected to SW4 = 1.8 V). SPIVCC must therefore remain enabled to allow for proper WDI detection. If WDI goes low, the system will transition to the Off state or Cold Start (depending on the configuration).

STANDBY AND STANDBYSEC

Standby input signal from processor and from peripherals respectively.

To ensure that shared resources are properly powered when required, the system will only be allowed into Standby when both the application processor (which typically controls the STANDBY pin) and peripherals (which typically control the STANDBYSEC pin) allow it. This is referred to as a Standby event.

The Standby pins are programmable for Active High or Active Low polarity, and that decoding of a Standby event will take into account the programmed input polarities associated with each pin. Since the Standby pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes.

The state of the Standby pins only have influence in the On mode and are therefore ignored during start up and in the Watchdog phase. This allows the system to power up without concern of the required Standby polarities, since software can make adjustments accordingly, as soon as it is running.

INT

Interrupt to processor. Unmasked interrupt events are signaled to the processor by driving the INT pin high.

PWRON1, 2 AND 3

A turn on event can be accomplished by connecting an open drain NMOS driver to the PWRONx pin of the MC13892, so that it is in effect a parallel path for the power key.

In addition to the turn on event, the MC13892A/B/C/D versions include a global reset feature on the PWRON3 pin. On the A/B/C/D versions, the GLBRSTENB defaults to 0. In the MC13892A/C versions global reset is active low. Since GLBRSTENB defaults to 0, the global reset feature is enabled by default. In the MC13892B/D versions global reset is active high. Since GLBRSTENB defaults to 0, the global reset feature is disabled by default. The global reset function can be enabled or disabled by changing the SPI bit GLBRSTENB at any time, as shown in table below:

Device	Global Reset Function	GLBRSTENB Configuration	GLBRSTENB
MC13892	NO	N/A	N/A
MC13892A	YES	Active low	0 = Enabled (default) 1 = Disabled
MC13892B	YES	Active HI	0 = Disabled (default) 1 = Enabled
MC13892C	YES	Active low	0 = Enabled (default) 1 = Disabled
MC13892D	YES	Active HI	0 = Disabled (default) 1 = Enabled

The global reset feature powers down the part, disables the charger, resets the SPI registers to their default value and then powers back on. To generate a global reset, the PWRON3 pin needs to be pulled low for greater than 12 seconds and then pulled back high. If the PWRON3 pin is held low for less than 12 seconds, the pin will act as a normal PWRON pin.

PUMS1 AND PUMS2

Power up mode supply setting. Default start-up of the device is selectable by hardwiring the Power Up Mode Select pins. The Power Up Mode Select pins (PUMS1 and PUMS2) are used to configure the start-up characteristics of the regulators. Supply enabling and output level options are selected by hardworking the PUMS pins for the desired configuration.

MODE

USB LBP mode, normal mode, test mode selection & anti-fuse bias. During evaluation and testing, the IC can be configured for normal operation or test mode via the MODE pin as summarized in the following table.

MODE PIN STATE	MODE
Ground	Normal Operation
VCOREDIG	USB Low-power Boot Allowed
VCORE	Test Mode

GNDCTRL

Ground for control logic.

SPIVCC

Supply for SPI bus and audio bus

CS

CS held low at Cold Start configures the interface for SPI mode. Once activated, CS functions as the SPI Chip Select. CS tied to VCORE at Cold Start configures the interface for I^2C mode; the pin is not used in I^2C mode other than for configuration.

Because the SPI interface pins can be reconfigured for reuse as an I^2C interface, a configuration protocol mandates that the CS pin is held low during a turn on event for the IC (a weak pull-down is integrated on the CS pin).

CLK

Primary SPI clock input. In I^2C mode, this pin is the SCL signal (I^2C bus clock).

MOSI

Primary SPI write input. In I^2C mode, the MOSI pin hard wired to ground or VCORE is used to select between two possible addresses (A0 address selection).

MISO

Primary SPI read output. In I^2C mode, this pin is the SDA signal (bi-directional serial data line).

GNDSPI

Ground for SPI interface.

USB

UID

This pin identifies if a mini-A or mini-B style plug has been connected to the application. The state of the ID detection can be read via the SPI, to poll dedicated sense bits for a floating, grounded, or factory mode condition on the UID pin.

UVBUS

1. USB transceiver cable interface.
2. OTG supply output.

When SWBST is configured to supply the UVBUS pin in OTG mode, the feedback will switch to sense the UVBUS pin instead of the SWBSTFB pin.

VUSB

This is the regulator used to provide a voltage to an external USB transceiver IC.

VINUSB

Input option for VUSB; supplied by SWBST. This pin is internally connected to the UVBUS pin for OTG mode operation (for more details about OTG mode).

Note: When VUSBIN = 1, UVBUS will be connected via internal switches to VINUSB and incur some current drain on that pin, as much as 270 μA maximum, so care must be taken to disable this path and set this SPI bit (VUSBIN) to 0 to minimize current drain, even if SWBST and/or VUSB are disabled.

VBUSEN

External VBUS enable pin for the OTG supply. VBUS is defined as the power rail of the USB cable (+5.0 V).

A TO D CONVERTER

Note: The ADIN5/6/7 inputs must not exceed BP.

ADIN5

ADC generic input channel 5. ADIN5 may be used as a general purpose unscaled input, but in a typical application, ADIN5 is used to read out the battery pack thermistor. The thermistor must be biased with an external pull-up to a voltage rail greater than the ADC input range. In order to save current when the thermistor reading is not required, it can be biased from one of the general purpose IOs such as GPO1. A resistor divider network should assure the resulting voltage falls within the ADC input range, in particular when the thermistor check function is used.

ADIN6

ADC generic input channel 6. ADIN6 may be used as a general purpose unscaled input, but in a typical application, the PA thermistor is connected here.

ADIN7

ADC generic input channel 7, group 1. ADIN7 may be used as a general purpose unscaled input or as a divide by 2 scaled input. In a typical application, an ambient light sensor is connected here. A second general purpose input ADIN7B is available on channel 7. This input is muxed on the GPO4 pin. In the application, a second ambient light sensor is supposed to be connected here.

TSX1 AND TSX2, TSY1 AND TSY2 - Note: The TS[xy] [12] inputs must not exceed BP or VCORE.

Touch Screen Interfaces X1 and X2, Y1 and Y2. The touch screen X plate is connected to TSX1 and TSX2, while the Y plate is connected to Y1 and Y2. In inactive mode, these pins can also be used as general purpose ADC inputs. They are respectively mapped on ADC channels 4, 5, 6, and 7. In interrupt mode, a voltage is applied to the X-plate (TSX2) via a weak current source to VCORE, while the Y-plate is connected to ground (TSY1).

TSREF

Touch Screen Reference regulator. This regulator is powered from VCORE. In applications not supporting touch screen, the TSREF can be used as a low current general purpose regulator, or it can be kept disabled and the bypass capacitor omitted.

ADTRIG

ADC trigger input. A rising edge on this pin will start an ADC conversion.

GNDADC

Ground for A to D circuitry.

THERMAL GROUNDS

GNDSUB1-9

General grounds and thermal heat sinks.

FUNCTIONAL DEVICE OPERATION

PROGRAMMABILITY

INTERFACING OVERVIEW AND CONFIGURATION OPTIONS

The MC13892 contains a number of programmable registers for control and communication. The majority of registers are accessed through a SPI interface in a typical application. The same register set may alternatively be accessed with an I^2C interface that is muxed on SPI pins. The following table describes the muxed pin options for the SPI and I^2C interfaces. Further details for each interface mode follow in this chapter.

Table 7. SPI / I^2C Bus Configuration

Pin Name	SPI Mode Functionality	I2C Mode Functionality
CS	Configuration (43), Chip Select	Configuration (44)
CLK	SPI Clock	SCL: I^2C bus clock
MISO	Master In, Slave Out (data output)	SDA: Bi-directional serial data line
MOSI	Master Out, Slave In (data input)	A0 Address Selection (45)

Notes

43. CS held low at Cold Start configures interface for SPI mode; once activated, CS functions as the SPI Chip Select.
44. CS tied to VCORE at Cold Start configures interface for I^2C mode; the pin is not used in I^2C mode other than for configuration.
45. In I^2C mode, the MOSI pin hard wired to ground or VCORE is used to select between two possible addresses.

SPI INTERFACE

The MC13892 contains a SPI interface port, which allows access by a processor to the register set. Via these registers, the resources of the IC can be controlled. The registers also provide status information about how the IC is operating, as well as information on external signals.

The SPI interface pins can be reconfigured for reuse as an I^2C interface. As a result, a configuration protocol mandates that the CS pin is held low during a turn on event for the IC (a weak pull-down is integrated on the CS pin. With the CS pin held low during startup (as would be the case if connected to the CS driver of an unpowered processor, due to the integrated pull-down), the bus configuration will be latched for SPI mode.

The SPI port utilizes 32-bit serial data words comprised of 1 write/read_b bit, 6 address bits, 1 null bit, and 24 data bits. The addressable register map spans 64 registers of 24 data bits each.

The general structure of the register set is given in the following table. Bit names, positions, and basic descriptions are provided in SPI Bitmap. Expanded bit descriptions are included in the following functional chapters for application guidance. For brevity's sake, references are occasionally made herein to the register set as the “SPI map” or “SPI bits”, but note that bit access is also possible through the I^2C interface option, so such references are implied as generically applicable to the register set accessible by either interface.

Table 8. Register Set

Register		Register		Register		Register	
0	Interrupt Status 0	16	Unused	32	Regulator Mode 0	48	Charger 0
1	Interrupt Mask 0	17	Unused	33	Regulator Mode 1	49	USB0
2	Interrupt Sense 0	18	Memory A	34	Power Miscellaneous	50	Charger USB1
3	Interrupt Status 1	19	Memory B	35	Unused	51	LED Control 0
4	Interrupt Mask 1	20	RTC Time	36	Unused	52	LED Control 1
5	Interrupt Sense 1	21	RTC Alarm	37	Unused	53	LED Control 2
6	Power Up Mode Sense	22	RTC Day	38	Unused	54	LED Control 3
7	Identification	23	RTC Day Alarm	39	Unused	55	Unused
8	Unused	24	Switchers 0	40	Unused	56	Unused
9	ACC 0	25	Switchers 1	41	Unused	57	Trim 0
10	ACC 1	26	Switchers 2	42	Unused	58	Trim 1
11	Unused	27	Switchers 3	43	ADC 0	59	Test 0

Table 8. Register Set

Register		Register		Register		Register	
12	Unused	28	Switchers 4	44	ADC 1	60	Test 1
13	Power Control 0	29	Switchers 5	45	ADC 2	61	Test 2
14	Power Control 1	30	Regulator Setting 0	46	ADC 3	62	Test 3
15	Power Control 2	31	Regulator Setting 1	47	ADC4	63	Test 4

The SPI interface is comprised of the package pins listed in Table 9.

Table 9. SPI Interface Pin Description

SPI Bus	Description
CLK	Clock input line, data shifting occurs at the rising edge
MOSI	Serial data input line
MISO	Serial data output line
CS	Clock enable line, active high
Interrupt	**Description**
INT	Interrupt to processor
Supply	**Description**
SPIVCC	Processor SPI bus supply

SPI INTERFACE DESCRIPTION

The control bits are organized into 64 fields. Each of these 64 fields contains 32-bits. A maximum of 24 data bits are used per field. In addition, there is one “dead” bit between the data and address fields. The remaining bits include 6 address bits to address the 64 data fields and one write enable bit to select whether the SPI transaction is a read or a write.

The register set will be to a large extent compatible with the MC13783, in order to facilitate software development.

For each SPI transfer, first a one is written to the read/write bit if this SPI transfer is to be a write. A zero is written to the read/write bit if this is to be a read command only.

The CS line must remain high during the entire SPI transfer. To start a new SPI transfer, the CS line must go inactive and then go active again. The MISO line will be tri-stated while CS is low.

To read a field of data, the MISO pin will output the data field pointed to by the 6 address bits loaded at the beginning of the SPI sequence.

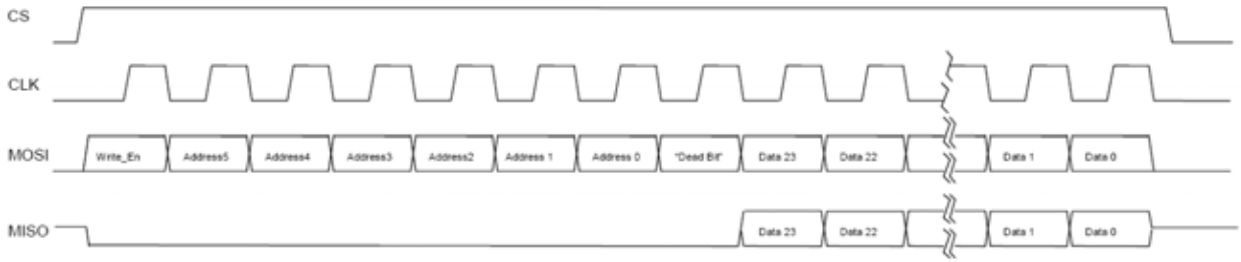


Figure 5. SPI Transfer Protocol Single Read/Write Access

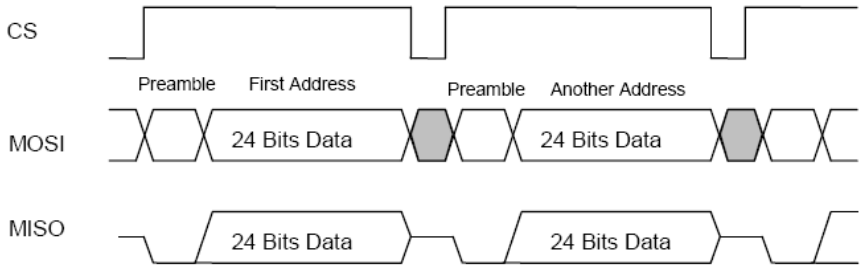


Figure 6. SPI Transfer Protocol Multiple Read/Write Access

SPI ELECTRICAL & TIMING REQUIREMENTS

The following diagram and table summarize the SPI electrical and timing requirements. The SPI input and output levels are set independently via the SPIVCC pin by connecting it to the desired supply. This would typically be tied to SW4 programmed for 1.80 V. The strength of the MISO driver is programmable through the SPIDRV[1:0] bits.

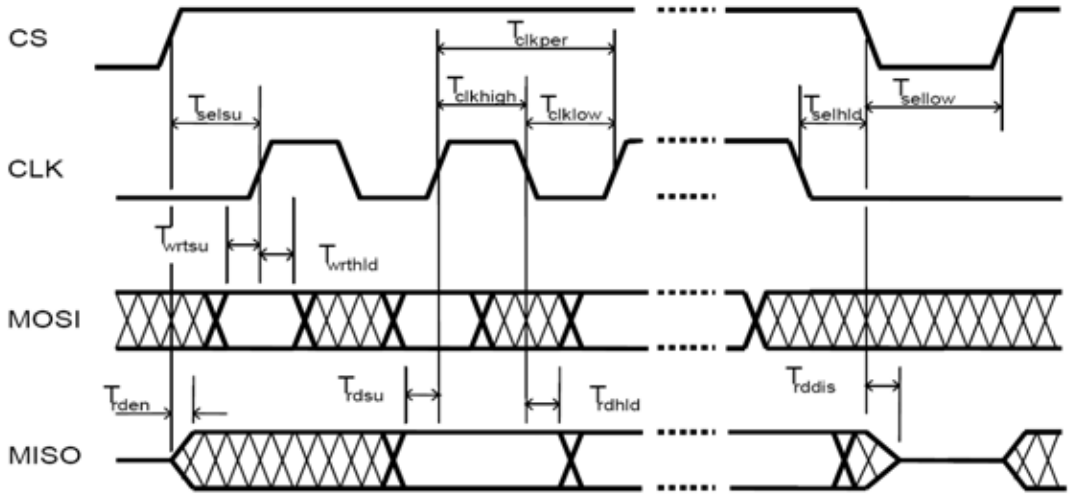


Figure 7. SPI Interface Timing Diagram

Table 10. SPI Interface Timing Specifications

Parameter	Description	t min (ns)
t_{SELSU}	Time CS has to be high before the first rising edge of CLK	15
t_{SELHLD}	Time CS has to remain high after the last falling edge of CLK	15
t_{SELLOW}	Time CS has to remain low between two transfers	15
t_{CLKPER}	Clock period of CLK	38
$t_{CLKHIGH}$	Part of the clock period where CLK has to remain high	15
t_{CLKLOW}	Part of the clock period where CLK has to remain low	15
t_{WRTSU}	Time MOSI has to be stable before the next rising edge of CLK	4.0
t_{WRTHLD}	Time MOSI has to remain stable after the rising edge of CLK	4.0
t_{RDSU}	Time MISO will be stable before the next rising edge of CLK	4.0
t_{RDHLD}	Time MISO will remain stable after the falling edge of CLK	4.0
t_{RDEN}	Time MISO needs to become active after the rising edge of CS	4.0
t_{RDDIS}	Time MISO needs to become inactive after the falling edge of CS	4.0

Notes
46. This table reflects a maximum SPI clock frequency of 26 MHz

Table 11. SPI Interface Logic IO Specifications

Parameter	Condition	Min	Typ	Max	Units
Input Low CS, MOSI, CLK		0.0	–	0.3*SPIVCC	V
Input High CS, MOSI, CLK		0.7*SPIVCC	–	SPIVCC+0.3	V
Output Low MISO, INT	Output sink 100 μA	0	–	0.2	V
Output High MISO, INT	Output source 100 μA	SPIVCC-0.2	–	SPIVCC	V
SPIVCC Operating Range		1.75	–	3.1	V
MISO Rise and Fall Time	CL = 50 pF, SPIVCC = 1.8 V				
	SPIDRV[1:0] = 00 (default)	–	11	–	ns
	SPIDRV[1:0] = 01	–	6.0	–	ns
	SPIDRV[1:0] = 10	–	High Z	–	ns
	SPIDRV[1:0] = 11	–	22	–	ns

I²C INTERFACE

I²C CONFIGURATION

When configured for I²C mode (see Table 7) the interface may be used to access the complete register map previously described for SPI access. The MC13892 can function only as an I²C slave device, not as a host.

I²C interface protocol requires a device ID for addressing the target IC on a multi-device bus. To allow flexibility in addressing for bus conflict avoidance, pin programmable selection is provided through the MOSI pin to allow configuration for the address LSB(s). This product supports 7-bit addressing only; support is not provided for 10-bit or General Call addressing.

The I²C mode of the interface is implemented generally following the Fast Mode definition which supports up to 400 kbits/s operation. Timing diagrams, electrical specifications, and further details can be found in the I²C specification.

Standard I²C protocol utilizes packets of 8-bits (bytes), with an acknowledge bit (ACK) required between each byte. However, the number of bytes per transfer is unrestricted. The register map of the MC13892 is organized in 24-bit registers which corresponds to the 24-bit words supported by the SPI protocol of this product. To ensure that the I²C operation mimics SPI transactions in behavior of a complete 24-bit word being written in one transaction, software is expected to perform write transactions to the device in 3 byte sequences, beginning with the MSB. Internally, data latching will be gated by the acknowledge at the completion of writing the third consecutive byte.

Failure to complete a 3 byte write sequence will abort the I²C transaction and the register will retain its previous value. This could be due to a premature STOP command from the master.

I²C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and 3 bytes will be sent out, unless a STOP command or NACK is received prior to completion.

The following examples show how to write and read data to the IC. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device will respond to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NAK is received, the host should terminate the current transaction and retry the transaction.

I²C DEVICE ID

The I²C interface protocol requires a device ID for addressing the target IC on a multi-device bus. To allow flexibility in addressing for bus conflict avoidance, pin programmable selection is provided to allow configuration for the address LSB(s). This product supports 7-bit addressing only. Support is not provided for 10-bit or General Call addressing.

Because the MOSI pin is not utilized for I²C communication, it is reassigned for pin programmable address selection by hardwiring to VCORE or GND at the board level, when configured for I²C mode. MOSI will act as Bit 0 of the address. The I²C address assigned to FSL PM ICs (shared amongst our portfolio) is as follows:

00010-A1-A0, where the A1 and A0 bits are allowed to be configured for either 1 or 0. It is anticipated for a maximum of two FSL PM ICs on a given board, which could be sharing an I²C bus. The A1 address bit is internally hard wired as a “0”, leaving the LSB A0 for board level configuration. The A1 bit will be implemented such that it can be re-wired as a “1” (with a metal change or fuse trim), if conflicts are encountered before the final production material is manufactured. The designated address is defined as: 000100-A0.

I²C OPERATION

The I²C mode of the interface is implemented, generally following the Fast mode definition, which supports up to 400 kbits/s operation. The exceptions to the standard are noted to be 7-bit only addressing, and no support for General Call addressing. Timing diagrams, electrical specifications, and further details can be found in the I²C specification, which is available for download at:

http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

Standard I²C protocol utilizes bytes of 8-bits, with an acknowledge bit (ACK) required between each byte. However, the number of bytes per transfer are unrestricted. The register map is organized in 24-bit registers, which corresponds to the 24-bit words supported by the SPI protocol of this product. To ensure that I²C operation mimics SPI transactions in behavior of a complete 24-bit word being written in one transaction. The software is expected to perform write transactions to the device in 3 byte sequences, beginning with the MSB. Internally, data latching will be gated by the acknowledge at the completion of writing the third consecutive byte.

Failure to complete a 3 byte write sequence will abort the I²C transaction, and the register will retain its previous value. This could be due to a premature STOP command from the master, for example. I²C read operations are also performed in byte

increments separated by an ACK. Read operations also begin with the MSB, and 3 bytes will be sent out unless a STOP command or NACK is received prior to completion.

The following examples show how to write and read data to the IC. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device will respond to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NAK is received, the host should terminate the current transaction and retry the transaction.

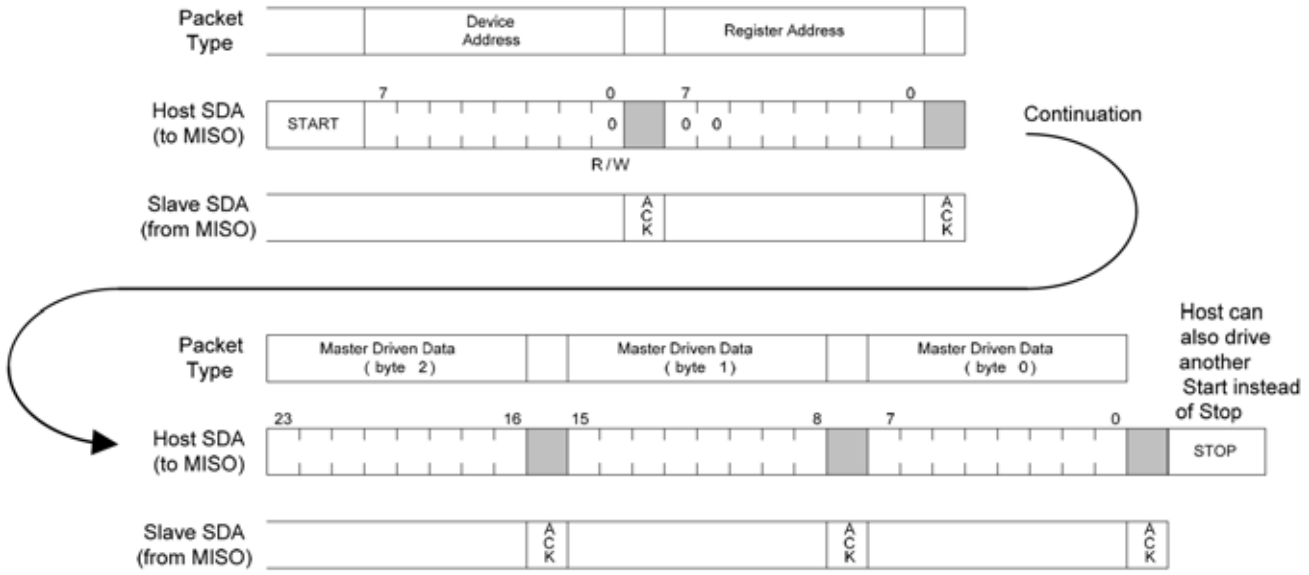


Figure 8. I²C 3 Byte Write Example

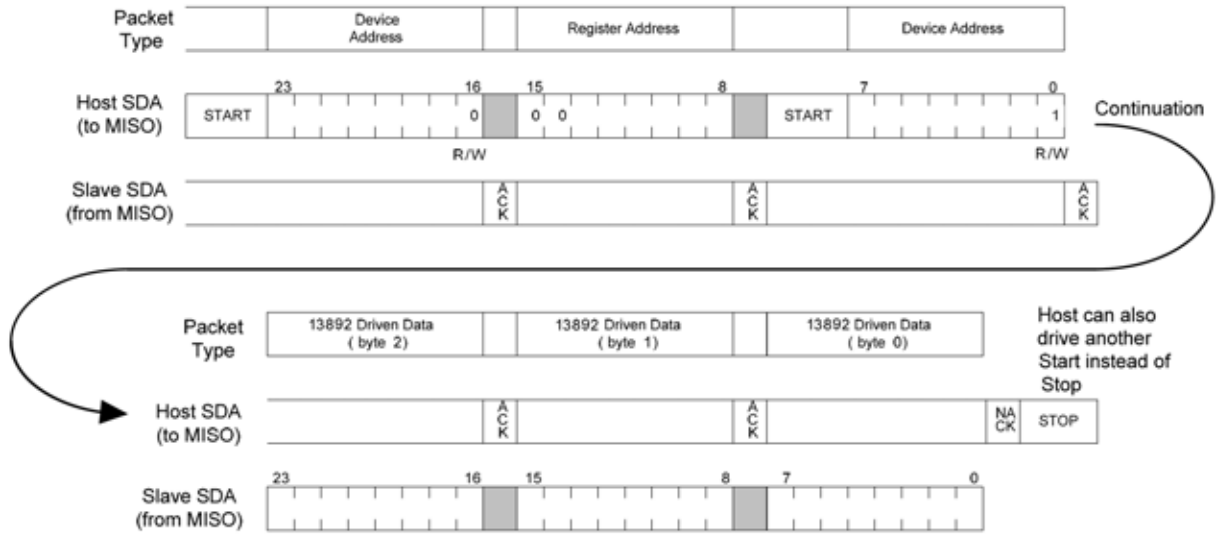


Figure 9. I²C 3 Byte Read Example

INTERRUPT HANDLING

CONTROL

The MC13892 has interrupt generation capability to inform the system on important events occurring. An interrupt is signaled to the processor by driving the INT pin high. This is true whether the communication interface is configured for the SPI or I^2C.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain set until cleared. Each interrupt can be cleared by writing a 1 to the appropriate bit in the Interrupt Status register. This will also cause the interrupt line to go low. If a new interrupt occurs while the processor clears an existing interrupt bit, the interrupt line will remain high.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the interrupt line will not go high. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked except the USB low-power boot, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the interrupt line will go high after unmasking.

The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable.

Interrupts generated by external events are debounced, meaning that the event needs to be stable throughout the debounce period before an interrupt is generated.

BIT SUMMARY

Table 12 summarizes all interrupt, mask, and sense bits associated with INT control. For more detailed behavioral descriptions, refer to the related chapters.

Table 12. Interrupt, Mask and Sense Bits

Interrupt	Mask	Sense	Purpose	Trigger	DebounceTime	Section
ADCDONEI	ADCDONEM	–	ADC has finished requested conversions	L2H	0	page 100
ADCBISDONEI	ADCBISDONEM	–	ADCBIS has finished requested conversions	L2H	0	page 100
TSI	TSM	–	Touch screen wake-up	Dual	30ms	page 100
CHGDETI	CHGDETM	CHGDETS CHGENS	Charger detection sense is 1 if detected Charger state sense is 1 if active	Dual	32 ms 100 ms	page 89
USBOVI	USBOVM	USBOVS	VBUS over-voltage Sense is 1 if above threshold	Dual	60 µs	page 89
CHGREVI	CHGREVM	–	Charger path reverse current	L2H	1.0 ms	page 89
CHGSHORTI	CHGSHORTM	–	Charger path short circuit	L2H	1.0 ms	page 89
CHGFAULTI	CHGFAULTM	CHGFAULTS[1:0]	Charger fault detection 00 = Cleared, no fault 01 = Charge source fault 10 = Battery fault 11 = Battery temperature	L2H	10 ms	page 89
CHGCURRI	CHGCURRM	CHGCURRS	Charge current below threshold Sense is 1 if above threshold	H2L	1.0 ms	page 89
CCCVI	CCCVM	CCCVS	CCCVI transition detection	Dual	100 ms	page 89
BPONI	BPONM	BPONS	BP turn on threshold detection. Sense is 1 if above threshold.	L2H	30 ms	page 54
LOBATLI	LOBATLM	LOBATLS	Low battery detect Sense is 1 if below LOBATL threshold	L2H	0	page 54
BVALIDI	BVALIDM	BVALIDS	USB B-session valid Sense is 1 if above threshold	Dual	L2H: 20-24 ms H2L: 8-12 ms	page 111

Table 12. Interrupt, Mask and Sense Bits

Interrupt	Mask	Sense	Purpose	Trigger	DebounceTime	Section
LOBATHI	LOBATHM	LOBATHS	Low battery warning Sense is 1 if above LOBATH threshold.	Dual	30 µs	page 54
VBUSVALIDI	VBUSVALIDM	VBUSVALIDS	Detects A-Session Valid on VBUS	Dual	L2H: 20-24 ms H2L: 8-12 ms	page 111
IDFLOATI	IDFLOATM	IDFLOATS	ID floating detect. Sense is 1 if above threshold	Dual	90 µs	page 111
IDGNDI	IDGNDM	IDGNDS	USB ID ground detect. Sense is 1 if not to ground	Dual	90 µs	page 111
IDFACTORYI	IDFACTORYM	IDFACTORYS	ID voltage for Factory mode detect Sense is 1 if above threshold	Dual	90 µs	page 111
CHRGSE1BI	CHRGSE1BM	CHRSE1BS	Wall charger detect Regulator short-circuit protection tripped	Dual L2H	1.0 ms 200 µs	page 89
SCPI	SCPS	–	Short circuit protection trip detection	L2H	0	page 71
BATTDETBI	BATTDETBM	BATTDETBS	Battery removal detect	Dual	30 ms	page 100
1HZI	1HZM	–	1.0 Hz time tick	L2H	0	page 49
TODAI	TODAM	–	Time of day alarm	L2H	0	page 49
PWRON1I	PWRON1M	PWRON1S	PWRON1 event Sense is 1 if pin is high.	H2L	30 ms (1)	page 54
				L2H	30 ms	page 54
PWRON2I	PWRON2M	PWRON2S	PWRON2 event Sense is 1 if pin is high.	H2L	30 ms (47)	page 54
				L2H	30 ms	page 54
PWRON3I	PWRON3M	PWRON3S	PWRON3 event Sense is 1 if pin is high.	H2L	30 ms (47)	page 54
				L2H	30 ms	page 54
SYSRSTI	SYSRSTM	–	System reset through PWRONx pins	L2H	0	page 54
WDIRESETI	WDIRESETM	–	WDI silent system restart	L2H	0	page 54
PCI	PCM	–	Power cut event	L2H	0	page 54
WARMI	WARMM	–	Warm Start event	L2H	0	page 54
MEMHLDI	MEMHLDM	–	Memory Hold event	L2H	0	page 54
CLKI	CLKM	CLKS	Clock source change Sense is 1 if source is XTAL	Dual	0	page 49
RTCRSTI	RTCRSTM	–	RTC reset or intrusion has occurred	L2H	0	page 49
THWARNHI	THWARNHM	THWARNHS	Thermal warning higher threshold Sense is 1 if above threshold	Dual	30 ms	page 71
THWARNLI	THWARNLM	THWARNLS	Thermal warning lower threshold Sense is 1 if above threshold	Dual	30 ms	page 71
LPBI	LPBM	LPBS	Low-power boot interrupt	Dual	1.0 ms	page 89

Notes
47. Debounce timing for the falling edge can be extended with PWRONxDBNC[1:0]; refer to Power Control System for details.

Additional sense bits are available to reflect the state of the power up mode selection pins, as summarized in Table 13.

Table 13. Additional Sense Bits

Sense	Description	Section
MODES[1:0]	00 = MODE grounded 10 = MODE to VCOREDIG 11 = MODE to VCORE	page 40
PUMSxS[1:0]	00 = PUMS grounded 01 = PUMS open 10 = PUMS to VCOREDIG 11 = PUMS to VCORE	page 54
CHRGSSS	0 = Single path 1 = Serial path	page 89

SPECIFIC REGISTERS

IDENTIFICATION

The MC13892 parts can be identified though identification bits which are hardwired on chip.

The version of the MC13892 can be identified by the ICID[2:0] bits. This is used to distinguish future derivatives or customizations of the MC13892. The bits are set to ICID[2:0] = 111 and are located in the revision register.

The revision of the MC13892 is tracked with the revision identification bits REV[4:0]. The bits REV[4:3] track the full mask set revision, where bits REV[2:0] track the metal revisions. These bits are hardwired.

Table 14. IC Revision Bit Assignment

Bits REV[4:0]	IC Revision
10001	Pass 3.1

The bits FIN[3:0] are Freescale use only and are not to be explored by the application.

The MC13892 die is produced using different wafer fabrication plants. The plants can be identified via the FAB[1:0] bits. These bits are hardwired.

MEMORY REGISTERS

The MC13892 has a small general purpose embedded memory of two times 24-bits to store critical data. The data is maintained when the device is turned off and when in a power cut. The contents are only reset when a RTC reset occurs, see Clock Generation and Real Time Clock.

CLOCK GENERATION AND REAL TIME CLOCK

CLOCK GENERATION

The MC13892 generates a 32.768 kHz clock as well as several 32.768 kHz derivative clocks that are used internally for control.

Support is also provided for an external Secure Real Time Clock (SRTC) which may be integrated on a companion system processor IC. For media protection in compliance with Digital Rights Management (DRM) system requirements, the CLK32KMCU can be provided as a reference to the SRTC module where tamper protection is implemented.

CLOCKING SCHEME

The MC13892 contains an internal 32 kHz oscillator, that delivers a 32 kHz nominal frequency (20%) at its outputs when an external 32.768 kHz crystal is not present.

If a 32.768 kHz crystal is present and running, then all control functions will run off the crystal derived 32 kHz oscillator. In absence of a valid supply at the BP supply node (for instance due to a dead battery), the crystal oscillator continues running, supplied from the coin cell battery until the coin cell is depleted.

The 32 kHz clock is driven to two output pins, CLK32KMCU (intended as the CKIL input to the system processor) is referenced to VSRTC, and CLK32K (provided as a clock reference for the peripherals) is referenced to SPIVCC. The driver is enabled by the startup sequencer, and CLK32KMCU is programmable for Low-power Off mode, controlled by the state machine. Additionally, a SPI bit CLK32KMCUEN bit is provided for direct SPI control. The CLK32KMCUEN bit defaults to a 1 and resets on RTCPORB, to ensure the buffer is activated at the first power up and configured as desired for subsequent power ups. CLK32K is restricted to state machine activation in normal On mode.

The drive strength of the CLK32K output drivers are programmable with CLK32KDRV[1:0] (master control bits that affect the drive strength of CLK32K).

During a switchover between the two clock sources (such as when the crystal oscillator is starting up), the output clock is maintained at a stable active low or high phase of the internal 32 kHz clock to avoid any clocking glitches. If the XTAL clock source suddenly disappears during operation, the IC will revert back to the internal clock source. Given the unpredictable nature of the event and the startup times involved, the clock may be absent long enough for the application to shut down during this transition, for example, due to a sag in the switchover output voltage, or absence of a signal on the clock output pins.

A status bit, CLKS, is available to indicate to the processor which clock is currently selected: CLKS=0 when the internal RC is used, and CLKS=1 if the XTAL source is used. The CLKI interrupt bit will be set whenever a change in the clock source occurs, and an interrupt will be generated if the corresponding CLKM mask bit is cleared.

OSCILLATOR SPECIFICATIONS

The crystal oscillator has been designed for use in conjunction with the Micro Crystal CC7V-T1A-32.768 kHz-9pF-30 ppm or equivalent (such as Micro Crystal CC5V-T1A or Epson FC135).

Table 15. RTC Crystal Specifications

Nominal Frequency	32.768 kHz
Make Tolerance	+/-30 ppm
Temperature Stability	-0.038 ppm /C^2
Series Resistance	80 kOhm
Maximum Drive Level	1.0 μW
Operating Drive Level	0.25 to 0.5 μW
Nominal Load Capacitance	9.0 pF
Pin-to-pin Capacitance	1.4 pF
Aging	3 ppm/year

The oscillator also accepts a clock signal from an external source. This clock signal is to be applied to the XTAL1 pin, where the signal can be DC or AC coupled. A capacitive divider can be used to adapt the source signal to the XTAL1 input levels. When applying an external source, the XTAL2 pin is to be connected to VCOREDIG.

The electrical characteristics of the 32 kHz Crystal oscillator are given in the table below, taking into account the above crystal characteristics

Table 16. Crystal Oscillator Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage	Oscillator and RTC Block from BP	1.2	–	4.65	V
Coin cell Disconnect Threshold	At LICELL	1.8	–	2.0	V
RTC oscillator startup time	Upon application of power	-	–	1.0	sec
XTAL1 Input Level	External clock source	0.3	–	-	V_{PP}
XTAL1 Input Range	External clock source	-0.5	–	1.2	V
Output Low CLK32K, CLK32KMCU	Output sink 100 μA	0	–	0.2	V
Output High	CLK32K Output source 100 μA	SPIVCC-0.2	–	SPIVCC	V
	CLK32KMCU Output source 100 μA	VSRTC-0.2	–	VSRTC	V
CLK32K Rise and Fall Time	CL=50 pF				
	CLK32KDRV[1:0] = 00 (default)	–	22	–	ns
	CLK32KDRV[1:0] = 01	–	11	–	ns
	CLK32KDRV[1:0] = 10	–	High Z	–	ns
	CLK32KDRV[1:0] = 11	–	44	–	ns
CLD32KMCU Rise and Fall Time	CL=12 pF	–	22	–	ns
CLK32K and CLK32KMCU Output Duty Cycle	Crystal on XTAL1, XTAL2 pins	45	–	55	%

OSCILLATOR APPLICATION GUIDELINES

The guidelines below may prove to be helpful in providing a crystal oscillator that starts reliably and runs with minimal jitter.

PCB leakage: The RTC amplifier is a low-current circuit. Therefore, PCB leakage may significantly change the operating point of the amplifier and even the drive level to the crystal. (Changing the drive level to the crystal may change the aging rate, jitter, and even the frequency at a given load capacitance.) The traces should be kept as short as possible to minimize the leakage, and good PCB manufacturing processes should be maintained.

Layout: The traces from the MC13892 to the crystal, load capacitance, and the RTC Ground are sensitive. They must be kept as short as possible with minimal coupling to other signals. The signal ground for the RTC is to be connected to GNDRTC, and via a single connection, GNDRTC to the system ground. The CLK32K and CLK32KMCU square wave outputs must be kept away from the crystal / load capacitor leads, as the sharp edges can couple into the circuit and lead to excessive jitter. The crystal / load capacitance leads and the RTC Ground must form a minimal loop area.

Crystal Choice: Generally speaking, crystals are not interchangeable between manufacturers, or even different packages for a given manufacturer. If a different crystal is considered, it must be fully characterized with the MC13892 before it can be considered.

Tuning Capacitors: The nominal load capacitance is 9.0 pF, therefore the total capacitance at each node should be 18 pF, composed out of the load capacitance, the effective input capacitance at each pin, plus the PCB stray capacitance for each pin.

SRTC SUPPORT

The MC13892 provides support for processors which have an integrated SRTC for Digital Rights Management (DRM), by providing a VSRTC voltage to bias the SRTC module of the processor, as well as a CLK32KMCU at the VSRTC output level.

When configured for DRM mode (SPI bit DRM = 1), the CLK32MCU driver will be kept enabled through all operational states, to ensure that the SRTC module always has its reference clock. If DRM = 0, the CLK32KMCU driver will not be maintained in the Off state. Refer to Table 23 for the operating behavior of the CLK32KMCU output in User Off, Memory Hold, User off Wait, and internal MEMHOLD PCUT modes.

It is also necessary to provide a means for the processor to do an RTC initiated wake-up of the system, if it has been programmed for such capability. This can be accomplished by connecting an open drain NMOS driver to the PWRON pin of the MC13892, so that it is in effect a parallel path for the power key. The MC13892 will not be able to discern the turn on event from a normal power key initiated turn on, but the processor should have the knowledge, since the RTC initiated turn on is generated locally.

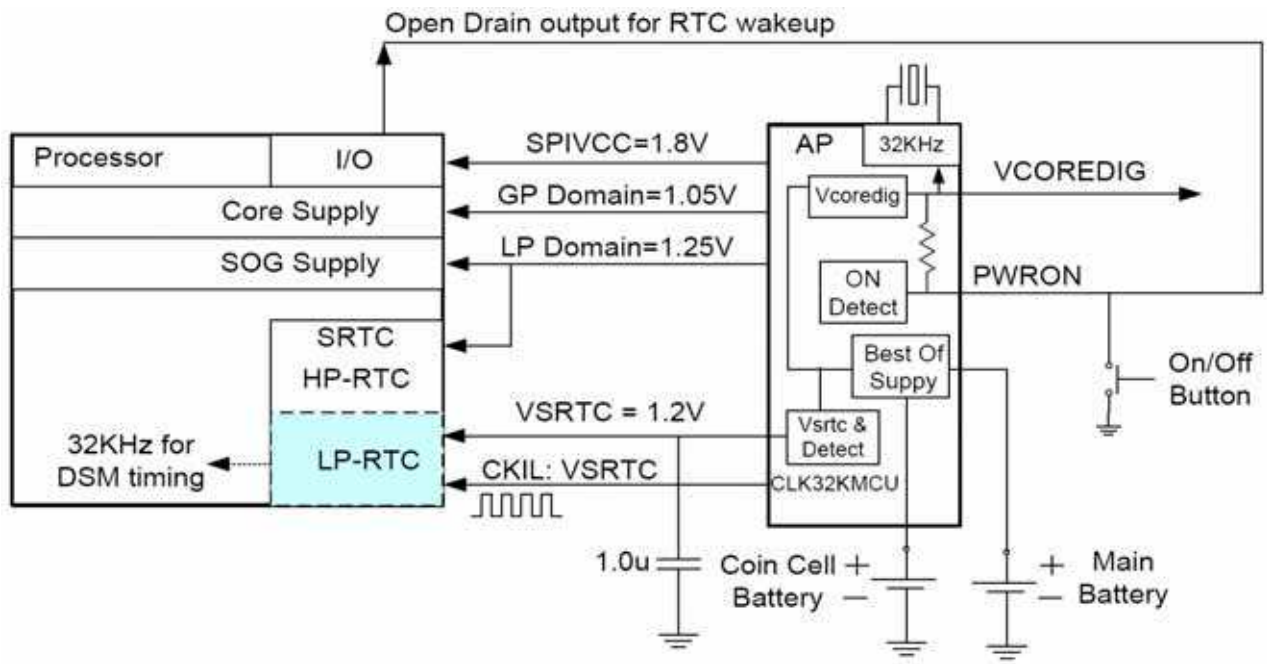


Figure 10. SRTC block diagram

VSRTC

The VSRTC regulator provides the CLK32KMCU output level. It is also used to bias the Low-power SRTC domain of the SRTC module integrated on certain FSL processors. The VSRTC regulator is enabled as soon as the RTCPORB is detected. The VSRTC cannot be disabled.

Table 17. VSRTC Specifications

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range, V_{INMIN} to V_{INMAX}	Valid Coin Cell range or valid BP	1.8	–	3.6	V
		UVDET	–	4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}		0.0	–	50	µA
Bypass Capacitor Value		–	1.0	–	µF
Active Mode - DC					
Output Voltage V_{OUT}	$V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$	1.150	1.20	1.25	V

REAL TIME CLOCK

A real Time Clock (RTC) function is provided including time and day counters as well as an alarm function. The utilizes a 32 kHz clock, either the RC oscillator or the 32.768 kHz crystal oscillator as a time base, and is powered by the coin cell backup supply when BP has dropped below operational range. In configurations where the SRTC is used, the RTC can be disabled to conserve current drain by setting the RTCDIS bit to a 1 (defaults on at power up).

TIME AND DAY COUNTERS

The 32 kHz clock is divided down to a 1.0 Hz time tick which drives a 17-bit Time Of Day (TOD) counter. The TOD counter counts the seconds during a 24 hour period from 0 to 86,399, and will then roll over to 0. When the roll over occurs, it increments the 15-bit DAY counter. The DAY counter can count up to 32767 days. The 1.0 Hz time tick can be used to generate a 1HZI interrupt if unmasked.

TIME OF DAY ALARM

A Time Of Day Alarm (TODA) function can be used to turn on the application and alert the processor. If the application is already on, the processor will be interrupted. The TODA and DAYA registers are used to set the alarm time. Only a single alarm can be programmed at a time. When the TOD counter is equal to the value in TODA, and the DAY counter is equal to the value in DAYA, the TODAI interrupt will be generated.

At initial power up of the application (application of the coin cell), the state of the TODA and DAYA registers will be all 1's. The interrupt for the alarm (TODAI) is backed up by LICELL and will be valid at power up. If the mask bit for the TOD alarm (TODAM) is high, then the TODAI interrupt is masked and the application will not turn on with the time of day alarm event (TOD[16:0] = TODA[16:0] and DAY[14:0] = DAYA[14:0]). By default, the TODAM mask bit is set to 1, thus masking the interrupt and turn on event.

TIMER RESET

As long as the supply at BP is valid, the real time clock will be supplied from VCORE. If not, it can be backed up from a coin cell via the LICELL pin. When the backup voltage drops below RTCUVDET, the RTCPORB reset signal is generated and the contents of the RTC will be reset. Additional registers backed up by coin cell will also reset with RTCPORB. To inform the processor that the contents of the RTC are no longer valid due to the reset, a timer reset interrupt function is implemented with the RTCRSTI bit.

RTC TIMER CALIBRATION

A clock calibration system is provided to adjust the 32,768 cycle counter that generates the 1.0 Hz timer for RTC timing registers to comply with digital rights management specifications of ±50 ppm. This calibration system can be disabled, if not needed to reduce the RTC current drain. The general implementation relies on the system processor to measure the 32.768 kHz crystal oscillator against a higher frequency and more accurate system clock such as a TCXO. If the RTC timer needs a correction, a 5-bit 2's complement calibration word can be sent via the SPI to compensate the RTC for inaccuracy in its reference oscillator as defined in Table 18.

Table 18. RTC Calibration Settings

Code in RTCCAL[4:0]	Correction in Counts per 32768	Relative correction in ppm
01111	+15	+458
00011	+3	+92
00001	+1	+31
00000	0	0
11111	-1	-31
11101	-3	-92
10001	-15	-458
10000	-16	-488

Note that the 32.768 kHz oscillator is not affected by RTCCAL settings. Calibration is only applied to the RTC time base counter. Therefore, the frequency at the clock outputs CLK32K and CLK32KMCU are not affected.

The RTC system calibration is enabled by programming the RTCCALMODE[1:0] for desired behavior by operational mode.

Table 19. RTC Calibration Enabling

RTCCALMODE	Function
00	RTC Calibration disabled (default)
01	RTC Calibration enabled in all modes except coin cell only
10	Reserved for future use. Do not use.
11	RTC Calibration enabled in all modes

A slight increase in consumption will be seen when the calibration circuitry is activated. To minimize consumption and maximize lifetime when the RTC system is maintained by the coin cell, the RTC Calibration circuitry can be automatically disabled when main battery contact is lost, or if it is so deeply discharged that RTC power draw is switched to the coin cell (configured with RTCCALMODE = 01).

Because of the low RTC consumption, RTC accuracy can be maintained through long periods of the application being shut down, even after the main battery has discharged. However, it is noted that the calibration can only be as good as the RTCCAL

data that has been provided, so occasional refreshing is recommended to ensure that any drift influencing environmental factors have not skewed the clock beyond desired tolerances.

COIN CELL BATTERY BACKUP

The LICELL pin provides a connection for a coin cell backup battery or supercap. If the main battery is deeply discharged, removed, or contact-bounced (i.e., during a power cut), the RTC system and coin cell maintained logic will switch over to the LICELL for backup power. This switch over occurs for a BP below the UVDET threshold with LICELL greater than BP. A small capacitor should be placed from LICELL to ground under all circumstances.

Upon initial insertion of the coincell, it is not immediately connected to the on chip circuitry. The cell gets connected when the IC powers on, or after enabling the coincell charger when the IC was already on. During operation, coincells can get damaged and their lifetime reduced when deeply discharged. In order to avoid such, the internal circuitry supplied from LICELL is automatically disconnected for voltages below the coincell disconnect threshold. The cell gets reconnected again under the same conditions as for initial insertion.

The coin cell charger circuit will function as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHEN bit. The coin cell voltage is programmable through the VCOIN[2:0] bits. The coin cell charger voltage is programmable in the ON state where the charge current is fixed at ICOINHI.

If COINCHEN=1 when the system goes into Off or User Off state, the coin cell charger will continue to charge to the predefined voltage setting but at a lower maximum current ICOINLO. This compensates for self discharge of the coin cell and ensures that if/when the main cell gets depleted, that the coin cell will be topped off for maximum RTC retention. The coin cell charging will be stopped for the BP below UVDET. The bit COINCHEN itself is only cleared when an RTCPORB occurs.

Table 20. Coin cell Charger Voltage Specifications

VCOIN[2:0]	Output Voltage
000	2.50
001	2.70
010	2.80
011	2.90
100	3.00
101	3.10
110	3.20
111	3.30

Table 21. Coin cell Charger Specifications

Parameter	Typ	Units
Voltage Accuracy	100	mV
Coin Cell Charge Current in On and Watchdog modes ICOINHI	60	µA
Coin Cell Charge Current in Off and Low-power Off modes (User Off / Memory Hold) ICOINLO	10	µA
Current Accuracy	30	%
LICELL Bypass Capacitor	100	nF
LICELL Bypass Capacitor as coin cell replacement	4.7	µF
LICELL Bypass Capacitor	100	nF
LICELL Bypass Capacitor as coin cell replacement	4.7	µF

POWER CONTROL SYSTEM

INTERFACE

The power control system on the MC13892 interfaces with the processor via different IO signals and the SPI/I2C bus. It also uses on chip signals and detector outputs. Table 22 gives a listing of the principal elements of this interface.

Table 22. Power Control System Interface Signals

Name	Type of Signal	Function
PWRON1	Input pin	Power on/off 1 button connection
PWRON2	Input pin	Power on/off 2 button connection
PWRON3	Input pin	Power on/off 3 button connection
PWRONxI/M/S	SPI bits	PWRONx pin interrupt /mask / sense bits
PWRON1DBNC[1:0]	SPI bits	Sets time for the PWRON1 pin hardware debounce
PWRON2DBNC[1:0]	SPI bits	Sets time for the PWRON2 pin hardware debounce
PWRON3DBNC[1:0]	SPI bits	Sets time for the PWRON3 pin hardware debounce
PWRON1RSTEN	SPI bit	Allows for system reset through the PWRON1 pin
PWRON2RSTEN	SPI bit	Allows for system reset through the PWRON2 pin
PWRON3RSTEN	SPI bit	Allows for system reset through the PWRON3 pin
RESTARTEN	SPI bit	Allows for system restart after a PWRON initiated system reset
SYSRSTI/M	SPI bits	PWRONx System restart interrupt / mask bits
WDI	Input pin	Watchdog input has to be kept high by the processor to keep the MC13892 active
WDIRESET	SPI bit	Allows for system restart through the WDI pin
WDIRESETI/M	SPI bits	WDI System restart interrupt / mask bits
RESET	Output pin	Reset Bar output (active low) to the application. Requires an external pull-up
RESETMCU	Output pin	Reset Bar output (active low) to the processor core. Requires an external pull-up
PUMS1	Input pin	Switchers and regulators power up sequence and defaults selection 1
PUMS2	Input pin	Switchers and regulators power up sequence and defaults selection 2
STANDBY	Input pin	Signal from primary processor to put the MC13892 in a Low-power mode
STANDBYINV	SPI bit	Standby signal polarity setting
STANDBYSEC	Input pin	Signal from secondary processor to put the MC13892 in a Low-power mode
STANDBYSECINV	SPI bit	Secondary standby signal polarity setting
STBYDLY[1:0]	SPI bits	Sets delay before entering standby mode
BPON	Threshold	Threshold validating turn on events
BPONI/M/S	SPI bits	BP turn on threshold interrupt / mask / sense bits
LOBATH	Threshold	Threshold for a low battery warning
LOBATHI/M/S	SPI bits	Low battery warning interrupt / mask / sense bits
LOBATL	Threshold	Threshold for a low battery detect
LOBATLI/M/S	SPI bits	Low battery detect interrupt / mask / sense bits
BPSNS [1:0]	SPI bits	Selects for different settings of LOBATL and LOBATH thresholds
UVDET	Threshold	Threshold for under-voltage detection, will shut down the device
LICELL	Input pin	Connection for Lithium based coin cell
CLK32KMCU	Output pin	Low frequency system clock output for the processor 32.768 kHz
CLK32K	Output pin	Low frequency system clock output for application (peripherals) 32.768 kHz
CLK32KMCUEN	SPI bit	Enables the CLK32KMCU clock output
DRM	SPI bit	Keeps VSRTC and CLK32KMCU active in all states for digital rights management, including off mode
PCEN	SPI bit	Enables power cut support
PCI/M	SPI bits	Power cut detect interrupt / mask bits
PCT[7:0]	SPI bits	Allowed power cut duration
PCCOUNTEN	SPI bit	Enables power cut counter
PCCOUNT[3:0]	SPI bits	Power cut counter

Table 22. Power Control System Interface Signals

Name	Type of Signal	Function
PCMAXCNT[3:0]	SPI bits	Maximum number of allowed power cuts
PCUTEXPB	SPI bit	Indicates a power cut timer counter expired

OPERATING MODES

POWER CONTROL STATE MACHINE

Figure 11 shows the flow of the power control state machine. This diagram serves as the basis for the description in the remainder of this chapter.

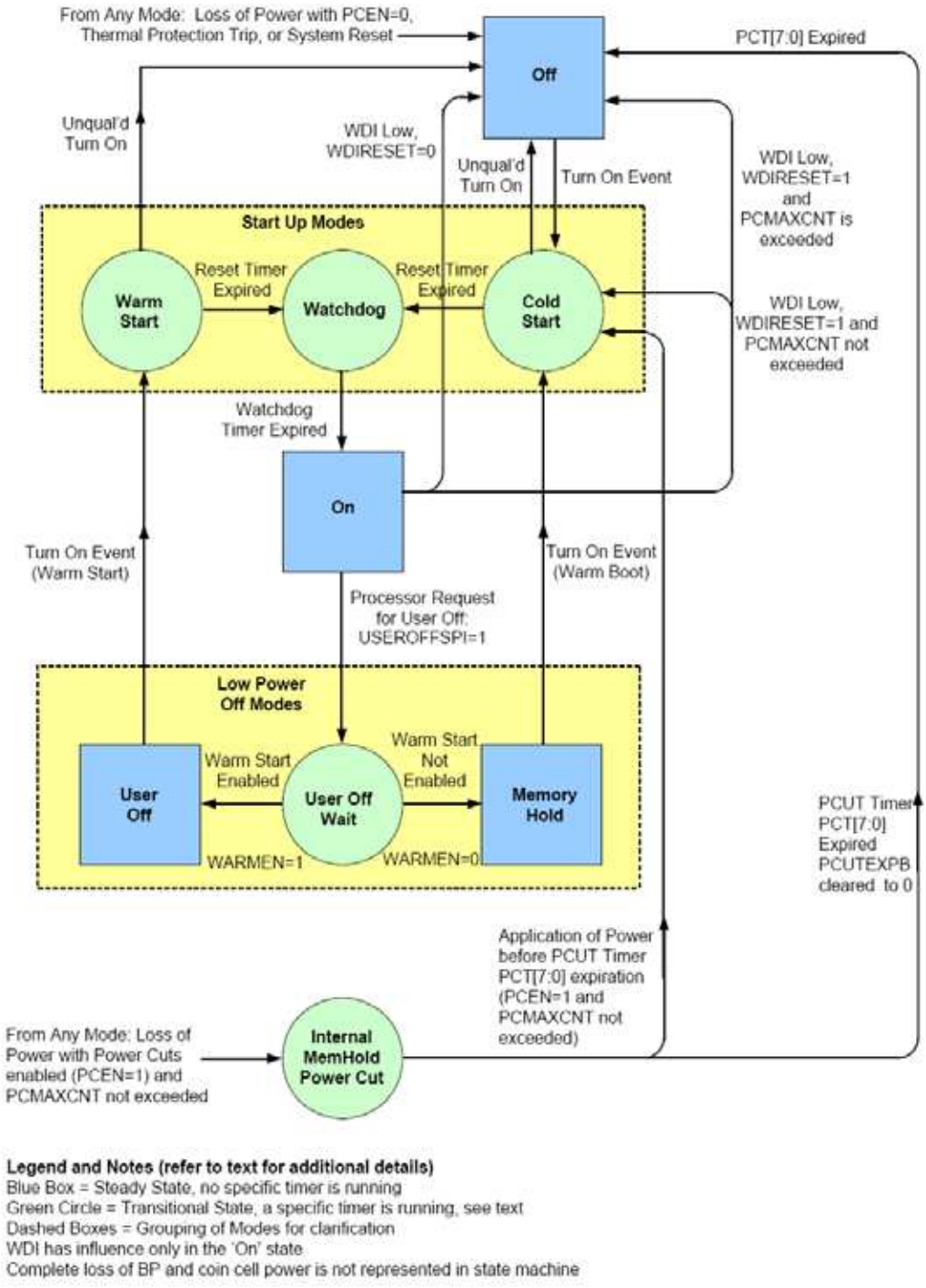


Figure 11. Power Control State Machine Flow Diagram

POWER CONTROL MODES DESCRIPTION

Following are text descriptions of the power states of the system, which give additional details of the state machine, and complement Figure 11. Note that the SPI control is only possible in the Watchdog, On, and User Off Wait states, and that the interrupt line INT is kept low in all states except for Watchdog and On.

Off

If the supply at BP is above the UVDET threshold, only the IC core circuitry at VCOREDIG and the RTC module are powered, all other supplies are inactive. To exit the Off mode, a valid turn on event is required. No specific timer is running in this mode.

If the supply at BP is below the UVDET threshold no turn on events are accepted. If a valid coin cell is present, the core gets powered from LICELL. The only active circuitry is the RTC module, with BP greater than UVDET detection, and the SRTC support circuitry, if so configured.

Cold Start

Entered upon a Turn On event from Off, Warm Boot, successful PCUT, or Silent System Restart. The switchers and regulators are powered up sequentially to limit the inrush current. See the Power Up section for sequencing and default level details. The reset signals RESETB and RESETBMCU are kept low. The Reset timer starts running when entering a Cold Start. When expired, the Cold Start state is exited for the Watchdog state, and both RESETB and RESETBMCU become high (open drain output with external pull ups). The input control pins WDI, and STANDBYx are ignored.

Watchdog

The system is fully powered and under SPI control. RESETB and RESETBMCU are high. The Watchdog timer starts running when entering the Watchdog state. When expired, the system transitions to the On state, where WDI will be checked and monitored. The input control pins WDI and STANDBYx are ignored while in the Watchdog state.

On

The system is fully powered and under SPI control. RESETB and RESETBMCU are high. The WDI pin must be high to stay in this mode. The WDI IO supply voltage is referenced to SPIVCC (Normally connected to SW4). SPIVCC must therefore remain enabled to allow for proper WDI detection. If WDI goes low, the system will transition to the Off state or Cold Start (depending on the configuration. Refer to the section on Silent System Restart with WDI Event for details).

User Off Wait

The system is fully powered and under SPI control. The WDI pin no longer has control over the part. The Wait mode is entered by a processor request for User Off by setting the USEROFFSPI bit high. This is normally initiated by the end user via the power key. Upon receiving the corresponding interrupt, the system will determine if the product has been configured for User Off or Memory Hold states (both of which first require passing through User Off Wait) or just transition to Off.

The Wait timer starts running when entering User Off Wait mode. This leaves the processor time to suspend or terminate its tasks. When expired, the Wait mode is exited for User Off mode or Memory Hold mode, depending on warm starts being enabled or not via the WARMEN bit. The USEROFFSPI bit is being reset at this point by RESETB going low.

Memory Hold and User Off (Low-power Off states)

As noted in the User Off Wait description, the system is directed into Low-power Off states based on a SPI command in response to an intentional turn off by the end user. The only exit then will be a turn on event. To an end user, the Memory Hold and User Off states look like the product has been shut down completely. However, a faster startup is facilitated by maintaining external memory in self-refresh mode (Memory Hold and User Off mode) as well as powering portions of the processor core for state retention (User Off only). The switcher mode control bits allow selective powering of the buck regulators for optimizing the supply behavior in the Low-power Off modes. Linear regulators and most functional blocks are disabled (the RTC module, and Turn On event detection are maintained).

Memory Hold

RESETB and RESETBMCU are low, and both CLK32K and CLK32KMCU are disabled. If DRM is set, the CLK32KMCU is kept active. To ensure that SW1, SW2, and SW3 shut off in Memory Hold, appropriate mode settings should be used such as SW1MHMODE = SW2MHMODE = SW3MHMODE = 0 (refer to the mode control description later in this chapter). Since SW4 should be powered in PFM mode, SW4MHMODE could be set to 1.

Any peripheral loading on SW4 should be isolated from the SW4 output node by the PWGT2 switch, which opens in both Low-power off modes due to the RESETB transition. In this way, leakage is minimized from the power domain maintaining the memory subsystem.

Upon a Turn On event, the Cold Start state is entered, the default power up values are loaded, and an the MEMHLDI interrupt bit is set. A Cold Start out of the Memory Hold state will result in shorter boot times compared to starting out of the Off state, since software does not have to be loaded and expanded from flash. The startup out of Memory Hold is also referred to as Warm Boot. No specific timer is running in this mode.

Buck regulators that are configured to stay on in MEMHOLD mode by their SWxMHMODE settings will not be turned off when coming out of MEMHOLD and entering a Warm Boot. The switchers will be reconfigured for their default settings as selected by the PUMS pin in the normal time slot that would affect them.

User Off

RESETB is low and RESETBMCU is kept high. The 32 kHz peripheral clock driver CLK32K is disabled. CLK32KMCU (connected to the processor's CKIL input) is maintained in this mode if the CLK32KMCUEN and USEROFFCLK bits are both set, or if DRM is set.

The memory domain is held up by setting SW4UOMODE = 1. Similarly, the SW1, and/or SW2, and/or SW3 supply domains can be configured for SWxUOMODE = 1 to keep them powered through the User Off event. If one of the switchers can be shut down on in User Off, its mode bits would typically be set to 0.

Any peripheral loading on SW1 and/or SW2 should be isolated from the output node(s) by the PWGT1 switch, which opens in both Low-power Off modes due to the RESETB transition. In this way, leakage is minimized from the power domain maintaining the processor core.

Since power is maintained for the core (which is put into its lowest power state) and since MCU RESETBMCU does not trip, the processor's state may be quickly recovered when exiting USEROFF upon a turn on event. The CLK32KMCU clock can be used for very low frequency / low-power idling of the core(s), minimizing battery drain while allowing a rapid recovery from where the system left off before the USEROFF command.

Upon a turn on event, Warm Start state is entered, and the default power up values are loaded. A Warm Start out of User Off will result in an almost instantaneous startup of the system, since the internal states of the processor were preserved along with external memory. No specific timer is running in this mode.

Warm Start

Entered upon a Turn On event from User Off. The switchers and regulators are powered up sequentially to limit the inrush current; see the Power Up section for sequencing and default level details. If SW1, SW2, SW3, and/or SW4 were configured to stay on in User Off mode, they will not be turned off when coming out of User Off and entering a Warm Start. The buck regulators will be reconfigured for their default settings as selected by the PUMS pin in the respective time slot defined in the sequencer selection.

RESETB is kept low and RESETBMCU is kept high. CLK32KMCU is kept active if enabled via the SPI. The reset timer starts running when entering Warm Start. When expired, the Warm Start state is exited for the Watchdog state, a WARMI interrupt is generated, and RESETB will go high.

Internal MemHold Power Cut

Refer to the next section for details about Power Cuts and the associated state machine response.

POWER CUT DESCRIPTION

When the supply at BP drops below the UVDET threshold due to battery bounce or battery removal, the Internal MemHold Power Cut mode is entered and a Power Cut (PCUT) timer starts running. The backup coin cell will now supply the RTC as well as the on chip memory registers and some other power control related bits. All other supplies will be disabled.

The maximum duration of a power cut is determined by the PCUT timer PCT[7:0] preset via SPI. When a PCUT occurs, the PCUT timer will internally be decremented till it expires, meaning counted down to zero. The contents of PCT[7:0] does not reflect the actual count down value but will keep the programmed value and therefore does not have to be reprogrammed after each power cut.

If power is not reestablished above BPON before the PCUT timer expires, the state machine transitions to the Off mode at expiration of the counter, and clears the PCUTEXB bit by setting it to 0. This transition is referred to as an “unsuccessful” PCUT.

Upon re-application of power before expiration (an “successful PCUT”, defined as BP first rising above the UVDET threshold and then above the BPON threshold before the PCUT timer expires), a Cold Start is engaged.

In order to distinguish a non-PCUT initiated Cold Start from a Cold Start after a PCUT, the PCI interrupt should be checked by software. The PCI interrupt is cleared by software or when cycling through the Off state.

Because the PCUT system quickly disables all of the power tree, the battery voltage may recover to a level with the appearance of a valid supply once the battery is unloaded. However, upon a restart of the IC and power sequencer, the surge of current through the battery and trace impedances can once again cause the BP node to drop below UVDET. This chain of cyclic power down / power up sequences is referred to as “ambulance mode”, and the power control system includes strategies to minimize the chance of a product falling into and getting stuck in ambulance mode.

First, the successful recovery out of a PCUT requires the BP node to rise above BPON, providing hysteretic margin from the UVDET threshold. Secondly, the number of times the PCUT mode is entered is counted with the counter PCCOUNT[3:0], and the allowed count is limited to PCMAXCNT[3:0] set through the SPI. When the contents of both become equal, then the next PCUT will not be supported and the system will go to Off mode.

After a successful power up after a PCUT (i.e., valid power is reestablished, the system comes out of reset, and the processor reassumes control), software should clear the PCCOUNT[3:0] counter. Counting of PCUT events is enabled via the PCCOUNTEN bit. This mode is only supported if the power cut mode feature is enabled by setting the PCEN bit. When not enabled, in case of a power failure, the state machine will transition to the Off state. SPI control is not possible during a PCUT event and the interrupt line is kept low. SPI configuration for PCUT support should also include setting the PCUTEXPB=1 (see the Silent Restart from PCUT Event section later in this chapter).

Internal MemHold Power Cut

As described above, a momentary power interruption will put the system into the Internal MemHold Power Cut state if PCUTs are enabled. The backup coin cell will now supply the MC13892 core along with the 32 kHz crystal oscillator, the RTC system and coin cell backed up registers. All regulators and switchers will be shut down to preserve the coin cell and RTC as long as possible.

Both RESETB and RESETBMCU are tripped, bringing the entire system down along with the supplies and external clock drivers, so the only recovery out of a Power Cut state is to reestablish power and initiate a Cold Start.

If the PCT timer expires before power is reestablished, the system transitions to the Off state and awaits a sufficient supply recovery.

SILENT RESTART FROM PCUT EVENT

If a short duration power cut event occurs (such as from a battery bounce, for example), it may be desirable to perform a silent restart, so the system is re-initialized without alerting the user. This can be configured by setting the PCUTEXPB bit to a “1” at booting or after a Cold Start. This bit resets on RTCPORB, therefore any subsequent Cold Start can first check the status of PCUTEXPB and the PCI bit. The PCUTEXPB is cleared to “0” when transitioning from PCUT to Off. If there was a PCUT interrupt and PCUTEXPB is still a “1”, then the state machine has not transitioned through Off, which confirms that the PCT timer has not expired during the PCUT event (i.e., a successful power cut). In case of a successful power cut, a silent restart may be appropriate.

If PCUTEXPB is found to be a “0” after the Cold Start where PCI is found to be a “1”, then it is inferred that the PCT timer has expired before power was reestablished, flagging an unsuccessful power cut or first power up, so the startup user greeting may be desirable for playback.

SILENT SYSTEM RESTART WITH WDI EVENT

A mechanism is provided for recovery if the system software somehow gets into an abnormal state which requires a system reset, but it is desired to make the reset a silent event so as to happen without end user awareness. The default response to WDI going low is for the state machine to transition to the Off state (when WDIRESET = 0). However, if WDIRESET = 1, the state machine will go to Cold Start without passing through Off mode

A WDIRESET event will generate a maskable WDIRESETI interrupt and also increment the PCCOUNT counter. This function is unrelated to PCUTs, but it shares the PCUT counter so that the number of silent system restarts can be limited by the programmable PCMAXCNT counter.

When PCUT support is used, the software should set the PCUTEXPB bit to “1”. Since this bit resets with RTCPORB, it will not be reset to “0” if a WDI falls and the state machine goes straight to the Cold Start state. Therefore, upon a restart, the software can detect a silent system restart, if there is a WDIRESETI interrupt and PCUTEXPB = 1. The application may then determine that an inconspicuous restart without showing may be more appropriate than launching into the welcoming routine.

A PCUT event does not trip the WDIRESETI bit.

GLOBAL SYSTEM RESTART

A global system reset can be enabled through the GLBRSTENB SPI bit. The global reset on the MC13892A/C versions is active low so it is enabled when the GLBRSTENB = 0. In the MC13892B/D versions global reset is active high and it is enabled when the GLBRSTENB = 1. When global reset is enabled and the PWRON3 button is held for 12 seconds, the system will reset and the following actions will take place:

- Power down
- Disable the charger
- Reset all the registers including the RTCPORB registers
- Power back up after the difference between the 12sec timer, and when the user releases the button as the power off time (for example, if the power button was held for 12.1 s, then the time that the IC would be off would be only 100 mS)

If PWRON3 is held low for less than 12 seconds, it will act as a normal PWRON pin. This feature is enabled by default in the MC13892A/C versions, and disabled by default in the MC13892B/D versions.

CLK32KMCU CLOCK DRIVER CONTROL THROUGH STATES

As described previously, the clocking behavior is influenced by the state machine is in and the setting of the clocking related SPI bits. A summary is given in Table 23 for the clock output CLK32KMCU.

Table 23. CLK32MCU Control Logic Table

Mode	DRM	CLK32KMCUEN	USEROFFCLK	Clock Output CLK32KMCU
Off, Memory Hold, Internal MEMHOLD PCUT	0	X	X	Disabled
	1	X	X	Enabled
On, Cold Start, Warm Start, Watchdog, User Off Wait	0	0	X	Disabled
	1	X	X	Enabled
	0	1	X	Enabled
User Off	0	X	0	Disabled
	1	X	X	Enabled
	0	1	1	

TURN ON EVENTS

When in Off mode, the MC13892 can be powered on via a Turn On event. The Turn On events are listed in Table 24. To indicate to the processor what event caused the system to power on, an interrupt bit is associated with each of the Turn On events. Masking the interrupts related to the turn on events will not prevent the part to turn on, except for the time of day alarm.

Power Button Press

PWRON1, PWRON2, or PWRON3 pulled low with corresponding interrupts and sense bits PWRON1I, PWRON2I, or PWRON3I, and PWRON1S, PWRON2S, or PWRON3S. A power on/off button is connected here. The PWRONx can be hardware debounced through a programmable debouncer PWRONxDBNC[1:0] to avoid the application to power up upon a very short key press. In addition, a software debounce can be applied. BP should be above UVDET. The PWRONxI interrupt is generated for both the falling and the rising edge of the PWRONx pin. By default, a 30 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with PWRONxDBNC[1:0] as defined in the following table. The PWRONxI interrupt is cleared by software or when cycling through the Off mode.

Table 24. PWRONx Hardware Debounce Bit Settings

Bits	State	Turn On Debounce (ms)	Falling Edge INT Debounce (ms)	Rising Edge INT Debounce (ms)
PWRONxDBNC[1:0]	00	0	31.25	31.25
	01	31.25	31.25	31.25
	10	125	125	31.25
	11	750	750	31.25

Notes
48. The sense bit PWRONxS is not debounced and follows the state of the PWRONx pin

Charger Attach

CHRGRAW is pulled high with corresponding interrupt and sense bits CHGDETI and CHGDETS. This is equivalent to plugging in a charger. BP should be above BPON. The charger turn on event is dependent on the charge mode selected. For details on the charger detection and turn on, see Battery Interface and Control.

Battery Attach

BP crossing the BPON threshold which corresponds to attaching a charged battery to the product. A corresponding BPONI interrupt is generated, which can be cleared by software or when cycling through the Off mode. Note that BPONI is also generated after a successful power cut and potentially when applying a charger.

USB Attach

VBUS pulled high with corresponding interrupt and sense bits BVALIDI and BVALIDS. This is equivalent to plugging in a USB cable. BP should be above BPON and the battery voltage above BATTON. For details on the USB detection, see Connectivity.

RTC Alarm

TOD and DAY become equal to the alarm setting programmed. This allows powering up a product at a preset time. BP should be above BPON. For details and related interrupts, see Clock Generation and Real Time Clock.

System Restart

System restart may occur after a system reset. This is an optional function, see also the following Turn Off events section. BP should be above BPON.

TURN OFF EVENTS

Power Button Press

User shut down of a product is typically done by pressing the power button connected to the PWRONx pin. This will generate an interrupt (PWRONxI), but will not directly power off the part. The product is powered off by the processor's response to this interrupt, which will be to pull WDI low. Pressing the power button is therefore under normal circumstances not considered as a turn off event for the state machine.

Note that software can configure a user initiated power down via a power button press for transition to a Low-power off mode (Memory Hold or User Off) for a quicker restart than the default transition into the Off state.

Power Button System Reset

A secondary application of the PWRON pin is the option to generate a system reset. This is recognized as a Turn Off event. By default, the system reset function is disabled but can be enabled by setting the PWRONxRSTEN bits. When enabled, a 4 second long press on the power button will cause the device to go to the Off mode and as a result the entire application will power down. An SYSRSTI interrupt is generated upon the next power up. Alternatively, the system can be configured to restart automatically by setting the RESTARTEN bit.

Thermal Protection

If the die gets overheated, the thermal protection will power off the part to avoid damage. A Turn On event will not be accepted while the thermal protection is still being tripped. The part will remain in Off mode until cooling sufficiently to accept a Turn On event. There are no specific interrupts related to this other than the warning interrupts.

Under-Voltage Detection

When the voltage at BP drops below the under-voltage detection threshold UVDET, the state machine will transition to Off mode if PCUT is not enabled, or if the PCT timer expires when PCUT is enabled.

TIMERS

The different timers as used by the state machine are in Table 25. This listing does not include RTC timers for timekeeping. A synchronization error of up to one clock period may occur with respect to the occurrence of an asynchronous event. The duration listed below is therefore the effective minimum time period.

Table 25. Timer Main Characteristics

Timer	Duration
Under-voltage Timer	4.0 ms
Reset Timer	40 ms
Watchdog Timer	128 ms
Power Cut Timer	Programmable 0 to 8 seconds in 31.25 ms steps

TIMING DIAGRAMS

A Turn On event timing diagram example shows in Figure 12.

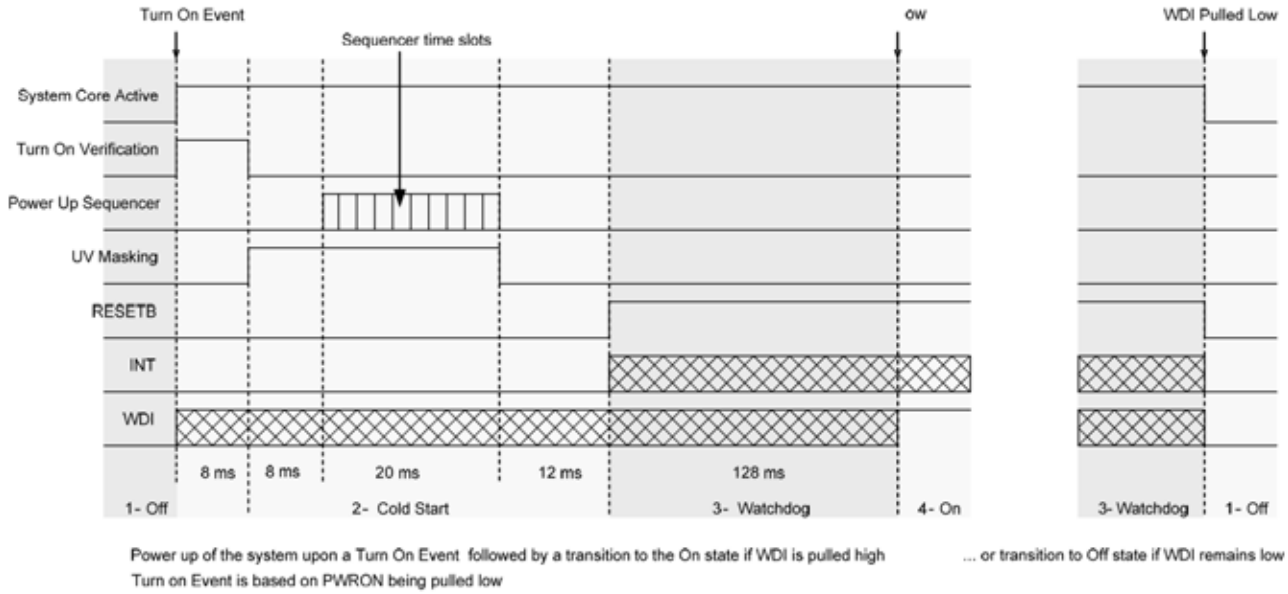


Figure 12. Power Up Timing Diagram

POWER UP

At power up, switchers and regulators are sequentially enabled in time slots of 2.0 ms steps to limit the inrush current after an initial delay of 8.0 ms, in which the core circuitry gets enabled. To ensure a proper power up sequence, the outputs of the switchers are discharged at the beginning of a Cold Start. For that reason, an 8.0 ms delay allows the outputs of the linear regulators to be fully discharged as well through the built-in discharge path. Time slots which include multiple regulator startups will be sub-sequenced for additional inrush balancing. The peak inrush current per event is limited. Any under-voltage detection at BP is masked while the power up sequencer is running.

The Power Up mode Select pins (PUMS1 and 2) are used to configure the startup characteristics of the regulators. Supply enabling and output level options are selected by hardwiring the PUMSx pins for the desired configuration. The state of the PUMSx pins can be read out via the sense bits PUMSSxx[1:0]. Tying the PUMSx pins to ground corresponds to 00, open to 01, VCOREDIG to 10, and VCORE to 11.

The recommended power up strategy for end products is to bring up as little of the system as possible at booting, essentially sequestering just the bare essentials, to allow processor startup and software to run. With such a strategy, the startup transients are controlled at lower levels, and the rest of the system power tree can be brought up by software. This allows optimization of supply ordering where specific sequences may be required, as well as supply default values. Software code can load up all of the required programmable options to avoid sneak paths, under/over-voltage issues, startup surges, etc., without any change in hardware. For this reason, the Power Gate drivers are limited to activation by software rather than the sequencer, allowing the core(s) to startup before any peripheral loading is introduced.

The power up defaults Table 26 shows the initial setup for the voltage level of the switchers and regulators, and whether they get enabled.

Table 26. Power Up Defaults Table

i.MX	37/51	37/51	37/51	37/51	35	27/31
PUMS1	**GND**	**Open**	**VCOREDIG**	**VCORE**	**GND**	**Open**
PUMS2	**Open**	**Open**	**Open**	**Open**	**GND**	**GND**
SW1 (49)	0.775	1.050	1.050	0.775	1.200	1.200
SW2 (49)	1.025	1.225	1.225	1.025	1.350	1.450
SW3 (49)	1.200	1.200	1.200	1.200	1.800	1.800
SW4 (49)	1.800	1.800	1.800	1.800	1.800	1.800
SWBST	Off	Off	Off	Off	5.000	5.000
VUSB	3.300 (50)	3.300 (50)	3.300 (50)	3.300 (50)	3.300 (52)	3.300 (52)
VUSB2	2.600	2.600	2.600	2.600	2.600	2.600
VPLL	1.800	1.800	1.800	1.800	1.500	1.500
VDIG	1.250	1.250	1.250	1.250	1.250	1.250
VIOHI	2.775	2.775	2.775	2.775	2.775	2.775
VGEN2	3.150	Off	3.150	Off	3.150	3.150
VSD	Off	Off	Off	Off	3.150	3.150

Notes
49. The switchers SWx are activated in PWM pulse skipping mode, but allowed when enabled by the startup sequencer.
50. USB supply VUSB, is only enabled if 5.0 V is present on UVBUS.
51. The following supplies are not included in the matrix since they are not intended for activation by the startup sequencer: VCAM, VGEN1, VGEN3, VVIDEO, and VAUDIO
52. SWBST = 5.0 V powers up and does VUSB regardless of 5.0 V present on UVBUS. By default VUSB will be supplied by SWBST.

The power up sequence is shown in Table 27. VCOREDIG, VSRTC, and VCORE are brought up in the pre-sequencer startup. Once VCOREDIG is activated (i.e., at the first-time power application), it will be continuously powered as long as a valid coin cell is present.

Table 27. Power Up Sequence

Tap x 2ms	PUMS2 = Open (i.MX37, i.MX51)	PUMS2 = GND (i.MX35, i.MX27)
0	SW2	SW2
1	SW4	VGEN2
2	VIOHI	SW4
3	VGEN2	VIOHI, VSD
4	SW1	SWBST, VUSB (56)
5	SW3	SW1
6	VPLL	VPLL
7	VDIG	SW3
8	-	VDIG
9	VUSB (55), VUSB2	VUSB2

Notes
53. Time slots may be included for blocks which are defined by the PUMS pin as disabled to allow for potential activation.
54. The following supplies are not included in the matrix since they are not intended for activation by the startup sequencer: VCAM, VGEN1, VGEN3, VVIDEO, and VAUDIO. SWBST is not included on the PUMS2 = Open column.
55. USB supply VUSB, is only enabled if 5.0 V is present on UVBUS.
56. SWBST = 5.0 V powers up and so does VUSB regardless of 5.0 V present on UVBUS. By default VUSB will be supplied by SWBST.

POWER MONITORING

The voltage at BPSNS and BP is monitored by detectors as summarized in Table 28.

Table 28. BP Detection Thresholds

		Threshold in V			
Bit setting		**Falling Edge**			**Rising Edge**
BPSNS1	**BPSNS0**	**UVDET**	**LOBATL**	**LOBATH**	**BPON**
0	0	2.55	2.8	3.0	3.2
0	1	2.55	2.9	3.1	3.2
1	0	2.55	3.0	3.3	3.2
1	1	2.55	3.1	3.4	3.2

Notes

57. Default setting for BPSNS[1:0] is 00. The above specified thresholds are ±50 mV accurate for the indicated edge. A hysteresis is applied to the detectors on the order of 100 mV. BPON is monitoring BP. UVDET, LOBATL and LOBATH are monitoring BPSNS and thresholds are correlated.

The UVDET and BPON thresholds are related to the power on/off events as described earlier in this chapter. The LOBATH threshold is used as a weak battery warning. An interrupt LOBATHI is generated when crossing the threshold (dual edge). The LOBATL threshold is used as a low battery detect. An interrupt LOBATLI is generated when dropping below the threshold. The sense bits are coded in line with previous generation parts.

Table 29. Power Monitoring Summary

BPSNS	BPONS	LOBATHS	LOBATLS
< LOBATL	0	0	1
LOBATL-LOBATH	0	0	0
LOBATH-BPON	0	1	0
>BPON	1	1	0

POWER SAVING

SYSTEM STANDBY

A product may be designed to go into DSM after periods of inactivity, such as if a music player completes a play list and no further activity is detected, or if a gaming interface sits idle for an extended period. Two Standby pins are provided for board level control of timing in and out of such deep sleep modes.

When a product is in DSM it may be able to reduce the overall platform current by lowering the switcher output voltage, disabling some regulators, or forcing some GPO low. This can be obtained by SPI configuration of the Standby response of the circuits along with control of the Standby pins.

To ensure that shared resources are properly powered when required, the system will only be allowed into Standby when both the STANDBY and the STANDBYSEC are activated. The states of the Standby pins only have influence in On mode. A command to transition to one of the Low-power Off states (User Off or Memory Hold, initiated with USEROFFSPI = 1) has priority over Standby.

Note that the Standby pins are programmable for Active High or Active Low polarity, and that decoding of a Standby event will take into account the programmed input polarities associated with each pin.

Table 30. Standby Pin and Polarity Control

STANDBY (Pin)	STANDBYINV (SPI bit)	STANDBYSEC (Pin)	STANDBYSECINV (SPI bit)	STANDBY Control [58]
0	0	x	x	0
x	x	0	0	0
1	1	x	x	0
x	x	1	1	0
0	1	0	1	1

Table 30. Standby Pin and Polarity Control

STANDBY (Pin)	STANDBYINV (SPI bit)	STANDBYSEC (Pin)	STANDBYSECINV (SPI bit)	STANDBY Control [58]
0	1	1	0	1
1	0	0	1	1
1	0	1	0	1

Notes
58. STANDBY = 0: System is not in Standby; STANDBY = 1: System is in Standby and Standby programmability is activated.

When requesting standby, a programmable delay (STBYDLY) of 0 to 3 clock cycles of the 32 kHz clock is applied before actually going into standby (i.e. before turning off some supplies). No delay is applied when coming out of standby.

Table 31. Delay of STANDBY- Initiated Response

STBYDLY[1:0]	Function (1)
00	No Delay
01	One 32 K period (default)
10	Two 32 K periods
11	Three 32 K periods

REGULATOR MODE CONTROL

The regulators with embedded pass devices (VDIG, VPLL, VIOHI, VUSB, VUSB2, and VAUDIO) have an adaptive biasing scheme, thus, there are no distinct operating modes such as a Normal mode and a Low-power mode. Therefore, no specific control is required to put these regulators in a Low-power mode.

The regulators with external pass devices (VSD, VVIDEO, VGEN1, and VGEN2) can also operate in a Normal and Low-power mode. However, since a load current detection cannot be performed for these regulators, the transition between both modes is not automatic and is controlled by setting the corresponding mode bits for the operational behavior desired.

The regulators VGEN3 and VCAM can be configured for using the internal pass device or external pass device as explained in Power Control System. For both configurations, the transition between Normal and Low-power modes is controlled by setting the VxMODE bit for the specific regulator. Therefore, depending on the configuration selected, the automatic Low-power mode is available.

The regulators can be disabled and the general purpose outputs can be forced low when going into Standby as described previously. Each regulator and GPO has an associated SPI bit for this. When the bit is not set, STANDBY is of no influence. The actual operating mode of the regulators as a function of STANDBY is not reflected through the SPI. In other words, the SPI will read back what is programmed, not the actual state.

Table 32. LDO Regulator Control (External Pass Device LDOs)

VxEN	VxMODE	VxSTBY	STANDBY	Regulator Vx
0	X	X	X	Off
1	0	0	X	On
1	1	0	X	Low-power
1	X	1	0	On
1	0	1	1	Off
1	1	1	1	Low-power

Notes
59. This table is valid for regulators with an external pass device
60. STANDBY refers to a Standby event as described earlier

For regulators with internal pass devices and general outputs, the previous table can be simplified.

Table 33. LDO Regulator Control (Internal Pass Device LDOs)

VxEN	VxSTBY	STANDBY	Regulator Vx
0	X	X	Off
1	0	X	On
1	1	0	On
1	1	1	Off

Notes
61. This table is valid for regulators with an internal pass device
62. STANDBY refers to a Standby event as described earlier

BUCK REGULATORS

Operational modes of the Buck regulators can be controlled by direct SPI programming, altered by the state of the STANDBY pins, by direct state machine influence, or by load current magnitude when so configured. Available modes include PWM with No Pulse Skipping (PWM), PWM with Pulse Skipping (PWMPS), Pulse Frequency Mode (PFM), and Off. The transition between the two modes PWMPS and PFM can occur automatically, based on the load current. Therefore, no specific control is required to put the switchers in a Low-power mode. When the buck regulators are not configured in the Auto mode, power savings may be achieved by disabling switchers when not needed, or running them in PFM mode if loading conditions are light enough.

SW1, SW2, SW3, and SW4 can be configured for mode switching with STANDBY or autonomously based on load current with adaptive mode control (Auto). Additionally, provisions are made for maintaining PFM operation in USEROFF and MEMHOLD modes to support state retention for faster startup from the Low-power Off modes for Warm Start or Warm Boot.

Table 34 summarizes the Buck regulator programmability for Normal and Standby modes.

Table 34. Switcher Mode Control for Normal and Standby Operation

SWxMODE[3:0]	Normal mode(63)	Standby Mode(63)
0000	Off	Off
0001	PWM	Off
0010	PWMPS	Off
0011	PFM	Off
0100	Auto	Off
0101	PWM	PWM
0110	PWM	Auto
0111	NA	NA
1000	Auto	Auto
1001	PWM	PWMPS
1010	PWMPS	PWMPS
1011	PWMPS	Auto
1100	Auto	PFM
1101	PWM	PFM
1110	PWMPS	PFM
1111	PFM	PFM

Notes
63. STANDBY defined as logical AND of STANDBY and STANDBYSEC pin

In addition to controlling the operating mode in Standby, the voltage setting can be changed. The transition in voltage is handled in a controlled slope manner, see Supplies, for details. Each switcher has an associated set of SPI bits for Standby mode set points. By default the Standby settings are identical to the non-Standby settings, which are initially defined by PUMS programming.

The actual operating mode of the switchers as a function of STANDBY pins is not reflected through the SPI. The SPI will read back what is programmed in SWxMODE[3:0], not the actual state that may be altered as described previously.

Table 35 and Table 36 show the switcher mode control in the Low-power Off states. Note that a Low-power Off activated SWx should use the Standby set point as programmed by SWxSTBY[4:0]. The activated switcher(s) will maintain settings for mode and voltage until the next startup event. When the respective time slot of the startup sequencer is reached for a given switcher, its mode and voltage settings will be updated the same as if starting out of the Off state (except that switchers active through a Low-power Off mode will not be off when the startup sequencer is started).

Table 35. Switcher Control In Memory Hold

SWxMHMODE	Memory Hold Operational Mode (64)
0	Off
1	PFM

Notes

64. For Memory Hold mode, an activated SWx should use the Standby set point as programmed by SWxSTBY[4:0].

Table 36. Switcher Control In User Off

SWxUOMODE	User Off Operational Mode (65)
0	Off
1	PFM

Notes

65. For User Off mode, an activated SWx should use the Standby set point as programmed by SWxSTBY[4:0].

POWER GATING SYSTEM

The Low-power Off states are provided to allow faster system booting from two pseudo Off conditions: Memory Hold, which keeps the external memory powered for self refresh, and User Off, which keeps the processor powered up for state retention. For reduced current drain in Low-power Off states, parts of the system can benefit from power gating to isolate the minimum essentials for such operational modes. It is also necessary to ensure that the power budget on backed up domains are within the capabilities of switchers in PFM mode. An additional benefit of power gating peripheral loads during system startup is to enable the processor core to complete booting, and begin running software before additional supplies or peripheral devices are powered. This allows system software to bring up the additional supplies and close power gating switches in the most optimum order, to avoid problems with supply sequencing or transient current surges. The power gating switch drivers and integrated control are included for optimizing the system power tree.

The power gate drivers could be used for other general power gating as well. The text herein assumes the standard application of PWGT1 for core supply power gating and PWGT2 for Memory Hold power gating.

USER OFF POWER GATING

User Off configuration maintains PFM mode switchers on both the processor and external memory power domains. PWGTDRV1 is provided for power gating peripheral loads sharing the processor core supply domain(s) SW1, and/or SW2, and/or SW3. In addition, PWGTDRV2 is provided support to power gate peripheral loads on the SW4 supply domain.

In the typical application, SW1, SW2, and SW3 will all be kept active for the processor modules in state retention, and SW4 retained for the external memory in self refresh mode. SW1, SW2, and SW3 power gating FET drive would typically be connected to PWGTDRV1 (for parallel NMOS switches); SW4 power gating FET drive would typically be connected to PWGTDRV2. When Low-power Off mode is activated, the power gate drive circuitry will be disabled, turning off the NMOS power gate switches to isolate the maintained supply domains from any peripheral loading.

The power gate switch driver consist of a fully integrated charge pump (~5.0 V) which provides a low-power output to drive the gates of external NMOS switches placed between power sources and peripheral loading. The processor core(s) would typically be connected directly to the SW1 output node so that it can be maintained by SW1, while any circuitry that is not essential for booting or User Off operation is decoupled via the power gate switch. If multiple power domains are to be controlled together, power gating NMOS switches can share the PWGT1 gate drive. However, extra gate capacitance may require additional time for the charge pump gate drive voltage to reach its full value for minimum switch RDS_on.

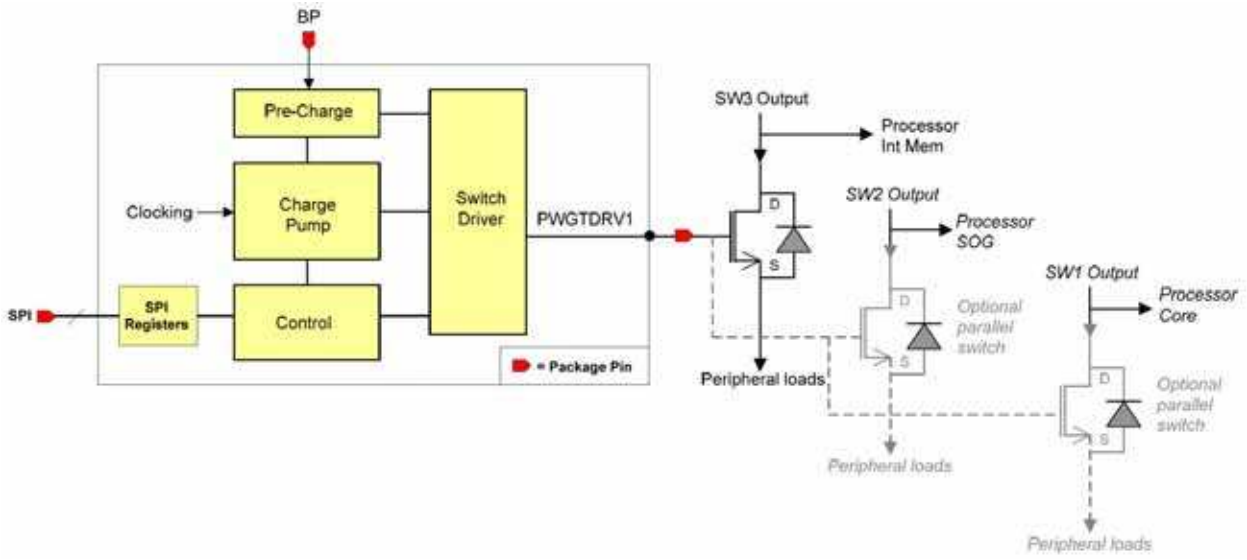


Figure 13. Power Gating Diagram

MEMORY HOLD POWER GATING

As with the User Off power gating strategy described previously, Memory Hold power gating is intended to allow isolation of the SW4 power domain, to selected circuitry in Low-power modes while cutting off the switcher domain from other peripheral loads. The only difference is that processor supplies SW1, and/or SW2, and/or SW3, are shut down in Memory Hold, so just the external memory is maintained in self refresh mode.

An external NMOS is to be placed between the direct-connected memory supply and any peripheral loading. The PWGTDRV2 pin controls the gate of the external NMOS and is normally pulled up to a charge pumped voltage (~5.0 V). During Memory Hold or User Off, PWGTDRV2 will go low to turn off the NMOS switch and isolate memory on the SW4 power domain.

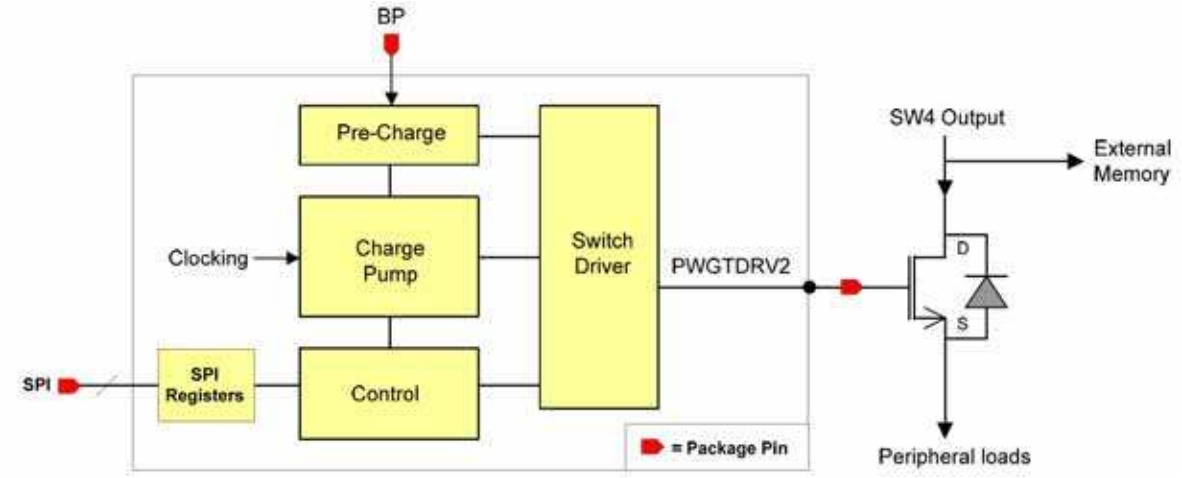


Figure 14. Memory Hold Circuit

EXITING FROM LOW-POWER OFF MODES

When a Turn On event occurs, any switchers that are active through Low-power Off modes will stay in PFM mode at their Standby voltage set points until the applicable time slot of the startup sequencer. At that point, the respective switcher is updated for the PUMSx defined default state for mode and voltage. Subsequent closing of the power gate switches will be coordinated by software to complete restoration of the full system power tree.

POWER GATING SPECIFICATIONS AND CONTROL

Table 37. Power Gating Characteristics

Parameter	Condition	Min	Typ	Max	Units
Output Voltage V_{OUT}	Output High	5.0	5.40	5.70	V
	Output Low	–	–	100	mV
Turn-on Time (66), (67)	Enable to $V_{OUT} = V_{OUTMIN}$ -250 mV	–	50	100	µs
Turn Off Time	Disable to V_{OUT} < 1.0 V	–	–	1.0	µs
Average Bias Current	t > 500 µs after Enable	–	1.0	5.0	µA
PWGTx Input Voltage	NMOS drain voltage	0.6	–	2.0	V
DC Load Current	At PWGTDRVx output	–	–	100	nA
Load Capacitance (66)	Used as a condition for the other parameters	0.5	–	1.0	nF

Notes
66. Larger capacitive loading values will lead to longer turn on times exceeding the given limits; smaller values will lead to larger ripple at the output.
67. Input supply is assumed in the range of 3.0 < BP < 4.65 V; lower BP values may extend turn on time, and functionality not supported for BP less than ~2.7 V.

A power gate driver pulled low may be thought of as power gating being active since this is the condition where a power source is isolated (or power gated) from its loading on the other side of the switch. The power gate drive outputs are SPI controlled in the active modes as shown in Table 38.

Table 38. Power Gate Drive State Control

Mode	PWGTDRV1	PWGTDRV2
Off	Low	Low
Cold Start	Low	Low
Warm Start	Low	Low
Watchdog, On, User Off Wait	SPI Controlled	SPI Controlled
User Off, Memory Hold, Internal Memory Hold Power Cut	Low	Low

When SPI controlled (Watchdog, On, and User Off Wait states), the PWGTDRVx power gate drive pin states are determined by SPI enable bits PWGTxSPIEN, according to Table 39.

Table 39. Power Gating Logic Table

PWGTxSPIEN	PWGTDRVx
1	Low
0	High

Notes
68. Applicable for Watchdog, On and User Off Wait modes only. If PWGT1SPIEN AND PWGT2SPIEN both = 1 then the charge pump is disabled.

GENERAL PURPOSE OUTPUTS

GPO drivers included can provide useful system level signaling with SPI enabling and programmable Standby control. Key use cases for GPO outputs include battery pack thermistor biasing and enabling of peripheral devices, such as light sensor(s), camera flash, or even supplemental regulators.

SPI enabling can be used for coordinating GPOs with ADC conversions for consumption efficiency and desired settling characteristics.

Four general purpose outputs are provided, summarized in Table 40 and Table 41 (active high polarities assumed).

Table 40. GPO Control Bits

SPI Bit	GPO Control
GPOxEN	GPOx enable
GPOxSTBY	GPOx controlled by STANDBY
x = 1, 2, 3, or 4	

Table 41. GPO Control Scheme

GPOxEN	GPOxSTBY	STANDBY	Output GPOx
0	X	X	Low
1	0	X	High
1	1	0	High
1	1	1	Low

Notes
69. GPO1 is automatically made active high when a charger is detected, see Battery Interface and Control for more information.

The GPO1 output is intended to be used for battery thermistor biasing. For accurate thermistor reading by the ADC, the output resistance of the GPO1 driver is of importance; see ADC Subsystem.

Table 42. GPO1 Driver Output Characteristics

Parameter	Condition	Min	Typ	Max	Units
GPO1 Output Impedance	Output VCORE Impedance to VCORE	200	–	500	Ohm

Finally, a muxing option is included to allow GPO4 to be configured for a muxed connection into Channel 7 of the GP ADC. As an application example, for a dual light sensor application, Channel 7 can be toggled between the ADIN7 (ADINSEL7 = 00) and GPO4 (ADINSEL7 = 11) for convenient connectivity and monitoring of two sensors. The GPO4 pin is configured for ADC input mode by default (GPO4ADIN = 1) so that the GPO driver stage is high-impedance at power up. The GPO4 pin can be configured by software for GPO operation with GPO4ADIN = 0. Refer to ADC Subsystem for GP ADC details.

SUPPLIES

SUPPLY FLOW

The switched mode power supplies and the linear regulators are dimensioned to support a supply flow based upon Figure 15.

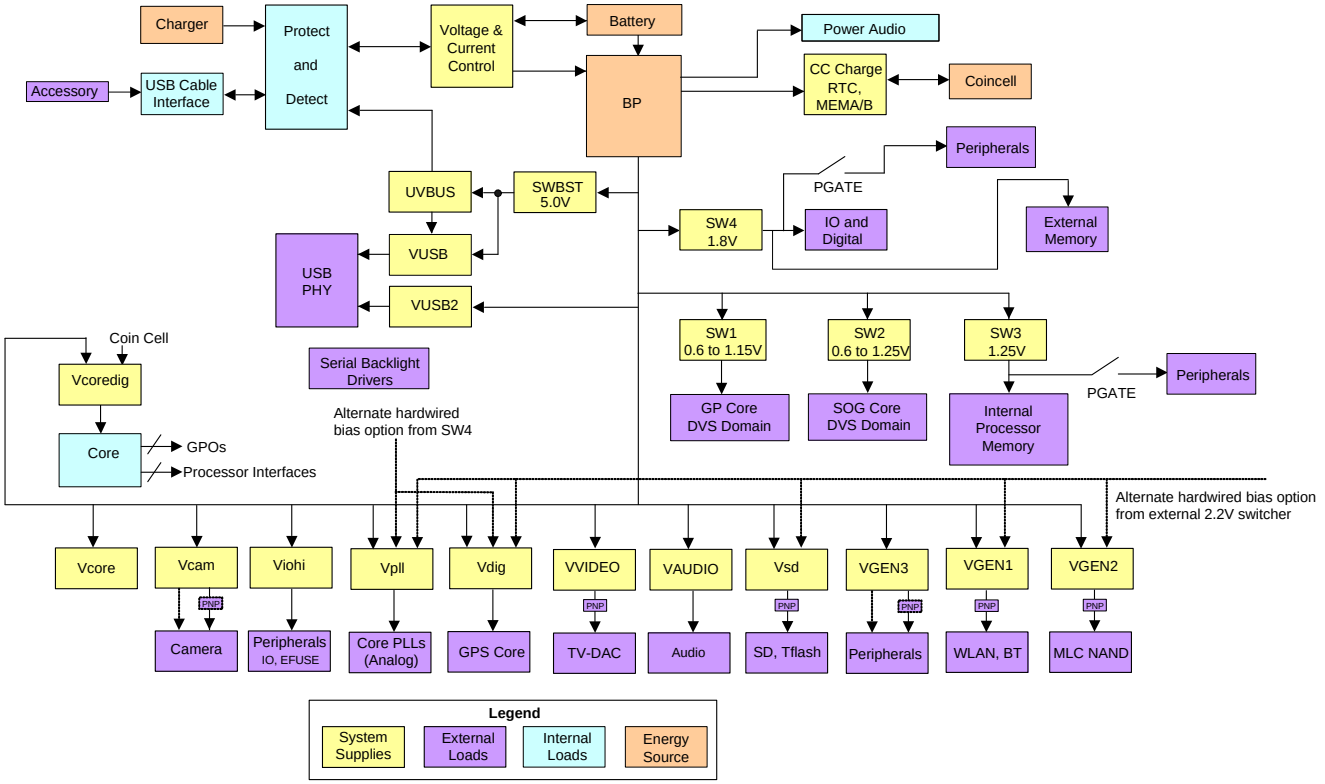


Figure 15. Supply Distribution

While maintaining the performance as specified, the minimum operating voltage for the supply tree is 3.0 V. For lower voltages, the performance may be degraded.

Table 43 summarizes the available power supplies.

Table 43. Power Tree Summary

Supply	Purpose (Typical Application)	Output Voltage (in V)	Load Capability (in mA)
SW1	Buck regulators for processor core(s)	0.600-1.375	1050
SW2	Buck regulators for processor SOG, etc.	0.600-1.375; 1.100-1.850	800
SW3	Buck regulators for internal processor memory and peripherals	0.600-1.375; 1.100-1.850	800
SW4	Buck regulators for external memory and peripherals	0.600-1.375; 1.100-1.850	800
SWBST	Boost regulator for USB OTG, Tri-color LED drivers	5.0	300
VIOHI	IO and Peripheral supply, eFuse support	2.775	100
VPLL	Quiet Analog supply (PLL, GPS)	1.2/1.25/1.5/1.8	50
VDIG	Low voltage digital (DPLL, GPS)	1.05/1.25/1.65/1.8	50
VSD	SD Card, external PNP	1.8/2.0/2.6/2.7/2.8/2.9/3.0/3.15	250
VUSB2	External USB PHY supply	2.4/2.6/2.7/2.775	50
VVIDEO	TV DAC supply, external PNP	2.5/2.6/2.7/2.775	350
VAUDIO	Audio supply	2.3/2.5/2.775/3.0	150

Table 43. Power Tree Summary

Supply	Purpose (Typical Application)	Output Voltage (in V)	Load Capability (in mA)
VCAM	Camera supply, internal PMOS	2.5/2.6/2.75/3.0	65
	Camera supply, external PNP	2.5/2.6/2.75/3.0	250
VGEN1	General peripherals supply #1, external PNP	1.2/1.5/2.775/3.15	200
VGEN2	General peripherals supply #2, external PNP	1.2/1.5/1.6/1.8/2.7/2.8/3.0/3.15	350
VGEN3	General peripherals supply #3, internal PMOS	1.8/2.9	50
	General peripherals supply #3, external PNP	1.8/2.9	250
VUSB	USB Transceiver supply	3.3	100

BUCK REGULATOR SUPPLIES

Four buck regulators are provided with integrated power switches and synchronous rectification. In a typical application, SW1 and SW2 are used for supplying the application processor core power domains. Split power domains allow independent DVS control for processor power optimization, or to support technologies with a mix of device types with different voltage ratings. SW3 is used for powering internal processor memory as well as low voltage peripheral devices and interfaces which can run at the same voltage level. SW4 is used for powering external memory as well as low voltage peripheral devices and interfaces which can run at the same voltage level.

An anticipated platform use case applies SW1 and SW2 to processor power domains that require voltage alignment to allow direct interfacing without bandwidth limiting synchronizers.

The buck regulators have to be supplied from the system supply BP, which is drawn from the main battery or the battery charger (when present). Figure 16 shows a high level block diagram of the buck regulators.

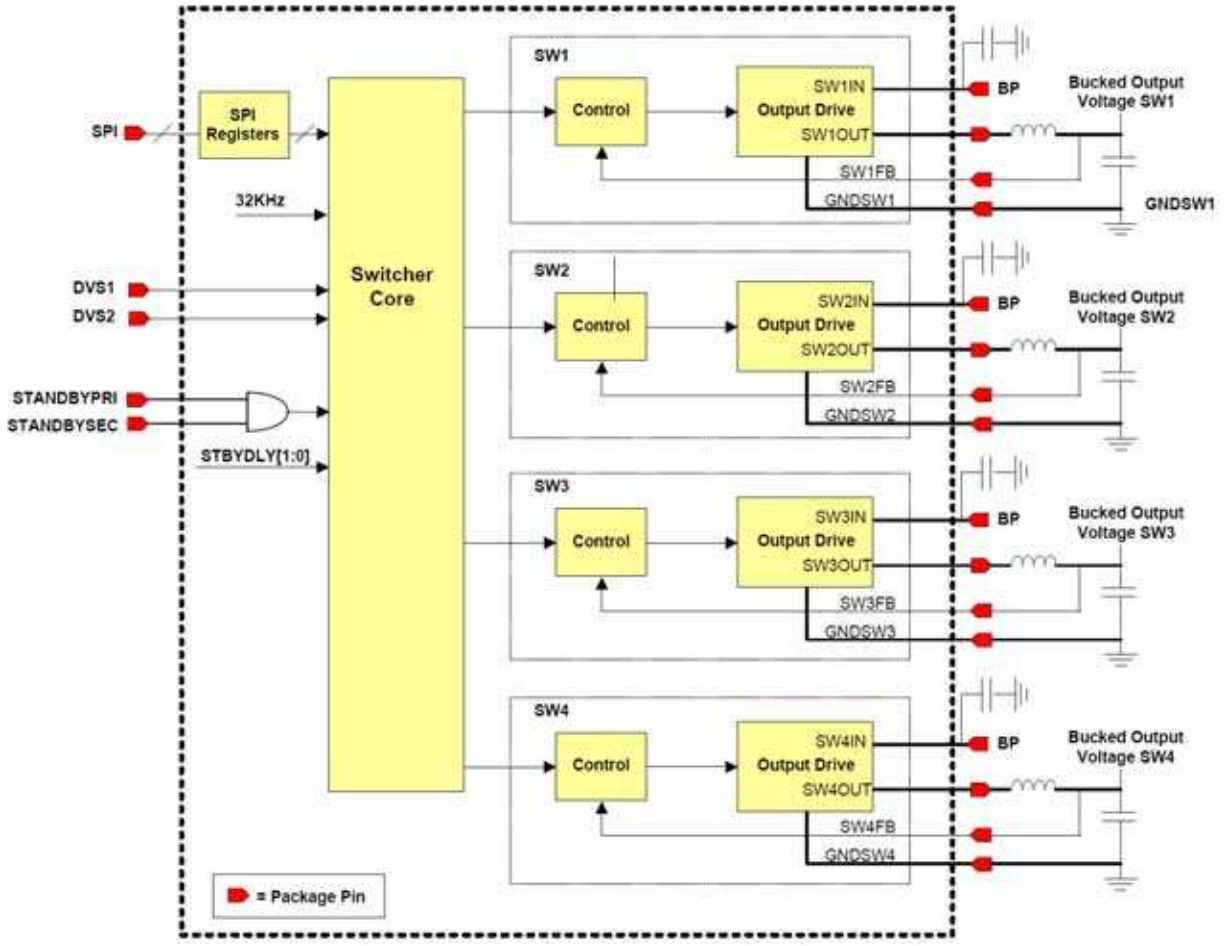


Figure 16. Buck Regulator Architecture

The Buck regulator topology includes an integrated synchronous rectifier, meaning that the rectifying diode is implemented on the chip as a low ohmic FET. The placement of an external diode is therefore not required, but overall switcher efficiency may benefit from this. The buck regulators permit a 100% duty cycle operation.

During normal operation, several power modes are possible depending on the loading. For medium and full loading, synchronous PWM control is the most efficient, while maintaining a constant switching frequency. Two PWM modes are available: the first mode sacrifices low load efficiency for a continuous switching operation (PWM-NPS). The second mode offers better low load efficiency by allowing the absence of switching cycles at low output loading (PWM-PS). This pulse skipping feature improves efficiency by reducing dynamic switching losses by simply switching less often.

In its lowest power mode, the switcher can regulate using hysteresis control known as a Pulse Frequency Modulation (PFM) control scheme. The frequency spectrum in this case will be a function of input and output voltage, loading, and the external components. Due to its spectral variance and lighter drive capability, PFM mode is generally reserved for non-active radio modes and Deep Sleep operation.

Buck modes of operation are programmable for explicitly defined or load-dependent control (Adaptive). Refer to the Buck regulators section in Power Control System for details.

Common control bits available to each buck regulator may be designated with a suffix “x” within this specification, where x stands for 1, 2, 3, or 4 (i.e., SWx = SW1, SW2, SW3, and SW4).

The output voltages of the buck regulators are SPI configurable, and two output ranges are available, individually programmed with SWxHI for SW2, SW3, and SW4 bucks, SW1 is limited to only one output range. Presets are available for both the Normal and Standby operation. SW1 and SW2 also include pin controlled DVS operation. When transitioning from one voltage to another, the output voltage slope is controlled in steps of 25 mV per time step (time step as defined for DVS stepping for SW1 and SW2, fixed at 4.0 μs for SW3 and SW4). This allows for support of dynamic voltage scaling (DVS) by using SPI driven voltage steps, state machine defined modes, and direct DVSx pin control.

When initially activated, switcher outputs will apply controlled stepping to the programmed value. The soft start feature limits the inrush current at startup. A built-in current limiter ensures that during normal operation, the maximum current through the coil is not exceeded. This current limiter can be disabled by setting the SWILIMB bit.

Point of Load feedback is intended for minimizing errors due to board level IR drops.

SWITCHING FREQUENCY

The switchers are driven by a high frequency clock. By default, the PLL generates an effective 3.145728 MHz signal based upon the 32.768 kHz oscillator signal by multiplying it by 96. To reduce spurious radio channels, the PLL can be programmed via PLLX[2:0] to different values as shown in Table 44.

Table 44. PLL Multiplication Factor

PLLX[2:0]	Multiplication Factor	Switching Frequency (Hz)
000	84	2 752 512
001	87	2 850 816
010	90	2 949 120
011	93	3 047 424
100 (default)	96	3 145 728
101	99	3 244 032
110	102	3 342 336
111	105	3 440 640

To reduce overall current drain, the PLL is automatically turned off if all switchers are in a PFM mode or turned off, and if the PLL clock signal is not needed elsewhere in the system. The clocking system provides nearly instantaneously, a high frequency clock to the switchers when the switchers are activated or exit the PFM mode for PWM mode. The PLL can be configured for continuous operation by setting the SPI bit PLLEN = 1.

Table 45. PLL Main Characteristics

Parameter	Condition [70]	Min	Typ	Max	Units
Frequency Accuracy		–	–	100	ppm
Bias Current	PLLEN = 1	–	50	80	µA
	1 Buck Regulator active	–	100	150	µA
	2 Buck Regulators active	–	115	170	µA
	3 Buck Regulators active	–	130	190	µA
	4 Buck Regulators active	–	145	210	µA
Start up Time	Cold Start	–	–	700	ns
	PFM to PWM	–	–	600	ns

Notes
70. Clock input to PLL is 32.768 kHz

Table 46. PLL Control Registers

Name	R/W	Reset Signal	Reset State	Description
PLLEN	R/W	RESETB	0	1 = Forces PLL on 0 = PLL automatically enabled
PLLX[2:0]	R/W	RESET	100	Selects PLL multiplication factor

BUCK REGULATOR CORE

Table 47. Buck Regulators (SW1, 2, 3, 4) Output Voltage Programmability

Set point	SWx[4:0]	SWx Output, SWxHI = 0 (Volts)	SWx Output [71], SWxHI = 1 (Volts)
0	00000	0.600	1.100
1	00001	0.625	1.125
2	00010	0.650	1.150
3	00011	0.675	1.175
4	00100	0.700	1.200
5	00101	0.725	1.225
6	00110	0.750	1.250
7	00111	0.775	1.275
8	01000	0.800	1.300
9	01001	0.825	1.325
10	01010	0.850	1.350
11	01011	0.875	1.375
12	01100	0.900	1.400
13	01101	0.925	1.425
14	01110	0.950	1.450
15	01111	0.975	1.475
16	10000	1.000	1.500
17	10001	1.025	1.525
18	10010	1.050	1.550
19	10011	1.075	1.575
20	10100	1.100	1.600
21	10101	1.125	1.625
22	10110	1.150	1.650
23	10111	1.175	1.675
24	11000	1.200	1.700
25	11001	1.225	1.725
26	11010	1.250	1.750
27	11011	1.275	1.775

Table 47. Buck Regulators (SW1, 2, 3, 4) Output Voltage Programmability

Set point	SWx[4:0]	SWx Output, SWxHI = 0 (Volts)	SWx Output [71], SWxHI = 1 (Volts)
28	11100	1.300	1.800
29	11101	1.325	1.825
30	11110	1.350	1.850
31	11111	1.375	1.850

71. Output range not available for SW1. SW1 output range is 0.600-1.375, therefore SW1HI = 1 does not apply to SW1. The SW1HI bit should always be set to 0.

Since the startup default values of the buck regulators are dependent on the state of the PUMS pin, the SWxHI bit settings will likewise be determined by the PUMS pin. The settings are aligned to the likely application ranges for use cases as given in the Defaults tables in Power Control System. The following tables define the SWxHI bit states after a startup event is completed, but can be reconfigured via the SPI if desired, if an alternate range is needed. Care should be taken when changing SWxHI bit to avoid unintended jumps in the switcher output. The SWxHI setting applies to Normal, Standby, and DVS set points for the corresponding switcher.

Table 48. SWxHI States for Power Up Defaults

PUMS1	Ground	Open	VCOREDIG	VCORE	Ground	Open
PUMS2	**Open**	**Open**	**Open**	**Open**	**Ground**	**Ground**
SW1HI	0	0	0	0	0	0
SW2HI	0	0	0	0	1	1
SW3HI	0	0	0	0	1	1
SW4HI	1	1	1	1	1	1

Note that the following efficiency curves were measured with the MC13892 in a socket.

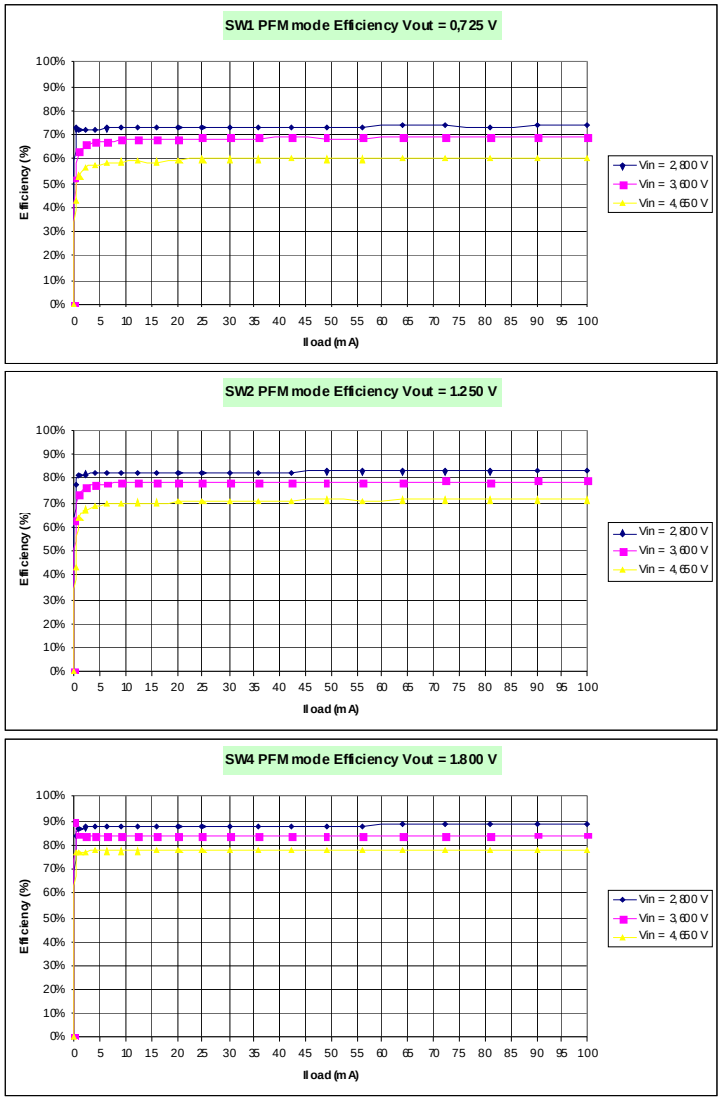


Figure 17. Buck Regulator PFM Efficiency

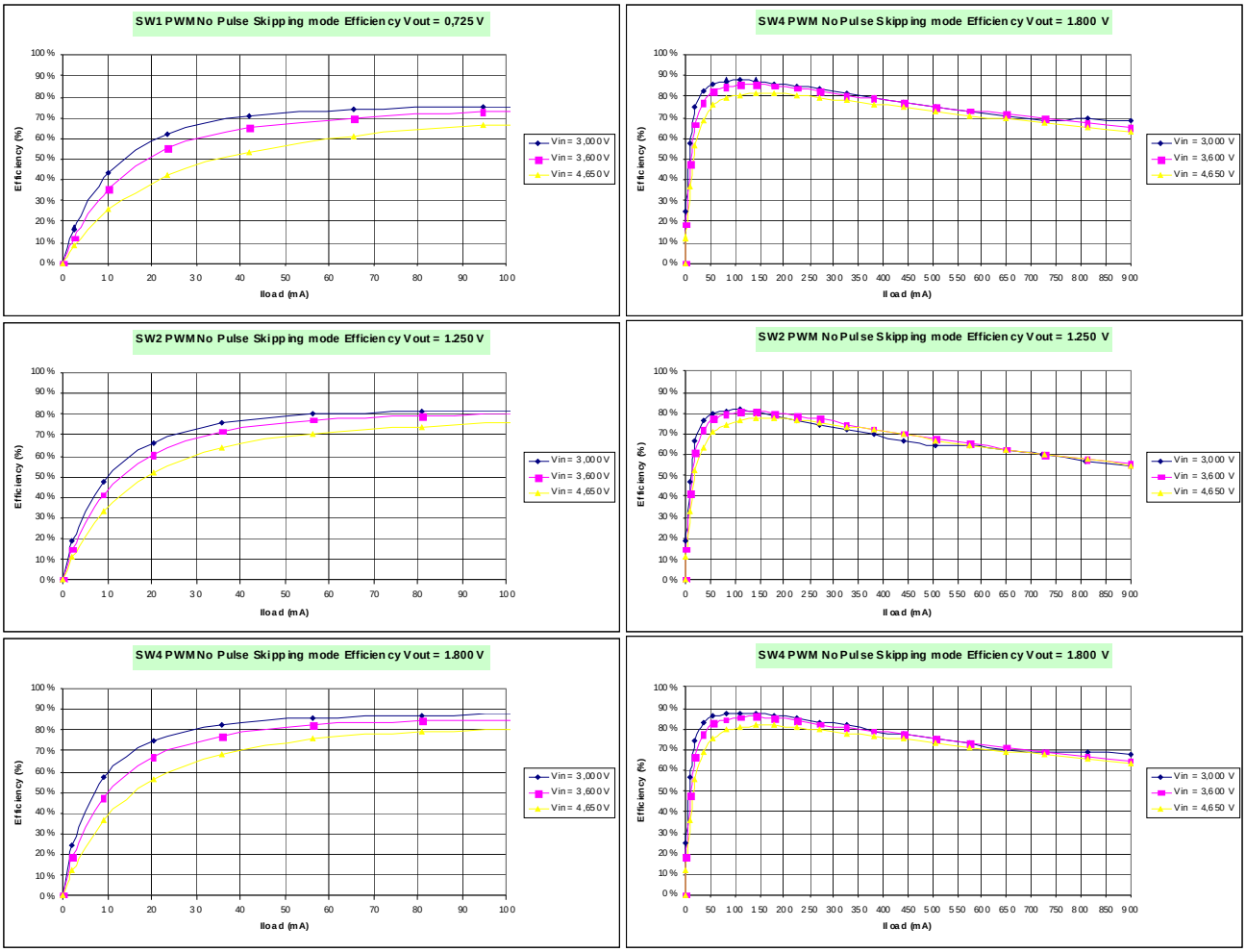


Figure 18. Buck Regulator PWM (No Pulse Skipping) Efficiency

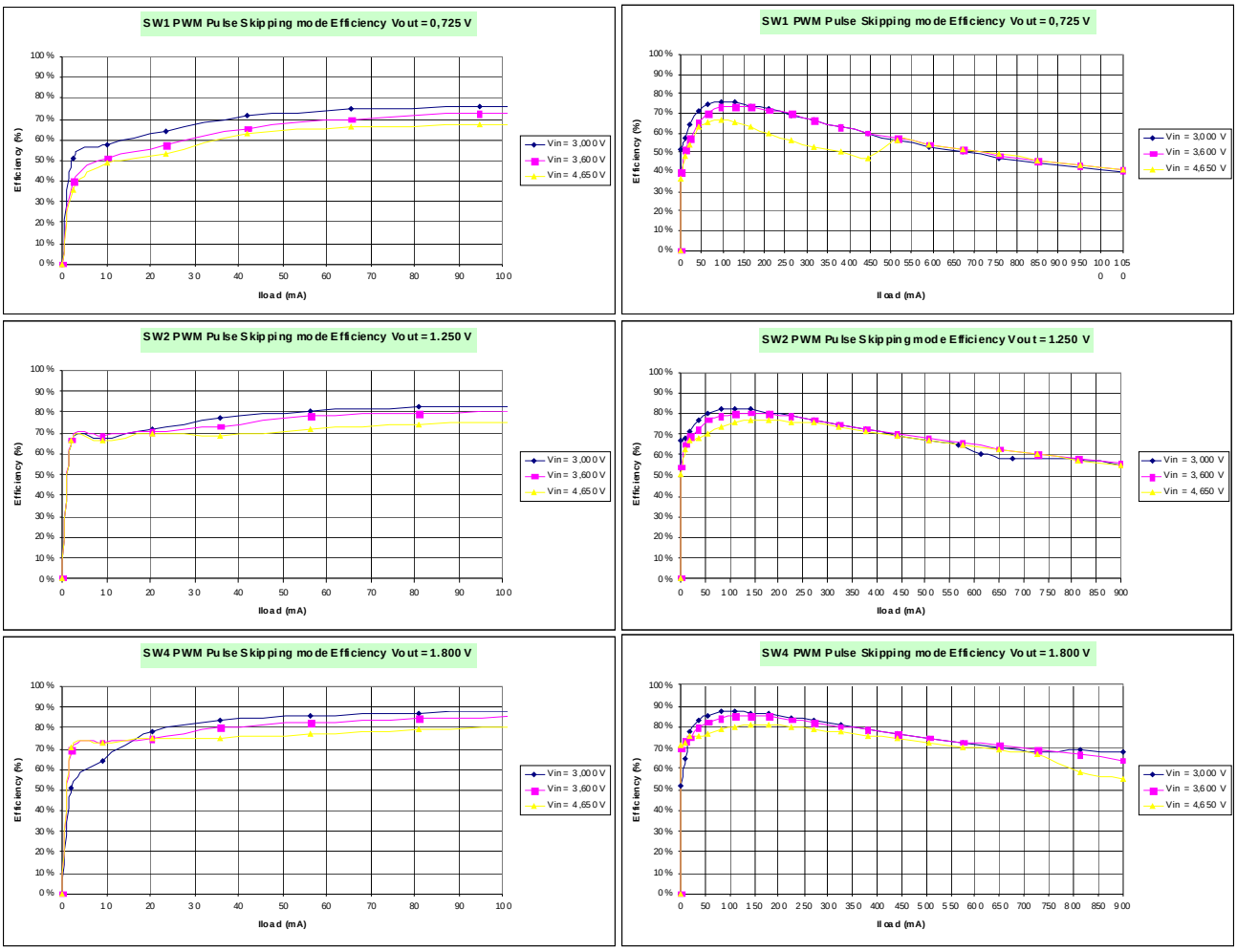


Figure 19. Buck Regulator PWM (Pulse Skipping) Efficiency

DYNAMIC VOLTAGE SCALING

To reduce overall power consumption, processor core voltages can be varied depending on the mode or activity level of the processor. SW1 and SW2 allow for three different set points with controlled transitions to avoid sudden output voltage changes, which could cause logic disruptions on their loads. Preset operating points for SW1 and SW2 can be set up for:

- Normal operation: output value selected bySPI bits SWx[4:0]. Voltage transitions initiated by SPI writes to SWx[4:0] are governed by the same DVS stepping rate that is programmed for DVSx pin initiated transitions.
- DVS: output can be higher or lower than normal operation for tailoring to application requirements. Configured by SPI bits SWxDVS[4:0] and controlled by a DVSx pin transition.
- Standby (Deep Sleep): can be higher or lower than normal operation, but is typically selected to be the lowest state retention voltage of a given process. Set by SPI bits SWxSTBY[4:0] and controlled by a Standby event (STANDBY logically anded with STANDBYSEC). Voltage transitions initiated by Standby are governed by the same DVS stepping that is programmed for DVSx pin initiated transitions.

The following tables summarize the set point control and DVS time stepping applied to SW1 and SW2.

Table 49. DVS Control Logic Table for SW1 and SW2

STANDBY (72)	DVSx Pin	Set Point Selected by
0	0	SWx[4:0]
0	1	SWxDVS[4:0]
1	X	SWxSTBY[4:0]

Notes
72. STANDBY is the logical anding of STANDBY and STANDBYSEC

Table 50. DVS Speed Selection for SW1 and SW2

SWxDVSSPEED[1:0]	Function
00	25 mV step each 2.0 μs
01 (default)	25 mV step each 4.0 μs
10	25 mV step each 8.0 μs
11	25 mV step each 16 μs

Since the switchers have a strong sourcing capability but no active sinking capability, the rising slope is determined by the switcher, but the falling slope can be influenced by the load. Additionally, as the current capability in PFM mode is reduced, controlled DVS transitions in PFM mode could be affected. Critically timed DVS transitions are best assured with PWM mode operation.

Note that there is a special mode of DVS control for Switcher Increment / Decrement (SID) operation described later in this chapter.

DVS pin controls are not included for SW3 and SW4. However, voltage transitions programmed through the SPI will step in increments of 25 mV per 4.0 μs, to allow SPI controlled voltage stepping with SWx[4:0]. Additionally, SW3 and SW4 include Standby mode set point programmability.

Figure 20 shows the general behavior for the switchers when initiated with pin controlled DVS, SPI programming or standby control.

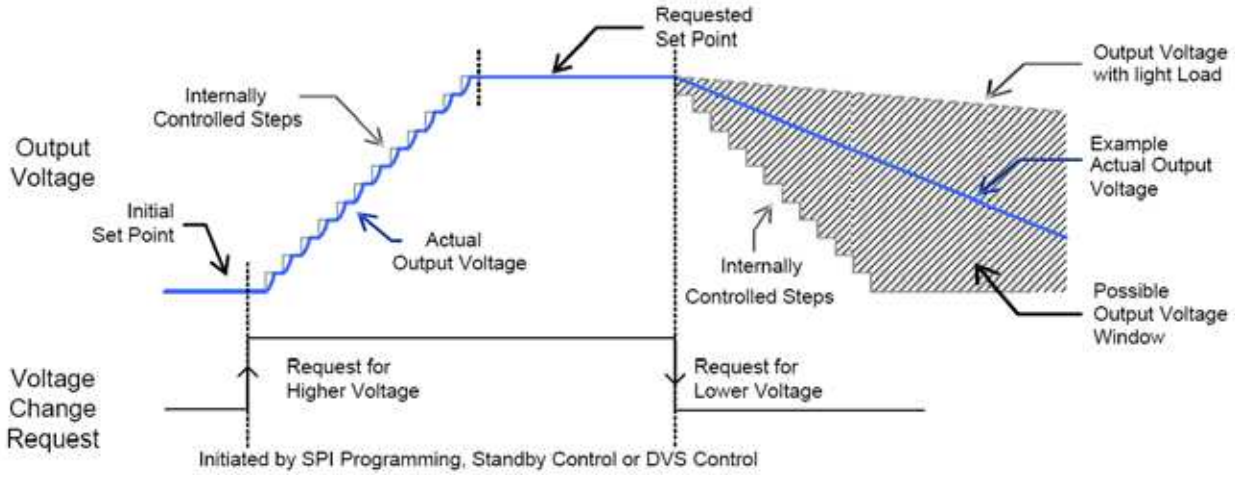


Figure 20. SW1 Voltage Stepping with Pin Controlled DVS

Note that the DVSx input pins are reconfigured for Switcher Increment / Decrement (SID) control mode when SPI bit SIDEN = 1. Refer to the SID description below for further details.

SWITCHER INCREMENT / DECREMENT

A scheme for incrementing or decrementing the operating set points of SW1 and SW2 is desirable for improved Dynamic Process and Temperature Compensation (DPTC) control in support of fine tuning power domains for the processor supply tree. An increment command will increase the set point voltage by a single 25 mV step. A decrement command will decrease the set point by a single 25 mV step. The transition time for the step will be the same as programmed with SWxDVSSPEED[1:0] for DVS

stepping. If a switcher runs out of programmable range (in either direction), as constrained by programmable stops, then the increment or decrement command shall be ignored.

The Switcher Increment / Decrement (SID) function is enabled with SIDEN = 1. This will reassign the function of the DVS1 and DVS2 pins, from the default toggling between Normal and DVS operating modes, to a jog control mode for the switcher which DVSx is assigned. Once enabled, the switcher being controlled will start at the Normal mode set point as programmed with SWx[4:0] and await any jog commands from the processor. The adjustment scheme essentially intercepts the Normal mode set point SPI bits (i.e., but not DVS or Standby programmed set points), and makes any necessary adjustments based on jog up or jog down commands. The modified set point bits are then immediately passed to the switching regulator, which would then do a DVS step in the appropriate direction. The SPI bits containing Normal mode programming are not directly altered.

When configured for SID mode, a high pulse on the DVSx pin will indicate one of 3 actions to take, with the decoding as a function of how many contiguous SPI clock falling edges are seen while the DVSx pin is held high.

Table 51. SID Control Protocol

Number of SPI CLK Falling Edges while DVSx = 1	Function
0	No action. Switcher stays at its presently programmed configuration
1	Jog down. Drive buck regulator output down a single DVS step
2	Jog up. Drive buck regulator output up a single DVS step
3 or more	Panic Mode. DVS step the buck regulator output to the Normal mode value as programmed in the SPI register

The SID protocol is illustrated by way of example, assuming SIDEN = 1, and that DVS1 is controlling SW1. SW1 starts out at its default value of 1.250 V (SW1 = 11010) and is stepped both up and down via the DVS1 pin. The SPI bits SW1 = 11010 do not change. The set point adjustment takes place in the SID block prior to bit delivery to the switcher's digital control.

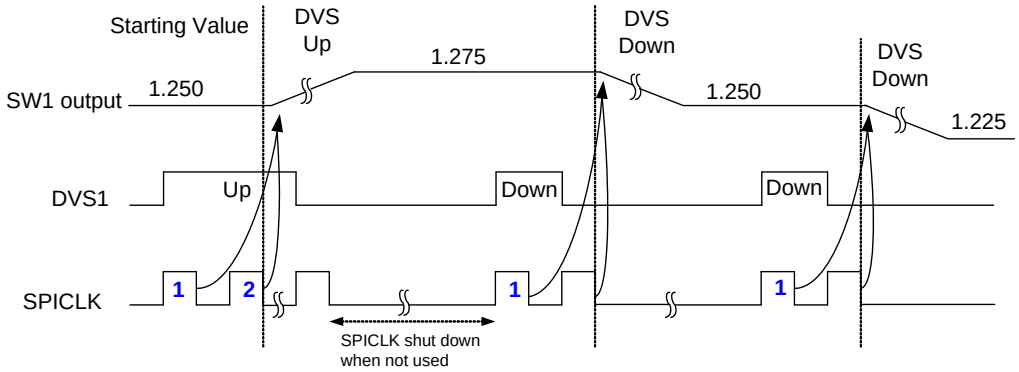


Figure 21. SID Control Example for Increment & Decrement

SID Panic Mode is provided for rapid recovery to the programmed Normal mode output voltage, so the processor can quickly recover to its high performance capability with a minimum of communication latency. In Figure 22, Panic Mode recovery is illustrated as an Increment step, initiated by the detection of the second falling SPI clock edge, followed by a continuation to the programmed SW1[4:0] level (1.250 V in this example), due to the detection of the third contiguous falling edge of SPI clock while DVS1 is held high.

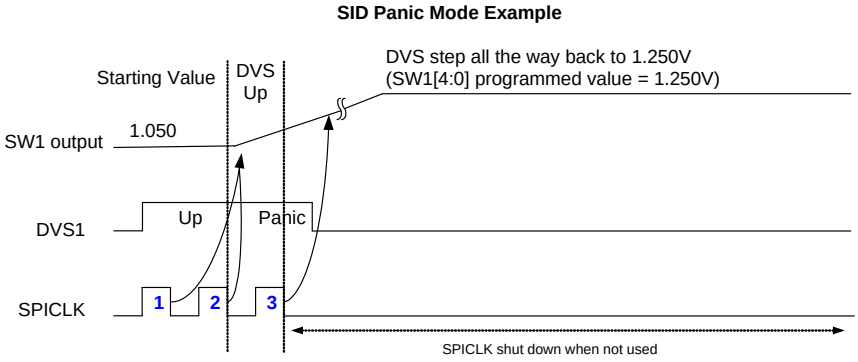


Figure 22. SID Control Example for Panic Mode Recovery

The system will not respond to a new jog command until it has completed a DVS step that may be in progress. Any missed jog requests will not be stored. For instance, if a switcher is stepping up in voltage with a 25 mV step over a 4.0 μs time, response to the DVSx pin for another step will be ignored until the DVS step period has expired. However, the Panic Mode step recovery should respond immediately upon detection of the third SPICLK edge while the corresponding DVSx pin is high, even if the initial decode of the jog up command is ignored, because it came in before the previous step was completed.

While in SID mode, programmable stops are used to set limits on how far up and how far down a SID-controlled buck regulator will be allowed to step. The SWxSIDMIN[3:0] and SWxSIDMAX[3:0] bits can be used to ensure that voltage stepping is confined to within the acceptable bounds for a given process technology used for the BB IC.

To contain all of the SWx voltage setting bits in single banks, the SWxSIDMIN[3:0] word is shortened to 4-bits, but should be decoded by logic to have an implied leading 0 (i.e., MSB = 0, but is not included in the programmable word). For instance, SW1SIDMIN = 1000 (default value) should be decoded as 01000, which corresponds to 0.800 V (assuming SW1HI = 0).

Likewise, the SWxSIDMAX[3:0] word is shortened to 4-bits, but should be decoded by logic to have an implied leading 1 (MSB = 1, but is not included in the programmable word). For instance, SW1SIDMAX = 1010 (default value) should be decoded as 11010, which corresponds to 1.250 V (again, assuming SW1HI = 0).

A new SPI write for the active switcher output value with SWx[4:0] should take immediate effect, and this becomes the new baseline from which succeeding SID steps are referenced. The SWxDVS[4:0] value is not considered during SID mode. The system only uses the SWx[4:0] bits and the min/max stops SWxSIDMIN[3:0] and SWxSIDMAX[3:0].

When in SID mode, a STANDBY = 1 event (pin states of STANDBY and STANDBYSEC) will have the “immediate” effect (after any STBYDLY delay has timed out) of changing the set point and mode to those defined for Standby operation. Exiting Standby puts the system back to the normal mode set point with no stored SID adjustments -- the system will recalibrate itself again from the refreshed baseline.

BOOST REGULATOR

SWBST is a boost switching regulator with a fixed 5.0 V output. It runs at 2/3 of the switcher PLL frequency. SWBST supplies the VUSB regulator for the USB system in OTG mode, and it also supplies the power for the RGB LED's. When SWBST is configured to supply the VBUS pin in OTG mode, the feedback will be switched to sense the UVBUS pin instead of the SWBSTFB pin. Therefore, when driving the VBUS for OTG mode the output of the switcher may rise to 5.75 V to compensate for the voltage drops on the internal switches. Note that the parasitic leakage path for a boost regulator will cause the output voltage SWBSTOUT and SWBSTFB to sit at a Schottky drop below the battery voltage whenever SWBST is disabled. The switching NMOS transistor is integrated on-chip. An external fly back Schottky diode, inductor and capacitor are required.

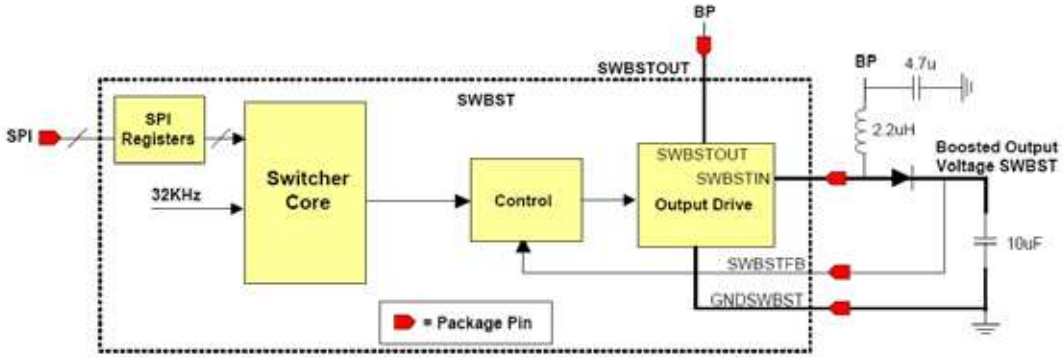


Figure 23. Boost Regulator Architecture

Enabling of SWBST is accomplished through the SWBSTEN SPI control bit.

Table 52. Switch Mode Supply SWBST Control Function Summary

Parameter	Value	Function
SWBSTEN	0	SWBST OFF
	1	SWBST ON

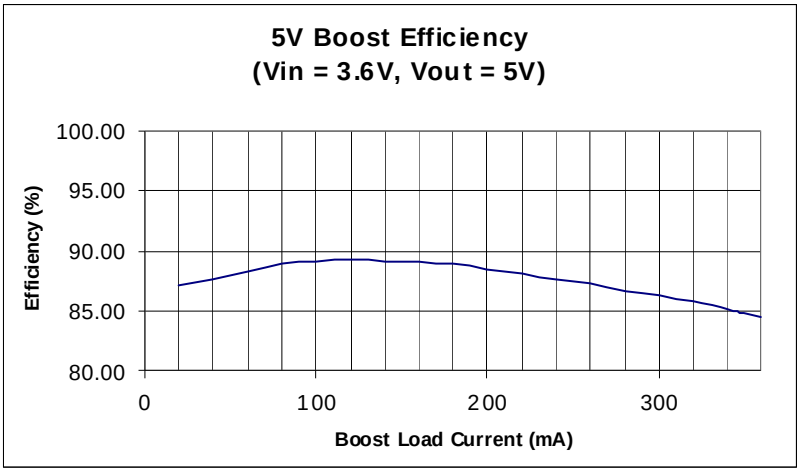


Figure 24. Boost Regulator Efficiency

LINEAR REGULATORS

This section describes the linear regulators provided. For convenience, these regulators are named to indicate their typical or possible applications, but the supplies are not limited to these uses and may be applied to any loads within the specified regulator capabilities.

A low-power standby mode controlled by STANDBY is provided in which the bias current is aggressively reduced. This mode is useful for deep sleep operation where certain supplies cannot be disabled, but active regulation can be tolerated with lesser parametric requirements. The output drive capability and performance are limited in this mode. Refer to STANDBY Event Definition and Control in Power Control System for more details.

Some dedicated regulators are covered in their related chapters rather than in the Supplies chapter (i.e., the VUSB and VUSB2 supplies are included in Connectivity).

Apart from the integrated linear regulators, there are also GPO output pins provided to enable and disable discrete regulators or functional blocks, or to use as a general purpose output for any system need. For example, one application may be to enable a battery pack thermistor bias in synchronization with timed ADC conversions.

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at REFCORE. The bandgap and the rest of the core circuitry is supplied from VCORE. The performance of the regulators is directly dependent on the performance of VCOREDIG and the bandgap. No external DC loading is allowed on VCOREDIG or REFCORE. VCOREDIG is kept powered as long as there is a valid supply and/or coin cell. Table 53 captures the main characteristics of the core circuitry.

Table 53. Core Specifications

Reference	Parameter	Target
VCOREDIG (Digital core supply)	Output voltage in ON mode (73),(74)	1.5 V
	Output voltage in Off mode(74)	1.2 V
	Bypass Capacitor	2.2 µF typ (0.65 µF derated)
VCORE (Analog core supply)	Output voltage in ON mode (73),(74)	2.775 V
	Output voltage in Off mode (74)	0.0 V
	Bypass Capacitor	2.2 µF typ (0.65 µF derated)
REFCORE (Bandgap / Regulator Reference)	Output voltage (73)	1.20 V
	Absolute Accuracy	0.50%
	Temperature Drift	0.25%
	Bypass Capacitor	100 nF typ (65 nF derated)

Notes

73. 3.0 V < BP < 4.65 V, no external loading on VCOREDIG, VCORE, or REFCORE. Extended operation down to UVDET, but no system malfunction.
74. The core is in On mode when charging or when the state machine of the IC is not in the Off mode nor in the power cut mode. Otherwise, the core is in Off mode.

REGULATORS GENERAL CHARACTERISTICS

The following applies to all linear regulators unless otherwise specified.

- Specifications are for an ambient temperature of -40 to +85 °C.
- Advised bypass capacitor is the Murata™ GRM155R60G225ME15 which comes in a 0402 case.
- In general, parametric performance specifications assume the use of low ESR X5R ceramic capacitors with 20% accuracy and 15% temperature spread, for a worst case stack up of 35% from the nominal value. Use of other types with wider temperature variation may require a larger room temperature nominal capacitance value to meet performance specs over temperature. In addition, capacitor derating as a function of DC bias voltage requires special attention. Finally, minimum bypass capacitor guidelines are provided for stability and transient performance. Larger values may be applied; performance metrics may be altered and generally improved, but should be confirmed in system applications.
- Regulators which require a minimum output capacitor ESR (those with external PNPs) can avoid an external resistor if ESR is assured with capacitor specifications, or board level trace resistance.
- The output voltage tolerance specified for each of the linear regulators include process variation, temperature range, static line regulation, and static load regulation.
- The PSRR of the regulators is measured with the perturbed signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements care must be taken not to reach the drop out of the regulator under test.
- In the Low-power mode the output performance is degraded. Only those parameters listed in the Low-power mode section are guaranteed. In this mode, the output current is limited to much lower currents than in the Active mode.
- Regulator performance is degraded in the extended input voltage range. This means that the supply still behaves as a regulator and will try to hold up the output voltage by turning the pass device fully on. As a result, the bias current will increase and all performance parameters will be heavily degraded, such as PSRR and load regulation.
- Note that in some cases, the minimum operating range specifications may be conflicting due to numerous set point and biasing options, as well as the potential to run BP into one of the software or hardware shutdown thresholds. The specifications are general guidelines which should be interpreted with some care.
- When a regulator gets disabled, the output will be pulled towards ground by an internal pull-down. The pull-down is also activated when RESETB goes low.
- 32kHz spur levels are specified for fully loaded conditions.

- Short-circuit protection (SCP) is included on certain LDOs (seethe SCP section later in this chapter). Exceeding the SCP threshold will disable the regulator and generate a system interrupt. The output voltage will not sag below the specified voltage for the rated current being drawn. For the lower current LDOs without SCP, they are less accessible to the user environment and essentially self-limiting.
- The power tree of a given application must be scrubbed for critical use cases to ensure consistency and robustness in the power strategy.

TRANSIENT RESPONSE WAVEFORMS

The transient load and line response are specified with the waveforms as depicted in Figure 25. Note that the transient load response refers to the overshoot only, excluding the DC shift itself. The transient line response refers to the sum of both overshoot and DC shift. This is also valid for the mode transition response.

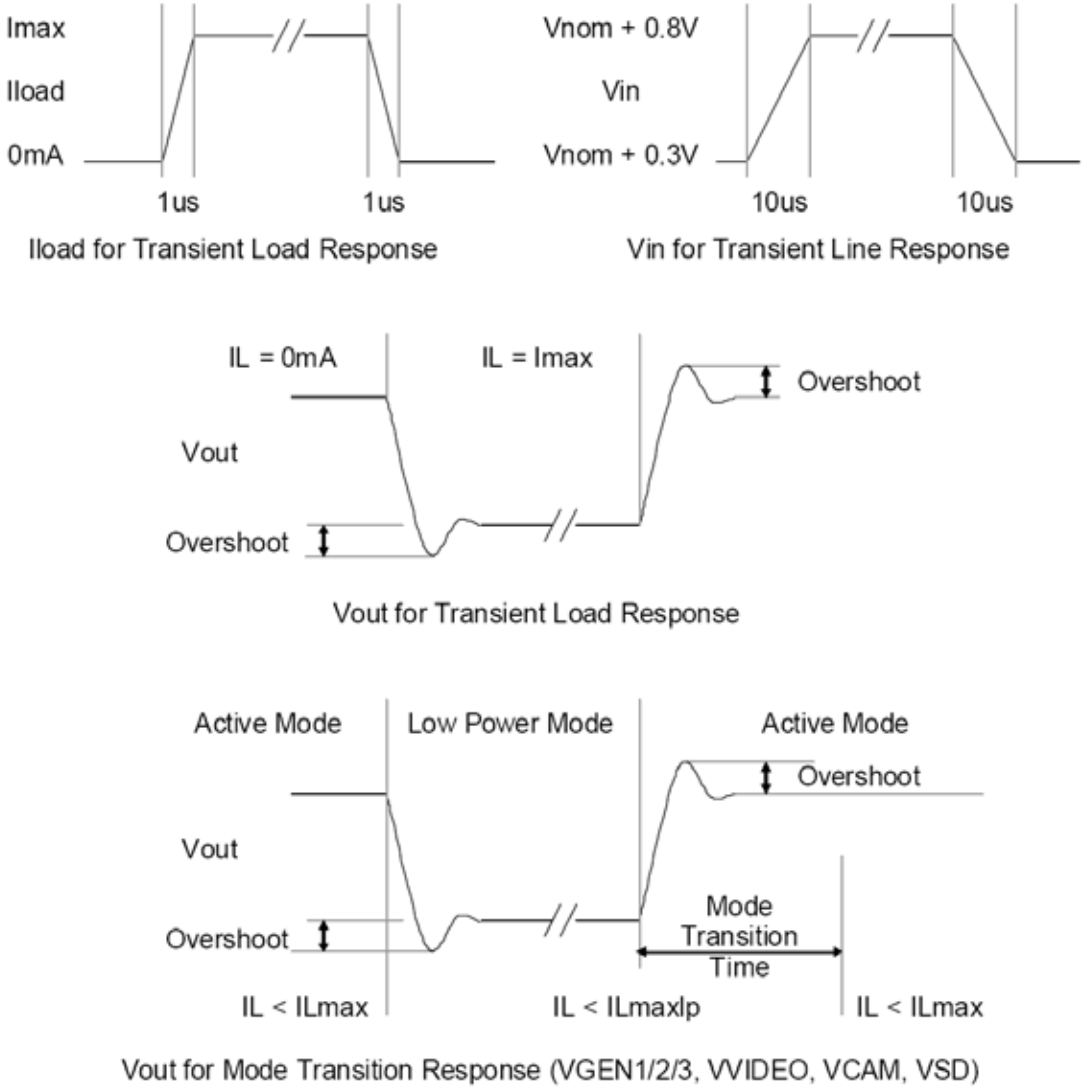


Figure 25. Transient Waveforms

SHORT-CIRCUIT PROTECTION

The higher current LDOs and those most accessible in product applications include short-circuit detection and protection (VVIDEO, VAUDIO, VCAM, VSD, VGEN1, VGEN2, and VGEN3). The short-circuit protection (SCP) system includes debounced fault condition detection, regulator shutdown, and processor interrupt generation, to contain failures and minimize chance of

product damage. If a short-circuit condition is detected, the LDO will be disabled by resetting its VxEN bit while at the same time an interrupt SCPI will be generated to flag the fault to the system processor.

The SCPI interrupt is maskable through the SCPM mask bit.

The SCP feature is enabled by setting the REGSCPEN bit. If this bit is not set, then not only is no interrupt generated, but also the regulators will not automatically be disabled upon a short-circuit detection. However, the built-in current limiter will continue to limit the output current of the regulator. Note that by default, the REGSCPEN bit is not set, so at startup none of the regulators that are in an overload condition will be disabled

VAUDIO AND VVIDEO SUPPLIES

The primary applications of these power supplies are for audio, and TV-DAC. However these supplies could also be used for other peripherals if one of these functions is not required. Low-power modes and programmable Standby options can be used to optimize power efficiency during Deep Sleep modes.

An external PNP is utilized for VVIDEO to avoid excess on-chip power dissipation at high loads, and large differential between BP and output settings. For stability reasons a small minimum ESR may be required. In the Low-power mode for VVIDEO an internal bypass path is used instead of the external PNP. External PNP devices are always to be connected to the BP line in the application. The recommended PNP device is the ON Semiconductor NSS12100XV6T1G which is capable of handling up to 250 mW of continuous dissipation at minimum footprint and 75 ℃ of ambient. For use cases where up to 500mW of dissipation is required, the recommended PNP device is the ON Semiconductor™ NSS12100UW3TCG. For stability reasons a small minimum ESR may be required.

VAUDIO is implemented with an integrated PMOS pass FET and has a dedicated input supply pin VINAUDIO.

The following tables contain the specifications for the VVIDEO, VAUDIO.

Table 54. VVIDEO and VAUDIO Voltage Control

Parameter	Value	Function	ILoad max
VVIDEO	00	Output = 2.700 V	250 mA / 350 mA
	01	Output = 2.775 V	250 mA / 350 mA
	10	Output = 2.500 V	250 mA / 350 mA
	11	Output = 2.600 V	250 mA / 350 mA
VAUDIO	00	Output = 2.300 V	150 mA
	01	Output = 2.500 V	150 mA
	10	Output = 2.775 V	150 mA
	11	Output = 3.000 V	150 mA

LOW VOLTAGE SUPPLIES

VDIG and VPLL are provided for isolated biasing of the Baseband system PLLs for clock generation in support of protocol and peripheral needs. Depending on the lineup and power requirements, these supplies may be considered for sharing with other loads, but noise injection must be avoided and filtering added if necessary, to ensure suitable PLL performance. The VDIG and VPLL regulators have a dedicated input supply pin: VINDIG for the VDIG regulator, and VINPLL for the VPLL regulator. VINDIG and VINPLL can be connected to either BP or a 1.8V switched mode power supply rail, such as from SW4 for the two lower set points of each regulator VPLL[1:0] and VDIG[1:0] = [00], [01]. In addition, when the two upper set points are used VPLL[1:0] and VDIG[1:0] = [10], [11], the inputs (VINDIG and VINPLL) can be connected to either BP of a 2.2 V nominal external switched mode power supply rail to improve power dissipation.

Table 55. VPLL and VDIG Voltage Control

Parameter	Value	Function	ILoad max	Input Supply
VPLL[1:0]	00	output = 1.2 V	50 mA	BP or 1.8 V
	01	output = 1.25 V	50 mA	BP or 1.8 V
	10	output = 1.5 V	50 mA	BP or External Switcher
	11	output = 1.8 V	50 mA	BP or External Switcher
VDIG[1:0]	00	output = 1.05 V	50 mA	BP or 1.8 V
	01	output = 1.25 V	50 mA	BP or 1.8 V
	10	output = 1.65 V	50 mA	BP or External Switcher
	11	output = 1.8 V	50 mA	BP or External Switcher

PERIPHERAL INTERFACING

IC interfaces in the lineups generally fall in two categories: low voltage IO primarily associated with the AP IC and certain peripherals at SPIVCC level (powered from SW4), and a higher voltage interface level associated with other peripherals not compatible with the 1.8 V SPIVCC. VIOHI is provided at a fixed 2.775 V level for such interfaces, and may also be applied to other system needs within the guidelines of the regulator specifications. The input VINIOHI is not only used by the VIOHI regulator, but also by other blocks, therefore it should always be connected to BP, even if the VIOHI regulator is not used by the system.

VIOHI has an internal PMOS pass FET which will support loads up to 100 mA.

CAMERA

The camera module is supplied by the regulator VCAM. This allows powering the entire module independent of the rest of other parts of the system, as well as to select from a number of VCAM output levels for camera vendor flexibility. In applications with a dual camera, it is anticipated that only one of the two cameras is active at a time, allowing the VCAM supply to be shared between them.

VCAM has an internal PMOS pass FET which will support up to 2.0 Mpixel Camera modules (<65 mA). To support higher resolution cameras, an external PNP is provided. The external PNP configuration is offered to avoid excess on-chip power dissipation at high loads, and large differential between BP and output settings. For lower current requirements, an integrated PMOS pass FET is included. The input pin for the integrated PMOS option is shared with the base current drive pin for the PNP option. The external PNP configuration must be committed as a hardwired board level implementation, while the operating mode is selected through the VCAMCONFIG bit after startup. The VCAM is not automatically enabled during the power up sequence, allowing software to properly set the VCAMCONFIG bit before the regulator is activated. The recommended PNP device is the ON Semiconductor NSS12100XV6T1G which is capable of handling up to 250 mW of continuous dissipation at a minimum footprint and 75 ℃ of ambient. For use cases where up to 500 mW of dissipation is required, the recommended PNP device is the ON Semiconductor NSS12100UW3TCG. For stability reasons a small minimum ESR may be required.

The input VINCAM should always be connected to BP, even if the VCAM regulator is not used by the system.

Table 56. VCAM Voltage Control

Parameter	Value	Output Voltage	ILoad max	
			VCAMCONFIG=0 Internal Pass FET	VCAMCONFIG=1 External PNP
VCAM[1:0]	00	2.5 V	65 mA	250 mA
	01	2.6 V	65 mA	250 mA
	10	2.75 V	65 mA	250 mA
	11	3.00 V	65 mA	250 mA

MULTI-MEDIA CARD SUPPLY

This supply domain is generally intended for user accessible multi-media cards, such as Micro-SD (TransFlash), RS-MMC, and the like. An external PNP is utilized for this LDO to avoid excess on-chip power dissipation at high loads and large differential between BP and output settings. The external PNP device is always connected to the BP line in the application. VSD may also be applied to other system needs within the guidelines of the regulator specifications. The recommended PNP device is the ON Semiconductor NSS12100XV6T1G, which is capable of handling up to 250 mW of continuous dissipation at a minimum footprint and 75 ℃ of ambient. For use cases where up to 500 mW of dissipation is required, the recommended PNP device is the ON Semiconductor NSS12100UW3TCG. For stability reasons a small minimum ESR may be required. At the 1.8 V set point, the VSD regulator can be powered from an external buck regulator (2.2 V typ) for an efficiency advantage and reduced power dissipation in the pass devices.

Table 57. VSD Voltage Control

Parameter	Value	Output Voltage	ILoad max	Input Supply
VSD[2:0]	000	1.80 V	250 mA	BP or External Switcher
	001	2.00 V	250 mA	BP
	010	2.60 V	250 mA	BP
	011	2.70 V	250 mA	BP
	100	2.80 V	250 mA	BP
	101	2.90 V	250 mA	BP
	110	3.00 V	250 mA	BP
	111	3.15 V	250 mA	BP

GEN1, GEN2, AND GEN3 REGULATORS

General purpose LDOs VGEN1, VGEN2, and VGEN3 are provided for expansion of the power tree to support peripheral devices, which could include WLAN, BT, GPS, or other functional modules. All the regulators include programmable set points for system flexibility. At the 1.2 V and 1.5 V set points, both VGEN1 and VGEN2 can be powered from an external buck regulator (2.2 V typ) for an efficiency advantage, and reduced power dissipation in the pass devices. (Note that a connection to BP or the external buck regulator as the input to the regulators is a hardwired board level commitment, and not changed on-the-fly).

Table 58. VGEN1 Control Register Bit Assignments

Parameter	Value	Function	ILoad max[75]	Input Supply
VGEN1[1:0]	00	output = 1.20 V	200 mA	BP or external switcher
	01	output = 1.50 V	200 mA	BP or external switcher
	10	output = 2.775 V	200 mA	BP
	11	output = 3.15 V	200 mA	BP

Notes

75. The max load given for VGEN1MODE = 0 and must take into account the capabilities of the external pass device and operating conditions, to manage its power dissipation. Load capability is 3.0 mA for VGEN1MODE = 1.

Table 59. VGEN2 Control Register Bit Assignments

Parameter	Value	Function	ILoad max [76]	Input Supply
VGEN2[2:0]	000	output = 1.20 V	350 mA	BP or external switcher
	001	output = 1.50 V	350 mA	BP or external switcher
	010	output = 1.60 V	350 mA	BP
	011	output = 1.80 V	350 mA	BP
	100	output = 2.70 V	350 mA	BP
	101	output = 2.80 V	350 mA	BP
	110	output = 3.00 V	350 mA	BP
	111	output = 3.15 V	350 mA	BP

Notes

76. The max load is given for as VGEN2MODE = 0, and must take into account the capabilities of the external pass device and operating conditions to manage its power dissipation. Load capability is 3.0 mA for VGEN2MODE = 1.

VGEN3 has an internal PMOS pass FET which will support loads up to 50 mA. For higher current capability, drive for an external PNP is provided. The external PNP configuration is offered to avoid excess on-chip power dissipation at high loads, and large differential between BP and output settings. The input pin for the integrated PMOS option is shared with the base current drive pin for the PNP option. The external PNP configuration must be committed as a hardwired board level implementation, while the operating mode is selected through the VGEN3CONFIG bit after startup. The VGEN3 is not automatically enabled during the power up sequence, allowing software to properly set the VGEN3CONFIG bit before the regulator is activated. The recommended PNP device is the ON Semiconductor NSS12100XV6T1G, which is capable of handling up to 250 mW of

continuous dissipation at minimum footprint and 75 ℃ of ambient. For use cases where up to 500 mW of dissipation is required, the recommended PNP device is the ON Semiconductor NSS12100UW3TCG. For stability reasons a small minimum ESR may be required.

A short circuit condition will shut down the VGEN3 regulator and generate an interrupt for SCPI.

Table 60. VGEN3 Voltage Control

VGEN3 bit	Output Voltage	ILoad max	
		VGEN3CONFIG = 0 Internal Pass FET	VGEN3CONFIG = 1 External PNP
0	1.80 V	50 mA	200 mA
1	2.90 V	50 mA	200 mA

BATTERY INTERFACE AND CONTROL

The battery management interface is optimized for applications with a single charger connector to which a standard wall charger or a USB host can be connected. It can also support dead battery operation and unregulated chargers.

CHARGE PATH

CHARGER LINE UP

The charge path is depicted in the following diagram.

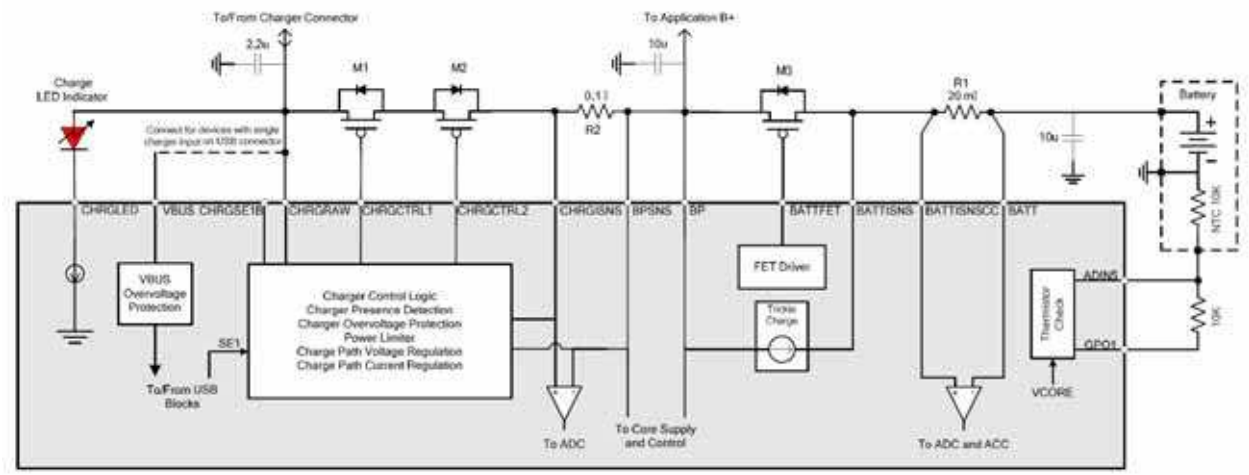


Figure 26. Charge Path Block Diagram

Transistors M1 and M2 control the charge current and provide voltage regulation. The latter is used as the top off change voltage, and as the regulated supply voltage to the application in case of a dead battery operation. In order to support dead battery operation, a so called “serial path” charging configuration including M3 needs to be used. Then in case of a dead battery, the transistor M3 is made non-conducting and the internal trickle charge current charges the battery. If the battery is sufficiently charged, the transistor M3 is made conducting which connects the battery to the application just like during normal operation without a charger. In so called single path charging, M3 is replaced by a short and the pin BATTFET must be floating. Dead battery operation is not supported in this case. Transistors M1 and M2 become non-conducting if the charger voltage is too high. The VBUS must be shorted to CHRGRAW in cases where the wall charger and VBUS voltages are contained on a common pin. A current can be supplied from the battery to an accessory with all transistors M1, M2, and M3 conducting, by enabling the reverse supply mode. An unregulated wall charger configuration can be built, in which case CHRGSE1B must be pulled low. The battery current monitoring resistor R1 and the charge LED indicator are optional. More detail on the battery current monitoring can be found in ADC Subsystem.

The preferred devices for M1 and M2 are Fairchild™ FDZ193P, due to their small package outline and thermal characteristics. The preferred device for M3 is the On Semiconductor NTHS2101P for its low R_{DSON} and small footprint.

CHARGER SIGNALS

The charger uses a number of thresholds for proper operation and will also signal various events to the processor through interrupts. Table 61 summarizes the main signals given, including the control bits. For details see the related sections in this chapter and the SPI bit summary in SPI Bitmap.

Table 61. Main Control Bit Signals

Name	Description
Control Bits	
VCHRG[2:0]	Charger regulator voltage setting
ICHRG[3:0]	Charger regulator current setting
TREN	Internal trickle charger enabling

Table 61. Main Control Bit Signals

Name	Description
THCHKB	Battery thermistor check disable
FETOVRD, FETCTRL	SPI control over BATTFET pin (M3) FETOVRD: 0 = BATTFET output are controlled by hardware 1 = BATTFET controlled by the state of the FETCTRL bit FETOCTRL: 0 = BATTFET is driven high if FETOVRD is set 1 = BATTFET is driven low if FETOVRD is set
RVRSMODE	Reverse mode enabling 0 = Reverse mode disabled 1 = Reverse mode enabled
PLIM[1:0], PLIMDIS	Power limiter setting and disabling PLIMDIS: 0 = Power limiter enabled 1 = Power limiter disabled
CHRGLEDEN	Charge LED indicator enabling 0 = CHRGLED disabled 1 = CHRGLED enabled
CHGRESTART	Charger state machine restart
CHGAUTOB	Selects between standalone or software controlled charging operation 0 = Standalone charging 1 = Software controlled charging
CHGAUTOVIB	Allows for SPI control over-voltage and current settings in standalone charging mode
CYCLB	Controls charging resume behavior 0 = Enables cycling 1 = Disables cycling
Interrupt and Status bits	
CHGDETI	Charger attach
CHGFAULTI	CHRGRAW over-voltage, excessive power dissipation, timeout, battery out of temperature range
CHGFAULTS[1:0]	Charger fault mode sense bits
CHGENS	Charger enable sense bit
USBOVI	USB over-voltage
CHGSHORTI	Short-circuit detection in reverse mode
CHGREVI	Charger path reverse current, detection based on CHGCURR threshold
CHGCURRI	Charge current threshold, detection based on CHGCURR threshold
CCCVI	Charger path regulation mode, detection based on BATTCYCL threshold
CHRGSE1BI	Wall Charger Detect
CHRGSE1BS	CHRSE1B pin sense
CHRGSSS	Charger configuration sense, serial versus single. A logic 1 indicates a serial path.
Thresholds	
CHGCURR	CHRGISNS-BPSNS at 35 mA flowing into phone, used for end of charge detection, charger removal and charge current reversal
BATTMIN	BATT at 3.0 V, used to increase charge current (40/80 mA and 80/560 mA), detect a dead battery insertion while charging
BPON	BP at 3.2 V, used to allow turn on when charging from USB, closes M3 when in serial path
BATTON	BATT at 3.4 V, used to allow turn on when charging from USB, closes M3 when in serial path
BATTCYCL	BPSNS at 98% of charger voltage setting, used to restart charging, used by CCCVI

BUILDING BLOCKS AND FUNCTIONS

The battery management interface consists of several building blocks and functions as depicted in the block diagram shown in the previous paragraph. These building blocks and functions are described below while the charger operation is described in the next section.

CHARGE PATH REGULATOR

The M1 and M2 are permanently used as a combined pass device for a super regulator, with a programmable output voltage and programmable current limit.

The voltage loop consists of M1, M2, and an amplifier with voltage feedback taken from the BPSNS pin. The value of the sense resistor is of no influence on the output voltage. The output voltage is programmable by SPI through VCHRG[2:0] bits.

Table 62. Charge Path Regulator Voltage Settings

VCHRG[2:0]	Charge Regulator Output Voltage (V)
000	3.800
001	4.100
010	4.150
011 (default)	4.200
100	4.250
101	4.300
110	4.375
111	4.450

The current loop is composed of the M1 and M2 as control elements, the external sense resistor, a programmable current limit, and an amplifier. The control loop will regulate the voltage drop over the external resistor. The value of the external resistor therefore is of influence on the charge current. The charge current is programmable by SPI through ICHRG[3:0] bits. Each setting corresponds to a common use case. Software controlled pulsed charging can be obtained by programming the current periodically to zero.

Table 63. Charge Path Regulator Current Limit Settings

ICHRG[3:0]	Charge Regulator Current Limit (mA)	Specific Use Case
0000	0.0	Off
0001	80	Standalone Charging Default for pre-charging, USB charging, and LPB
0010	240	
0011	320	
0100	400	Advised setting for USB charging with PHY active
0101	480	
0110	560	Standalone Charging Default
0111	640	
1000	720	
1001	800	
1010	880	
1011	960	
1100	1040	
1101	1200	High Current Charger
1110	1600	High Current Charger
1111	Fully On – M3 Open	Externally Powered

Table 64. Charge Path Regulator Characteristics

Parameter	Condition	Min	Typ	Max	Units
Input Operating Voltage	CHRGRAW	BATTMIN	–	5.6	V
Output voltage trimming accuracy	VCHRG[2:0] = 011 Charge current 50 mA at T = 25 ℃	–	–	0.35	%
Output Voltage Spread	VCHRG[2 :0] = 011, 1xx				
	Charge current 1.0 to 100 mA	-1.5	–	1.5	%
	Charge current > 100 mA and above	-3.0	–	1.5	%
Current Limit Tolerance(77)	ICHRG[3:0] =0 001	68	80	92	mA
	ICHRG[3:0] = 0100	360	400	440	mA
	ICHRG[3:0] = 0110	500	560	620	mA
	All other settings	–	–	15	%
Start-up Overshoot	Unloaded	–	–	2.0	%
Configuration					
Input Capacitance	CHRGRAW (78)	–	2.2	–	µF
Load Capacitor	BPSNS (78)	10	–	4.7	µF
Cable Length	(79)	-	–	3.0	m

Notes
77. Excludes spread and tolerances due to board routing and 100 mOhm sense resistor tolerances.
78. An additional derating of 35% is allowed.
79. This condition applies when using an external charger with a 3.0 m long cable.

OVER-VOLTAGE PROTECTION

In order to protect the application, the voltage at the CHRGRAW pin is monitored. When crossing the threshold, the charge path regulator will be turned off immediately, by opening M1 and M2, while M3 gets closed. When the over-voltage condition disappears for longer than the debounce time, charging will resume and previously programmed SPI settings will be reloaded. An interrupt CHGFAULTI is generated with associated CHGFAULTM mask bit with the CHGFAULTS[1:0] bits set to 01.

In order to ensure immediate protection, the control of M1, M2, and M3 occurs real-time, so asynchronously to the charger state machine. As a result, for over-voltage conditions of up to 30 µs, the charger state machine may not always end up in the over-voltage fault state, and therefore an interrupt may not always be generated.

Table 65. Charger Over-voltage Protection Characteristics

Parameter	Condition	Min	Typ	Max	Units
Over-voltage Comparator High Voltage Threshold	High to Low, Low to High	16	–	20	V
Over-voltage Comparator Debounce Time	High to Low	–	10	–	ms

The VBUS pin is also protected against over-voltages. This will occur at much lower levels for CHRGRAW. When a VBUS over-voltage is detected the internal circuitry of the USB block is disconnected. A USBOVI is generated in this case. For more details see Connectivity.

When the maximum voltage of the IC is exceeded, damage will occur to the IC and the state of M1 and M2 cannot be guaranteed. If the user wants to protect against these failure conditions, additional protection will be required.

POWER DISSIPATION

Since the charge path operates in a linear fashion, the dissipation can be significant and care must be taken to ensure that the external pass FETs M1 and M2 are not over dissipating when charging. By default, the charge system will protect against this by a built-in power limitation circuit. This circuit will monitor the voltage drop between CHRGRAW and CHRGISNS, and the current through the external sense resistor connected between CHRGISNS and BPSNS. When required,.a duty cycle is applied to the M1 and M2 drivers and thus the charge current, in order to stay within the power budget. At the same time M3 is forced to conduct to keep the application powered. In case of excessive supply conditions, the power limiter minimum duty cycle may not be sufficiently small to maintain the actual power dissipation within budget. In that case, the charge path will be disabled and the CHGFAULTI interrupt generated with the CHGFAULTS[1:0] bits set to 01.

The power budget can be programmed by SPI through the PLIM[1:0] bits. The power dissipation limiter can be disabled by setting the PLIMDIS bit. In this case, it is advised to use close software control to estimate the dissipated power in the external pass FETs. The power limiter is automatically disabled in serial path factory mode and in reverse mode.

Since a charger attachment can be a Turn-on event when a product is initially in the Off state, any non-default settings that are intended for PLIM[1:0] and PLIMDIS, should be programmed early in the configuration sequence, to ensure proper supply conditions adapted to the application. To avoid any false detection during power up, the power limiter output is blanked at the start of the charge cycle. As a safety precaution though, the power dissipation is monitored and the desired duty cycle is estimated. When this estimated duty cycle falls below the power limiter minimum duty cycle, the charger circuit will be disabled.

Table 66. Charger Power Dissipation Limiter Control

PLIM[1:0]	Power Limit (mW)
00 (default)	600
01	800
10	1000
11	1200

Table 67. Charger Power Dissipation Limiter Characteristics

Parameter	Condition	Min	Typ	Max	Units
Power Limiter Accuracy	Up to 2x the power set by PLIM[1:0]	–	–	15	%
Power Limiter Control Period		–	500	–	ms
Power Limiter Blanking Period	Upon charging enabling	–	1500	–	ms
Power Limiter Minimum Duty Cycle		–	10	–	%

REVERSE SUPPLY MODE

The battery voltage can be applied to an external accessory via the charge path, by setting the RVRSMODE bit high. The current through the accessory supply path is monitored via the charge path sense resistor R2, and can be read out via the ADC. The accessory supply path is disabled and an interrupt CHGSHORTI is generated when the slow or fast threshold is crossed. The reverse path is disabled when a current reversal occurs and an interrupt CHREVI is generated.

Table 68. Accessory Supply Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
Short-circuit Current Slow Threshold		500	–	–	mA
Slow Threshold Debounce Time		–	1.0	–	ms
Short-circuit Current Fast Threshold		–	–	1840	mA
Fast Threshold Debounce Time		–	100	–	µs
Current Reversal Threshold	Current from Accessory	–	CHGCURR	–	mA

INTERNAL TRICKLE CHARGE CURRENT SOURCE

An internal current source between BP and BATTISNS provides small currents to the battery in cases of trickle charging a dead battery. As can be seen under the description of the standalone charging, this source is activated by the charger state machine, and its current level is selected based on the battery voltage. The source can also be enabled in software controlled charging mode by setting the TREN bit. This source cannot be used in single path configurations because in that case, BATTISNS and BP are shorted on the board.

Table 69. Internal Trickle Charger Control

BATT	Trickle Charge Current (mA)
0 < BATT < BATTMIN	40
BATTMIN < BATT < BATTON	80

Table 70. Internal Trickle Charger Characteristics

Parameter	Condition	Min	Typ	Max	Units
Trickle Charge Current Accuracy		–	–	30	%
Operating Voltage	BATTISNS	0.0	–	–	V
	BP-BATTISNS	1.0	–	–	V
Extended Operating Range [80]	BP-BATTISNS	0.3	–	–	V

Notes
80. The effective trickle current may be significantly reduced

CHARGER DETECTION AND COMPARATORS

The charger detection is based on three comparators. The “charger valid” monitors CHRGRAW, the “charger presence” that monitors the voltage drop between CHRGRAW and BPSNS, and the “CHGCURR” comparator that monitors the current through the sense resistor connected between CHRGISNS and BPSNS. A charger insertion is detected based on the charger presence comparator and the “charger valid” comparator both going high. For all but the lowest current setting, a charger removal is detected based on both the “charger presence” comparator going low and the charger current falling below CHGCURR. In addition, for the lowest current settings or if not charging, the “charger valid” comparator going low is an additional cause for charger removal detection. The table below summarizes the charger detection logic.

Table 71. Charger Detection

Setting ICHRG[3:0]	Charger Valid Comparator	Charger Presence Comparator	CHGCURR Comparator	Charger Detected
0000, 0001	0	X	X	No
	1	0	X	No
	1	1	X	Yes
Other Settings	X	0	0	No
	X	1	X	Yes
	X	X	1	Yes

In addition to the aforementioned comparators, three more comparators play a role in battery charging. These comparators are “BATTMIN”, which monitors BATT for the safe charging battery voltage, “BATTON”, which monitors BATT for the safe operating battery voltage, and “BATTCYCL”, which monitors BPSNS for the constant current to constant voltage transition. The BATTMIN and BATTON comparators have a normal and a long (slow) debounced output. The slow output is used in some places in the charger flow to provide enough time to the battery protection circuit to reconnect the battery cell.

Table 72. Charger Detectors Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
BATTMIN Threshold	At BATT	2.9	–	3.1	Volts
BATTON Threshold	At BATT	3.3	–	3.5	Volts
BATTCYCL Threshold	At BPSNS relative to VCHRG[2:0]	–	98	–	%
Charger Presence	CHRGRAW-BPSNS	10	–	50	mV
Charger Valid	CHRGRAW	–	3.8	–	V
CHGCURR Threshold	CHRGISNS-BPSNS, current from charger	10	–	50	mA

Table 72. Charger Detectors Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Debounce Period	BATTMIN, BATTON rising edge (normal	–	32	–	ms
	BATTMIN, BATTON rising edge (slow)	–	1.0	–	s
	BATTMIN falling edge (slow)	–	1.0	–	s
	BATTMIN falling edge (fast)	–	1.0	–	s
	BATTCYCL dual edge	–	100	–	ms
	CHGCURR	–	1.0	–	ms
	Charger Detect dual edge	–	100	–	ms

Crossing the thresholds BATTCYCL and CHGCURR will generate the interrupts CCCVI and CHGCURRI respectively. These interrupts can be used as a simple way to implement a three-bar battery meter.

BATTERY THERMISTOR CHECK CIRCUITRY

A battery pack may be equipped with a thermistor, which value decreases over temperature (NTC). The relationship between temperature T (in Kelvin) and the thermistor value (RT) is well characterized and can be described as RT = R0*e^(B*(1/T-1/T0), with T0 being room temperature, R0 the thermistor value at T0 and B being the so called B-factor which indicates the slope of the thermistor over temperature. In order to read out the thermistor value, it is biased from GPO1 through a pull-up resistor R_{PU}. See also the ADC chapter. The battery thermistor check circuit compares the fraction of GPO1 at ADIN5 with two preset thresholds, which correspond to 0 and 45 °C, see Table 73. Charging is generally allowed when the thermistor is within the range, see next section for details.

Table 73. Battery Thermistor Check Main Characteristics

Temperature Threshold	Voltage at ADIN5	Corresponding Resistor Values		Corresponding Temperature (in °C) *		
		Rpu	RT	B=3200	B=3500	B=3900
T_{LOW}	24/32 * GPO1	10 k	30 k	-3.0	0.0	+2.0
T_{HIGH}	10/32 * GPO1	10 k	4.5 k	+49	+46	+44

CHARGE LED INDICATOR

Since normal LED control via the SPI bus is not always possible in the charging mode, an 8.0 mA max current sink is provided at the CHRGLED pin for an LED connected to CHRGRAW.

The LED will be activated when standalone charging is started, and will remain under control of the state machine also when the application is powered on. At the end of charge, the LED is automatically disabled. Through the CHRGLEDEN bit, the LED can be forced on. In software controlled charging, the LED is under full control of this CHRGLEDEN bit.

Table 74. Charge LED Drivers Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
Trickle LED current	CHRGLED = 2.5 V	–	–	8.0	mA
	CHRGLED = 0.7 V	5.0	–	–	mA

Notes
81. Above conditions represent respectively a USB and a collapsed charger case

Table 75. Charge LED Driver Control

CHRGLEDEN	CHRGLED
0 (default)	Auto
1	On

CHARGER OPERATION

USB CHARGING

The USB VBUS line in this case, is used to provide a supply within the USB voltage limits and with at least 500 mA of current drive capability.

When trickle charging from the USB cable, it is important not to exceed the 100 mA, in case of a legacy USB bus. The appropriate charge current level ICHRG[2:0] = (0001) is 80 mA typical which accounts for the additional current through the charge LED indicator.

WALL CHARGING

No distinction can be made between a USB Host or a wall charger. Therefore, when attaching a wall charger, the CHRGSE1B pin must be forced low as a charger attach indicator. The CHRGSE1B pin has a built-in weak pull-up to VCORE. In the application, this pin is preferably pulled low, with for instance an NPN of which the base is pulled high through a resistor to CHRGRAW. The state of the CHRGSE1B pin is reflected through the CHRGSE1BS bit. When CHRGSE1B changes state a CHRGSE1BI is generated. No specific debounce is applied to the CHRGSE1B detector.

Table 76. Charger Detector Characteristics

Parameter	Condition	Min	Typ	Max	Units
CHRGSE1B Pull-up	To VCORE	–	100	–	kOhm
Logic Low		0.0	–	0.3	V
Logic High		1.0	–	VCORE	V

If an application is to support wall chargers and USB on separate connectors, it is advised to separate the VBUS and the CHRGRAW on the PCB. For these applications, charging from USB is no longer possible. For proper operation, a 120 kOhm pull-down resistor should be placed at VBUS.

STANDALONE CHARGING

A standalone charge mode of operation is provided to minimize software interaction. It also allows for a completely discharged battery to be revived without processor control. This is especially important when charging from a USB host or when in single path configuration (M3 replaced by short, BATTFET floating). Since the default voltage and current setting of the charge path regulator may not be the optimum choice for a given application, these values can be reprogrammed through the SPI if the CHGAUTOVIB bit is set. Note that the power limiter can be programmed independent of this bit being set.

Upon connecting a USB host to the application with a dead battery, the trickle cycle is started and the current set to the lowest charge current level (80 mA). When the battery voltage rises above the BATTON = 3.4 V threshold, a power up sequence is automatically initiated. The lowest charge current level remains selected until a higher charge current level is set through the SPI after negotiation with the USB host. In case of a power up failure, a second power up will not be initiated to avoid an ambulance mode, the charger circuitry will though continue to charge. The USB dead battery operation following the low-power boot scheme is described further in this chapter.

Upon connecting a charger to an application with a dead battery the behavior will be different for serial path and single path configurations.

In serial path (M3 present), the application will be powered up with the current through M1M2 set to 500 mA minimum. The internal trickle charge current source will be enabled, set to its lowest level (40 mA) up to BATTMIN, followed by the highest setting (80 mA). The internal trickle charge current is not programmable, but can be turned off by the SPI. In this mode, the voltage and current regulation to BP through the external pass devices M1M2 can be reprogrammed through the SPI. Once the battery is greater than BATTON, it will be connected to BP and further charged through M1/M2 at the same time as the application.

In single path (M3 replaced by a short, BATTFET floating), the battery (and therefore BP) is below the BPON threshold. This will be detected and the external charge path will be used to precharge the battery, up to BATTMIN at the lowest level (80 mA), and above at the 500 mA minimum level. Once exceeding BPON, a turn on event is generated and the voltage and current levels can be reprogrammed.

When in the serial path and upon initialization of the charger circuitry, and it appears BP stays below BPON, the application will not be powered up, and the same charging scheme is followed as for single path.

The precharge will timeout and stop charging, in case it did not succeed in raising the battery to a high enough level: BATTON for internal precharge, external precharge in the case of USB, and BPON for the external precharge, in case of a charger. This is a fault condition and is flagged to the processor by the CHGFAULTI interrupt, and the CHGFAULTS[1:0] bits are set to 10.

The charging circuit will stop charging and generate a CHGCURRI interrupt after the battery is fully charged. This is detected by the charge current dropping below the CHGCURR limit. The charger automatically restarts if the battery voltage is below BATTCYCL. Software can bypass this cyclic mode of operation by setting the CYCLB bit. Setting the bit does not prevent interrupts to be generated.

During charging, a charge timer is running. When expiring before the CHGCURR limit is reached, the charging will be stopped and an interrupt generated. The charge timer can be reset before it expires by setting the self clearing CHGTMRRST bit. After expiration, the charger needs to be restarted. Proper charge termination and restart is a relatively slow process. Therefore in both of the previous cases, the charging will rapidly resume, in case of a sudden battery bounce. This is detected by BP dropping below the BATTON threshold.

Out of any state and after a timeout, the charger state machine can be restarted by removing and reapplying the charger. A software restart can also be initiated by setting the self clearing CHGRESTART bit.

The state of the charger logic is reflected by means of the CHGENS bit. This bit is therefore a 1 in all states of the charger state machine, except when in a fault condition or when at the end of charge. In low-power boot mode, the bit is not set until the ACKLPB bit is set. This also means that the CHGENS bit is not cleared when the power limiter interacts, or when the battery temperature is out of range. The charge LED At CHRGLED follows the state of the CHGENS bit with the exception that software can force the LED driver on.

The detection of a serial path versus a single path is reflected through the CHRGSSS bit. A logic 1 indicates a serial path. In cases of single path, the pin BATTFET must be left floating.

The charging circuit will stop charging, in case the die temperature of the IC exceeds the thermal protection threshold. The state machine will be re-initiated again when the temperature drops below this threshold.

Table 77. Charger Timer Characteristics

Parameter	Condition	Min	Typ	Max	Units
Charger Timer		–	120	–	min
Precharge Timer	External precharge 80 mA Internal precharge 40/80 mA	–	270	–	min
	External precharge 400/560 mA	–	60	–	min

Table 78. Charger Fault Conditions

Fault Condition	CHGFAULTS[1:0]	CHGFAULTI
Cleared or no fault condition	00	Not generated
Over-voltage at CHRGRAW	01	Rising edge
Excessive dissipation on M1/M2	01	Rising edge
Sudden battery drop below BATTMIN	10	Rising edge
Any charge timeout	10	Rising edge
Out of temperature	11	Dual edge

SOFTWARE CONTROLLED CHARGING

The charger can also be operated under software control. By setting CHGAUTOB = 1, full control of the charger settings is assumed by software. The state machine will no longer determine the mode of charging. The only exceptions to this are a charger removal, a charger over-voltage detection and excessive power dissipation in M1/M2.

For safety reasons, when a RESETB occurs, the software controlled charging mode is exited for the standalone charging operation mode.

In the software controlled charging mode, the internal trickle charger settings can be controlled as well as the M3 operation through FETCTRL (1 = conducting). The latter is only possible if the FETOVRD bit is set. If a sudden drop in BP occurs (BP < BPON) while M3 is open, the charger control logic will immediately close M3 under the condition that BATT > BATTMIN.

FACTORY MODE

In factory mode, power is provided to the application with no battery present. It is not a situation which should occur in the field. The factory mode is differentiated from a USB Host by, in addition to a valid VBUS, a UID being pulled high to the VBUS level during the attach, see Connectivity.

In case of a serial path (M3 present), the application will be powered up with M1M2 fully on. The M3 is opened (non conducting) to a separate BP from BATT. However, the internal trickle charge current source is not enabled. All the charger timers as well as the power limiter are disabled.

In case of a single path (M3 replaced by a short, BATTFET floating), the behavior is similar to a normal charging case. The application will power up and the charge current is set to the 500 mA minimum level. All the internal timers and pre-charger timers are enabled, while only the charger timer and power limiter function are disabled.

In both cases, by setting the CHGAUTOVIB bit, the charge voltage and currents can be programmed. When setting the CHGAUTOB bit the factory mode is exited.

USB LOW-POWER BOOT

USB low-power boot allows the application to boot with a dead battery within the 100 mA USB budget until the processor has negotiated for the full current capability. This mode expedites the charging of the dead battery and allows the software to bring up the LCD display screen with the message “Charging battery”. This is enabled on the IC by hardwiring the MODE pin on the PCB board, as shown in Table 79.

Table 79. MODE Pin Programming

MODE Pin State	Mode
Ground	Normal Operation
VCOREDIG	Low-power Boot Allowed

Below are the steps required for USB low-power booting:

1. First step: detect a potential low-power boot condition, and qualify if it is enabled.
   a) VBUS present and not in Factory Mode (either via a wall charger or USB host, since the IC has no knowledge of what kind of device is connected)
   b) BP<BPON (full power boot if BP>BPON)
   c) Board level enabling of LPB with MODE pin hardwired to VCOREDIG
   d) M3 included in charger system (Serial path charging, not Single). If all of these are true, then LPBS=1 and the system will proceed with LPB sequence. If any are false, LPBS = 0.
2. If LPBS = 0, then a normal booting of the system will take place as follows:
   a) MODE = GND. The INT pin should behave normally, i.e. can go high during Watchdog phase based on any unmasked interrupt. If BP>BATTON, the application will turn on. If BP < BATTON, the PMIC will default to trickle charge mode and a turn on event will occur when the battery is charged above the BATTON threshold. The processor does not support a low-power boot mode, so it powers up normally.
   b) MODE = VCOREDIG. When coming from Cold Start the INT is kept low throughout the watchdog phase. The processor detects this and will boot normally. The INT behavior is becomes 'normal' when entering On mode, and also when entering watchdog phase from warm start.
3. If LPBS = 1, then the system will boot in low-power as follows:
   a) Cold Start is initiated in a “current starved bring-up” limited by the charger system's DAC step ICHRG[3:0] = 0001 to stay within 100 mA USB budget. The startup sequence and defaults as defined in the startup table will be followed. Since VBUS is present the USB supplies will be enabled. The charge LED driver is maintained off.
   b) After the power up sequence, but before entering Watchdog phase, thus releasing the reset lines, the charger DAC current is stepped up to ICHRG[3:0] = 0100. This is in advance of negotiation and the application has to ensure that the total loading stays below the un-negotiated 100 mA limit.
   c) The INT pin is made high before entering watchdog phase and releasing RESETBMCU. All other interrupts are held off during the watchdog phase. The processor detects this and starts up in a Low-power mode at low clock speed.
   d) The application processor will enable the PHY in serial FS mode for enumeration.
   e) If the enumeration fails to get the stepped up current, the processor will bring WDI low. The power tree is shut down, and the charging system will revert to trickle recovery, LPBS reset to 0. (or any subsequent failure: WDI = 0). Also if RESETB transitions to 0 while in LPB (i.e., if BP loading misbehaves and causes a UVDET for example), the system will transition to USB trickle recover, LPBS reset to 0.

f) If the enumeration is successful to get the stepped up current the processor will hold WDI high and continues with the booting procedure.

- When the SPI is activated, the LPB interrupt LPBI can be cleared; other unmasked interrupts may now become active. When leaving watchdog phase for the On mode, the interrupts will work 'normally' even if LPBI is not cleared.
- The SPI bit ACKLPB bit is set to enable the internal trickle charger. The charge LED gets activated. When the battery crosses the BATTMIN threshold the M3.transistor is automatically closed and the battery is charged with the current not taken by the application.
- When BP exceeds BPON, the charger state machine will successfully exit the trickle charge mode. This will make LPBS = 0 which generates a LPBI. This interrupt will inform the processor that a full turn on is allowed. Once this happens the application code is allowed to run full speed.

BATTERY THERMISTOR CHECK OPERATION

By default, the battery thermistor value is taken into account for charging the battery. Upon detection of a supply at CHRGRAW, the core circuitry powers up including VCORE. As soon as VCORE is ready, the output GPO1 is made active high, independently of the state of GPO1EN bit. The resulting voltage at ADIN5 is compared to the corresponding temperature thresholds. If the voltage at ADIN5 is within range, the charging will behave as described thus far, however if out of range the charger state machine will go to a wait state, pause the charge timers, and no current will be sourced to the battery. When the temperature comes back in range, charging is continued again. The actual behavior depends on the configuration the charger circuitry at the moment the temperature range is exceeded.

Table 80. Battery Thermistor Check Charger States

Configuration	State for temperature	State for temperature back in range	
	out of range	ICin “On” State	IC in “Off” State
Internal precharging on a charger	M1M2 = 560 mA / SPI setting, M3 = Open, Itrickle = 0mA	Internal precharge	Initialization
Internal precharging on USB in USB Low-power Boot	M1M2 = 400 mA M3 = Open, Itrickle = 0mA	Low-power Boot Precharge	Initialization
All other non fault charging modes and configurations	M1M2 = 0 mA M3 Closed	Initialization	Initialization

The battery thermistor check can be disabled by setting the THCHKB bit. This is useful in applications where battery packs without thermistor may be used. This bit defaults to '0', which means that initial power up only can be achieved with an already charged battery pack or on a charger, but not on a USB Host without low-power boot support. Alternatively, one can bias ADIN5 to get within the temperature window. Setting the SPI bit to disable the thermistor check will also inhibit the automatic enabling of the GPO1 output. The GPO1 output still remains controllable through GPO1EN. As an additional feature, the charger state machine will end up in an out of temperature state when the die temperature is below -20 °C, independent of the setting of the THCHKB bit.

Notes:

- When using the battery charger as the only source of power, as in a battery-less application, the following precautions should be observed:
- It is still necessary to connect ADIN5 to either VCOREDIG or a midpoint of a divider from GPIO1 to ground since the battery charger will still interpret this voltage as the battery pack thermistor by default.
- Very careful budgeting of the total current consumption and voltage standoff from CHRGRAW to BPSNS must be made, since the power limiter is operational by default, and a battery less system won't have a source of current if the power dissipation limit is reached.
- If operating from a USB host the unit load limit (100mA max.) must still be observed.
- If operating from a “wall charger”, and if there is no battery, there is an period of approximately 85 ms after RESETB is released, but before the current limit is set to a nominal 560 mA. If the total current demand is greater than this limit, the voltage may collapse and RESETB may pulse a few times (depending in part in the system load and dependence on RESETB.) Therefore, at the end of this time, RESETB may or may not be active. It may be necessary to use one of the other turn on events (such as PWRONx) to turn it back on.

ADC SUBSYSTEM

CONVERTER CORE

The ADC core is a 10-bit converter. The ADC core and logic run on 2/3 of the switcher PLL generated frequency, so approximately 2.0 MHz. If an ADC conversion is requested while the PLL was not active, it will automatically be enabled by the ADC. A 32.768 kHz equivalent time base is derived from this to the ADC time events. The ADC is supplied from VCORE. The ADC core has an integrated auto calibration circuit which reduces the offset and gain errors.

The switcher PLL is programmable, see Supplies. When the switcher frequency is changed, the frequency applied to the ADC converter will change accordingly. Although the conversion time is inversely proportional to the PLLX[2:0] setting, this will not influence the ADC performance. The locally derived 32.768 kHz will remain constant in order not to influence the different timings depending on this time base.

INPUT SELECTOR

The ADC has 8 input channels. Table 81 gives an overview of the attributes of the A to D channels.

Table 81. ADC Inputs

Channel	ADA1[2:0] ADA2[2:0]	Signal read	Input Level	Scaling	Scaled Version
0	000	Battery Voltage (BATT)	0 – 4.8 V	/2	0 – 2.4 V
1	001	Battery Current (BATT-BATTISNSCC)	-60 mV – 60 mV (82)	x20	-1.2 – 1.2 V
2	010	Application Supply (BPSNS)	0 – 4.8 V	/2	0 – 2.4 V
3	011	Charger Voltage (CHRGRAW)	0 – 12 V 0 – 20 V	/5 /10	0 – 2.4 V 0 – 2.4 V
4	100	Charger Current (CHRGISNS-BPSNS)	-300 mV – 300 mV (83)	x4	-1.2 – 1.2 V
5	101	General Purpose ADIN5 (Battery Pack Thermistor)	0 – 2.4 V	x1	0 – 2.4 V
6	110	General Purpose ADIN6 Backup Voltage (LICELL)	0 – 2.4 V 0 – 3.6 V	x1 x2/3	0 – 2.4 V 0 – 2.4 V
7	111	General Purpose ADIN7/ADIN7B	0 – 2.4 V	x1	0 – 2.4 V
		General Purpose ADIN7	0 – BP	/2	0 – 2.4 V
		General Purpose ADIN7B	0 – VIOHI	/2	0 – 1.4 V
		Die Temperature	–	–	1.2 – 2.4 V
		UID	0 – 4.8 V	/2	0 – 2.4 V

Notes
82. Equivalent to -3.0 to +3.0 A of current with a 20 mOhm sense resistor
83. Equivalent to -3.0 to +3.0 A of current with a 100 mOhm sense resistor

The above table is valid when setting the bit ADSEL = 0 (default). If setting the bit to a 1, the touch screen interface related inputs are mapped on the ADC channels 4 to 7 and channels 0 to 3 become unused. For more details see the touch screen interface section.

Some of the internal signals are first scaled to adapt the signal range to the input range of the ADC. The charge current and the battery current are indirectly read out by the voltage drop over the resistor in the charge path and battery path respectively. For details on scaling see the dedicated readings section.

In case the source impedance is not sufficiently low on the directly accessible inputs ADIN5, ADIN6, ADIN7, and the muxed GPO4 path, an on chip buffer can be activated through the BUFFEN bit. If this bit is set, the buffer will be active on these specific inputs during an active conversion. Outside of the conversions the buffer is automatically disabled. The buffer will add some offset, but will not impact INL and DNL numbers except for input voltages close to zero.

Table 82. ADC Input Specification

Parameter	Condition	Min	Typ	Max	Units
Source Impedance	No bypass capacitor at input	–	–	5.0	kOhm
	Bypass capacitor at input 10 nF	–	–	30	kOhm
Input Buffer Offset	BUFFEN = 1	-5.0	–	5.0	mV
Input Buffer Input Range	BUFFEN = 1	0.02	–	2.4	V

When considerably exceeding the maximum input of the ADC at the scaled or unscaled inputs, the reading result will return a full scale. It has to be noted that this full scale does not necessarily yield a 1023 DEC reading, due to the offsets and calibration applied. The same applies for when going below the minimum input where the corresponding 0000 DEC reading may not be returned.

CONTROL

The ADC parameters are programmed by the processors via the SPI. Up to two ADC requests can be queued, and locally these requests are arbitrated and executed. When a conversion is finished, an interrupt ADCDONEI is generated. The interrupt can be masked with the ADCDONEM bit.

The ADC can start a series of conversions by a rising edge on the ADTRIG pin or through the SPI programming by setting the ASC bit. The ASC bit will self clear once the conversions are completed. A rising edge on the ADTRIG pin will automatically make the ASC bit high during the conversions.

When started, always eight conversions will take place; either 1 for each channel (multiple channel mode, RAND = 0) or eight times the same channel (single channel mode, bit RAND = 1). In single channel mode, the to be converted channel needs to be selected with the ADA1[2:0] setting. This setting is not taken into account in multiple channel mode.

In order to perform an auto calibration cycle, a series of ADC conversions is started with ADCCAL = 1. The ADCCAL bit is cleared automatically at the end of the conversions and an ADCDONEI interrupt is generated. The calibration only needs to be performed before a first utilization of the ADC after a cold start.

The conversion will begin after a small synchronization error of a few microseconds plus a programmable delay from 1 (default) to 256 times the 32 kHz equivalent time base by programming the bits ATO[7:0]. This delay cannot be programmed to 0 times the 32 kHz in order to allow the ADC core to be initialized during the first 32 kHz clock cycle. The ATO delay can also be included between each of the conversions by setting the ATOX bit.

Once a series of eight A/D conversions is complete, they are stored in a set of eight internal registers and the values can be read out by software (except when having done an auto calibration cycle). In order to accomplish this, the software must set the ADA1[2:0] and ADA2[2:0] address bits to indicate which values will be read out. This is set up by two sets of addressing bits to allow any two readings to be read out from the 8 internal registers. For example, if it is desired to read the conversion values stored in addresses 2 and 6, the software will need to set ADA1[2:0] to 010 and ADA2[2:0] to 110. A SPI read of the A/D result register will return the values of the conversions indexed by ADA1[2:0] and ADA2[2:0]. ADD1[9:0] will contain the value indexed by ADA1[2:0], and ADD2[9:0] will contain the conversion value indexed by ADA2[2:0].

An additional feature allows for automatic incrementing of the ADA1[2:0] and ADA2[2:0] addressing bits. This is enabled with bits ADINC1 and ADINC2. When these bits are set, the ADA1[2:0] and ADA2[2:0] addressing bits will automatically increment during subsequent readings of the A/D result register. This allows for rapid reading of the A/D results registers with a minimum of SPI transactions.

The ADC core can be reset by setting the self clearing ADRESET bit. As a result the internal data and settings will be reset but the SPI programming or readout results will not. To restart a new ADC conversion after a reset, all ADC SPI control settings should therefore be reprogrammed.

DEDICATED READINGS

CHANNEL 0 BATTERY VOLTAGE

The battery voltage is read at the BATT pin at channel 0. The battery voltage is first scaled as V(BATT)/2 in order to fit the input range of the ADC.

Table 83. Battery Voltage Reading Coding

Conversion Code ADDn[9:0]	Voltage at input ADC in V	Voltage at BATT in V
1 111 111 111	2.400	4.800
1 000 010 100	1.250	2.500
0 000 000 000	0.000	0.000

CHANNEL 1 BATTERY CURRENT

The current flowing out of and into the battery can be read via the ADC, by monitoring the voltage drop over the sense resistor between BATT and BATTISNSCC. This function is enabled by setting BATTICON = 1.

The battery current can be read either in multiple channel mode or in single channel mode. In both cases, the battery terminal voltage at BATT, and the voltage difference between BATT and BATTISNS, are sampled simultaneously but converted one after the other. This is done to effectively perform the voltage and current reading at the same time. In multiple channel mode, the converted values are read at the assigned channel. In single channel mode and ADA1[2:0] = 001, the converted result is available in 4 pairs of battery voltage and current reading as shown in Table 84.

Table 84. Battery Current Reading Sequence

ADC Trigger	Signals Sampled	Signal Converted	Readout	Contents
0	BATT, BATT – BATTISNSCC	BATT	Channel 0	BATT
1	–	BATT – BATTISNSCC	Channel 1	BATT – BATTISNSCC
2	BATT, BATT – BATTISNSCC	BATT	Channel 2	BATT
3	–	BATT – BATTISNSCC	Channel 3	BATT – BATTISNSCC
4	BATT, BATT – BATTISNSCC	BATT	Channel 4	BATT
5	–	BATT – BATTISNSCC	Channel 5	BATT – BATTISNSCC
6	BATT, BATT – BATTISNSCC	BATT	Channel 6	BATT
7	–	BATT – BATTISNSCC	Channel 7	BATT – BATTISNSCC

If the BATTICON bit is not set, the ADC will return a 0 reading for channel 1.

The voltage difference between BATT and BATTISNS is first amplified to fit the ADC input range as V(BATT-BATTISNS)*20. Since battery current can flow in both directions, the conversion is read out in 2's complement format. Positive readings correspond to the current flow out of the battery, and negative readings to the current flowing into the battery.

Table 85. Battery Current Reading Coding

Conversion Code, ADDn[9:0]	Voltage at Input, ADC in mV	BATT – BATTISNS in mV	Current through 20 mOhm in mA	Current Flow
0 111 111 111	1200.00	60	3000	From battery
0 000 000 001	2.346	0.117	5.865	From battery
0 000 000 000	0.0	0.0	0.0	–
1 111 111 111	-2.346	-0.117	5.865	To battery
1 000 000 000	-1200.00	-60	3000	To battery

The value of the sense resistor used, determines the accuracy of the result as well as the available conversion range. Note that excessively high values can impact the operating life of the device due to extra voltage drop across the sense resistor.

Table 86. Battery Current Reading Specification

Parameter	Condition	Min	Typ	Max	Units
Amplifier Gain		19	20	21	
Amplifier Offset		-2.0	–	2.0	mV
Sense Resistor		–	20	–	mOhm

CHANNEL 2 APPLICATION SUPPLY

The application supply voltage is read at the BP pin at channel 2. The battery voltage is first scaled as V(BP)/2 in order to fit the input range of the ADC.

Table 87. Application Supply Voltage Reading Coding

Conversion Code ADDn[9:0]	Voltage at input ADC in V	Voltage at BP in V
1 111 111 111	2.400	4.800
1 000 010 101	1.250	2.500
0 000 000 000	0.000	0.000

CHANNEL 3 CHARGER VOLTAGE

The charger voltage is measured at the CHRGRAW pin at channel 3. The charger voltage is first scaled in order to fit the input range of the ADC. If the CHRGRAWDIV bit is set to a 1 (default), then the scaling factor is a divide by 5, when set to a 0 a divide by 10.

Table 88. Charger Voltage Reading Coding

Conversion Code ADDn[9:0]	Voltage at input ADC in V	Voltage at CHGRAW in V, CHRGRAWDIV = 0	Voltage at CHGRAW in V, CHRGRAWDIV = 1
1 101 010 100	2.000	20.000	10.000
0 000 000 000	0.000	0.000	0.000

CHANNEL 4 CHARGER CURRENT

The charge current is read by monitoring the voltage drop over the charge current sense resistor. This resistor is connected between CHRGISNS and BPSNS. The voltage difference is first amplified to fit the ADC input range as V(CHRGISNS-BPSNS)*4. The conversion is read out in a 2's complement format, see Table 89. The positive reading corresponds to the current flow from charger to battery, the negative reading to the current flowing into the charger terminal. Unlike the battery current and voltage readings, the charger current readings are not interleaved with the charger voltage readings, so when RAND = 1 a total of 8 readings are executed. The conversion circuit is enabled by setting the CHRGICON bit to a one. If the CHRGICON bit is not set, the ADC will return a 0 reading for channel 4.

Table 89. Charge Current Reading Coding

Conversion Code ADDn[9:0]	Voltage at input ADC in mV	CHRGISNS – BPSNS in mV	Current through 100 mOhm in mA	Current Flow
0 111 111 111	1200	300.0	3000	To application/battery
0 000 000 001	2.4	0.586	5.865	To application/battery
0 000 000 000	0.0	0.0	0.0	-
1 111 111 111	-2.346	-0.586	5.865	To charger connection
1 000 000 000	-1200	-300.0	3000	To charger connection

The value of the sense resistor used determines not only the accuracy of the result as well as the available conversion range, but also the charge current levels. It is therefore advised not to select another value than 100 mOhm.

CHANNEL 5 ADIN5 AND BATTERY THERMISTOR AND BATTERY DETECT

On channel 5, ADIN5 may be used as a general purpose unscaled input, but in a typical application, ADIN5 is used to read out the battery pack thermistor. The thermistor will have to be biased with an external pull-up to a voltage rail greater than the ADC input range. In order to save current when the thermistor reading is not required, it can be biased from one of the general purpose IO's such as GPO1. A resistor divider network should assure the resulting voltage falls within the ADC input range in particular when the thermistor check function is used, see Battery Thermistor Check Circuitry.

When the application is on and supplied by the charger, a battery removal can be detected by a battery thermistor presence check. When the thermistor terminal becomes high-impedance, the battery is considered being removed. This detection function is available at the ADIN5 input and can be enabled by setting the BATTDETEN bit. The voltage at ADIN5 is compared to the output voltage of the GPO1 driver, and when the voltage exceeds the battery removal detect threshold, the sense bit BATTDETBS is made high and after a debounce the BATTDETBI interrupt is generated.

Table 90. Battery Removal Detect Specification

Parameter	Condition	Min	Typ	Max	Units
Battery Removal Detect Threshold[84]		–	31/32 * GPO1	–	V

Notes
84. This is equivalent to a 10 kOhm pull-up and a 10 kOhm thermistor at -35 ℃.

CHANNEL 6 ADIN6 AND COIN CELL VOLTAGE

On channel 6, ADIN6 may be used as a general purpose unscaled input.

In addition, on channel 6, the voltage of the coin cell connected to the LICELL pin can be read (LICON=1). Since the voltage range of the coin cell exceeds the input voltage range of the ADC, the LICELL voltage is first scaled as V(LICELL)*2/3. In case the voltage at LICELL drops below the coin cell disconnect threshold (see Clock Generation and Real Time Clock), the voltage at LICELL can still be read through the ADC.

Table 91. Coin Cell Voltage Reading Coding

Conversion Code ADDn[9:0]	Voltage at ADC input (V)	Voltage at LICELL (V)
1 111 111 111	2.400	3.6
1 000 000 000	1.200	1.8
0 000 000 000	0.000	0.0

CHANNEL 7 ADIN7 AND ADIN7B, UID AND DIE TEMPERATURE

On channel 7, ADIN7 may be used as a general purpose unscaled input (ADIN7DIV = 0) or as a divide by 2 scaled input (ADIN7DIV = 1). The latter allows converting signals that are up to twice the ADC converter core input range. In a typical application, an ambient light sensor is connected here.

A second general purpose input ADIN7B is available on channel 7. This input is muxed on the GPO4 pin. The input voltage can be scaled by setting the ADIN7DIV bit. In the application, a second ambient light sensor is supposed to be connected here. Note that the GPO4 will have to be configured to allow for the proper routing of GPO4 to the ADC, see General Purpose Outputs.

In addition, on channel 7, the voltage of the USB ID line connected to the UID pin can be read. Since the voltage range of the ID line exceeds the input voltage range of the ADC, the UID voltage is first scaled as V(UID)/2.

Table 92. UID Voltage Reading Coding

Conversion Code ADDn[9:0]	Voltage at ADC input (V)	Voltage at UID (V)
1 111 111 111	2.400	4.80 - 5.25
0 000 000 000	0.000	0.0

Also on channel 7, the die temperature can be read out. The relation between the read out code and temperature is given in Table 93.

Table 93. Die Temperature Voltage Reading

Parameter	Minimum	Typical	Maximum	Unit
Die Temperature Read Out Code at 25 ℃	–	680	–	Decimal
Temperature change per LSB	–	+0.4244 ℃	–	℃/LSB
Slope error	–	–	5.0	%

Table 94. ADC Channel 7 Scaling Selection

ADIN7DIV	ADIN7SEL1	ADIN7SEL0	Channel 7 Routing and Scaling
0	0	0	General purpose input ADIN7, Scaling = 1
1	0	0	General purpose input ADIN7, Scaling = 1 / 2
x	0	1	Die temperature
x	1	0	UID pin voltage, Scaling = 1 / 2
0	1	1	General purpose input ADIN7B, Scaling = 1
1	1	1	General purpose input ADIN7B, Scaling = 1 / 2

ADC ARBITRATION

The ADC converter and its control is based on a single ADC converter core with the possibility to store two requests, and to store both their results as shown in Figure 27. This allows two independent pieces of software to perform ADC requests.

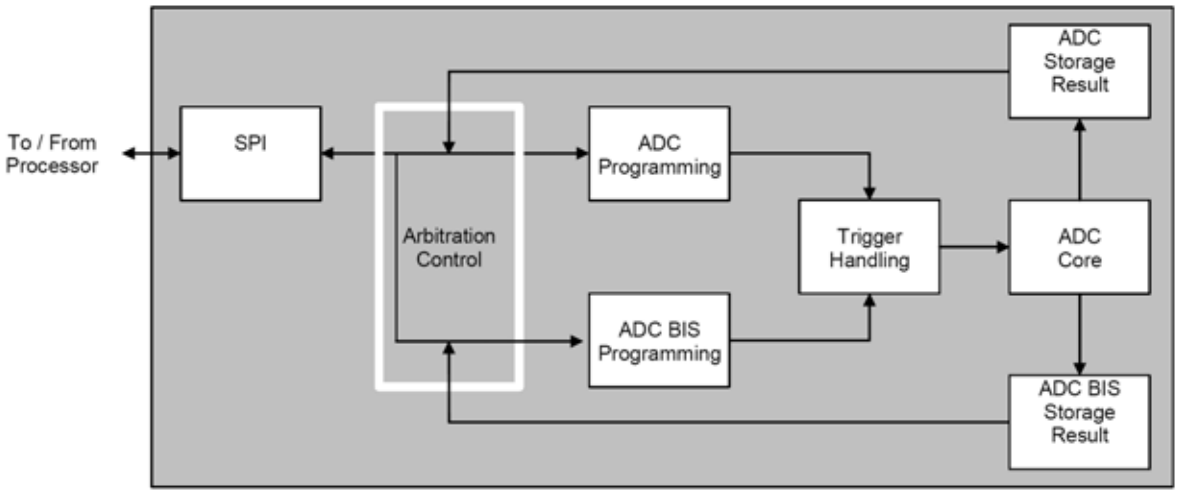


Figure 27. ADC Request Handling

The programming for the two requests, the one to the 'ADC' and to the 'ADC BIS', uses the same SPI registers. The write access to the control of 'ADC BIS' is handled via the ADCBISn bits located at bit position 23 of the ADC control registers, which functions as an extended address bit. By setting this bit to a 1, the control bits which follow are destined for the 'ADC BIS'. ADCBISn will always read back 0 and there is no read access to the control bits related to 'ADC BIS'. The read results from the 'ADC' and 'ADC BIS' conversions are available in two separate registers.

The following diagram schematically shows how the ADC control and result registers are set-up.

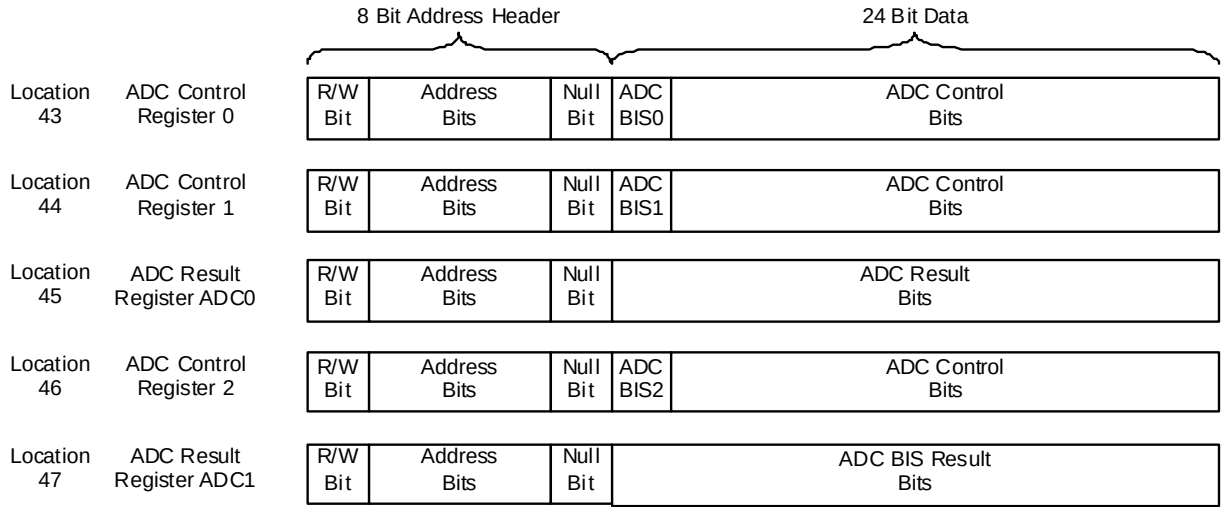


Figure 28. ADC Register Set for ADC BIS Access

There are two interrupts available to inform the processor when the ADC has finished its conversions, one for the standard ADC conversion ADCDONEI, and one for the ADCBIS conversion ADCBISDONEI. These interrupts will go high after the conversion, and can be masked.

When two requests are queued, the request for which the trigger event occurs the first will be converted the first. During the conversion of the first request, an ADTRIG trigger event of the other request is ignored, if for the other request the TRIGMASK bit was set to 1. When this bit is set to 0, the other request ADTRIG trigger event is memorized, and the conversion will take place directly after the conversions of the first request are finished.

The following diagram shows the influence of the TRIGMASK bit. The TRIGMASK bit is particularly of use when an ADC conversion has to be lined up to a periodically ADTRIG initiated conversion. In case of ASC initiated conversions, the TRIGMASK bit is of no influence.

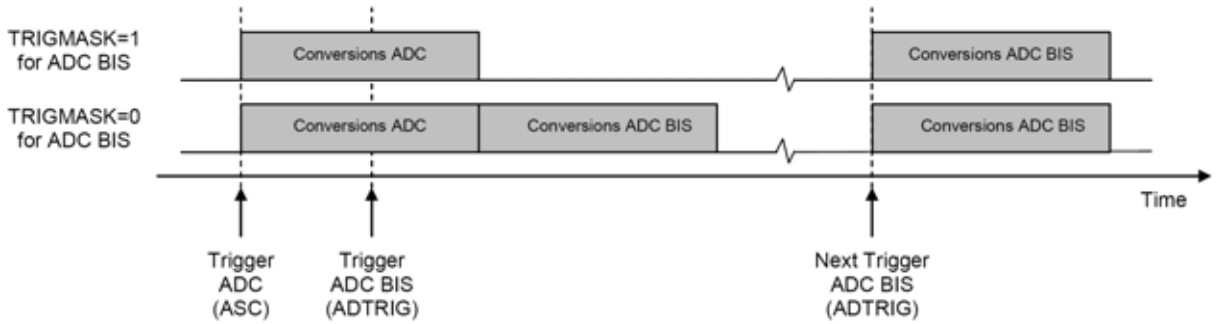


Figure 29. TRIGMASK Functional Diagram

To avoid results of previous conversions getting overwritten by a periodical ADTRIG signal, a single shot function is enabled by setting the ADONESHOT bit to a one. In that case, only at the first following conversion, an ADTRIG trigger event is accepted. ASC events are not affected by this setting. Before performing a new single shot conversion, the ADONESHOT bit first needs to be cleared. Note that this bit is available for each of the conversion requests 'ADC' or 'ADC BIS', so can be set independently.

It is possible to queue two ADTRIG triggered conversions. Both conversions will be executed with a priority based on the TRIGMASK setting. If both conversion requests have identical TRIGMASK settings, priority is given to the 'ADC' conversion over the 'ADC BIS' conversion. Note that the ADONESHOT is also taken into account.

To avoid that the ADTRIG input inadvertently triggers a conversion, the ADTRIGIGN bit can be set which will ignore any transition on the ADTRIG pin. The ADC completely ignores either ADTRIG or ASC pulses while ADEN is low. When reading conversion results, it is preferable to make ADEN = 0.

TOUCH SCREEN INTERFACE

The touch screen interface provides all circuitry required for the readout of a 4-wire resistive touch screen. The touch screen X plate is connected to TSX1 and TSX2 while the Y plate is connected to TSY1 and TSY2. A local supply TSREF will serve as a reference. Several readout possibilities are offered.

In order to use the ADC inputs and properly convert and readout the values, the bit ADSEL should be set to a 1. This is valid for touch screen readings as well as for general purpose reading on the same inputs.

The touch screen operating modes are configured via the TSMOD[2:0] bits show in the following table.

Table 95. Touch Screen Operating Mode

TSMOD2	TSMOD1	TSMOD0	Mode	Description
x	0	0	Inactive	Inputs TSX1, TSX2, TSY1, TSY2 can be used as general purpose ADC inputs
0	0	1	Interrupt	Interrupt detection is active. Generates an interrupt TSI when plates make contact. TSI is dual edge sensitive and 30 ms debounced
1	0	1	Reserved	Reserved for a different interrupt mode
0	1	x	Touch Screen	ADC will control a sequential reading of 2 times a XY coordinate pair and 2 times a contact resistance
1	1	x	Reserved	Reserved for a different reading mode

In inactive mode, the inputs TSX1, TSX2, TSY1, and TSY2 can be used as general purpose inputs. They are respectively mapped on ADC channels 4, 5, 6, and 7.

In interrupt mode, a voltage is applied to the X-plate (TSX2) via a weak current source to VCORE, while the Y-plate is connected to ground (TSY1). When the two plates make contact both will be at a low potential. This will generate a pen interrupt to the processor. This detection does not make use of the ADC core or the TSREF regulator, so both can remain disabled.

In touch screen mode, the XY coordinate pairs and the contact resistance are read.

The X-coordinate is determined by applying TSREF over the TSX1 and TSX2 pins while performing a high-impedance reading on the Y-plate through TSY1. The Y coordinate is determined by applying TSREF between TSY1 and TSY2, while reading the TSX1 pin.

The contact resistance is measured by applying a known current into the TSY1 terminal of the touch screen and through the terminal TSX2, which is grounded. The voltage difference between the two remaining terminals TSY2 and TSX1 is measured by the ADC, and equals the voltage across the contact resistance. Measuring the contact resistance helps in determining if the touch screen is touched with a finger or stylus.

To perform touch screen readings, the processor will have to select the touch screen mode, program the delay between the conversions via the ATO and ATOX settings, trigger the ADC via one of the trigger sources, wait for an interrupt indicating the conversion is done, and then read out the data. In order to reduce the interrupt rate and to allow for easier noise rejection, the touch screen readings are repeated in the readout sequence.

Table 96. Touch Screen Reading Sequence

ADC Conversion	Signals sampled	Readout Address (85)
0	X position	000
1	X position	001
2	Dummy	010
3	Y position	011
4	Y position	100
5	Dummy	101
6	Contact resistance	110
7	Contact resistance	111

Notes

85. Address as indicated by ADA1[2:0] and ADA2[2:0]

The dummy conversion inserted between the different readings is to allow the references in the system to be pre-biased for the change in touch screen plate polarity and will read out as '0'.

Figure 30 shows how the ATO and ATOX settings determine the readout sequence. The ATO should be set long enough so that the touch screen can be biased properly before conversions start.

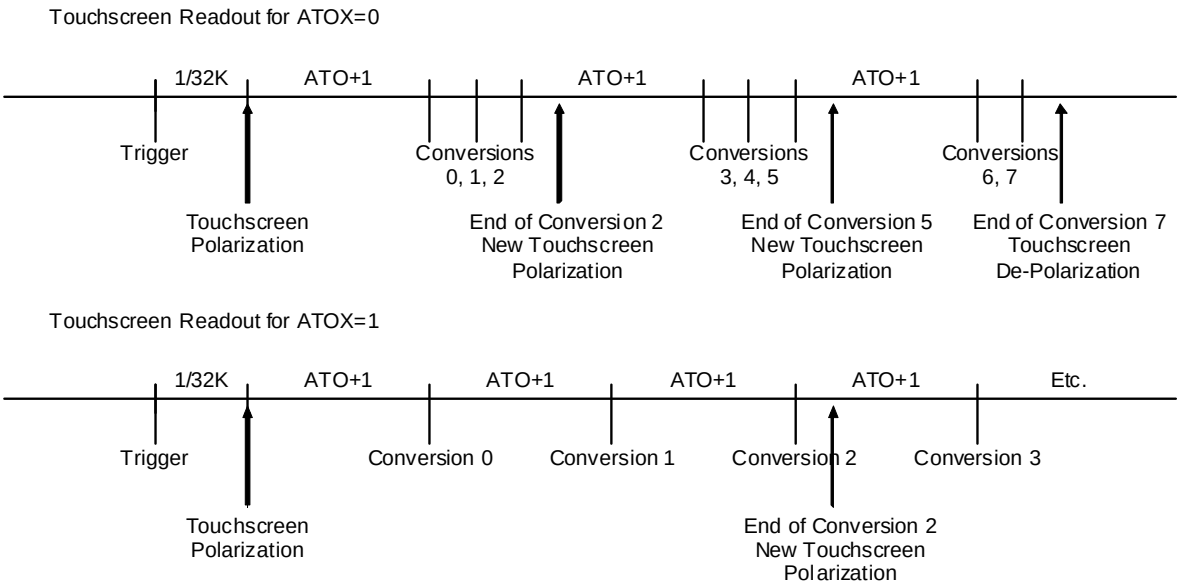


Figure 30. Touch Screen Reading Timing

The main resistive touch screen panel characteristics are listed in Table 5. The switch matrix and readout scheme is designed such that the on chip switch resistances are of no influence on the overall readout. The readout scheme however does not account for contact resistances as present in the touch screen connectors. Therefore, the touch screen readings will have to be calibrated by the user or in the factory where one has to point with a stylus the opposite corners of the screen.

When reading out the X-coordinate, the 10-bit ADC reading represents a 10-bit coordinate with '0' for a coordinate equal to TSX2, and full scale '1023' when equal to TSX1. When reading out the Y-coordinate, the 10-bit ADC reading represents a 10-bit coordinate with '0' for a coordinate equal to TSY2, and full scale '1023' when equal to TSY1. When reading the contact resistance the 10-bit ADC reading represents the voltage drop over the contact resistance created by the known current source multiplied by two.

Table 97. Touchscreen Interface Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Interrupt Threshold for Pressure Application		40	50	60	kOhm
Interrupt Threshold for Pressure Removal		60	80	95	kOhm
Current Source Inaccuracy	Over-temperature	–	–	20	%

The reference for the touch screen is TSREF and is powered from VCORE. In touch screen operation, TSREF is a dedicated regulator. No other loads than the touch screen should be connected here. When the ADC performs non touch screen conversions, the ADC does not rely on TSREF and the reference can be disabled. In applications not supporting touch screen at all, the TSREF can be used as a low current general purpose regulator, or it can be kept disabled and the bypass capacitor omitted. The operating mode of TSREF can be controlled with the TSREFEN bit in the same way as some other general purpose regulators are controlled, see Linear Regulators.

COULOMB COUNTER

As indicated earlier on in this Section, the current into and from the battery can be read out through the general purpose ADC as a voltage drop over the R1 sense resistor. Together with battery voltage reading, the battery capacity can be estimated. A more accurate battery capacity estimation can be obtained by using the integrated Coulomb Counter.

The Coulomb Counter (or CC) monitors the current flowing in/out of the battery by integrating the voltage drop across the battery current sense resistor R1, followed by an A to D conversion. The result of the A to D conversion is used to increase/ decrease the contents of a counter that can be read out by software. This function will require a 10 μF output capacitor to perform

a first order filtering of the signal across R1. Due to the sampling of the A to D converter and the filtering applied, the longer the software waits before retrieving the information from the CC, the higher the accuracy. The capacitor will be connected between the pins CFP and CFM, see Figure 31.

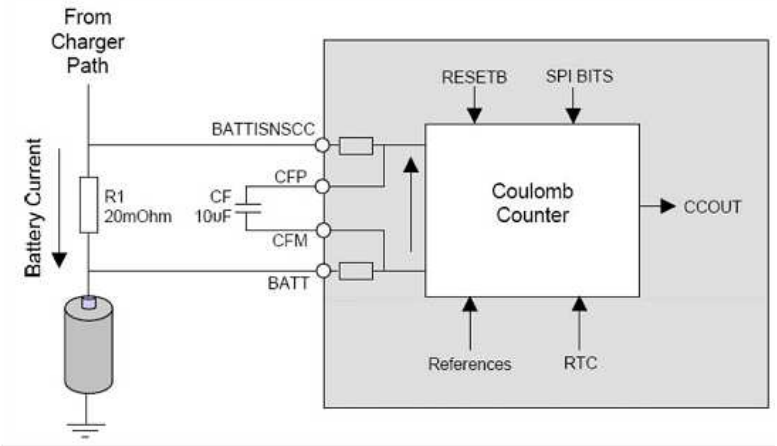


Figure 31. Coulomb Counter Block Diagram

The CC results are available in the 2's complement CCOUT[15:0] counter. This counter is preferably reflecting 1 Coulomb per LSB. As a reminder, 1 Coulomb is the equivalent of 1 Ampere during 1 second, so a current of 20 mA during 1 hour is equivalent to 72C. However, since the resolution of the A to D converter is much finer than 1C, the internal counts are first to be rescaled. This can be done by setting the ONEC[14:0] bits. The CCOUT[15:0] counter is then increased by 1 with every ONEC[14:0] counts of the A to D converter. For example, ONEC[14:0] = 000 1010 0011 1101 BIN = 2621 DEC yields 1C count per LSB of CCOUT[15:0] with R1 = 20 mOhm.

The CC can be reset by setting the RSTCC bit. This will reset the digital blocks of the CC and will clear the CCOUT[15:0] counter. The RSTCC bit gets automatically cleared at the end of the reset period which may take up to 40 μs. The CC is started by setting the STARTCC bit. The CC is disabled by setting this bit low again. This will not reset the CC settings nor its counters, so when restarting the CC with STARTCC, the count will continue.

When the CC is running it can be calibrated. An analog and a digital offset calibration is available. The digital portion of the CC is by default permanently corrected for offset and gain errors. This function can be disabled by setting the CCCALDB bit. However, this is not advisable.

In order to calibrate the analog portion of the CC, the CCCALA bit is set. This will disconnect the inputs of the CC from the sense resistor and will internally short them together. The CCOUT[15:0] counter will accumulate the analog error over time. The calibration period can be freely chosen by the implementer and depends on the accuracy required. By setting the ONEC[14:0] = 1 DEC this process is sped up significantly. By reading out the contents of the CCOUT[15:0] and taking into account the calibration period, software can now calculate the error and account for it. Once the calibration period has finished the CCCALA bit should be cleared again.

One optional feature is to apply a dithering to the A to D converter to avoid any error in the measurement due to repetitive events. To enable dithering the CCDITHER bit should be set. In order for this feature to be operational, the digital calibration should remain enabled, so the CCCALDB bit should not be set.

Table 98. Coulomb Counter Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Sense resistor R1	Placed in Battery path of Charger system	-–	20	–	mΩ
Sensed current	Through R1	±1.0	–	±3000	mA
On consumption	CC active	–	10	20	μA
Resolution	1LSB Increment	–	381.47	–	μC

As follows from the previous description, using the CC requires a number of programming steps. A typical programming example is given below.

1. SPI Access 1: Initialize
   - Reg 9: Write STARTCC= 1, RSTCC = 1, CCCALA = 1, CCDITHER = 1, CCCALDB = 0
   - RSTCC will be self clearing
   - Register 10 is NOT to be programmed since bydefault the ONEC[14:0] scaler is set to 1
2. Wait for analog calibration period
3. SPI Access 2: Set scaler
   - Reg 10: Write ONEC to desired value for CC use, for instance 2621DEC
4. SPI Access 3: Read analog offset and reset CC
   - Reg 9: Write STARTCC= 1, RSTCC = 1, CCCALA = 0, CCDITHER = 1, CCCALDB = 0
   - During the write access, on the MISO read line the most recent CCOUT[15:0] is available
   - RSTCC will be self clearing

From this point on the ACC is running properly and CCOUT[15:0] reflects the accumulated charge. In order to be sure the contents of the CCOUT[15:0] are valid, a CCFAULT bit is available. CCFAULT will be set '1' if the CCOUT content is no longer valid, this means the bit gets set when a fault condition occurs and stays latched till cleared by software. There is no interrupt associated to this bit. The following fault conditions are covered.

Counter roll over: CCOUT[15:0] = 8000HEX

This occurs when the contents of CCOUT[15:0] go from a negative to a positive value or vice versa. Software may interpret incorrectly the battery charge by this change in polarity. When CCOUT[15:0] becomes equal to 8000HEX the CCFAULT is set. The counter stays counting so its contents can still be exploited.

Battery removal: 'BP<UVDET'

When removing and replacing the battery, the contents of the counter are no longer valid. A battery removal is characterized by the input supply to the IC dropping below the under voltage detect threshold, so BP<UVDET. To avoid false detection due to short power cuts, the CCFAULT is set only after a long debounce of 1 second.

Battery removal when charging: BATTDETBS = 1

The battery removal detection as described previously, is not applicable when charging, since the charger will continue to supply the application and the BP will not drop below UVDET. To still detect a battery removal, one can use the battery detect function as described in the channel description earlier in this chapter. When the sense bit BATTDETBS becomes a 1, the CCFAULT is set only after a long debounce of 1 second.

CONNECTIVITY

USB INTERFACE

The MC13892 contains the regulators required to supply the PHY contained in the i.MX51, i.MX37, i.MX35, and i.MX27 processors. The regulators used to power the external PHY in the i.MX51 and i.MX37 are VUSB, VUSB2, and VUSB for the i.MX35 and i.MX27 processors. The MC13892 also provides the 5.0 V supply for USB OTG operation. The USB interface may be used for portable product battery charging (refer to Battery Interface and Control for more details on the charging system). Finally included are comparators/detectors for VBUS and ID detection. The USB interface is illustrated in the following diagram.

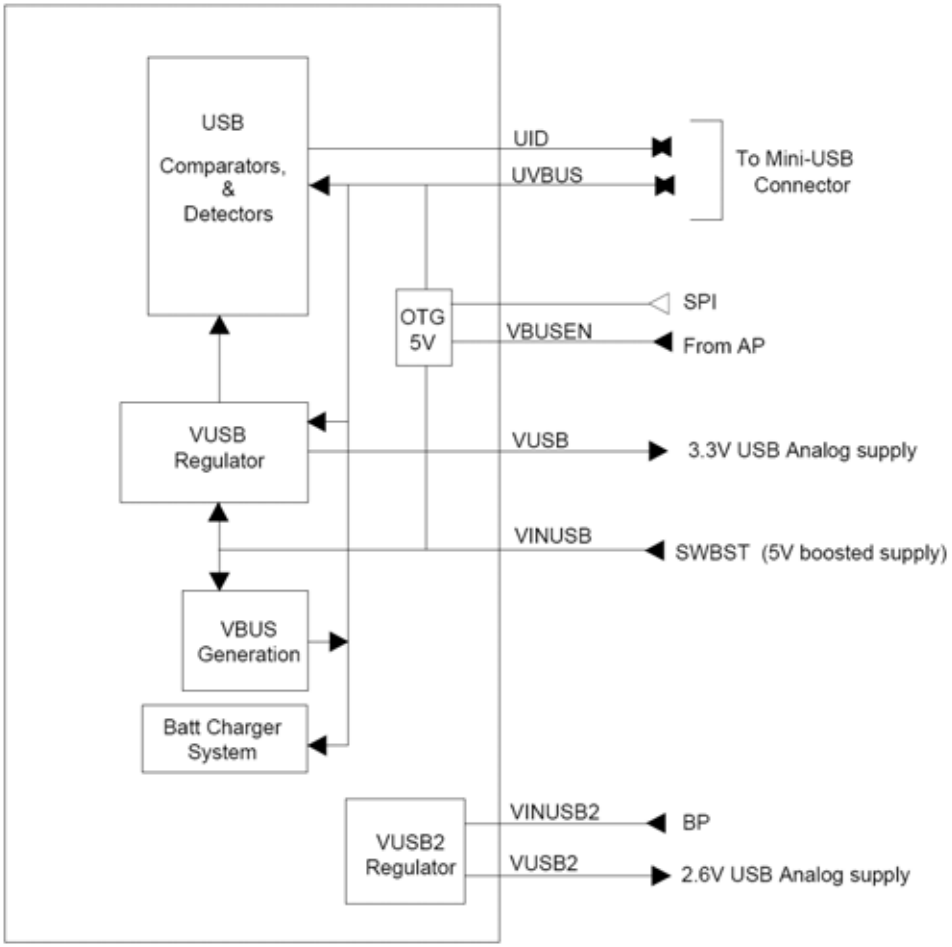


Figure 32. USB Interface

SUPPLIES

The VUSB regulator is used to supply 3.3 V to the external USB PHY. The UVBUS line of the USB interface is supplied by the host in the case of host mode operation, or by the integrated VBUS generation circuit, in the case of USB OTG mode operation. The VBUS circuit is powered from the SWBST boost supply to ensure OTG current sourcing compliance through the normal discharge range of the main battery.

The VUSB regulator can be supplied from the UVBUS wire of the cable when supplied by a host in the case of host mode operation, or by the SWBST voltage brought in at the VINUSB pin and internally connected to the VBUS pin for OTG mode operation. The VUSBIN SPI bit is used to make the selection between host or OTG mode operation as defined in Table 99.

Table 99. VUSB Input Source Control

Parameter	Value	Function
VUSBIN	0	Powered by Host: UVBUS powers VUSB
	1	OTG mode: SWBST internally switched to supply the VUSB regulator, and SWBST will drive VBUS from the VUSBIN pin as long as VBUSEN pin is logic high = 1

Notes

86. Note that (VUSBIN = 1 and VBUSEN = 1) only closes the switch between the VINUSB and UVBUS pins, but does not enable the SWBST boost regulator (which should be enabled with OTGSWBSTEN = 1).
87. VUSBIN SPI bit initialized by PUMS2 pin configuration at cold start
PUMS2 = Open, VUSBIN = 0
PUMS2 = Ground, VUSBIN = 1

The VBUSEN pin along with the VUSBIN SPI bit shown in Table 99, control switching SWBST to drive VBUS in OTG mode. When VBUSEN = 1 and VUSBIN = 1, SWBST will be driving the VBUS. In all other cases, the switch from VINUSB to UVBUS will be open. The VUSBIN SPI bit is initialized by the PUMS2 pin configuration at cold start. When the PUMS2 is open the VUSBIN SPI bit will default to 0, and when PUMS2 is grounded the VUSBIN SPI bit will default to 1. When PUMS2 is grounded, the SWBST will also be enabled by default by setting the OTGSWBSTEN bit = 1. Note that (VBUSEN = 1 and VUSBIN = 1) only closes the switch between VINUSB and UVBUS pins, but does not enable SWBST (this needs to be enabled by setting the SPI bit OTGSWBSTEN = 1).

In OTG mode, VUSB and VUSB2 will be automatically enabled by setting the SPI bit VUSBIN to a 1. When SWBST is supplying the UVBUS pin (OTG Mode), it will generate VBUSVALID and BVALID interrupts. These interrupts should not be interpreted as being powered by the host by the software, and the VUSB supply will continue to be supplied by the SWBST output. To prevent the charger from charging in OTG mode, the charger should be put into software controlled mode by setting the CHGAUTOB = 1, and the charge current set to 0 prior to enabling the SWBST to supply the UVBUS pin.

The VUSB regulator defaults to on when PUMS2 = Ground, and is supplied by the SWBST output. If a USB host is attached, the switchover to supply the VUSB input by the USB cable (UVBUS pin) is a manual switchover, which will require the following steps via software to switch over properly: receive BVALID interrupt, disable the VUSB regulator (VUSBEN = 0), change the input VUSB to UVBUS instead of SWBST (set VINUSB = 0), and then enable the VUSB regulator (VUSBEN = 1). It will be up to the processor to determine what type of device is connected, either a USB host or a wall charger, and take appropriate action.

When the PUMS2 = OPEN, the VUSB regulator will default to off, unless 5.0 V is present on the UVBUS pin. If UVBUS is detected during cold start then the VUSB regulator will be enabled and powered on in the sequence, shown in Power Control System, and it will default, which is supplied by the UVBUS pin. If UVBUS is not detected at cold start then the VUSB will default to off. If UVBUS is detected later, the VUSB regulator will be automatically be enabled and supplied from the UVBUS pin.

The VUSB regulator can be enabled independent of OTG or Host Mode by setting the VUSBEN SPI bit The VUSBEN SPI bit is initialized by at startup based on the PUMS2 configuration. With PUMS2 OPEN, the VUSBEN will default to a 1 on power up and will reset to a 1, when either RESETB is valid or VBUS is invalid. This allows the VUSBEN regulator to be enabled automatically if the VUSB regulator was disabled by software. With PUMS2 = GND the VUSBEN bit will be enabled in the power up sequence shown in Power Control System.

Since UVBUS is shared with the charger input at the board level (see Battery Interface and Control), the UVBUS node must be able to withstand the same high voltages as the charger. In over-voltage conditions, the VUSB regulator is disabled. The following tables show the USB supplies.

VUSB2 is implemented with an integrated PMOS pass FET and has a dedicated supply pin VINUSB2. The pin VINUSB2 should always be connected to BP even in cases where the regulators are not used by the application.

Table 100. VUSB2 Voltage Control

Parameter	Value	Function	ILoad max
VUSB2[1:0]	00	output = 2.400 V	50 mA
	01	output = 2.600 V	50 mA
	10	output = 2.700 V	50 mA
	11	output = 2.775 V	50 mA

DETECTION COMPARATORS

VBUS detection and qualification is accomplished with two comparators, detailed in Table 101. Comparator results are used to generate associated interrupts, and sense and masking bits are available through SPI (refer to SPI Bitmap). Comparator thresholds are specified for the minimum detect levels, and bits can be used in combination to qualify a VBUS window. Events are communicated via (INT pin) interrupts and managed through SPI registers to allow the application processor to turn off the PHY.

As described in Battery Interface and Control, the battery charger system is designed to work with the USB system physical connector. The power input is then brought into an end product on the VBUS pin of the USB connector. For fault condition robustness, VBUS over-voltage protection is included to protect the system and flag an over-voltage situation to the processor via the USBOVI interrupt.

Table 101. USB Detect Specifications

Parameter	Condition	Min	Typ	Max	Units
V_{BUS}Valid Comparator trip level		4.4	–	4.65	V
V_{BUS}Valid trip delay	Including the USBI debounce				
	Rising trip delay	20	–	24	ms
	Falling trip delay	8.0	–	12	ms
BVALID Comparator Threshold	Rising and falling edge	4.0	–	4.4	V
BVALID Trip Delay	Rising trip delay for turn on event Falling trip delay for turn on event	20 8.0	– –	40 12	ms
Over-voltage Protection Level	Rising and falling edge	5.6	–	6.0	V
Over-voltage Protection Disconnect Time		–	–	1.0	µs

ID DETECTOR

The ID detector is primarily used to determine if a mini-A or mini-B style plug has been inserted into a mini-AB style receptacle on the application. However, it is also supports two additional modes which are outside of the USB standards: a factory mode and a non-USB accessory mode. The state of the ID detection can be read via the SPI to poll dedicated sense bits for a floating, grounded, or factory mode condition on the UID pin. There are also dedicated maskable interrupts for each UID condition as well.

The ID detector is based on an on-chip pull-up controlled by the IDPUCNTRL bit. If set high the pull-up is a current source, if set low it is a resistor. ID100KPU switches in an additional pull-up from VCORE to UID (independent of IDPUCNTRL). The UID voltage can be read out via the ADC channel ADIN7, see ADC Subsystem.

The ID detector thresholds are listed in Table 102. Further interpretations of non-USB accessory detection may be made for custom vendor applications by evaluation of the ADIN7 conversion reading.

Table 102. ID Detection Thresholds

UID Pin External Connection	UID Pin Voltage	IDFLOATS	IDGNDS	IDFACTORYS	Accessory
Resistor to Ground	0.18 * VCORE < UID < 0.77 * VCORE	0	1	0	Non-USB accessory is attached (per CEA-936-A spec)
Grounded	0 < UID < 0.12 * VCORE	0	0	0	A type plug (USB Default Slave) is attached (per CEA-936-A spec)
Floating	0.89 * VCORE < UID < VCORE	1	1	0	B type plug (USB Host, OTG default master or no device) is attached.
Voltage Applied	3.6V < UID [88]	1	1	1	Factory mode

Notes
88. UID maximum voltage is 5.25 V

Table 103. USB OTG Specifications

Parameter	Condition	Min	Typ	Max	Units
VBUS Input Impedance	As A_device	40	-	100	kΩ
UID 220K Pull-up (89)	IDPUCNTRL = 0, Resistor to VCORE	132	220	308	kΩ
UID Pull-up (89)	IDPUCNTRL = 1, Current source from VCORE	4.75	5.0	5.25	µA
UID Parallel Pull-up (89)	ID100KPU = 1, Resistor to VCORE	60	100	140	kΩ

Notes
89. Note that the UID Pull-ups are not mutually exclusive of each other; they are independently controlled by their enable bits and thus multiple pull-ups can be engaged simultaneously.

LIGHTING SYSTEM

The lighting system includes backlight drivers for main display, auxiliary display, and keypad. The backlight LEDs are configured in series. Three additional drivers are provided for RGB or general purpose signaling.

BACKLIGHT DRIVERS

The backlight drivers LEDMD, LEDAD and LEDKP are independent current sink channels. Each driver channel features programmable current levels via LEDx[2:0] as well as programmable PWM duty cycle settings with LEDxDC[5:0]. By a combination of level and PWM settings, the backlight intensity can be adjusted, or a soft start and dimming feature can be implemented. The on period of the serial LED backlight drivers will be adapted to take into account that the serial LED switcher startup time is longer than one half the minimum of the period of the backlight drivers.

When applying a duty cycle of less than 100% the backlight drivers will be turned on and off at a repetition rate high enough to avoid flickering and or beat frequencies with the different types of displays. Also, to avoid high frequency spur coupling in the application, the switching edges of the output drivers are softened.

The current level is programmable in a low range mode and in a high range mode through the LEDxHI bit. This facilitates the current setting, in case two or more serial LED strings are connected in parallel to the same driver or when using super bright LEDs.

Table 104. Backlight Drivers Current Programming

LEDx[2:0](90)	LEDx Current Level (mA)	
	LEDxHI = 0	LEDxHI = 1
000	0	0
001	3	6
010	6	12
011	9	18
100	12	24
101	15	30
110	18	36
111	21	42

Notes
90. “x Represents MD, AD and KP

Table 105. Backlight Drivers Duty Cycle Programming

LEDxDC[5:0](91)	Duty Cycle
000000	0/32, Off
000001	1/32
…	…
010000	16/32
…	…
011111	31/32
100000 to 111111	32/32, Continuously On

Notes
91. “x” represents MD, AD, or KP

Ramp up and ramp down patterns are implemented in hardware to reduce the burden of real time software control via the SPI to orchestrate dimming and soft start lighting effects. Ramp patterns for each of the drivers is accessed with the corresponding LEDxRAMP bit.

The ramp itself is generated by increasing or decreasing the PWM duty cycle with a 1/32 step every 1/64 seconds. The ramp time is therefore a function of the initial set PWM cycle and the final PWM cycle. As an example, starting from 0/32 and going to 32/32 will take 500 ms, while going to from 8/32 to 16/32 takes 125 ms. Note that the ramp function is executed upon every change in PWM cycle setting when the corresponding LEDxRAMP = 1. If a PWM change is programmed via SPI when LEDxRAMP = 0, then the change is immediate rather than spread out over a PWM sweep.

A maximum of only two backlight drivers can be activated at the same time, for instance, the main display plus keypad. If all three backlight drivers are enabled through the LEDxEN bits, meaning none of the duty cycles equals 0/32, then none of the drivers will be activated.

If two backlight drivers are enabled, they time-share the external boost regulator output. The drivers will automatically be enabled and disabled in a 50/50 percent fashion at a sufficiently high rate. The LED drive current will automatically be doubled to the same luminosity as in a single backlight driver configuration.

Figure 33 illustrates the time sharing principle. Assume the MD domain is represented by 6 series white LEDs, and the KP domain is represented by 3 ballasted stacks, that include 3 blue LEDs in each (a diagram of Serial LED configurations is included later in this chapter).

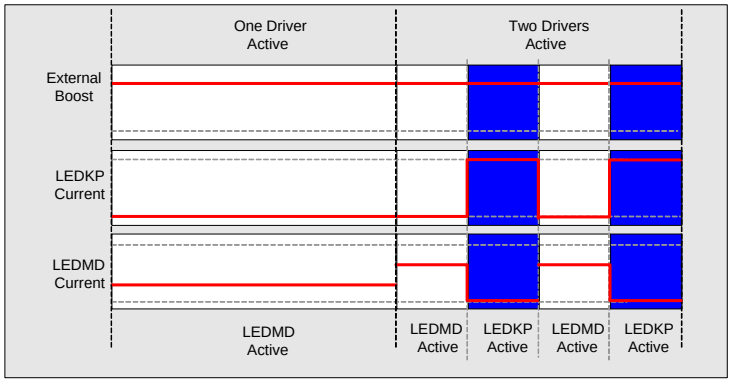


Figure 33. Backlight Drivers Time Sharing Example

The “One Driver Active” case shows the general response when driving a single zone of 6 white LEDs. The “Two Drivers Active” case shows the LEDMD zone driven at twice the current for half the time.

Table 106. Serial LED Driver Characteristics

Parameter[92]	Condition	Min	Typ	Max	Units
Output Current Setting	Low Range Mode	0.0	–	15	mA
	High Range Mode	0.0	–	30	
Current Programming Granularity	Low Range Mode	–	3.0	–	mA
	High Range Mode	–	6.0	–	
PWM Granularity		–	1/32	–	
Repetition Rate	Not blinking	–	256	–	Hz
Absolute Accuracy		–	–	15	%
Matching	At 400 mV, 21 mA	–	–	3.0	%
Glow and Dimming Speed	Per 1/32 duty cycle step	–	1/64*	–	S

Notes
92. Equivalent to 500 ms ramp time when going from 0/32 to 32/32

Figure 34 illustrates some possible configurations for the backlight driver. Note that when parallel strings are ganged together on a driver channel, ballasting resistance is recommended to help balance the currents in each leg.

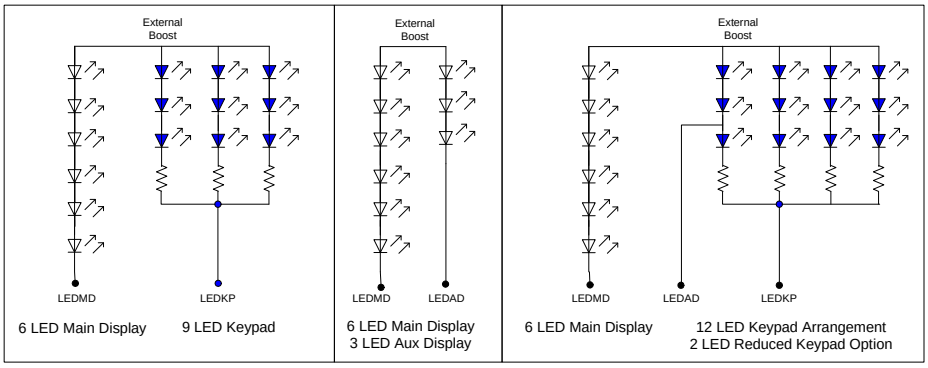


Figure 34. Serial LED Configurations

In the left most example in Figure 34: LEDMD is set at 15 mA (low range), LEDKP is set at 30 mA (high range). When both are operated, then the LEDMD current will pulse at 30 mA and the LEDKP current at 60 mA. This provides an average of 15 mA through the main display backlight LEDs and 30 mA through the keypad backlights LEDs.

SIGNALING LED DRIVERS

The signaling LED drivers LEDR, LEDG, LEDB are independent current sink channels. Each driver channel features programmable current levels via LEDx[2:0] as well as programmable PWM duty cycle settings with LEDxDC[5:0]. By a combination of both, the LED intensity can be adjusted. By driving LEDs of different colors, color mixing can be achieved.

Table 107. Signaling LED Drivers Current Programming

LEDx[2:0][93]	LEDx Current Level (mA)
000	0.0
001	3.0
010	6.0
011	9.0
100	12
101	15
110	18
111	21

Notes
93. "x" represents for R, G and B

Table 108. Signaling LED Drivers Duty Cycle Programming

LEDxDC[5:0][94]	Duty Cycle
000000	0/32, Off
000001	1/32
…	…
010000	16/32
…	…
011111	31/32
1xxxxx	32/32, Continuously On

Notes
94. "x" represents R, G and B

Blue LEDs or bright green LEDs require more headroom than red and normal green signal LEDs. In the application, a 5.0 V or equivalent supply rail is therefore required. This is provided by the integrated boost regulator SWBST. To make software programming easier, an LEDSWBSTEN SPI bit has been provided in the Blue LED register to enable the boost regulator. Note the enable for the boost regulator is an OR of the following SPI bits (SWBSTEN, USBSWBSTEN, and LEDSWBSTEN). For more details on the boost regulator and its control, see Supplies.

As with the backlight driver channels, the signaling LED drivers include ramp up and ramp down patterns are implemented in hardware. Ramp patterns for each of the drivers is accessed with the corresponding LEDxRAMP bit.

The ramp itself is generated by increasing or decreasing the PWM duty cycle with a 1/32 step every 1/64 seconds. The ramp time is therefore a function of the initial set PWM cycle and the final PWM cycle. As an example, starting from 0/32 and going to 32/32 will take 500 ms while going to from 8/32 to 16/32 takes 125 ms.

Note that the ramp function is executed upon every change in PWM cycle setting. If a PWM change is programmed via SPI when LEDxRAMP = 0, then the change is immediate rather than spread out over a PWM sweep.

For color mixing and in order to guarantee a constant color, the color mixing should be obtained by the current level setting so that the intensity is set through the PWM duty cycle.

In addition, programmable blink rates are provided. Blinking is obtained by lowering the PWM repetition rate of each of the drivers through LEDxPER[1:0], while the on period is determined by the duty cycle setting. To avoid high frequency spur coupling in the application, the switching edges of the output drivers are softened. During blinking, so LEDxPER[1:0] is not "00", ramping and dimming patterns cannot be applied.

Table 109. Signal LED Drivers Period Control

LEDxPER[1:0]	Repetition Rate	Units
00	1/256	s
01	1/8	s
10	1	s
11	2	s

Table 110. Signaling LED Driver Characteristics

Parameter	Condition	Min	Typ	Max	Units
Absolute Accuracy		–	–	15	%
Matching	At 400 mV, 21 mA	–	–	10	%
Leakage	LEDxDC[5:0] = 000000	–	–	1.0	µA

Apart from using the signal LED drivers for driving LEDs they can also be used as general purpose open drain outputs for logic signaling or as generic PWM generator outputs. For the maximum voltage ratings.

the enable for the boost regulator is an OR of the following SPI bits (SWBSTEN, USBSWBSTEN, and LEDSWBSTEN). For more details on the boost regulator and its control, see Supplies.

As with the backlight driver channels, the signaling LED drivers include ramp up and ramp down patterns are implemented in hardware. Ramp patterns for each of the drivers is accessed with the corresponding LEDxRAMP bit.

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Note that the ramp function is executed upon every change in PWM cycle setting. If a PWM change is programmed via SPI when LEDxRAMP = 0, then the change is immediate rather than spread out over a PWM sweep.

For color mixing and in order to guarantee a constant color, the color mixing should be obtained by the current level setting so that the intensity is set through the PWM duty cycle.

In addition, programmable blink rates are provided. Blinking is obtained by lowering the PWM repetition rate of each of the drivers through LEDxPER[1:0], while the on period is determined by the duty cycle setting. To avoid high frequency spur coupling in the application, the switching edges of the output drivers are softened. During blinking, so LEDxPER[1:0] is not “00”, ramping and dimming patterns cannot be applied.

SPI BITMAP

The complete SPI bitmap is given in Table 111 with one register per row for a general overview. A color coding is applied which indicates the type of reset for the bits.

Table 111. SPI Bitmap

MC13892 Bitmap										Color Coding:			Bits Reset by RESETB			Bits Reset by RTCPORB		Bits Reset by OFFB			Bits Without Reset			Bits Reloaded at Cold Start			Reserved Bits		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
Register	Register Label	R/W R/T	Address 5:0						Null	Data[23:16]								Data[15:7]										Data[7:0]		
0	Interrupt Status 0	R/W	0	0	0	0	0	0	0	Reserved	Reserved	CHGRGSE1BI	IDGNDI	IDFLOATI	Reserved	Reserved	BVALIDI	Reserved	LOBATHI	LOBATLI	BPONI	CHGCURRI	CCCVI	CHGSHORTI	CHGREVI	CHGFAULTI	CHGDETI	USBOVI	IDFACTORYI	VBUSVA
1	Interrupt Mask 0	R/W	0	0	0	0	0	1	0	Reserved	Reserved	CHGRGSE1BM	IDGNDM	IDFLOATM	Reserved	Reserved	BVALIDM	Reserved	LOBATHM	LOBATLM	BPONM	CHGCURRM	CCCVM	CHGSHORTM	CHGREVM	CHGFAULTM	CHGDETM	USBOVM	IDFACTORYM	VBUSVA
2	Interrupt Sense 0	R	0	0	0	0	1	0	0	Reserved	Reserved	Reserved	IDGNDS	IDFLOATS	Reserved	Reserved	BVALIDS	Reserved	LOBATHS	LOBATLS	BPONS	CHGCURRS	CCCVS	CHGFAULTS[1:0]		CHGENS	CHGDETS	USBOVS	IDFACTORYS	VBUSVA
3	Interrupt Status 1	R/W	0	0	0	0	1	1	0	Spare	BATTDETBI		Reserved	Reserved	Reserved	Reserved	SCPI	Spare	CLKI	THWARNHI	THWARNLI	LPBI	MEMHLDI	WARMI	PCI	RTCRSTI	SYSRSTI	WDIRESTI	PWRON2I	PWRO
4	Interrupt Mask 1	R/W	0	0	0	1	0	0	0	Spare	BATTDETBIM		Reserved	Reserved	Reserved	Reserved	SCPM	Spare	CLKM	THWARNHM	THWARNLM	LPBM	MEMHLDM	WARMM	PCM	RTCRSTM	SYSRSTM	WDIRESTM	PWRON2M	PWRO
5	Interrupt Sense 1	R	0	0	0	1	0	1	0	Spare	BATTDETBS		Reserved	Reserved	Reserved	Reserved		Spare	CLKS	THWARNHS	THWARNLS	LPBS							PWRON2S	PWRO
6	Power Up Mode Sense	R	0	0	0	1	1	0	0	Spare	Spare	Reserved	Reserved	Spare	Spare				Reserved		Spare		CHRGSE1BS	CHRGSSS	Reserved	Reserved	Reserved	PUMS2S[1:0]		
7	Identification	R	0	0	0	1	1	1	0						ICIDCODE[5:0]						FAB[1:0]		FIN[1:0]		ICID[2:0]					
8	Unused	R/W	0	0	1	0	0	0	0																					
9	Unused	R/W	0	0	1	0	0	1	0	CCOUT[15:0]																CCFAULT	Reserved	Reserved	CCCALA	CCCAL
10	Unused	R/W	0	0	1	0	1	0	0									ONEC[14:0]												
11	Unused	R/W	0	0	1	0	1	1	0																					
12	Unused	R/W	0	0	1	1	0	0	0																					
13	Power Control 0	R/W	0	0	1	1	0	1	0	COINCHEN	VCOIN[2:0]			BATTDETEN	Reserved	BPSNS[1:0]								PCUTEXPB	THSEL	GLBRSTENB	CLK32KMCUEN	USEROFFCLK	DRM	USEROF
14	Power Control 1	R/W	0	0	1	1	1	0	0									PCMAXCNT[3:0]				PCCOUNT[3:0]				PCT[7:0]				
15	Power Control 2	R/W	0	0	1	1	1	1	0	STBYDLY[1:0]		Reserved	Reserved	Reserved	CLKDRV[1:0]		Reserved	Reserved	SPIDRV[1:0]		WDIRESET	STANDBYSECINV	STANDBYPRIINV	PWRON3DBNC[1:0]		PWRON2DBNC[1:0]		PWRON1BDBNC[1:0]		PWRON3
16	Unused	R/W	0	1	0	0	0	0	0																					
17	Unused	R/W	0	1	0	0	0	1	0																					
18	Memory A	R/W	0	1	0	0	1	0	0	MEMA[23:0]																				
19	Memory B	R/W	0	1	0	0	1	1	0	MEMB[23:0]																				
20	RTC Time	R/W	0	1	0	1	0	0	0	RTCCALMODE[1:0]		RTCCAL[4:0]				TOD[16:0]														
21	RTC Alarm	R/W	0	1	0	1	0	1	0	RTCDIS	Spare					TODA[16:0]														

Table 111. SPI Bitmap

MC13892 Bitmap										Color Coding:			Bits Reset by RESETB			Bits Reset by RTCPORB			Bits Reset by OFFB			Bits Without Reset			Bits Reloaded at Cold Start			Reserved Bits		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
22	RTC Day	R/W	0	1	0	1	1	0	0										DAY[14:0]											
23	RTC Day Alarm	R/W	0	1	0	1	1	1	0										DAYA[14:0]											
24	Switchers 0	R/W	0	1	1	0	0	0	0	SW1HI	SW1SIDMIN[3:0]				SW1SIDMAX[3:0]				SW1STBY[4:0]			SW1DVS[4:0]								
25	Unused	R/W	0	1	1	0	0	1	0	SW2HI	SW2SIDMIN[3:0]				SW2SIDMAX[3:0]				SW2STBY[4:0]			SW2DVS[4:0]								
26	Switchers 2	R/W	0	1	1	0	1	0	0	SW3HI	Reserved								SW3STBY[4:0]			Spare								
27	Unused	R/W	0	1	1	0	1	1	0	SW4HI									SW4STBY[4:0]			Spare								
28	Switchers 4	R/W	0	1	1	1	0	0	0	Reserved	SWILIMB	PLLX[2:0]			PLLEN	SW2DVSSPEED[1:0]		SW2UOMODE	SW2MHMIDE	SW2MODE[3:0]		Reserved	SIDEN	SW1DVSSPEED[1:0]			SW1UOMODE	SW1MHMIDE	
29	Switchers 5	R/W	0	1	1	1	0	1	0				SWBSTEN						SW4UOMODE	SW4MHMIDE	SW4MODE[3:0]							SW3UOMODE	SW3MHMIDE	
30	Regulator Setting 0	R/W	0	1	1	1	1	0	0					Spare	VCAM[2:0]				VGEN3		VUSB2[1:0]		VPLL[1:0]		VGEN[2:0]			VDIG[1:0]		
31	Regulator Setting 1	R/W	0	1	1	1	1	1	0																VSD[2:0]			VAUDIO[1:0]		
32	Regulator Mode 0	R/W	1	0	0	0	0	0	0				Spare	VUSB2STBY	VUSB2EN	Spare	VPLLSTBY	VPLLEN	VGEN2MODE	VGEN2STBY	VGEN2EN	Spare	VDIGSTBY	VDIGEN				Spare	VIOHISTBY	VIOHI
33	Regulator Mode 1	R/W	1	0	0	0	0	1	0				VSDMODE	VSDSTBY	VSDEN	Spare	VAUDIOSTBY	VAUDIOEN	VVIDEOMODE	VVIDEOSTBY	VVIDEOEN	Reserved		VCAMCONFIG	VCAMMODE	VCAMSTBY	VCAMEN	Spare	Reserved	VGEN3CO
34	Power Miscellaneous	R/W	1	0	0	0	1	0	0			GPO4ADIN				Spare	PWGT2SPIEN	PWGT1SPIEN		GPO4STBY	GPO4EN	GPO3STBY	GPO3EN	GPO2STBY	GPO2EN	GPO1STBY	GPO1EN			
35	Unused	R/W	1	0	0	0	1	1	0																					
36	Audio Rx 0	R/W	1	0	0	1	0	0	0																					
37	Audio Rx 1	R/W	1	0	0	1	0	1	0																					
38	Audio Tx	R/W	1	0	0	1	1	0	0																					
39	SSI Network	R/W	1	0	0	1	1	1	0																					
40	Audio Codec	R/W	1	0	1	0	0	0	0																					
41	Audio Stereo DAC	R/W	1	0	1	0	0	1	0																					
42	Unused	R/W	1	0	1	0	1	0	0																					
43	ADC 0	R/W	1	0	1	0	1	1	0	ADCBIS0				Spare		ADINC2	ADINC1	CHRGRAWDIV	TSMOD[2:0]			Reserved	TSREFEN	ADIN7DIV	ADRESET		ADIN7SEL[1:0]		BUFF
44	ADC 1	R/W	1	0	1	1	0	0	0	ADCBIS1	ADONESHOT	ADTRIGIGN	ASC	ATOX	ATO[7:0]							ADA2[2:0]			ADA1[2:0]			TRIGMASK		ADSE
45	ADC 2	R	1	0	1	1	0	1	0	ADD2[9:0]									Spare		Spare	ADD1[9:0]								
46	ADC 3	R/W	1	0	1	1	1	0	0	Reserved															ICID[2:0]					
47	ADC 4	R	1	0	1	1	1	1	0	ADDBIS2[9:0]									Spare		Spare	ADDBIS1[9:0]								

Table 111. SPI Bitmap

MC13892 Bitmap										Color Coding:			Bits Reset by RESETB			Bits Reset by RTCPORB			Bits Reset by OFFB			Bits Without Reset			Bits Reloaded at Cold Start			Reserved Bits			Not Available Bits		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
48	Charger 0	R/W	1	1	0	0	0	0	0	CHGAUTOVIB	CYCLB	CHGAUTOB	CHRGRESTART	CHGTMRRST	CHRGLEDEN	PLIMDIS	PLIM[1:0]			RVRSMODE	Spare	FETCTRL	FETOVRD	THCHKB	ACLPB	TREN	ICHRG[3:0]			VCHRG[2:0]		
49	USB 0	R/W	1	1	0	0	0	1	0	Reserved	IDPUCNTRL	Reserved	Reserved	Reserved			Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Spare	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
50	Charger USB 1	R/W	1	1	0	0	1	0	0						Spare	Spare	Reserved			Reserved	Reserved	Reserved	OTGSWBSTEN	Reserved	ID100KPU	Reserved	Reserved			VUSBEN			VUSBIN
51	LED Control 0	R/W	1	1	0	0	1	1	0	LEDAD[2:0]			LEDADDC[5:0]						LEDADRAMP	LEDADHI	Spare	LEDMD[2:0]			LEDMDDC[5:0]						LEDMDRAMP	LEDMDHI	Spare
52	LED Control 1	R/W	1	1	0	1	0	0	0										Spare	Spare	Spare	LEDKP[2:0]			LEDKPDC[5:0]						LEKPDRAMP	LEDKPHI	Spare
53	LED Control 2	R/W	1	1	0	1	0	1	0	LEDG[2:0]			LEDGDC[5:0]						LDEDGRAMP	LEDGPER[1:0]		LEDR[2:0]			LEDRDC[5:0]						LDEDRRAMP	LEDRPER[1:0]	
54	LED Control 3	R/W	1	1	0	1	1	0	0										Spare	Spare	LEDSWBSTEN	LEDB[2:0]			LEDBDC[5:0]						LDEDBRAMP	LEDBPER[1:0]	
55	Unused	R/W	1	1	0	1	1	1	0																								
56	Unused	R/W	1	1	1	0	0	0	0																								
57	FSL Use Only	R/W	1	1	1	0	0	1	0																								
58	FSL Use Only	R/W	1	1	1	0	1	0	0																								
59	FSL Use Only	R/W	1	1	1	0	1	1	0																								
60	FSL Use Only	R/W	1	1	1	1	0	0	0																								
61	FSL Use Only	R/W	1	1	1	1	0	1	0																								
62	FSL Use Only	R/W	1	1	1	1	1	0	0																								
63	FSL Use Only	R/W	1	1	1	1	1	1	0																								

The 24 bit wide registers are numbered from 0 to 63, and are referenced throughout this document by register number, or representative name as given in the corresponding captions. The contents of all registers are given in the tables defined in this chapter; each table includes the following information:

Name: Name of the bit. Spare bits are implemented in the design for future use, but are not assigned. Unused bits are not available in the design. Reserved bits are not implemented in the design, but are used on other PMICs.

Bit #: The bit location in the register (0-23)

R/W: Read / Write access and control

- R is read access
- W is write access
- R/W is read and write access
- RW1C is read and write access with write 1 to clear
- RWM is read and write access while the device can modify the bit

Reset: Resetting signal

- RESETB, which is the same signal as the RESETB pin (so bit is held in reset as long as RESETB is low)
- RTCPORB which is the reset signal of the RTC module (sobit is no longer held in reset once RTC power is good)
- OFFB which is an internal signal generated when transitioning into the Off state
- NONE. There is no reset signal for hardwired bits nor for the bits of which the state is determined by the power up mode settings

Default: The value after reset as noted in the Default column of the SPI map.

- Fixed defaults are explicitly declared as 0 or 1.
- * corresponds to Read / Write bits that are initialized at startup based on power up mode settings (board level pin connections) validated at the beginning of Cold or Warm Start. Bits are subsequently SPI modifiable.
- S corresponds to Read only sense bits that continuously monitor an input signal (sense signal is not latched).
- L corresponds to Read only sense bits that are latched at startup.
- X indicates that the state does not havean explicitly defined default value which can be specified. For instance, some bits default to a value which is dependent on the version of the IC.

Description: A short description of the bit function, in some cases additional information is included

The following tables are intended to give a summarized overview, for details on the bit description, see the individual chapters.

Table 112. Register 0, Interrupt Status 0

Name	Bit #	R/W	Reset	Default	Description
ADCDONEI	0	RW1C	RESETB	0	ADC has finished requested conversions
ADCBISDONEI	1	RW1C	RESETB	0	ADCBIS has finished requested conversions
TSI	2	RW1C	RESETB	0	Touch screen wake-up
VBUSVALIDI	3	RW1C	OFFB	0	VBUSVALID detect
IDFACTORYI	4	RW1C	RESETB	0	ID factory mode detect
USBOVI	5	RW1C	RTCPORB	0	USB over-voltage detection
CHGDETI	6	RW1C	OFFB	0	Charger attach
CHGFAULTI	7	RW1C	RTCPORB	0	Charger fault detection
CHGREVI	8	RW1C	RESETB	0	Charger path reverse current
CHGSHORTI	9	RW1C	RESETB	0	Charger path short circuit
CCCVI	10	RW1C	RESETB	0	Charger path CC / CV transition detect

Table 112. Register 0, Interrupt Status 0

Name	Bit #	R/W	Reset	Default	Description
CHGCURRI	11	RW1C	RESETB	0	Charge current below threshold warning
BPONI	12	RW1C	OFFB	0	BP turn on threshold
LOBATLI	13	RW1C	RESETB	0	Low battery low threshold warning
LOBATHI	14	RW1C	RESETB	0	Low battery high threshold warning
Reserved	15	R		0	For future use
BVALIDI	16	RW1C	OFFB	0	USB B-session valid interrupt
Reserved	17	R		0	For future use
Reserved	18	R		0	For future use
IDFLOATI	19	RW1C	RESETB	0	USB ID float detect
IDGNDI	20	RW1C	RESETB	0	USB ID ground detect
CHRGSE1BI	21	RW1C	RESETB	0	Wall Charger detect
Reserved	22	R		0	For future use
Reserved	23	R		0	For future use

Table 113. Register 1, Interrupt Mask 0

Name	Bit #	R/W	Reset	Default	Description
ADCDONEM	0	R/W	RESETB	1	ADCDONEI mask bit
ADCBISDONEM	1	R/W	RESETB	1	ADCBISDONEI mask bit
TSM	2	R/W	RESETB	1	TSI mask bit
VBUSVALIDM	3	R/W	OFFB	1	VBUSVALIDI mask bit
IDFACTORYM	4	R/W	RESETB	1	ID factory mask bit
USBOVM	5	R/W	RTCPORB	1	USBOVI mask bit
CHGDETM	6	R/W	OFFB	1	CHGDETI mask bit
CHGFAULTM	7	R/W	RTCPORB	1	CHGFAULTI mask bit
CHGREVM	8	R/W	RESETB	1	CHGREVI mask bit
CHGSHORTM	9	R/W	RESETB	1	CHGSHORTI mask bit
CCCVM	10	R/W	RESETB	1	CCCV mask bit
CHGCURRM	11	R/W	RESETB	1	CHGCURRI mask bit
BPONM	12	R/W	OFFB	1	BPONI mask bit
LOBATLM	13	R/W	RESETB	1	LOBATLI mask bit
LOBATHM	14	R/W	RESETB	1	LOBATHI mask bit
Reserved	15	R		1	For future use
BVALIDM	16	R/W	OFFB	1	BVALIDI mask bit
Reserved	17	R		1	For future use
Reserved	18	R		1	For future use
IDFLOATM	19	R/W	RESETB	1	IDFLOATI mask bit
IDGNDM	20	R/W	RESETB	1	IDGNDI mask bit
CHRGSE1BM	21	R/W	RESETB	1	Wall Charger mask bit

Table 113. Register 1, Interrupt Mask 0

Reserved	22	R		1	For future use
Reserved	23	R		1	For future use

Table 114. Register 2, Interrupt Sense 0

Name	Bit #	R/W	Reset	Default	Description
Unused	0	R		0	Not available
Unused	1	R		0	Not available
Unused	2	R		0	Not available
VBUSVALIDS	3	R	NONE	S	VBUSVALIDI sense bit
IDFACTORYS	4	R	NONE	S	ID factory sense bit
USBOVS	5	R	NONE	S	USBOVI sense bit
CHGDETS	6	R	NONE	S	CHGDETI sense bit
CHGENS	7	R	NONE	0	Charger enable sense bit
CHGFAULTS0	8	R	NONE	S	CHGREVI sense bit
CHGFAULTS1	9	R	NONE	S	CHRGFAULT sense bit 0
CCCVS	10	R	NONE	S	CHRGFAULT sense bit 1
CHGCURRS	11	R	NONE	S	CHGCURRI sense bit
BPONS	12	R	NONE	S	BPONI sense bit
LOBATLS	13	R	NONE	S	LOBATLI sense bit
LOBATHS	14	R	NONE	S	LOBATHI sense bit
Reserved	15	R		0	For future use
BVALIDS	16	R	NONE	S	USB B-session valid sense
Reserved	17	R		0	For future use
Reserved	18	R		0	For future use
IDFLOATS	19	R	NONE	S	ID float sense bit
IDGNDS	20	R	NONE	S	ID ground sense bit
Reserved	21	R		0	For future use
Reserved	22	R		0	For future use
Reserved	23	R		0	For future use

Table 115. Register 3, Interrupt Status 1

Name	Bit #	R/W	Reset	Default	Description
1HZI	0	RW1C	RTCPORB	0	1.0 Hz time tick
TODAI	1	RW1C	RTCPORB	0	Time of day alarm
PWRON3I	2	RW1C	OFFB	0	PWRON3 event
PWRON1I	3	RW1C	OFFB	0	PWRON1 event

Table 115. Register 3, Interrupt Status 1

PWRON2I	4	RW1C	OFFB	0	PWRON2 event
WDIRESETI	5	RW1C	RTCPORB	0	WDI system reset event
SYSRSTI	6	RW1C	RTCPORB	0	PWRON system reset event
RTCRSTI	7	RW1C	RTCPORB	1	RTC reset event
PCI	8	RW1C	OFFB	0	Power cut event
WARMI	9	RW1C	RTCPORB	0	Warm start event
MEMHLDI	10	RW1C	RTCPORB	0	Memory hold event
LPBI	11	RW1C	RTCPORB	0	Low-power USB boot detection
THWARNLI	12	RW1C	RESETB	0	Thermal warning low threshold
THWARNHI	13	RW1C	RESETB	0	Thermal warning high threshold
CLKI	14	RW1C	RESETB	0	Clock source change
Spare	15	RW1C	RESETB	0	For future use
SCPI	16	RW1C	RESETB	0	Short-circuit protection trip detection
Reserved	17	R		0	For future use
Reserved	18	R		0	For future use
Reserved	19	R		0	For future use
Reserved	20	R		0	For future use
Unused	21	R		0	Not available
BATTDETBI	22	RW1C	RESETB	0	Battery removal detect
Spare	23	RW1C	RESETB	0	For future use

Table 116. Register 4, Interrupt Mask 1

Name	Bit #	R/W	Reset	Default	Description
1HZM	0	R/W	RTCPORB	1	1HZI mask bit
TODAM	1	R/W	RTCPORB	1	TODAI mask bit
PWRON3M	2	R/W	OFFB	1	PWRON3 mask bit
PWRON1M	3	R/W	OFFB	1	PWRON1 mask bit
PWRON2M	4	R/W	OFFB	1	PWRON2 mask bit
WDIRESETM	5	R/W	RTCPORB	1	WDIRESETI mask bit
SYSRSTM	6	R/W	RTCPORB	1	SYSRSTI mask bit
RTCRSTM	7	R/W	RTCPORB	1	RTCRSTI mask bit
PCM	8	R/W	OFFB	1	PCI mask bit
WARMM	9	R/W	RTCPORB	1	WARMI mask bit
MEMHLDM	10	R/W	RTCPORB	1	MEMHLDI mask bit
LPBM	11	R/W	RTCPORB	0	Low-power USB detect mask bit
THWARNLM	12	R/W	RESETB	1	THWARNLI mask bit
THWARNHM	13	R/W	RESETB	1	THWARNHI mask bit
CLKM	14	R/W	RESETB	1	CLKI mask bit
Spare	15	R/W	RESETB	1	For future use
SCPM	16	R/W	RESETB	1	Short-circuit protection trip mask bit
Reserved	17	R		1	For future use
Reserved	18	R		1	For future use
Reserved	19	R		1	For future use
Reserved	20	R		1	For future use
Unused	21	R		1	Not available
BATTDETBM	22	R/W	RESETB	1	Battery detect removal mask bit
Spare	23	R/W	RESETB	1	For future use

Table 117. Register 5, Interrupt Sense 1

Name	Bit #	R/W	Reset	Default	Description
Unused	0	R		0	Not available
Unused	1	R		0	Not available
PWRON3S	2	R	NONE	S	PWRON3I sense bit
PWRON1S	3	R	NONE	S	PWRON1I sense bit
PWRON2S	4	R	NONE	S	PWRON2I sense bit
Unused	5	R		0	Not available
Unused	6	R		0	Not available
Unused	7	R		0	Not available
Unused	8	R		0	Not available
Unused	9	R		0	Not available
Unused	10	R		0	Not available
LPBS	11	R	NONE	0	Low-power USB boot sense bit
THWARNLS	12	R	NONE	S	THWARNLI sense bit
THWARNHS	13	R	NONE	S	THWARNHI sense bit
CLKS	14	R	NONE	S	CLKI sense bit
Spare	15	R	NONE	0	For future use
Unused	16	R		0	Not available
Reserved	17	R		0	For future use
Reserved	18	R		0	For future use
Reserved	19	R		0	For future use
Reserved	20	R		0	For future use
Unused	21	R		0	Not available
BATTDETBS	22	R	NONE	S	Battery removal detect sense bit
Spare	23	R	NONE	0	For future use

Table 118. Register 6, Power Up Mode Sense

Name	Bit #	R/W	Reset	Default	Description
MODES0	0	R	NONE	S	MODE sense decode
IMODES1	1	R	NONE	S	
PUMS1S0	2	R	NONE	L	PUMS1 state
PUMS1S1	3	R	NONE	L	
PUMS2S0	4	R	NONE	L	PUMS2 state
PUMS2S1	5	R	NONE	L	
Reserved	6	R		0	For future use
Reserved	7	R		0	For future use
Reserved	8	R		0	For future use
CHRGSSS (1)	9	R	NONE	L	Charger Serial/Single mode sense
CHRGSE1BS	10	R	NONE	S	CHRGSE1BS sense bit
Unused	11	R		0	Not available
Spare	12	R	NONE	0	For future use
Unused	13	R		0	Not available
Reserved	14	R		0	For future use
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Spare	18	R	NONE	0	For future use
Spare	19	R	NONE	0	For future use
Reserved	20	R		0	For future use
Reserved	21	R		0	For future use

Table 118. Register 6, Power Up Mode Sense

Name	Bit #	R/W	Reset	Default	Description
Spare	22	R	NONE	0	For future use
Spare	23	R	NONE	0	For future use

Notes
95. CHRGSSS will latch an updated sense value when the charger is enabled.

Table 119. Register 7, Identification

Name	Bit #	R/W	Reset	Default	Description
REV0	0	R	NONE	X	Revision
REV1	1	R	NONE	X	
REV2	2	R	NONE	X	
REV3	3	R	NONE	X	
REV4	4	R	NONE	X	
Unused	5	R		0	Not available
ICID0	6	R	NONE	1	Generation ID
ICID1	7	R	NONE	1	
ICID2	8	R	NONE	1	
FIN0	9	R	NONE	X	MC13892 fin version
FIN1	10	R	NONE	X	
FAB0	11	R	NONE	X	MC13892 fab identifier
FAB1	12	R	NONE	X	
ICIDCODE0	13	R	NONE	0	IC ID Within generation
ICIDCODE1	14	R	NONE	1	
ICIDCODE2	15	R	NONE	0	
ICIDCODE3	16	R	NONE	0	
ICIDCODE4	17	R	NONE	0	
ICIDCODE5	18	R	NONE	0	
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 120. Register 8, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 121. Register 9, ACC 0

Name	Bit #	R/W	Reset	Default	Description
STARTCC	0	R/W	RTCPORB	0	1 = Run, 0=Stop
RSTCC	1	RWC	RTCPORB	0	1 = Reset, self clearing
CCDITHER	2	R/W	RTCPORB	0	1 = ACC Dithering enabled, 0=ACC Dithering disabled
CCCALDB	3	R/W	RTCPORB	0	1 = Disable Digital Offset Cancellation
CCCALA	4	R/W	RTCPORB	0	1 = Enable Analog Offset Calibration Mode
Reserved	5	R		0	Reserved for future use for scaler
Reserved	6	R		0	Reserved for future use (for scaler)
CCFAULT	7	R/W	RTCPORB	0	1 = CCOUT contents no longer valid

Table 121. Register 9, ACC 0

CCOUT0	8	R	RTCPORB	0	Coulomb Counter
CCOUT1	9	R	RTCPORB	0	
CCOUT2	10	R	RTCPORB	0	
CCOUT3	11	R	RTCPORB	0	
CCOUT4	12	R	RTCPORB	0	
CCOUT5	13	R	RTCPORB	0	
CCOUT6	14	R	RTCPORB	0	
CCOUT7	15	R	RTCPORB	0	
CCOUT8	16	R	RTCPORB	0	
CCOUT9	17	R	RTCPORB	0	
CCOUT10	18	R	RTCPORB	0	
CCOUT11	19	R	RTCPORB	0	
CCOUT12	20	R	RTCPORB	0	
CCOUT13	21	R	RTCPORB	0	
CCOUT14	22	R	RTCPORB	0	
CCOUT15	23	R	RTCPORB	0	

Table 122. Register 10, ACC 1

Name	Bit #	R/W	Reset	Default	Description
ONEC0	0	R	RTCPORB	1	Accumulated Current Counter output
ONEC1	1	R	RTCPORB	0	
ONEC2	2	R	RTCPORB	0	
ONEC3	3	R	RTCPORB	0	
ONEC4	4	R	RTCPORB	0	
ONEC5	5	R	RTCPORB	0	
ONEC6	6	R	RTCPORB	0	
ONEC7	7	R	RTCPORB	0	
ONEC8	8	R	RTCPORB	0	
ONEC9	9	R	RTCPORB	0	
ONEC10	10	R	RTCPORB	0	
ONEC11	11	R	RTCPORB	0	
ONEC12	12	R	RTCPORB	0	
ONEC13	13	R	RTCPORB	0	
ONEC14	14	R	RTCPORB	0	
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 123. Register 11, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 124. Register 12, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 125. Register 13, Power Control 0

Name	Bit #	R/W	Reset	Default	Description
PCEN	0	R/W	RTCPORB	0	Power cut enable
PCCOUNTEN	1	R/W	RTCPORB	0	Power cut counter enable
WARMEN	2	R/W	RTCPORB	0	Warm start enable
USEROFFSPI	3	R/W	RESETB	0	SPI command for entering user off modes
DRM	4	R/W	RTCPORB	0	Keeps VSRTC and CLK32KMCU on for all states
USEROFFCLK	5	R/W	RTCPORB	0	Keeps the CLK32KMCU active during user off
CLK32KMCUEN	6	R/W	RTCPORB	1	Enables the CLK32KMCU
GLBRSTENB[(96)]	7	R/W	RTCPORB	0	Global Reset Function enabled on the PWRON3 pin
THSEL	8	R/W	RESETB	0	Thermal protection threshold select
PCUTEXPB	9	RWM	RTCPORB	0	PCUTEXPB=1 at a startup event indicates that PCUT timer did not expire (assuming it was set to 1 after booting)
Unused	10	R		0	Not available
Unused	11	R		0	Not available

Table 125. Register 13, Power Control 0

Name	Bit #	R/W	Reset	Default	Description
Unused	12	R		0	Not available
Unused	13	R		0	Not available
Unused	14	R		0	Not available
Unused	15	R		0	Not available
BPSNS0	16	R/W	RTCPORB	0	
BPSNS1	17	R/W	RTCPORB	0	
Reserved	18	R		0	For future use
BATTDETEN	19	R/W	RTCPORB	0	Enables battery detect function
VCOIN0	20	R/W	RTCPORB	0	Coin cell charger voltage setting
VCOIN1	21	R/W	RTCPORB	0	
VCOIN2	22	R/W	RTCPORB	0	
COINCHEN	23	R/W	RTCPORB	0	Coin cell charger enable

Notes
96. MC13892A/C versions global reset is active low (GLBRSTENB = 0)
MC13892B/D versions global reset is active high (GLBRSTENB = 1)

Table 126. Register 14, Power Control 1

Name	Bit #	R/W	Reset	Default	Description
PCT0	0	R/W	RTCPORB	0	Power cut timer
PCT1	1	R/W	RTCPORB	0	
PCT2	2	R/W	RTCPORB	0	
PCT3	3	R/W	RTCPORB	0	
PCT4	4	R/W	RTCPORB	0	
PCT5	5	R/W	RTCPORB	0	
PCT6	6	R/W	RTCPORB	0	
PCT7	7	R/W	RTCPORB	0	
PCCOUNT0	8	R/W	RTCPORB	0	Power cut counter
PCCOUNT1	9	R/W	RTCPORB	0	
PCCOUNT2	10	R/W	RTCPORB	0	
PCCOUNT3	11	R/W	RTCPORB	0	
PCMAXCNT0	12	R/W	RTCPORB	0	Maximum allowed number of power cuts
PCMAXCNT1	13	R/W	RTCPORB	0	
PCMAXCNT2	14	R/W	RTCPORB	0	
PCMAXCNT3	15	R/W	RTCPORB	0	
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 127. Register 15, Power Control 2

Name	Bit #	R/W	Reset	Default	Description
RESTARTEN	0	R/W	RTCPORB	0	Enables automatic restart after a system reset
PWRON1RSTEN	1	R/W	RTCPORB	0	Enables system reset on PWRON1 pin
PWRON2RSTEN	2	R/W	RTCPORB	0	Enables system reset on PWRON2 pin
PWRON3RSTEN	3	R/W	RTCPORB	0	Enables system reset on PWRON3 pin

Table 127. Register 15, Power Control 2

Name	Bit #	R/W	Reset	Default	Description
PWRON1DBNC0	4	R/W	RTCPORB	0	Sets debounce time on PWRON1 pin
PWRON1DBNC1	5	R/W	RTCPORB	0	
PWRON2DBNC0	6	R/W	RTCPORB	0	Sets debounce time on PWRON2 pin
PWRON2DBNC1	7	R/W	RTCPORB	0	
PWRON3DBNC0	8	R/W	RTCPORB	0	Sets debounce time on PWRON3 pin
PWRON3DBNC1	9	R/W	RTCPORB	0	
STANDBYINV	10	R/W	RTCPORB	0	If set then STANDBY is interpreted as active low
STANDBYSECINV	11	R/W	RTCPORB	0	If set then STANDBYSEC is interpreted as active low
WDIRESET	12	R/W	RESETB	0	Enables system reset through WDI
SPIDRV0	13	R/W	RTCPORB	0	SPI drive strength
SPIDRV1	14	R/W	RTCPORB	0	
Reserved	15	R		0	For future use
Reserved	16	R		0	
CLK32KDRV0	17	R/W	RTCPORB	0	CLK32K and CLK32KMCU drive strength (master control bits)
CLK32KDRV1	18	R/W	RTCPORB	0	
Reserved	19	R		0	For future use
Reserved	20	R		0	
Reserved	21	R		0	
STBYDLY0	22	R/W	RESETB	1	Standby delay control
STBYDLY1	23	R/W	RESETB	0	

Table 128. Register 16, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 129. Register 17, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 130. Register 18, Memory A

Name	Bit #	R/W	Reset	Default	Description
MEMA0	0	R/W	RTCPORB	0	Backup memory A
MEMA1	1	R/W	RTCPORB	0	
MEMA2	2	R/W	RTCPORB	0	
MEMA3	3	R/W	RTCPORB	0	
MEMA4	4	R/W	RTCPORB	0	
MEMA5	5	R/W	RTCPORB	0	
MEMA6	6	R/W	RTCPORB	0	
MEMA7	7	R/W	RTCPORB	0	
MEMA8	8	R/W	RTCPORB	0	
MEMA9	9	R/W	RTCPORB	0	
MEMA10	10	R/W	RTCPORB	0	
MEMA11	11	R/W	RTCPORB	0	
MEMA12	12	R/W	RTCPORB	0	
MEMA13	13	R/W	RTCPORB	0	
MEMA14	14	R/W	RTCPORB	0	
MEMA15	15	R/W	RTCPORB	0	
MEMA16	16	R/W	RTCPORB	0	
MEMA17	17	R/W	RTCPORB	0	
MEMA18	18	R/W	RTCPORB	0	
MEMA19	19	R/W	RTCPORB	0	
MEMA20	20	R/W	RTCPORB	0	
MEMA21	21	R/W	RTCPORB	0	
MEMA22	22	R/W	RTCPORB	0	
MEMA23	23	R/W	RTCPORB	0	

Table 131. Register 19, Memory B

Name	Bit #	R/W	Reset	Default	Description
MEMB0	0	R/W	RTCPORB	0	Backup memory B
MEMB1	1	R/W	RTCPORB	0	
MEMB2	2	R/W	RTCPORB	0	
MEMB3	3	R/W	RTCPORB	0	
MEMB4	4	R/W	RTCPORB	0	
MEMB5	5	R/W	RTCPORB	0	
MEMB6	6	R/W	RTCPORB	0	
MEMB7	7	R/W	RTCPORB	0	
MEMB8	8	R/W	RTCPORB	0	
MEMB9	9	R/W	RTCPORB	0	
MEMB10	10	R/W	RTCPORB	0	
MEMB11	11	R/W	RTCPORB	0	
MEMB12	12	R/W	RTCPORB	0	
MEMB13	13	R/W	RTCPORB	0	
MEMB14	14	R/W	RTCPORB	0	
MEMB15	15	R/W	RTCPORB	0	
MEMB16	16	R/W	RTCPORB	0	
MEMB17	17	R/W	RTCPORB	0	
MEMB18	18	R/W	RTCPORB	0	
MEMB19	19	R/W	RTCPORB	0	
MEMB20	20	R/W	RTCPORB	0	
MEMB21	21	R/W	RTCPORB	0	
MEMB22	22	R/W	RTCPORB	0	
MEMB23	23	R/W	RTCPORB	0	

Table 132. Register 20, RTC Time

Name	Bit #	R/W	Reset	Default	Description
TOD0	0	R/W	RTCPORB	0	Time of day counter
TOD1	1	R/W	RTCPORB	0	
TOD2	2	R/W	RTCPORB	0	
TOD3	3	R/W	RTCPORB	0	
TOD4	4	R/W	RTCPORB	0	
TOD5	5	R/W	RTCPORB	0	
TOD6	6	R/W	RTCPORB	0	
TOD7	7	R/W	RTCPORB	0	
TOD8	8	R/W	RTCPORB	0	
TOD9	9	R/W	RTCPORB	0	
TOD10	10	R/W	RTCPORB	0	
TOD11	11	R/W	RTCPORB	0	
TOD12	12	R/W	RTCPORB	0	
TOD13	13	R/W	RTCPORB	0	
TOD14	14	R/W	RTCPORB	0	
TOD15	15	R/W	RTCPORB	0	
TOD16	16	R/W	RTCPORB	0	
RTCCAL0	17	R/W	RTCPORB	0	RTC calibration count
RTCCAL1	18	R/W	RTCPORB	0	
RTCCAL2	19	R/W	RTCPORB	0	
RTCCAL3	20	R/W	RTCPORB	0	
RTCCAL4	21	R/W	RTCPORB	0	

Table 132. Register 20, RTC Time

Name	Bit #	R/W	Reset	Default	Description
RTCCALMODE0	22	R/W	RTCPORB	0	RTC calibration mode
RTCCALMODE1	23	R/W	RTCPORB	0	

Table 133. Register 21, RTC Alarm

Name	Bit #	R/W	Reset	Default	Description
TODA0	0	R/W	RTCPORB	1	Time of day alarm
TODA1	1	R/W	RTCPORB	1	
TODA2	2	R/W	RTCPORB	1	
TODA3	3	R/W	RTCPORB	1	
TODA4	4	R/W	RTCPORB	1	
TODA5	5	R/W	RTCPORB	1	
TODA6	6	R/W	RTCPORB	1	
TODA7	7	R/W	RTCPORB	1	
TODA8	8	R/W	RTCPORB	1	
TODA9	9	R/W	RTCPORB	1	
TODA10	10	R/W	RTCPORB	1	
TODA11	11	R/W	RTCPORB	1	
TODA12	12	R/W	RTCPORB	1	
TODA13	13	R/W	RTCPORB	1	
TODA14	14	R/W	RTCPORB	1	
TODA15	15	R/W	RTCPORB	1	
TODA16	16	R/W	RTCPORB	1	
Spare	17	R/W	RTCPORB	0	For future use
Spare	18	R/W	RTCPORB	0	
Spare	19	R/W	RTCPORB	0	
Spare	20	R/W	RTCPORB	0	
Spare	21	R/W	RTCPORB	0	
Spare	22	R/W	RTCPORB	0	
RTCDIS	23	R/W	RTCPORB	0	Disable RTC

Table 134. Register 22, RTC Day

Name	Bit #	R/W	Reset	Default	Description
DAY0	0	R/W	RTCPORB	0	Day counter
DAY1	1	R/W	RTCPORB	0	
DAY2	2	R/W	RTCPORB	0	
DAY3	3	R/W	RTCPORB	0	
DAY4	4	R/W	RTCPORB	0	
DAY5	5	R/W	RTCPORB	0	
DAY6	6	R/W	RTCPORB	0	
DAY7	7	R/W	RTCPORB	0	
DAY8	8	R/W	RTCPORB	0	
DAY9	9	R/W	RTCPORB	0	
DAY10	10	R/W	RTCPORB	0	
DAY11	11	R/W	RTCPORB	0	
DAY12	12	R/W	RTCPORB	0	
DAY13	13	R/W	RTCPORB	0	
DAY14	14	R/W	RTCPORB	0	

Table 134. Register 22, RTC Day

Name	Bit #	R/W	Reset	Default	Description
Unused	15	R		0	Not available
Unused	16	R		0	
Unused	17	R		0	
Unused	18	R		0	
Unused	19	R		0	
Unused	20	R		0	
Unused	21	R		0	
Unused	22	R		0	
Unused	23	R		0	

Table 135. Register 23, RTC Day Alarm

Name	Bit #	R/W	Reset	Default	Description
DAYA0	0	R/W	RTCPORB	1	Day alarm
DAYA1	1	R/W	RTCPORB	1	
DAYA2	2	R/W	RTCPORB	1	
DAYA3	3	R/W	RTCPORB	1	
DAYA4	4	R/W	RTCPORB	1	
DAYA5	5	R/W	RTCPORB	1	
DAYA6	6	R/W	RTCPORB	1	
DAYA7	7	R/W	RTCPORB	1	
DAYA8	8	R/W	RTCPORB	1	
DAYA9	9	R/W	RTCPORB	1	
DAYA10	10	R/W	RTCPORB	1	
DAYA11	11	R/W	RTCPORB	1	
DAYA12	12	R/W	RTCPORB	1	
DAYA13	13	R/W	RTCPORB	1	
DAYA14	14	R/W	RTCPORB	1	
Unused	15	R		0	Not available
Unused	16	R		0	
Unused	17	R		0	
Unused	18	R		0	
Unused	19	R		0	
Unused	20	R		0	
Unused	21	R		0	
Unused	22	R		0	
Unused	23	R		0	

Table 136. Register 24, Switchers 0

Name	Bit #	R/W	Reset	Default	Description
SW10	0	R/W	NONE	*	SW1 setting in normal mode
SW11	1	R/W	NONE	*	
SW12	2	R/W	NONE	*	
SW13	3	R/W	NONE	*	
SW14	4	R/W	NONE	*	

Table 136. Register 24, Switchers 0

Name	Bit #	R/W	Reset	Default	Description
SW1DVS0	5	R/W	NONE	*	SW1 setting in DVS mode
SW1DVS1	6	R/W	NONE	*	
SW1DVS2	7	R/W	NONE	*	
SW1DVS3	8	R/W	NONE	*	
SW1DVS4	9	R/W	NONE	*	
SW1STBY0	10	R/W	NONE	*	SW1 setting in Standby mode
SW1STBY1	11	R/W	NONE	*	
SW1STBY2	12	R/W	NONE	*	
SW1STBY3	13	R/W	NONE	*	
SW1STBY4	14	R/W	NONE	*	
SW1SIDMAX0	15	R/W	RESETB	0	SW1 SID mode maximum level
SW1SIDMAX1	16	R/W	RESETB	1	
SW1SIDMAX2	17	R/W	RESETB	0	
SW1SIDMAX3	18	R/W	RESETB	1	
SW1SIDMIN0	19	R/W	RESETB	0	SW1 SID mode minimum level (leading 0 implied)
SW1SIDMIN1	20	R/W	RESETB	0	
SW1SIDMIN2	21	R/W	RESETB	0	
SW1SIDMIN3	22	R/W	RESETB	1	
SW1HI	23	R/W	NONE	*	SW1 output range selection

Table 137. Register 25, Switchers 1

Name	Bit #	R/W	Reset	Default	Description
SW20	0	R/W	NONE	*	SW2 setting in normal mode
SW21	1	R/W	NONE	*	
SW22	2	R/W	NONE	*	
SW23	3	R/W	NONE	*	
SW24	4	R/W	NONE	*	
SW2DVS0	5	R/W	NONE	*	SW2 setting in DVS mode
SW2DVS1	6	R/W	NONE	*	
SW2DVS2	7	R/W	NONE	*	
SW2DVS3	8	R/W	NONE	*	
SW2DVS4	9	R/W	NONE	*	
SW2STBY0	10	R/W	NONE	*	SW2 setting in Standby mode
SW2STBY1	11	R/W	NONE	*	
SW2STBY2	12	R/W	NONE	*	
SW2STBY3	13	R/W	NONE	*	
SW2STBY4	14	R/W	NONE	*	
SW2SIDMAX0	15	R/W	RESETB	0	SW2 SID mode maximum level
SW2SIDMAX1	16	R/W	RESETB	1	
SW2SIDMAX2	17	R/W	RESETB	0	
SW2SIDMAX3	18	R/W	RESETB	1	
SW2SIDMIN0	19	R/W	RESETB	0	SW2 SID mode minimum level (leading 0 implied)
SW2SIDMIN1	20	R/W	RESETB	0	
SW2SIDMIN2	21	R/W	RESETB	0	
SW2SIDMIN3	22	R/W	RESETB	1	
SW2HI	23	R/W	NONE	*	SW2 output range selection

Table 138. Register 26, Switchers 2

Name	Bit #	R/W	Reset	Default	Description
SW30	0	R/W	NONE	*	SW3 setting in normal mode
SW31	1	R/W	NONE	*	
SW32	2	R/W	NONE	*	
SW33	3	R/W	NONE	*	
SW34	4	R/W	NONE	*	
Spare	5	R/W	NONE	*	For future use
Spare	6	R/W	NONE	*	
Spare	7	R/W	NONE	*	
Spare	8	R/W	NONE	*	
Spare	9	R/W	NONE	*	
SW3STBY0	10	R/W	NONE	*	SW3 setting in Standby mode
SW3STBY1	11	R/W	NONE	*	
SW3STBY2	12	R/W	NONE	*	
SW3STBY3	13	R/W	NONE	*	
SW3STBY4	14	R/W	NONE	*	
Unused	15	R		0	Not available
Unused	16	R		0	
Unused	17	R		0	
Unused	18	R		0	
Unused	19	R		0	
Unused	20	R		0	
Unused	21	R		0	
Reserved	22	R		0	For future use
SW3HI	23	R/W	NONE	*	SW3 output range selection

Table 139. Register 27, Switchers 3

Name	Bit #	R/W	Reset	Default	Description
SW40	0	R/W	NONE	*	SW4 setting in normal mode
SW41	1	R/W	NONE	*	
SW42	2	R/W	NONE	*	
SW43	3	R/W	NONE	*	
SW44	4	R/W	NONE	*	
Spare	5	R/W	NONE	*	For future use
Spare	6	R/W	NONE	*	
Spare	7	R/W	NONE	*	
Spare	8	R/W	NONE	*	
Spare	9	R/W	NONE	*	
SW4STBY0	10	R/W	NONE	*	SW4 setting in Standby mode
SW4STBY1	11	R/W	NONE	*	
SW4STBY2	12	R/W	NONE	*	
SW4STBY3	13	R/W	NONE	*	
SW4STBY4	14	R/W	NONE	*	

Table 139. Register 27, Switchers 3

Name	Bit #	R/W	Reset	Default	Description
Unused	15	R		0	Not available
Unused	16	R		0	
Unused	17	R		0	
Unused	18	R		0	
Unused	19	R		0	
Unused	20	R		0	
Unused	21	R		0	
Unused	22	R		0	
SW4HI	23	R/W	NONE	*	SW4 output range selection

Table 140. Register 28, Switchers 4

Name	Bit #	R/W	Reset	Default	Description
SW1MODE0	0	R/W	RESETB	0	SW1 operating mode
SW1MODE1	1	R/W	RESETB	1	
SW1MODE2	2	R/W	RESETB	0	
SW1MODE3	3	R/W	RESETB	1	
SW1MHMODE	4	R/W	OFFB	0	SW1 Memory Hold mode
SW1UOMODE	5	R/W	OFFB	0	SW1 User Off mode
SW1DVSSPEED0	6	R/W	RESETB	1	SW1 DVS speed setting
SW1DVSSPEED1	7	R/W	RESETB	0	
SIDEN	8	R/W	RESETB	0	SID mode enable
Reserved	9	R		0	For future use
SW2MODE0	10	R/W	RESETB	0	SW2 operating mode
SW2MODE1	11	R/W	RESETB	1	
SW2MODE2	12	R/W	RESETB	0	
SW2MODE3	13	R/W	RESETB	1	
SW2MHMODE	14	R/W	OFFB	0	SW2 Memory Hold mode
SW2UOMODE	15	R/W	OFFB	0	SW2 User Off mode
SW2DVSSPEED0	16	R/W	RESETB	1	SW2 DVS speed setting
SW2DVSSPEED1	17	R/W	RESETB	0	
PLLEN	18	R/W	RESETB	0	Switcher PLL enable
PLLX0	19	R/W	RESETB	0	Switcher PLL multiplication factor
PLLX1	20	R/W	RESETB	0	
PLLX2	21	R/W	RESETB	1	
SWILIMB	22	R/W	RESETB	0	Switcher current limit disable
Reserved	23	R		0	For future use

Notes

97. SWxMODE[3:0] bits will be reset to their default values by the startup sequencer based on PUMS settings. An enabled switcher will default to PWM mode (no pulse skipping) for both Normal and Standby operation.

Table 141. Register 29, Switchers 5

Name	Bit #	R/W	Reset	Default	Description
SW3MODE0	0	R/W	RESETB	0	SW3 operating mode
SW3MODE1	1	R/W	RESETB	1	
SW3MODE2	2	R/W	RESETB	0	
SW3MODE3	3	R/W	RESETB	1	
SW3MHMODE	4	R/W	OFFB	0	SW3 Memory Hold mode
SW3UOMODE	5	R/W	OFFB	0	SW3 User Off mode

Table 141. Register 29, Switchers 5

Name	Bit #	R/W	Reset	Default	Description
Unused	6	R		0	Not available
Unused	7	R		0	
SW4MODE0	8	R/W	RESETB	0	SW4 operating mode
SW4MODE1	9	R/W	RESETB	1	
SW4MODE2	10	R/W	RESETB	0	
SW4MODE3	11	R/W	RESETB	1	
SW4MHMODE	12	R/W	OFFB	0	SW4 Memory Hold mode
SW4UOMODE	13	R/W	OFFB	0	SW4 User Off mode
Unused	14	R		0	Not available
Unused	15	R		0	
Unused	16	R		0	
Unused	17	R		0	
Unused	18	R		0	
Unused	19	R		0	
SWBSTEN	20	R/W	NONE	*	SWBST enable
Unused	21	R		0	Not available
Unused	22	R		0	
Unused	23	R		0	

Notes

98. SWxMODE[3:0] bits will be reset to their default values by the startup sequencer based on PUMS settings. An enabled switcher will default to PWM mode (no pulse skipping) for both Normal and Standby operation.

Table 142. Register 30, Regulator Setting 0

Name	Bit #	R/W	Reset	Default	Description
VGEN10	0	R/W	RESETB	0	VGEN1 setting
VGEN11	1	R/W	RESETB	0	
Unused	2	R		0	Not available
Unused	3	R		0	
VDIG0	4	R/W	NONE	*	VDIG setting
VDIG1	5	R/W	NONE	*	
VGEN20	6	R/W	NONE	*	VGEN2 setting
VGEN21	7	R/W	NONE	*	
VGEN22	8	R/W	NONE	*	
VPLL0	9	R/W	NONE	*	VPLL setting
VPLL1	10	R/W	NONE	*	
VUSB20	11	R/W	NONE	*	VUSB2 setting
VUSB21	12	R/W	NONE	*	
Unused	13	R		0	Not available
VGEN3	14	R/W	RESETB	1	VGEN3 setting
Unused	15	R		0	Not available
VCAM0	16	R/W	RESETB	0	VCAM setting
VCAM1	17	R/W	RESETB	1	
Spare	18	R/W	RESETB	0	For future use
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 143. Register 31, Regulator Setting 1

Name	Bit #	R/W	Reset	Default	Description
Reserved	0	R		0	For future use
Reserved	1	R		0	
VVIDEO0	2	R/W	RESETB	0	VVIDEO setting
VVIDEO1	3	R/W	RESETB	1	
VAUDIO0	4	R/W	RESETB	1	VAUDIO setting
VAUDIO1	5	R/W	RESETB	0	
VSD10	6	R/W	RESETB	1	VSD setting
VSD11	7	R/W	RESETB	1	
VSD12	8	R/W	RESETB	1	
Unused	9	R		0	Not available
Unused	10	R		0	
Unused	11	R		0	
Unused	12	R		0	
Unused	13	R		0	
Unused	14	R		0	
Unused	15	R		0	
Unused	16	R		0	
Unused	17	R		0	
Unused	18	R		0	
Unused	19	R		0	
Unused	20	R		0	
Unused	21	R		0	
Unused	22	R		0	
Unused	23	R		0	

Table 144. Register 32, Regulator Mode 0

Name	Bit #	R/W	Reset	Default	Description
VGEN1EN	0	R/W	RESETB	0	VGEN1 enable
VGEN1STBY	1	R/W	RESETB	0	VGEN1 controlled by standby
VGEN1MODE	2	R/W	RESETB	0	VGEN1 operating mode
VIOHIEN	3	R/W	NONE	*	VIOHI enable
VIOHISTBY	4	R/W	RESETB	0	VIOHI controlled by standby
Spare	5	R/W	RESETB	0	For future use
Unused	6	R		0	Not available
Unused	7	R		0	Not available
Unused	8	R		0	Not available
VDIGEN	9	R/W	NONE	*	VDIG enable
VDIGSTBY	10	R/W	RESETB	0	VDIG controlled by standby
Spare	11	R/W	RESETB	0	For future use
VGEN2EN	12	R/W	NONE	*	VGEN2 enable
VGEN2STBY	13	R/W	RESETB	0	VGEN2 controlled by standby
VGEN2MODE	14	R/W	RESETB	0	VGEN2 operating mode
VPLLEN	15	R/W	NONE	*	VPLL enable
VPLLSTBY	16	R/W	RESETB	0	VPLL controlled by standby
Spare	17	R/W	RESETB	0	For future use
VUSB2EN	18	R/W	RESETB	0	VUSB2 enable
VUSB2STBY	19	R/W	RESETB	0	VUSB2 controlled by standby
Spare	20	R/W	RESETB	0	For future use

Table 144. Register 32, Regulator Mode 0

Name	Bit #	R/W	Reset	Default	Description
Unused	21	R		0	Not available
Unused	22	R		0	
Unused	23	R		0	

Table 145. Register 33, Regulator Mode 1

Name	Bit #	R/W	Reset	Default	Description
VGEN3EN	0	R/W	RESETB	0	VGEN3 enable
VGEN3STBY	1	R/W	RESETB	0	VGEN3controlled by standby
VGEN3MODE	2	R/W	RESETB	0	VGEN3 operating mode
VGEN3CONFIG	3	R/W	RESETB	0	VGEN3 with external PNP
Reserved	4	R		0	For future use
Spare	5	R/W	RESETB	0	For future use
VCAMEN	6	R/W	RESETB	0	VCAM enable
VCAMSTBY	7	R/W	RESETB	0	VCAM controlled by standby
VCAMMODE	8	R/W	RESETB	0	VCAM operating mode
VCAMCONFIG	9	R/W	RESETB	0	VCAM with external PNP
Unused	10	R		0	Not available
Reserved	11	R		0	For future use
VVIDEOEN	12	R/W	RESETB	0	VVIDEO enable
VIDEOSTBY	13	R/W	RESETB	0	VVIDEO controlled by standby
VVIDEOMODE	14	R/W	RESETB	0	VVIDEO operating mode
VAUDIOEN	15	R/W	RESETB	0	VAUDIO enable
VAUDIOSTBY	16	R/W	RESETB	0	VAUDIO controlled by standby
Spare	17	R/W	RESETB	0	For future use
VSDEN	18	R/W	RESETB	0	VSD enable
VSDSTBY	19	R/W	RESETB	0	VSD controlled by standby
VSDMODE	20	R/W	RESETB	0	VSD operating mode
Unused	21	R		0	Not available
Unused	22	R		0	
Unused	23	R		0	

Table 146. Register 34, Power Miscellaneous

Name	Bit #	R/W	Reset	Default	Description
REGSCPEN	0	R/W	RESETB	0	Regulator short circuit protection enable
Unused	1	R		0	Not available
Unused	2	R		0	
Unused	3	R		0	
Unused	4	R		0	
Unused	5	R		0	
GPO1EN	6	R/W	RESETB	0	GPO1 enable
GPO1STBY	7	R/W	RESETB	0	GPO1 controlled by standby
GPO2EN	8	R/W	RESETB	0	GPO2 enable
GPO2STBY	9	R/W	RESETB	0	GPO2 controlled by standby
GPO3EN	10	R/W	RESETB	0	GPO3 enable
GPO3STBY	11	R/W	RESETB	0	GPO3 controlled by standby
GPO4EN	12	R/W	RESETB	0	GPO4 enable
GPO4STBY	13	R/W	RESETB	0	GPO4 controlled by standby
Unused	14	R		0	Not available

Table 146. Register 34, Power Miscellaneous

Name	Bit #	R/W	Reset	Default	Description
PWGT1SPIEN	15	R/W	RESETB	1	Power Gate 1 enable
PWGT2SPIEN	16	R/W	RESETB	1	Power Gate 2 enable
Spare	17	R/W	RESETB	0	For future use
Unused	18	R		0	Not available
Unused	19	R		0	
Unused	20	R		0	
GPO4ADIN	21	R/W	RESETB	1	GPO4 configured as ADC input (GPO drive tri-stated)
Unused	22	R		0	Not available
Unused	23	R		0	

Table 147. Register 35, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 148. Register 36, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 149. Register 37, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 150. Register 38, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 151. Register 39, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 152. Register 40, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 153. Register 41, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 154. Register 42, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 155. Register 43, ADC 0

Name	Bit #	R/W	Reset	Default	Description
LICELLCON	0	R/W	RESETB	0	Enables lithium cell reading
CHRGICON	1	R/W	RESETB	0	Enables charge current reading
BATICON	2	R/W	RESETB	0	Enables battery current reading
BUFFEN	3	R/W	RESETB	0	Input buffer enable
ADIN7SEL0	4	R/W	RESETB	0	GP ADC Channel 7 mux selection 0
ADIN7SEL1	5	R/W	RESETB	0	GP ADC Channel 7 mux selection 1
Unused	6	R		0	Not available
Unused	7	R		0	
ADRESET	8	RWM	RESETB	0	Reset GP ADC system
ADIN7DIV	9	R/W	RESETB	0	Divide by 2 enable for ADIN7
TSREFEN	10	R/W	RESETB	0	Enables the touch screen reference
Reserved	11	R		0	For future use
TSMOD0	12	R/W	RESETB	0	Sets the touch screen interface mode
TSMOD1	13	R/W	RESETB	0	
TSMOD2	14	R/W	RESETB	0	
CHRGRAWDIV	15	R/W	RESETB	1	Sets CHRGRAW scaling to divide by 5
ADINC1	16	R/W	RESETB	0	Auto increment for ADA1
ADINC2	17	R/W	RESETB	0	Auto increment for ADA2
Unused	18	R		0	Not available
Spare	19	R/W	RESETB	0	For future use
Unused	20	R		0	Not available
Unused	21	R		0	
Unused	22	R		0	
ADCBIS0	23	W		0	Access to the ADCBIS control

Table 156. Register 44, ADC 1

Name	Bit #	R/W	Reset	Default	Description
ADEN	0	R/W	RESETB	0	Enables the ADC
RAND	1	R/W	RESETB	0	Sets the single channel mode
ADCCAL	2	RWM	RESETB	0	ADC Calibration
ADSEL	3	R/W	RESETB	0	Selects the set of inputs
TRIGMASK	4	R/W	RESETB	0	Trigger event masking
ADA10	5	R/W	RESETB	0	Channel selection 1
ADA11	6	R/W	RESETB	0	
ADA12	7	R/W	RESETB	0	
ADA20	8	R/W	RESETB	0	Channel selection 2
ADA21	9	R/W	RESETB	0	
ADA22	10	R/W	RESETB	0	
ATO0	11	R/W	RESETB	0	Delay before first conversion
ATO1	12	R/W	RESETB	0	
ATO2	13	R/W	RESETB	0	
ATO3	14	R/W	RESETB	0	
ATO4	15	R/W	RESETB	0	
ATO5	16	R/W	RESETB	0	
ATO6	17	R/W	RESETB	0	
ATO7	18	R/W	RESETB	0	
ATOX	19	R/W	RESETB	0	Sets ATO delay for any conversion
ASC	20	RWM	RESETB	0	Starts conversion
ADTRIGIGN	21	R/W	RESETB	0	Ignores the ADTRIG input

Table 156. Register 44, ADC 1

Name	Bit #	R/W	Reset	Default	Description
ADONESHOT	22	R/W	RESETB	0	Single trigger event only
ADCBIS1	23	W	RESETB	0	Access to the ADCBIS control

Table 157. Register 45, ADC 2

Name	Bit #	R/W	Reset	Default	Description
Spare	0	R	NONE	0	For 12-bit use
Spare	1	R	NONE	0	
ADD10	2	R	NONE	0	Results for channel selection 1
ADD11	3	R	NONE	0	
ADD12	4	R	NONE	0	
ADD13	5	R	NONE	0	
ADD14	6	R	NONE	0	
ADD15	7	R	NONE	0	
ADD16	8	R	NONE	0	
ADD17	9	R	NONE	0	
ADD18	10	R	NONE	0	
ADD19	11	R	NONE	0	
Spare	12	R	NONE	0	For 12-bit use
Spare	13	R	NONE	0	
ADD20	14	R	NONE	0	Results for channel selection 2
ADD21	15	R	NONE	0	
ADD22	16	R	NONE	0	
ADD23	17	R	NONE	0	
ADD24	18	R	NONE	0	
ADD25	19	R	NONE	0	
ADD26	20	R	NONE	0	
ADD27	21	R	NONE	0	
ADD28	22	R	NONE	0	
ADD29	23	R	NONE	0	

Table 158. Register 46, ADC 3

Name	Bit #	R/W	Reset	Default	Description
Unused	0	R		0	Not available
Unused	1	R		0	
Unused	2	R		0	
Unused	3	R		0	
Unused	4	R		0	
Unused	5	R		0	
ICID0	6	R	NONE	1	Generation ID
ICID1	7	R	NONE	1	
ICID2	8	R	NONE	1	

Table 158. Register 46, ADC 3

Name	Bit #	R/W	Reset	Default	Description
Unused	9	R		0	Not available
Unused	10	R		0	
Unused	11	R		0	
Unused	12	R		0	
Unused	13	R		0	
Unused	14	R		0	
Unused	15	R		0	
Unused	16	R		0	
Unused	17	R		0	
Unused	18	R		0	
Unused	19	R		0	
Unused	20	R		0	
Unused	21	R		0	
Unused	22	R		0	
Reserved	23	R		0	For future use

Table 159. Register 47, ADC 4

Name	Bit #	R/W	Reset	Default	Description
Spare	0	R	NONE	0	For 12-bit use
Spare	1	R	NONE	0	
ADDBIS10	2	R	NONE	0	Result for channel selection 1 of ADCBIS
ADDBIS11	3	R	NONE	0	
ADDBIS12	4	R	NONE	0	
ADDBIS13	5	R	NONE	0	
ADDBIS14	6	R	NONE	0	
ADDBIS15	7	R	NONE	0	
ADDBIS16	8	R	NONE	0	
ADDBIS17	9	R	NONE	0	
ADDBIS18	10	R	NONE	0	
ADDBIS19	11	R	NONE	0	
Spare	12	R	NONE	0	For 12-bit use
Spare	13	R	NONE	0	
ADDBIS20	14	R	NONE	0	Result for channel selection 2 of ADCBIS
ADDBIS21	15	R	NONE	0	
ADDBIS22	16	R	NONE	0	
ADDBIS23	17	R	NONE	0	
ADDBIS24	18	R	NONE	0	
ADDBIS25	19	R	NONE	0	
ADDBIS26	20	R	NONE	0	
ADDBIS27	21	R	NONE	0	
ADDBIS28	22	R	NONE	0	
ADDBIS29	23	R	NONE	0	

Table 160. Register 48, Charger 0

Name	Bit #	R/W	Reset	Default	Description
VCHRG0	0	R/W	RESETB	1	Sets the charge regulator output voltage
VCHRG1	1	R/W	RESETB	1	
VCHRG2	2	R/W	RESETB	0	
ICHRG0	3	RWM	RESETB	0	Sets the main charger DAC current
ICHRG1	4	RWM	RESETB	0	
ICHRG2	5	RWM	RESETB	0	
ICHRG3	6	RWM	RESETB	0	
TREN	7	R/W	RESETB	0	Enables the internal trickle charger current
ACKLPB	8	R/W	RESETB	0	Acknowledge Low-power Boot
THCHKB	9	R/W	RESETB	0	Battery thermistor check disable
FETOVRD	10	R/W	RESETB	0	Allows BATTFET Control
FETCTRL	11	R/W	RESETB	0	BATTFET Control
Spare	12	R/W	RESETB	0	For future use
RVRSMODE	13	RWM	RESETB	0	Reverse mode enable
Unused	14	R		0	Not available
PLIM0	15	R/W	RESETB	0	Power limiter setting
PLIM1	16	R/W	RESETB	0	
PLIMDIS	17	R/W	RESETB	0	Power limiter disable
CHRGLEDEN	18	R/W	RESETB	0	CHRGLED enable
CHGTMRRST	19	RWM	RESETB	0	Charge timer reset
CHGRESTART	20	RWM	RESETB	0	Restarts charger state machine
CHGAUTOB	21	R/W	RESETB	0	Avoids automatic charging while on
CYCLB	22	R/W	RESETB	1	Disables cycling
CHGAUTOVIB	23	R/W	RESETB	0	Allows V and I programming

Table 161. Register 49, USB 0

Name	Bit #	R/W	Reset	Default	Description
Reserved	0	R		0	For future use
Reserved	1	R		0	
Reserved	2	R		0	
Reserved	3	R		0	
Reserved	4	R		0	
Reserved	5	R		0	
Spare	6	R/W	RESETB	1	
Reserved	7	R		0	
Reserved	8	R		0	For future use
Reserved	9	R		0	
Reserved	10	R		0	
Reserved	11	R		0	
Reserved	12	R		0	
Reserved	13	R		0	
Reserved	14	R		0	
Reserved	15	R		0	
Reserved	16	R		0	
Unused	17	R		0	Not available
Unused	18	R		0	
Reserved	19	R		0	For future use
Reserved	20	R		0	
Reserved	21	R		0	

Table 161. Register 49, USB 0

Name	Bit #	R/W	Reset	Default	Description
IDPUCNTRL	22	R/W	RESETB	0	UID pin pull up source select
Reserved	23	R		0	For future use

Table 162. Register 50, Charger USB 1

Name	Bit #	R/W	Reset	Default	Description
VUSBIN	0	R/W	NONE	*	Slave or Host configuration for VBUS
Unused	1	R		0	Not available
Unused	2	R		0	
VUSBEN	3	R/W	RESETB	1	VUSB enable (PUMS2=Open) Also reset to 1 by invalid VBUS
			NONE	*	VUSB enable (PUMS2=GND)
Unused	4	R		0	Not available
Unused	5	R		0	
Reserved	6	R		0	For future use
Reserved	7	R		0	
ID100KPU	8	R/W	RESETB	0	Switches in 100K UID pull-up
Reserved	9	R		0	For future use
OTGSWBSTEN	10	R/W	RESETB	0	Enable SWBST for USB OTG mode
Reserved	11	R		0	For future use
Reserved	12	R		0	
Reserved	13	R		0	
Unused	14	R		0	Not available
Unused	15	R		0	
Reserved	16	R		0	For future use
Spare	17	R/W	RESETB	0	
Spare	18	R/W	RESETB	0	For future use
Unused	19	R		0	Not available
Unused	20	R		0	
Unused	21	R		0	
Unused	22	R		0	
Unused	23	R		0	

Table 163. Register 51, LED Control 0

Name	Bit #	R/W	Reset	Default	Description
Spare	0	R/W	RESETB	0	For future use
LEDMDHI	1	R/W	RESETB	0	Main display driver high current mode
LEDMDRAMP	2	R/W	RESETB	0	Main display driver ramp enable
LEDMDDC0	3	R/W	RESETB	0	Main display driver duty cycle
LEDMDDC1	4	R/W	RESETB	0	
LEDMDDC2	5	R/W	RESETB	0	
LEDMDDC3	6	R/W	RESETB	0	
LEDMDDC4	7	R/W	RESETB	0	
LEDMDDC5	8	R/W	RESETB	0	
LEDMD0	9	R/W	RESETB	0	Main display driver current setting
LEDMD1	10	R/W	RESETB	0	
LEDMD2	11	R/W	RESETB	0	
Spare	12	R/W	RESETB	0	For future use
LEDADHI	13	R/W	RESETB	0	Auxiliary display driver high current mode
LEDADRAMP	14	R/W	RESETB	0	Auxiliary display driver ramp enable

Table 163. Register 51, LED Control 0

Name	Bit #	R/W	Reset	Default	Description
LEDADDC0	15	R/W	RESETB	0	Auxiliary display driver duty cycle
LEDADDC1	16	R/W	RESETB	0	
LEDADDC2	17	R/W	RESETB	0	
LEDADDC3	18	R/W	RESETB	0	
LEDADDC4	19	R/W	RESETB	0	
LEDADDC5	20	R/W	RESETB	0	
LEDAD0	21	R/W	RESETB	0	Auxiliary display driver current setting
LEDAD1	22	R/W	RESETB	0	
LEDAD2	23	R/W	RESETB	0	

Table 164. Register 52, LED Control 1

Name	Bit #	R/W	Reset	Default	Description
Spare	0	R/W	RESETB	0	For future use
LEDKPHI	1	R/W	RESETB	0	Keypad driver high current mode
LEDKPRAMP	2	R/W	RESETB	0	Keypad driver ramp enable
LEDKPDC0	3	R/W	RESETB	0	Keypad driver duty cycle
LEDKPDC1	4	R/W	RESETB	0	
LEDKPDC2	5	R/W	RESETB	0	
LEDKPDC3	6	R/W	RESETB	0	
LEDKPDC4	7	R/W	RESETB	0	
LEDKPDC5	8	R/W	RESETB	0	
LEDKP0	9	R/W	RESETB	0	Keypad driver current setting
LEDKP1	10	R/W	RESETB	0	
LEDKP2	11	R/W	RESETB	0	
Spare	12	R/W	RESETB	0	For future use
Spare	13	R/W	RESETB	0	
Spare	14	R/W	RESETB	0	
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	
Unused	18	R		0	
Unused	19	R		0	
Unused	20	R		0	
Unused	21	R		0	
Unused	22	R		0	
Unused	23	R		0	

Table 165. Register 53, LED Control 2

Name	Bit #	R/W	Reset	Default	Description
LEDRPER0	0	R/W	RESETB	0	Red channel blink period
LEDRPER1	1	R/W	RESETB	0	
LEDRRAMP	2	R/W	RESETB	0	Red channel driver ramp enable
LEDRDC0	3	R/W	RESETB	0	Red channel driver duty cycle
LEDRDC1	4	R/W	RESETB	0	
LEDRDC2	5	R/W	RESETB	0	
LEDRDC3	6	R/W	RESETB	0	
LEDRDC4	7	R/W	RESETB	0	
LEDRDC5	8	R/W	RESETB	0	

Table 165. Register 53, LED Control 2

Name	Bit #	R/W	Reset	Default	Description
LEDR0	9	R/W	RESETB	0	Red channel driver current setting
LEDR1	10	R/W	RESETB	0	
LEDR2	11	R/W	RESETB	0	
LEDGPER0	12	R/W	RESETB	0	Green channel blink period
LEDGPER1	13	R/W	RESETB	0	
LEDGRAMP	14	R/W	RESETB	0	Green channel driver ramp enable
LEDGDC0	15	R/W	RESETB	0	Green channel driver duty cycle
LEDGDC1	16	R/W	RESETB	0	
LEDGDC2	17	R/W	RESETB	0	
LEDGDC3	18	R/W	RESETB	0	
LEDGDC4	19	R/W	RESETB	0	
LEDGDC5	20	R/W	RESETB	0	
LEDG0	21	R/W	RESETB	0	Green channel driver current setting
LEDG1	22	R/W	RESETB	0	
LEDG2	23	R/W	RESETB	0	

Table 166. Register 54, LED Control 3

Name	Bit #	R/W	Reset	Default	Description
LEDBPER0	0	R/W	RESETB	0	Blue channel blink period
LEDBPER1	1	R/W	RESETB	0	
LEDBRAMP	2	R/W	RESETB	0	Blue channel driver ramp enable
LEDBDC0	3	R/W	RESETB	0	Blue channel driver duty cycle
LEDBDC1	4	R/W	RESETB	0	
LEDBDC2	5	R/W	RESETB	0	
LEDBDC3	6	R/W	RESETB	0	
LEDBDC4	7	R/W	RESETB	0	
LEDBDC5	8	R/W	RESETB	0	
LEDB0	9	R/W	RESETB	0	Blue channel driver current setting
LEDB1	10	R/W	RESETB	0	
LEDB2	11	R/W	RESETB	0	
LEDSWBSTEN	12	R/W	RESETB	0	Enable SWBST for RGB LED's
Spare	13	R/W	RESETB	0	For future use
Spare	14	R/W	RESETB	0	
Unused	15	R		0	Not available
Unused	16	R		0	
Unused	17	R		0	
Unused	18	R		0	
Unused	19	R		0	
Unused	20	R		0	
Unused	21	R		0	
Unused	22	R		0	
Unused	23	R		0	

Table 167. Register 55, Not Used

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 168. Register 56, Not Used

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0	Not available

Table 169. Register 57, FSL Use Only

Name	Bit #	R/W	Reset	Default	Description
FSL Use Only	23-0	R/W	RTCPORB	FSL	

Table 170. Register 58, FSL Use Only

Name	Bit #	R/W	Reset	Default	Description
FSL Use Only	23-0	R/W	RTCPORB	FSL	

Table 171. Register 59, FSL Use Only

Name	Bit #	R/W	Reset	Default	Description
FSL Use Only	23-0	R/W	RTCPORB	FSL	

Table 172. Register 60, FSL Use Only

Name	Bit #	R/W	Reset	Default	Description
FSL Use Only	23-0	R/W	RTCPORB	FSL	

Table 173. Register 61, FSL Use Only

Name	Bit #	R/W	Reset	Default	Description
FSL Use Only	23:0	R/W	RTCPORB	FSL	

Table 174. Register 62, FSL Use Only

Name	Bit #	R/W	Reset	Default	Description
FSL Use Only	23:0	R/W	RTCPORB	FSL	

Table 175. Register 63, FSL Use Only

Name	Bit #	R/W	Reset	Default	Description
FSL Use Only	23:0	R/W	RTCPORB	FSL	

TYPICAL APPLICATIONS

Figure 35 contains a typical application of the MC13892. For convenience, components for use with the MC13892 are cited within this document. Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

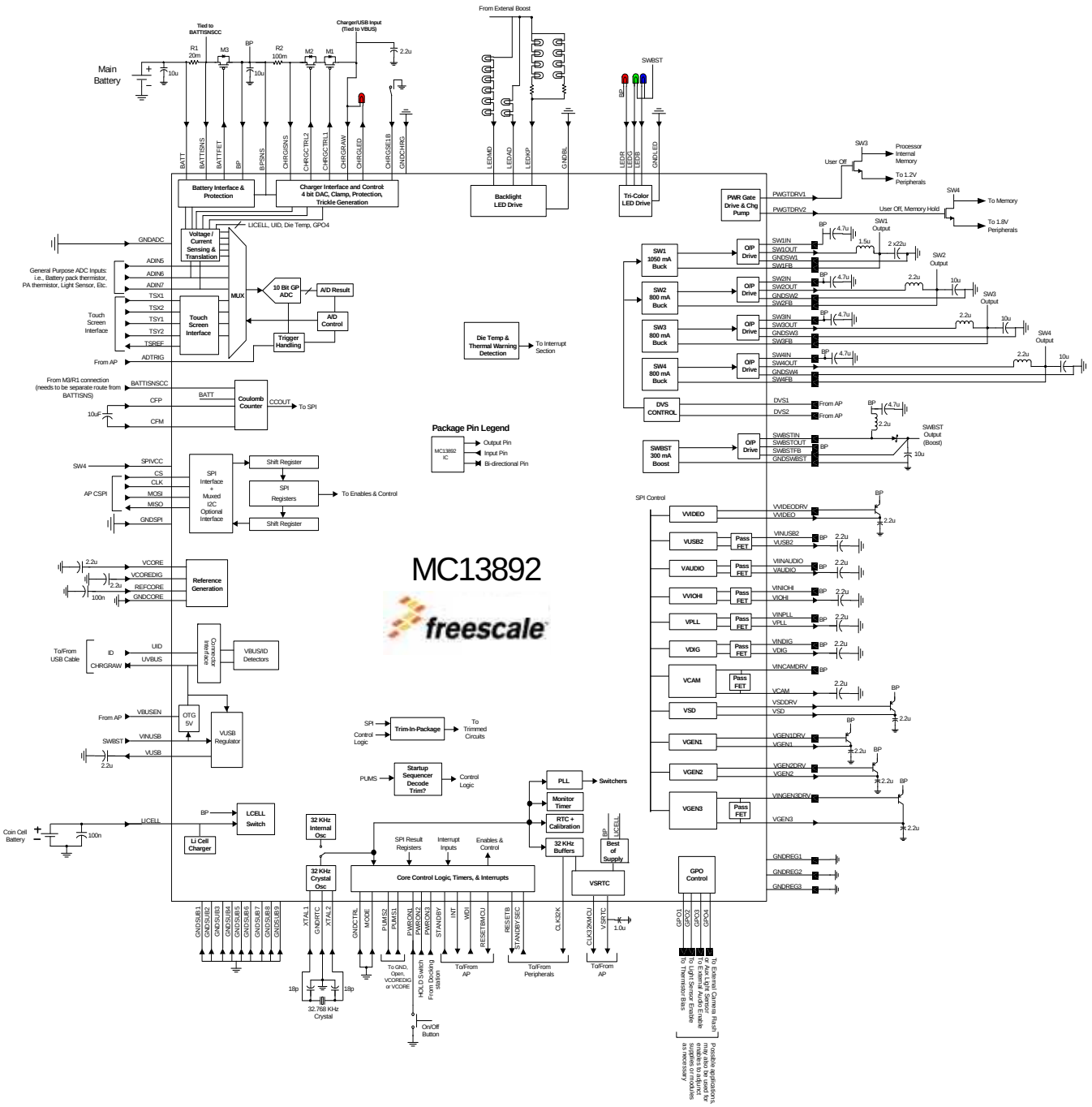
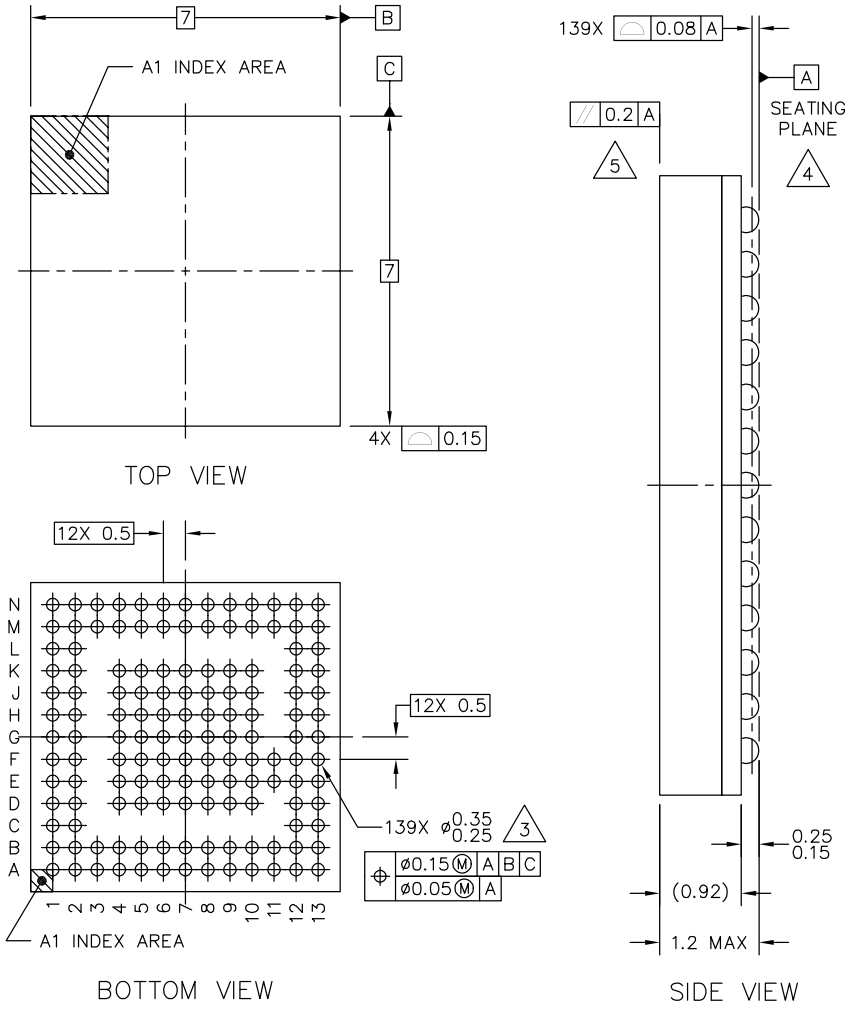


Figure 35. MC13892 Typical Application

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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TITLE: PBGA, THIN PROFILE, FINE PITCH, 139 I/O, 7 X 7 PKG, 0.5 MM PITCH (MAP)	DOCUMENT NO: 98ASA10820D	REV: O
	CASE NUMBER: 2007–01	30 JAN 2008
	STANDARD: MO–195–AD	

VK SUFFIX
139-PIN
98ASA10820D
REVISION 0

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PBGA, THIN PROFILE, FINE PITCH, 139 I/O, 7 X 7 PKG, 0.5 MM PITCH (MAP)	DOCUMENT NO: 98ASA10820D	REV: O
	CASE NUMBER: 2007–01	30 JAN 2008
	STANDARD: MO–195–AD	

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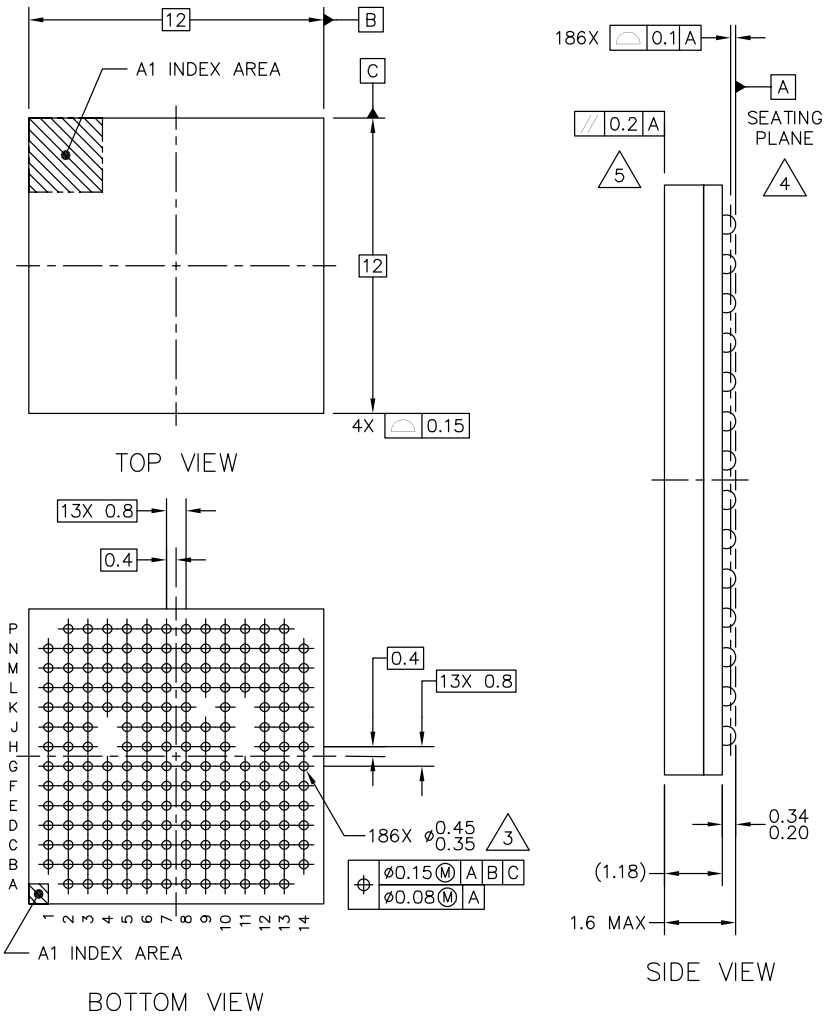

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TITLE: PBGA, LOW PROFILE, FINE PITCH, 186 I/O, 12 X 12 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA10849D	REV: O	
	CASE NUMBER: 2044–01	11 JUL 2008	
	STANDARD: NON–JEDEC		

VL SUFFIX
186-PIN
98ASA10849D
REVISION 0

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
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MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PBGA, LOW PROFILE, FINE PITCH, 186 I/O, 12 X 12 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA10849D	REV: O
	CASE NUMBER: 2044–01	11 JUL 2008
	STANDARD: NON–JEDEC	

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ADDITIONAL DOCUMENTATION

Table 176. Additional Documentation

Document Number	Description
MC13892ER	MC13892ER, Silicon Mask Errata
MC13783	MC13783, Power Management and Audio Circuit

REVISION HISTORY

REVISION	DATE	DESCRIPTION
14.0	11/2011	• Added MC13892CJVK and MC13892CJVL to the ordering information • Changed RT from 45k to 4.5 k in Table 73 for T_{HIGH} • In the Static Electrical Characteristics table, changed Input Operating Voltage - CHRGRAW from 17 V to 5.6 V on page 24. • Changed Input Operating Voltage - CHRGRAW from 17V to 5.6 V in Table 64.
15.0	4/2012	• Added MC13892DJVK and MC13892DJVL to Table 1, MC13892 Device Variations.
16.0	4/2012	• Corrected Global Reset Functions in Table 1
17.0	5/2012	• Clarified the Global Reset function for silicon versions A, B, C and D throughout the document • Section PWRON1, 2 and 3 on page 37 • Section Global System Restart on page 60 • Table 125. Register 13, Power Control 0

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05/2012